MICROCLOCK

MK1417
S3 Notebook Clock Source

Description

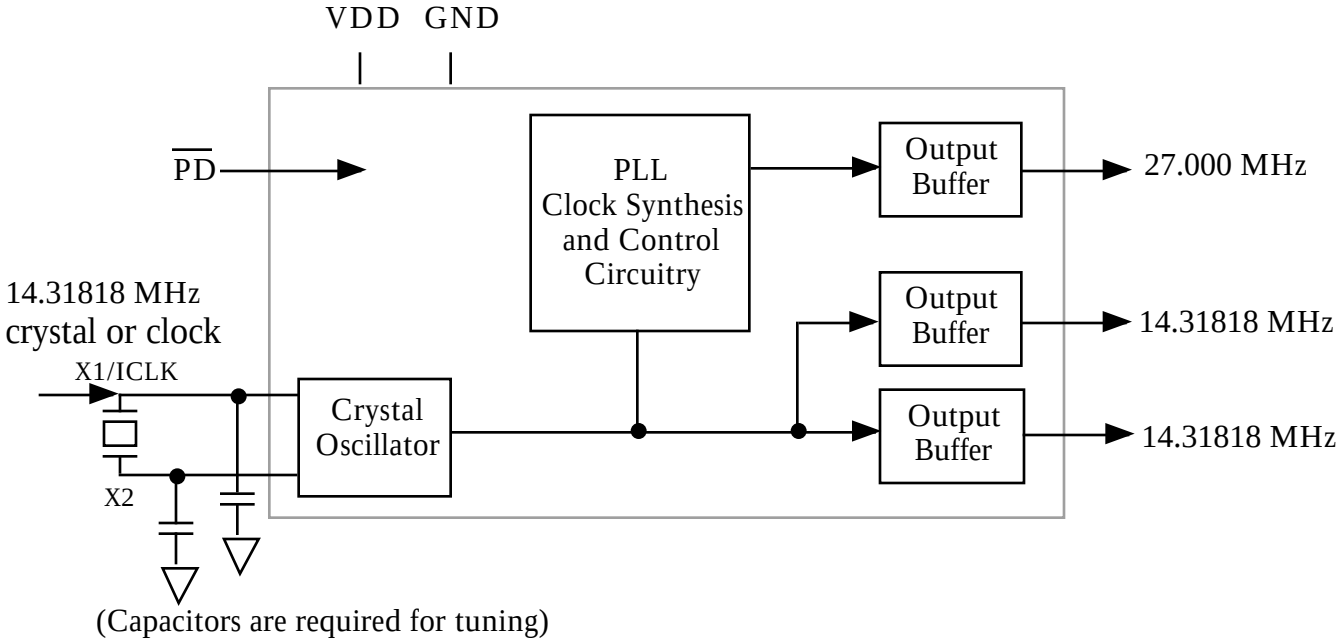
The MK1417 is an ideal way to generate clocks for S3's M5 processor. The chip is a cost reduction to the MK1416, maintaining the functionality of the MK1416, but with a different pinout. In an 8 pin SOIC, the chip saves cost over separate surface mount oscillators and increases reliability by eliminating mechanical (quartz-based) devices from the board. The power down pin turns off the device, drawing less than 30µA.

MicroClock offers many other clocks for computers and computer peripherals. Consult MicroClock when you need to remove crystals and oscillators from your board.

Features

- Packaged in 8 pin SOIC
- Functional, lower cost replacement of MK1416
- Differences from MK1416
  - no on-chip crystal capacitors
  - pinout is different
- Ideal for S3's M5 processor
- Input clock frequency of 14.31818 MHz
- Dual buffered 14.318 MHz clock outputs
- Output clock frequency of 27.0MHz
- Power down turns off chip
- Low jitter
- 25mA drive capability at TTL levels
- 3.3V or 5V supply voltage
- Advanced, low power CMOS process
- Insensitive to input clock duty cycle

Block Diagram



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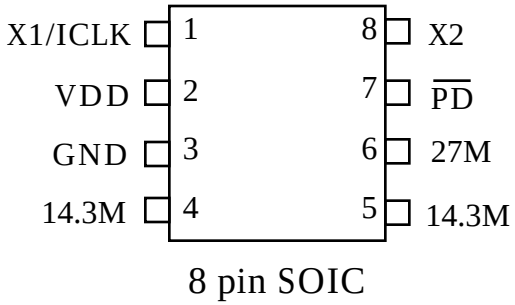
Pin Assignment



8 pin SOIC

$\overline{PD}$	All Clocks
0	LOW
1	ON

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal Connection. Connnect to a 14.31818 MHz crystal or clock.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	14.3M	O	14.31818 MHz buffered crystal clock output.
5	14.3M	O	14.31818 MHz buffered crystal clock output.
6	27M	O	27.00 MHz clock output.
7	$\overline{PD}$	I	Power Down input. Logic 0 takes all clocks low. Internal pullup.
8	X2	O	Crystal Connection for a 14.31818 MHz crystal, or leave unconnected for clock input.

Key: I = Input, O = output, P = power supply connection

External Components/Crystal Selection

A minimum number of external components are required for proper operation. For a crystal input, a parallel resonant 14.31818 MHz crystal is recommended. The frequency tolerance of the crystal should be ±30 ppm maximum. For tuning with a given crystal C_L, the formula $2•(C_L-6)$ gives the value of each capacitor that should be connected from X1 to GND and X2 to GND. For a clock input, connect to X1 and leave X2 unconnected. A decoupling capacitor of 0.1µF should be connected between VDD and GND on pins 2 and 3, and a 33Ω terminating resistor can be used on each clock output if the trace is longer than 1 inch.

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+.5V	V
Clock Outputs	Referenced to GND	-0.5		VDD+.5V	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (at 5.0V unless otherwise noted)					
Operating Voltage, VDD		3.0		5.5	V
Input High Voltage, VIH, input clock only		3.5	2.5		V
Input Low Voltage, VIL, input clock only			2.5	1.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Operating Supply Current, IDD, 5.0V	No Load		14		mA
Operating Supply Current, IDD, 3.3V	No Load		8		mA
Power Down Supply Current, IDDPD, 5V	No Load		25		µA
Input Capacitance	$\overline{PD}$ pin		7		pF
AC CHARACTERISTICS (at 5.0V unless otherwise noted)					
Input Clock			14.31818		MHz
Power up time, from power down to clocks stable	$\overline{PD}$ low to high		4	10	ms
Input Clock Duty Cycle	Time above 2.5V	20		80	%
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	Time above 1.5V	45	50	55	%
Absolute Maximum Clock Period Jitter	Variation from mean		130		ps
One Sigma Clock Period Jitter			40		ps

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Typical values are at 25°C.

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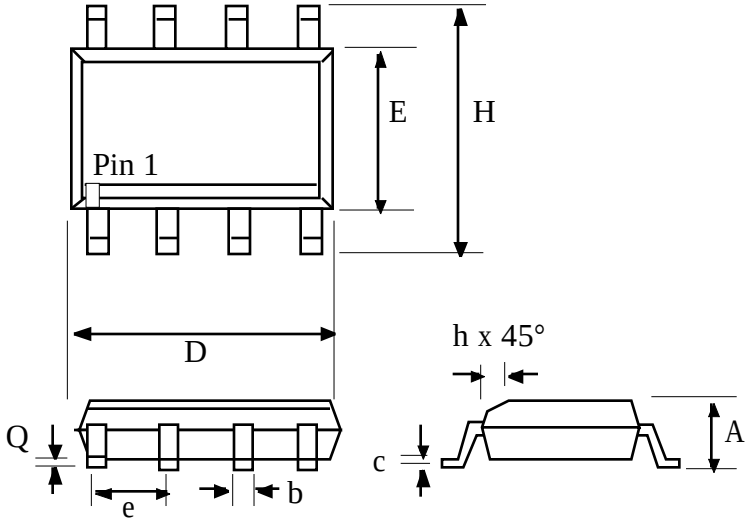
Package Outline and Package Dimensions

8 pin SOIC



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK1417S	MK1417S	8 pin SOIC	0-70°C
MK1417STR	MK1417S	Add tape and reel	0-70°C