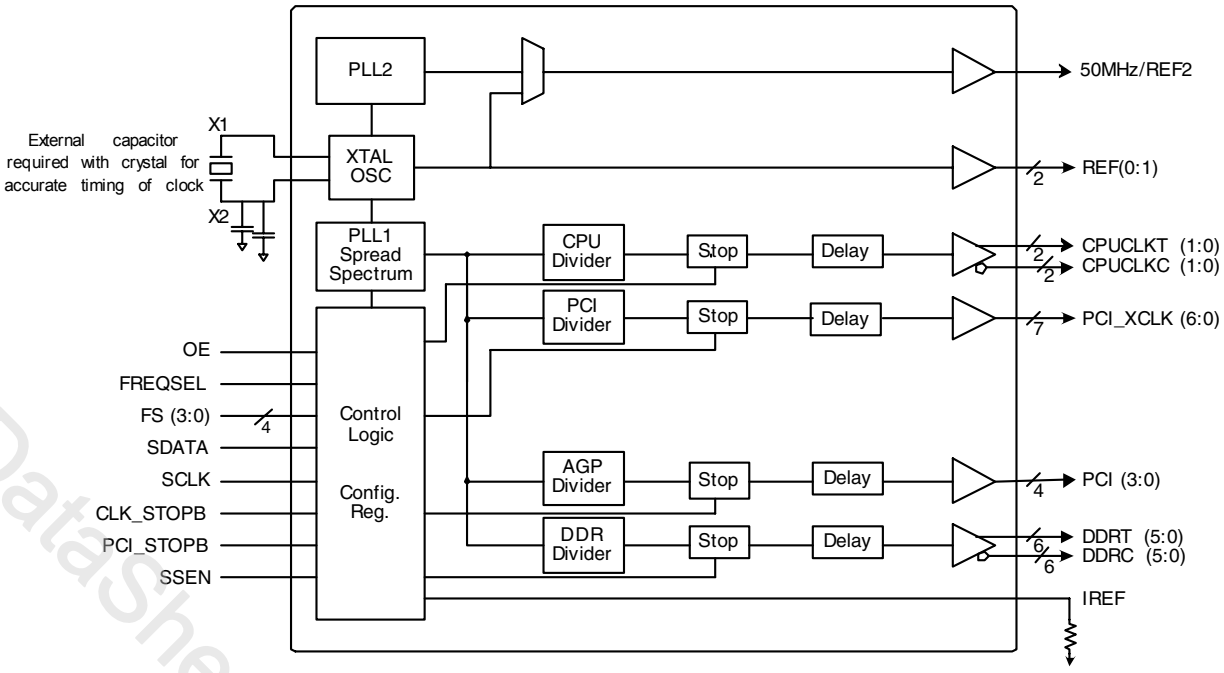
## Description

The MK1493-02A is a general purpose clock generator that provides an integrated clocking solution for PCI/Networking applications. It provides two pairs of differential CPU clocks, four PCI clocks, seven PCI_X clocks, two reference clocks, additional clock selectable from REF/50 MHz, and six pairs of SSTL2 DDR at 2.5 V. **All complementary outputs operate only from a 2.5 V power supply.**

## Input/Output Features

- Packaged in 56-pin TSSOP package
- 2 - Pairs of differential CPU clocks (differential current mode)
- 4 - PCI @ 3.3 V
- 7 - PCI_X @ 3.3 V
- 2 - REF @ 3.3 V, Fixed
- 6 - Pairs of differential SSTL2 DDR @ 2.5 V
- 1 - REF/50 MHz, selectable
- Spread spectrum for EMI control
- Supports SMBUS index read/write and blocks read/write operations
- Uses external 25 or 50 MHz crystal or clock
- CPU output jitter <125 ps
- PCI cycle to cycle output jitter <250 ps
- DDR cycle to cycle output jitter <150 ps

## Block Diagram



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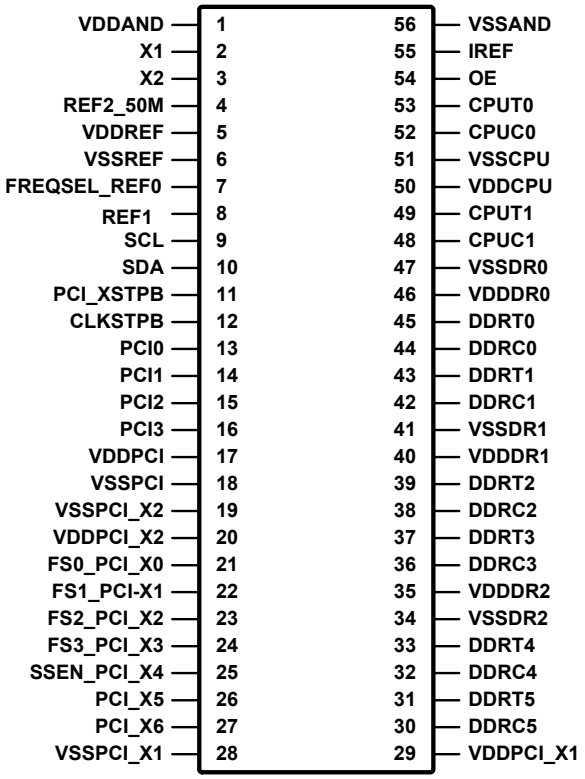
## Pin Assignment




**56 pin 240mil 0.50 mm pitch TSSOP**

## Functionality Table

| $F_{IN}$ MHz | FS3 | FS2 | FS1 | FS0 | CPUCLK MHz | DDR MHz | PCI MHz | PCI_X MHz |
|---|---|---|---|---|---|---|---|---|
| 50 | 0 | 1 | 0 | 0 | 33 | 33 | 33 | 33 |
| 50 | 0 | 1 | 0 | 1 | 100 | 133 | 33 | 33 |
| 25 | 0 | 1 | 1 | 0 | 33 | 33 | 33 | 33 |
| 25 | 0 | 1 | 1 | 1 | 33 | 33 | 33 | 133 |
| 25[1] | 1 | 0 | 0 | 0 | 100[1] | 200[1] | 66[1] | 33[1] |
| 25 | 1 | 0 | 0 | 1 | 200 | 200 | 66 | 33 |
| 25 | 1 | 0 | 1 | 0 | 133 | 133 | 33 | 66 |
| 25 | 1 | 0 | 1 | 1 | 133 | 133 | 33 | 33 |
| 25 | 1 | 1 | 0 | 0 | 133 | 133 | 66 | 66 |
| 25 | 1 | 1 | 0 | 1 | 150 | 150 | 33 | 33 |
| 25 | 1 | 1 | 1 | 0 | 125 | 125 | 33 | 33 |
| 25 | 1 | 1 | 1 | 1 | 166 | 166 | 33 | 33 |

[1] Default start Output Clock settings,

33M=33.33 MHz, 66M=66.66 MHz, 133M=133.33 MHz.



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## Pin Descriptions

| Pin | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | VDDAND | Power | Analog and digital power supply 3.3 V. |
| 2 | X1/CLK | XI | Crystal connection/input clock. Connect to a 25 MHz fundamental mode crystal. |
| 3 | X2 | XO | Connect to a 25 MHz fundamental mode crystal or leave unconnected if X1 is a |
| 4 | REF2_50M | Output | REF2 or 50 MHz output. |
| 5 | VDDREF | Power | Power supply for REF outputs. |
| 6 | VSSREF | Power | Ground for REF outputs. |
| 7 | FREQSEL_REF0 | I/O | **Input** frequency select input pin for 50 MHz/ REF2 (0=50 MHz select, 1=REF2 select). **Output** - REF0.( Internal Pull up resistor of 120K ohms see for page 21) |
| 8 | REF1 | Output | REF1 clock output. |
| 9 | SCL | I/O | Clock pin for SMBUS circuitry. 5 V tolerant. |
| 10 | SDA | Input | Data pin for SMBUS circuitry. 5 V tolerant. |
| 11 | PCI_XSTPB | Input | Asynchronous input Stops all PCI_XCLK at logic level 0 when pulled low.( Internal pull up resistor 120K) |
| 12 | CUP_STPB | Input | Asynchronous input halts CPU , DDR and PCI clocks at logic O when driven low. S. (Internal pull up resistor 120K see page 21) |
| 13 | PCI0 | Output | PCI Output clock 0. |
| 14 | PCI1 | Output | PCI Output clock 1. |
| 15 | PCI2 | Output | PCI Output clock 2. |
| 16 | PCI3 | Input | PCI Output clock 3. |
| 17 | VDDPCI1 | Power | Power supply for PCI clocks. |
| 18 | VSSPCI1 | Power | Ground supply for PCI clocks. |
| 19 | VSSPCI_X2 | Power | Ground for PCI_X clocks. |
| 20 | VDDPCI_X2 | Power | Power supply for PCI_X clocks. |
| 21 | FS0_PCI_X0 | I/O | FS0 input/PCI_X0 output. (Internal Pull Down resistor 120K , see page 21). |
| 22 | FS1_PCI-X1 | I/O | FS1 input/PCI_X1 output. (Internal Pull Down resistor 120K , see page 21) |
| 23 | FS2_PCI_X2 | I/O | FS2 input/PCI_X2 output. (Internal Pull Down resistor 120K , see page 21). |
| 24 | FS3_PCI_X3 | I/O | FS3 input/PCI_X3 output. (Internal Pull up resistor 120K , see page 21). |
| 25 | SSEN_PCI4 | I/O | Spread spectrum enable (0=SS disabled, 1=enabled). PCI clock output. (Internal pull down resistor 120K see page 21) |
| 26 | PCI_X5 | Output | PCI_X clock output. |
| 27 | PCI_X6 | Output | PCI_X clock output. |
| 28 | VSSPCI_X1 | Power | Ground for PCI clocks. |
| 29 | VDDPCI_X1 | Power | Power supply for PCI clocks. |
| 30 | DDRC5 | Output | Complementary clock output of DDRT5. |
| 31 | DDRT5 | Output | True clock output of DDRT5. |
| 32 | DDRC4 | Output | Complementary clock output of DDRT4. |
| 33 | DDRT4 | Output | True clock output of DDRT4. |
| 34 | VSSDR2 | Power | Ground for DDR clocks. |
| 35 | VDDDR2 | Power | Power supply for DDR clocks (2.5 V only for complementary outputs). |
| 36 | DDRC3 | Output | Complementary clock output of DDRT3. |



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| Pin | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 37 | DDRT3 | Output | True clock output of DDRT3. |
| 38 | DDRC2 | Output | Complementary clock output of DDRT2. |
| 39 | DDRT2 | Output | True clock output of DDRT2. |
| 40 | VDDDR1 | Power | Power supply for DDR clocks 2.5 V only for complementary outputs. (Can use 3.3 V supply for single ended outputs) |
| 41 | VSSDR1 | Power | Ground for DDR clocks. |
| 42 | DDRC1 | Output | Complementary clock output of DDRT1. |
| 43 | DDRT1 | Output | True clock output of DDRT1. |
| 44 | DDRC0 | Output | Complementary clock output of DDRT0. |
| 45 | DDRT0 | Output | True clock output of DDRT0. |
| 46 | VDDDR0 | Power | Power supply for DDR clocks 2.5 V only for complementary outputs). (Can use 3.3 V supply for single ended outputs) |
| 47 | VSSDR0 | Power | Ground for DDR clocks. |
| 48 | CPUC1 | Output | Complementary CPU clock output. |
| 49 | CPUT1 | Output | True CPU clock output. |
| 50 | VDDCPU | Power | Power supply for CPU Clocks 3.3 V. |
| 51 | VSSCPU | Power | Ground for CPU clocks. |
| 52 | CPUC0 | Output | Complementary CPU clock output. |
| 53 | CPUT0 | Output | True CPU clock output. |
| 54 | OE | Input | Enables all outputs when high, tri-state outputs when low. Pull-up. |
| 55 | IREF | Output | A precision resistor connected to ground establishes the external reference current. |
| 56 | VSSAND | Power | Analog and digital ground power supply. |

# General SMBUS Serial Interface Info

# General SM-Bus Serial Interface Information

### How to Write:

- Controller (host) sends a start bit
- Controller (host) sends the write address D2 (H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = **N**
- ICS clock will **acknowledge**
- Controller sends Byte Count **X**
- ICS clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- ICS clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **ICS (Slave/Receiver)** |
| T | starT | | |
| Slave Address D2 (H) | WR | | |
| | | | ACK |
| Beg Location = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O<br>O<br>O | | | |
| | | | O |
| | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP | | |

### How to Read:

- Controller (host) will send a start bit
- Controller (host) sends the write address D2 (H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning Byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a repeat start bit
- Controller (host) sends the read address Byte D3 (H)
- ICS clock will **acknowledge**
- ICS clock will send the data Byte count = X
- ICS clock sends Byte **N**
- ICS clock sends Byte **N+X-1**
- Controller (host) will need to acknowledge each Byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **ICS (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address D2 (H) | WR =0 | | |
| | | | ACK |
| Beginning Loc = N | | | |
| | | | ACK |
| RT | repeat starT | | |
| Slave Address D2 (H) | RD =1 | | |
| | | | ACK |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X BYTES | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | NAK | | |
| P | stoP bit | | |



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## Serial Configuration Command Bitmap Byte 0: Functionary and frequency select register (default = 0)

| Bit | Description | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SSEN | FS3 | FS2 | FS1 | FS0 | CPUCLK (MHz) | DDR (MHz) | PCI (MHz) | PCI_X | F in | DDR Diff Out | Spread Percentage | Power up |
| | Bit2 | Bit7 | Bit6 | Bit5 | Bit4 | | | | | | | | |
| | 0 | 0 | 0 | 0 | 0 | Reserved | | | | | N | N | |
| | 0 | 0 | 0 | 0 | 1 | Reserved | | | | | N | N | |
| | 0 | 0 | 0 | 1 | 0 | Reserved | | | | | N | N | |
| | 0 | 0 | 0 | 1 | 1 | Reserved | | | | | N | N | |
| | 0 | 0 | 1 | 0 | 0 | 33 | 33 | 33 | 33 | 50 | N | N | |
| | 0 | 0 | 1 | 0 | 1 | 100 | 133 | 33 | 33 | 50 | N | N | |
| | 0 | 0 | 1 | 1 | 0 | 33 | 33 | 33 | 33 | 25 | N | N | |
| | 0 | 0 | 1 | 1 | 1 | 33 | 33 | 33 | 133 | 25 | N | N | |
| | 0 | 1 | 0 | 0 | 0 | 100 | 200 | 66 | 33 | 25 | Y | N | Default |
| | 0 | 1 | 0 | 0 | 1 | 200 | 200 | 66 | 33 | 25 | Y | N | |
| | 0 | 1 | 0 | 1 | 0 | 133 | 133 | 33 | 66 | 25 | Y | N | |
| | 0 | 1 | 0 | 1 | 1 | 133 | 133 | 33 | 33 | 25 | Y | N | |
| | 0 | 1 | 1 | 0 | 0 | 133 | 133 | 66 | 66 | 25 | Y | N | |
| | 0 | 1 | 1 | 0 | 1 | 150 | 150 | 33 | 33 | 25 | Y | N | |
| | 0 | 1 | 1 | 1 | 0 | 125 | 125 | 33 | 33 | 25 | Y | N | |
| | 0 | 1 | 1 | 1 | 1 | 166 | 166 | 33 | 33 | 25 | Y | N | |
| | 1 | 0 | 0 | 0 | 0 | Reserved | | | | | N | (1% down spread) | |
| | 1 | 0 | 0 | 0 | 1 | Reserved | | | | | N | (1% down spread) | |
| | 1 | 0 | 0 | 1 | 0 | Reserved | | | | | N | (1% down spread) | |
| | 1 | 0 | 0 | 1 | 1 | Reserved | | | | | N | (1% down spread) | |
| | 1 | 0 | 1 | 0 | 0 | 33 | 33 | 33 | 33 | 50 | N | (1% down spread) | |
| | 1 | 0 | 1 | 0 | 1 | 100 | 133 | 33 | 33 | 50 | N | (1% down spread) | |
| | 1 | 0 | 1 | 1 | 0 | 33 | 33 | 33 | 33 | 25 | N | (1% down spread) | |
| | 1 | 0 | 1 | 1 | 1 | 33 | 33 | 33 | 133 | 25 | N | (1% down spread) | |
| | 1 | 1 | 0 | 0 | 0 | 100 | 200 | 66 | 33 | 25 | Y | (1% down spread) | |
| | 1 | 1 | 0 | 0 | 1 | 200 | 200 | 66 | 33 | 25 | Y | (1% down spread) | |
| | 1 | 1 | 0 | 1 | 0 | 133 | 133 | 33 | 66 | 25 | Y | (1% down spread) | |
| | 1 | 1 | 0 | 1 | 1 | 133 | 133 | 33 | 33 | 25 | Y | (1% down spread) | |
| | 1 | 1 | 1 | 0 | 0 | 133 | 133 | 66 | 66 | 25 | Y | (1% down spread) | |
| | 1 | 1 | 1 | 0 | 1 | 150 | 150 | 33 | 33 | 25 | Y | (1% down spread) | |
| | 1 | 1 | 1 | 1 | 0 | 125 | 125 | 33 | 33 | 25 | Y | (1% down spread) | |
| | 1 | 1 | 1 | 1 | 1 | 166 | 166 | 33 | 33 | 25 | Y | (1% down spread) | |
| Bit3 | 0 - Frequency is selected by hardware select, Latched inputs<br>1 - Frequency is selected by Bit 2, 7:4 | | | | | | | | | | | | |
| Bit 1 | RESERVED | | | | | | | | | | | | |
| Bit 0 | 0 - Running<br>1 - Tristate all outputs | | | | | | | | | | | | |



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**Byte 1: Output Enable Register**

(1 = enable, 0 = tristate)

| Bit | Pin # | PUP | Description |
|---|---|---|---|
| Bit7 | - | X | RESERVED |
| Bit6 | 49, 48 | 1 | CPUT/C1 |
| Bit5 | 53, 52 | 1 | CPUT/C0 |
| Bit4 | 25 | X | SSEN Read back |
| Bit3 | 24 | X | FS3 Read back |
| Bit2 | 23 | X | FS2 Read back |
| Bit1 | 22 | X | FS1 Read back |
| Bit0 | 21 | X | FS0 Read back |

**Byte 2: Output Enable Register**

(1 = enable, 0 = tristate)

| Bit | Pin # | PUP | Description |
|---|---|---|---|
| Bit7 | - | X | RESERVED |
| Bit6 | 27 | 1 | PCI_X6 |
| Bit5 | 26 | 1 | PCI_X5 |
| Bit4 | 25 | 1 | PCI_X4 |
| Bit3 | 24 | 1 | PCI_X3 |
| Bit2 | 23 | 1 | PCI_X2 |
| Bit1 | 22 | 1 | PCI_X1 |
| Bit0 | 21 | 1 | PCI_X0 |

**Byte 3: Output Enable Register**

(1 = enable, 0 = tristate)

| Bit | Pin # | PUP | Description |
|---|---|---|---|
| Bit7 | 42, 43, 44, 45 | 1 | DDRT/C (0:1) |
| Bit6 | 36, 37, 38, 39 | 1 | DDRT/C (2:3) |
| Bit5 | 30, 31, 32, 33 | 1 | DDRT/C (4:5) |
| Bit4 | - | - | RESERVED |
| Bit3 | 16 | 1 | PCI3 |
| Bit2 | 15 | 1 | PCI2 |
| Bit1 | 14 | 1 | PCI1 |
| Bit0 | 13 | 1 | PCI0 |



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**Byte 4: Output Enable Register**

(1 = enable, 0 = Tristate )

| Bit | Pin # | PUP | Description |
|---|---|---|---|
| Bit7 | - | 1 | RESERVED |
| Bit6 | - | 1 | RESERVED |
| Bit5 | - | 1 | RESERVED |
| Bit4 | - | 1 | RESERVED |
| Bit3 | - | 1 | RESERVED |
| Bit2 | - | 1 | REF2_50M (1= ENABLE, 0=Tri state) |
| Bit1 | - | 1 | REF1 (1= ENABLE, 0=Tri state) |
| Bit0 | - | 1 | REF0 (1= ENABLE, 0=Tri state) |

**Byte 5: Reserved**

| Bit | Pin # | PUP | Description |
|---|---|---|---|
| Bit7 | X | X | RESERVED |
| Bit6 | X | 1 | RESERVED |
| Bit5 | X | 1 | RESERVED |
| Bit4 | X | 1 | RESERVED |
| Bit3 | X | 1 | RESERVED |
| Bit2 | X | 1 | RESERVED |
| Bit1 | X | 1 | RESERVED |
| Bit0 | X | 1 | RESERVED |

**Byte 6: Vendor ID Register**

(1 = enable, 0 = disable)

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | Revision ID Bit3 | 0 | Revision ID values will be based on individual device revisions |
| Bit 6 | Revision ID Bit 2 | 0 | |
| Bit 5 | Revision ID Bit1 | 0 | |
| Bit 4 | Revision ID Bit0 | 0 | |
| Bit 3 | Vendor ID Bit3 | 0 | RESERVED |
| Bit 2 | Vendor ID Bit2 | 0 | RESERVED |
| Bit 1 | Vendor ID Bit1 | 0 | RESERVED |
| Bit 0 | Vendor ID Bit0 | 1 | ICS |



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### Byte 7: Revision ID and Device ID Register

(1 = enable, 0 = disable)

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | Device ID7 | 0 | Device ID values will be based on individual device "02" in this case |
| Bit 6 | Device ID6 | 0 | |
| Bit 5 | Device ID5 | 0 | |
| Bit 4 | Device ID4 | 0 | |
| Bit 3 | Device ID3 | 0 | |
| Bit 2 | Device ID2 | 0 | |
| Bit 1 | Device ID1 | 1 | |
| Bit 0 | Device ID0 | 0 | |

### Byte 8: Byte Count and Readback Regsiter.

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | Byte7 | 0 | Note: Writing to this register will configure byte count and how many bytes will be read back. Default is $0F_H$ = 15 bytes |
| Bit 6 | Byte6 | 0 | |
| Bit 5 | Byte5 | 0 | |
| Bit 4 | Byte4 | 0 | |
| Bit 3 | Byte3 | 1 | |
| Bit 2 | Byte2 | 1 | |
| Bit 1 | Byte1 | 1 | |
| Bit 0 | Byte0 | 1 | |

### Byte 9: Watchdog Timer Count Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | WD7 | 0 | RESERVED |
| Bit 6 | WD6 | 0 | |
| Bit 5 | WD5 | 0 | |
| Bit 4 | WD4 | 1 | |
| Bit 3 | WD3 | 0 | |
| Bit 2 | WD2 | 0 | |
| Bit 1 | WD1 | 0 | |
| Bit 0 | WD0 | 0 | |



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### Byte 10: Programming Enable Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | M/N Program Enable | 0 | Programming Enable bit<br>0 = no programming. Frequencies are selected by HW latches or by Byte 0,<br>1 = enable all SMBUS programming |
| Bit 6 | WD Enable | 0 | RESERVED |
| Bit 5 | WD Alarm | 0 | RESERVED |
| Bit 4 | - | - | RESERVED |
| Bit 3 | - | - | |
| Bit 2 | - | - | |
| Bit 1 | - | - | |
| Bit 0 | - | - | |

### Byte 11: VCO Frequency M Divider (Reference divider) Control Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | Ndiv8 | X | N divider bit 8 |
| Bit 6 | Mdiv6 | X | The decimal representation of Mdiv (6:0) corresponds to the reference divider value. Default at power up is equal to the latched inputs selection. |
| Bit 5 | Mdiv5 | X | |
| Bit 4 | Mdiv4 | X | |
| Bit 3 | Mdiv3 | X | |
| Bit 2 | Mdiv2 | X | |
| Bit 1 | Mdiv1 | X | |
| Bit 0 | Mdiv0 | X | |

### Byte 12: VCO Frequency N Divider (VCO divider) Control Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | Ndiv7 | X | The decimal representation of Ndiv (7:0) corresponds to the VCO divider value. Default at power up is equal to the latched inputs selection. Notice Ndiv 8 is located in Byte 11. |
| Bit 6 | Ndiv6 | X | |
| Bit 5 | Ndiv5 | X | |
| Bit 4 | Ndiv4 | X | |
| Bit 3 | Ndiv3 | X | |
| Bit 2 | Ndiv2 | X | |
| Bit 1 | Ndiv1 | X | |
| Bit 0 | Ndiv0 | X | |



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### Byte 13: Spread Spectrum Control Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | SS 7 | X | The Spread Spectrum (13:0) (or see Byte 14) bit will program the spread percentage. Spread percent needs to be calculated based on the VCO frequency, spreading profile, spreading amount, and spread frequency. It is recommended to use ICS software forspread programming. Default power on is latched FS divider. |
| Bit 6 | SS 6 | X | |
| Bit 5 | SS 5 | X | |
| Bit 4 | SS 4 | X | |
| Bit 3 | SS 3 | X | |
| Bit 2 | SS 2 | X | |
| Bit 1 | SS 1 | X | |
| Bit 0 | SS 0 | X | |

### Byte 14: Spread Spectrum Control Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | RESERVED | X | RESERVED |
| Bit 6 | RESERVED | X | RESERVED |
| Bit 5 | SS 13 | X | Spread Spectrum Bit 13 |
| Bit 4 | SS 12 | X | Spread Spectrum Bit 12 |
| Bit 3 | SS 11 | X | Spread Spectrum Bit 11 |
| Bit 2 | SS 10 | X | Spread Spectrum Bit 10 |
| Bit 1 | SS 9 | X | Spread Spectrum Bit 9 |
| Bit 0 | SS 8 | X | Spread Spectrum Bit 8 |

### Byte 15: Output Divider Control Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | DDR Div 3 | X | DDRC clock divider ratio can be configured via these four bits individually. For divider selection table, refer to Table 1. Default at power up is latched FS divider. |
| Bit 6 | DDR Div 2 | X | |
| Bit 5 | DDR Div 1 | X | |
| Bit 4 | DDR Div 0 | X | |
| Bit 3 | CPU Div 3 | X | CPU clock divider ratio can be configured via these four bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider. |
| Bit 2 | CPU Div 2 | X | |
| Bit 1 | CPU Div 1 | X | |
| Bit 0 | CPU Div 0 | X | |



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### Byte 16: Output Divider Control Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | PCI Div 3 | X | PCI clock divider ratio can be configured via these four bits individually. For divider selection table, refer to Table 2. Default at power up is latched FS divider. |
| Bit 6 | PCI Div 2 | X | |
| Bit 5 | PCI Div 1 | X | |
| Bit 4 | PCI Div 0 | X | |
| Bit 3 | | X | RESERVED |
| Bit 2 | | X | |
| Bit 1 | | X | |
| Bit 0 | | X | |

### Byte 17: Output Divider Control Register

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | PCI_XINV | X | PCI_X Phase Inversion bit |
| Bit 6 | PCI_INV | X | PCI Phase Inversion bit |
| Bit 5 | DDR_INV | X | DDR Phase Inversion bit |
| Bit 4 | CPU_INV | X | CPUCLK Phase Inversion bit |
| Bit 3 | PCI _XDiv 3 | X | PCI clock divider ratio can be configured via these |
| Bit 2 | PCI _XDiv 2 | X | |
| Bit 1 | PCI _XDiv 1 | X | |
| Bit 0 | PCI_X Div 0 | X | |

### Table 1 CPU/DDR Output Divide

| Div (3:2) / Div (1:0) | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| 00 | /2 | /4 | /8 | /16 |
| 01 | /3 | /6 | /12 | /24 |
| 10 | /5 | /10 | /20 | /40 |
| 11 | /9 | /18 | /36 | /72 |

### Table 2 PCI/PCI_X Output Divide

| Div (3:2) / Div (1:0) | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| 00 | /2 | /4 | /8 | /16 |
| 01 | /3 | /6 | /12 | /24 |
| 10 | /9 | /18 | /36 | /72 |
| 11 | /15 | /30 | /60 | /120 |



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### Byte 18: Group Skew Control Register

| Bit | Name | PWD | Programming Sequence | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | RESERVED | 0 | 0 | 0 | 0 | 0 | 0ps |
| Bit 6 | | 0 | 0 | 1 | 0 | 0 | 150ps |
| Bit 5 | | 0 | 1 | 0 | 0 | 0 | 300ps |
| Bit 4 | | 0 | 1 | 1 | 0 | 0 | 450ps |
| Bit 3 | These four bits control all clocks to CPU (1:0) | 0 | 1 | 1 | 0 | 1 | 600ps |
| Bit 2 | | 0 | 1 | 1 | 1 | 0 | 750ps |
| Bit 1 | | 0 | 1 | 1 | 1 | 1 | 900ps |
| Bit 0 | | 0 | Reserved | | | | |

### Byte 19: Group Skew Control Register

| Bit | Name | PWD | Programming Sequence | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | These four bits control DDR (5:0) | 0 | 0 | 0 | 0 | 0 | 0ps |
| Bit 6 | | 0 | 0 | 1 | 0 | 0 | 150ps |
| Bit 5 | | 0 | 1 | 0 | 0 | 0 | 300ps |
| Bit 4 | | 0 | 1 | 1 | 0 | 0 | 450ps |
| Bit 3 | These four bits control PCI (3:0) | 0 | 1 | 1 | 0 | 1 | 600ps |
| Bit 2 | | 0 | 1 | 1 | 1 | 0 | 750ps |
| Bit 1 | | 0 | 1 | 1 | 1 | 1 | 900ps |
| Bit 0 | | 0 | Reserved | | | | |

### Byte 20: Slew Rate Control Register

| Bit | Name | PWD | Programming Sequence | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | These four bits control Skew PCI _X:0) | 0 | 0 | 0 | 0 | 0 | 0ps |
| Bit 6 | | 0 | 0 | 1 | 0 | 0 | 150ps |
| Bit 5 | | 0 | 1 | 0 | 0 | 0 | 300ps |
| Bit 4 | | 0 | 1 | 1 | 0 | 0 | 450ps |
| Bit 3 | RESERVED | 0 | 1 | 1 | 0 | 1 | 600ps |
| Bit 2 | | 0 | 1 | 1 | 1 | 0 | 750ps |
| Bit 1 | | 0 | 1 | 1 | 1 | 1 | 900ps |
| Bit 0 | | 0 | Reserved | | | | |



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**Byte 21: Slew Rate Control Register**

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | REF0 | 0 | Clock slew rate control bits.<br>01 = strong: 11 = 00 medium: 10 = weak |
| Bit 6 | | 1 | |
| Bit 5 | RESERVED | X | RESERVED |
| Bit 4 | RESERVED | X | RESERVED |
| Bit 3 | PCI (1:0) | 0 | Clock slew rate control bits.<br>(00=0.7X, 01=0.8X, 10=0.90X, 11=1.0X) |
| Bit 2 | | 1 | |
| Bit 1 | PCI (3:2) | 0 | Clock skew rate control bits.<br>(00=0.7X, 01=0.8X, 10=0.90X, 11=1.0X) |
| Bit 0 | | 1 | |

**Byte 22: Slew Rate Control Register**

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | PCI_X6 | 0 | Clock slew rate control bits.<br>AGP Phase Inversion bit |
| Bit 6 | | 1 | |
| Bit 5 | PCI_X(5) | 0 | Clock slew rate control bits.<br>(00=0.63X, 01=0.75X, 10=0.88X, 11=1.0X) |
| Bit 4 | | 1 | |
| Bit 3 | PCI_X(4:3:2) | 0 | Clock slew rate control bits.<br>(00=0.63X, 01=0.75X, 10=0.88X, 11=1.0X) |
| Bit 2 | | 1 | |
| Bit 1 | PCI_X(1:0) | 0 | Clock slew rate control bits.<br>(00=0.63X, 01=0.75X, 10=0.88X, 11=1.0X) |
| Bit 0 | | 1 | |

**Note for PCI_X frequency selection of 133.33 MHz use 11=1.0X buffer s.**

**Byte 23: Slew Rate Control Register**

| Bit | Name | PUP | Description |
|---|---|---|---|
| Bit 7 | RESERVED | X | RESERVED |
| Bit 6 | | X | |
| Bit 5 | RESERVED | X | RESERVED |
| Bit 4 | | X | |
| Bit 3 | IREFSGL | 1 | 00 = 5x, 01 = 4x, 10 = 6x, 11 = 7x |
| Bit 2 | | 0 | |
| Bit 1 | REF_50M | 0 | Clock slew rate control bits.<br>01 = strong: 11 = 00 medium: 10 = weak |
| Bit 0 | | 1 | |



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## External Components

The MK1493-02A requires a minimum number of external components for proper operation.

### Decoupling Capacitor

Decoupling Capacitors of 0.1μF and 0.001μF must be connected between each VDD and GND as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over one inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ohms.

### Crystal Information

The crystal used should be a fundamental mode, parallel resonant crystal. Do not use third overtone. Crystal capacitors should be connected from pins X1 to ground and from X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, $C_L$ is the crystal load capacitance. So for a crystal with 16 pF load capacitance, two 20 pF [(1606) x 2] capacitors should be used.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1493-02A. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 5.5 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

## Electrical Characteristics - Input/Supply/Common Output Parameters

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +75°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2.4 | | VDD +0.3 | V |
| Input Low Voltage | $V_{IL}$ | | -0.3 | | 0.8 | V |
| Input High Current | $I_{IH}$ | $V_{IN} = V_{DD}$ | -5 | | 5 | mA |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0V; Inputs w/no pull-up resistors | -5 | | | mA |
| | $I_{IL2}$ | VIN = 0V; Inputs with pull-up resistors | -200 | | | mA |
| Operating Supply Current | $I_{DD}$ | CL = 0pF; Select @ 66M | | 135 | | mA |
| | | CL = full load | | 325 | | mA |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH |
| Input Capacitance | $C_{IN}$ | Logic inputs | | | 5 | pF |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF |
| Transition Time | $T_{trans}$ | To 1st crossing of target frequency | | | 3 | ms |
| Setting Time | $T_S$ | From 1st crossing to 1% target frequency | | | 3 | ms |
| Clock Stabilization | $T_{STAB}$ | From $V_{DD}$ = 3.3 V to 1% target frequency | | | 3 | ms |
| Delay | $t_{PZH}$, $t_{PZH}$ | output enable delay (all outputs) | 1 | | 10 | ns |
| | $t_{PLZ}$, $t_{PZH}$ | output disable delay (all outputs) | 1 | | 10 | ns |
| Modulation Frequency | | | 28 | | 33 | kHz |
| Rise Time | $t_{RISE}$ | OE, CLKSTPB, PCISTPB | | | 5 | ns |
| Fall Time | $t_{FALL}$ | OE, CLKSTPB, PCISTPB | | | 5 | ns |
| SMBUS Voltage | $V_{DD}$ | | 2.7 | | 5.5 | V |
| Low-Level Output Voltage | $V_{OL}$ | | | | 0.4 | V |
| Current Sinking | $I_{pullup}$ | $V_{OL}$ = 0.4 V | 4 | | | mA |
| SCLK/SDATA CLK/Data Rise Time | $T_{RI}$ | Max $V_{IL}$-0.15 to Min $V_{IH}$+0.15 | | | 1000 | ns |
| SCLK/SDATA CLK/Data Fall Time | $T_{FI}$ | Max $V_{IL}$-0.15 to Min $V_{IH}$+0.15 | | | 300 | ns |
| OE Enable Time | | tri state to active output after powerup | | | 10 | ns |
| OE Disable Time | | Active data to tri state, after powerup | | | 10 | ns |



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## Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C, $C_L$= 2 pF

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Current Source Output Impedance | $Z_O$ | $V_O = V_X$ | 3000 | | | Ω |
| Voltage High | $V_{HIGH}$ | Statistical measurement on a single ended signal using oscilloscope math function | 660 | 770 | 850 | mV |
| Voltage Low | $V_{LOW}$ | | -150 | 5 | 150 | |
| Max Voltage | $V_{OVS}$ | Measurement on single ended signal using absolute value | | 756 | 1150 | mV |
| Min Voltage | $V_{UDS}$ | | -300 | -7 | | mV |
| Crossing Voltage (abs) | $V_{ABS}$ | Abolute value of crossing Voltage | 250 | 350 | 550 | mV |
| Crossing Voltage (varaition) | $V_{cross}$ | Variation of crossing over all edges | | 12 | 140 | mV |
| Rise Time | $t_{RISE}$ | $V_{OL}$ = 0.175 V, $V_{OH}$ = 0.525 V | 175 | 332 | 700 | ps |
| Fall Time | $t_{FALL}$ | $V_{OL}$ = 0.175 V, $V_{OH}$ = 0.525 V | 175 | 344 | 700 | ps |
| Rise Time Variation | d-$t_{RISE}$ | | | 30 | 125 | ps |
| Fall Time Variation | d-$t_{FALL}$ | | | 30 | 125 | ps |
| Duty Cycle | | Measurement from differential wave forms | 45 | 49 | 55 | % |
| Skew | | $V_T$ = 50%( mesurement threshold) | | | 100 | ps |
| Jitter, Cycle to Cycle | | Measurement from differential wave forms | | 60 | 125 | ps |

## Electrical Characteristics - PCI_XCLK

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C, $C_L$= 10-30 pF

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output Frequency | | | 33.33 | | 133.33 | MHz |
| Output Impedance | | $V_O = V_{DD}$*(0.5) | 12 | | 55 | Ω |
| Output High Voltage | $V_{OH1}$ | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL1}$ | $I_{OL}$ = 1 mA | | | 0.55 | V |
| Output High Current | $I_{OH1}$ | $V_{OH}$@MIN = 1.0 V, $V_{OH}$@MAX = 3.135 V | -33 | | -33 | mA |
| Output Low Current | $I_{OL1}$ | $V_{OL}$@MIN = 1.95 V, $V_{OL}$@MAX = 0.4 V | 30 | | 38 | mA |
| Rise Time | $t_{RISE}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 3 | ns |
| Fall Time | $t_{FALL}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns |
| Duty Cycle | | $V_T$ = 1.5 V | 45 | | 55 | % |
| Skew | | $V_T$ = 1.5 V | | | 200 | ps |
| Jitter PCI (6:0) | | $V_T$ = 1.5 V | | | 250 | ps |



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## Electrical Characteristics/DDR Buffers - Input/Supply/Common Output Parameters

Unless stated otherwise, **VDD = 2.5 V ±0.2 V** , Ambient Temperature 0 to +75°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Analog /core supply Voltage | $V_{DD}$, $A_{VDD}$ | | 2.3 | 2.5 | 2.7 | |
| Operating Supply Current | $I_{DD}$ | $C_L$ = 0pF; Select @ 133M | | 245 | 300 | mA |
| High Impedance Output Current | $I_{OZ}$ | $V_{DD}$ = 2.7 V, $V_{OUT}$ = $V_{DD}$ or GND | | | 10 | µA |
| Input Clamp Voltage | $V_{IK}$ | Iin = -18 mA | | | -1.2 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{DD}$ = min to max, $I_{OH}$ = -1 mA | 2.1 | 2.42 | | V |
| | | $V_{DD}$ = 2.3 V, $I_{OH}$ = -12 mA | 1.7 | 1.87 | | V |
| Low Level Output Voltage | $V_{OL}$ | $V_{DD}$ = min to max, $I_{OL}$ = 1 mA | | 0.04 | 0.1 | V |
| | | $V_{DD}$ = 2.3 V, $I_{OL}$ = 12 mA | | 0.35 | 0.6 | V |
| Input Capacitance | $C_{IN}$ | $V_I$ = $V_{DD}$ or GND | | | | pF |
| Output Capacitance | $C_{OUT}$ | $V_I$ = $V_{DD}$ or GND | | 3 | | pF |
| Input Voltage leve | VIL | | | | VDD/2-0.5 V | V |
| Input Voltage level | VIH | | VDD/2+0.5 V | | | V |
| Input Duty Cycle | | | 40% | | 50% | |
| Input mac jitter | | | | | 150 | ps |

## Timing Requirements

Unless stated otherwise, **VDD = 2.5 V ±0.2 V**, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Clock Frequency | | | 33.33 | | 200 | MHz |
| Input Clock Duty Cycle | | | 40 | | 60 | % |
| Clock Stabilization | $t_{STAB}$ | from $V_{DD}$ = 2.5 V to 1% target freq. | | | 3 | ms |

## Switching Characteristics

Unless stated otherwise, **VDD = 2.5 V ±0.2 V**, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Absolute Jitter | $t_{jabs}$ | 33 MHz | | | 120 | ps |
| | | 100/125/133/150/167/200 MHz | | | 100 | ps |
| Cycle to cycle jitter | | 33 MHz | | 50 | 110 | ps |
| | | 100/125/133/150/167 MHz | | 60 | 100 | ps |
| Output to output Skew | | with input clock 0-2.5 V 0.8 ns rise/fall | | 40 | 100 | ps |
| Duty Cycle (differential)[1] | $D_C$ | no loads, 66 MHz to 167 MHz | 47 | 50 | 53 | % |
| Rise Time, Fall Time | $t_{RISE}$, $t_{FALL}$ | Single-ended 20 - 80%; Load = 120Ω/12 pF | 450 | 550 | 950 | ps |



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[1] While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = $t_{wH}/t_C$, where the cycle time ($t_C$) decreases as the frequency increases.

## Electrical Characteristics - PCI

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C, $C_L$ = 10 - 30 pF

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output Frequency | $F_O$ | | 33.33 | | 66.66 | MHz |
| Output Impedance | $R_{DSP}$ | $V_O = V_{DD}*0.5$ | 12 | | 55 | W |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH}$ | $V_{OH}$@MIN = 1.0 V, $V_{OH}$ @MAX = 3.135 V | -33 | | -33 | mA |
| Output Low Current | $I_{OL}$ | $V_{OH}$@MIN = 1.95 V, $V_{OH}$ @MAX = 0.4 V | 30 | | 38 | mA |
| Rise Time | $T_{RISE}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 2 | ns |
| Fall Time | $T_{FALL}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns |
| Duty Cycle | $d_t$ | $V_T$ = 1.5 V | 45 | | 55 | % |
| Skew | $t_{SK}$ | $V_T$ = 1.5 V | | | 100 | ps |
| Jitter | | $V_T$ = 1.5 V | | | 300 | ps |

## Electrical Characteristics - 50 MHz (pin 4)

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C, $C_L$ = 10 - 30 pF

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V |
| Output High Current | $I_{OH}$ | $V_{OH}$@MIN = 1.0 V, $V_{OH}$ @MAX = 3.135 V | -29 | | -23 | mA |
| Output Low Current | $I_{OL}$ | $V_{OH}$@MIN = 1.95 V, $V_{OH}$ @MAX = 0.4 V | 29 | | 27 | mA |
| Rise Time | $T_{RISE}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | | | 2.0 | ns |
| Fall Time | $T_{FALL}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | | | 1.8 | ns |
| Duty Cycle | $d_t$ | $V_T$ = 1.5 V | 45 | | 55 | % |
| Jitter | | $V_T$ = 1.5 V | | | 400 | ps |

## Electrical Characteristics - REF(Pins 7,8)



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Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature 0 to +70°C, $C_L$ = 10 - 30 pF

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output Impedance | $R_{DSP}$ | $V_O = V_{DD}*0.5$ | 20 | | 60 | Ω |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH}$ | $V_{OH}$@MIN = 1.0 V, $V_{OH}$ @MAX = 3.135 V | -29 | | -23 | mA |
| Output Low Current | $I_{OL}$ | $V_{OH}$@MIN = 1.95 V, $V_{OH}$ @MAX = 0.4 V | 29 | | 27 | mA |
| Rise Time | $T_{RISE}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | | 2 | | ns |
| Fall Time | $T_{FALL}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | | 1.8 | | ns |
| Duty Cycle | $d_t$ | $V_T$ = 1.5 V | 45 | | 55 | % |
| Skew | $t_{SK}$ | $V_T$ = 1.5 V | | 70 | | ps |
| Jitter | | $V_T$ = 1.5 V | | | 1000 | ps |

## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a five-bit internal data latch. At the end of Power-on resent, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode, the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operation period.

**Figure 1**

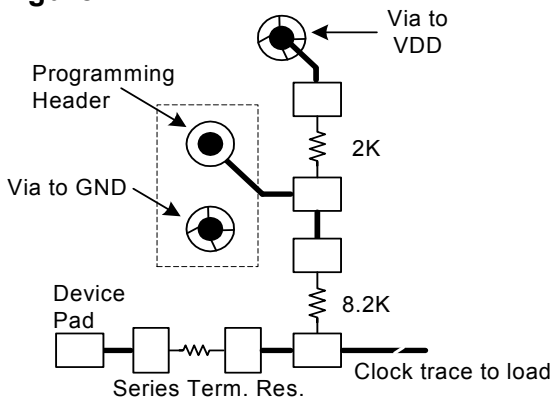


Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper installed, the pin will be pulled high. With the jumper in place, the pin will be pulled low. If programmability is not necessary, then only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to place the series termination resistor close to the driver than to the programming resistor.



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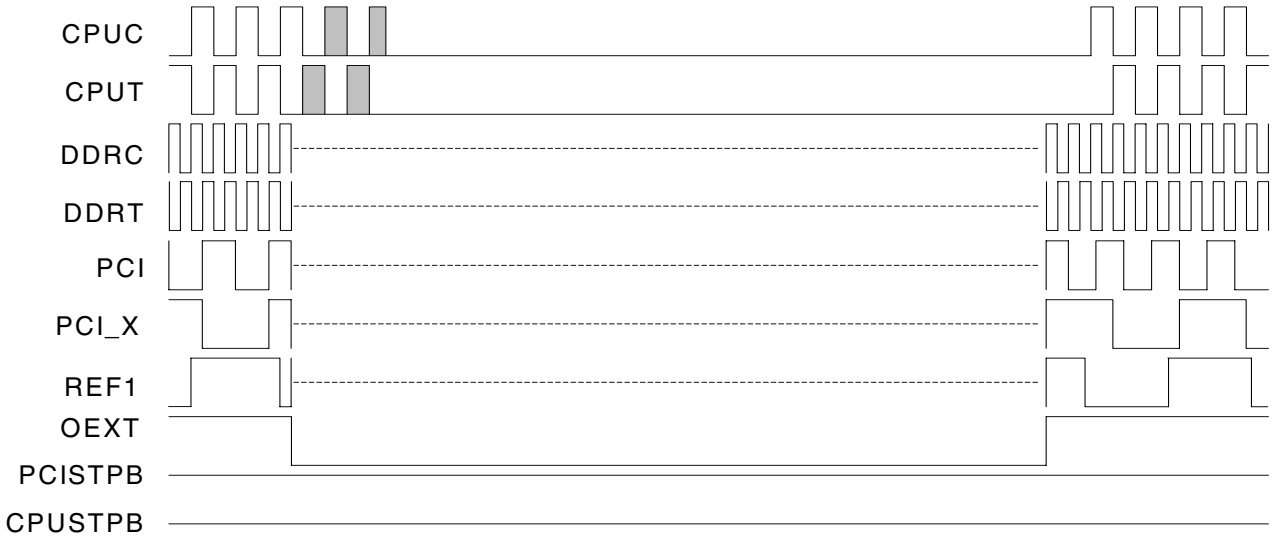
## OE - ASSERTION (transition from logic “1” to logic “0”)

When the asynchronous OE pin is pulled low, the REF clocks, PCI clocks, PCI_XClocks, the DDRT/C Clocks, are tristated in 20 ns. The CPUT/C clocks are pulled low. See waveform 1.

## OE - DEASSERTION (transition from logic “0” to logic “1”)

When the asynchronous OE pin is pulled high, the REF clocks, PCI clocks, PCI_X Clocks, DDRT/C Clocks, and the CPUT/C clock are enabled in 20 ns. See waveform 1.

### Waveform 1



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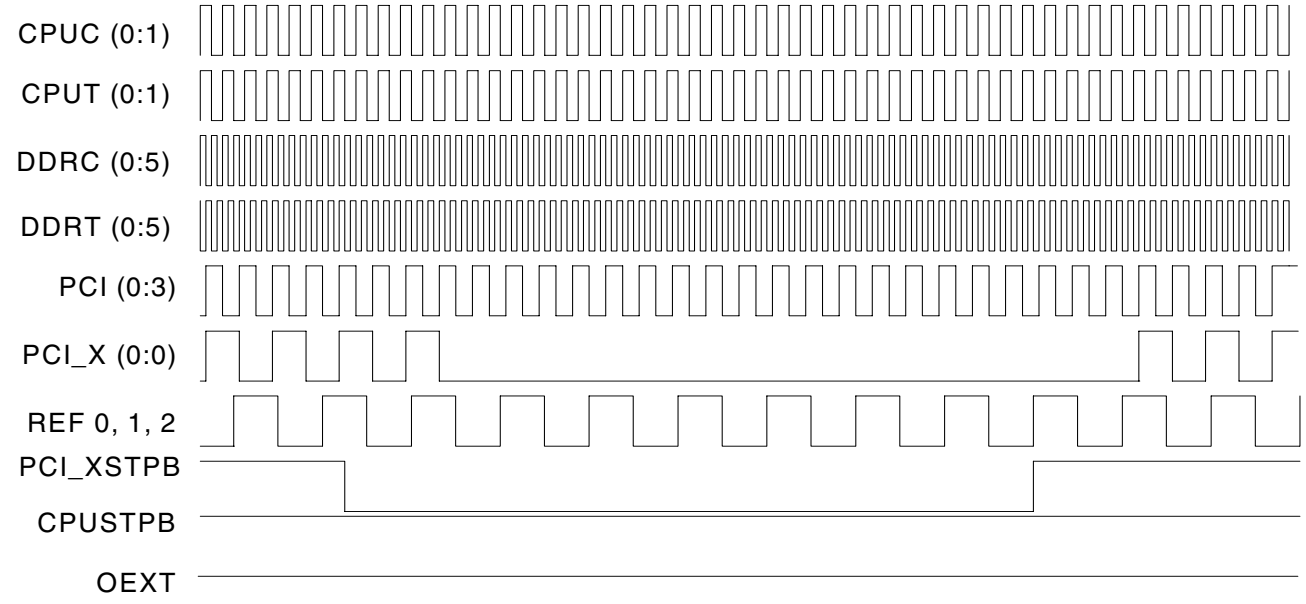
## PCI_XSTPB Input Timing - ASSERTION (transition from logic “1” to logic “0”)

When the input of the PCI_XSTPB signal is pulled low, PCI_X (6:0) outputs are latched low in their next high to low transition. The PCI_XSTPB set up time is 10ns for the transtions to be recognized by the next rising edge (see waveform 2; one cycle latency). All other waveforms are not affected. This timing assumes that the seven PCI_X outputs are enabled via Byte 2 (bits 0:6). See waveform 2.

## PCI_XSTPB - DEASSERTION (transition from logic “0” to logic “1”)

When the PCI_XSTPB signal is pulled high, the PCI_X signals are enabled after a setup time of 10 ns with a one cycle latency (see waveform 2). All PCI_X outputs are enabled via Byte 2 (bits 0:6).

### Waveform 2



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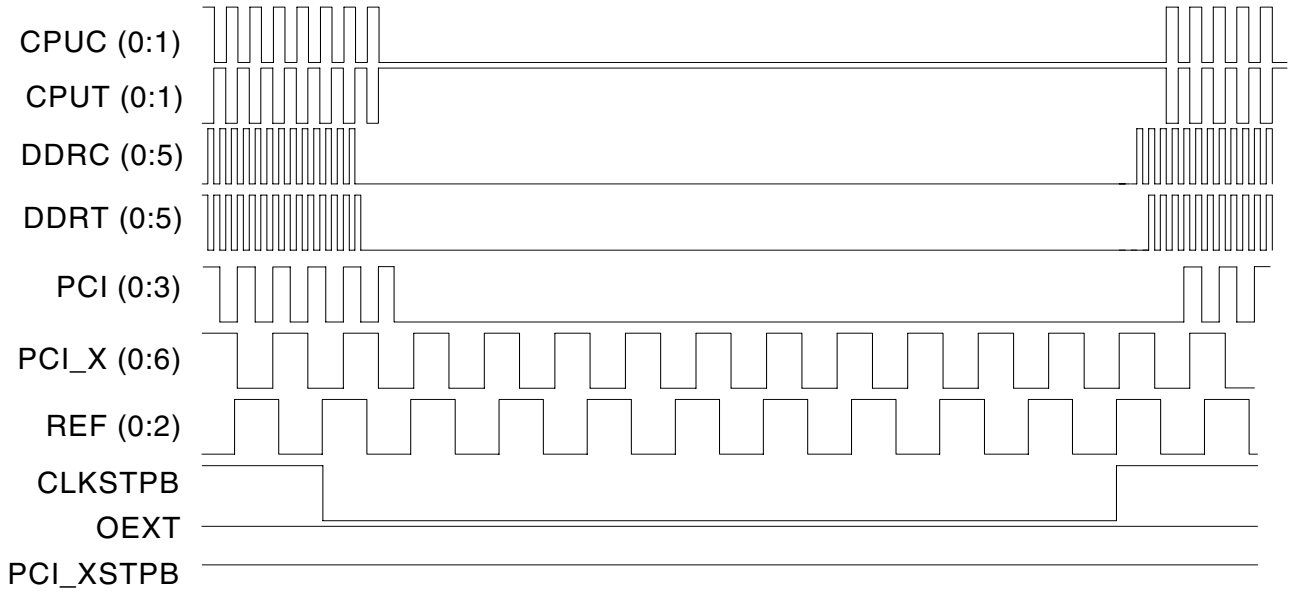
### CLK_STPB - Assertion (transition from logic “0” to logic “1”)

When this asynchronous input is pulled low, all clocks (CPUT/C, DDRT/C, PCI) are pulled low with a two cycle latency. See waveform 3. This condition assumes all CPUT/C, DDRT/C, and PCI clocks are enabled via Byte 3 (Bit 5, Bit 6), Byte 3 (Bit 0, 1, 2, 3, 5, 6, 7). The set up time is 10 ns.

### CLK_STPB - Deassertion (transition from logic “1” to logic “0”)

When this asynchronous input is pulled high, all clocks (CPUT/C, DDRT/C, PCI) are enabled after a setup time of 10 ns and two cycle latency. See waveform 3. The waveform assumes that the CPUT/C, DDRT/C, and PCI clocks are enabled via Byte 1 (Bit 5, Bit 6), Byte 3 (Bit 0, 1, 2, 3, 5, 6, 7). The set up time is 10 ns.

### Waveform 3




## IREF

If board target trace impedance (Z) is 50Ω, then Rr = 475Ω (1%), providing IREF of 2.32 mA, output current ($I_{OH}$) is equal to 6*IREF.



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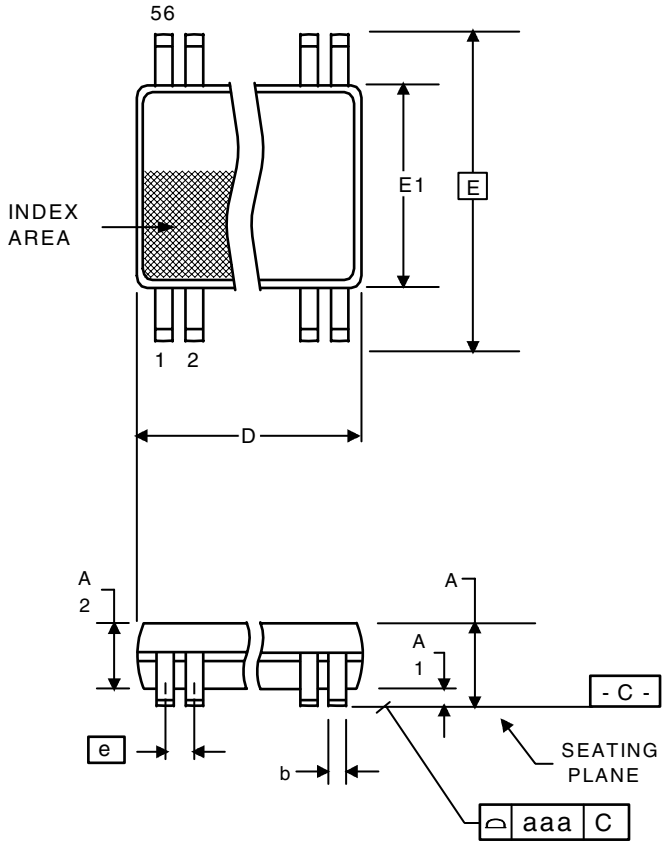
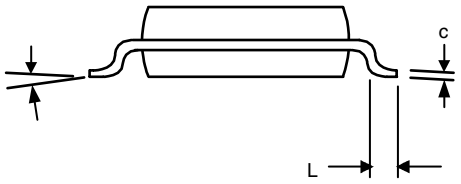
## Package Outline and Package Dimension

**56-pin TSSOP 6.10 mm (240 mil) body, 0.50 mm. (20 mil) pitch**
Package dimensions are kept current with JEDEC Publication No. 95




| | Millimeters | | Inches | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** |
| A | -- | 1.20 | -- | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.17 | 0.27 | 0.007 | 0.011 |
| C | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 13.90 | 14.10 | 0.547 | 0.555 |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | 0.236 | 0.244 |
| e | 0.50 Basic | | 0.020 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| $\alpha$ | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

## Ordering Information

| Part / Order Number | Marking | Shipping packaging | Package | Temperature |
|---|---|---|---|---|
| MK1493-02AG | MK1493-02AG | Tubes | 56-pin TSSOP | 0 to +70° C |
| MK1493-02AGTR | MK1493-02AG | Tape and Reel | 56-pin TSSOP | 0 to +70° C |

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