MK1518C LDMOS TRANSISTOR

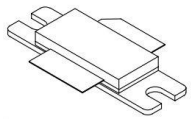
Document Number: MK1518C
Preliminary Datasheet V1.0

180W, 28V High Power RF LDMOS FETs

Description

The MK1518C is a 180-watt high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.5GHz.

MK1518C



- Typical Performance (On Innogration 1GHz narrow band fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 200 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)
1000 MHz	18	180	65

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 1GHz below high performance amplifier where demands single ended device
- 1300MHz particle accelerator
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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	65	70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	———	———	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	———	———	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	V_{GS}(th)	———	1.98	———	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	———	2.53	———	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V)	Rds(on)		220		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		170		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		70		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		3		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 1000 MHz, CW Signal Measurements.

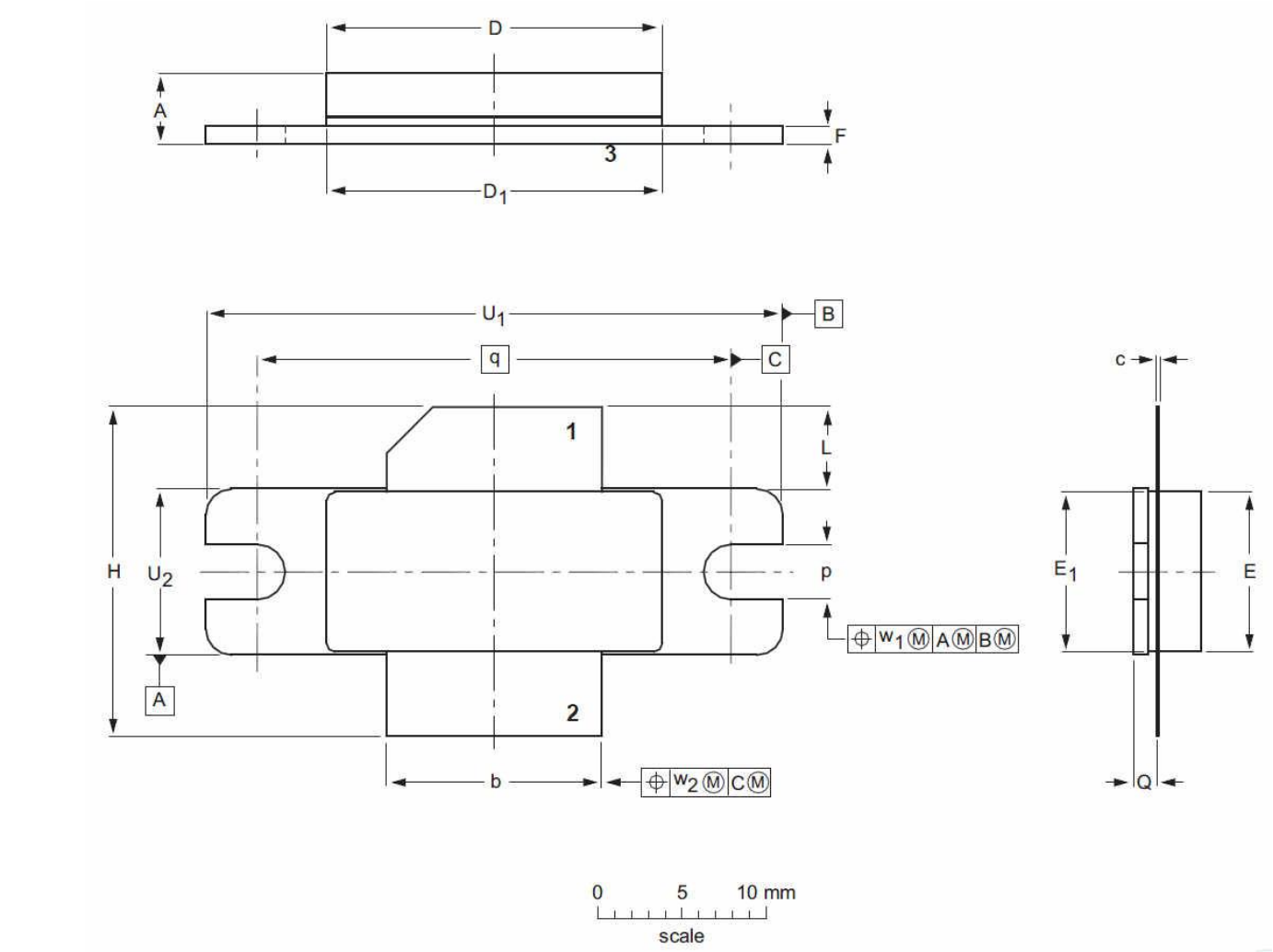
Power Gain	Gp	———	18	———	dB
Drain Efficiency@P1dB	η_D	———	65	———	%
1 dB Compression Point	P_{-1dB}	———	100	———	W
Input Return Loss	IRL	———	-7	———	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 200 mA, f = 1000 MHz

VSWR 10:1 at 180W CW Output Power	No Device Degradation

Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/8/2	Rev 1.0	Preliminary Datasheet Creation

Disclaimers