



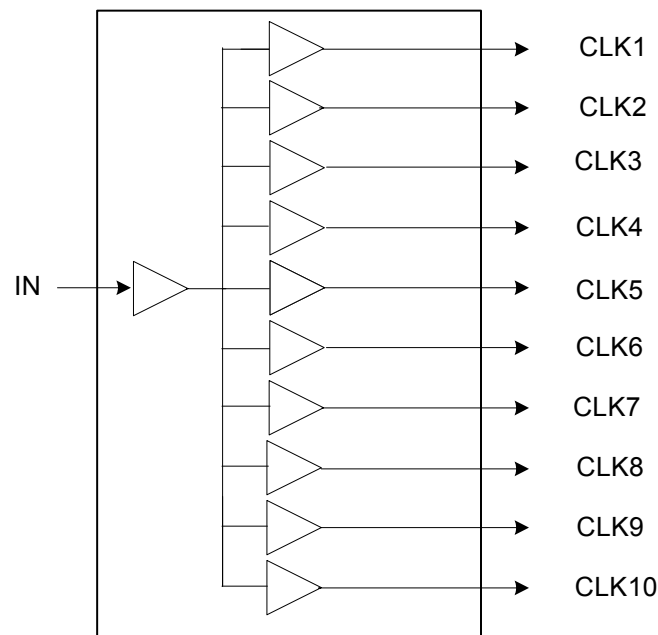
Description

The MK3807-01 is a low skew 3.3 V, 1 to 10 fanout buffer. The large fanout from a single input line reduces loading on the input clock. The TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

Features

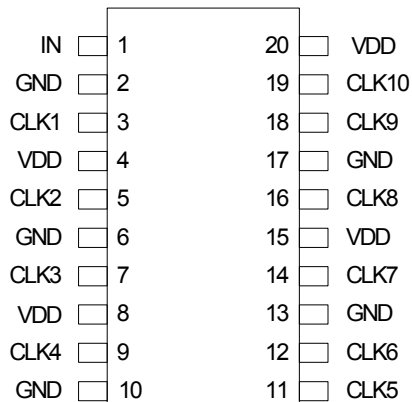
- Packaged in 20-pin SSOP, TSSOP, & SOIC
- Available in Pb (lead) free package
- 1 to 10 fanout buffer
- Maximum skew between outputs of same package 0.35 ns
- Maximum skew between outputs of different packages 0.75 ns
- Max propagation delay of 3.8 ns
- Operating voltage of 3.3 V
- Advanced, low power, CMOS process
- Industrial temperature range -40° C to +85° C
- Hysteresis on all inputs

Block Diagram





Pin Assignment



20 pin SOIC, SSOP, TSSOP

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--------------------|
| 1 | IN | Input | Clock input. |
| 2 | GND | Power | Connect to ground. |
| 3 | CLK1 | Output | Clock output. |
| 4 | VDD | Power | Connect to +3.3 V. |
| 5 | CLK2 | Output | Clock output. |
| 6 | GND | Power | Connect to ground. |
| 7 | CLK3 | Output | Clock output. |
| 8 | VDD | Power | Connect to +3.3 V. |
| 9 | CLK4 | Output | Clock output. |
| 10 | GND | Power | Connect to ground. |
| 11 | CLK5 | Output | Clock output. |
| 12 | CLK6 | Output | Clock output. |
| 13 | GND | Power | Connect to ground. |
| 14 | CLK7 | Output | Clock output. |
| 15 | VDD | Power | Connect to +3.3 V. |
| 16 | CLK8 | Output | Clock output. |
| 17 | GND | Power | Connect to ground. |
| 18 | CLK9 | Output | Clock output. |
| 19 | CLK10 | Output | Clock output. |
| 20 | VDD | Power | Connect to +3.3 V. |



External Components

The MK3807-01 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μ F must be connected between VDD and GND, as close to these pins as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance) place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω .

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) The 0.01 μ F decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.
- 2) To minimize EMI, the 33 Ω series termination resistor, (if needed) should be placed close to the clock output.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3807-01. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|--------|------|--------|-------|
| Ambient Operating Temperature | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.135 | +3.3 | +3.465 | V |



DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40° C to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------------|------------------|---|----------------|------|-------------------|-------|
| Operating Voltage | VDD | | 3.135 | 3.3 | 3.465 | V |
| Quiescent Power Supply Current | ICC | VCC=Max VIN=GND or VCC | | 3 | 30 | μA |
| | | VCC=Max VIN=@TTL HIGH (VCC-0.6 V) | | 2.0 | 300 | μA |
| Input High Voltage | V _{IH} | High Level Input pins | 2 | | 5.5 | V |
| Input Low Voltage | V _{IL} | Low Level Input pins | -0.5 | | 0.8 | V |
| Output High Voltage | V _{OH} | VCC=min VIN=VIH or VIL I _{OH} = -0.1 mA, I _{OH} = -8 mA | VDD-0.2 2.4 | 3.0 | | V |
| Output Low Voltage | V _{OL} | VCC=min VIN=VIH or VIL I _{OL} = -0.1 mA, I _{OL} = 16 mA I _{OL} = 24 mA | | | 0.2 0.4 0.5 | V |
| Short Circuit Current | I _{OS} | VCC=Max, V _{OUT} =GND | -60 | -135 | -240 | mA |
| Input Capacitance | C _{IN} | VIN=0V, Note1 | | 5 | 6.0 | pF |
| Output Capacitance | C _{OUT} | V _{OUT} =0V, Note1 | | 5.5 | 8.0 | pF |
| Input Hysteresis | V _H | | | 150 | | mV |

Note1: This parameter is not tested.



AC Electrical Characteristics

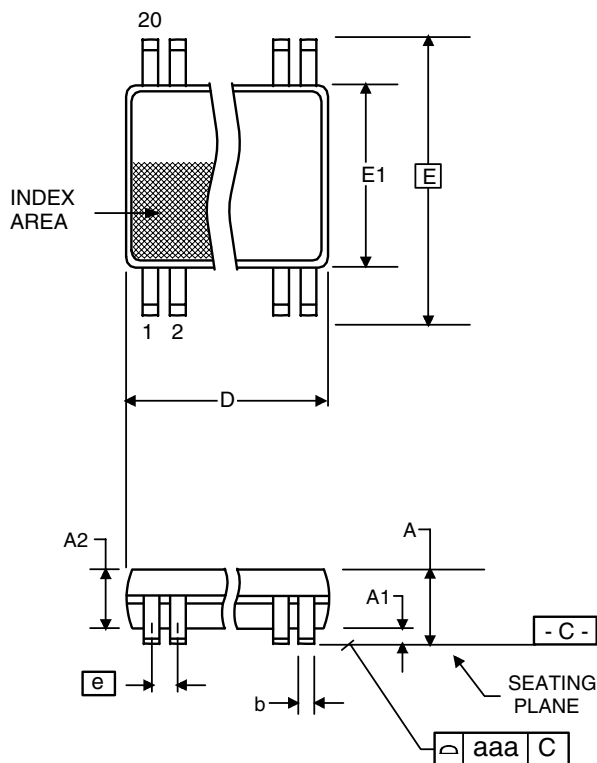
Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$, Ambient Temperature -40°C to $+85^{\circ}\text{C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|-------------------|---------------------------------------|------|------|------|-------|
| Skew between outputs of same package | $tsk_{g(0)}$ | $CL=50\text{ pF}$, $RL=500\Omega$ | | | 0.35 | ns |
| Skew between opposite transitions of same output | $tsk_{(p)}$ | $CL=50\text{ pF}$, $RL=500\Omega$ | | | 0.35 | ns |
| Propagation Delay IN to ON | tp_{LH}/tp_{HL} | $CL=50\text{ pF}$, $RL=500\Omega$ | 1.5 | | 3.8 | ns |
| Skew between outputs of different package at same power supply, temperature and speed grade | $tsk_{(t)}$ | $CL=50\text{ pF}$, $RL=500\Omega$ | | | 0.75 | ns |
| Output Rise Time 0.8 V to 2.0 V | $tr_{(o)}$ | $CL=50\text{ pF}$, $RL=500\Omega$ | | | 1.5 | ns |
| Output Fall Time 2.0 V to 0.8 V | $tf_{(o)}$ | $CL=50\text{ pF}$, $RL=500\Omega$ | | | 1.5 | ns |
| Duty Cycle Measured at $V_{DD}/2$ | DC | $CL=50\text{ pF}$, $RL=500\Omega$ | 45 | | 55 | % |
| Test Frequency | | | 1 | | 100 | MHz |



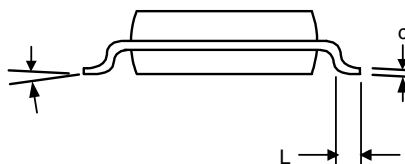
Package Outline and Package Dimensions (20-pin TSSOP, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches* | |
|--------|-------------|------|--------------|-------|
| | Min | Max | Min | Max |
| A | | 1.20 | | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 6.40 | 6.60 | 0.252 | 0.260 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

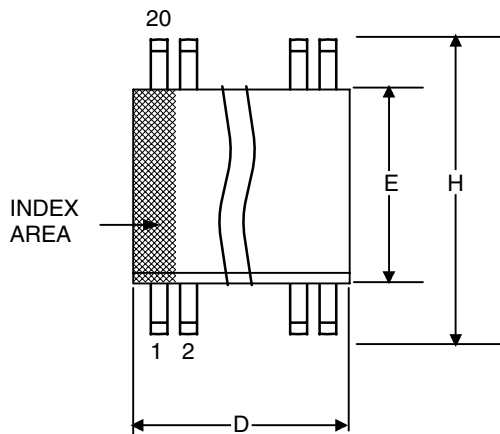
*For reference only. Controlling dimensions in mm.





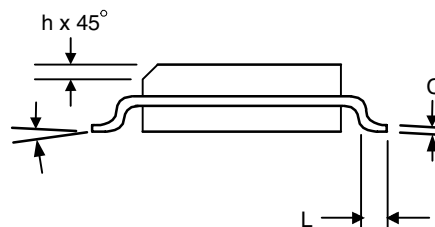
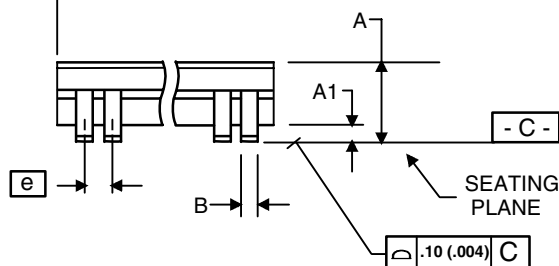
Package Outline and Package Dimensions (20-pin SOIC, 300Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches* | |
|----------|-------------|-------|-------------|------|
| | Min | Max | Min | Max |
| A | -- | 2.65 | -- | .104 |
| A1 | 0.10 | -- | .0040 | -- |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.18 | 0.32 | .007 | .013 |
| D | 12.60 | 13.00 | .496 | .512 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.25 | 0.75 | .010 | .029 |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |

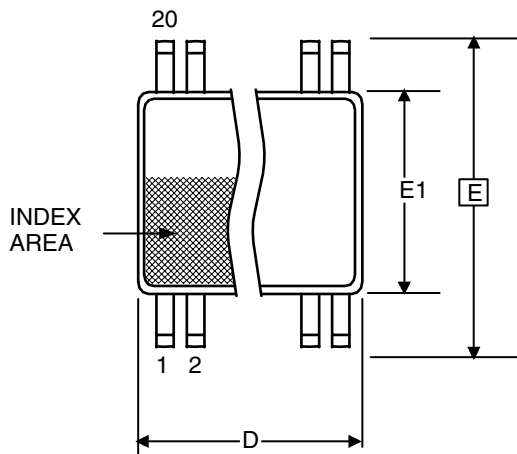
*For reference only. Controlling dimensions in mm.





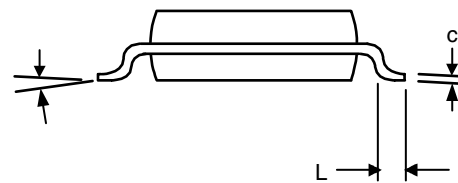
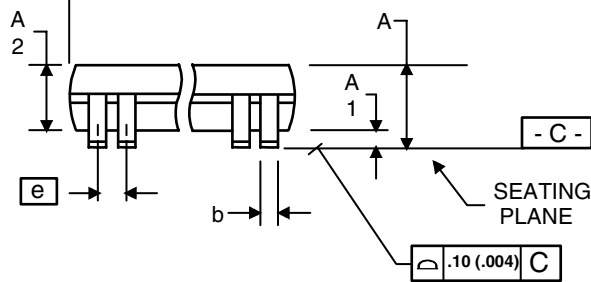
Package Outline and Package Dimensions (20 pin SSOP, 150Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches* | |
|----------|-------------|------|-------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.10 | 0.25 | .0040 | .010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| C | 0.18 | 0.25 | .007 | .010 |
| D | 8.55 | 8.75 | .337 | .344 |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 Basic | | 0.025 Basic | |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.





Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------------|--------------------|--------------|---------------|
| MK3807-01SI | MK3807-01SI | Tubes | 20-pin SOIC | -40 to +85° C |
| MK3807-01SIT | MK3807-01SI | Tape and Reel | 20-pin SOIC | -40 to +85° C |
| MK3807-01SILF | MK3807-01SILF | Tubes | 20-pin SOIC | -40 to +85° C |
| MK3807-01SILFT | MK3807-01SILF | Tape and Reel | 20-pin SOIC | -40 to +85° C |
| MK3807-01RI | MK3807-01RI | Tubes | 20-pin SSOP | -40 to +85° C |
| MK3807-01RIT | MK3807-01RI | Tape and Reel | 20-pin SSOP | -40 to +85° C |
| MK3807-01RILF | 3807-01RILF | Tubes | 20-pin SSOP | -40 to +85° C |
| MK3807-01RILFT | 3807-01RILF | Tape and Reel | 20-pin SSOP | -40 to +85° C |
| MK3807-01GI | 3807-01GI | Tubes | 20-pin TSSOP | -40 to +85° C |
| MK3807-01GIT | 3807-01GI | Tape and Reel | 20-pin TSSOP | -40 to +85° C |
| MK3807-01GILF | 380701GIL | Tubes | 20-pin TSSOP | -40 to +85° C |
| MK3807-01GILFT | 380701GIL | Tape and Reel | 20-pin TSSOP | -40 to +85° C |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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