

## 65,536 x 1-BIT DYNAMIC RAM MK4564(P/N/J/E)-12

### FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V ( $\pm 10\%$ ) supply operation
- On chip substrate bias generator for optimum performance
- Low power: 330 mW active, max  
22 mW standby, max
- 120 ns access time, 220 ns cycle time
- Extended  $D_{OUT}$  hold using  $\overline{CAS}$  control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5™ technology
- 128 refresh cycles (2 msec)  
Pin 9 is not needed for refresh

**IV**

### DESCRIPTION

The MK4564 is the new generation dynamic RAM. Organized 65,536 words by 1 bit, it is the successor to the industry standard MK4116. The MK4564 utilizes Mostek's Scaled Poly 5 process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permits the MK4564 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MK4564 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

The output of the MK4564 can be held valid up to 10  $\mu$ sec by holding  $\overline{CAS}$  active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

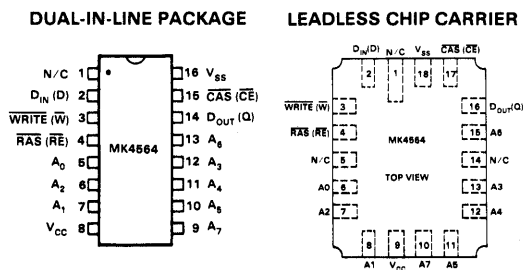
The 64K RAM from Mostek is the culmination of several years of circuit and process development, proven in predecessor products.

### PIN FUNCTIONS

$A_0$ - $A_7$	Address Inputs	$\overline{RAS}$ ( $\overline{RE}$ )	Row Address Strobe
$\overline{CAS}$ ( $\overline{CE}$ )	Column Address Strobe	$\overline{WRITE}$ ( $\overline{W}$ )	Read/Write Input
$D_{IN}$ (D)	Data In	$V_{CC}$	Power (5V)
$D_{OUT}$ (Q)	Data Out	$V_{SS}$	GND
		N/C	Not Connected

### PIN OUT

Figure 1



## ABSOLUTE MAXIMUM RATINGS\*

Voltage on $V_{CC}$ supply relative to $V_{SS}$ .....	-1.0 V to +7.0 V
Operating Temperature, $T_A$ (Ambient) .....	0°C to +70°C
Storage Temperature (Ceramic) .....	-65°C to +150°C
Storage Temperature (Plastic) .....	-55°C to +125°C
Power Dissipation .....	1 Watt
Short Circuit Output Current .....	50 mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤  $T_A$  ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	1
$V_{IH}$	Input High (Logic 1) Voltage, All Inputs	2.4	—	$V_{CC}+1$	V	1
$V_{IL}$	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1,18

## DC ELECTRICAL CHARACTERISTICS

(0°C ≤  $T_A$  ≤ 70°C) ( $V_{CC}$  = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$I_{CC1}$	OPERATING CURRENT Average power supply operating current ( $\overline{RAS}$ , $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min.)		60	mA	2
$I_{CC2}$	STANDBY CURRENT Power supply standby current ( $\overline{RAS} = V_{IH}$ , $D_{OUT} =$ High Impedance)		4	mA	
$I_{CC3}$	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ ; $t_{PC} = t_{PC}$ min.)		50	mA	2
$I_{CC4}$	PAGE MODE CURRENT Average power supply current, page mode operation ( $\overline{RAS} = V_{IL}$ , $t_{RAS} = t_{RAS}$ max., $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min.)		40	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ( $0 \text{ V} \leq V_{IN} \leq V_{CC}$ ), all other pins not under test = 0 volts	-10	10	$\mu\text{A}$	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current ( $D_{OUT}$ is disabled, $0 \text{ V} \leq V_{OUT} \leq V_{CC}$ )	-10	10	$\mu\text{A}$	
$V_{OH}$ $V_{OL}$	OUTPUT LEVELS Output High (Logic 1) voltage ( $I_{OUT} = -5 \text{ mA}$ ) Output Low (Logic 0) voltage ( $I_{OUT} = 4.2 \text{ mA}$ )	2.4	0.4	V V	

**NOTES:**

1. All voltages referenced to V<sub>SS</sub>.
2. I<sub>CC</sub> is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500 μs is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. Note that  $\overline{\text{RAS}}$  may be cycled during the initial pause.
4. AC characteristics assume  $t_T = 5$  ns.
5. V<sub>IH</sub> min. and V<sub>IL</sub> max. are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
7. Load = 2 TTL loads and 50 pF.
8. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ . If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table, t<sub>TRAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds the value shown.
9. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ .
10. t<sub>OFF</sub> max defines the time at which the output achieves the open circuit condition and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
11. Operation within the t<sub>RCD</sub>(max) limit permits t<sub>TRAC</sub>(max) to be met. t<sub>TRAC</sub>(max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub>(max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
12. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.
13. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WRITE}}$  leading edge in delayed write or read-modify-write cycles.
14. t<sub>WCS</sub>, t<sub>CWD</sub>, and t<sub>RWD</sub> are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If t<sub>WCS</sub> ≥ t<sub>WCS</sub>(min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If t<sub>CWD</sub> ≥ t<sub>CWD</sub>(min) and t<sub>RWD</sub> ≥ t<sub>RWD</sub>(min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until  $\overline{\text{CAS}}$  goes back to V<sub>IH</sub>) is indeterminate.
15. In addition to meeting the transition rate specification, all input signals must transmit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
16. Effective capacitance calculated from the equation  $C = I \frac{\Delta t}{\Delta V}$  with  $\Delta V = 3$  volts and power supply at nominal level.
17.  $\overline{\text{CAS}} = V_{IH}$  to disable D<sub>OUT</sub>.
18. Includes the DC level and all instantaneous signal excursions.
19. WRITE = don't care. Data out depends on the state of  $\overline{\text{CAS}}$ . If  $\overline{\text{CAS}} = V_{IH}$ , data output is high impedance. If  $\overline{\text{CAS}} = V_{IL}$ , the data output will contain data from the last valid read cycle.



**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(3,4,5,15) (0°C ≤ T<sub>A</sub> ≤ 70°C), V<sub>CC</sub> = 5.0 V ± 10%

SYMBOL		PARAMETER	MK4564-12		UNITS	NOTES
STD	ALT		MIN	MAX		
t <sub>RELREL</sub>	t <sub>RC</sub>	Random read or write cycle time	220		ns	6,7
t <sub>RELREL</sub> (RMW)	t <sub>RMW</sub>	Read-modify-write cycle time	260		ns	6,7
t <sub>RELREL</sub> (PC)	t <sub>PC</sub>	Page mode cycle time	145		ns	6,7
t <sub>RELQV</sub>	t <sub>RAC</sub>	Access time from $\overline{\text{RAS}}$		120	ns	7,8
t <sub>CELQV</sub>	t <sub>CAC</sub>	Access time from $\overline{\text{CAS}}$		75	ns	7,9
t <sub>CEHOZ</sub>	t <sub>OFF</sub>	Output buffer turn-off delay	0	40	ns	10
t <sub>T</sub>	t <sub>T</sub>	Transition time (rise and fall)	3	50	ns	5,15
t <sub>REHREL</sub>	t <sub>RP</sub>	$\overline{\text{RAS}}$ precharge time	90		ns	
t <sub>RELREH</sub>	t <sub>RAS</sub>	$\overline{\text{RAS}}$ pulse width	120	10,000	ns	
t <sub>CELREH</sub>	t <sub>RSH</sub>	$\overline{\text{RAS}}$ hold time	75		ns	
t <sub>RELCEH</sub>	t <sub>CSH</sub>	$\overline{\text{CAS}}$ hold time	120		ns	
t <sub>CELCEH</sub>	t <sub>CAS</sub>	$\overline{\text{CAS}}$ pulse width	75	10,000	ns	
t <sub>RELCEL</sub>	t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	15	45	ns	11
t <sub>REHWX</sub>	t <sub>RRH</sub>	Read command hold time referenced to $\overline{\text{RAS}}$	10		ns	12
t <sub>AVREL</sub>	t <sub>ASR</sub>	Row address set-up time	0		ns	
t <sub>RELAX</sub>	t <sub>RAH</sub>	Row address hold time	15		ns	
t <sub>AVCEL</sub>	t <sub>ASC</sub>	Column address set-up time	0		ns	
t <sub>CELAX</sub>	t <sub>CAH</sub>	Column address hold time	15		ns	
t <sub>RELA(C)X</sub>	t <sub>AR</sub>	Column address hold time referenced to $\overline{\text{RAS}}$	70		ns	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**  
 (3,4,5,15) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ),  $V_{CC} = 5.0\text{ V} \pm 10\%$

SYMBOL		PARAMETER	MK4564-12		UNITS	NOTES
STD	ALT		MIN	MAX		
$t_{WHCEL}$	$t_{RCS}$	Read command set-up time	0		ns	
$t_{CEHWX}$	$t_{RCH}$	Read command hold time referenced to $\overline{\text{CAS}}$	0		ns	12
$t_{CELWX}$	$t_{WCH}$	Write command hold time	30		ns	
$t_{RELWX}$	$t_{WCR}$	Write command hold time referenced to $\overline{\text{RAS}}$	75		ns	
$t_{WLWH}$	$t_{WP}$	Write command pulse width	15		ns	
$t_{WLREH}$	$t_{RWL}$	Write command to $\overline{\text{RAS}}$ lead time	35		ns	
$t_{WLCEH}$	$t_{CWL}$	Write command to $\overline{\text{CAS}}$ lead time	35		ns	
$t_{DVCEL}$	$t_{DS}$	Data-in set-up time	0		ns	13
$t_{CELDX}$	$t_{DH}$	Data-in hold time	30		ns	13
$t_{RELDX}$	$t_{DHR}$	Data-in hold time referenced to $\overline{\text{RAS}}$	75		ns	
$t_{CEHCEL}$ (PC)	$t_{CP}$	$\overline{\text{CAS}}$ precharge time (for page-mode cycle only)	60		ns	
$t_{RVRV}$	$t_{REF}$	Refresh Period		2	ms	
$t_{WLCEL}$	$t_{WCS}$	$\overline{\text{WRITE}}$ command set-up time	0		ns	14
$t_{CELWL}$	$t_{CWD}$	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	50		ns	14
$t_{RELWL}$	$t_{RWD}$	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	95		ns	14
$t_{CEHCEL}$	$t_{CPN}$	$\overline{\text{CAS}}$ precharge time	25		ns	

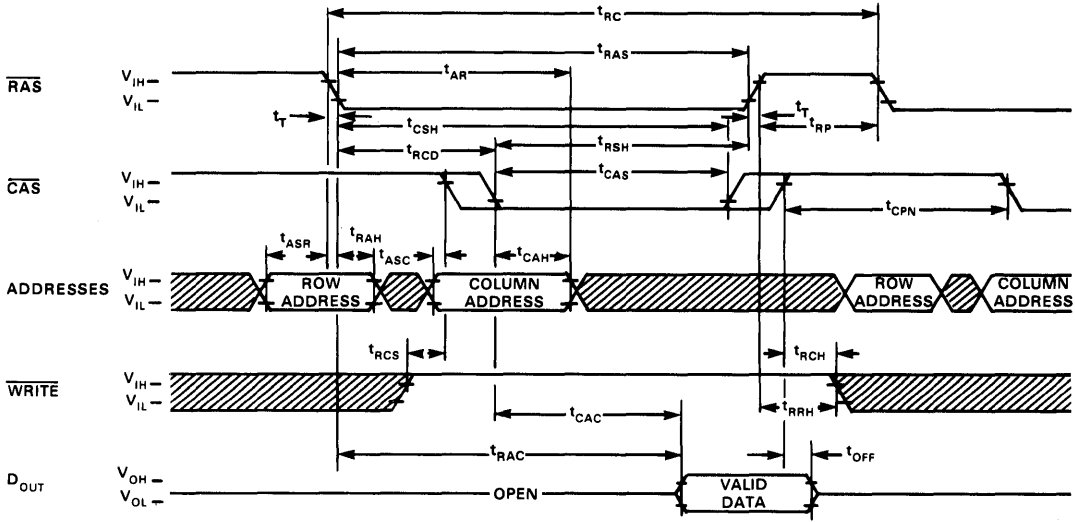
**AC ELECTRICAL CHARACTERISTICS**

( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ) ( $V_{CC} = 5.0\text{ V} \pm 10\%$ )

SYM	PARAMETER	MAX	UNITS	NOTES
$C_{I1}$	Input Capacitance ( $A_0 - A_7$ ), $D_{IN}$	5	pF	16
$C_{I2}$	Input Capacitance $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$	10	pF	16
$C_O$	Output Capacitance ( $D_{OUT}$ )	7	pF	16,17

## READ CYCLE

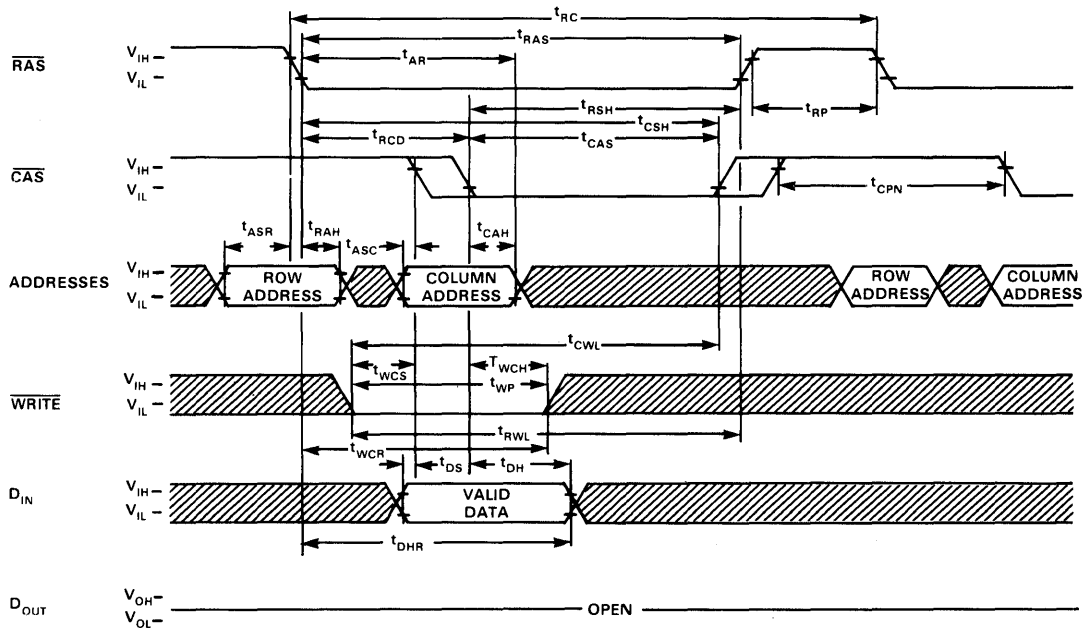
Figure 2



IV

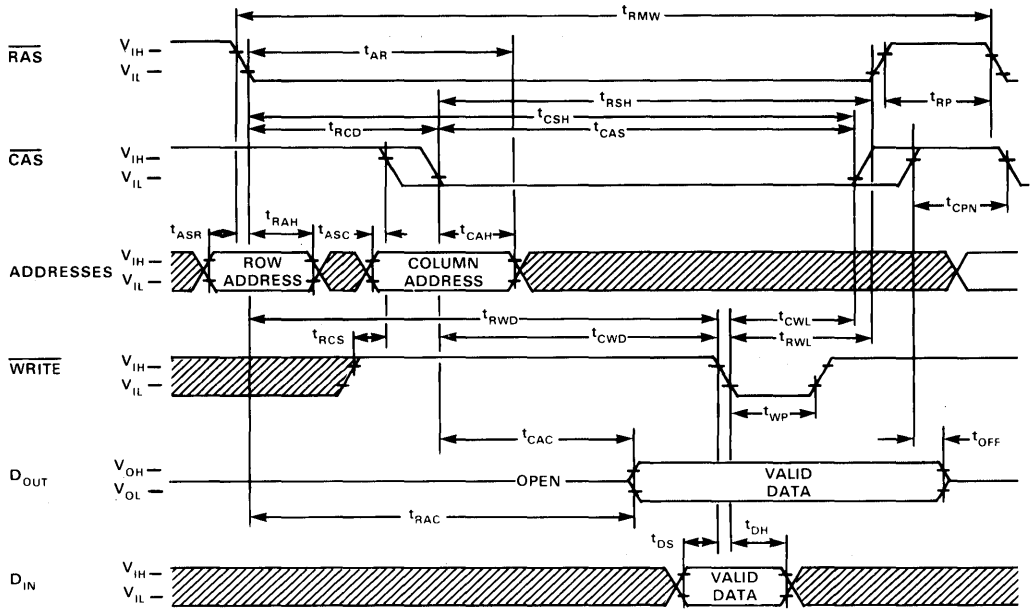
## WRITE CYCLE (EARLY WRITE)

Figure 3



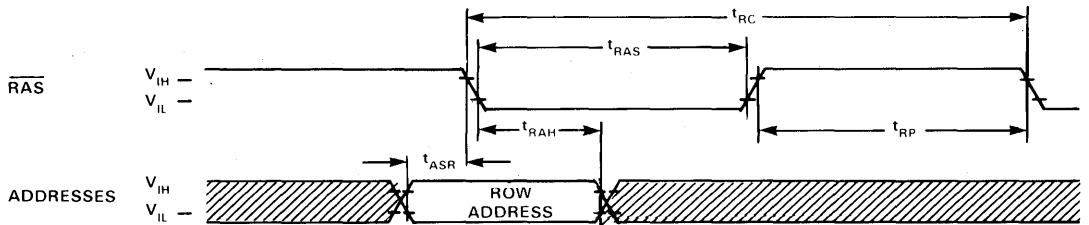
# READ-WRITE/READ-MODIFY-WRITE CYCLE

Figure 4



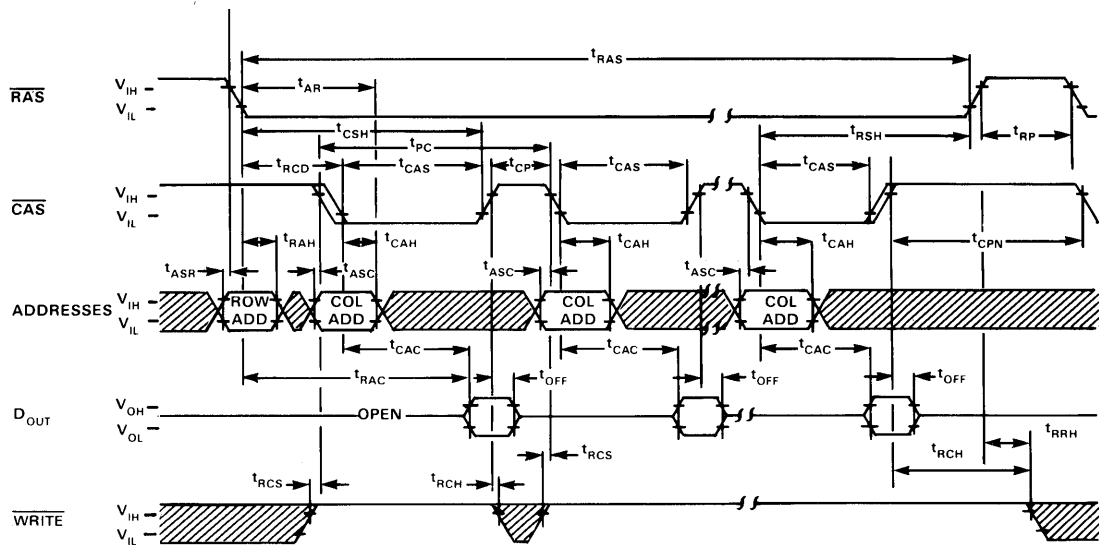
# "RAS-ONLY" REFRESH CYCLE

Figure 5



## PAGE MODE READ CYCLE

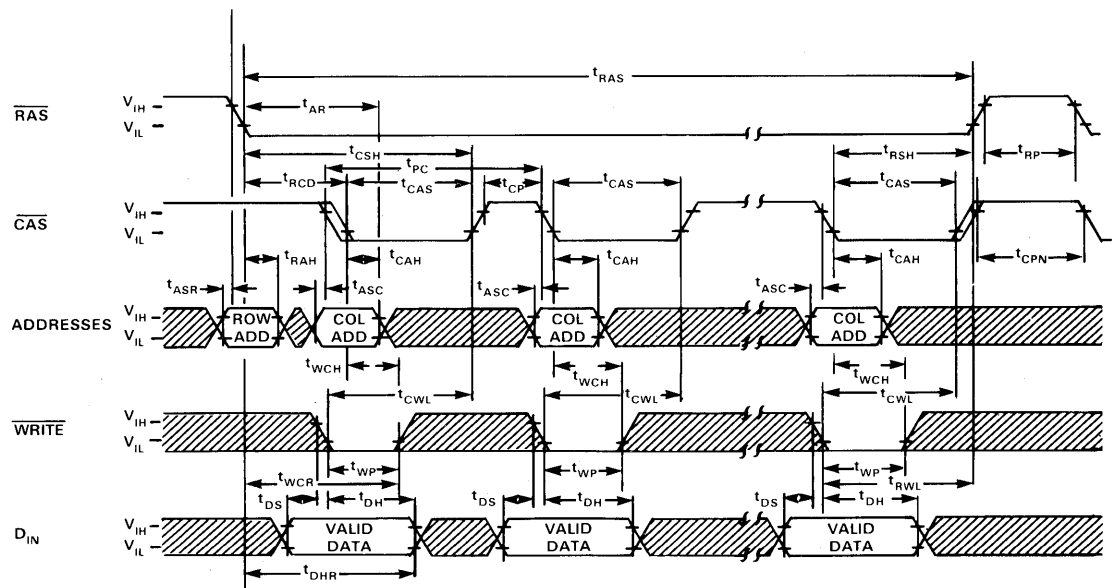
Figure 6



IV

## PAGE MODE WRITE CYCLE

Figure 7



## OPERATION

The eight address bits required to decode 1 of the 65,536 cell locations within the MK4564 are multiplexed onto the eight address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ( $\overline{RAS}$ ), latches the eight row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ( $\overline{CAS}$ ), subsequently latches the eight column addresses into the chip. Each of these signals,  $\overline{RAS}$  and  $\overline{CAS}$ , triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the  $\overline{CAS}$  clock sequence are inhibited until the occurrence of a delayed signal derived from the  $\overline{RAS}$  clock chain. This "gated  $\overline{CAS}$ " feature allows the  $\overline{CAS}$  clock to be externally activated as soon as the Row Address Hold specification ( $t_{RAH}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated  $\overline{CAS}$ " feature permits  $\overline{CAS}$  to be activated at any time after  $t_{RAH}$  and it will have no effect on the worst case data access time ( $t_{RAC}$ ) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of  $\overline{CAS}$  which are called  $t_{RCD}$  (min) and  $t_{RCD}$  (max). No data storage or reading errors will result if  $\overline{CAS}$  is applied to the MK4564 at a point in time beyond the  $t_{RCD}$  (max) limit. However, access time will then be determined exclusively by the access time from  $\overline{CAS}$  ( $t_{CAC}$ ) rather than from  $RAS$  ( $t_{RAC}$ ), and  $RAS$  access time will be lengthened by the amount that  $t_{RCD}$  exceeds the  $t_{RCD}$  (max) limit.

## DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of  $\overline{WRITE}$  and  $\overline{CAS}$  while  $RAS$  is active. The latter of  $\overline{WRITE}$  or  $\overline{CAS}$  to make its negative transition is the strobe for the Data In ( $D_{IN}$ ) register. This permits several options in the write cycle timing. In a write cycle, if the  $\overline{WRITE}$  input is brought low (active) prior to  $\overline{CAS}$  being brought low (active), the  $D_{IN}$  is strobed by  $\overline{CAS}$ , and the Input Data set-up and hold times are referenced to  $\overline{CAS}$ . If the input data is not available at  $\overline{CAS}$  time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the  $\overline{WRITE}$  signal should be delayed until after  $\overline{CAS}$  has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of  $\overline{WRITE}$  rather than  $\overline{CAS}$ .

Data is retrieved from the memory in a read cycle by maintaining  $\overline{WRITE}$  in the inactive or high state throughout the portion of the memory cycle in which both the  $\overline{RAS}$  and  $\overline{CAS}$  are low (active). Data read from the selected cell is available at the output port within the specified access time.

The output data is the same polarity (not inverted) as the input data.

## DATA OUTPUT CONTROL

The normal condition of the Data Output ( $D_{OUT}$ ) of the MK4564 is the high impedance (open-circuit) state; anytime  $\overline{CAS}$  is high (inactive) the  $D_{OUT}$  pin will be floating. Once the output data port has gone active, it will remain valid until  $\overline{CAS}$  is taken to the precharge (inactive high) state.

## PAGE MODE OPERATION

The Page Mode feature of the MK4564 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the  $\overline{RAS}$  signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at  $t_{RAC}$  or  $t_{CAC}$  time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at  $t_{CAC}$  time (referenced to  $\overline{CAS}$ ). With the MK4564 this results in approximately a 45% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4564 is limited to the 256 column locations determined by all combinations of the eight column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

## REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "RAS-only" cycles.

The  $\overline{RAS}$ -only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when  $\overline{RAS}$  goes low (active). The state of the output data port during a  $\overline{RAS}$ -only refresh is controlled by  $\overline{CAS}$ . If  $\overline{CAS}$  is high (inactive) during the entire time that  $\overline{RAS}$  is asserted, the output will remain in the high impedance state. If  $\overline{CAS}$  is low (active) the entire time the  $\overline{RAS}$  is asserted, the output port will remain in the same state that it was prior to the issuance of the  $\overline{RAS}$  signal. If  $\overline{CAS}$  makes a low-to-high transition during the  $\overline{RAS}$ -only refresh cycle, the output data buffer will assume the high impedance state. However, the  $\overline{CAS}$  may not make a high to low transition during the  $\overline{RAS}$ -only refresh cycle since the device interprets this as a normal  $RAS/\overline{CAS}$  (read or write) type cycle.



## HIDDEN REFRESH

A  $\overline{\text{RAS}}$ -only refresh cycle may take place while maintaining valid output data by extending the  $\overline{\text{CAS}}$  active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

### HIDDEN REFRESH CYCLE (SEE NOTE 19)

