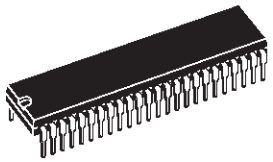
MK50H28

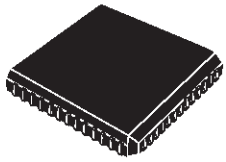
MULTI LOGICAL LINK FRAME RELAY CONTROLLER

SECTION 1 - FEATURES

- Based on ITU Q.933 Annex A and T1.617 Annex D Standards for Frame Relay Service and Additional Pocedures for Permanent Virtual Circuits(PVCs).
- Optional Transparent Mode (no LMI Protocol Processing - all frame data received).
- Local Management Link Protocol with optional Bi-directional message processing.
- Detects and indicates service-affecting errors in the timing or content of events.
- Programmable Timers/Counters: nT1/T391, nT2/T392, nN1/N391, nN2/N392, nN3/N393 and dN1 for the LMI/LIV channel.
- Provides Error Counters for the LMI channel and Congestion Statistics for all the active channels.
- LMI/LIV Frames can be transmitted/received on DLCI 0 or 1023.
- Supports reception of up to 4 octets of address field with a maximum of 8192 active channels or DLCIs (Data Link Connection Identifiers)
- Priority DLCI scheme for channels requiring higher rate of service.
- Buffer Management includes:
  - Initialization Block
  - Address Look Up Table
- - Context Table
  - Separate Receive and Transmit Rings of variable size for each active channel
- On chip DMA control with programmable burst length.
- Handles all HDLC frame formatting:
  - Zero bit insertion and deletion
  - FCS (CRC) generation and detection
  - Frame delimiting with flags
- Programmable minimum frame spacing on transmission (1-62 flags between frames).
- Selectable FCS (CRC) of 16 or 32 bits.
- Testing Facilities: Internal Loopback, Silent Loopback, Clockless Loopback, and Self Test.
- System clock rates up to 25 MHz.
- CMOS process; Fully compatible with both 8 and 16 bit systems; All inputs and outputs are TTL compatible.
- Programmable for full or half duplex operation.



DIP48



PLCC52

- Pin-for-pin compatible and architecturally the same as the MK50H25 (X.25/LAPD) and MK50H27 (CCS#7).

SECTION 2 - DESCRIPTION

The STMicroelectronics MK50H28 Multi-Logical Link Communications Controller is a CMOS VLSI device which provides link level data communications control for Frame Relay Applications on Permanent Virtual Circuits (PVCs). The MK50H28 will perform frame formating including: frame delimiting with flags, transparency (so-called ”bit-stuffing”), plus FCS (CRC) generation and detection. It also supports Local Management Interface (LMI) protocol with the ”Optional Bidirectional Procedures” (Annex D, T1.617 - 1991 and T1.617a-1994).

One of the outstanding features of the MK50H28 is its buffer management which includes on-chip dual channel DMA. This feature allows users to receive and transmit multiple data frames at a time. (A conventional serial communications control chip plus a separate DMA chip would handle data for only a single block at a time.) The

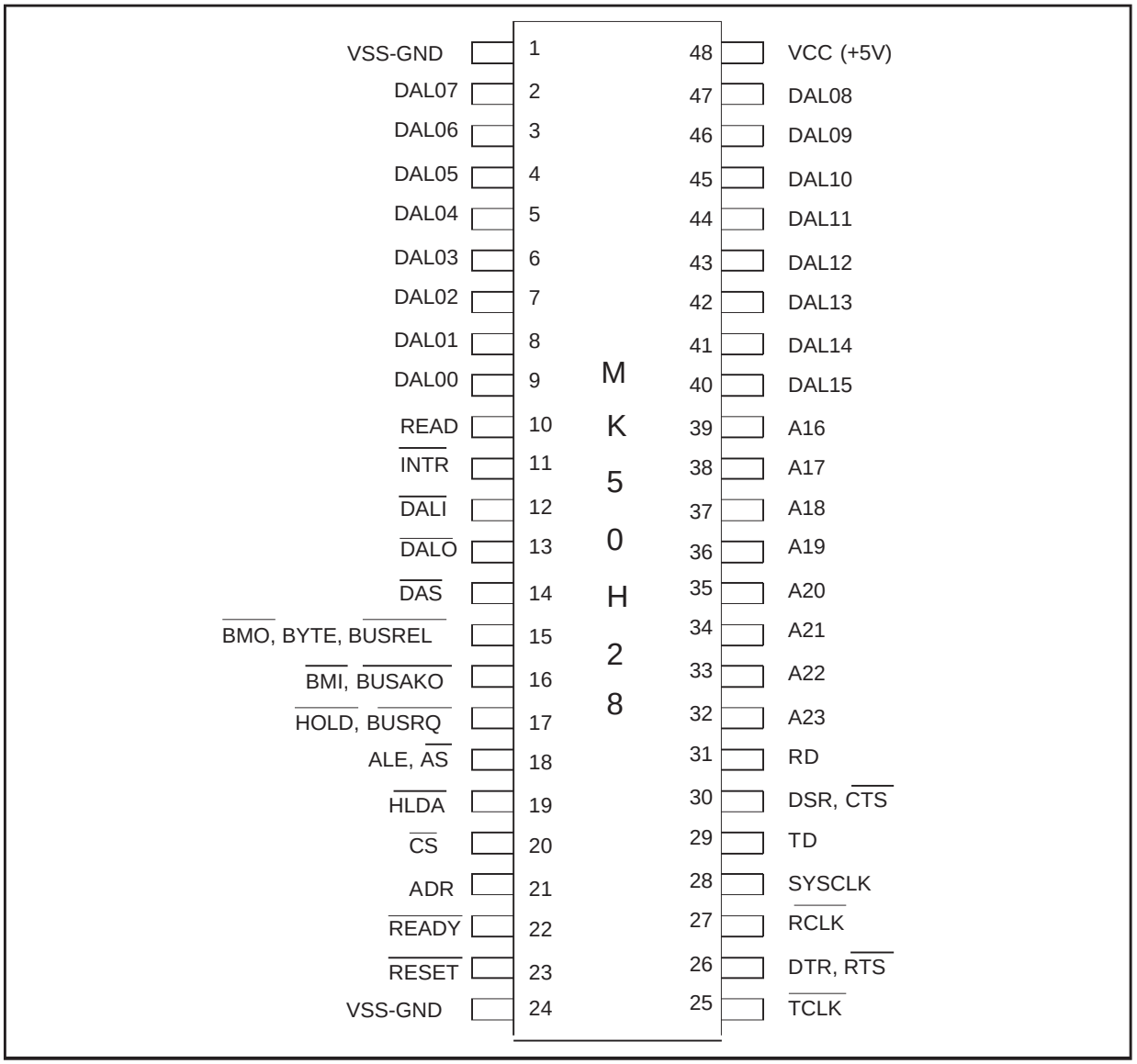
DESCRIPTION (Continued)

MK50H28 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. Moreover, the memory management capability includes the chaining of long frames. A possible system configuration for the MK50H28 is shown in Figure 1.

The MK50H28 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI- 11, 8086, 8088, 8080, etc.

The MK50H28 may be operated in either full or half duplex mode. In half duplex mode, the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins. All signal pins on the MK50H28 are TTL compatible. This has the advantage of making the MK50H28 independent of the physical interface. As shown in Figure 1, line drivers and receivers are used for electrical connection to the physical layer.

DIP48 PIN CONNECTION (Top view)



PLCC52 PIN CONNECTION (Top view)

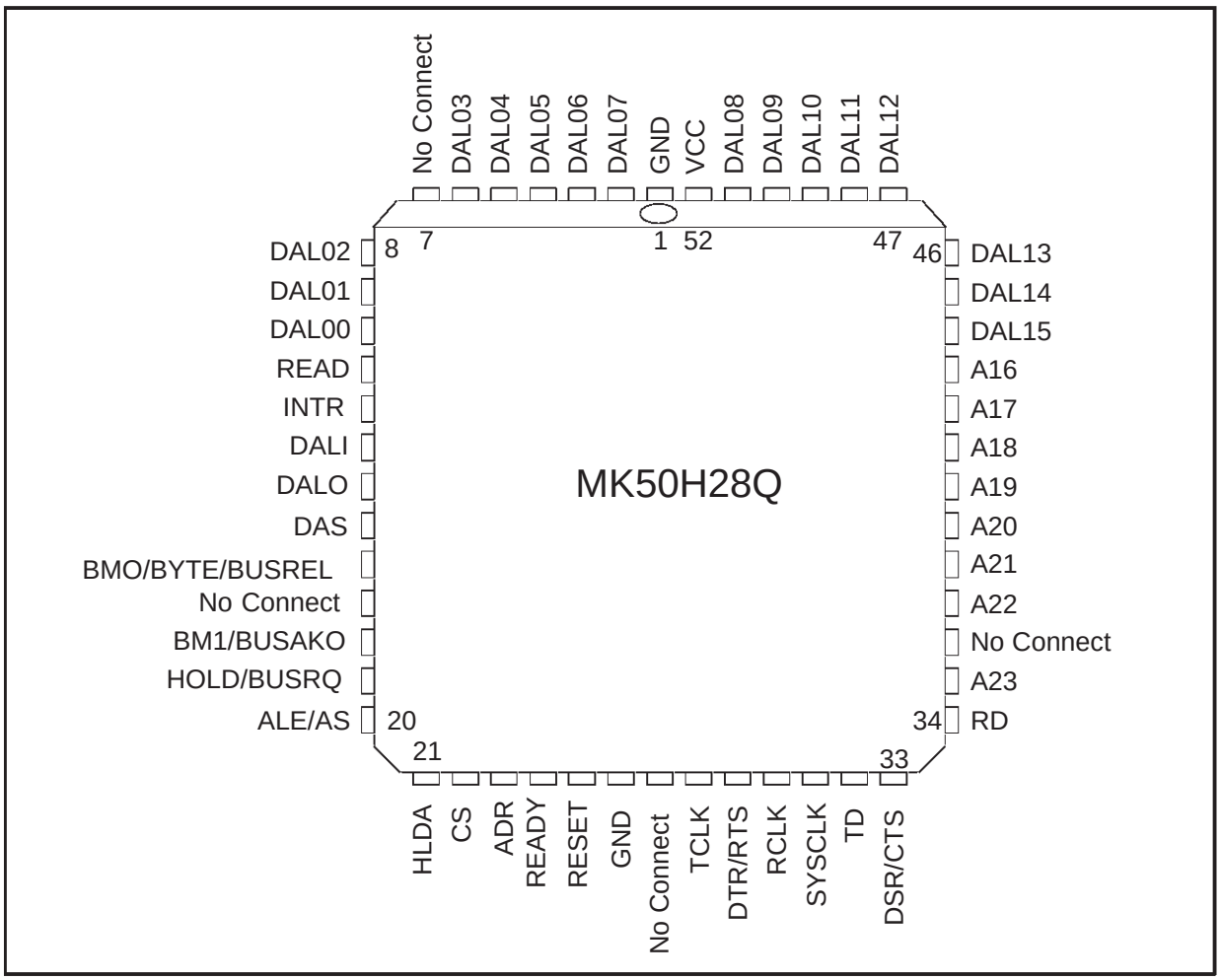


TAble 1 - PIN DESCRIPTION

LEGEND:

I	Input only	O	Output only
IO	Input / Output	3S	3-State
OD	Open Drain (no internal pull-up)		

Note: Pin out for 52 pin PLCC is shown in brackets.

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
DAL<15:00>	2-9 40-47 [2-10 44-51]	IO/3S	The time multiplexed Data/Address bus. During the address portion of a memory transfer, DAL<15:00> contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer.
READ	10 [11]	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK50H28 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times. MK50H28 as a Bus Slave : READ = HIGH - Data is placed on the DAL lines by the chip. READ = LOW - Data is taken off the DAL lines by the chip. MK50H28 as a Bus Master : READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip.
$\overline{\text{INTR}}$	11 [12]	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.
$\overline{\text{DALI}}$	12 [13]	O/3S	DAL IN is an external bus transceiver control line. $\overline{\text{DALI}}$ is driven by the MK50H28 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by the MK50H28 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.
$\overline{\text{DALO}}$	13 [14]	O/3S	DAL OUT is an external bus transceiver control line. DALO is driven by the MK50H28 only while it is the BUS MASTER. DALO is asserted by the MK50H28 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
$\overline{\text{DAS}}$	14 [15]	IO/3S	DATA STROBE defines the data portion of a bus transaction. By definition, data is stable and valid at the low to high transition of DAS. This signal is driven by the MK50H28 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated.
$\overline{\text{BMO}}$ BYTE BUSREL	15 [16]	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input BUSREL and is used by the host to signal the MK50H28 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear then pin 15 is an output and behaves as described below for pin 16.
$\overline{\text{BM1}}$ BUSAKO	16 [18]	O/3S	Pins 15 and 16 are programmable through bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0, I/O PIN 15 = BMO (O/3S) I/O PIN 16 = $\overline{\text{BM1}}$ (O/3S) BYTE MASK<1:0> Indicates the byte(s) on the DAL to be read or written during this bus transaction. MK50H28 drives these lines only as a Bus Master. MK50H28 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table. $\overline{\text{BM1}}$ $\overline{\text{BM0}}$ TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH UPPER BYTE (DAL<15:08>) HIGH LOW LOWER BYTE (DAL<07:00>) HIGH HIGH NONE

Table 1: PIN DESCRIPTION (continued)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			If CSR4<00> BCON = 1, I/O PIN 15 = BYTE (O/3S) I/O PIN 16 = BUSAKO (O) Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK50H28 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table. BYTE DAL<00> TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH ILLEGAL CONDITION HIGH LOW LOWER BYTE HIGH HIGH UPPER BYTE BUSAKO is a bus request daisy chain output. If MK50H28 is not requesting the bus and it receives HLDA, BUSAKO will be driven low. If MK50H28 is requesting the bus when it receives HLDA, BUSAKO will remain high Note: All transfers are entire word unless the MK50H28 is configured for 8 bit operation.
$\overline{\text{HOLD}}$ BUSRQ	17 [19]	IO/OD	Pin 17 is configured through bit 0 of CSR4. If CSR4<00> BCON = 0, I/O PIN 17 = HOLD HOLD request is asserted by MK50H28 when it requires a DMA cycle, if HLDA is inactive, regardless of the previous state of the HOLD pin. HOLD is held low for the entire ensuing bus transaction. If CSR4<00> BCON = 1, I/O PIN 17 = $\overline{\text{BUSRQ}}$ $\overline{\text{BUSRQ}}$ is asserted by MK50H28 when it requires a DMA cycle if the prior state of the $\overline{\text{BUSRQ}}$ pin was high and HLDA is inactive. BUSRQ is held low for the entire ensuing bus transaction.
ALE $\overline{\text{AS}}$	18 [20]	O/3S	The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK50H28 while it is the BUS MASTER. At all other times, the signal is tristated. If CSR4<01> ACON = 0, I/O PIN 18 = ALE ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. If CSR4<01> ACON = 1, I/O PIN 18 = $\overline{\text{AS}}$ As $\overline{\text{AS}}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{\text{AS}}$ can be used by a slave device to strobe the address into a register. $\overline{\text{AS}}$ is effectively the inversion of ALE.
$\overline{\text{HLDA}}$	19 [21]	I	HOLD ACKNOWLEDGE is the response to HOLD. When $\overline{\text{HLDA}}$ is low in response to MK50H28's assertion of $\overline{\text{HOLD}}$, the MK50H28 is the Bus Master. $\overline{\text{HLDA}}$ should be deasserted ONLY after $\overline{\text{HOLD}}$ has been released by the MK50H28.
$\overline{\text{CS}}$	20 [22]	I	CHIP SELECT indicates, when low, that the MK50H28 is the slave device for the data transfer. CS must be valid throughout the entire transaction.
ADR	21 [23]	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{\text{CS}}$ is low. ADR PORT LOW REGISTER DATA PORT HIGH REGISTER ADDRESS PORT
$\overline{\text{READY}}$	22 [24]	IO/OD	When the MK50H28 is a Bus Master, READY is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle.

Table 1: PIN DESCRIPTION (continued)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			As a Bus Slave, the MK50H28 asserts $\overline{\text{READY}}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. $\overline{\text{READY}}$ is a response to $\overline{\text{DAS}}$ and it will be released after $\overline{\text{DAS}}$ or $\overline{\text{CS}}$ is negated.
$\overline{\text{RESET}}$	23 [25]	I	RESET is the Bus signal that will cause MK50H28 to cease operation, clear its internal logic and enter an idle state with the Power Off bit of CSR0 set.
$\overline{\text{TCLK}}$	25 [28]	I	TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of TCLK. The frequency of $\overline{\text{TCLK}}$ may not be greater than the frequency of SYSCL
DTR / $\overline{\text{RTS}}$	26 [29]	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output RTS or as programmable IO pin DTR. If configured as $\overline{\text{RTS}}$, the MK50H28 will assert this pin if it has data to send and throughout the transmission of a signal unit.
$\overline{\text{RCLK}}$	27 [30]	I	RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of RCLK. The frequency of $\overline{\text{RCLK}}$ may not be greater than the frequency of SYSCLK.
SYSCLK	28 [31]	I	SYSTEM CLOCK. System clock used for internal timing of the MK50H28. SYSCLK should be as defined in the Electrical Specifications in Section 5.
TD	29 [32]	O	TRANSMIT DATA. Transmit serial data output.
DSR / $\overline{\text{CTS}}$	30 [33]	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{\text{CTS}}$ or as programmable IO pin DSR. If configured as $\overline{\text{CTS}}$, the MK50H28 will transmit all ones while $\overline{\text{CTS}}$ is high.
RD	31 [34]	I	RECEIVE DATA. Received serial data input.
A<23:16>	32-39 [37-43]	o/3s	Address bits <23:16> used in conjunction with DAL<15:00> to produce a 24 bit address. MK50H28 drives these lines only as a Bus Master. A23-A20 may be driven continuously as described in the CSR4<7> BAE bit.
VSS-GND	1,24 [1,26]		Ground Pins
VCC	48 [52]		Power Supply Pin +5.0 VDC ± 5%

SECTION 3
OPERATIONAL DESCRIPTION

The STMicroelectronics MK50H28 Multi-Logical Link Communications Controller device is a VLSI product intended for high performance data communication applications requiring Frame Relay Service on Permanent Virtual Circuits. The MK50H28 will perform all frame formatting, such as: frame delimiting with flags, FCS (CRC) generation and detection, and zero bit insertion and deletion for transparency. The MK50H28 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple frames for each active channel or DLCI. Contained in the buffer management is an on-chip dual channel DMA: one channel for receive and one channel for transmit.

The MK50H28 can be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK50H28 is shown in Figure 1. This document assumes that the processor has a byte addressable memory organization.

The MK50H28 will move multiple blocks of receive and transmit data directly in and out of memory through the Host's bus.

The MK50H28 may be operated in full or half duplex mode. In half duplex mode the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins.

All signal pins on the MK50H28 are TTL compatible. This has the advantage of making the MK50H28 independent of the physical interface. As shown in Fig. 1, line drivers and receivers are used for electrical connection to the physical layer.

Figure 1: Possible System Configuration for the MK50H28

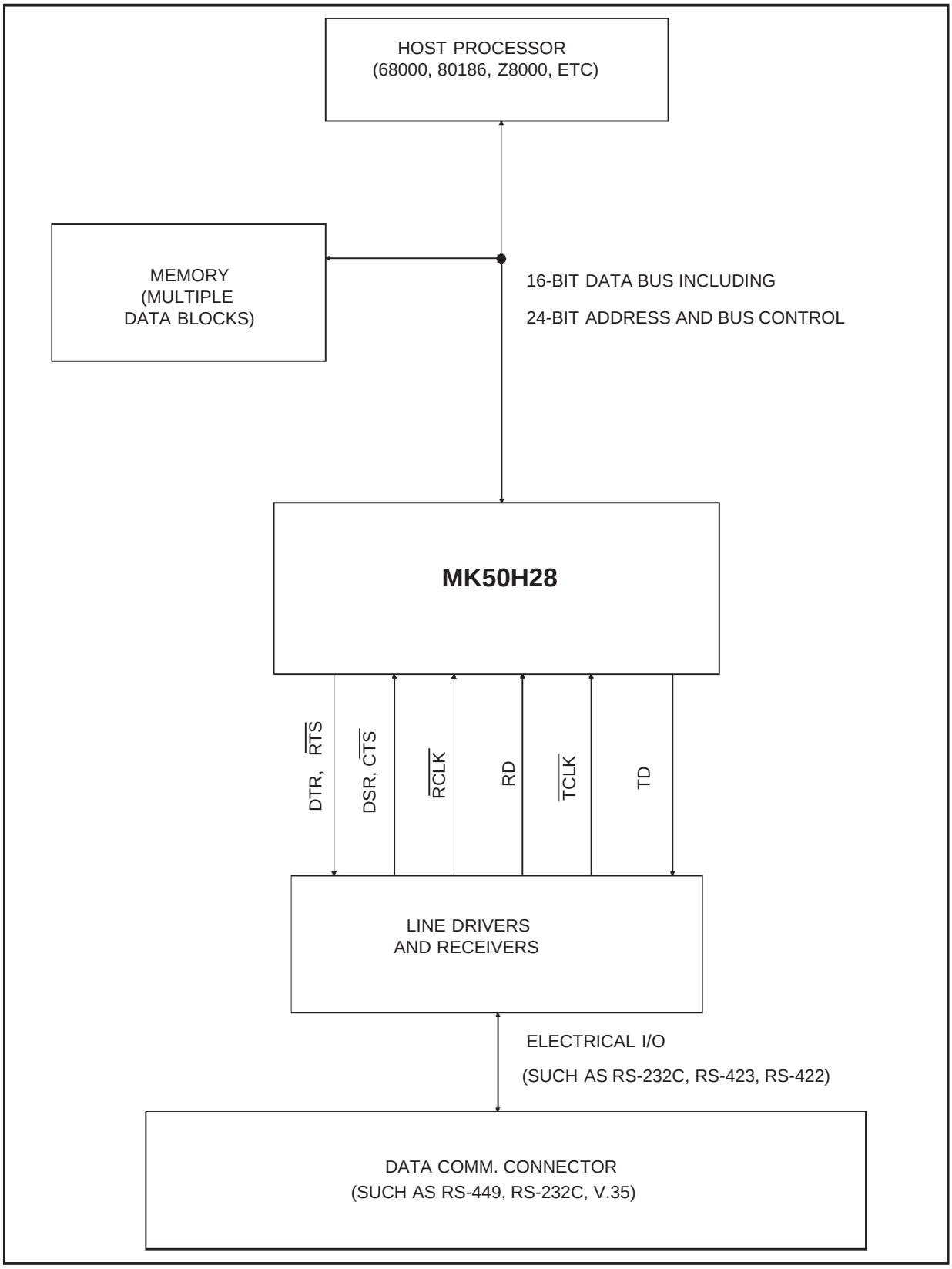
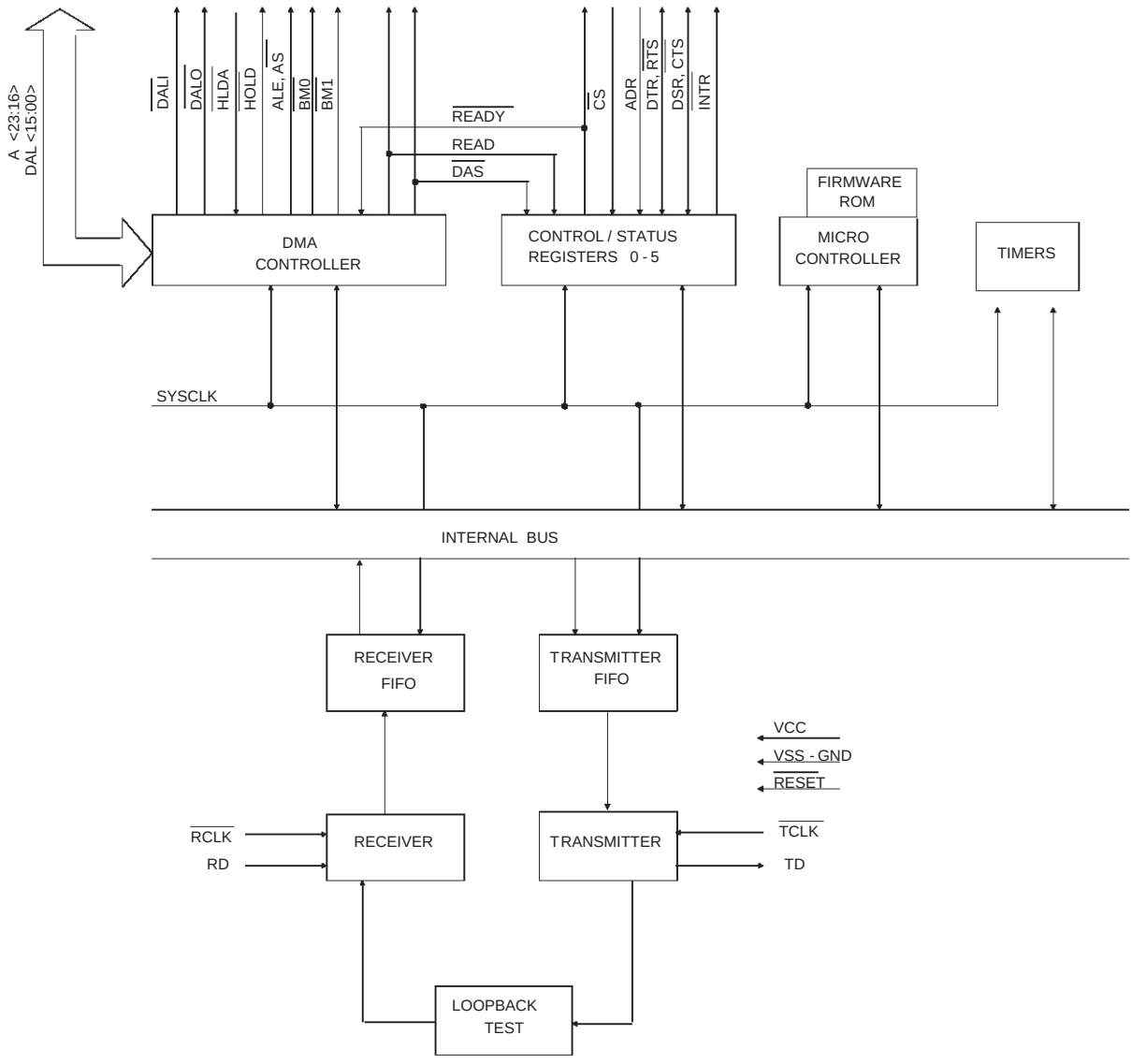


Figure 2: MK50H28 Simplified Block Diagram



3.1 Functional Blocks

Refer to the block diagram in Figure 2.

The MK50H28 is primarily initialized and controlled through six 16-bit Control and Status Registers (CSR0 thru CSR5). The CSR's are accessed through two bus addressable ports, the Register Address Port (RAP), and the Register Data Port (RDP). The MK50H28 may also generate an interrupt(s) to the Host. These interrupts are enabled and disabled through CSR0.

The on-chip microcontroller is used to control the movement of parallel receive and transmit data, and to handle the Address field filtering.

3.1.1 Microcontroller

The microcontroller controls all of the other blocks of the MK50H28. The microcontroller performs frame processing and protocol processing. All primitive processing and generation is also done here. The microcode ROM contains the control program of the microcontroller.

3.1.2 Receiver

Serial receive data comes into the Receiver (Figure 2). The Receiver is responsible for:

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good and bad FCS (CRC).
5. Monitoring Receiver FIFO status.
6. Detection of Receiver Over-Run.
7. Odd byte detection.

NOTE: If frames are received that have an odd number of bytes then the last byte of the frame is said to be an odd byte.

8. Detection of non-octet aligned frames. Such frames are treated as invalid frames.

3.1.3 Transmitter

The Transmitter is responsible for:

1. Serialization of outgoing data.
2. Generating and appending the FCS (CRC).
3. Framing the outgoing frame with flags.
4. Zero bit insertion for transparency.
5. Transmitter Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS control.

3.1.4 Frame Check Sequence or Cyclic Redundancy Check

The FCS (CRC) on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual FCS computation circuits. The characteristics of the FCS are:

Transmitted Polarity: Inverted

Transmitted Order: High Order Bit First

Pre-set Value: All 1's

Polynomial 16 bit:

$$X^{16} + X^{12} + X^5 + 1$$

Remainder 16 bit (if received correctly):
High order bit-->0001 1101 0000 1111

Polynomial 32 bit:

$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

Remainder 32 bit (if received correctly):
high order bit-->1100 0111 0000 0100
1101 1101 0111 1011

3.1.5 Receive FIFO

The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microcontroller until it contains enough data to reach the watermark level. This watermark level can be programmed in CSR4 to occur when the FIFO contains at least 18 or more bytes; 34 or more bytes; or 50 or more bytes. This programmability , along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK50H28 must use the host bus. For more information, see Control/Status Register 4.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK50H28 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

3.1.6 Transmit FIFO

The Transmit FIFO buffers the data to be transmitted by the MK50H28. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to burst read data from the host's memory buffers; making both the MK50H28 and the host bus more efficient.

3.1.7 DMA Controller

The MK50H28 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK50H28 requires access to the host memory it will negotiate for mastership of the bus. Upon gaining control of the bus the MK50H28 will begin transferring data to or from memory. The MK50H28 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the BUSREL pin is driven low. In any case, it will complete the current bus transfer before releasing bus mastership back to the host. If during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK50H28 will release ownership of the bus immediately and the MERR bit will be set in CSR0. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode the limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode,it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1 Mbps) a burst limit of 8 words, 16 bytes or unlimited is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed separately for data and control information. Data information is defined as all contents of data buffers; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see section 4.1.2.5 on Control and Status Register 4.

3.1.8 Bus Slave Circuitry

The MK50H28 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave. The contents of these registers are listed in Section 4 and bus signal timing is described in Figures 13 and 14.

3.2 Memory/Buffer Management Overview

The MK50H28 memory structure (Fig. 3) consists of various blocks of off-chip memory. Only the Control/Status registers, some RAM and firmware ROM are onboard the chip. The Initialization Block, Priority DLCI Block, Status Buffer, Address Lookup Table (ALT), Context Table (CT), Transmit/Receive Rings and Buffers are in the off-chip memory.

The buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. The MK50H28 buffer management mechanism will handle data frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK50H28 tests the next segment in the descriptor ring in a look-ahead manner. If the packet is too long for one buffer, the next buffer will be used after filling the first buffer (that is chained to the previous buffer). The MK50H28 will then look ahead to the next buffer, and chain that buffer also if necessary, and so on.

3.2.1 Initialization Block

The MK50H28 initialization information is located in a block of off- chip memory called the Initialization Block. The Initialization Block consists of 44 contiguous words of memory starting on a word boundary. The starting address for the initialization block, IADR, is defined in the CSR2 and CSR3 registers inside the MK50H28. This memory is assembled by the HOST, and the first 15 words are accessed by the MK50H28 during initialization. The Initialization Block (refer to section 4.2) is comprised of:

A. Mode of Operation.

B. The nN1, nN2, and nN3 counters.

C. The dN1(Max Frame Length) counter.

D. The nT1, nT2 and TP (Transmit Polling) timers.

E. Pointer to the beginning of Context Table.

F. Pointer to the beginning of Address Lookup Table.

G. Pointer to the beginning of Status Buffer.

H. Error Counters and Statistics.

3.2.1.1 Priority DLCI Block (PDB)

The Priority DLCI Block consists of Context Table indices for the priority channels. These indices are a mechanism through which the host can demand the MK50H28 to immediately service certain desired DLCIs. The host should first set up entries in the PDB before setting the PTDMD bit in CSR2. In response to that, the MK50H28, after completing transmission service of its current DLCI, will jump to the PDB rather than advancing to the next entry in the context table. After servicing all active entries in the PDB, the MK50H28 will return to the Context Table and resume the transmission service that was in progress before it was interrupted.

3.2.1.2 Interrupt Descriptor Rings

The MK50H28 has two descriptor ring structures for the purpose of queing Transmit and Receive interrupts. The pointers to these two descriptor rings are located at IADR+24 thru IADR+30 in the initialization Block. These descriptor rings are of

a fixed size of 128 entries each. Each entry will consist of two 16-bit words containing the24-bit address of the context table entry (XCTADR or RCTADR) corresponding to the interrupt, a 7-bit field for the descriptor index (CURXD or CURRD) into the associated descriptor ring, and a bit SRVC which is used to indicate whether the interrupt has been serviced. The SRVC bit is set by the MK50H28 when it writes an interrupt to the interrupt ring, and it should be cleared by the host when it services the interrupt. If the MK50H28 attempts to write an interrupt to the interrupt descriptor ring and finds that SRVC is not clear then it will issue a Provider Primitive 7 to indicate an Interrupt Ring MISS (with PPARM=0 to indicate a Receive Interrupt Ring MISS or PPARM=1 to indicate a Transmit Interrupt Ring MISS).

3.2.2 Address Lookup Table(ALT)

The ALT contains the maximum of 1024 or 8192 addresses formed by the Data Link Connection Identifier (DLCI). The MK50H28 can support upto 4 octets of address field. The ALT is used to identify which of the 1024 or 8192 addresses are active. For each active channel it has an Index to the Context Table(CT). The ALT is only used by the receive process of the MK50H28.

3.2.3 Context Table(CT)

The MK50H28 performs multi-tasking by means of a Context Table. Each entry in this table contains all the information relevant to one DLCI channel. Associated with each DLCI are a set of descriptor rings that are used for transmitting and receiving frames. All channel entries, except the LMI Channel,, have equal priority. The MK50H28 scans each entry in the CT sequentially, or through the use of an index pointer mechanism, for any available frames to be transmitted. When a User Primitive 8 with UPARM=2 is issued to the MK50H28. polling of the LMI/LIV channel will be enabled to occur between each poll of the other CT entries.

3.2.4 Transmit Descriptor Ring(s)

The transmit descriptor ring is a circular queue of tasks that point to data buffers. A variable number of buffers may be queued-up on a descriptor ring awaiting execution by the MK50H28. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds values for the length of the buffer and the length of the frame to be transmitted. Each segment also contains an OWNA control bit to denote whether the MK50H28, or the HOST "owns" the buffer. For transmit, when the MK50H28 owns the buffer, the MK50H28 is allowed and commanded to transmit the contents of the buffer. When the MK50H28 does not own the buffer, it will not transmit the data in that buffer.

3.2.5 Receive Descriptor Ring(s)

The receive descriptor ring is circular queue of tasks that point to data buffers. A variable number of buffers may be queued-up on a descriptor ring awaiting execution by the MK50H28. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds values for the length of the buffer and the length of the frame received. Each segment also contains an OWNA control bit to denote whether the MK50H28, or the HOST "owns" the buffer. For receive, when the MK50H28 owns the buffer, the MK50H28 may place received data into that buffer. Conversely, when the MK50H28 does not own a receive buffer, it will not place received data in that buffer.

3.2.6 Frame Format

The frame format supported by the MK50H28 is shown below. Each frame may consist of a programmable number of leading flag patterns (01111110), an address field, an information field, an FCS (CRC) of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags transmitted is programmable through the Mode

FLAG	ADDRESS	INFO	FCS	FLAG
8	16/24/32	8*n	16/32	8

Register in the Initialization Block. The MK50H28 is capable of transmitting and receiving a single flag between adjacent frames.

TRANSMITTED FIRST

3.2.7 MK50H28 Supported Frame Types

The MK50H28 supports all frame types shown in Table 1. In LMI, both **User** and **Network** Modes of operation, along with "Optional **Bidirectional** Network Procedures" (Annex D, ANSI T1.617 - 1991) are supported.

Figure 3: MK50H28 Memory Management Structure

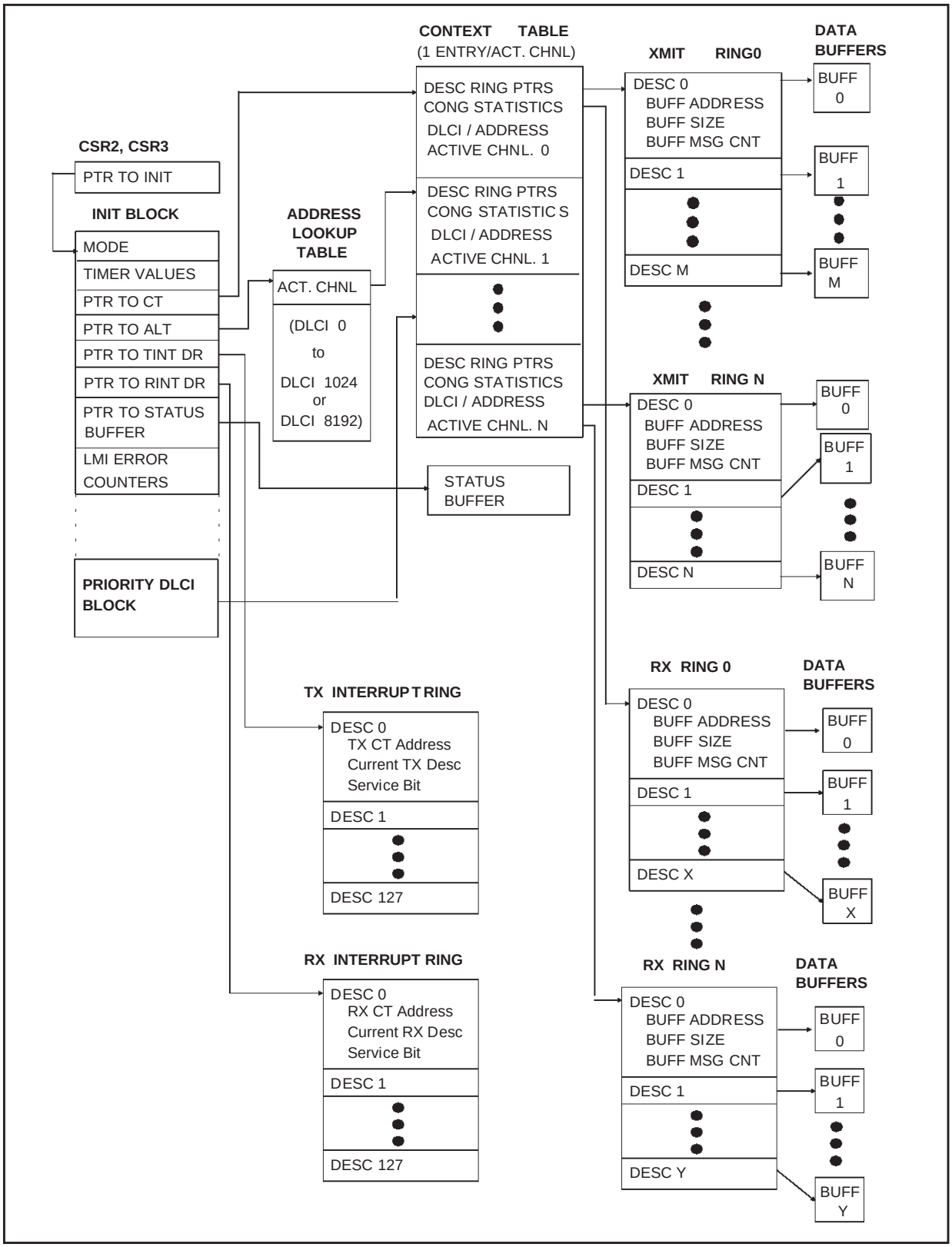


Table 1 - MK50H28 Frame Types

INFORMATION ELEMENT	NAME	DIRECTION	Message Type Encoding MSB LSB
Message Type	STATUS_ENQUIRY	User -> Network	0 1 1 1 0 1 0 1
	STATUS	Network -> User	0 1 1 1 1 1 0 1
	UPDATE_STATUS	Network <-> User	0 1 1 1 1 0 1 1

NOTES:
1. STATUS_ENQUIRY Frame - This Frame has the format as shown in Figure 4.
2. STATUS Frame - This Frame has the format as shown in Figure 5. If Full STATUS information is to be sent, the host must specify the PVC_STATUS Information Element(s) in the transmit buffer(s).
3. Asynchronous STATUS Frame - This Frame has the format as shown in Figure 6. The host must specify the PVC_ STATUS Information Element in the transmit buffer(s).
4. UPDATE_STATUS Frame - Not used in most current applications, MK50H28 supported for backwards compatibility.

3.2.8 Modes of Protocol Operation

The **User** mode of operation is entered by issuing an Auto LMI primitive 7 with UPARM=0. In this mode, the device transmits STATUS ENQUIRY messages to the network with an interval determined by the nT1 timer. After every nN1 transmissions of STATUS ENQUIRY with Report Type of "Length Integrity Verification (LIV) Only" the MK50H28 transmits a STATUS ENQUIRY with Report Type of "Full Status".

When a STATUS frame is received in response to a STATUS ENQUIRY(LIV only), the receive sequence number received from the Network side is checked against the User send sequence number. A received Full STATUS frame will be stored into the LMI/LIV channel buffer, the sequence number checking will be performed, and its reception will be indicated to the host via Provider Primitive 13. An available transmit or receive buffer is not required for the MK50H28 automatic processing of "LIV only" frames.

A received Asynchronous STATUS frame will be stored into the LMI/LIV channel buffer and its reception will be indicated to the host via Provider Primitive 14. If a STATUS ENQUIRY frame (Full or LIV only) is received in this mode of operation, the MK50H28 will discard the frame and increment the Discarded Frames Counter in Context Table enrtry 0. Also see nT1 description in 4.2.2 Timer/Counter section.

The **Network** mode of operation is entered by issuing an Auto LMI primitive 7 with UPARM=1. In this mode, the device automatically responds to STATUS ENQUIRY with Report Type of "Length Integrity Verification (LIV) Only" by transmitting a STATUS frame with Report Type of "LIV Only" along with restarting the nT2 timer. An available transmit or receive buffer is not required for the MK50H28 automatic processing of "LIV only" frames.

When a STATUS ENQUIRY with Report Type of "Full Status" is received, the device issues the LMI Received primitive 13 (with PPARM=1) and expects the host to respond with an LMI Status Request Primitive 11 with UPARM=0 (when the host is ready to transmit the Full STATUS frame).

Asynchronous STATUS frames may be transmitted by placing the data to be transmitted into the appropriate buffer and issueing Primtive 11 with UPARM=2. If a STATUS frame (Full, LIV Only, or Asynchronous) is received in this mode of operation, the MK50H28 will discard the frame and increment the Discarded Frames Counter in Context Table enrtry 0. Also see nT2 description in 4.2.2 Timer/Counter section.

The **Bi-directional Network Procedures** mode is entered by issuing an Auto LMI primitive 7 with UPARM=2. The MK50H28 supports this operation using separate User and Network sequence numbers and N392 and N393 counters. In this mode, the device transmits STATUS ENQUIRY messages with a User set of sequence numbers at an interval determined by the nT1/T391 timer. The expected response is a STATUS frame with corresponding sequence numbers. After every nN1/N391 transmissions of STATUS ENQUIRY with Report Type of "LIV Only", the MK50H28 transmits a STATUS ENQUIRY with Report Type of "Full Status".

A received Full STATUS frame will be stored into the LMI/LIV channel buffer, the sequence number checking will be performed, and its reception will be indicated to the host via Provider Primitive 13. A received Asynchronous STATUS frame will be stored into the LMI/LIV channel buffer and its reception will be indicated to the host via Provider Primitive 14.

In this mode, the device also automatically responds to STATUS ENQUIRY ("LIV Only") by transmitting a STATUS ("LIV Only") frame along with restarting the nT2 timer. When a "Full Status"

STATUS ENQUIRY is received, the device issues the LMI Received primitive 13 (with PPARM=1) and expects the host to respond with LMI Status Request Primitive 11 with UPARM=0 (when the host is ready to transmit the Full STATUS frame).

Asynchronous STATUS frames may be transmitted by placing the data to be transmitted into the appropriate buffer and issueing Primtive 11 with UPARM=2.

LMI frames received in any mode will not cause Receive Interrupts (RINT) to be generated, nor will the Receive Interrupt Ring be updated. Instead, the MK50H28 will issue primitives corresponding to those LMI Frame received which are not automatically processed by the MK50H28 (i.e. non "LIV only" frames). See the description of primitives in section 4.1.2.2. In addition to the primitives, bits 09-11 of the Receive Message Descriptor 0 (RMD0) for the LMI channel will indicate the type of frame received. See section 4.3.1.2 for details.

In Non-Auto-LMI mode of operation, LMI frames received on the LMI Channel (typically DLCI 0) will be written into the receive buffer as Transparent or SVC frames.

Also refer to **Detailed Programming Procedures** (section 4.4) for more information on using the device in the previously mentioned modes of Protocol Operation.

Figure 4: Sample Annex A STATUS_ENQUIRY Frame

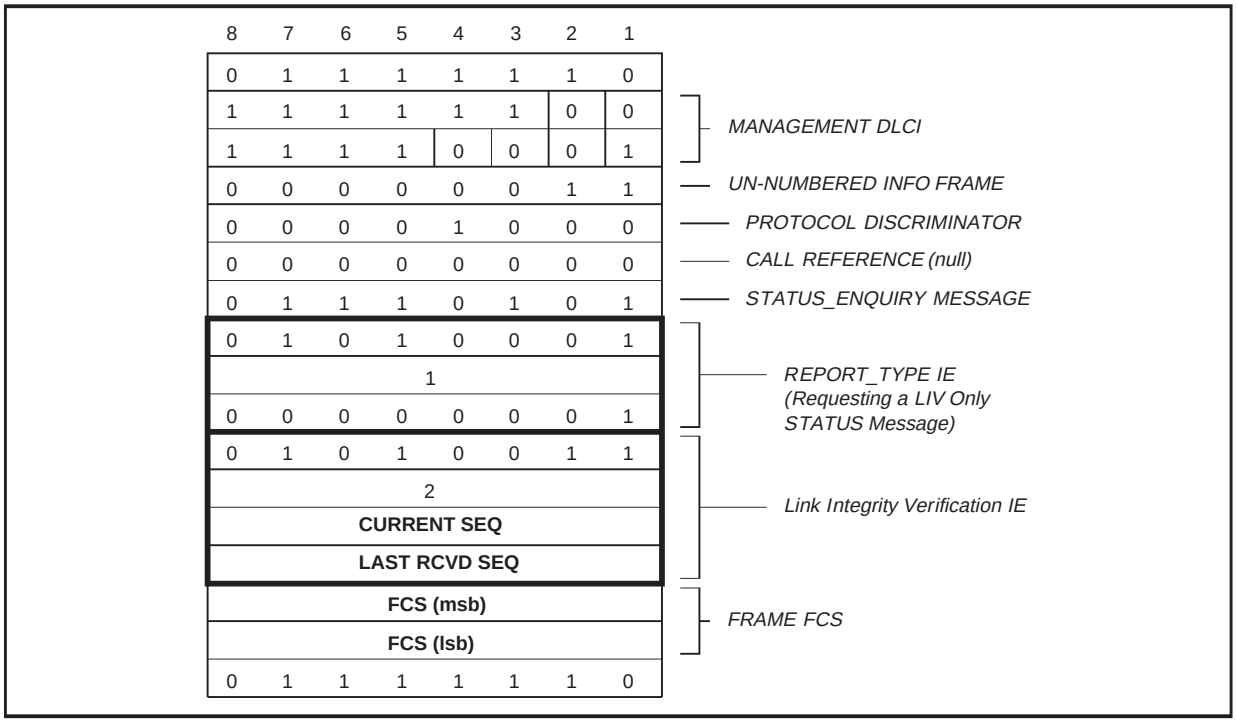


Figure 5: Sample Annex A STATUS Frame (Full)

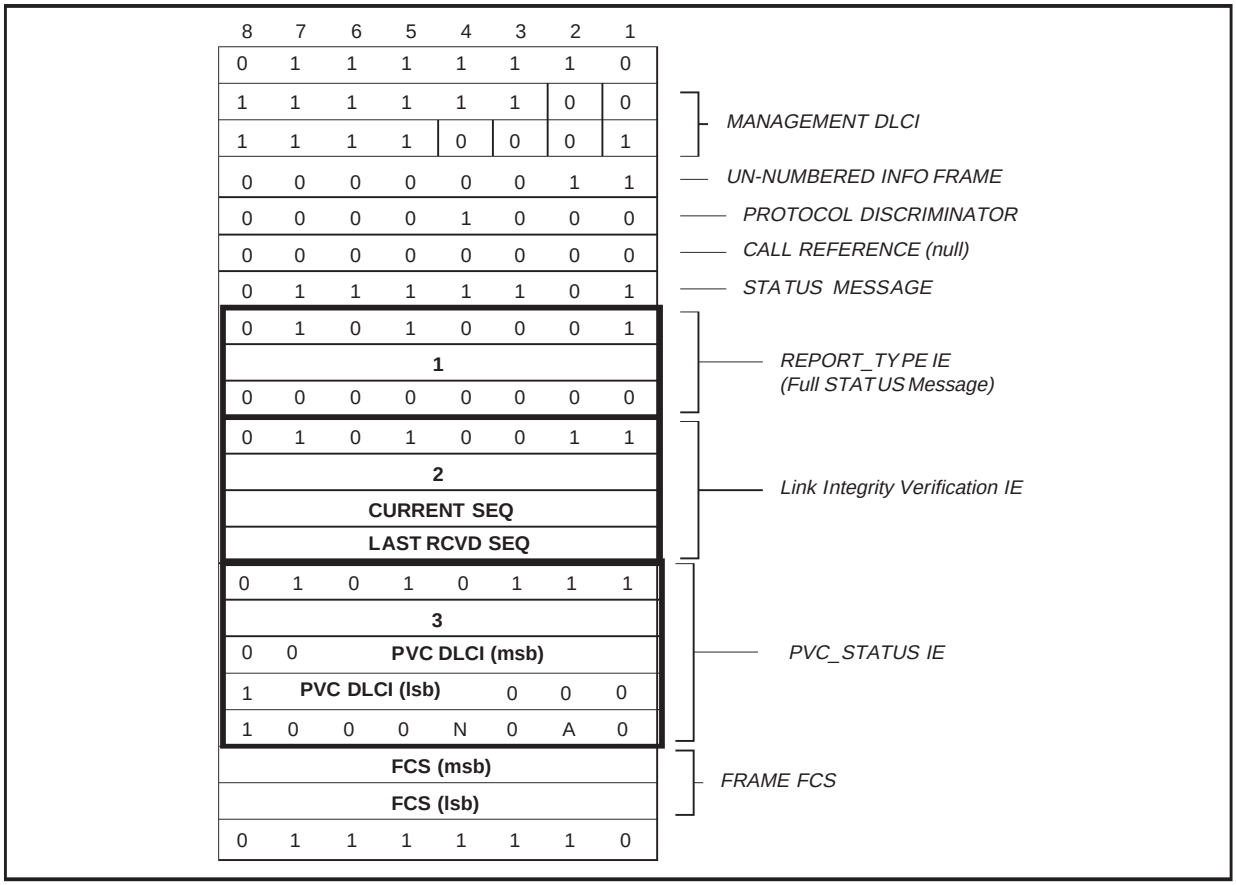


Figure 6: Sample Annex D STATUS Frame (Full)

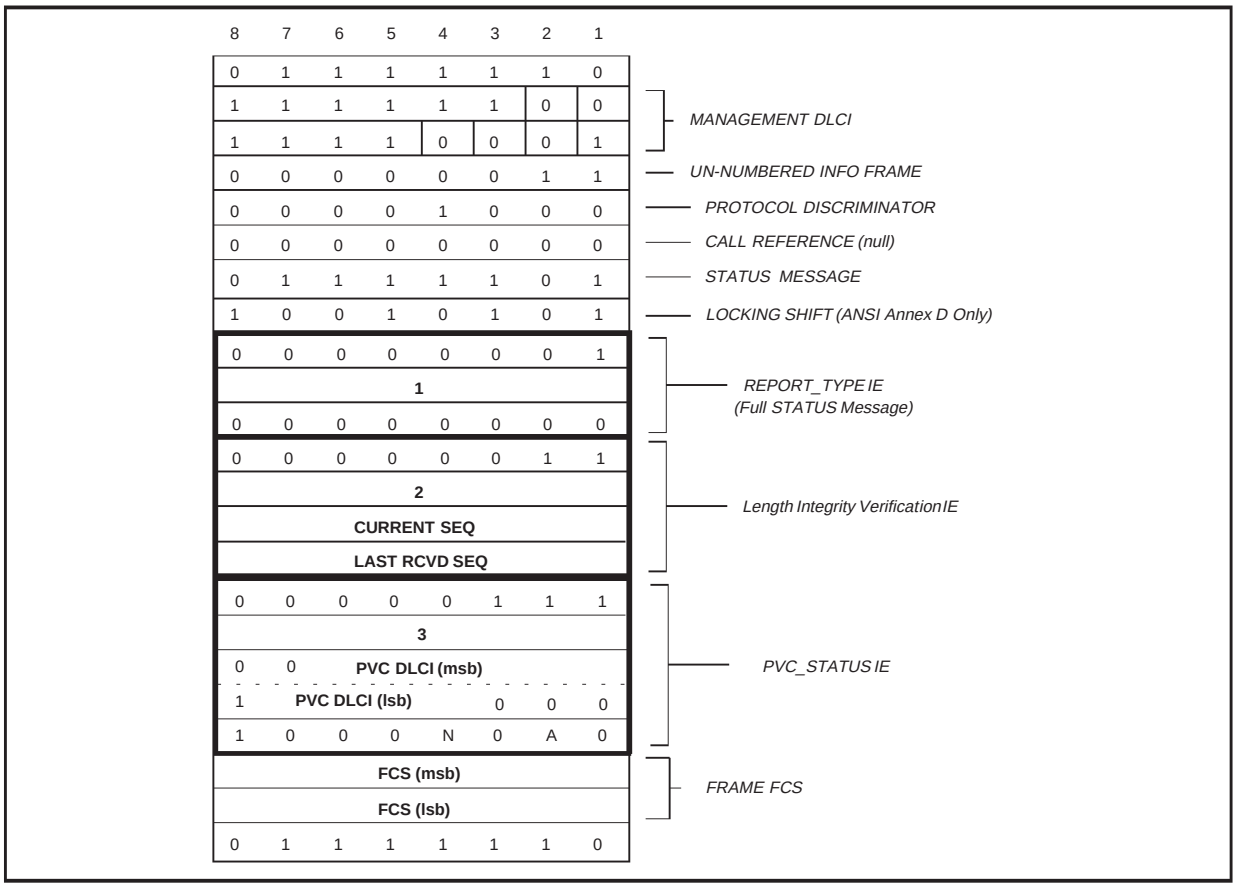
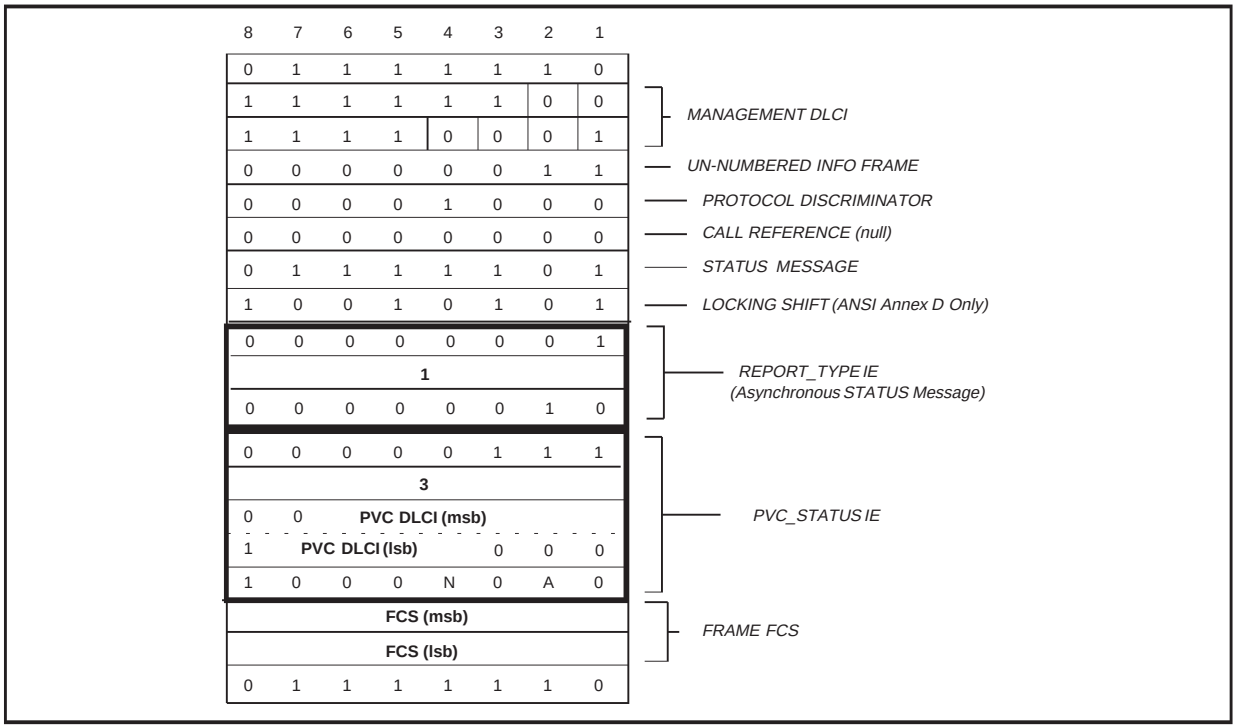


Figure 7: Sample Asynchronous STATUS Frame (Annex D)



SECTION 4

PROGRAMMING SPECIFICATION

This section defines the Control and Status Registers and the memory data structures required to program the MK50H28.

4.1 Control and Status Registers

There are six Control and Status Registers (CSR's) resident within the MK50H28. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP), thus requiring only two locations in the system memory or I/O map.

4.1.1 Accessing the Control and Status Registers

The CSR's are read (or written) in a two step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten or upon a bus reset. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

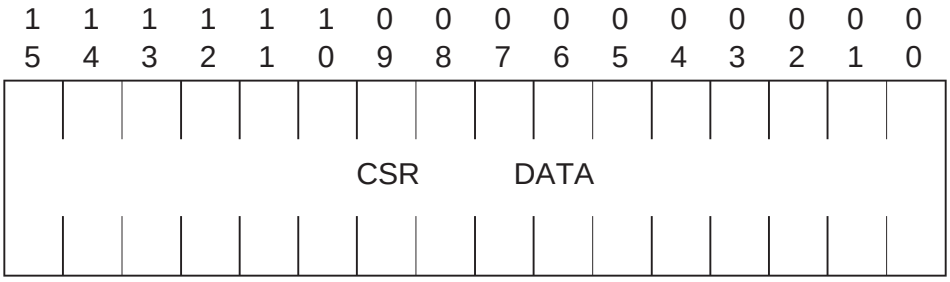
ADR	Port

4.1.1.1 Register Address Port (RAP)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	BM8	0	0	0	CSR <2:0>			HBYTE

BIT	NAME	DESCRIPTION
15:08	RESERVED	Must be written as zeroes
07	BM8	When set, places chip into 8 bit mode. CSR's, Init Block, and data transfers are all 8 bit transfers; this provides compatibility with 8 bitmicroprocessors. When clear, all transfers are 16 bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is READ/WRITE and cleared on Bus RESET.
06:04	RESERVED	Must be written as zeroes
03:01	CS3<2:0>	CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET. CSR<2:0> — CSR 0 — CSR0 1 — CSR1 2 — CSR2 3 — CSR3 4 — CSR4 5 — CSR5
00	HBYTE	Determines which byte is addressed for 8 bit mode. If set, the high byte of the register referred to by CSR<2:0> is addressed, otherwise the low byte is addressed. This bit is only meaningful in 8 bit mode and must be written as zero if BM8=0. HBYTE is READ/WRITE and cleared on bus reset.

4.1.1.2 Register Data Port (RDP)

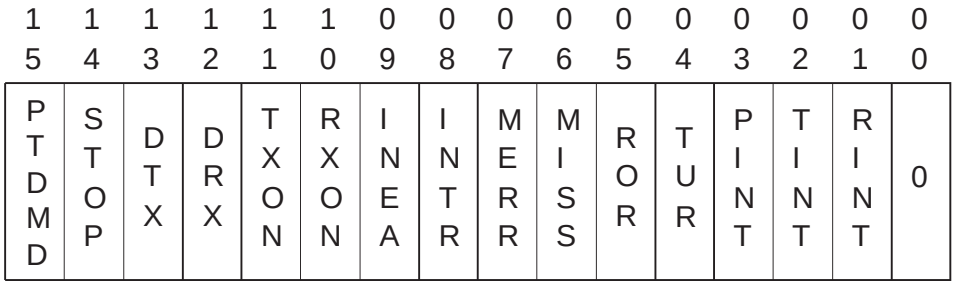


BIT	NAME	DESCRIPTION
15:00	CSR DATA	Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

4.1.2 Control and Status Register Definition

4.1.2.1 Control and Status Register 0 (CSR0)

RAP<3:1> = 0

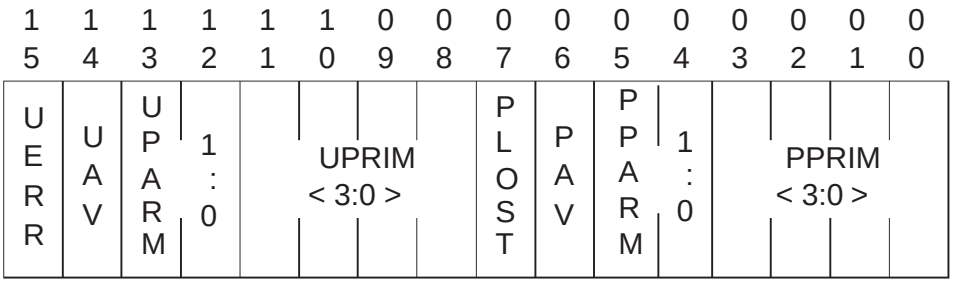


BIT	NAME	DESCRIPTION
15	PTDMD	Transmit Demand for Priority DLCIs. Setting this bit to 1 causes the MK50H28 to jump to Priority DLCI Block (PDB). This bit is cleared by the MK50H28 after servicing all active entries in the PDB. (Note: See section 4.2.9 for more details.)
14	STOP	STOP, when set, indicates that MK50H28 is operating in the STOPPED Phase of operation. All external activity is disabled and internal logic is reset. MK50H28 remains inactive except for primitive processing until a START primitive is issued. STOP IS READ ONLY and set by Bus RESET or a STOP primitive. Writing to this bit has no effect.
13	DTX	Disable Transmitter. Prevents the MK50H28 from further access to the Transmitter Descriptor Rings. No transmissions are attempted after finishing transmission of any frame in transmission at the time of DTX being set. Even LMI frames normally generated automatically will not be transmitted if DTX=1. TXON acknowledges changes to DTX, see below. DTX is READ/WRITE.
12	DRX	Disable the Receiver prevents the MK50H28 from further access to the Receiver Descriptor Rings. No received frames are accepted after finishing reception of any frame in reception at the time of DRX being set. Setting DRX will put the MK50H28 in the LOCAL BUSY Phase. RXON acknowledges changes to DRX, see description of RXON. DRX is READ/WRITE.

BIT	NAME	DESCRIPTION
11	TXON	TRANSMITTER ON indicates that the transmit ring access is enabled. TXON is set as the Start primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Rings entries regardless of the state of the OWNA bits. TXON is READ ONLY; writing to this bit has no effect.
10	RXON	RECEIVER ON indicates that the receive ring access is enabled. RXON is set as the Start primitive is issued if the DRX bit is "0" or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. RXON is READ ONLY; writing to this bit has no effect.
09	INEA	INTERRUPT ENABLE allows the $\overline{\text{INTR}}$ I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. If INEA = 0 the $\overline{\text{INTR}}$ I/O pin will be high, regardless of the state of the Interrupt Flag (TINT, RINT, or PINT) or whether the Interrupt Desciptor Ring has been updated. INEA is READ/WRITE set by writing a "1" into this bit and is cleared by writing a "0" into this bit, by Bus RESET, or by issuing a Stop primitive. INEA may not be set while in the STOPPED Phase.
08	INTR	INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occurred: MISS, MERR, RINT, TINT, PINT. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a Stop primitive.
07	MERR	MEMORY ERROR is set when the MK50H28 is the Bus Master and $\overline{\text{READY}}$ has not been asserted within 256 SYSCLKs (25.6 usec @ 10MHz) after asserting the address on the DAL lines. When a Memory Error is detected, the MK50H28 releases the bus, the receiver and transmitter are turned off, and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
06	MISS	MISSED frame is set when the receiving channel loses a frame because it is either not ready or does not own a receive buffer indicating loss of data. The Memory Address for which MISS occurred can be determined by issuing a Status Request primitive (see section 4.3.3 Status Buffer for additional details). When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by MK50H28 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
05	ROR	RECEIVER OVERRUN indicates that the Receiver FIFO was full when the receiver was ready to input data to the Receiver FIFO. The frame being received is lost, but is probably recoverable if an upper level protocol is used. When ROR is set, an interrupt is generated if INEA=1. ROR is READ/CLEAR ONLY and is set by MK50H28 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
04	TUR	TRANSMITTER UNDERRUN indicates that the MK50H28 has aborted a frame since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a frame. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by MK50H28 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
03	PINT	PRIMITIVE INTERRUPT is set after the chip updates the primitive register to issue a provider primitive. When PINT is set, an interrupt is generated if INEA =1. PINT is READ/CLEAR ONLY and is set by MK50H28 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
02	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit Descriptor Ring. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by the MK50H28 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
01	RINT	RECEIVER INTERRUPT is set after the MK50H28 updates an entry in the Receive Descriptor Ring (this is done once per received frame, not per received buffer). When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by the MK50H28 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
00	0	This bit is READ ONLY and will always read as zero.

4.1.2.2 Control and Status Register 1 (CSR1)

RAP <3:1> = 133/



BIT	NAME	DESCRIPTION
15	UERR	USER PRIMITIVE ERROR is set by the MK50H28 when a primitive is issued by the user which is in conflict with the current status of the chip. UERR is READ/CLEAR ONLY and is set by MK50H28 and cleared by writing a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.
14	UAV	USER PRIMITIVE AVAILABLE is set by the user when a primitive is written into UPRIM. It is cleared by the MK50H28 after the primitive has been processed. This bit is also cleared by a Bus RESET.
13:12	UPARM	USER PARAMETER is written by the host in conjunction with the user primitives in UPRIM. This User Parameter field provides information to the MK50H28 concerning the corresponding user primitive. NOTE: For all primitives UPARM = 0 unless otherwise indicated.
11:08	UPRIM	USER PRIMITIVE is written by the user, in conjunction with setting UAV, to control the MK50H28 link procedures. The following primitives are available:
	0	**Stop**: Causes MK50H28 to enter the STOPPED Phase. All link activity is terminated and the STOP bit is set. All DMA activity ceases. The transmitter outputs all ones, and all received data is ignored.
	1	**Start**: Instructs the MK50H28 to exit the STOPPED Phase and enter the INFORMATION TRANSFER Phase. The Context Table and the Descriptor Rings are Reset. The transmitter begins to output flags. The Start primitive is valid only after the device is initialized (Init Request performed.) **If the Auto LMI primitive is not issued after a Start primitive, then the only way to transmit LMI frames is through the use of LMI primitives (10, 11, 12, & 14), and processing is performed on received LMI frames, but no automatic response or action is taken.** Valid only in STOPPED phase.
	2	**Init Request**: Instructs the MK50H28 to read the Initialization Block from memory. This should be performed prior to the Start primitive or Transparent primitive after a bus reset or power-up. Valid only in STOPPED phase.
	3	**Transparent Mode:** Instructs the device to exit the STOPPED Phase, enter the TRANSPARENT Phase, and reset the Context Table and Descriptor Rings. No header stripping or pre-pending is done for any DLCI channel, and no automatic LMI processing is possible in this mode. **All frames are received to Context Table entry 0** associated descriptor ring and buffers, and the **RTAN bit in CT0 should be set** so that the entire received frame will be written to the buffer. **Transmission of frames can occur from any Context Table entry, including CT0**, and the **XTRAN bit should be set** so that only the data in the buffer will be transmitted for the entire frame. This primitive is only valid after device Initialization (Init Request performed). Valid only in STOPPED phase.
	4	**Status Request**: Instructs the MK50H28 to write the current chip status into the STATUS BUFFER. Valid in all states, but only after the Init primitive has been previously issued.
	5	**Self-Test Request**: Instructs the MK50H28 to perform the built in internal self test. Valid only in the STOPPED Phase. See section 4.4.10 for the self test procedure.

BIT	NAME	DESCRIPTION
	7	**Auto LMI:** Instructs the device to enter the **Auto LMI Mode** of operation. **Auto LMI with UPARM=0** causes the device to enter **User** mode of operation. **Auto LMI with UPARM=1** causes the device to enter **Network** mode of operation. **Auto LMI with UPARM=2** causes the device to enter **Bi-directional** mode of operation These modes are defined in sections 3.2.7 and 3.2.8 (Modes of Protocol Operation) Valid only in INFORMATION TRANSFER phase. See also Start primitive.
	8	**Start Timer nT1(UPARM=0)**: Instructs the MK50H28 to start the nT1 **(User)** timer. Issuing this primitive while in the **User** mode of Auto LMI operation may lead to erroneous results. Not valid in TRANSPARENT Mode. **Enable LMI Channel Polling (UPARM=2):** Instructs the MK50H28 to start polling the LMI Channel (Context Table Entry 0) for any LMI frames to be transmitted. The type of LMI frame to be transmitted will be determined by the Frame Type bits in the TMD0 (see section 4.3.2.2). The polling of the LMI Channel will be interleaved between polling each other CT Entry or channel, thus giving the LMI Channel a high degree of priority. **Disable LMI Channel Polling (UPARM=3):** Instructs the MK50H28 to stop polling of the LMI Channel. The default initialization condition of the MK50H28 is for LMI Channel Polling to be disabled, so this primitive only need be issued if polling was enabled earlier.
	9	**Start Timer nT2**: Instructs the MK50H28 to start the nT2 **(Network)** timer. Issuing this primitive while in the **Network** mode of Auto LMI operation may lead to erroneous results. Not valid in TRANSPARENT Mode.
	10	**LMI STATUS_ENQUIRY Request**: Instructs the MK50H28 to send a STATUS_ENQUIRY frame to the remote site (network). **If UPARM = 1**, will request Sequence Numbers only. Otherwise, requests Full STATUS frame. Not valid in TRANSPARENT Mode.
	11	**LMI STATUS Request**: Instructs the MK50H28 to send a STATUS frameto the remote site (user). **If UPARM=0**, it will send a FULL STATUS frame with the data in the associated LMI Channel buffer (this is a typical response to a received STATUS ENQUIRY with Report' Type of FULL STATUS). **If UPARM = 1**, it will send a Sequence Numbers Only (LIV Only) frame. **If UPARM=2**, it will send an Aysnchronous STATUS frame with the data in the associated LMI Channel buffer. Not valid in TRANSPARENT Mode.
	12	**LMI UPDATE_STATUS Request**: Instructs MK50H28 to send UPDATE_STATUS frame with the data in the associated LMI Channel buffer. Not valid in TRANSPARENT Mode.
	13	**Receive LMI Full Status Enquiry Request** (UPRIM =13, UPARM=0); Instructs the MK50H28 to cause the next received Sequence Number Only (LIV Only) Status Enquiry Frame to be received to a buffer, as if it were a FULL STATUS ENQUIRY Frame. However, the statistics corresponding to the actual type of frame received wil be incremented No response frame will be automatically generated by the MK50H28. Issueing UPRIM 13 with UPARM =1 prior to receipt of the next LIV Only Status Enquiry Frame will cancel the action originally requested by the Receive LMI Full Status Enquiry Request Primitive.
	14	**Send LMI:** Instructs the chip to send a frame using the contents of the buffer(s) pointed to by the Context Table LMI Channel (either 0 or 1023 based upon the setting of LMICH bit in CSR2). The frame will be transmitted using the header information from the Context Table LMI Channel. Valid in all Phases of operation except for STOPPED mode. NOTE: Only one frame will be transmitted per Send LMI primitive.
	15	**Indicate Protocol Event:** This primitive can be used by the host to inform the MK50H28 of errored events not monitored by the chip (such as a received PVC status IE with New bit=0 for a PVC not currently defined) **If UPARM=0**, it instructs the MK50H28 to add one **good** event to the N392/nN2 count. **If UPARM=1**, it instructs the MK50H28 to add one **errored** event to the N392/nN2 count.

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>07</td><td>PLOST</td><td>PROVIDER PRIMITIVE LOST is set by the MK50H28 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared or by a Bus RESET. Writing to this bit has no effect.</td></tr>
<tr><td>06</td><td>PAV</td><td>PROVIDER PRIMITIVE AVAILABLE is set by the MK50H28 when a new provider primitive has been placed in PPRIM. PAV is READ/CLEAR ONLY and is set by the chip and cleared by writing a ”1” to the bit or by Bus RESET. Under normal operation the host should clear the PAV bit after PPRIM is read.</td></tr>
<tr><td>05:04</td><td>PPARM</td><td>PROVIDER PARAMETER provides additional information about the reason for the receipt of certain primitives. The following table shows the parameters for the applicable provider primitives. This field is undefined for other provider primitives.
<table>
<tr><th>PPARM</th><th>LMI Frame Received</th></tr>
<tr><td>0</td><td>STATUS ENQUIRY with Report Type of Sequence Numbers Exchange Only</td></tr>
<tr><td>1</td><td>STATUS ENQUIRY with Report Type of FULL STATUS</td></tr>
<tr><td>2</td><td>STATUS frame received</td></tr>
<tr><td>3</td><td>SVC or UPDATED STATUS frame received</td></tr>
</table></td></tr>
<tr><td rowspan="15">03:00</td><td>PPRIM</td><td>PROVIDER PRIMITIVE is written by the MK50H228, in conjunction with setting the PAV bit, to inform the user of link control conditions. Valid Provider Primitives are as follows:</td></tr>
<tr><td>2</td><td>Init Confirmation: Indicates MK50H28 Init Block reading has completed.</td></tr>
<tr><td>3</td><td>Watchdog Timer Expiry Indication: Indicates expiration of TCLK or RCLK watchdog timer as determined by the value of PPARM (PPARM=1 indicatesTCLK, PPARM=2 indicates RCLK. If PLOST is set it indicates both RCLK and TCLK watchdog timers expired). This primitive is issued only if enabled by setting CSR5<15:12> bits to something other than 0.</td></tr>
<tr><td>4</td><td>Alarm Indication: nN2 of the last nN3 LMI events are corrupted in timing or content.</td></tr>
<tr><td>6</td><td>Alarm Clear Indication: Indicates reception of nN3 correct sequential LMI events after the Alarm Indication. The issueing of Alarm Clear Indication and Alarm Indication primitives will be re-attempted if PLOST is set, and will be repeated until issued without PLOST set.</td></tr>
<tr><td>7</td><td>Interrupt Descriptor Ring MISS: Indicates inability to write to the Interrupt Descriptor Ring due to the SRVC bit not being clear. With PPARM = 0 it indicates a Transmit Interrupt Ring MISS. With PPARM = 1 it indicates a Receive Interrupt Ring MISS.</td></tr>
<tr><td>8</td><td>Timer nT1 Expiration: Indicates expiration of the timer nT1.</td></tr>
<tr><td>9</td><td>Timer nT2 Expiration: Indicates expiration of the timer nT2.</td></tr>
<tr><td>10</td><td>Counter nN1 Overflow: Indicates that the counter nN1 has overflowed.</td></tr>
<tr><td>11</td><td>Clear New Bit Indicatiojn: This primitive is issued when the sequence number received in a Status Enquiry frame matches the sequence number sent in the last Full Status frame.</td></tr>
<tr><td>12</td><td>LMI Frame Transmitted: Indicates that a LMI frame was just transmitted.</td></tr>
<tr><td>13</td><td>LMI Frame Received: Indicates that a LMI frame was just received and stored in the buffer(s) corresponding to the LMI channel. The PPARM field will indicate the type of frame received. In Auto LMI mode, a required host response to a received STATUS ENQUIRY with Report Type of FULL STATUS is to issue an LMI STATUS Request primitive with UPARM = 0 (STATUS Request with Report Type of FULL STATUS). The device will not automatically respond to a received STATUS ENQUIRY with Report Type of FULL STATUS.
Note: If a LMI frame is received while the PAV bit is still set (because a previously received primitive has not yet been processed by the host), the MK50H28 will set the PLOST bit and the received LMI frame will be discarded. No counters will be updated.</td></tr>
<tr><td>14</td><td>Aysnchronous STATUS Frame Received: Indicates that an Aysnchronous STATUS frame was just received. Received Aysnchronous STATUS frames are stored in the LMI channel buffer without the DLCI header information.</td></tr>
</table>

4.1.2.3 Control and Status Register 2 (CSR2)

RAP<3:1> = 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CYCLE	EIBEN	DLCI1K	LMICH	TRAN	0	ANXD	TDMD	IADR<23:16>							

BIT	NAME	DESCRIPTION
15	CYCLE	Setting this bit selects a shorter DMA Cycle (5 vs 6 SYSCLK)
14	EIBEN	Extended Initialization Block Enable. Setting this bit causes the MK50H28 to use an extended Initialization Block which uses all of IADR+08 as a 16-bit scaler and moves nN1 to the upper byte of IADR+40.
13	DLCI1K	Setting this bit causes the chip to recognize the 8192 possible DLCIs.If this bit is cleared, the chip will ignore all received frames with DLCI greater than 1023.
12	LMICH	CHLMI Channel Select: Setting this bit to 0 causes frames received on DLCI 0 to be treated as LMI frames.. Setting it to 1 causes frames received on DLCI 1023 to be treated as LMI frames. **NOTE: Regardless of the setting of this bit, only the first entry in the Context Table table (CT0) will be used for transmission and reception of LMI frames.**
11	TRAN	Should be set only if frames need to be transmitted without protocol processing from the transmit buffers. With this bit set, the chip will not prepend an address field when transmitting data from the buffers, but rather, the buffers should have both address and data information for proper Frame Relay protocol.
10	0	Reserved. Must be written as zeroes.
09	ANXD	Setting this bit enables operation in conformance with T1.617 Annex D specifications. With ANXD=0, the MK50H28 operates in conformance with CCITTQ.933 Annex A.
08	TDMD	Transmit Demand. Setting this bit causes the MK50H28 to ignore the TP (Transmit Poll timer) and continuously poll all Context Table entries until TDMD is cleared by the host.
07:00	IADR	The high order 8 bits of the address of the first word in the Initialization Block. IADR must be written by the Host prior to issuing an Init Request primitive.

4.1.2.4 Control and Status Register 3 (CSR3)

RAP<3:1> = 3

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IADR <15:00>															0

BIT	NAME	DESCRIPTION
15:00	IADR	The low order 16 bits of the address of the first word in the Initialization Block. Must be written by the Host prior to issuing an Init Request primitive. The Initialization block must begin on a word boundary.

4.1.2.5 Control and Status Register 4 (CSR4)

CSR4 allows redefinition of the bus master interface.
RAP<3:1> = 4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
XWD1	XWD0	RWD1	RWD0	0	XHOLD	FWM		BAE	BUSR	BSWPC	BURST	1:0	BSWPD	ACON	BCON

BIT	NAME	DESCRIPTION
15:12	XWD0/1, RWD0/1	Watchdog Timers. These bits enable and determine the timer values for the Transmit and Receive Watchdog Timers. These timers are independently programmable and are reset by any transition on the TCLK and RCLK pins respectively. The watchdog timers will expire after approximately Wn SYSCLK cycles (if not reset by transition on TCLK/RCLK) and Provider Primitive 3 will be issued. The following table shows the selections for Wn: XWD1/RWD1 | XWD0/RWD0 | Wn 0 | 0 | Disabled 0 | 1 | 2^{18} 1 | 0 | 2^{19} 1 | 1 | 2^{20}
11	0	Reserved, must be written as zero.
10	XHOLD	Setting this bit enables the Transmit FIFO Hold-Off mechanism of the MK50H28. If XHOLD=1 and the Transmit FIFO is emplty, the MK50H28 transmitter will be "held off" from transmitting a frame until the FIFO has at least the XHOLD Watermark (selected with FWM below) of data, or the entire frame , in the Transmit FIFO.
09:08	FWM	These bits define the FIFO watermarks. FIFO watermarks prevent the MK50H28 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive, data will only be transferred to the buffers after the receive FIFO has at least N 16-bit words or end of frame has been received. Conversely, for transmit, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. The Transmit Hold-Off Watermark enabled by setting XHOLD=1 is also defined by these bits. N is defined as follows: FWM <1:0> | FWM N | XHOLD N 11 | Not Allowed | Not Allowed 10* | 9 words | 19 Words 01 | 17 words | 11 Words 00 | 25 words | 3 Words * Suggested setting
07	BAE	Bus Address Enable: if BAE is set then the A23-A20 pins are driven by the MK50H28 constantly providing the ability to use A23-A20 for memory bus selection. If clear, A23-A20 behave identically to A19- A16.
06	BUSR	If this bit is set, pin 15 becomes input $\overline{\text{BUSREL}}$. If this bit is clear then pin 15 is either $\overline{\text{BM0}}$ or BYTE depending on bit 00. For more information see the description for pin 15 in this document. BUSR is READ/WRITE and cleared on bus Reset.

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>05</td><td>BSWPC</td><td>This bit determines the byte ordering of all ”non-data” DMA transfers. This transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMAtransfers. BSWPC allows the MK50H28 to operate with memory organizations that have bits 07:00 at even addresses and with bits 15:08 at odd addressses or vice versa. BSWPC is Read/Write and cleared by BUS RESET.

With BSWPC = 0:
Address Address
XX0 | 0 | . . . | 7 XX1 | 8 | . . . | 15

With BSWPC = 1:
Address Address
XX0 | 8 | . . . | 15 XX1 | 0 | . . . | 7</td></tr>
<tr><td>04:03</td><td>BURST</td><td>This field determines the maximum number of data transfers performed each time control of the host bus is obtained. BURST is READ/WRITE and cleared on bus Reset.

<table>
<tr><th>BURST <1:0></th><th>8 bit mode</th><th>16 bit mode</th></tr>
<tr><td>00</td><td>2</td><td>1</td></tr>
<tr><td>10*</td><td>16</td><td>8</td></tr>
<tr><td>01</td><td>unlimited</td><td>unlimited</td></tr>
</table>
*Suggested setting</td></tr>
<tr><td>02</td><td>BSWPD</td><td>This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above). For most applications, including most 68000 based systems, this bit should be set.</td></tr>
<tr><td>01</td><td>ACON</td><td>ALE CONTROL defines the assertive state of pin 18 when the MK50H28 is a Bus Master. ACON is READ/ WRITE and cleared by Bus RESET.

<table>
<tr><th>ACON</th><th>PIN18</th><th>NAME</th></tr>
<tr><td>0</td><td>ASSERTED HIGH</td><td>ALE</td></tr>
<tr><td>1</td><td>ASSERTED LOW</td><td>$\overline{AS}$</td></tr>
</table></td></tr>
<tr><td>00</td><td>BCON</td><td>BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by Bus RESET.

<table>
<tr><th>BCON</th><th>PIN16</th><th>PIN15</th><th>PIN17</th></tr>
<tr><td>0</td><td>$\overline{BM1}$</td><td>$\overline{BM0}$</td><td>HOLD</td></tr>
<tr><td>1</td><td>$\overline{BUSAKO}$</td><td>BYTE</td><td>$\overline{BUSRQ}$</td></tr>
</table></td></tr>
</table>

4.1.2.6 Control and Status Register 5 (CSR5)

CSR5 facilitates control and monitoring of modem controls.
RAP<3:1> = 5

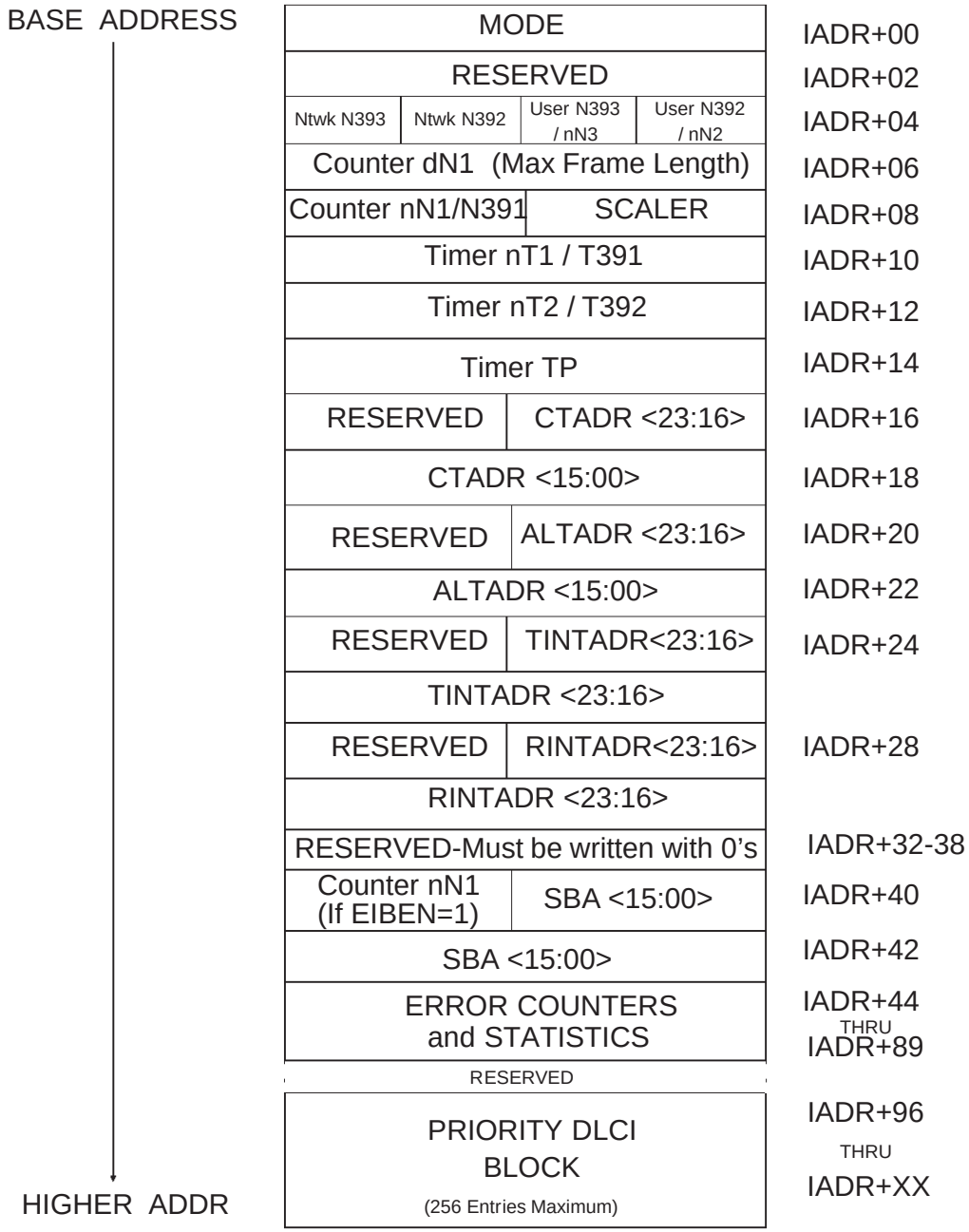
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	XEDGE	RTSEN	DTRD	DSRD	DTR	DSR

BIT	NAME	DESCRIPTION
15:06	0	Reserved, must be written as zeroes.
5	XEDGE	Setting this bit causes the TD output to change on the rising edge of $\overline{TCLK}$ rather than on the falling edge as indicated in the pin 25 description.
4	RTSEN	RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set, pin 26 becomes $\overline{RTS}$ and pin 30 becomes $\overline{CTS}$. $\overline{RTS}$ is driven low whenever the MK50H28 has data to transmit and is kept low during transmission. $\overline{RTS}$ will be driven high after the closing flag of a signal unit is transmited if either no other frames are in the FIFO or if the minimum signal unit spacing is higher than 2 (see Mode Register). The MK50H28 will not begin transmission and TD will remain HIGH if $\overline{CTS}$ is high. If RTSEN = 0 then pins 26 and 30 become programmable I/O pins DTR and DSR. The direction and behavior of DSR and DTR are controlled by the following bits.
3	DTRD	DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR/RTS pin. If DTRD = 0, the DTR/RTS pin becomes an input pin and the DTR bit reflects the current value of the pin; if DTRD = 1, the DTR/RTS pin is an output pin controlled by the DTR bit below.
2	DSRD	DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR/CTS pin. If DSRD = 0, the DSR/CTS pin becomes an input pin and the DSR bit reflects the current value of the pin; if DSRD = 1, the DSR/CTS pin is an output pin controlled by the DSR bit below.
1	DTR	DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR/RTS pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR/RTS pin.
0	DSR	DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR/CTS pin. If DSRD = 1 this bit becomes READ/WRITE and any value written to this bit appears on the DSR/CTS pin.

4.2 Initialization / Priority DLCI Block

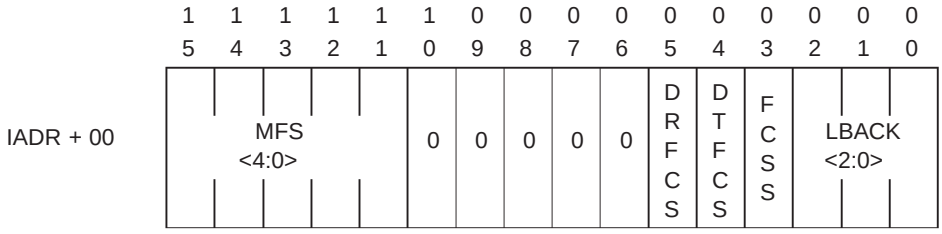
MK50H28 initialization includes the reading of the Initialization Block in the off-chip memory to obtain the operating parameters. The Initialization Block is defined below. Upon receiving an Init primitive, the first 16 words of the Initialization block are read by the MK50H28. The remainder of the Initialization block will be read as needed by the MK50H28. Memory at IADR+32 - IADR+38 should always be initialized with 0's prior to issuing the Init Primitive. Any changes to IADR+00 - IADR+31 after initialization require that the device be stopped and Init primitive be issued again in order to take effect. It is not necessary that the device be re-initialized after changes to bits in the CSRs (Control and Status Registers).

Figure 8: Initialization / Priority DLCI Block



4.2.1 Mode Register

The Mode Register allows alteration of the MK50H28's operating parameters.



BIT	NAME	DESCRIPTION
15:11	MFS<4:0>	Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK50H28. This only affects frames transmitted by the MK50H28 and does not restrict the spacing of the frames received by the MK50H28. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after CTS is driven low (minus one for the trailing flag). See the following table for encoding of this field.

NUMBER OF FLAGS	MFS<4:0>	NUMBER OF FLAGS	MFS<4:0>
1	1	32	28
2	0	34	24
4	2	36	17
6	4	38	3
8	9	40	6
10	18	42	13
12	5	44	27
14	11	46	23
16	22	48	14
18	12	50	29
20	25	52	26
22	19	54	21
24	7	56	10
26	15	58	20
28	31	60	8
30	30	62	16

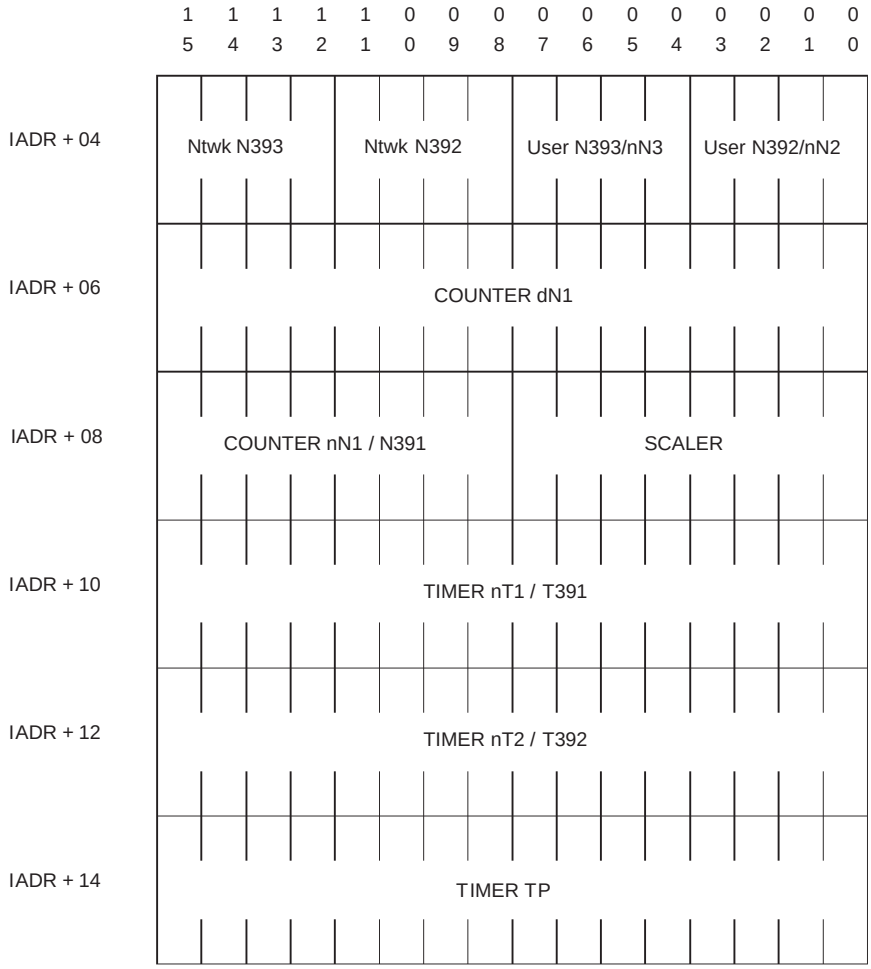
10:06	0	Reserved. Must be written as zeros.
05	DRFCS	Disable Receiver FCS (CRC). When DRFCS = 0, the receiver will extract and check the FCS field at the end of each frame. When DRFCS = 1, the receiver continues to extract the last 16 or 32 bits of each frame, depending on FCSS, but no check is performed to determine whether the FCS is correct. If the received frame is an even number of bytes, the first 16 bits of the FCS will be appended to the end (as indicated by MCNT) of the receive buffer data.
04	DTFCS	Disable Transmitter FCS. When DTFCS=0, the transmitter will generate and append the FCS to each signal unit. When DTFCS = 1, the FCS logic is disabled, and no FCS is generated with transmitted frames. Setting DTFCS = 1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect FCS.
03	FCSS	FCS Select. When FCSS = 1, a 16-bit FCS is selected otherwise a 32-bit FCS is used.

BIT	NAME	DESCRIPTION
02:00	LBACK	Loopback Control puts MK50H28 into one of several loopback configurations.

LBACK	DESCRIPTION
0	Normal operation. No loopback.
4	Simple loopback. Receive data and clock are driven internally by transmit data and clock. Transmit clock must be supplied externally
5	Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.
6	Silent loopback. Same as simple loopback with td pin forced to all ones.
7	Silent clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. The TD pin is forced to all ones.

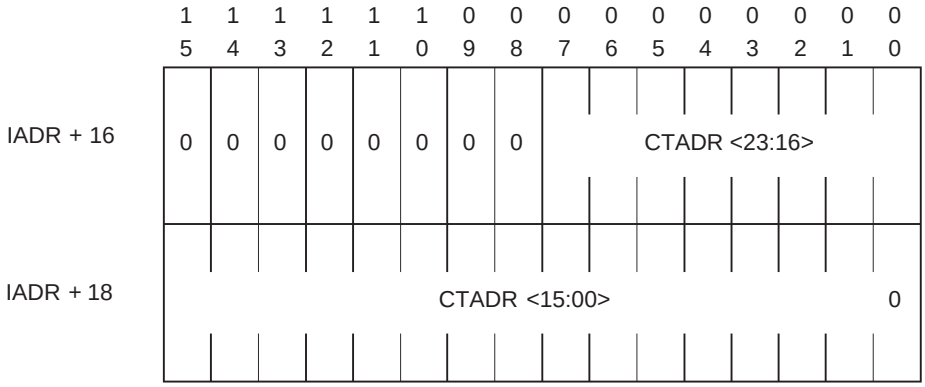
4.2.2 Timers/Counters

There are 8 independent counter-timers. The lower 8 bits of IADR+08 are used as a scaler for nT1, nT2 and TP. The scaler is driven by a clock which is 1/32 of SYSCLK. The dN1 is a 16 bit counter and is used to count the number of bytes in a frame. The counters nN1, nN2, and nN3 are used for the LMI frames. The Host will write the periods of all the timers/counters into the Initialization Block.



TIMER	DESCRIPTION
User N392 / nN2	Number of errors occuring on the LMI channel before an alarm is declared. In **non-Auto LMI Mode**, timer time-outs are ignored and nN2 is only incremented when a STATUS frame is received with bad sequence number. In Auto LMI User & Bi-directional mode this is the User N392. The range for N392/nN2 must be 1 - 10 events.
User N393 / nN3	Measurement interval for N392/nN2. An alarm will be declared if there are errors in nN2 of the last nN3 LMI events. In **non-Auto LMI Mode**, timer time-outs are ignored and nN3 window is only advanced when a STATUS frame is received In Auto LMI User & Bi-directional mode this is the User N393. NOTE: nN2 must be less than or equal to nN3 and the range of nN3 must be 1 - 10 events.
Ntwk N392	Network N392. In Auto LMI Network & Bi-directional mode, this is the number of errors occuring on the LMI channel before an alarm is declared.
Ntwk N393	Network N393. In Auto LMI Network & Bi-directional mode, this is the measurement interval for Ntwk N392. NOTE: Ntwk N392 and N393 are updated for LMI frames received with second set of sequence numbers in Bi-directional mode
dN1	MAXIMUM FRAME LENGTH. This field must contain the two's complement of one less than the maximum allowable frame length, in bytes. Any frame that exceeds this count will be discarded. NOTE: The DLCI header and CRC are included in the maximum frame length count.
nN1 / N391	The rate at which Full STATUS_ENQUIRY frame is sent to the network by the MK50H28 upon hosts request. This field must contain the two's complement of one less than the desired value. If CSR2<14> bit EIBEN =1, the MK50H28 will expect the value for nN1 counter to be located in the upper byte of IADR+40.
SCALER	TIMER PRESCALER. Timers nT1, nT2 and TP are scaled by this number. The prescaler is incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field is interpreted as the two's complement of the prescaler period. If CSR2<14> bit EIBEN =1, the MK50H28 will use the entire 16-bit value at IADR+08 as the prescaler value. This may be required to achieve longer timer values when operating at high SYSCLK speeds. NOTE: a prescale value of one gives the smallest amount of scaling to the timers (64 clock pulses), zero gives the largest (8224 clock pulses if EIBEN=0, or 2,097,184 clock pulses if EIBEN=1).
nT1 / T391	USER POLL TIMER. In **Auto LMI mode**, the nT1/T391 timer is started when a STATUS ENQUIRY frame is transmitted. Following the expiration of this timer, the device transmits another STATUS ENQUIRY frame and increments the nT1/T391 Timeout Error Counter if a STATUS frame was not received within the polling interval. This is not valid for LMI frames with second set of sequence numbers. In **non-Auto LMI mode**, the nT1/T391 timer is started by issuing a Start Timer nT1/T391 user primitive 8. Only in this mode, does the device issue a Timer Expiration provider primitive 8 indicating that the nT1/T391 timer has expired. This field must contain the two's complement of the period of the Timer nT1. NOTE: nT1/T391 must be less than nT2/T392.
nT2 / T392	NETWORK POLL TIMER. In **Auto LMI mode**, the nT2/T392 timer is started when a STATUS frame is transmitted. Following the expiration of this timer the device increments the nT2/T392 Timeout Error Counter if a STATUS ENQUIRY frame was not received within the poll interval. This is not valid for LMI frames with second set of sequence numbers. In **non-Auto LMI mode** the nT2/T392 timer is started by issuing a Start Timer nT2 user primitive 9. Only in this mode, does the device issue a Timer Expiration provider primitive 9 indicating that the nT2 timer has expired. NOTE: nT2/T392 must be greater than nT1/T391.
TP	TRANSMIT POLLING PERIOD. This scaled timer works on the Context Table on a per channel basis. No attempt to transmit a frame on a link is made until TP expires. When the TP expires the MK50H28 will first check to see whether the next channel is ready (i.e., TXRDY = 1). If TXRDY is set, it will service that channel. Then it will either jump, based on ENIDX bit being set, or continue to the next sequential channel. The MK50H28 will continue this process until it finds a CT Entry with the EOR bit set, causing the device to go to the begining of the CT and service the first Non-LMI channel. This field must contain two's complement of the period of the timer TP. **NOTE:** Once the MK50H28 finishes servicing a channel (transmitting frames), it waits for TP to expire before begining to poll for the next available channel that has frames to be transmitted. The MK50H28 continues its search from channel to channel, without waiting for TP to expire, until it finds the next available channel that has frames to be transmitted. Setting the TDMD bit causes the MK50H28 to immediately begin polling without waiting for TP to expire.

4.2.3 Context Table (CT) Address



BIT	NAME	DESCRIPTION
15:08	0	Reserved, must be written as a zero.
07:00/15:00	CTADR	CONTEXT TABLE ADDRESS. The CT Address must begin on a word boundary.

4.2.4 Context Table (CT)

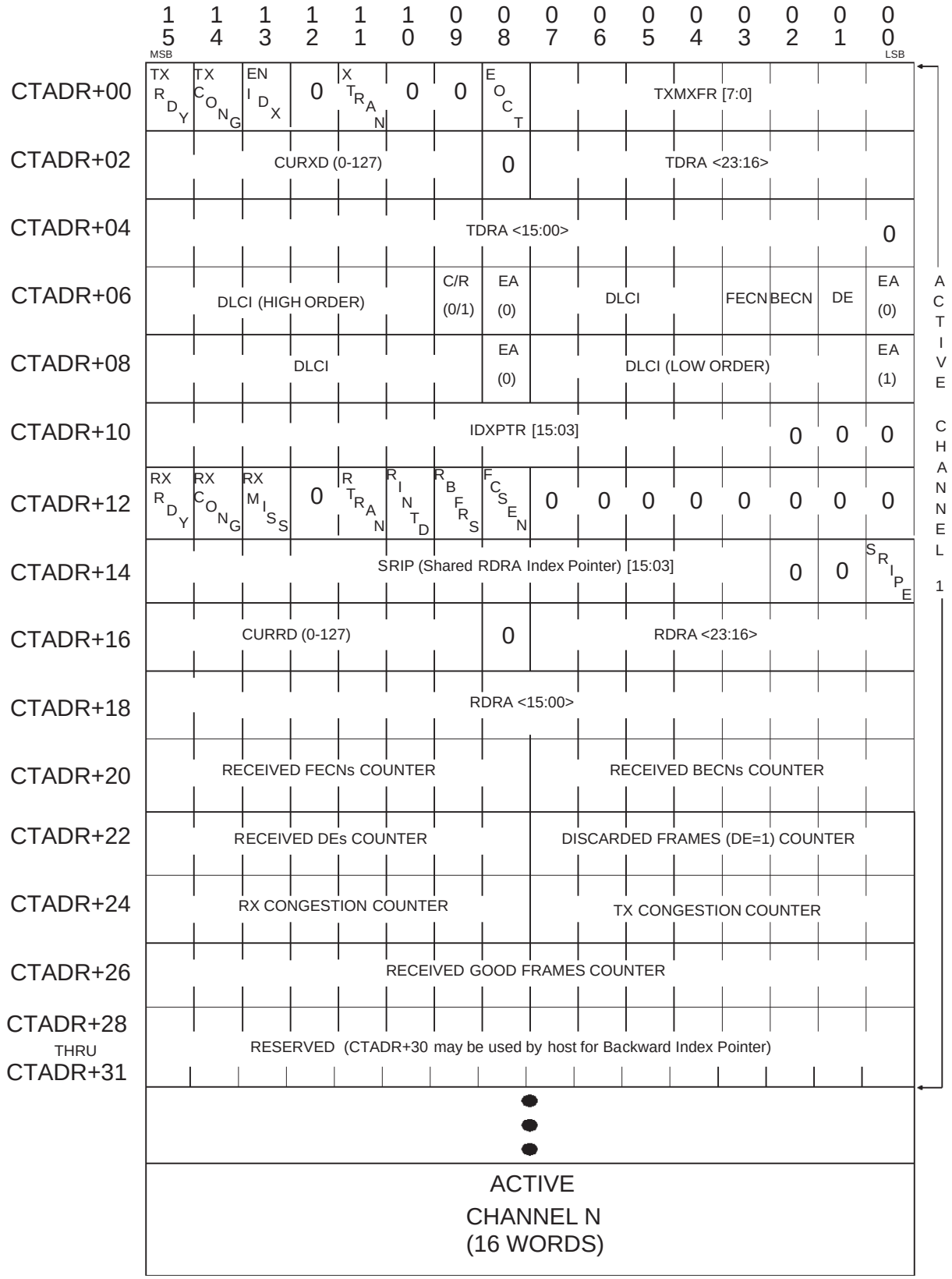
The MK50H28 performs multi-tasking by means of a Context Table (CT). Each entry in this table contains all the information relevant to one individual DLCI channel. Associated with each CTentry are a set of descriptor rings that are used for transmitting and receiving frames. Through the use of the SRIP field in the CT, more than on CT entry (or DLCI) may share the same Receive Rescriptor Ring while still keeping the individual DLCI statistics and error counters separately in each CT entry. All channel entries, except the LMI Channel (CT0), have equal priority. Each channel entry requires 16 words (or 32 bytes) of memory in the CT, and all channel entries in the Context Table are identical.

The MK50H28 sequentially scans each entry in the CT for any available frames to be transmitted, unless the ENIDX bit is set or scanning is interrupted by setting PTDMD in CSR2. If the MK50H28 finds the ENIDX bit set when scanning a CT entry, it unconditionally jumps to the CT entry pointed to by the IDXPTR field. Finally, the end of CT is marked by setting the EOCT bit in the last channel entry. In the Information Transfer phase, the MK50H28 is initialized to start transmission from the first non-LMI CT entry (the second CT entry: CT1). Upon finding the TXRDY bit set, it then reads the Transmit Descriptor Ring entry determined by the Transmit DescriptorRing Address and the CURXD index found in the CT. If the MK50H28 then finds the OWNA bit set in the Transmit Message Descriptor 0, it will transmit a frame with a DLCI found in the CT entry (at CTADR+06 & +08) and with data from the buffer pointed to by the Transmit Descriptor Ring entry. The MK50H28 automatically calculates and appends the correct CRC.

The MK50H28 reception process uses an Address Lookup Table (ALT) mechanism further specified in 4.2.6. The ALT contains a 1 word entry for each DLCI (selectable between 1024 or 8192 DLCIs) which consits of an index to the Context Table and an ACTIVE bit to indicate whether frames received with the associated DLCI should be processed or ignored. When a frame is received, its DLCI is used as an offset from the beginning of the ALT (containing the index to the CT for DLCI 0). If the ACTIVE bit is set for the ALT entry corresponding to the DLCI of the received frame, then the MK50H28 will proceed to access the CT entry pointed to by that ALT entry. The CT entry contains the address of the start of the corresponding Received Descriptor Ring and an index to the current descriptor in that ring. Each entry in the descriptor ring in turn points to a buffer into which the received frame is written. A received frame may span more than one buffer by use of the ELF buffer chaining mechanism described in 4.3.

Therefore, the MK50H28 transmission process is similar to the reception process except that it does not use the ALT (nor the ACTVE bit therein), but rather the TXRDY bit in the CT entry is used to determine what channels are active for transmission. In addition, both the ACTVE bit in the ALT and the RXRDY bit in CT must be set in order to receive frames.

Figure 8a: Context Table

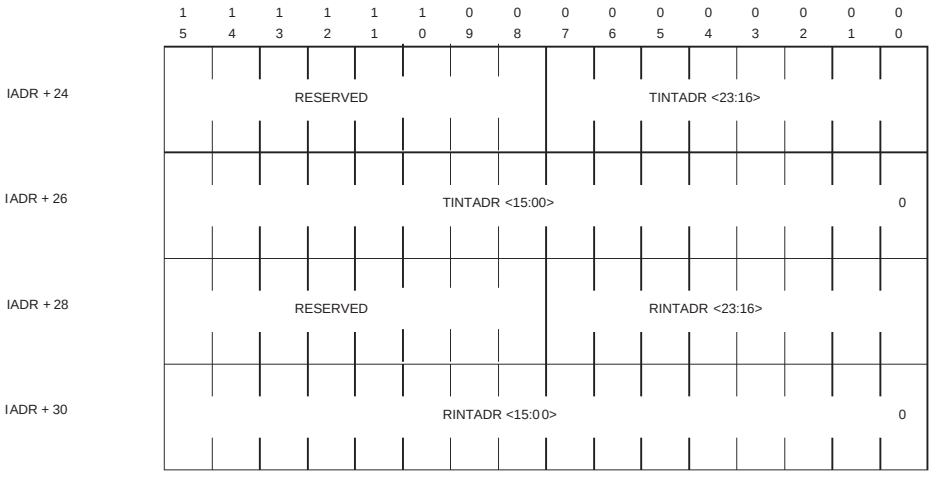


The contents of each CT entry block are described below:

WORD	NAME	DESCRIPTION
CT+00	TXRDY (15)	The host sets this bit only if the channel is ready to transmit. If this bit is not set, the MK50H28 will not transmit data for that channel.
	TXCONG (14)	The host sets this bit only if the channel is in congestion on the transmit path. If this bit is set, frames with the DE bit set in TMD0 will be discarded and not transmitted. This is also valid even if XTRAN=1. During normal transmission (i.e., no congestion), the host should clear this bit.
	ENIDX (13)	Enable Index Pointer to next entry in CT. Setting this bit, causes the device to jump and service the CT entry pointed to by the IDXPTR (CT+10) rather than servicing the next sequential CT entry.
	XTRAN (11)	Transmit Transparent. Setting this bit causes frames to be transmitted transparently from the corresponding TX Descriptor Ring and buffer without pre-pending any frame header. **This bit should typically be set for Transparent Mode operation.**
	EOCT (8)	End Of Context Table. Setting this bit indicates that this is the last entry in the CT. From here the device will advance to the begining of the CT and service the first non-LMI entry.
	TXMXFR (7:0)	Maximum Number of Frames to be consecutively transmitted. The device uses this value to determine the maximum number of frames to be transmitted before advancing to the next channel. This field is only used if the number of frames queued in the descriptor ring are greater than TXMXFR. This field must contain the two's complement number.
CT+02	CURXD (15:8)	Specifies the current transmit descriptor in the ring (0 - 127 in the upper 7 bits). This field should initially be written with zeroes.
CT+02,+04	TDRA	Starting address (must begin on a word boundary) of the Transmit Ring for channel.
CT+06,+08	DLCI Field	The MK50H28 can handle up to 4 octets of address field. For the LMI channel only, the MK50H28 transmits the entire address field as specified in the CT. For all other active channels, the explicit congestion bits (FECN, BECN, and DE) and the C/R bit are modified by the corresponding bits in the Transmit Message Descriptor 0 (TMD0) and should be written as 0. During reception for all the non-LMI active channels, the explicit congestion bits and the C/R bit will be written in the Receive Message Descriptor 0 (RMD0). For the LMI channel these bits are ignored.
CT+10	IDXPTR (15:3)	Index Pointer. The MK50H28 uses this field only when bit ENIDX is set. This field should contain the Index Pointer to the next CT entry to be serviced. All 13 bits of this field will be used as an index into the CT, regardless of the seting of DLCI1K in CSR2.
CT+12	RXRDY (15)	The host sets this bit only if the channel is ready to receive data. If the bit is not set, all received frames will be discarded for the channel.
	RXCONG (14)	The host sets this bit only if the channel is experiencing congestion on the receive path. When this bit is set the MK50H28 will discard only the received frames with Discard Eligibility (DE) = 1 for that channel. A counter in the CT (see below for more information) keeps track of received frames with DE = 1 that are discarded due to congestion. During normal reception (i.e., no congestion) & Transparent Mode this bit should be cleared to 0.
	RXMISS (13)	This bit is set by the MK50H28 when during reception of a frame either the channel is not ready (i.e., RXRDY = 0) or the receiver does not own a buffer (i.e., OWNA = 0. See 4.3.1 Receive Message Descriptor 0). Also if INEA = 1 in CSR 0, a MISS packet error interrupt will be generated under the above conditions. During normal reception the host should clear this bit. The address where the MISS occured can be determined by issuing a Status Request primitive. For more information see under Status Buffer.
	RTRAN (11)	Receive Transparent. When RTRAN=1, received frames will be written into the corresponding RX Descriptor Ring buffer without stripping any frame header, and FECN, BECN & DE bits in RMD0 will not be updated. CT counters and statistics will still be updated. **This bit should be set for Transparent Mode Operation.**
	RINTD (10)	Receive Interrupt Disable. Setting this bit prevents the device from generating Receive Interrupts (RINT) for this channel.
	RBFRS (9)	Receive Bad Frames. If set, the MK50H28 will receive both aborted and Bad FCS frames. For such received frames the FRER bit in the RMD0 will be set.
	FECSEN (8)	FCS Pass-Through Enable. Setting this bit allows the FCS or CRC to be stored in the buffer along with the frame data.

WORD	NAME	DESCRIPTION
CT+14	SRIP	Shared Receive Descriptro Ring Index Pointer. This field contains the Index Pointer to the CT entry with the CURRD and RDRA (CTADR+14, +16) to be used for received frames rather than the CURRD & RDRA specified in the current CT entry, if SRIPE = 1. All 13 bits of this field will be used to index into the CT, regardless of DLCI1K setting in CSR2.
	SRIPE(00)	SRIP Enable. **When set, this bit enables the sharing of one Receive Descriptor Ring by many DLCIs or CT entries**. When SRIPE=1, the Receive Descriptor Ring and buffer associated with the CURRD and RDRA values in the CT entry pointed to by the SRIP Index Pointer will be used for the received frame rather than the CURRD and RDRA values in the current CT entry associated with the DLCI of the received frame. The RCCNT & XCCNT used will also be those in the CT entry pointed to by the SRIP.
CT+16	CURRD (15:8)	Specifies the current receive descriptor in the ring (0 - 127 in the upper 7 bits). This field should initially be written with zeroes.
CT+16,+18	RDRA	Starting address of the Receive Descriptor Ring for a channel. It must be word aligned.
CT+20	Rcv FECNs	Counter for keeping track of the FECNs received when a channel is ready.
	Rcv BECNs	Counter for keeping track of the BECNs received when a channel is ready.
CT+22	Rcv DEs	Counter for keeping track of the DEs received when a channel is ready.
	Discard Frames	Counter for keeping track of received frames with DE = 1 that are discarded due to congestion on a channel. Incremented for LMI frames is received on CT0 inconsistent with the operating mode. (Stop or Re-Initialization will not reset this nor any CT Counter.)
CT+24	RCCNT	RX Congestion Counter. This counter is incremented each time a received frame is placed into the RX descriptor Ring for that channel. The MK50H28 does this just prior to clearing the OWNA bit(s) for the descriptor(s) corresponding to each received frame. NOTE: This counter should be programmed with an initial value of 00. It is the responsibility of the host processor to decrement and/or reset this counter as needed to do Receive Descriptor Ring congestion monitoring
	XCCNT	TX Congestion Counter. This counter is incremented each time a frame is transmitted from the TX descriptor Ring for that channel. The MK50H28 does this just prior to clearing the OWNA bit(s) for the descriptor(s) corresponding to each tranmitted frame. NOTE: It is the responsibility of the host processor to program this counter with the 2's complement value of the number of descriptors that it filled with frame data to be transmitted, if Transmit Descriptor Ring congestion monitoring is needed.
CT+26	RGF Cnt	Received Good Frames Counter. (Stop or Re-Init will not reset this nor any CT Counter.)
CT+28 - 31	0	Reserved. Must be written as zeros.

4.2.5 Interrupt Descriptor Ring Addresses

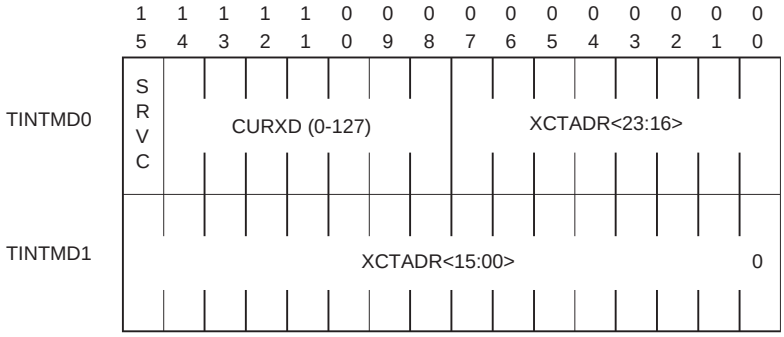


BIT	NAME	DESCRIPTION
15:08	0	Reserved, must be written as a zero.
07:00/15:00	TINTADR	Transmit Interrupt Descriptor Ring Address. (Must begin on a word boundary).
07:00/15:00	RINTADR	Receive Interrupt Descriptor Ring Address. (Must begin on a word boundary).

4.2.5a Transmit and Receive Interrupt Descriptor Rings

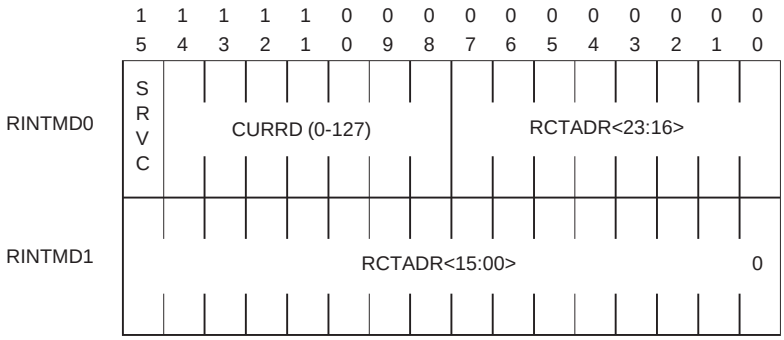
The MK50H28 has two descriptor ring structures for the purpose of queuing Transmit and Receive interrupts. The pointers to these two descriptor rings are located at IADR+24 through IADR+30. These descriptor rings consist of 128 entries. Each entry consists of two 16-bit words containing the 24-bit address of the Contest Table entry (XCTADR, RCTADR)corresponding to the interrupt, a 7-bit field for the descriptor index (CURXD, CURRD) into the associated descriptor ring, and a SRVC bit to indicate whether the interrupt has been serviced. No entry will be made in the Receive Interrupt Descriptor Ring (nor will interrupt be generated) if bit RINTD (CTADR+12 <10>) is set; likewise for TINTD (TMD0<08>).

4.2.5a.1 Transmit Interrupt Descriptor Ring Entry



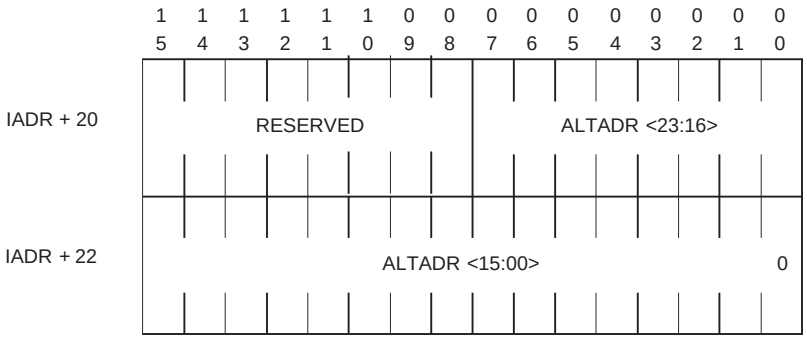
BIT	NAME	DESCRIPTION
15	SRVC	This bit is set by the MK50H28 when it writes an interrupt to the Interrupt Descriptor Ring and should be cleared by the host when it Services the interrupt. If it attempts to write TX interrupt information to a Transmit Interrupt Ring entry for which SRVC is not clear , the MK50H28 will issue PPRIM 7 with PPARM=0 (Tx Int MISS) in addition to giving TINT.
14:08	CURXD	Specifies the current transmit descriptor (0-127) at the time the interrupt ocurred.
07:00/15:00	XCTADR	Transmit Context Table Address. Indicates address of the CT entry at the time the interrupt ocurred. NOTE: XCTADR specifies which CT entry, and CURXD specifies the descriptor within the Tx Ring associated with the CT entry for which the interrupt ocurred.

4.2.5a.2 Receive Interrupt Descriptor Ring Entry



BIT	NAME	DESCRIPTION
15	SRVC	This bit is set by the MK50H28 when it writes an interrupt to the Interrupt Descriptor Ring and should be cleared by the host when it Services the interrupt. The MK50H28 will issue PPRIM 7 with PPARM=1(Rx Int MISS) in addition to RINT, and it will discard the received frame if it is unable to write to the Rececive Interrupt ring due to SRVC not being clear.
14:08	CURRD	Specifies the current receive descriptor (0-127) at the time the interrupt ocurred.
07:00/15:00	RCTADR	Receive Context Table Address. Indicates address of the CT entry at the time the interrupt ocurred. NOTE: RCTADR specifies the CT entry, and CURRD specifies the descriptor within the Rx Ring associated with the CT entry for which the interrupt ocurred.

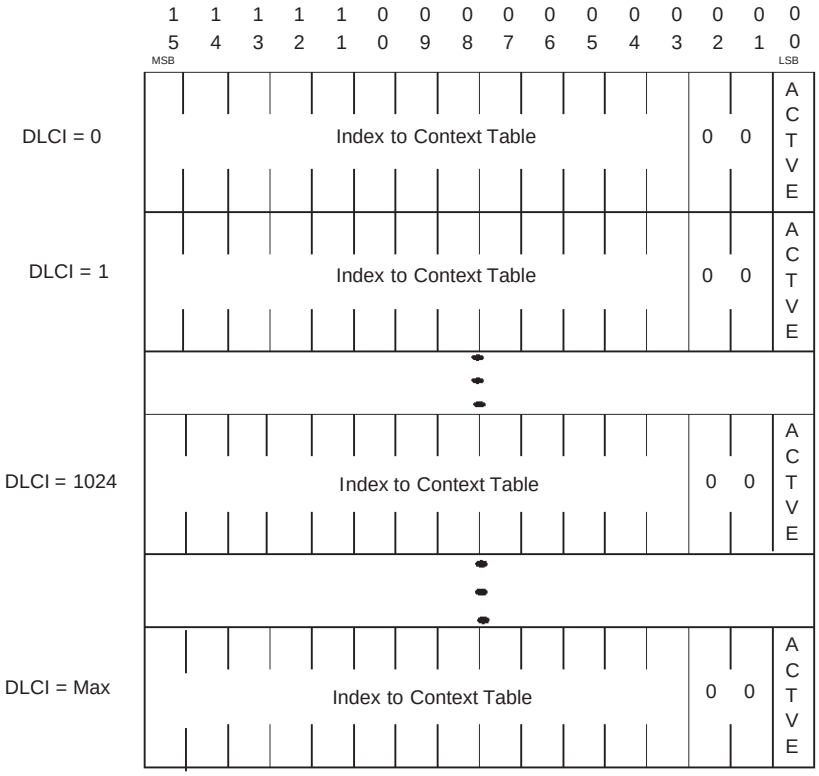
4.2.6 Address Lookup Table (ALT) Address



BIT	NAME	DESCRIPTION
15:08	0	Reserved, must be written as a zero.
07:00/15:00	ALTADR	ADDRESS LOOKUP TABLE ADDRESS. The ALT Address must begin on a word boundary.

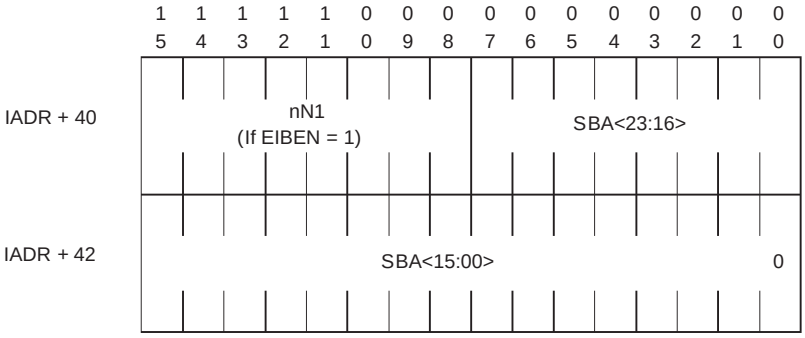
4.2.6a Address Lookup Table (ALT)

The ALT can support a maximum of 1024 or 8192 active DLCIs depending upon the setting of the DLCI1K bit in CSR2. Each channel needs a word (= 2 bytes) in the ALT. (NOTE: The ALT is only used by the receive process)



BIT	NAME	DESCRIPTION
0	ACTIVE	This bit is set by the host if the corresponding DLCI is active. If this bit is not set, the data received for the DLCI will be ignored by the MK50H28. This bit is only used by the receive process.
14:13	0	Reserved. Must be written as zeros.
15:03	Index to CT	13-bit index to Context Table.

4.2.7 Status Buffer Address



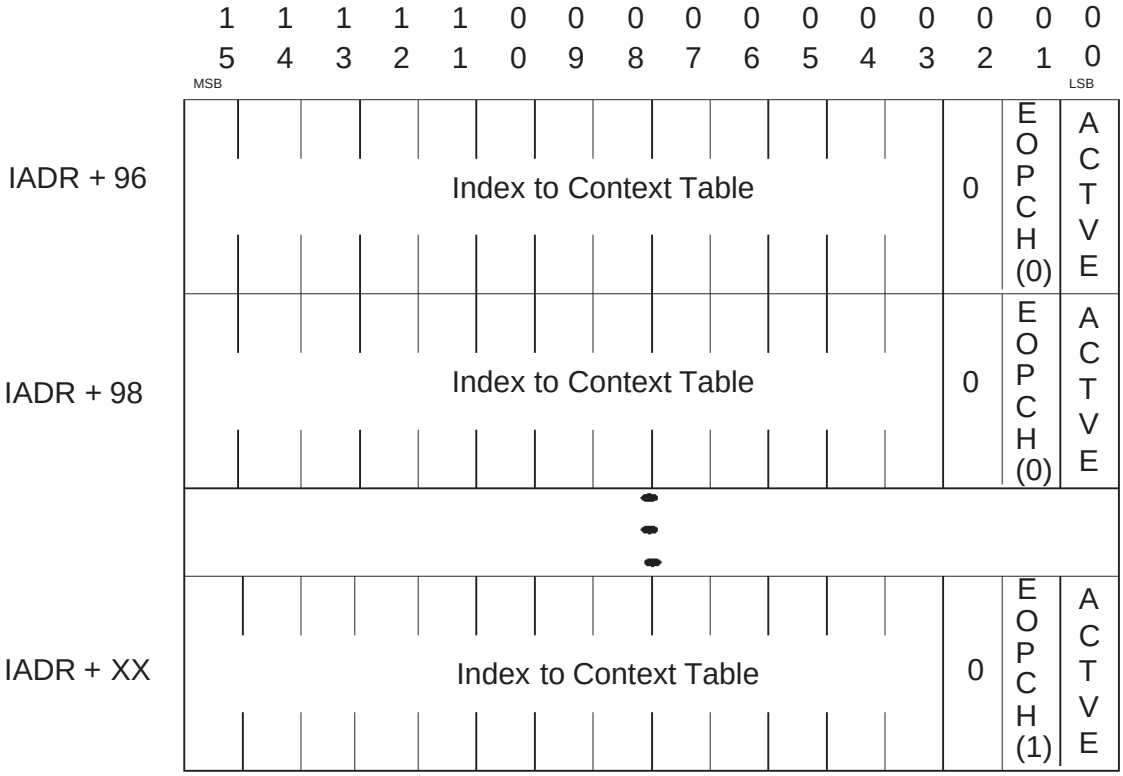
BIT	NAME	DESCRIPTION
15:08	0	Must be written as zeroe if CSR2<14> bit EIBEN = 0
07:00/15:00	SBA	STATUS BUFFER ADDRESS points to a 9 word status buffer into which status information is placed upon the issuance of the Status Request primitive by the HOST. The status buffer must begin on a word boundary.

4.2.8 Error Counters Twenty two words in the Initialization Block are reserved for use as error counters and statistics which the MK50H28 will increment as required. These counters are intended for use by the host CPU for statistical analysis on the LMI channel. The Error Counters at IADR+44, 46,48,64, and 66 are applicable to all the active channels (i.e., both LMI and non-LMI). If RBFRS bit (in Context Table CTADR+12, bit 09) = 0, bad frames are ignored by the MK50H28. However, if RBFRS = 1 even the bad frames will be received by the MK50H28. For such received bad frames the FRER bit will be set in the Receive Message Descriptor 0. The MK50H28 will only increment the Error Counters; it is up to the user to clear, reset, or preset them (Stop or Re-initialization will not reset them). The error counters are:

Memory Address	Error Counter
IADR+44	Bad Frames Received (Bad FCS or Non-Octet Aligned)
IADR+46	Short Frames (less than: 2 bytes non-LMI, 3 bytes Annex A/D, 4 bytes other LMI frame)
IADR+48	Aborted Frames received
IADR+50	LIV/LMI Frames with missing or incorrect Report Type IE received. (The appropriate corresponding IE Identifiers were not received). (Annex A)
IADR+52	LIV/LMI Frames with incorrect Report Type format Received. (Annex A or Annex D)
IADR+54	LIV/LMI Frames with incorrect Report Type format Received. (Annex A)
IADR+56	Number of nT1/T391 timeouts for LIV/LMI frames. This error counter is only incremented when nT1 expires without having received a STATUS frame.
IADR+58	Number of nT2/T392 timeouts for LIV/LMI frames. This error counter is only incremented when nT2 expires without having received a STATUS ENQUIRY frame.
IADR+60	Frames received with bad sequence errors.
IADR+62	Number of Annex D frames received with bad format.
IADR+64	Number of good frames received on unknown or inactive DLCIs.
IADR+66	Number of received frames exceeding the maximum frame length dN1.
IADR+68	LIV Status Enquiry Messages Received
IADR+70	LIV Status Messages Received
IADR+72	LIV Full Status Enquiry Messages Received
IADR+74	LIV Full Status Messages Received
IADR+76	Asynchronous Messages Received
IADR+78	LIV Status Enquiry Messages Transmitted
IADR+80	LIV Status Messages Transmitted
IADR+82	LIV Full Status Enquiry Messages Transmitted
IADR+84	LIV Full Status Messages Transmitted

4.2.9 Priority DLCI Block

The Priority DLCI Block (PDB) is a mechanism through which the host can demand the MK50H28 to immediately service certain desired DLCIs. The host should first set up entries in the PDB before setting the PTDMD bit in CSR2. In response to that, the MK50H28, after completing transmission service of its current DLCI, will jump to the PDB rather than advancing to the next entry in the Context Table. After servicing all active entries in the PDB, the MK50H28 will return to the Context Table and resume the transmission service that was in progress before it was interrupted. (NOTE: A maximum of 256 entries are allowed in the PDB.) The following is the format of the Priority DLCI Block.



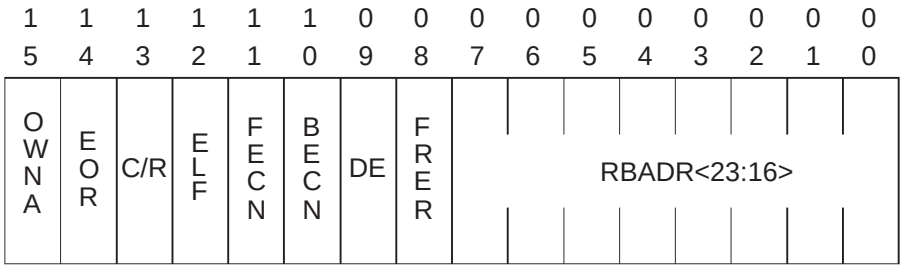
BIT	NAME	DESCRIPTION
15	Index to CT	13-bit index into Context Table
02	0	Reserved. Must be written as zeros.
01	EOPCH	End of PDB. Setting this bit to 1 indicates that this is the last entry in the PDB
00	ACTIVE	This bit is set by the host if the corresponding index into the Context Table is active. The MK50H28 ignores the entry if this bit is not set.

4.3 Receive and Transmit Descriptor Rings

Each active channel has an associated transmit and receive ring (Figure 3). Each ring can have a maximum of 128 descriptors, and each descriptor in the ring is a 4 word entry. Each ring is terminated by setting the EOR bit in the last descriptor. Except for the first word (see below for RMD0 or TMD0), all the descriptors are identical for both LMI and non-LMI channels. NOTE: The Buffer Byte Count (BMCT) for LMI channels should be greater than 14 bytes. The following is the format of the receive and transmit descriptors.

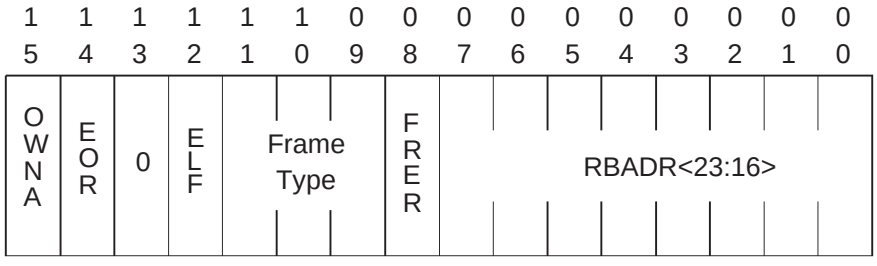
4.3.1 Receive Message Descriptor Entry

4.3.1.1 Receive Message Descriptor 0 (RMD0) For Non-LMI Channel



BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero the HOST owns this descriptor. When this bit is a one the MK50H28 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided a valid frame has been received. The Host sets the OWNA bit after emptying the buffer. Once the MK50H28 or the Host has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	EOR	End Of Ring. This bit is set by the host to indicate that this is the last descriptor in the ring.
13	C/R	Command/Response Indication Bit. This bit equals the state of the C/R bit for the received frame.
12	ELF	End of Long Frame indicates that this is the last buffer used by the MK50H28 for this frame. ELF is used for data chaining buffers and is set by the MK50H28. ELF=0 indicates that this buffer is one in a chain. When not chaining, ELF will always be one.
11	FECN	Forward Explicit Congestion Notification Bit. This bit equals the state of the FECN bit for the received frame.
10	BECN	Backward Explicit Congestion Notification Bit. This bit equals the state of the BECN bit for the received frame.
09	DE	Discard Eligibility Bit. This bit equals the state of the DE bit for the received frame.
08	FRER	Frame in Error Bit. This bit is valid only if RBFRS is set in CTADR+12. This bit will be set by the MK50H28 only if an aborted or a bad FCS frame is received.
07:00	RBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H28.

4.3.1.2 Receive Message Descriptor 0 (RMD0) For LMI Channel

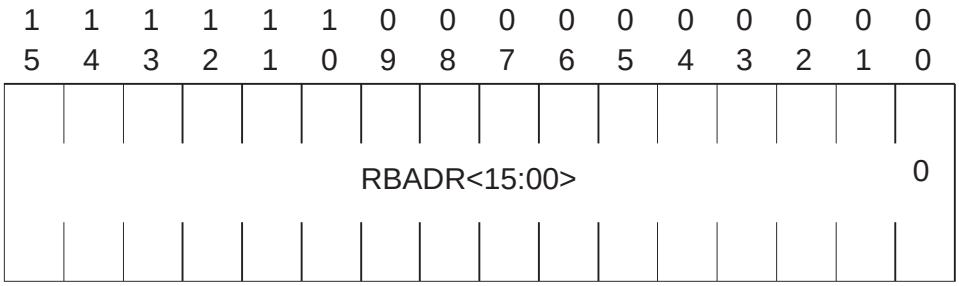


BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero, the HOST owns this descriptor. When this bit is a one the MK50H28 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry, provided a valid frame has been received. The Host should set the OWNA bit after emptying the buffer. Once the MK50H28 or Host relinquishes ownership of a buffer, it may not change any field in the descriptor entry.

4.3.1.2 Receive Message Descriptor 0 (RMD0) For LMI Channel (Contimued)

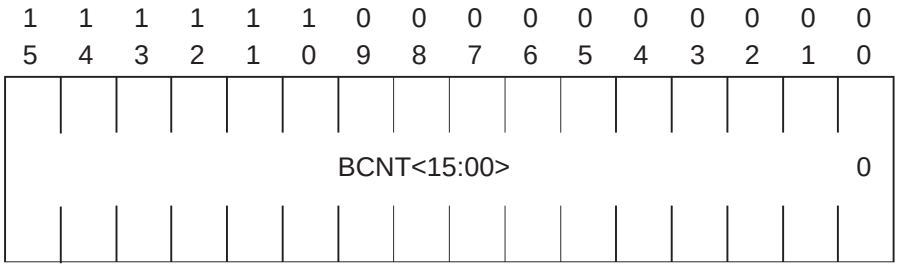
BIT	NAME	DESCRIPTION
14	EOR	End Of Ring. Setting this bit to 1 indicates that this is the last descriptor in the ring.
13	0	Reserved. Must be written as zero.
12	ELF	End of Long Frame indicates that this is the last buffer used by the MK50H28 for this frame. ELF=0 indicates that this buffer is one in a chain. ELF=1 indicates the end of the buffer chain. ELF is set by the MK50H28. When not chaining, ELF will always be one.
11:09	LMI Frame Type Received	These bits define the type of frame received, as detailed in the following table: Bit Encoding (MSB - LSB) — Frame Type 000 — SVC Frame or Transparent Mode frame 001 — Reserved 010 — Full Status Enquiry frame 011 — Status Enquiry frame (LIV only) 100 — Asynchronous Status Frame 101 — Update Status frame 110 — Full Status frame 111 — Status frame (LIV only)
08	FRER	Frame in Error Bit. This bit is valid only if RBFRS is set in CSR 2. This bit will be set by the MK50H28 only if an aborted or a bad FCS frame is received.
07:00	RBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H28.

4.3.1.3 Receive Message Descriptor 1 (RMD1)



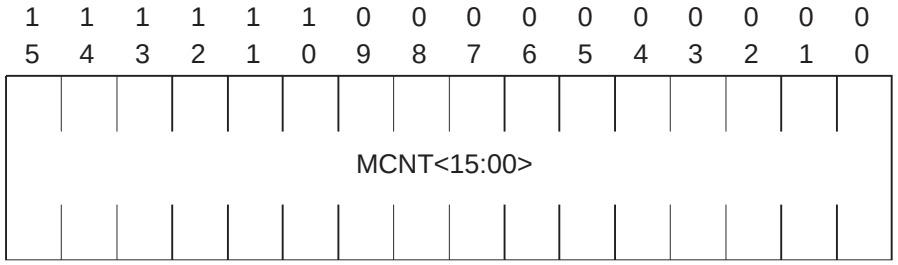
BIT	NAME	DESCRIPTION
15:01	RBADR	The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK50H28. The receive buffers must be word aligned.

4.3.1.4 Receive Message Descriptor 2 (RMD2)



BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK50H28. The value of BCNT must be an even number. For LMI channels this field should be set to greater than 14 bytes.

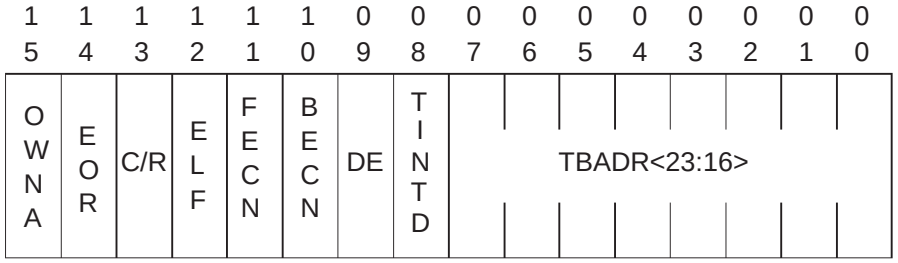
4.3.1.5 Receive Message Descriptor 3 (RMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message Byte Count is the length, in bytes, of the received signal unit. MCNT is valid only when ELF is set to a one. MCNT is written by MK50H28 and read by the Host. If ELF is set to a zero the entire buffer has been utilized and the message byte count is given in BCNT above. The value of this field is expressed in two's complement.

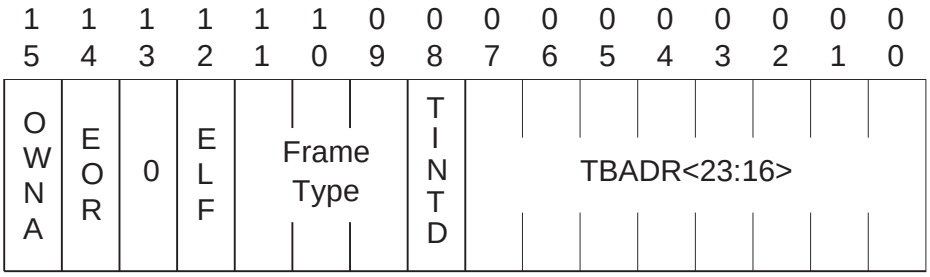
4.3.2 Transmit Message Descriptor Entry

4.3.2.1 Transmit Message Descriptor 0 (TMD0) For Non-LMI Channel



BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero, the HOST owns this descriptor. When this bit is a one the MK50H28 owns this descriptor. The host sets the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK50H28 releases the descriptor after transmitting the buffer. After the MK50H28 or the Host has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	EOR	End Of Ring. Setting this bit to 1 indicates that this is the last descriptor in the ring.
13	C/R	Command/Response Indication Bit. This bit determines the state of the C/R bit for the transmitted frame.
12	ELF	End of Long Frame indicates that this is the last buffer used by the MK50H28 for this frame. It is used for data chaining buffers. ELF is set by the Host. When not chaining, ELF should be set to a one.
11	FECN	Forward Explicit Congestion Notification Bit. This bit determines the state of the FECN bit for the transmitted frame.
10	BECN	Backward Explicit Congestion Notification Bit. This bit determines the state of the BECN bit for the transmitted frame.
09	DE	Discard Eligibility Bit. This bit determines the state of the DE bit for the transmitted frame. If in the CT entry TXCONG=1, any frame with DE=1 will not be transmitted, but discarded.
08	TINTD	Transmit Interrupt Disable. If this bit is set, no transmit interrupt is generated when ownership of this descriptor is released back to the host.
07:00	TBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H28.

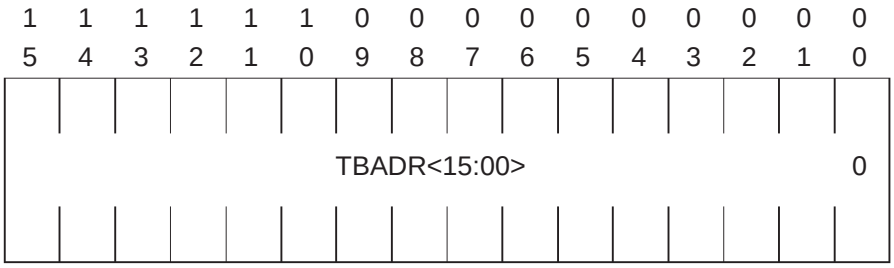
4.3.2.2 Transmit Message Descriptor 0 (TMD0) For LMI Channel



BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero, the HOST owns this descriptor. When this bit is a one the MK50H28 owns this descriptor. The host sets the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK50H28 releases the descriptor after transmitting the buffer. After the MK50H28 or the Host has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	EOR	End of Ring. Setting this bit to 1 indicates that this is the last descriptor in the ring.
13	0	Reserved. Must be written as zero
12	ELF	End of Long Frame indicates that this is the last buffer used by the MK50H28 for this frame. It is used for data chaining buffers. ELF is set by the Host. When not chaining, ELF should be set to a one.

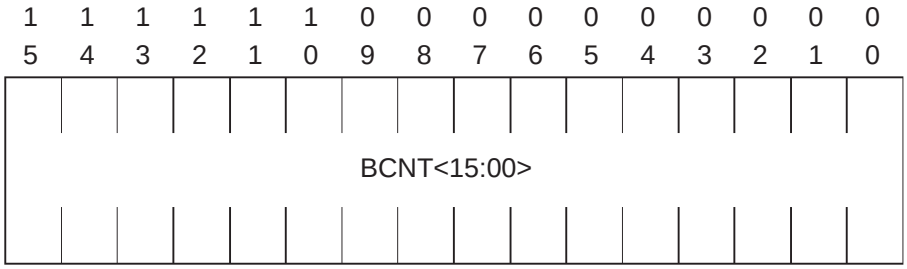
BIT	NAME	DESCRIPTION
11:09	LMI Frame Type to be Transmitted	These bits define the type of frame to be transmitted when transmission occurs due to LMI polling (enabled by UPRIM 8 with UPARM=2 - see 4.1.2.2). Bit Encoding (MSB - LSB) — Frame Type 000 — SVC Frame or Transparent Mode frame 001 — Reserved 010 — Full Status Enquiry frame 011 — Status Enquiry frame (LIV only) 100 — Asynchronous Status Frame 101 — Update Status frame 110 — Full Status frame 111 — Status frame (LIV only)
11:09	0	Reserved. Must be written as zero.
08	TINTD	Transmit Interrupt Disable. If this bit is set, no transmit interrupt is generated when ownership of this descriptor is released back to the host.
07:00	TBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H28.

4.3.2.3 Transmit Message Descriptor 1 (TMD1)



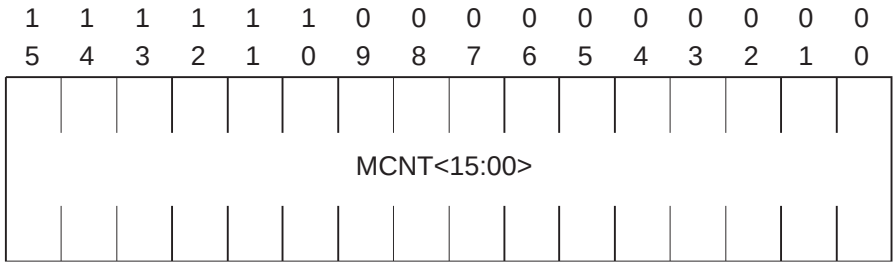
BIT	NAME	DESCRIPTION
15:00	TBADR	The Low Order 16 address bits of the buffer pointed to by this descriptor. TBADR is written by the Host and unchanged by MK50H28. The least significant bit is zero since the descriptor must be word aligned.

4.3.2.4 Transmit Message Descriptor 2 (TMD2)



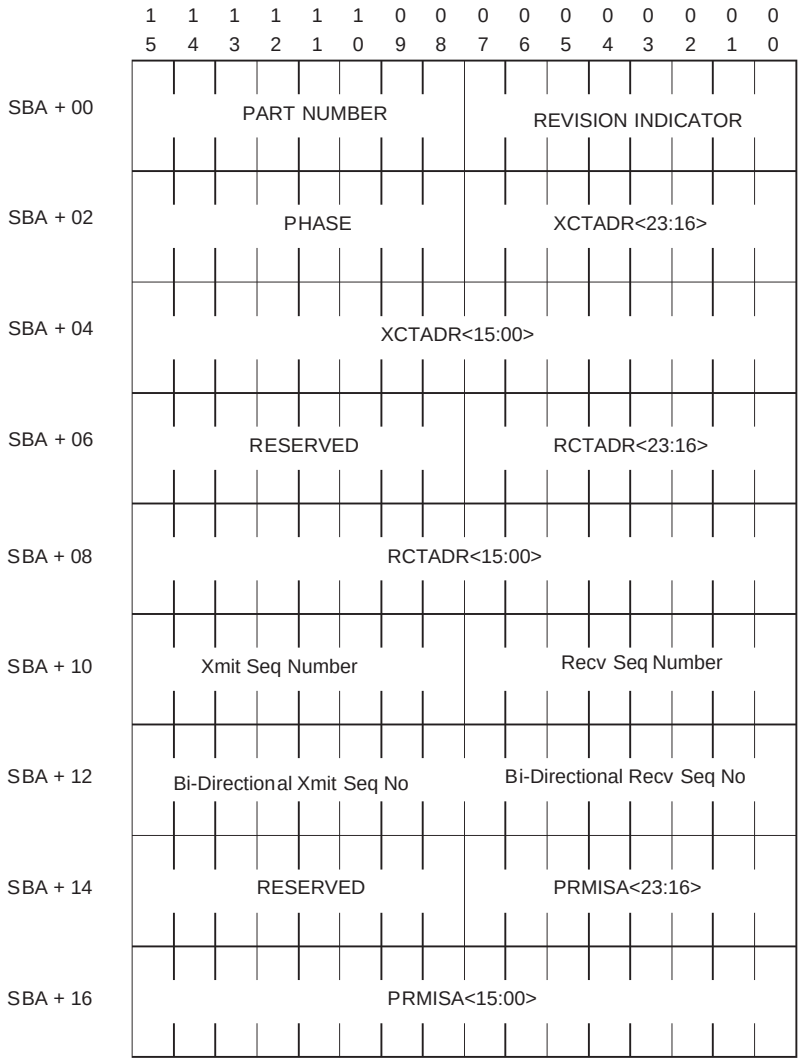
BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the usable lenght of the buffer pointed to by this descriptor expressed in two's complement. Thiis field is not used by the MK50H28.

4.3.2.5 **Transmit Message Descriptor 3 (TMD3)**



BIT	NAME	DESCRIPTION
15:00	MCNT	Message byte count is the length, in octets, of the data contained in the corresponding buffer. The value of this field is expressed in two's complement.

4.3.3 **Status Buffer**



FIELD	DESCRIPTION
PART NUMBER	Indicates the part number (28 Hex) for the MK50H28.
REV INDICATOR	Indicates the current revision of the part.
PHASE	Indicates the current phase of operation. 0: Stopped, TD is held at 1's, RD is ignored 10: Information Transfer Only 11: Information Transfer + Auto LMI Transmission - User Mode 12: Information Transfer + Auto LMI Transmission - Network Mode 13: Information Transfer + Auto LMI Transmission - Bi-directional Mode 20: Transparent Mode (all channels are treated as data channels) 30: Initialization Complete
XCTADR:<23:00>	Current Transmit Context Table Address. This pointer indicates the address of the entry in Context Table Memory Structure corresponding to the descriptor ring from which frames are currently being transmitted.
RCTADR:<23:00>	Current Receive Context Table Address. This pointer indicates the address of the entry in Context Table Memory Structure corresponding to the descriptor ring into which received frames are currently being placed.
Xmit Seq Number	Transmit Sequence Number. The Current Sequence number used by the most recently transmitted LMI frame.
Recv Seq Number	Receive Sequence Number. The Current Sequence number used by the most recently received LMI frame
By-Directional Xmit Seq	By-Directional Transmit Sequence Number. The Current Sequence number used by the most recently transmitted LMI frame using the Optional Bi-directional Procedures
By-Directional Recv Seq	By-Directional Receive Sequence Number. The Current Sequence number used by the most recently received LMI frame using the Optional Bi-directional Procedures
PRMISA:<23:00>	Previous MISS Address. This pointer indicates the address in the Context Table for the most current receive MISS. This value is updated by the MK50H28 whenever a MISS condition occurs and does not require issuing a Status Request primitive to update it, as do all the other fields in the Status Buffer.

4.4 Detailed Programming Procedures

4.4.1 Initialization (Reading of Initialization Block)

The following procedure should be followed to initialize the MK50H28:

1. Setup bus control information in CSR4.
2. Setup the Initialization Block, Address Lookup Table, Context Table, and Descriptor Rings.
3. Load the address of the initialization block information into CSR's 2 and 3.
4. Issue the INIT primitive through CSR1 (write 4200H to CSR1) instructing the MK50H28 to read the initialization block pointed to by CSR's 2 and 3.
5. Wait for the INIT confirmation primitive (CSR1 = 0242H) from the MK50H28. Then clear the PAV bit in CSR1 (write 0040H to CSR1).
6. Issue the Start primitive through CSR1 (write 4300H to CSR1). The MK50H28 will now be in INFORMATION TRANSFER phaseand the MK50H28 will begin to continuously transmit flags.
7. Enable interrupts in CSR0 if desired.

4.4.2 Link Setup

4.4.2.1 User Mode (Auto LMI Mode)

The following procedure should be followed for establishing a link.

1. Make sure that the ACTIVE bit in the Address Lookup Table is set for the LMI channel.
2. Issue the Auto LMI Primitive 7 with UPARM = 0 through CSR1 (write 4700H) to place the device in Auto LMI User Mode.

4.4.2.1 **User Mode (Auto LMI Mode) - Continued**

In User Mode the MK50H28 will perform the following functions:

1. Transmit STATUS ENQUIRY frames at an interval determined by the nT1 timer.
2. After every nN1 transmissions of STATUS ENQUIRY with Report Type of "LIV Only" the MK50H28 transmits a STATUS ENQUIRY with Report Type of "Full Status".
3. When a STATUS frame is received in response to a STATUS ENQUIRY, the receive sequence number received from the Network side is checked against the User send sequence number.
4. A received Full STATUS frame will be stored into the LMI channel buffer, the sequence number checking will be performed, and its reception will be indicated via Provider Primitive 13.
5. A received Asynchronous STATUS frame will be stored into the LMI channel buffer and its reception will be indicated via Provider Primitive 14.
6. An available transmit or receive buffer is not required for the MK50H28 automatic processing of "LIV only" frames.
7. A STATUS ENQUIRY frame (Full or LIV only) received in User mode will be discarded and the Discarded Frames Counter in Context Table entry 0 will be incremented.

4.4.2.2 **Network Mode (Auto LMI Mode)**

The following procedure should be followed for establishing a link.

1. Make sure that the ACTIVE bit in the ALT is set for the LMI channel.
2. Issue the Auto LMI Primitive 7 with UPARM = 1 through CSR1 (write 5700H) to place the device in Auto LMI Network Mode.

In Network Mode the MK50H28 will perform the following functions:

1. Automatically responds to STATUS ENQUIRY with Report Type of "LIV Only" by transmitting a STATUS frame with Report Type of "LIV Only" along with restarting the nT2 timer.
2. When a STATUS ENQUIRY with Report Type of "Full Status" is received, the device issues the LMI Received primitive 13 (with PPARM=1) and expects the host to respond with an LMI Status Request Primitive 11 with UPARM=0 (when ready to transmit the Full STATUS frame).
3. An available transmit or receive buffer is not required for the MK50H28 automatic processing of "LIV only" frames.
4. Asynchronous STATUS frames may be transmitted by placing the data to be transmitted into the appropriate buffer and issueing Primtive 11 with UPARM=2.
5. A STATUS frame (Full, LIV Only, or Asynchronous) received in Network mode will be discarded and the Discarded Frames Counter in Context Table entry 0 will be incremented.

4.4.2.3 **Bi-directional Procedures (Auto LMI Mode)**

The following procedure should be followed to implement the Optional Bi-directional Procedures

1. Make sure that the ACTIVE bit in the ALT and TXRDY in the CT are set for the LMI channel.
2. Make sure that the Transmit Ring Pointer, Current Transmit Descriptor and address field information in the CT is valid. This is necessary for transmission of Full STATUS frame.
3. Issue the Auto LMI Primitive with UPARM = 2 through CSR1 (write 6700H) to place the device in Bi-directional Mode. In Bi-directional Mode the MK50H28 will transmit STATUS ENQUIRY frames with one set of sequence numbers and use a separate set of sequence numbers to process received STATUS ENQUIRY frames. STATUS frames will be sent with the separate set of sequence numbers differing from those used in the processing of recived STATUS frames.

In Bi-directional Mode the MK50H28 will perform the following functions:

1. The MK50H28 supports this operation using separate User and Network sequence numbers and N392 and N393 counters.
2. The MK50H28 transmits STATUS ENQUIRY messages with a User set of sequence numbers at an interval determined by the nT1/T391 timer. The expected response is a STATUS frame with corresponding sequence numbers.

4.4.2.3 **Bi-directional Procedures (Auto LMI Mode) - Continued**

3. After every nN1/N391 transmissions of STATUS ENQUIRY with Report Type of "LIV Only", the MK50H28 transmits a STATUS ENQUIRY with Report Type of "Full Status".
4. A received Full STATUS frame will be stored into the LMI channel buffer, the sequence number checking will be performed, and its reception will be indicated to the host via Provider Primitive 13. A received Asynchronous STATUS frame will be stored into the LMI channel buffer and its reception will be indicated to the host via Provider Primitive 14.
5. The MK50H28 also automatically responds to a STATUS ENQUIRY ("LIV Only") frame received by transmitting a STATUS ("LIV Only") frame along with restarting the nT2 timer. When a "Full Status" STATUS ENQUIRY is received, the device issues the LMI Received primitive 13 (with PPARM=1) and expects the host to respond with LMI Status Request Primitive 11 with UPARM=0 (when ready to transmit the Full STATUS frame).
6. Asynchronous STATUS frames may be transmitted by placing the data to be transmitted into the appropriate buffer and issueing Primtive 11 with UPARM=2.

4.4.3 Sending Data On A Link

Use the following procedure to send a frame:

1. Make sure that ACTIVE bit in the ALT and TXRDY bit in the CT are set for that channel.
2. Make sure that the Transmit Ring Pointer, Current Transmit Descriptor and address field information in the CT is valid.
3. Wait for the OWNA bit of the current transmit descriptor to be cleared, if it is not already.
4. Fill the buffer associated with the current transmit descriptor with the data to be sent, or set the descriptor buffer address to any already filled buffer.
5. Repeat steps 3 & 4 for next buffer if chaining is necessary, setting ELF & MCNT appropriately.
6. Set the OWNA bit for each descriptor to be used in sending the frame.
7. Go on to next descriptor. The MK50H28 will clear OWNA bits when the frame has been transmitted.

4.4.4 Receiving Data On A Link

The following procedure should be followed when receiving a frame:

1. Make sure that ACTIVE bit in the ALT and RXRDY bit in the CT are set for that channel.
2. Make sure that the Index to CT in the ALT points to appropriate CT entry for that channel.
3. Also make sure that the Receive Ring Pointer, Current Receive Descriptor information in the CT is valid.
4. Make sure the OWNA bit of the current receive descriptor is clear.
5. A Receive Interrupt (RINT) will indicate reception of a frame.
6. Read the entry or entries in the Receive Interrupt Descriptor Ring that have the SRVC bit set. The Receive Context Table Address and Current Receive Descriptor index available here indicate the CT entry and the descriptor within the Rx Ring associated with the received frame.
6. Read data out of the buffer associated with the current receive descriptor.
8. Set the OWNA bit of the current receive descriptor to return ownership to the MK50H28.
9. If the ELF bit of the current receive descriptor is clear, then go on to the next descriptor and repeat from step 4 appending data from each buffer until a descriptor with ELF=1 is reached.
10. LMI frames received in any mode will not cause Receive Interrupts (RINT) to be generated, nor will the Receive Interrupt Ring be updated. Instead, the MK50H28 will issue primitives corresponding to the received LMI Frames which are not automatically processed by the MK50H28 (i.e. non "LIV only" frames). See the description of primitives in section 4.1.2.2.
11. For frames received on the LMI Channel (typically DLCI 0), bits 09-11 of the Receive Message Descriptor 0 (RMD0) for the LMI channel will indicate the type of frame received. A setting of 000 indicates a received SVC frame or Transparent Mode frame. See section 4.3.1.2 for details.

4.4.5 Receiving LMI Frames

The following procedure should be performed to receive the LMI frames:

1. Whenever a LMI frame is received the MK50H28 issues a PPRIM of 13. In response to that the host may look at the PPARM field to identify the frame type received
2. Except for the DLCI header field all of the data field will be placed in the receive buffer(s).
3. For LMI frames received, bits 9-11 in RMD0 of the receive descriptor will indicate the type of LMI frame received. A setting of 000 indicates a received SVC frame or Transparent Mode frame.
4. In Non-Auto-LMI mode of operation, LMI frames received on the LMI Channel (typically DLCI 0) will be written into the receive buffer as Transparent or SVC frames.

4.4.6 Link Congestion

1. The host determines congestion on a link. One way it can do is through the congestion statistics and counters in the CT.
2. The host will set TXCONG and/or RXCONG for transmit and receive congestions.
3. If TXCONG is set the MK50H28 will not transmit any frames with DE=1 for that link.
4. If RXCONG is set any frames received with DE = 1 will be discarded. The frame discarded counter in the CT will keep track of the frames with DE = 1 discarded during congestion. If this still does not help congestion, the host can clear the RXRDY bit. Then all the frames received on that link will be discarded. The MK50H28 will set RXMISS bit in the CT and will generate a MISS interrupt if INEA = 1 in the CSR 0.
5. When a channel comes out of congestion, the host should clear TXCONG, RXCONG and RXMISS bits in the CT.

4.4.7 Transmitting the LMI Frames (non-Auto LMI)

The following procedure should be performed to transmit the LMI frames:

1. The MK50H28 (user) sends the STATUS_ENQUIRY frame to the network using UPRIM = 10. A UPRIM of 10 with UPARM of 0 should be issued by the user to request Full STATUS frame from the network. For Sequence Numbers Exchange only a UPRIM of 10 with UPARM of 1 should be issued by the user.
2. The MK50H28 (network) sends the UPDATE_STATUS frame to the user using UPRIM of 12 with UPARM of 0. In order to transmit Optional Information Elements (MULTICAST_STATUS and PVC_STATUS), the host should place this information in the LMI Transmit Buffer(s).
3. The MK50H28 (network) will send the STATUS frame to the user when a UPRIM of 11 is issued. A UPRIM of 12 with UPARM of 0 causes the transmission of a Full STATUS frame. The Optional Information Elements (PVC_STATUS and may be MULTICAST_STATUS) should be placed in the LMI transmit buffer(s). A UPRIM of 12 with UPARM of 1 sends only the Sequence Number information to the user.

   NOTE: The host can use LMI Frame transmission provider primitive 12 to start nT1/T391 or nT2/T392 timers.

4.4.8 Transparent Transmission of Frames from LMI Buffer

The following procedure should be performed to transmit the LMI frames:

1. Follow the steps outlined in Programming Procedure 4.4.3 for sending data from any DLCI.
1. Set the bit XTRAN=1 in the Context Table 0 entry (the LMI CT entry).
2. Issue the Send LMI primitive 14. (See UPRIM14 and XTRAN descriptions for more details).

4.4.9 Transmission of Frames From Higher Priority DLCI(s)

1. Set up the Priority DLCI Block contiguous with the end of the Initialization Block.
2. Input appropriate index (indices) to the desired Context Table entry and set the ACTIVE bit.
3. Set the PTDMD bit in CSR0 (bit 15). See section 4.2.9 for more details.

4.4.10 Disabling the MK50H28

The following procedure should be followed to disable the MK50H28:

1. Issue the STOP primitive through CSR1. This will disable the MK50H28 from receiving or transmitting. The TD pin will be held high while the MK50H28 is in the Stopped mode. The STOP bit in CSR0 will be set and interrupts will be disabled. If reception or transmission of a frame is in progress, then received data may be lost, and the transmitted frame will be aborted.

4.4.11 Re-enabling the MK50H28

The same procedure should be followed for re-enabling the MK50H28 as was used to Initialize upon power up. If the Initialization Block and the hardware configuration have not changed, then steps 1,2,3, 4 and 5 of the Initialization sequence may be omitted.

4.4.12 MK50H28 Internal Self Test

The MK50H28 contains an easy to use internal self test designed to test, with a high fault coverage, all of the major blocks of the device except the DMA controller. It is suggested that a loopback test also be performed to more completely test the DMA controller.

The following procedure should be followed to execute the internal self test:

1. Reset the device using the $\overline{\text{RESET}}$ pin.
2. Set bit 04 of CSR4.
3. Issue a Self Test Request through CSR1.
4. Poll CSR1, waiting for the PAV bit in CSR1 to be set by the MK50H28.
5. After the PAV bit is set, read CSR1. The success or failure of the test is indicated in the PPARM and PPRIM fields as follows:

PPARM	PPRIM	RESULT
0	0	Passed self test.
1	1	Failed the reset test of the self test.
1	2	Failed the self test in the micro controller RAM.
1	3	Failed the self test in the ALU.
1	4	Failed the self test in the timers.
1	5	Failed the self test in the transmitter and/or receiver.
1	6	Failed the self test in the CSR's and/or bus master.
Otherwise		Failed device.

6. If the PAV bit is not set within 75 msec (SYSCLK = 10MHZ), then the MK50H28 is unable to respond to the Self Test Request and will not complete successfully. If the self test passes, then it may be immediately re-executed from step 3, otherwise re-execution should proceed from step 1.

SECTION 5
ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{UB}	Temperature Under Bias	-25 to +100	°C
T_{stg}	Storage Temperature	-65 to +150	°C
V_G	Voltage on any pin with respect to ground	-0.5 to V_{CC}+0.5	V
P_{tot}	Power Dissipation	0.5	W

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure

DC CHARACTERISTICS
T_A=0 °C to 70 °C, V_{CC} = +5 V ±5 percent unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IL}		-0.5		+0.8	V
V_{IH}		+2.0		V_{CC}+0.5	V
V_{OL}	@ IOL = 3.2 mA			+0.5	V
V_{OH}	@ IOH= -0.4 mA	+2.4			V
I_{IL}	@ VIN = 0.4 to V_{CC}			+10	mA
I_{CC}	@ TSCT = 100 ns		50		µA

CAPACITANCE
f = 1MHz

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{IN}	Capacitance on Input pins			10	pF
C_{OUT}	Capacitance on Output Pins			10	pF
C_{IO}	Capacitance on I/O pins			20	pF

AC TIMING SPECIFICATIONS
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

No	Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
1	SYSCLK	T_{SCT}	SYSCLK period		40		10000	ns
2	SYSCLK	T_{SCL}	SYSCLK low time		16			ns
3	SYSCLK	T_{SCH}	SYSCLK high time		16			ns
4	SYSCLK	T_{SCR}	Rise time of SYSCLK		0		8	ns
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0		8	ns
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		20			ns
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		8			ns
8	$\overline{TCLK}$	T_{TCH}	$\overline{TCLK}$ high time		8			ns
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$	CL = 50 pF	0		8	ns
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0		8	ns
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	CL = 50 pF			13	ns
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$		5			ns

AC TIMING SPECIFICATIONS CONTINUED
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

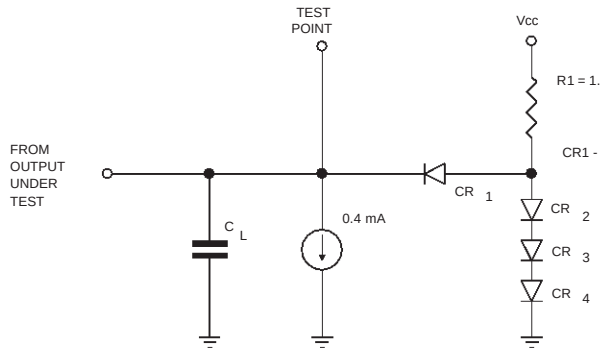
No	Signal	Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
13	$\overline{\text{RCLK}}$	T_{RCT}	$\overline{\text{RCLK}}$ period		20			ns
14	$\overline{\text{RCLK}}$	T_{RCH}	$\overline{\text{RCLK}}$ high time		8			ns
15	$\overline{\text{RCLK}}$	T_{RCL}	$\overline{\text{RCLK}}$ low time		8			ns
16	$\overline{\text{RCLK}}$	T_{RCR}	Rise time of $\overline{\text{RCLK}}$		0		8	ns
17	$\overline{\text{RCLK}}$	T_{RCF}	Fall time of $\overline{\text{RCLK}}$		0		8	ns
18	RD	T_{RDR}	RD data rise time		0		8	ns
19	RD	T_{RDF}	RD data fall time		0		8	ns
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{\text{RCLK}}$		2			ns
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{\text{RCLK}}$		8			ns
22	ALE/$\overline{\text{DAS}}$	T_{DOFF}	Bus Master driver disable	Output Delay	0		20	ns
23	ALE/$\overline{\text{DAS}}$	T_{DON}	Bus Master driver enable after rising edge T1 SYSCLK	Output Delay	0		20	ns
24	$\overline{\text{HLDA}}$	T_{HHA}	Delay to falling edge of $\overline{\text{HLDA}}$ from falling edge of HOLD (Bus Master)		0			ns
25	$\overline{\text{HLDA}}$	T_{HLAH}	$\overline{\text{HLDA}}$ input setup time		10			ns
26	$\overline{\text{HLDA}}$	T_{HLAS}	Delay to rising edge $\overline{\text{HLDA}}$ from rising edge HOLD		10			ns
27	A	T_{XAS}	Address setup time	Output Delay			30	ns
28	A	T_{XAH}	Address hold time	Output Delay			20	ns
29	DAL	T_{AS}	Address setup time	Output Delay			35	ns
30	DAL	T_{AH}	Address hold time	Output Delay	0		20	ns
31	DAL	T_{RDAS}	Data setup time (Bus Master read)		15			ns
32	DAL	T_{RDAH}	Data hold time (Bus Master read)		10			ns
33	DAL	T_{WAH}	Address hold time (Bus Master write)	Output Delay			15	ns
34	DAL	T_{WDS}	Data setup time (Bus Master write)	Output Delay			25	ns
35	DAL	T_{WDH}	Data hold time (Bus Master write)	Output Delay			25	ns
36	DAL	T_{SRDS}	Data setup time (Bus Slave read)				25	ns
37	DAL	T_{SRDH}	Data hold time (Bus slave read)				25	ns
38	DAL	T_{SWDH}	Data hold time (Bus slave write)		10			ns
39	DAL	T_{SWDS}	Data setup time (Bus slave write)		10			ns
40	ALE	T_{ALES}	ALE setup time	Output Delay			30	ns
41	ALE	T_{ALHB}	ALE hold time (asserted to de-asserted) (DMA Burst)	Output Delay			15	ns
42	ALE	T_{ALHS}	ALE hold time (asserted to 3-State) (Single DMA cycle)	Output Delay			20	ns
43	$\overline{\text{DAS}}$	T_{DASS}	DAS setup time from falling edge of T2 SYSCLK (Bus Master)	Output Delay			25	ns
44	$\overline{\text{DAS}}$	T_{DASH}	DAS hold time from rising edge of SYSCLK (Bus Master)	Output Delay	5		15	ns
45	DALI/$\overline{\text{DALO}}$ BM)/BM1	T_{BMDE}	Bus Master driver enable (from 3-State to driven) (Bus Master)	Output Delay			25	ns
46	$\overline{\text{DALI}}$	T_{RIS}	$\overline{\text{DALI}}$ setup time (Bus Master read)	Output Delay			15	ns
47	$\overline{\text{DALI}}$	T_{RIH}	$\overline{\text{DALI}}$ hold time (Bus Master read)	Output Delay			25	ns
48	$\overline{\text{DALI}}$	T_{BMDD}	Bus Master driver disable (from driven to 3-State) (Bus Master)	Output Delay			20	ns

AC TIMING SPECIFICATIONS CONTINUED

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

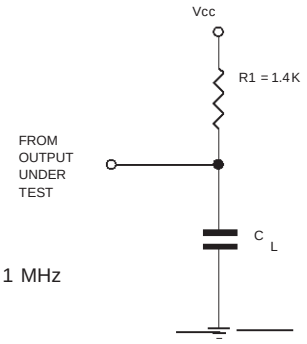
No	Signal	Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
49	$\overline{\text{DALO}}$	T_{ROS}	$\overline{\text{DALO}}$ setup time (Bus Master read)	Output Delay			30	ns
50	$\overline{\text{DALO}}$	T_{ROH}	$\overline{\text{DALO}}$ hold time (Bus Master read)	Output Delay			30	ns
52	$\overline{\text{CS}}$	T_{CSH}	$\overline{\text{CS}}$ hold time		10			ns
53	$\overline{\text{CS}}$	T_{CSS}	$\overline{\text{CS}}$ setup time		10			ns
54	ADR	T_{SAH}	ADR hold time		10			ns
55	ADR	T_{SAS}	ADR setup time		10			ns
56	$\overline{\text{DAS}}$	T_{SDAS}	$\overline{\text{DAS}}$ input setup time (Bus slave)		10			ns
57	$\overline{\text{DAS}}$	T_{SDSH}	$\overline{\text{DAS}}$ input hold time (Bus slave)		10			ns
58	$\overline{\text{READY}}$	T_{RDYS}	$\overline{\text{READY}}$ setup time (Bus slave)	Output Delay			15	ns
59	$\overline{\text{READY}}$	T_{SRYH}	$\overline{\text{READY}}$ hold time after rising edge of $\overline{\text{DAS}}$ (Bus slave read)				15	ns
60	$\overline{\text{READY}}$	T_{RSH}	$\overline{\text{READY}}$ setup time (Bus Master)		10			ns
61	$\overline{\text{READY}}$	T_{SRS}	$\overline{\text{READY}}$ hold time (Bus Master)		10			ns
62	READ	T_{REDS}	READ setup time (Bus slave)		10			ns
63	READ	T_{REDH}	READ hold time (Bus slave)		10			ns
64	$\overline{\text{HOLD}}$	T_{HLDS}	$\overline{\text{HOLD}}$ setup time (Bus Master)	Output Delay			15	ns
65	$\overline{\text{HOLD}}$	T_{HLDH}	$\overline{\text{HOLD}}$ hold time (Bus Master)	Output Delay			35	ns

Figure 9a: TTL Output Load Diagram



NOTE: This load is used on all outputs except INTR, HOLD, READY.

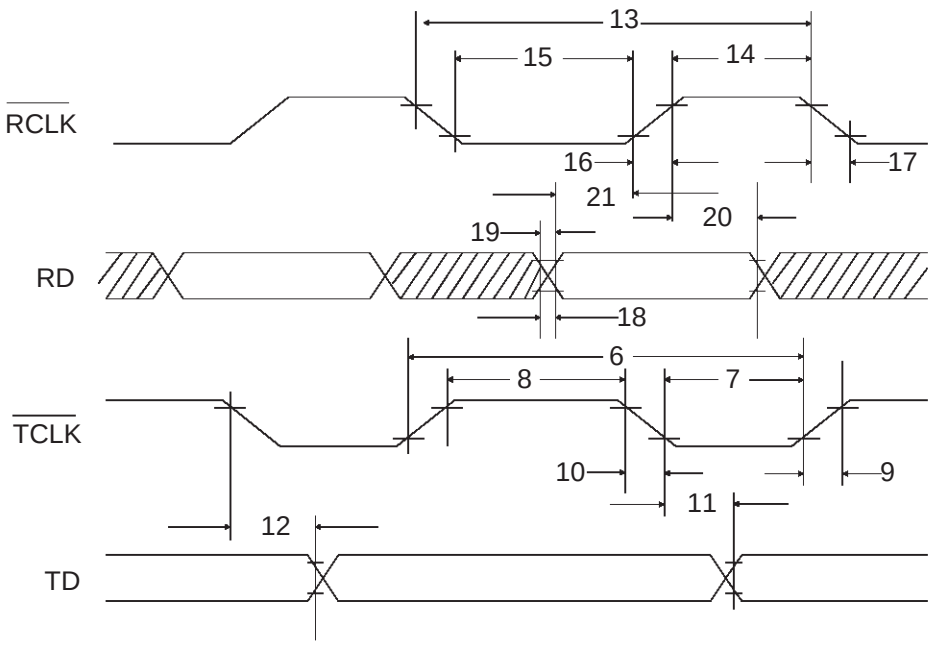
Figure 9b: Open Drain Output Load Diagram



C_L = 50pF min @ 1 MHz

NOTE: This load is used on open drain outputs INTR, HOLD, READY.

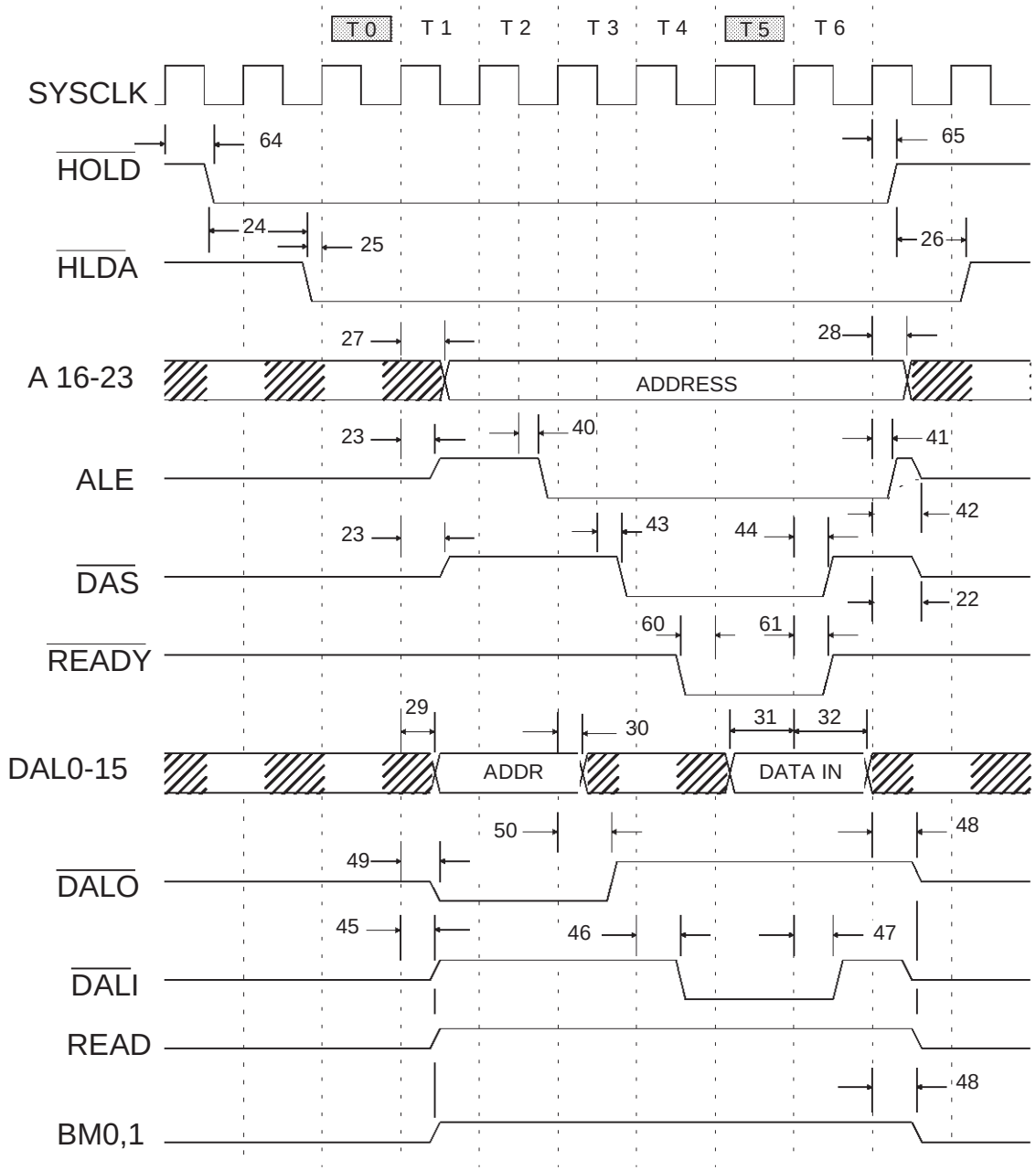
Figure 10: MK50H28 Serial Link Timing Diagram



TIMING MEASUREMENTS ARE MADE AT THE FOLLOWING VOLTAGES, UNLESS OTHERWISE SPECIFIED:

	"1"	"0"
OUTPUT	2.0 V	O.8 V
INPUT	2.0 V	O.8 V
FLOAT	10 %	90 %

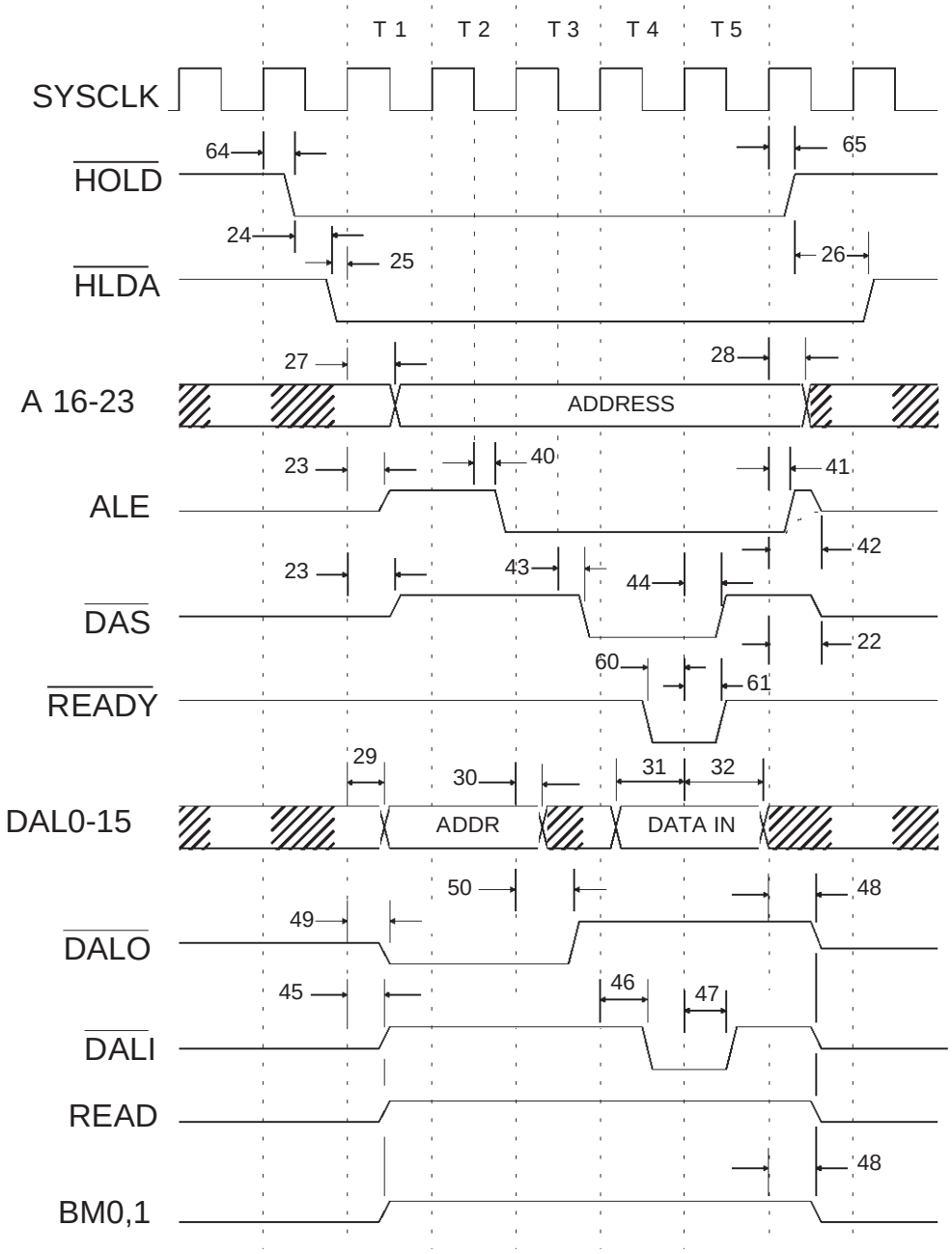
Figure 11: MK50H28 BUS Master Timing (Read) (for CYCLE = 0, CSR2<15>)



NOTES:

1. The shaded SYSCLK periods T0 and T5 will be removed when setting CSR2 bit 15, CYCLE =1 to select the shorter DMA cycle as shown in Figure 7a.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

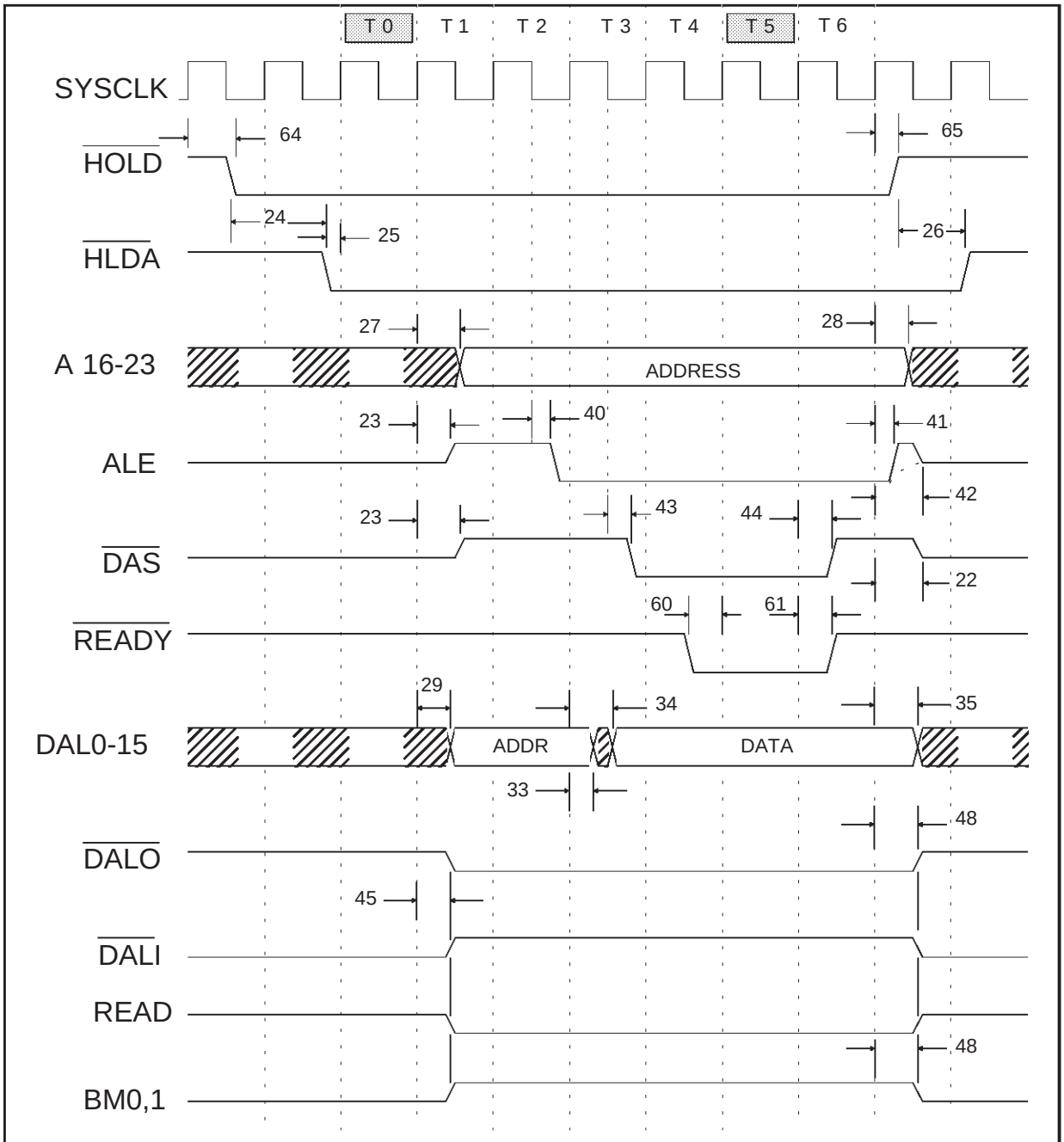
Figure 11a: MK50H28 Reduced Cycle BUS Master Timing (Read) (for CYCLE = 1, CSR2<15>)



NOTES:

1. This reduced DMA Cycle Time is selected by setting CSR2 bit 15, CYCLE =1.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

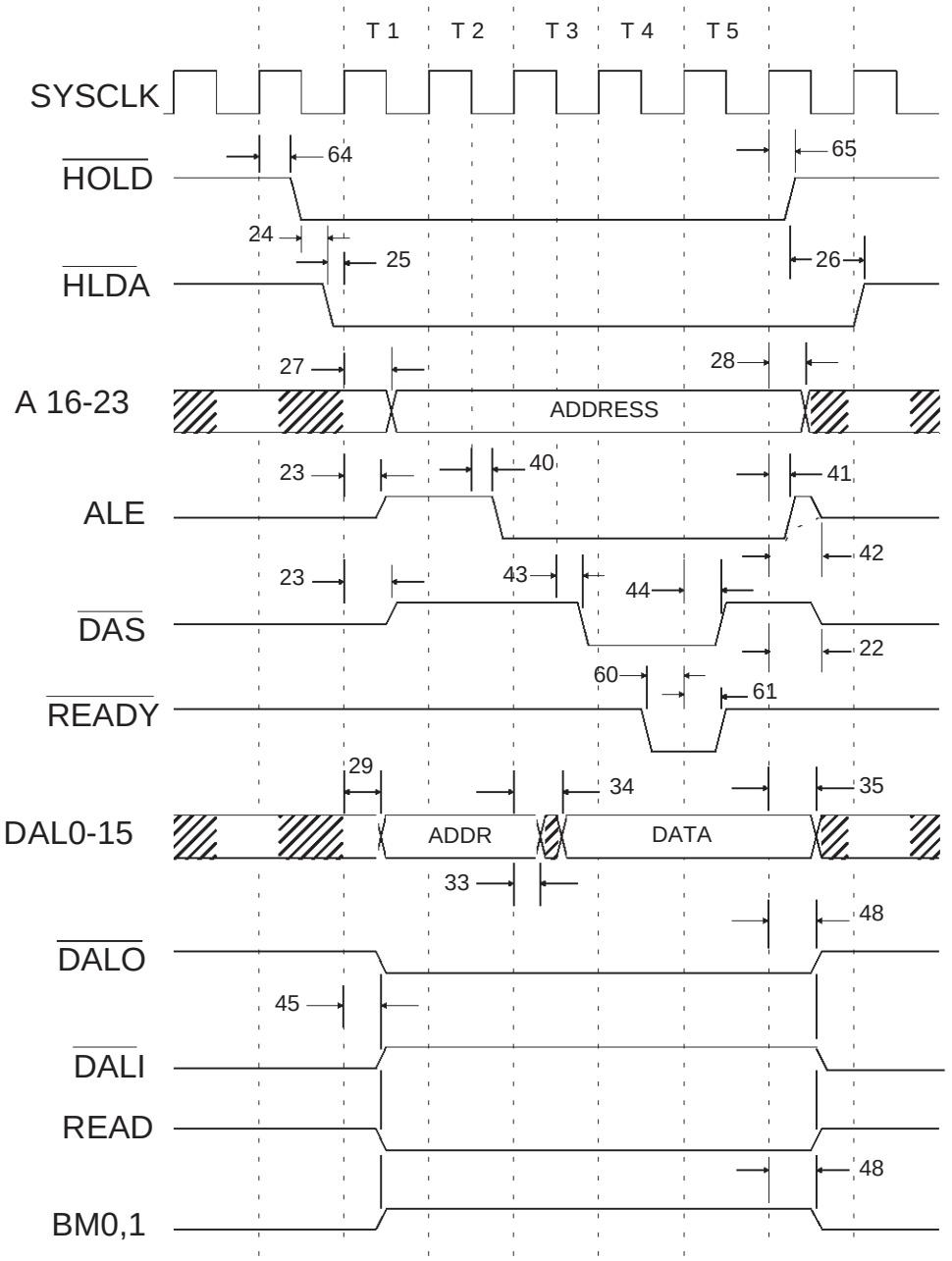
Figure 12: MK50H28 BUS Master Timing Diagram (Write) (for CYCLE = 0, CSR2<15>)



NOTES:

1. The shaded SYSCLK periods T0 and T5 will be removed when setting CSR2 bit 15, CYCLE =1 to select the shorter DMA cycle as shown in Figure 8a.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

Figure 12a: MK50H28 Reduced Cycle BUS Master Timing (Write) (for CYCLE = 1, CSR2<15>)



NOTES:

1. This Reduced DMA Cycle Time is selected by setting CSR2 bit 15, CYCLE = 1. Times T0 and T5 from the standard DMA Cycle are removed for this reduced timing.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

Figure 12b: BUS Master BURST Timing (Reduced Cycle - Write)

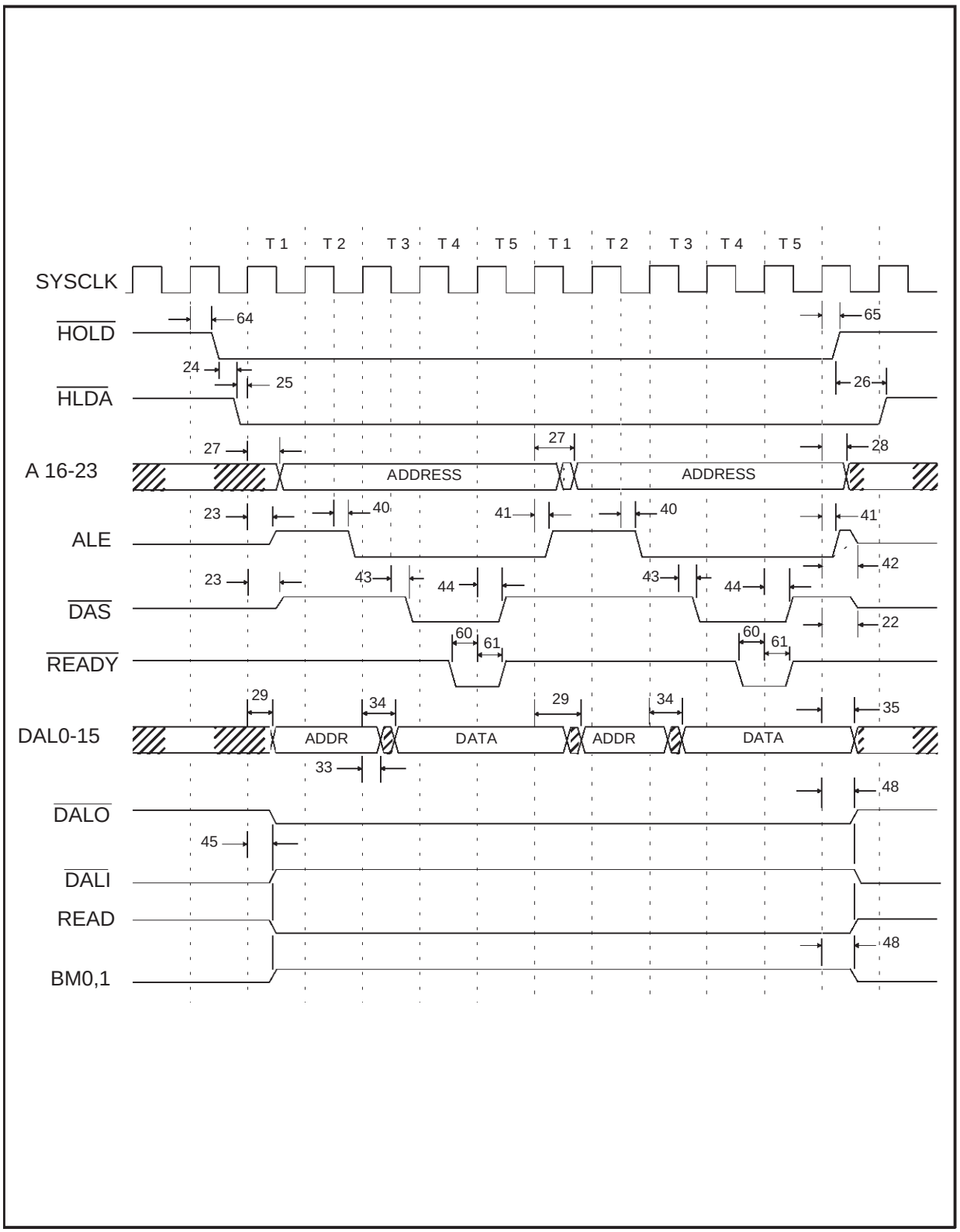
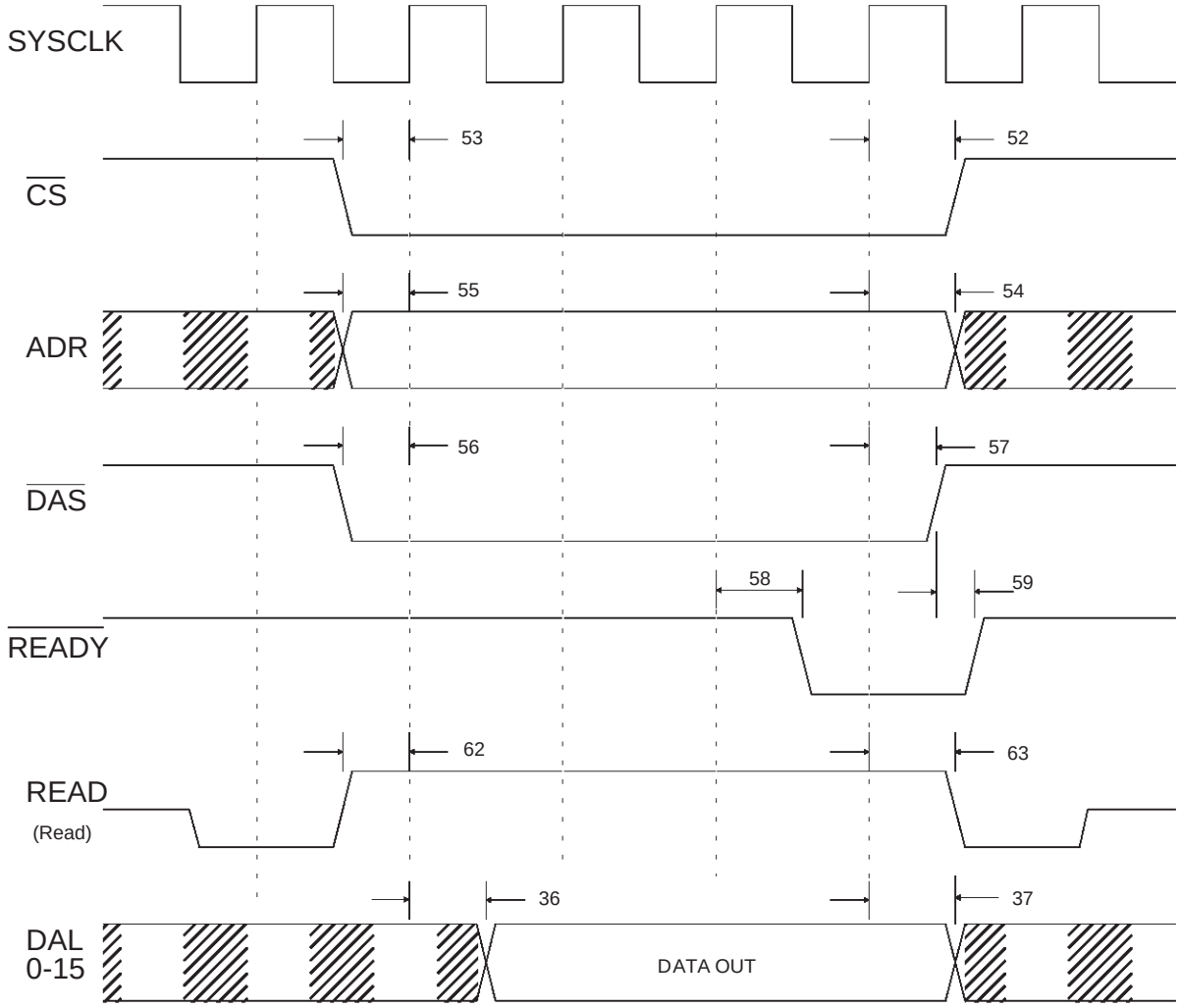


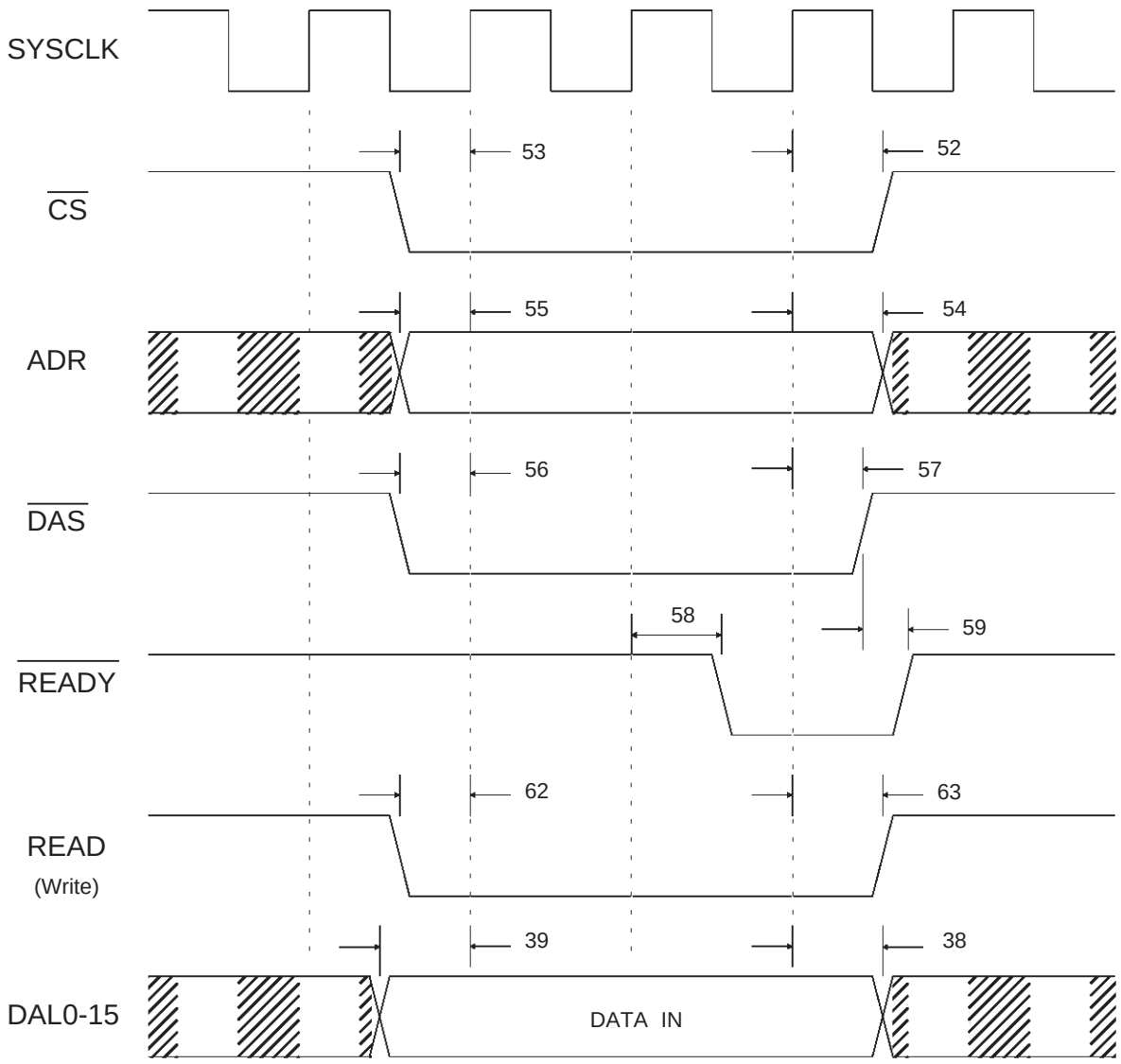
Figure 13: MK50H28 BUS Slave Timing Diagram (Read)



NOTES:

1. Input setup and hold times are in minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are from the specified edge to a valid output.

Figure 14: MK50H28 BUS Slave Timing Diagram (Write)



NOTES:

1. Input setup and hold times are the minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are from the specified edge to a valid output.

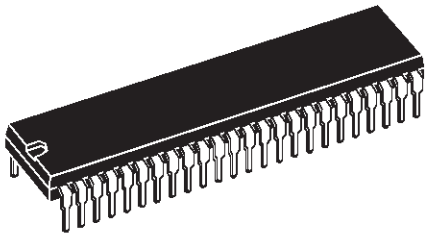
ORDERING INFORMATION:

MK50H28 N 25 / XX

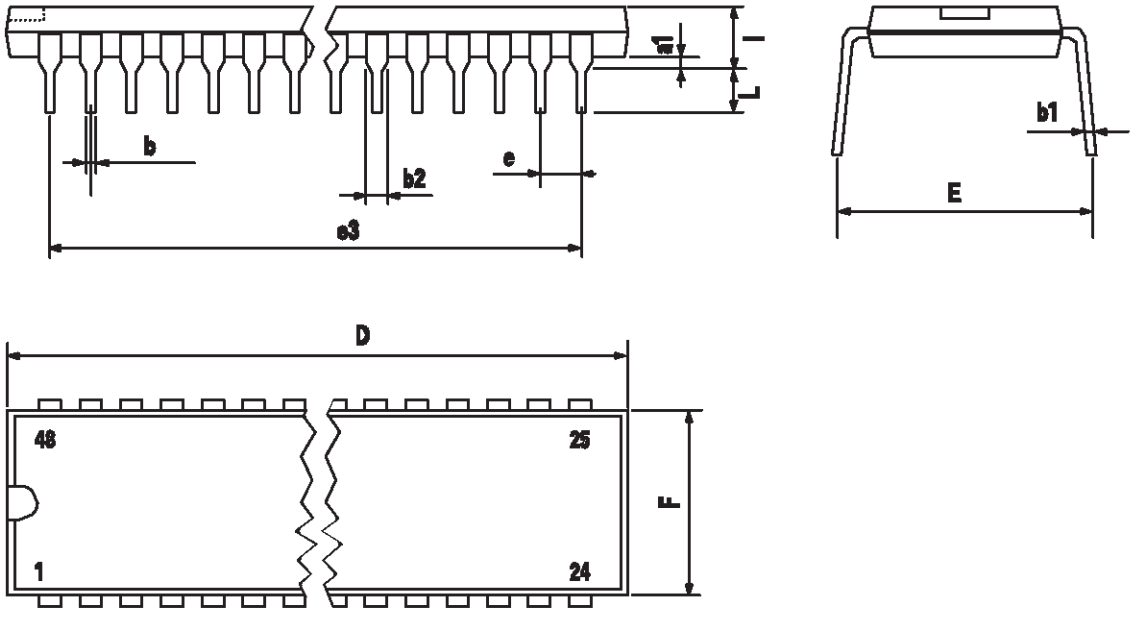
- XX — REVISION CODE (Contact factory representative for current revision)
- 25 — SPEED SORT (25 = 25MHz SYSCLK)
- N — PACKAGE
  - N = Plastic DIP (48 Pins)
  - Q = Plastic J-Leaded Chip Carrier (52 Pins)
- MK50H28 — PART # PROTOCOL
  - 50H28 = Frame Relay

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			62.74			2.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		58.42			2.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

OUTLINE AND MECHANICAL DATA

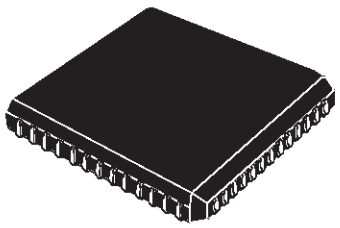


DIP48



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		4.20	5.08		0.165	0.20
A1		0.51			0.020	
A3		2.29	3.30		0.090	0.13
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C	0.25			0.01		
D		19.94	20.19		0.785	0.795
D1		19.05	19.20		0.750	0.756
D2		17.53	18.54		0.690	0.730
D3	15.24			0.60		
E		19.94	20.19		0.785	0.795
E1		19.05	19.20		0.750	0.756
E2		17.53	18.54		0.690	0.730
E3	15.24			0.60		
e	1.27			0.05		
L		0.64			0.025	
L1		1.53			0.060	
M		1.07	1.22		0.042	0.048
M1		1.07	1.42		0.042	0.056

OUTLINE AND MECHANICAL DATA



PLCC52