# 7V to 100V Input, Ultra-Low $I_Q$, 3 A Integrated High-Side MOSFET, Buck DC/DC Converter with 3.3V/50mA LDO

## 1 DESCRIPTION

The MK9118 operates over a wide input voltage range from 7 V to 100V. With integrated the main MOSFET, the MK9118 delivers up to 3A output current.

The MK9118 adopts a constant on-time (COT) control architecture to achieve excellent transient response.

MK9118 integrated a 3.3V fixed output LDO, which could deliver up to 50mA output current.

With patented standby circuits, the device can achieve ultra-low $I_Q$, and exit the standby mode fast.

## 2 APPLICATIONS

- GPS tracker
- Automotive and Industry Systems
- Motor Drives, Telecom
- BMS

## 3 FEATURES

- Wide Input Voltage 7V-100V
- Wide Output Voltage 1.22V-26V
- Integrated 120mΩ High-Side MOSFET
- <100μA quiescent current
- Adjustable $F_{SW}$ up to 1MHz
- Internal 3ms Soft-start
- Smart power saving and ultra-Fast Transient Response
- Precision ±1% Feedback Reference
- Integrated 3.3 V/50 mA LDO
- OC, OT Protection with Hiccup Mode
- No Loop Compensation Components
- ESOP8 Package with Thermal PAD



## 4 TYPICAL APPLICATIONS

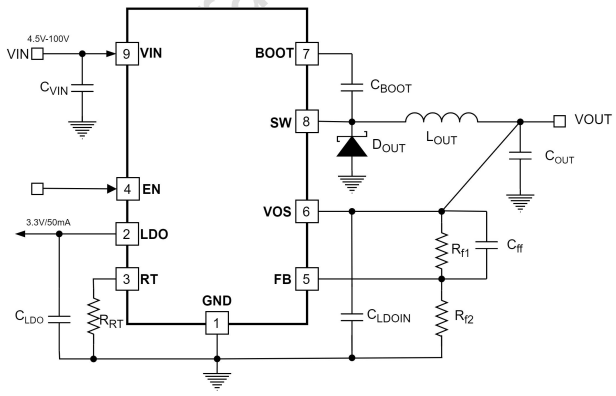



Figure 1. Typical Application Diagram

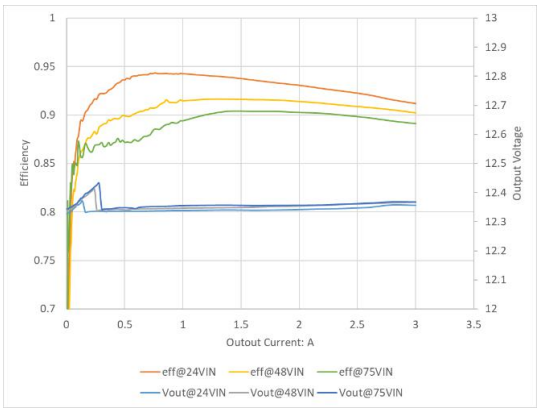
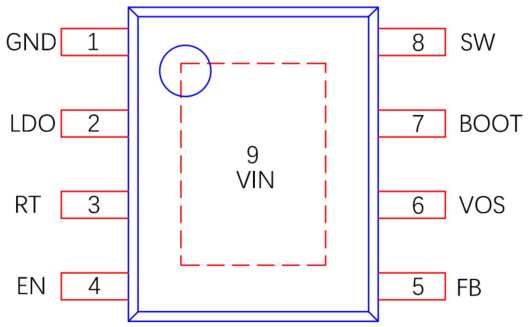



Figure 2. Efficiency and Load Regulation at 12Vout

# 5 PACKAGE REFERENCE AND PIN FUNCTION




**ESOP8 (top view)**

| Order No. | Description |
|---|---|
| MK9118AAD | ESOP-8, tape, 4k/reel |

| Pin # | MK9118 | Name | Description |
|---|---|---|---|
| 1 | GND | Analog Input | Ground |
| 2 | LDO | Analog Power Output | 3.3V LDO output, connect a capacitor to GND higher than 1uF; leave as float to disable internal LDO. |
| 3 | RT | Analog Input | Connect a resistor to GND, set the switching frequency. |
| 4 | EN | Analog input | Buck and LDO enable, internal pull down by 0.08uA. Source 2uA after device enabled.<br>Tie to VIN is if hysteresis function is not used. |
| 5 | FB | Analog Input | Feedback input, connect to output voltage resistor divider. |
| 6 | VOS | Analog Power Input | Output sense and internal LDO input, connect to output cap with 100mA current capability PCB trace; Place 0.1uF cap close to VOS pin. |
| 7 | BOOT | Analog Power Input | Boot-strap pin. Decouple this pin to SW pin with a >100nF (0.2V drop) ceramic capacitor. |
| 8 | SW | Analog Power Output | Inductor pin. Connect to the switch node of the power inductor and a shotty diode between SW and GND. |
| 9 | VIN | Analog Power Input | Input pin. Decouple this pin to GND with low ESR capacitor. Connect to a VIN power plane to improve thermal performance. |

## 6 ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN, SW to GND ····· -0.3V to 100V
SW to GND (20ns pulse) ····· -3V to 100V
BOOT to GND ····· SW+6.6V
RT to GND ····· -0.3V to 6.6V
FB to GND ····· -0.3V to 6.6V
VOS to GND ····· -0.3V to 26V
Power Dissipation, $P_D$ @$T_A$=25℃, ESOP8 ····· 3.3W
Package Thermal Resistance
$\theta_{JA}$ (Junction to ambient) ····· 30℃/W
$\theta_{JC}$ (Junction to case) ····· 10℃/W
Operating Junction Temperature, $T_J$ ····· -40℃ to 160℃
Storage Temperature，$T_{stg}$ ····· -65℃ to 160℃
Soldering Temperature(10 second)，$T_{sld}$ ····· 260℃

Notes:

(1)·· Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 7 RECOMMENDED OPERATING CONDITIONS

VIN Voltage ····· 7V to 100V
EN Voltage ····· -0.3V to 100V
SW Voltage ····· -0.3V to 100V
Ambient Temperature ····· -40℃ to 125℃

## 8 ESD RATINGS

| | | Value | Units |
|---|---|---|---|
| Electrostatic discharge $V_{ESD}$ | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, SW, BOOT, EN, RT, FB, PGOOD (1). | ±2000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, SW, BOOT, EN, RT, FB, PGOOD (2). | ±500 | V |

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

# 9 ELECTRICAL CHARACTERISTICS

$V_{IN}$=48V, $V_{OUT}$=12V, L=22μH, $C_{OUT}$=22uF, $T_A$=25℃, unless otherwise specified

| Parameter | | Test Conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Input Voltage** | | | | | | |
| $V_{IN}$ | Input Voltage | | 7 | | 100 | V |
| $V_{INUVLO}$ | Input UVLO Off | | | 6.3 | 7 | V |
| $V_{INUVLO-HYS}$ | Input UVLO hysteresis | | | 0.7 | | V |
| **Supply Current** | | | | | | |
| $I_{SHUTDOWN}$ | Shutdown Current | $V_{EN}$=0V | | 7.5 | | μA |
| $I_{Q1}$ | None switching quiet current | EN=$V_{IN}$, VOS higher than target, ILDO=0A | | 18 | | μA |
| $I_{STANDBY}$ | Standby Current | $I_{OUT}$=0A, ILDO=0A | | | 100 | μA |
| **Feedback** | | | | | | |
| $V_{REF}$ | Feedback reference voltage | | | 1.22 | | V |
| **EN/UVLO** | | | | | | |
| $V_{ENH}$ | EN rising threshold | $V_{IN}$=48V, $I_{OUT}$=0.1A | | 1.24 | | V |
| $I_{EN\ Hysteresis}$ | Hysteresis Input Current | $V_{IN}$=48V, $I_{OUT}$=0.1A | | -2 | | μA |
| **Frequency** | | | | | | |
| $F_{SW}$ | Programmable Switching Frequency Range | $Fsw(kHz)=\frac{22\times10^3}{RT(k\Omega)}$ | 100 | | 1000 | kHz |
| **LDO** | | | | | | |
| VLDO | LDO output voltage | Vos=12V, 0mA - 50mA | 3.26 | 3.3 | 3.33 | V |
| $I_{LDOOC}$ | LDO over current | VLDO=0V | | 75 | 125 | mA |
| **Timing** | | | | | | |
| $t_{ON-MIN}$ | Minimum on-time | | | 150 | | ns |
| $t_{OFF-MIN}$ | Minimum off-time | | | 190 | | ns |
| **Power Switches** | | | | | | |
| $R_{DSON-HS}$ | High-side MOSFET RDSON | | | 0.12 | | Ω |
| **Current Limit** | | | | | | |
| $I_{PEAK-HS}$ | High-side MOSFET Peak Current limit | | | 4.8 | | A |
| **Soft Start** | | | | | | |
| $t_{SS}$ | Soft-start time | | | 3 | | ms |
| $t_{hiccup}$ | UVP hiccup time | | | 56 | | ms |
| **Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Threshold | $T_J$ rising | | 160 | | ℃ |
| $T_{HYS}$ | Thermal Shutdown Hysteresis | | | 20 | | ℃ |

# 10 BLOCK DIAGRAM

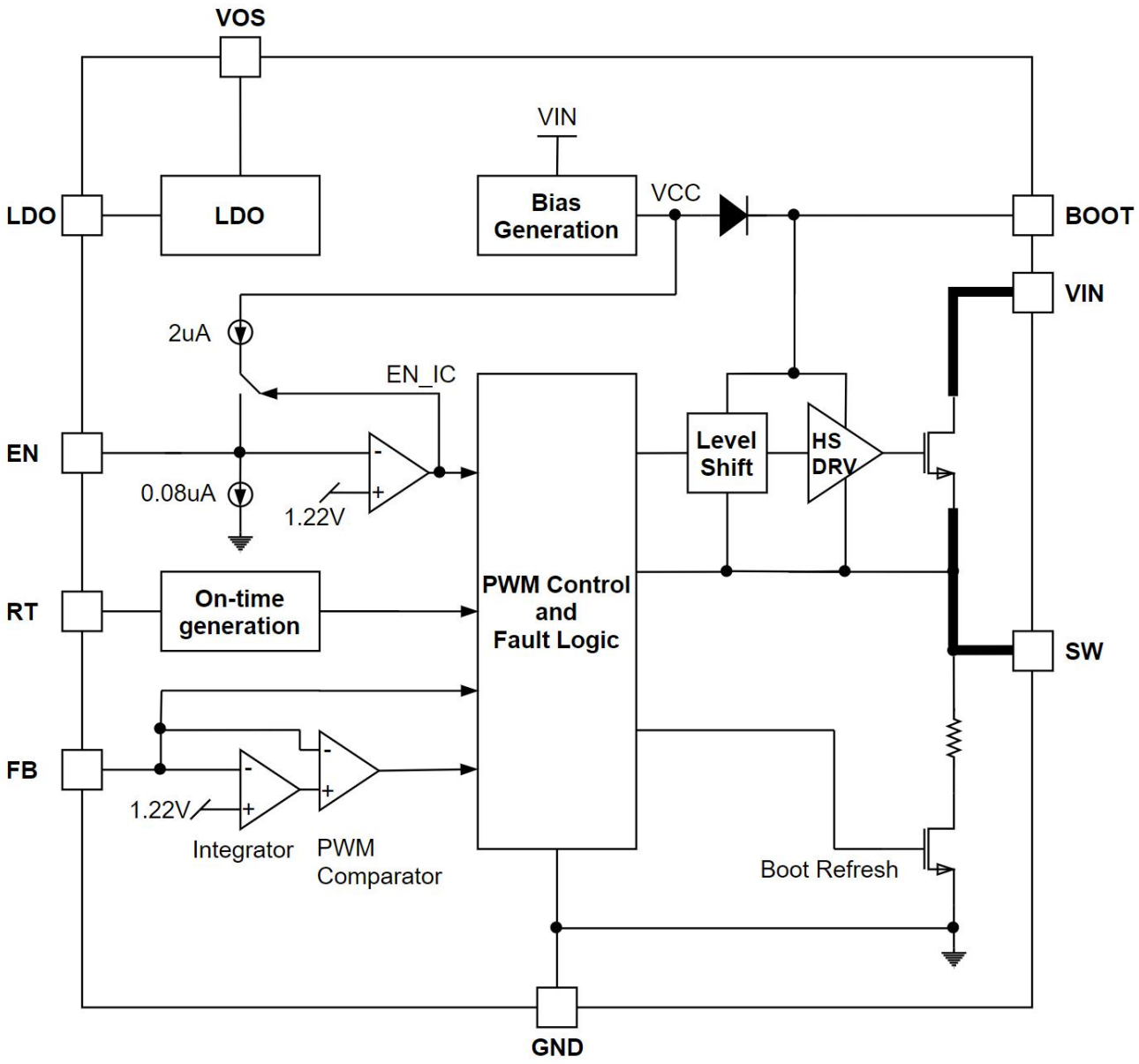



**Figure 3. Block Diagram**

# 11 TYPICAL CHARACTERISTICS

# 12 AIPPLICATIONS

## 12.1 Operation Overview

The MK9118 operates over a wide input voltage range from 7V to 100V. With integrated the main MOSFET, the MK9118 delivers up to 3A output current.

The MK9118 adopts a constant on-time (COT) control architecture to achieve excellent transient response.

MK9118 integrated a fixed output LDO, which could deliver up to 50mA output current.

With patented standby circuits, the device can achieve ultra-low $I_Q$, and exit the standby mode fast.

## 12.2 Switching Frequency ($R_T$)

The switch frequency of MK9118 is set by the on-time resistor RT. As shown below, in $5V_{OUT}$ application a 100kΩ resistor sets the switching frequency at 220kHz.

$$Fsw(kHz)=\frac{22\times10^3}{RT(k\Omega)}$$

Note that the final switching frequency is not only affected by component tolerant but also $t_{ON-MIN}$ and $t_{OFF-MIN}$.

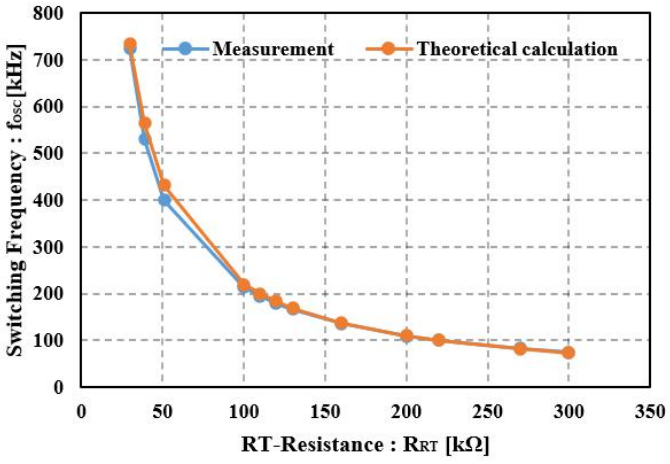



**Figure 4. Switching Frequency v.s. RT-Resistance**

## 12.3 Output Voltage Program

Choose $R_{f1}$ and $R_{f2}$ to program the output voltage. For target $V_{OUT}$ setpoint, calculate Rf1 and Rf2 using below equation:

$$V_{OUT} = 1.22\text{V} \times (1 + \frac{R_{f1}}{R_{f2}})$$

$R_{f1}$ in the range of 100kΩ to 500kΩ is recommended for most applications. Larger feedback resistors consumes less DC current, which is important if light-load efficiency is critical. But too large resistors is not recommended as the feedback path would become more susceptible.

The feedforward capacitor $C_{ff}$ and feedforward resistor $R_{ff}$ are strongly recommended, which can improve the system stability and transient responses.

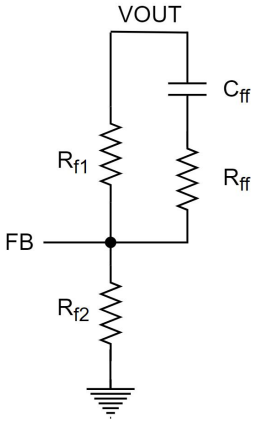



**Figure 5. Feedback Resistance**

## 12.4 Input Capacitor ($C_{IN}$)

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck converter at every switching cycle. The input ripple voltage $\Delta V_{IN}$ at input capacitor is calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To minimize the potential noise problem, a X5R or better grade capacitor with sufficient voltage rating is recommended. This capacitor should be close to the VIN and GND pins to minimize the loop area formed by $C_{IN}$ and VIN/GND pins. In this application, a 1μF low ESR ceramic capacitor is recommended.

## 12.5 Output Inductor (L)

It is recommended to choose the ripple current of inductor between 30% to 50% of the rated load current $I_{OUT}$(max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

And the peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OUT}(max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor must greater than the $I_L$(peak). An inductor whose saturation current is above the current limit setting of the MK9118 will be best choice. Note that inductor saturation current levels generally decrease as the inductor temperature increase.

## 12.5 Output Capacitor ($C_{OUT}$)

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

Above equation only take the steady state ripple into consideration. The transient requirements also must be taken into consideration when selecting the output capacitor. The X5R or better grade ceramic capacitor larger than 22μF is recommended. For high peak current applications, an E-cap larger than 100uF is recommended too.

## 12.6 Enable Operation

Input UVLO can be programmed by EN rising threshold. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN1}}{R_{EN2}}) \times V_{ENH}$$

$V_{ENH}$ is EN rising threshold voltage, typical is 1.24V.

The UVLO hysteresis is accomplished with an internal 2μA current source that is switched on or off into the impedance of the set-point divider. When the voltage at the EN pin exceeds the rising threshold, the current source is activated to quickly raise the voltage at the EN pin. The hysteresis can be calculated as:

$$V_{hys}(\mathrm{V}) = R_{EN1} \times 2\mu\mathrm{A}$$

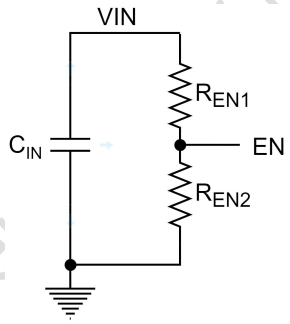



Figure 6. Enable Resistance Divider

Tie EN pin to VIN if hysteresis function is not used to improve quiescent current.

## 12.7 Boot-strap capacitor

This capacitor provides the energy for high-side gate driver. A high quality 10nF ceramic capacitor connected between the BS pin and the SW pin is recommended. Also a RC series net can be used to slow down the turn-on speed of high side MOSFET.

## 12.8 CATCH DIODE

MK9118 should be taken to connect external catch diode between the SW pin and the GND pin. The diode require adherence to absolute maximum ratings of application. Opposite direction voltage should be higher than maximum voltage of the VIN pin. Also for saturation current of diode, select the one with larger current than the total of maximum output current and 1/2 of inductor ripple current ΔIL. Choose catch diode with lower voltage drop to enhance efficiency and thermal performance.

## 12.9 LDO

MK9118 integrated a 3.3V/50mA LDO, which is suitable for MCU's bias input. The LDO converter VOS to 3.3V with 50mA capability, put a ceramic cap >1μF as close as possible to LDO pin in application.

## Application Examples

1.

| Parameter | Symbol | Specification Value |
|---|---|---|
| Input Voltage | $V_{IN}$ | 24 V ～ 75 V |
| Output Voltage | $V_{OUT}$ | 5.0 V |
| Switching Frequency | fosc | 200 kHz (Typ) |
| Maximum Output Current | $I_{OUTMAX}$ | 3 A |

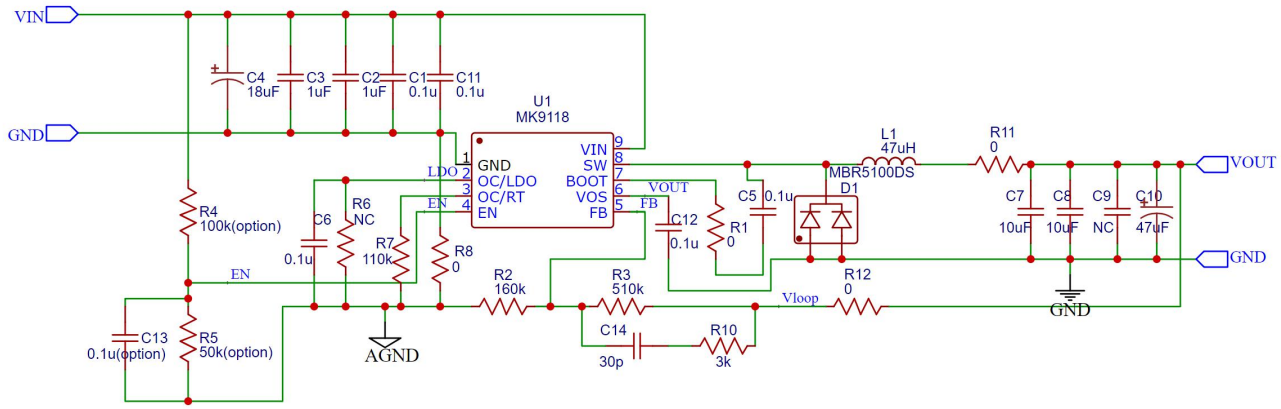



Figure 7. Vout=5V Schematic

2.

| Parameter | Symbol | Specification Value |
|---|---|---|
| Input Voltage | $V_{IN}$ | 24 V ～ 75 V |
| Output Voltage | $V_{OUT}$ | 12.3 V |
| Switching Frequency | fosc | 200 kHz (Typ) |
| Maximum Output Current | $I_{OUTMAX}$ | 3 A |

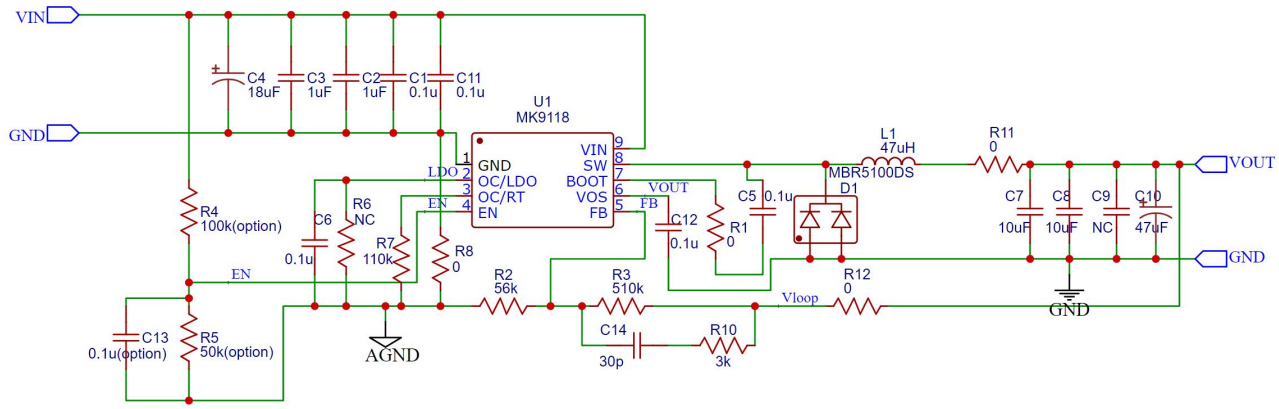



Figure 8. Vout=12.3V Schematic

# 13 LAYOUT

## 13.1 Layout Guide

To achieve high performance of the MK9118, the following layout tips must be followed.

(1)·· At least one low-ESR ceramic bypass capacitor $C_{IN}$ must be used. Place the $C_{IN}$ as close as possible to the MK9118 VIN and GND pins, place decoupling caps as close as possible between VIN and catch diode's GND.

(2)·· Minimize the loop area formed by $C_{IN}$ connections to VIN and GND pins.

(3)·· Inductor must be placed close to the SW pin. Minimize the area of SW trace to avoid the potential noise problem.

(4)·· Maximize the PCB area connecting to the VIN pin/thermal pad. If it is allowed, a ground plane can be used as noise shielding and heat dissipation path.

(5)·· Place the feedback resistors, $R_{f1}$ and $R_{f2}$, close to the FB pin. Route the feedback $V_{OUT}$ sense path away from noisy nodes such as the SW net.

(6)·· Connect VOS pin to output cap directly, place a 0.1uF cap between VOS and GND.

(7)·· The RT pin is sensitive to noise. The on-time set resistor $R_T$ must be close to the device.

## 13.2 Layout Example

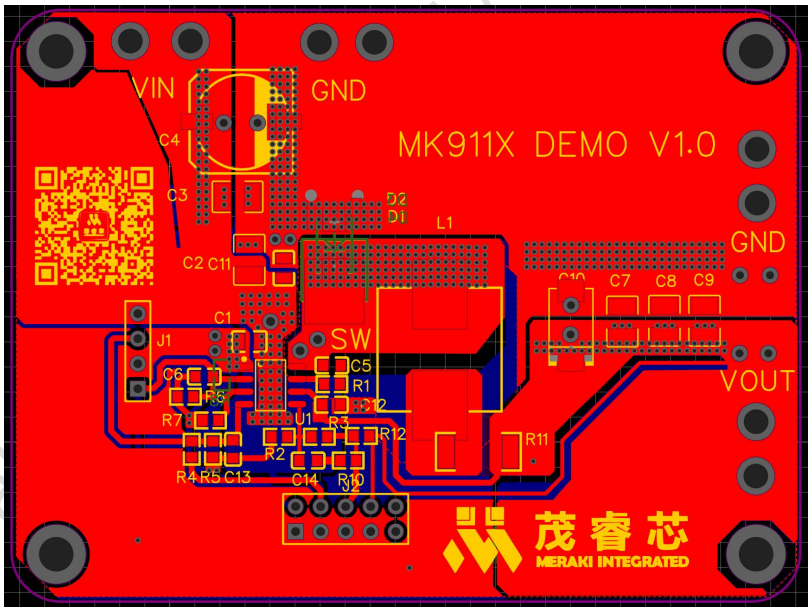



Figure 9. Evkit Layout (Tope Layer)

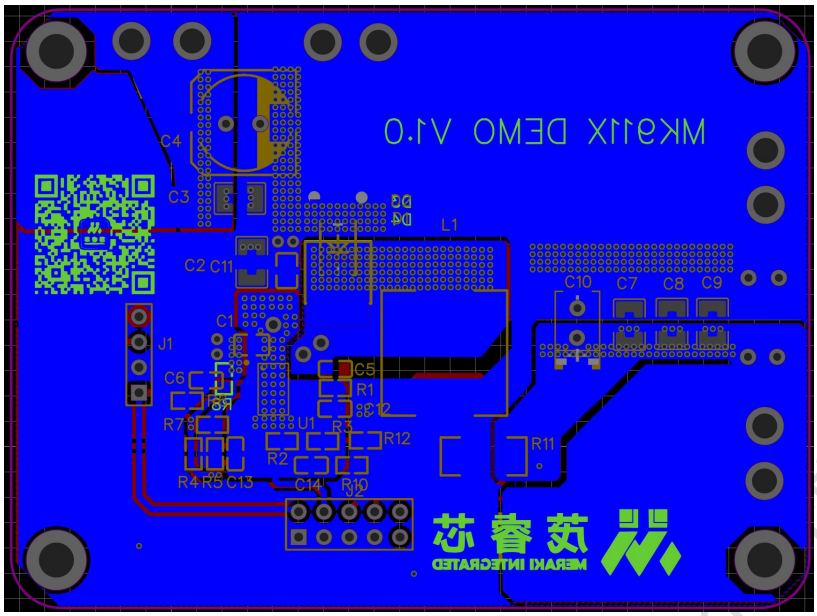



Figure 10. Evkit Layout (Bottom Layer)

# 14 PACKAGE SIZE

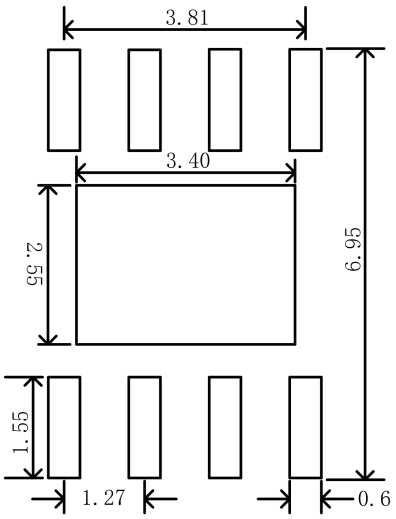



Figure17. Recommended Land Pattern (mm)

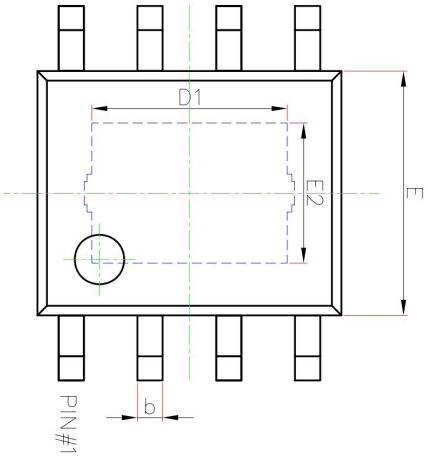



Figure 18. MK9118 Top View

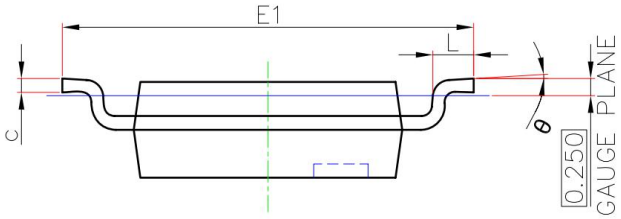



Figure19. MK9118 Side View

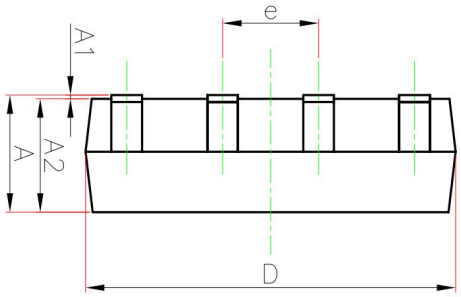
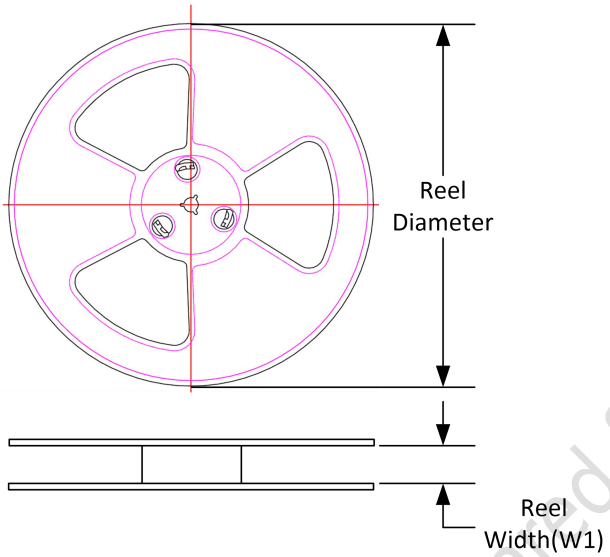



Figure20. MK9118 Side View

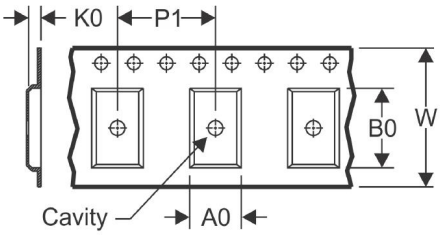
| SYMBOL | Millimeter | |
|---|---|---|
| | MIN | NOM |
| A | 1.300 | 1.700 |
| A1 | 0.000 | 0.100 |
| A2 | 1.350 | 1.550 |
| b | 0.330 | 0.510 |
| c | 0.170 | 0.250 |
| D | 4.700 | 5.100 |
| D1 | 3.050 | 3.250 |
| E | 3.800 | 4.000 |
| E1 | 5.800 | 6.200 |
| E2 | 2.160 | 2.360 |
| e | 1.270(BSC) | |
| L | 0.400 | 1.270 |
| θ | 0° | 8° |

# 15 REEL AND TAPE INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

| Device | Package Type | Pins | Quantities | Reel Diameter (mm) | Reel Width W1(mm) |
|---|---|---|---|---|---|
| MK9118 | ESOP8 | 8 | 4000 | 332 | 12.5 |
| A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | |
| 4.0 | 3.3 | 1.1 | 8.0 | 12.0 | |

# 16 TAPE AND REEL BOX DIMENSIONS