Ultra-Fast Turn-off Synchronous Rectifier Controller

Desciption

The MK91808 is a compact secondary side synchronous rectifier controller and driver for high performance flyback converters. It is compatible with DCM, CCM and QR operations.

The MK91808 generates its own supply while used in high-side rectification, which eliminates the need of external supply generated by auxiliary winding of the transformer.

The extremely low 10ns turn−off propagation delay time and high sink current (~4A) capability of the driver improve SR V_{DS} stress at CCM mode.

The unique VG clamping circuit works well to prevent VG from turning on by fast rising at VD pin with no VCC, that avoids the shoot through between primary side and secondary side during system startup even if the SR VCC is still below 2V.

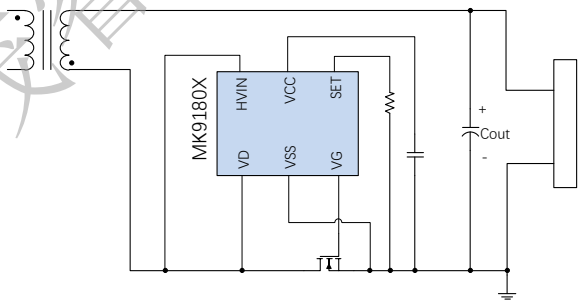
Typical Applications

- AC/DC Adapters for Mobile Phone and Notebook
- High Power density AC/DC Power Supplies
- Battery Powered System

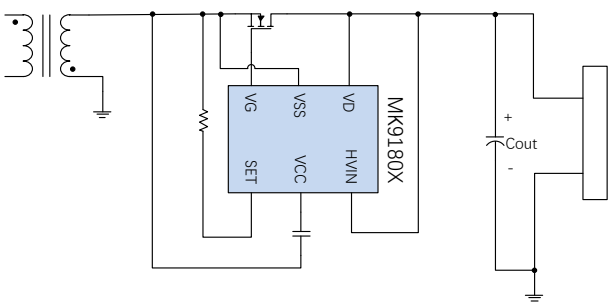
Features

- Operates in a Wide Output Voltage Range Down to Zero Voltage
- Self-supply for Operation with Low Output Voltage and/or High−side Rectification without an Auxiliary Winding
- Gate Drive Clamp Voltage is Up to 9V
- 10ns Fast Turn-off and 25ns Turn-on Delay
- VD/HVIN Pin Supports Negative Voltage Spikes Down to -3V
- Programmable Voltage Ringing Detection to Avoid Potential False Turn-on during DCM
- VG Clamping Circuit Works Well when VCC is Below 2V
- Optimized for <350kHz Frequency
- Supports Active Clamp Flyback with GaN FET or Super-junction MOSFET at Primary Side
- Supports DCM, QR and CCM Operations
- Supports both High-side and Low-side Rectification
- Adaptive Gate Drive for Maximum Efficiency
- SOT23-6 Package Available

Simplified Application



Used in low side rectification

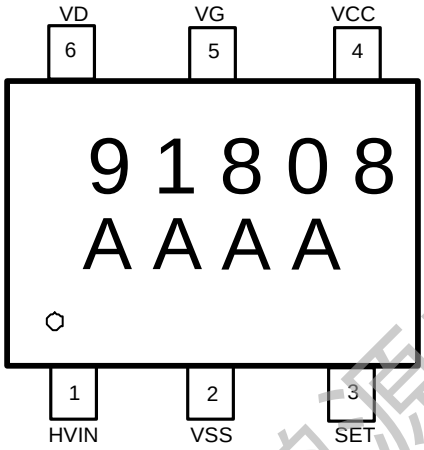


Used in high side rectification

Ordering Information

Ordering No.	Description
MK91808CSA	SOT23-6, 3000 pcs/reel

Pin Configuration and Marking Information



AAAA: Lot Code

SOT23-6

Absolute Maximum Ratings (1)

VCC to VSS ..... –0.3V to +20V
VG to VSS ..... –0.3V to +20V
VD, HVIN to VSS ..... –1V to +115V
SET to VSS..... –0.3V to +20V
VD, HVIN to VSS ..... –3V to +120V (2)

Recommended Operation Conditions

VCC to VSS…..... ……. .3.6V to 9.5V
D to VSS……..-0.7V to 100V
Maximum Junction Temp. (T_J)..... +125°C

THERMAL RESISTANCE (3) Θ_{JA} Θ_{JC}

SOT23-6.....100 66 °C/W

Notes:

(1) Exceeding these ratings may damage the device.

(2) Repetitive pulse< 200ns

(3) Measured on JESDSD51-7, 4 layers PCB

ELECTRICAL CHARACTERISTICS

T_A=25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY MANAGEMENT						
VCC UVLO Rising	VCC_{ON}		4.4	4.6	4.9	V
VCC UVLO Falling	VCC_{OFF}		3.8	4	4.3	V
VCC UVLO Hysteresis	VCC_{HYST}		0.35	0.6		V
VCC Maximum Charging Current	I_{VCC}	VCC=8V, VD=0V, HVIN=14V	40	80		mA
		VCC=5V, HVIN=0V, VD=12V	20	40		mA
VCC Regulation Voltage	VCC_{REG}	VD= 0V, HVIN=14V	8.2	9.1	10	V
		VD=10V, HVIN=0V	5	6	7	
Operating Current	I_{CC}	VCC=9V, C_{LOAD}=2.2nF, F_{SW}=100kHz		2.5	3.5	mA
		VCC=6.5V, C_{LOAD}=2.2nF, F_{SW}=100kHz		2	2.5	mA
Quiescent Current	$I_{q(VCC)}$	VCC=6.5V		350	550	μA
MOSFET VOLTAGE SENSING						
V_D–V_{SS} Adjusting Voltage	V_{DS_reg}		-55	-40	-25	mV
Turn-On Threshold (V_D–V_{SS})	V_{ON_th}		-350	-250	-150	mV
Turn Off Threshold (V_D–V_{SS})	V_{OFF_th}			0	10	mV
Turn-On Propagation Delay	T_{D_on}	C_{LOAD} = 0nF, VD step down from 3V to -0.5V in 5ns, measure VG rising to 1V		25	40	ns
Turn-Off Propagation Delay	T_{D_off}	C_{LOAD} = 0nF, VD step up from -0.5V to 3V in 5ns, measure VG falling to 90% of V_{G-H}		10	15	ns
Turn On Blanking Time	T_{B_ON}	C_{LOAD} = 2.2nF	0.75	1.0	1.2	us
Turn Off Blanking V_{DS} Threshold in T_{B_ON}	V_{B_OFF}			2		V
Turn Off Blanking Time	T_{B_OFF}	C_{LOAD} = 2.2nF	250		350	ns
Turn On VD dv/dt Detection Timer(1)	T_{dvt11}	SET pin tie to VSS, V_{DS} from 2V step down to 0V.		10		ns
GATE DRIVER						

V_G (Low)	VG_L	ILOAD= 100mA		0.1	0.2	V
V_G (High)	VG_H	ILOAD= 100mA	VCC-0.5	VCC-0.3		V
Maximum Source Current(1)	IVG_H			1		A
Maximum Sink Current(1)	IVG_L			4		A
Pull Down Impedance(1)	R_{SINK}	ILOAD= 100mA		0.53		Ω

Notes

(1) Values are verified by characterization on bench, not tested in production

Typical Characteristics VS Temperature

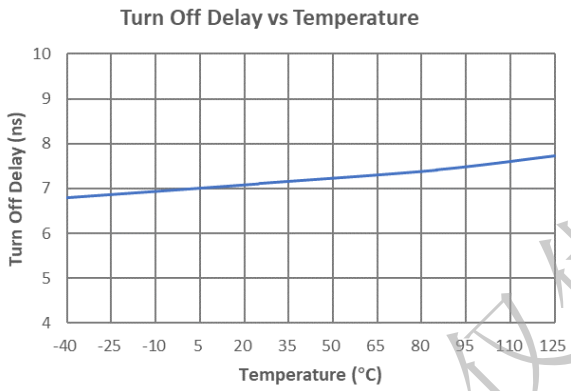


Figure 1. Turn Off Delay vs Temperature

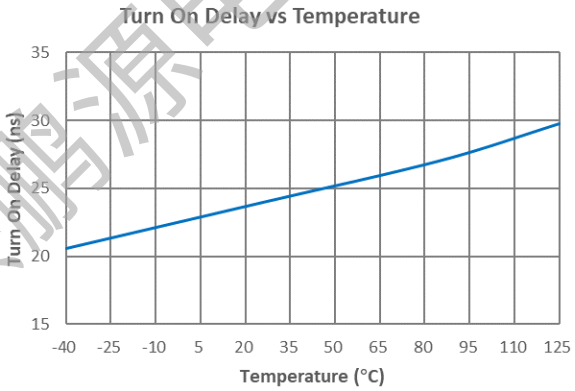


Figure 2. Turn On Delay vs Temperature

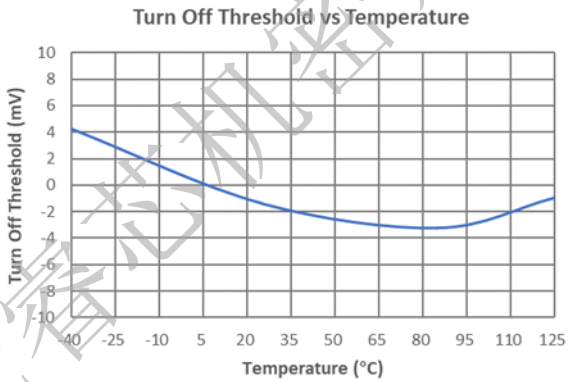


Figure 3. Turn Off Threshold vs Temperature

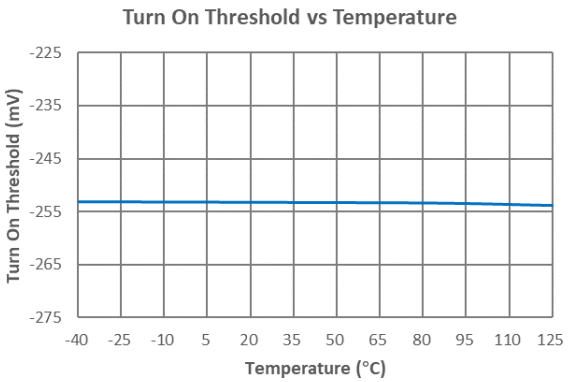


Figure 4. Turn On Threshold vs Temperature

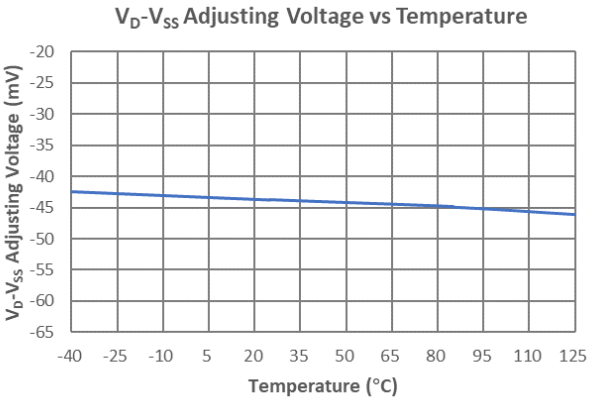


Figure 5. V_D-V_{SS} Adjusting Voltage vs Temperature

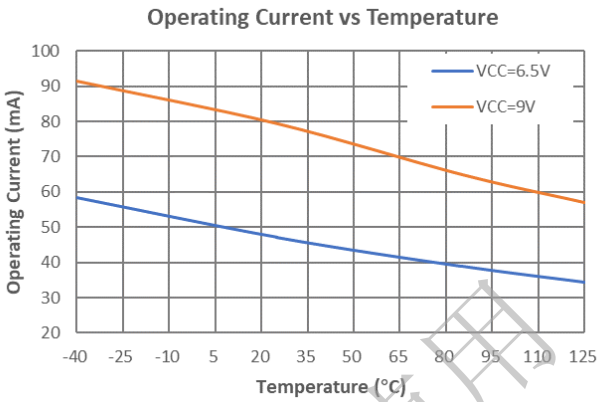


Figure 6. Operating Current vs Temperature (CLOAD=2.2nF, FSW=100kHz)

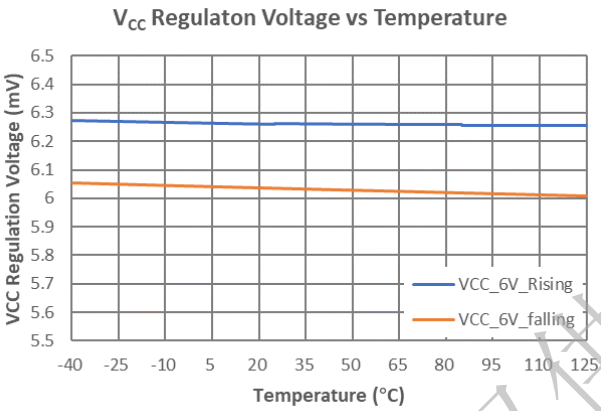


Figure 7. VCC Regulation Voltage vs Temperature (VD= 14V, HVIN=0V)

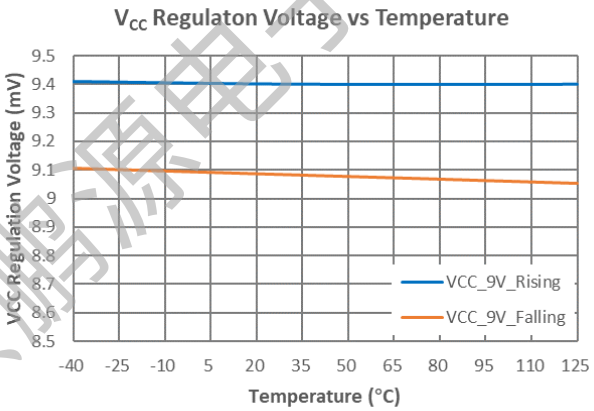


Figure 8. VCC Regulation Voltage vs Temperature (VD= 0V, HVIN=14V)

Pin Functions

Pin #	Name	Description
1	HVIN	HV Linear Regulator Input
2	VSS	Ground, also used as FET source sense reference for VD
3	SET	Programming for turn on signal slew rate detection. To prevent SR controller false turn on by ringing below turn on threshold at VD in DCM and QR modes, any signal slower than pre-set slew rate is not going to turn on VG;
4	VCC	Linear Regulator Output, supply MK9180X
5	VG	Gate drive output
6	VD	FET drain voltage sense; HV pulse LDO input

Block Diagram

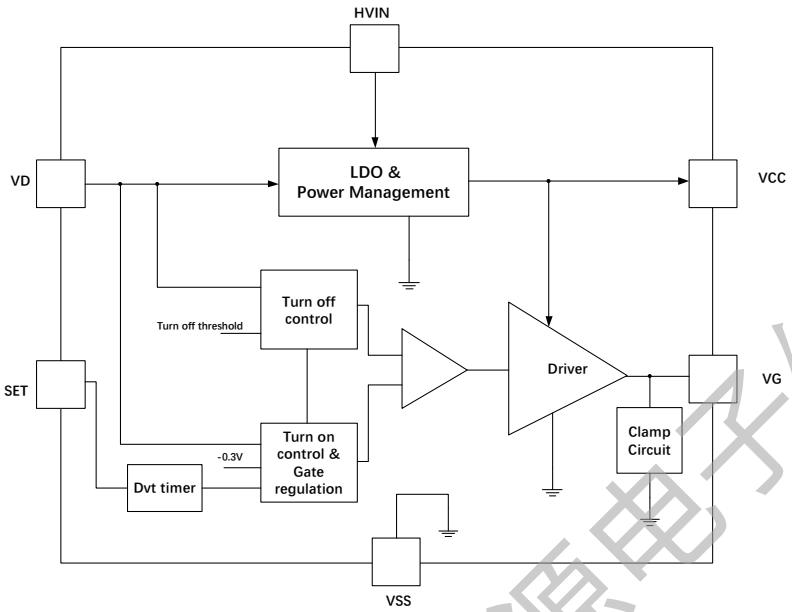


Figure 9. Functional Block Diagram

Operation Descriptions

The MK91808 is an advanced secondary side synchronous rectifier controller and driver for high performance flyback converters, which supports DCM, CCM and QR operations. The extremely low 10ns turn−off propagation delay time and high sink current (~4A) capability of the driver improve SR V_{DS} stress at CCM mode, particularly at the conditions of startup and V_{OUT} shorts to ground. The unique VG clamping circuit works well to prevent VG from turning on by fast rising at VD pin with no VCC, that avoids the shoot through between primary side and secondary side during system startup even if the SR VCC is still below 2V.

VCC AND STARTUP

In order to reduce switching loss and work with different voltage thresholds Vth of MOSFETs, MK91808 provides the flexibility of different VG voltage realized at VCC. VCC is regulated at 9V which supplies MK91808 including VG when connect HVIN pin to a voltage source higher than 9.2V. Here the source for HVIN pin can be a DC voltage such as V_{OUT} for low side rectification or an AC voltage such as the DRAIN of SR MOSFET. The maximum charging current is 80mA while VCC is regulated from HVIN voltage source.

When the voltage on HVIN pin is below 9.2V but above 6V, VCC follows HVIN with dropout voltage depending on the load current at VCC, until HVIN drops to around 6V. Once HVIN drops around 6V, a 40mA current source from VD starts charging up VCC and regulating it at 6V.

The typical system implementations with different bias connections are shown below. A 0.1uF to 1uF bypass capacitor is suggested at VCC pin.

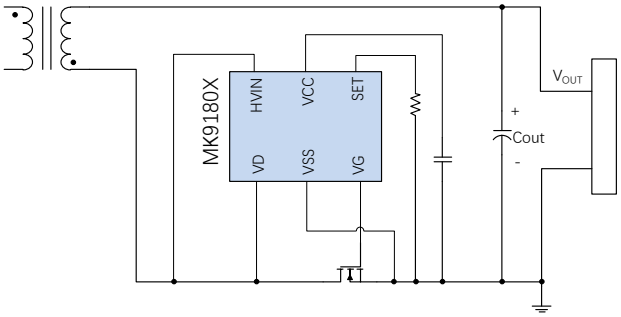


Figure 10. Low-side Rectification 1，$VCC_{\_REG}$=9V

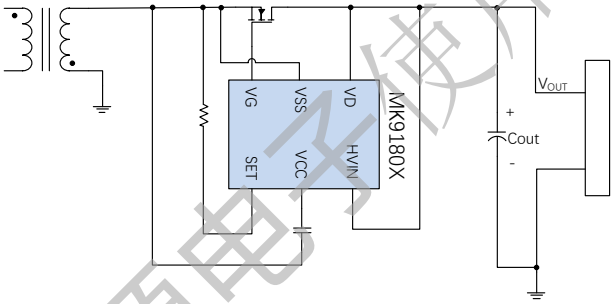


Figure 11. High-side Rectification 1, $VCC_{\_REG}$=9V

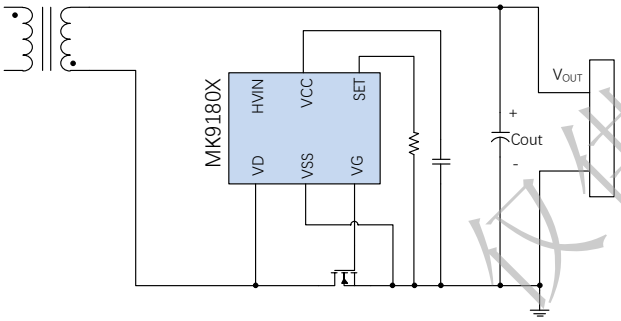


Figure 12. Low-side Rectification 2, $VCC_{\_REG}$=6V

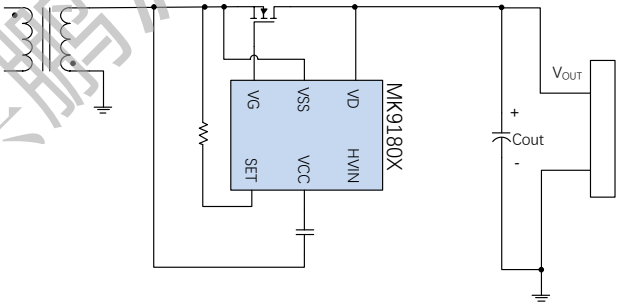


Figure 13. High-side Rectification 2, $VCC_{\_REG}$=6V

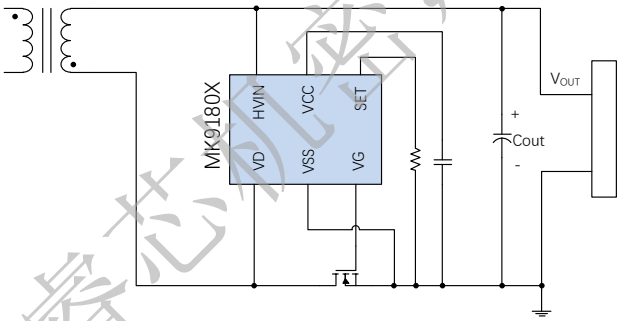


Figure 14. Low-side Rectification 3, $VCC_{\_REG}$=6V to 9V[1]

Note [1] In Low-side Rectification 3, VCC is supplied by VD and regulated at 6V if V_{OUT} is lower than 6V; VCC is regulated at 9V through HVIN if V_{OUT} voltage is larger than 9V; VCC is close to V_{OUT} while V_{OUT} is between 6V and 9V, which generated by HVIN path.

TURN ON PHASE

In order to prevent synchronous rectifier from false turning-on due to the Lp-Csw oscillations for DCM operations, MK91808 not only to set turn on threshold as low as -0.3V, but also has to meet the following criteria:

1. Not within minimum turn-off blanking time T_{B_OFF}, which is defined as the blanking time from VD rising from 2V after VG is off
2. The time for V_{DS} from 2V falling to 0V is less than T_{dvt}, which is set by SET pin

conduction Phase

After SR VG turns on, a minimum blanking time T_{B_ON} is required to prevent the parasitic ringing from falsely turning off SR VG. The minimum turn-on blanking time is around 1.1us for MK91808, during which the turn off threshold is increased to 2V. Right before T_{B_ON} timer expires, MK91808 starts monitoring V_{DS} against a -40mV value to determine if VG needs to be slowly discharged. This operation adjusts V_{DS} of SR MOSFET to be around -40mV until the current through SR MOSFET drops to zero. In CCM mode, VG is prepositioned to be lower than VCC by V_{DS} adjusting scheme so that VG is turned off even faster; In DCM/QR mode, this V_{DS} adjusting design makes V_{DS} cross 0V exponentially faster, which combines with the 10ns turn-off propagation delay to make turn-off timing more accurately regardless of the accuracy of turn-off threshold.

TURN OFF PHASE

MK91808's turn-off threshold is different at different time. Within the minimum turn-on blanking time T_{B_ON}, V_{DS} turn-off threshold is 2V which is the same as V_{B_OFF}. After the minimum turn-on blanking time T_{B_ON}, the turn-off threshold is around 0V, that combines with extremely fast 10ns turn-off propagation delay and 4A VG pull-down (sinking) current, synchronous rectifier is able to be turned off not too early which causes more SR FET body diode conduction time and more negative turn-off ringing, or not too late which creates risk of shoot through between primary side and SR side.

SET TIMER PROGRAMMING

VD falling slew rate is detected through a timer T_{dvt} which is programmed by SET pin, and defined as the time of V_{DS} falling from 2V to 0V. While SET is connected to VSS, T_{dvt} is set to the lowest value

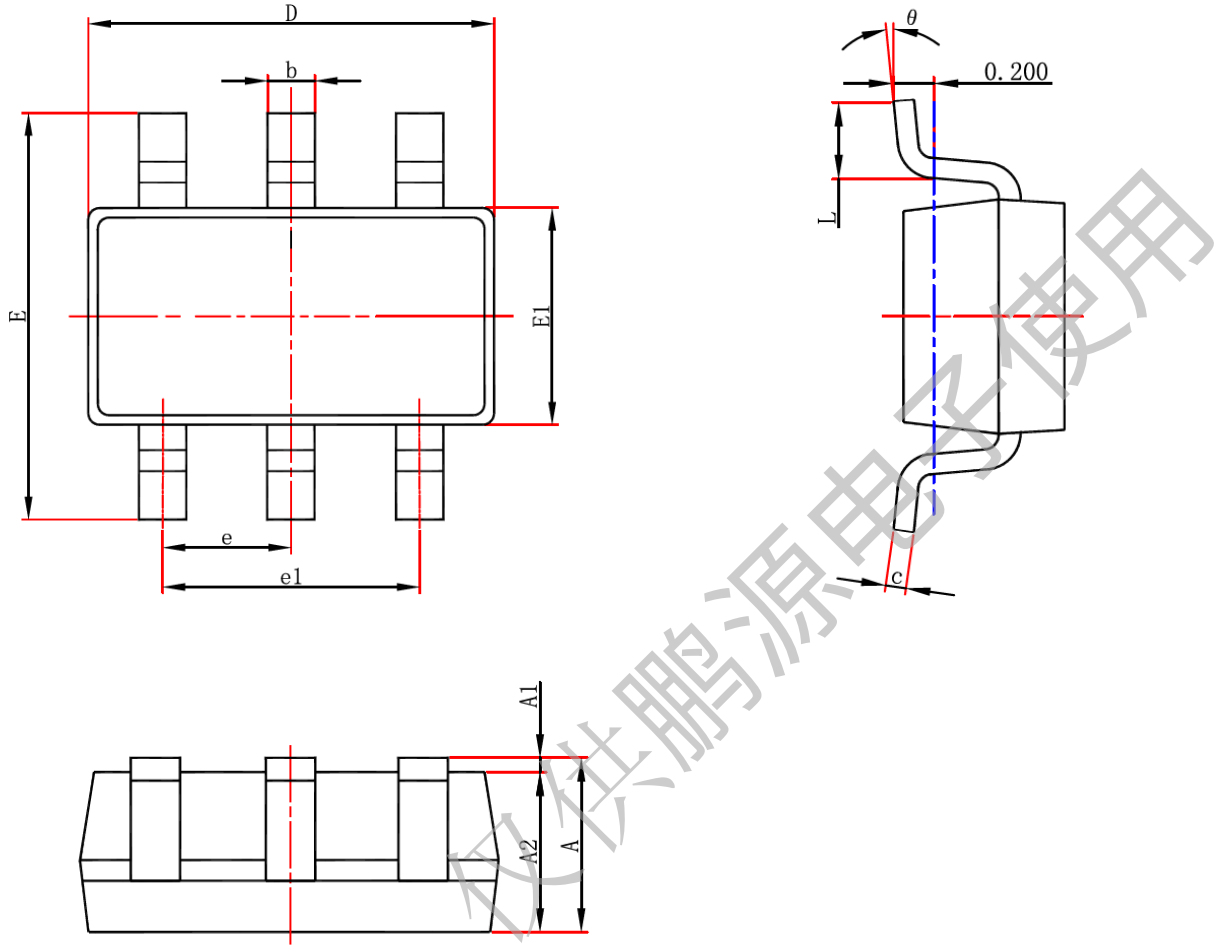
which is around 10ns; T_{dvt} reaches the largest value while SET is floating or connected to VCC; Any T_{dvt} value in-between is realized by an external resistor from SET to VSS. A 20kΩ resistor is recommended at SET pin to cover most applications.

PCB LAYOUT RECOMMENDATIONs

The PCB layout guidance are shown below:

1. The trace from VG pin to the GATE of SR MOSFET needs to be as short as possible. The VSS pin to the SOURCE of SR MOSFET needs to route with short and wide trace
2. The sense loop (VD pin and VSS pin) is as small as possible
3. In two-layer boards, avoid fast dv/dt traces underneath MK91808, such as the DRAIN of SR MOSFET network

Package Information (SOT23-6)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°