# LANSDALE
## *Semiconductor, Inc.*

**ML145151      ML145156**
**ML145152      ML145157**
**ML145155      ML145158**

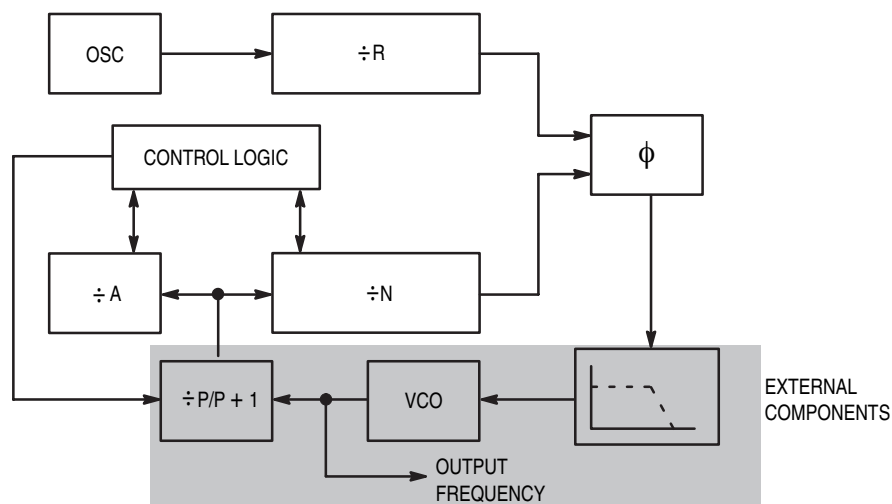### PLL Frequency Synthesizer Family - CMOS

The devices described in this document are typically used as low–power, phase–locked loop frequency synthesizers. When combined with an external low–pass filter and voltage–controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

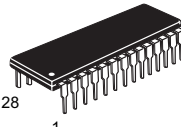| | |
|---|---|
| CATV | TV Tuning |
| AM/FM Radios | Scanning Receivers |
| Two–Way Radios | Amateur Radio |



## CONTENTS

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# LANSDALE
## *Semiconductor, Inc.*

# ML145151
# Parallel-Input PLL
# Frequency Synthesizer
## Interfaces with Single–Modulus Prescalers

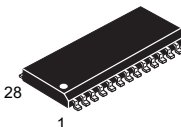**Legacy Device:** *Motorola/Freescale MC145151*

The ML145151 is programmed by 14 parallel–input data lines for the N counter and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, and 14–bit programmable divide–by–N counter.

- Operating Temperature Range: $T_A = -40$ to $85°C$
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates

**P DIP 28 = YP**
PLASTIC DIP
CASE 710

**SO 28W = -6P**
SOG PACKAGE
CASE 751F

### CROSS REFERENCE/ORDERING INFORMATION

| PACKAGE | MOTOROLA | LANSDALE |
|---|---|---|
| P DIP 28 | MC145151P2 | ML145151YP |
| SO 28W | MC145151DW2 | ML145151-6P |

**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| $f_{in}$ | 1 | 28 | LD |
| $V_{SS}$ | 2 | 27 | $OSC_{in}$ |
| $V_{DD}$ | 3 | 26 | $OSC_{out}$ |
| $PD_{out}$ | 4 | 25 | N11 |
| RA0 | 5 | 24 | N10 |
| RA1 | 6 | 23 | N13 |
| RA2 | 7 | 22 | N12 |
| $\phi_R$ | 8 | 21 | T/R |
| $\phi_V$ | 9 | 20 | N9 |
| $f_V$ | 10 | 19 | N8 |
| N0 | 11 | 18 | N7 |
| N1 | 12 | 17 | N6 |
| N2 | 13 | 16 | N5 |
| N3 | 14 | 15 | N4 |
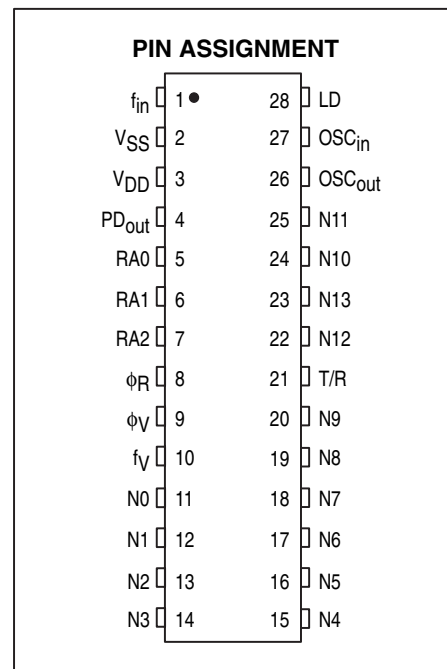
## ML145151 BLOCK DIAGRAM
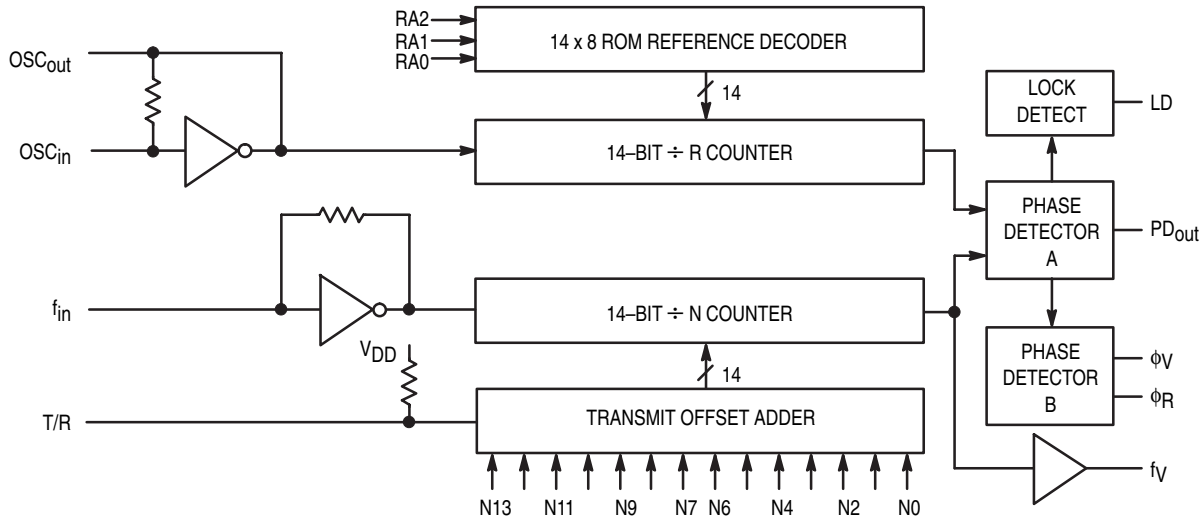


NOTE: N0 – N13 inputs and inputs RA0, RA1, and RA2 have pull–up resistors that are not shown.

### PIN DESCRIPTIONS

**INPUT PINS**

**$f_{in}$**
**Frequency Input (Pin 1)**

Input to the ÷N portion of the synthesizer. $f_{in}$ is typically derived from loop $V_{CO}$ and is AC coupled into the device. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

**RA0 – RA2**
**Reference Address Inputs (Pins 5, 6, 7)**

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

| Reference Address Code | | | Total Divide Value |
|---|---|---|---|
| RA2 | RA1 | RA0 | |
| 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 128 |
| 0 | 1 | 0 | 256 |
| 0 | 1 | 1 | 512 |
| 1 | 0 | 0 | 1024 |
| 1 | 0 | 1 | 2048 |
| 1 | 1 | 0 | 2410 |
| 1 | 1 | 1 | 8192 |

**N0 – N11**
**N Counter Programming Inputs (Pins 11 – 20, 22 – 25)**

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least sig-

nificant and N13 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only an SPST switch to alter data to the zero state.

**T/R**
**Transmit/Receive Offset Adder Input (Pin 21)**

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the $V_{CO}$ frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull–up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

**$OSC_{in}$, $OSC_{out}$**
**Reference Oscillator Input/Output (Pins 27, 26)**

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from $OSC_{in}$ to ground and $OSC_{out}$ to ground. $OSC_{in}$ may also serve as the input for an externally generated reference signal. This signal is typically AC coupled to $OSC_{in}$, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to $OSC_{out}$.

**OUTPUT PINS**

**PDout**
**Phase Detector A Output (Pin 4)**

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ΦV and ΦR).

Frequency $f_V > f_R$ or $f_V$ Leading: Negative Pulses
Frequency $f_V < f_R$ or $f_V$ Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

**φR,φV**
**Phase Detector B Outputs (Pins 8, 9)**

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see $PD_{out}$).

If frequency $f_V$ is greater than $f_R$ or if the phase of $f_V$ is leading, then error information is provided by φV pulsing low. φR remains essentially high.

If the frequency $f_V$ is less than $f_R$ or if the phase of $f_V$ is lagging, then error information is provided by φR pulsing low. φV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both φV and φR remain high except for a small minimum time period when both pulse low in phase.

**$f_V$**
**N Counter Output (Pin 10)**

This is the buffered output of the ÷ N counter that is inter-nally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

**LD**
**Lock Detector Output (Pin 28)**

Essentially a high level when loop is locked ($f_R$, $f_V$ of same phase and frequency). Pulses low when loop is out of lock.

**POWER SUPPLY**

**$V_{DD}$**
**Positive Power Supply (Pin 3)**

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to $V_{SS}$.

**$V_{SS}$**
**Negative Power Supply (Pin 2)**

The most negative supply potential. This pin is usually-ground.

**TYPICAL APPLICATIONS**



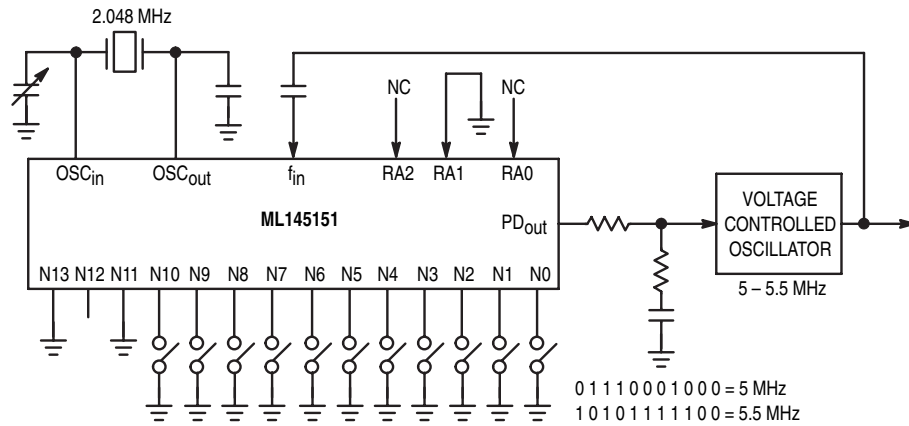0 1 1 1 0 0 0 1 0 0 0 = 5 MHz
1 0 1 0 1 1 1 1 1 0 0 = 5.5 MHz

**Figure 1. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz**
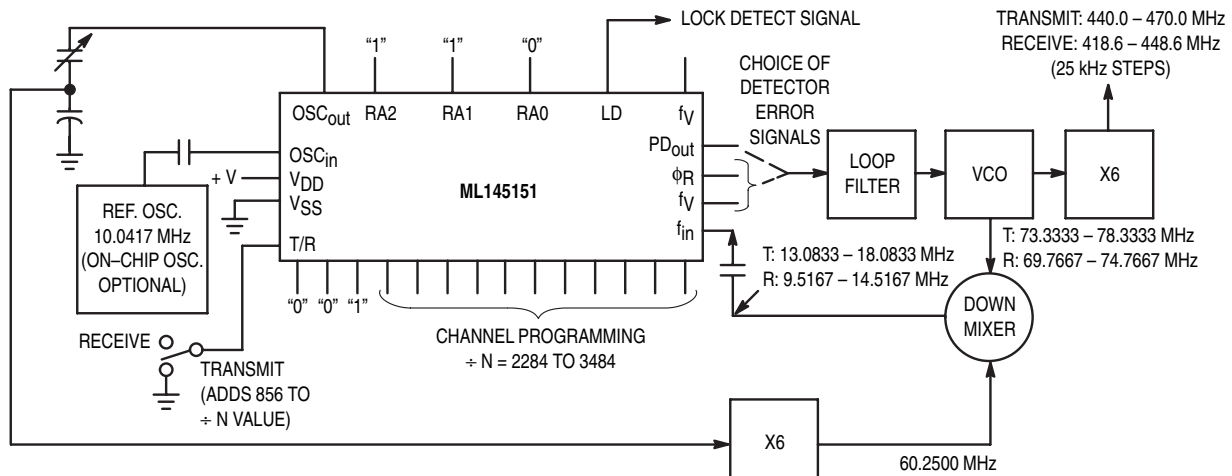


NOTES:
1. $f_R$ = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440 – 470 MHz band. Similar implementation applies to the 406 – 440 MHz band.
   For 470 – 512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

**Figure 2. Synthesizer for Land Mobile Radio UHF Bands**

*ML145151 Data Sheet Continued on Page 23*

# LANSDALE
## *Semiconductor, Inc.*

# ML145152
# Parallel-Input PLL
# Frequency Synthesizer
### Interfaces with Dual–Modulus Prescalers

**Legacy Device:** *Motorola/Freescale MC145152*

The ML145152 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, two–output phase detector, 10–bit programmable divide–by–N counter, and 6–bit programmable ÷ A counter.

- Operating Temperature Range: $T_A$ = – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
- See Application Note AN980
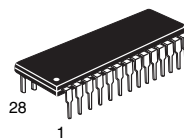
**P DIP 28 = YP**
PLASTIC DIP
CASE 710
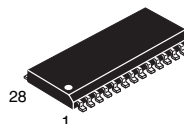
**SO 28W = -6P**
SOG PACKAGE
CASE 751F

**CROSS REFERENCE/ORDERING INFORMATION**

| PACKAGE | MOTOROLA | LANSDALE |
|---|---|---|
| P DIP 28 | MC145152P2 | ML145152YP |
| SO 28W | MC145152DW2 | ML145152-6P |

**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

**PIN ASSIGNMENT**

| | | | |
|---|---|---|---|
| $f_{in}$ | 1 ● | 28 | LD |
| $V_{SS}$ | 2 | 27 | $OSC_{in}$ |
| $V_{DD}$ | 3 | 26 | $OSC_{out}$ |
| RA0 | 4 | 25 | A4 |
| RA1 | 5 | 24 | A3 |
| RA2 | 6 | 23 | A0 |
| $\phi_R$ | 7 | 22 | A2 |
| $\phi_V$ | 8 | 21 | A1 |
| MC | 9 | 20 | N9 |
| A5 | 10 | 19 | N8 |
| N0 | 11 | 18 | N7 |
| N1 | 12 | 17 | N6 |
| N2 | 13 | 16 | N5 |
| N3 | 14 | 15 | N4 |

## ML145152 BLOCK DIAGRAM
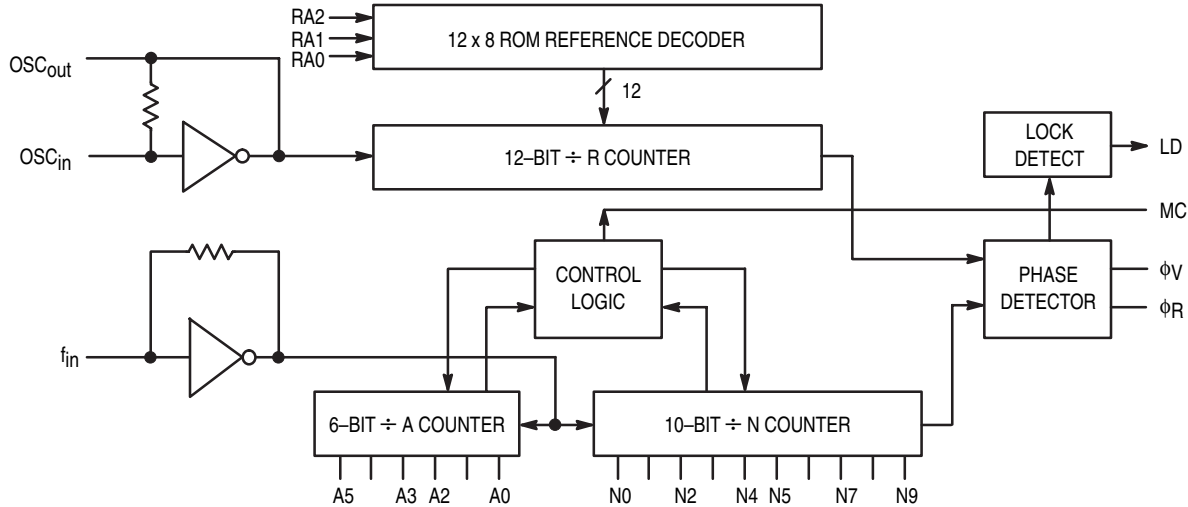


NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull–up resistors that are not shown.

## PIN DESCRIPTIONS

### INPUT PINS

### $f_{in}$
### Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. $f_{in}$ is typically derived from a dual–modulus prescaler and is AC coupled into the device. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

### RA0, RA1, RA2
### Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

| Reference Address Code | | | Total Divide Value |
|---|---|---|---|
| RA2 | RA1 | RA0 | |
| 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 64 |
| 0 | 1 | 0 | 128 |
| 0 | 1 | 1 | 256 |
| 1 | 0 | 0 | 512 |
| 1 | 0 | 1 | 1024 |
| 1 | 1 | 0 | 1160 |
| 1 | 1 | 1 | 2048 |

### N0 – N9
### N Counter Programming Inputs (Pins 11 – 20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

### A0 – A5
### A Counter Programming Inputs(Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of $f_{in}$ that require a logic 0 on the MC output (see Dual–Modulus Prescaling section). The A inputs all have internal pull–up resis-

tors that ensure that inputs left open will remain at a logic 1.

### $OSC_{in}$, $OSC_{out}$
### Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from $OSC_{in}$ to ground and $OSC_{out}$ to ground. $OSC_{in}$ may also serve as the input for an externally generated reference signal. This signal is typically AC coupled to $OSC_{in}$, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to $OSC_{out}$.

### OUTPUT PINS

### $\phi R, \phi V$
### Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop–error signal.

If the frequency $f_V$ is greater than $f_R$ or if the phase of $f_V$ is leading, then error information is provided by $\phi V$ pulsing low. $\phi R$ remains essentially high.

If the frequency $f_V$ is less than $f_R$ or if the phase of $f_V$ is lagging, then error information is provided by $\phi R$ pulsing low. $\phi V$ remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both $\phi V$ and $\phi R$ remain high except for a small minimum time period when both pulse low in phase.

### MC
### Dual–Modulus Prescale Control Output (Pin 9)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to

their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (NT)=N•P+A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

## LD
### Lock Detector Output (Pin 28)

Essentially a high level when loop is locked ($f_R$, $f_V$ of same phase and frequency). Pulses low when loop is out of lock.
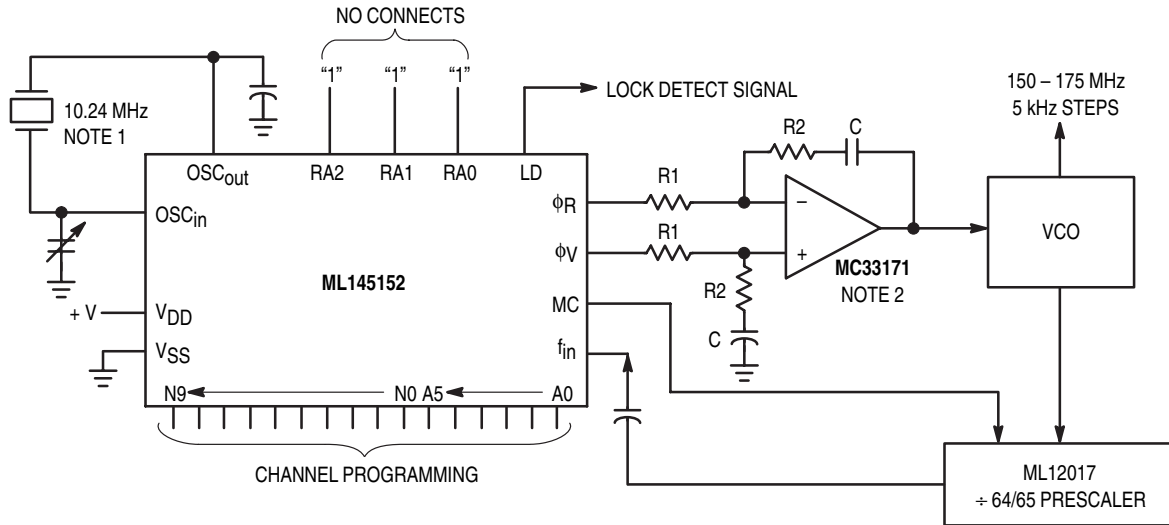
## POWER SUPPLY

### VDD
### Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to $V_{SS}$.

### $V_{SS}$
### Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually-ground.

## TYPICAL APPLICATIONS



NOTES:
1. Off–chip oscillator optional.
2. The $\phi_R$ and $\phi_V$ outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The $\phi_R$ and $\phi_V$ outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

**Figure 1. Synthesizer for Land Mobile Radio VHF Bands**
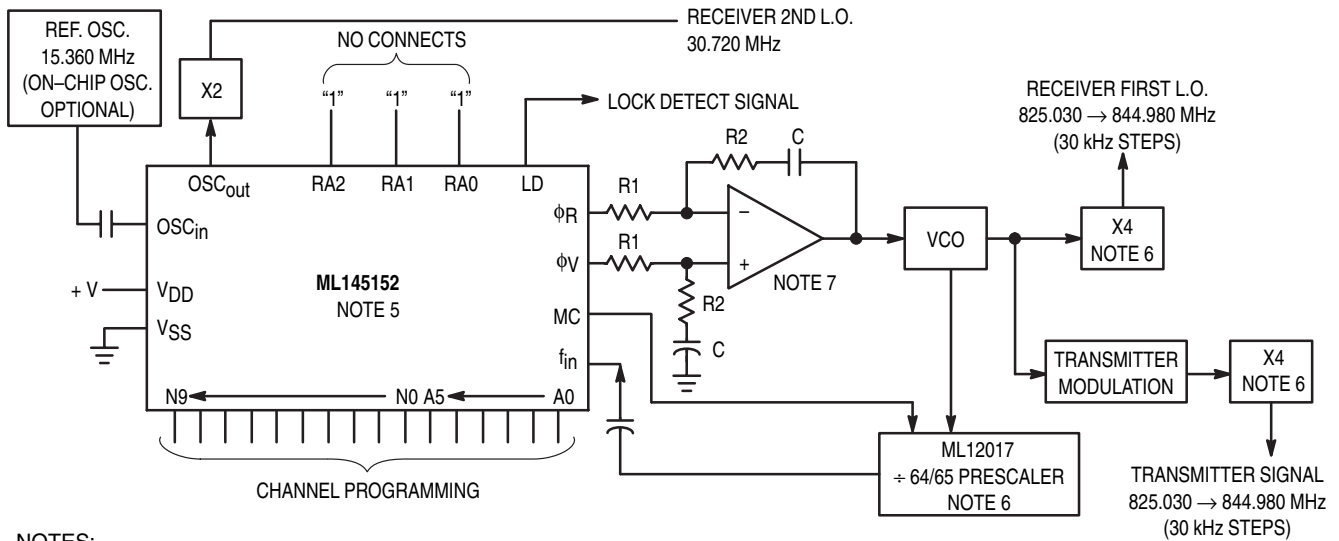
NOTES:
1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3. $f_R$ = 7.5 kHz; ÷ R = 2048.
4. $N_{total}$ = N • 64 + A = 27501 to 28166; N = 429 to 440; A = 0 to 63.
5. ML145158 may be used where serial data entry is desired.
6. High frequency prescalers may be used for higher frequency VCO and $f_{ref}$ implementations.
7. The $\phi_R$ and $\phi_V$ outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The $\phi_R$ and $\phi_V$ outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

**Figure 2. 666–Channel, Computer–Controlled, Mobile Radiotelephone Synthesizer**
**for 800 MHz Cellular Radio Systems**

# LANSDALE
## *Semiconductor, Inc.*

# ML145155
# Serial–Input PLL
# Frequency Synthesizer
## Interfaces with Single–Modulus Prescalers

**Legacy Device:** *Motorola/Freescale MC145155-2*

The ML145155 is programmed by a clocked, serial input, 16–bit data stream. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, 14–bit programmable divide–by–N counter, and the necessary shift register and latch circuitry for accepting serial input data.

- Operating Temperature Range: $T_A = -40$ to $85°C$
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open–Drain Switch Outputs
- 8 User–Selectable ÷ R Values: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates
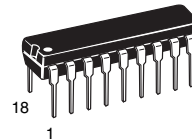
**P DIP 18 = VP**
PLASTIC DIP
CASE 707
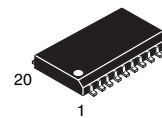
**SOG 20W = -6P**
SOG PACKAGE
CASE 751D

### CROSS REFERENCE/ORDERING INFORMATION

| PACKAGE | MOTOROLA | LANSDALE |
|---------|----------|----------|
| P DIP 18 | MC145155P2 | ML145155VP |
| SOG 20W | MC145155DW2 | ML145155-6P |

**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

## PIN ASSIGNMENTS

### PLASTIC DIP

| | | | | |
|---|---|---|---|---|
| RA1 | 1 | 18 | RA0 |
| RA2 | 2 | 17 | $OSC_{in}$ |
| $\phi V$ | 3 | 16 | $OSC_{out}$ |
| $\phi R$ | 4 | 15 | $REF_{out}$ |
| $V_{DD}$ | 5 | 14 | SW2 |
| $PD_{out}$ | 6 | 13 | SW1 |
| $V_{SS}$ | 7 | 12 | ENB |
| LD | 8 | 11 | DATA |
| $f_{in}$ | 9 | 10 | CLK |

### SOG PACKAGE

| | | | | |
|---|---|---|---|---|
| RA1 | 1 | 20 | RA0 |
| RA2 | 2 | 19 | $OSC_{in}$ |
| $\phi V$ | 3 | 18 | $OSC_{out}$ |
| $\phi R$ | 4 | 17 | $REF_{out}$ |
| $V_{DD}$ | 5 | 16 | NC |
| $PD_{out}$ | 6 | 15 | SW2 |
| $V_{SS}$ | 7 | 14 | SW1 |
| NC | 8 | 13 | ENB |
| LD | 9 | 12 | DATA |
| $f_{in}$ | 10 | 11 | CLK |
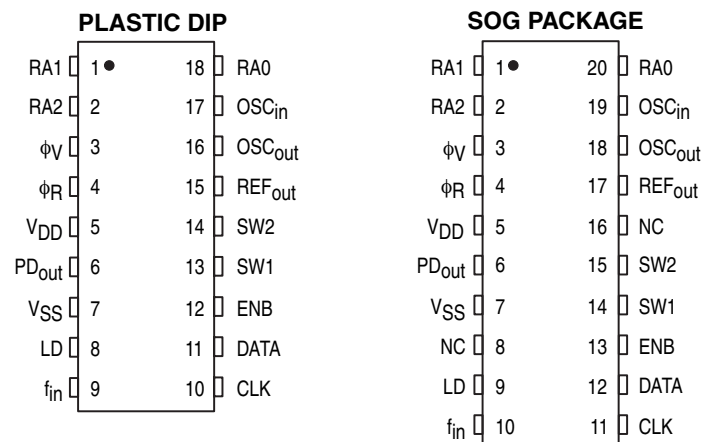
NC = NO CONNECTION

**ML145155  BLOCK DIAGRAM**



## PIN DESCRIPTIONS

**INPUT PINS**

**$f_{in}$**
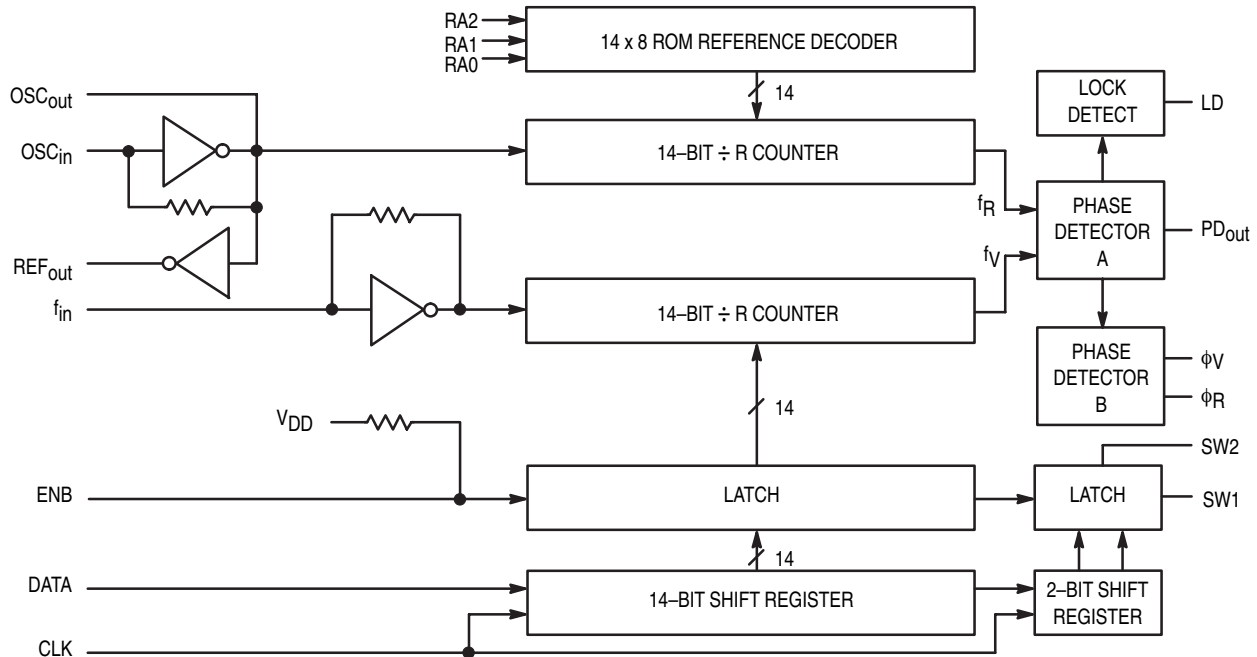
**Frequency Input (PDIP – Pin 9, SOG – Pin 10)**

Input to the ÷ N portion of the synthesizer. $f_{in}$ is typically derived from loop VCO and is AC coupled into the device. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

**RA0, RA1, RA2**

**Reference Address Inputs (PDIP – Pins 18, 1, 2; SOG – Pins 20, 1, 2)**

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

| Reference Address Code | | | Total Divide Value |
|---|---|---|---|
| **RA2** | **RA1** | **RA0** | |
| 0 | 0 | 0 | 16 |
| 0 | 0 | 1 | 512 |
| 0 | 1 | 0 | 1024 |
| 0 | 1 | 1 | 2048 |
| 1 | 0 | 0 | 3668 |
| 1 | 0 | 1 | 4096 |
| 1 | 1 | 0 | 6144 |
| 1 | 1 | 1 | 8192 |

**CLK, DATA**

**Shift Register Clock, Serial Data Inputs (PDIP – Pins 10, 11; SOG – Pins 11, 12)**

Each low–to–high transition clocks one bit into the on–chip 16–bit shift register. The Data input provides programming information for the 14–bit ÷ N counter and the two switch

signals SW1 and SW2. The entry format is as follows:



**ENB**
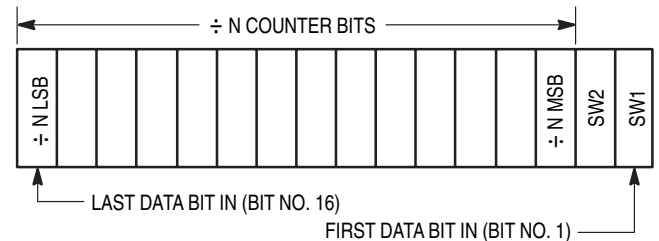
**Latch Enable Input (PDIP – Pin 12, SOG – Pin 13)**

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on–chip pull–up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

**$OSC_{in}$, $OSC_{out}$**

**Reference Oscillator Input/Output (PDIP – Pins 17, 16; SOG – Pins 19, 18)**

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from $OSC_{in}$ to ground and $OSC_{out}$ to ground. $OSC_{in}$ may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to $OSC_{in}$, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to $OSC_{out}$.

ML145155

**OUTPUT PINS**
**PD$_{out}$**
**Phase Detector A Output (PDIP, SOG – Pin 6)**
   Three–state output of phase detector for use as loop error signal. Double–ended outputs are also available for this purpose (see φV and φR).
   Frequency f$_V$ > f$_R$ or f$_V$ Leading: Negative Pulses
   Frequency f$_V$ < f$_R$ or f$_V$ Lagging: Positive Pulses
   Frequency f$_V$ = f$_R$ and Phase Coincidence: High–Impedance State

**φR, φV**
**Phase Detector B Outputs (PDIP, SOG – Pins 4, 3)**
   These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD$_{out}$**).
   If frequency f$_V$ is greater than f$_R$ or if the phase of f$_V$ is leading, then error information is provided by f$_V$ pulsing low. f$_R$ remains essentially high.
   If the frequency f$_V$ is less than f$_R$ or if the phase of f$_V$ is lagging, then error information is provided by f$_R$ pulsing low. f$_V$ remains essentially high.
   If the frequency of f$_V$ = f$_R$ and both are in phase, then both f$_V$ and f$_R$ remain high except for a small minimum time period when both pulse low in phase.

**LD**
**Lock Detector Output (PDIP – Pin 8, SOG – Pin 9)**
   Essentially a high level when loop is locked (f$_R$, f$_V$ of same

phase and frequency). LD pulses low when loop is out of lock.

**SW1, SW2**
**Band Switch Outputs (PDIP – Pins 13, 14; SOG – Pins 14, 15)**
   SW1 and SW2 provide latched open–drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V, independent of the V$_{DD}$ supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high–impedance state, while a logic 0 causes the output to be low.

**REF$_{out}$**
**Buffered Reference Oscillator Output (PDIP, SOG – Pin 15)**
   Buffered output of on–chip reference oscillator or externally provided reference–input signal.
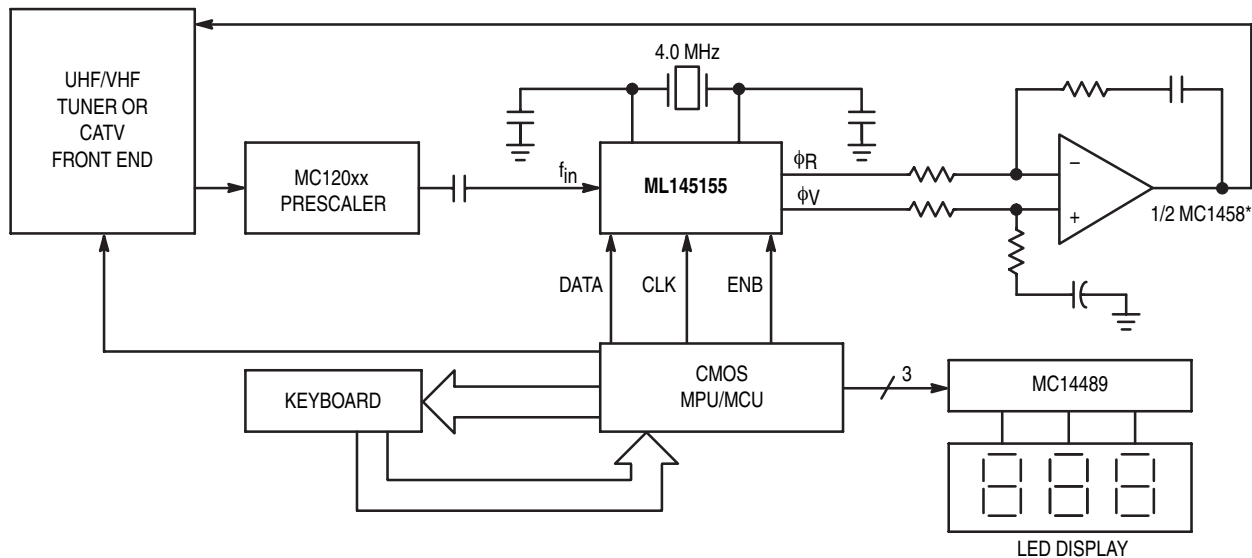
**POWER SUPPLY**

**VDD**
**Positive Power Supply (PDIP, SOG – Pin 5)**
   The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V$_{SS}$.

**VSS**
**Negative Power Supply (PDIP, SOG – Pin 7)**
   The most negative supply potential. This pin is usually ground.

**TYPICAL APPLICATIONS**



* The φR and φV outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop – Low–Pass Filter Design page for additional information. The φR and φV outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

**Figure 1. Microprocessor–Controlled TV/CATV Tuning System with Serial Interface**

**ML145155**



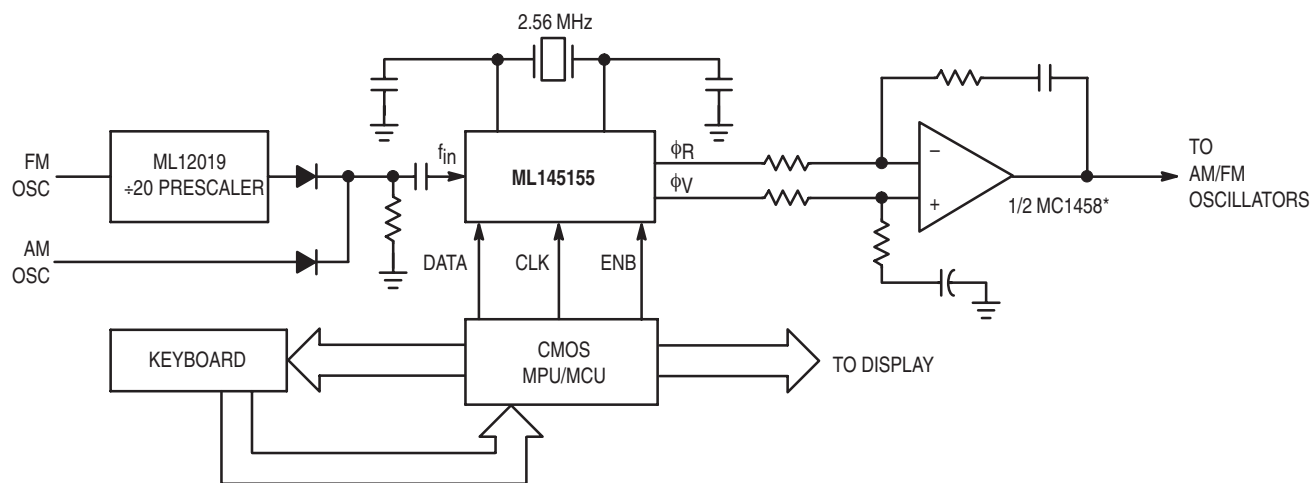\* The $\phi_R$ and $\phi_V$ outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop – Low–Pass Filter Design page for additional information. The $\phi_R$ and $\phi_V$ outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

**Figure 2. AM/FM Radio Synthesizer**

# LANSDALE
## *Semiconductor, Inc.*

# ML145156
# Serial–Input PLL
# Frequency Synthesizer
## Interfaces with Dual–Modulus Prescalers

**Legacy Device:** *Motorola/Freescale MC145156-2*

The ML145156 is programmed by a clocked, serial input, 19–bit data stream. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, 10–bit programmable divide–by–N counter, 7–bit program-mable divide–by–A counter, and the necessary shift register and latch circuitry for accepting serial input data.

- Operating Temperature Range: $T_A$ = – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open–Drain Switch Outputs
- Dual Modulus/Serial Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 640, 1000, 1024, 2048
- ÷ N Range = 3 to 1023, ÷A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates
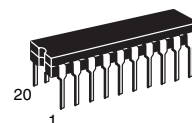
**P DIP 20 = RP**
PLASTIC DIP
CASE 738
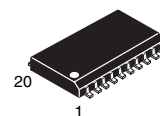
**SOG 20W = -6P**
SOG PACKAGE
CASE 751D

**CROSS REFERENCE/ORDERING INFORMATION**

| PACKAGE | MOTOROLA | LANSDALE |
|---|---|---|
| P DIP 20 | MC145156P2 | ML145156RP |
| SOG 20W | MC145156DW2 | ML145156-6P |

**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

**PIN ASSIGNMENT**

| | | | |
|---|---|---|---|
| RA1 | 1 | 20 | RA0 |
| RA2 | 2 | 19 | OSC$_{in}$ |
| φV | 3 | 18 | OSC$_{out}$ |
| φR | 4 | 17 | REF$_{out}$ |
| V$_{DD}$ | 5 | 16 | TEST |
| PD$_{out}$ | 6 | 15 | SW2 |
| V$_{SS}$ | 7 | 14 | SW1 |
| MC | 8 | 13 | ENB |
| LD | 9 | 12 | DATA |
| f$_{in}$ | 10 | 11 | CLK |

## ML145156 BLOCK DIAGRAM

RA2 → 
RA1 → 
RA0 → 12 x 8 ROM REFERENCE DECODER

/ 12

OSC$_{in}$ → 

OSC$_{out}$

REF$_{out}$

MC

12–BIT ÷ R COUNTER

LOCK DETECT → LD

CONTROL LOGIC

f$_R$

f$_V$

PHASE DETECTOR A → PD$_{out}$

f$_{in}$ → 

7–BIT ÷ A COUNTER ↔ 10–BIT ÷ N COUNTER

PHASE DETECTOR B → φV
φR

V$_{DD}$ → 

ENB

÷ A COUNTER LATCH

/ 7

÷ N COUNTER LATCH

/ 10

SW2

LATCH → SW1

DATA → 

CLK → 

7–BIT SHIFT REGISTER

/ 7

10–BIT SHIFT REGISTER

/ 10

2–BIT SHIFT REGISTER
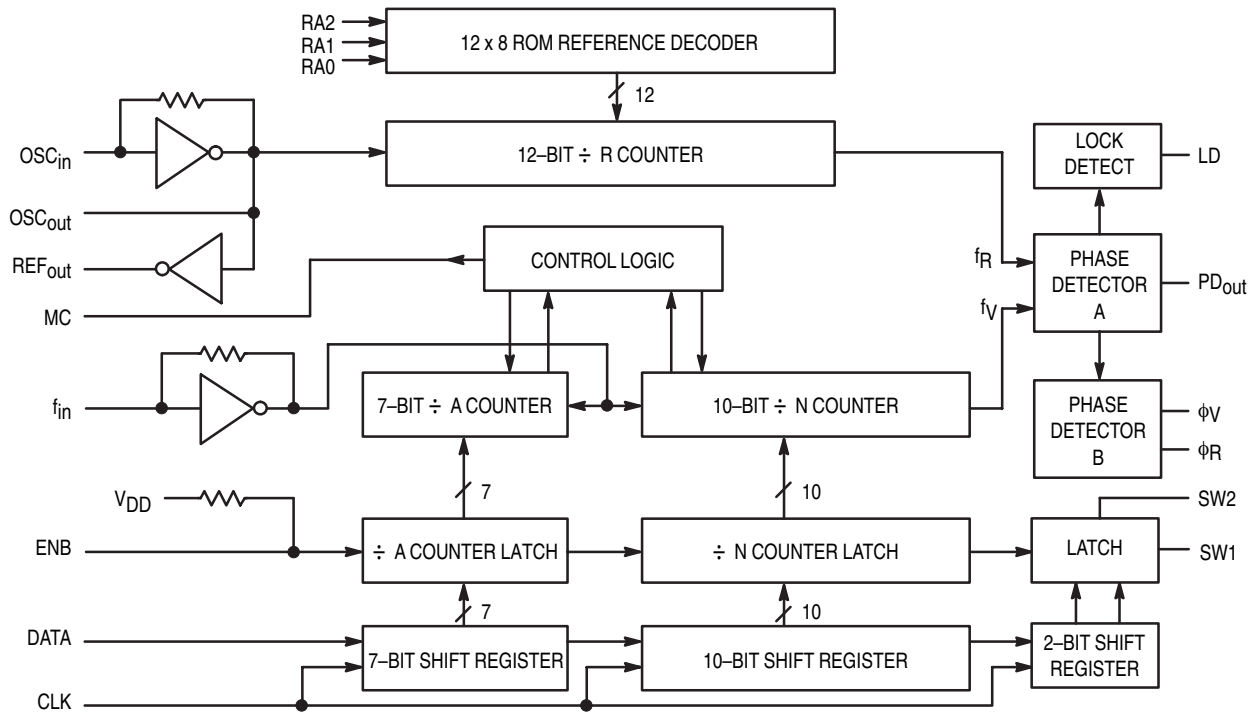
### PIN DESCRIPTIONS

**INPUT PINS**

#### f$_{in}$
**Frequency Input (Pin 10)**

Input to the positive edge triggered ÷ N and ÷ A counters. f$_{in}$ is typically derived from a dual–modulus prescaler and is AC coupled into the device. For larger amplitude signals (standard CMOS logic levels), DC coupling may be used.
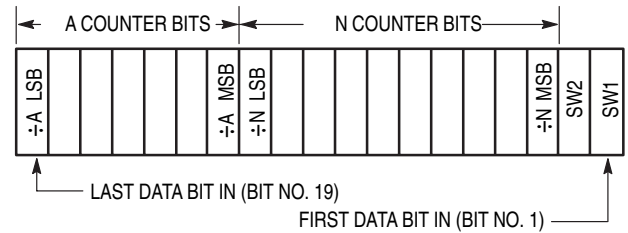
#### RA0, RA1, RA2
**Reference Address Inputs (Pins 20, 1, 2)**

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

| Reference Address Code | | | Total Divide Value |
|---|---|---|---|
| **RA2** | **RA1** | **RA0** | |
| 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 64 |
| 0 | 1 | 0 | 128 |
| 0 | 1 | 1 | 256 |
| 1 | 0 | 0 | 640 |
| 1 | 0 | 1 | 1000 |
| 1 | 1 | 0 | 1024 |
| 1 | 1 | 1 | 2048 |

#### CLK, DATA
**Shift Register Clock, Serial Data Inputs (Pins 11, 12)**

Each low–to–high transition clocks one bit into the on–chip 19–bit shift register. The data input provides programming information for the 10–bit ÷ N counter, the 7–bit ÷ A counter, and the two switch signals SW1 and SW2. The entry format is as follows:

|← A COUNTER BITS →|← N COUNTER BITS →|

÷A LSB | | | | | ÷A MSB | ÷N LSB | | | | | | | ÷N MSB | SW2 | SW1

↑ LAST DATA BIT IN (BIT NO. 19)

FIRST DATA BIT IN (BIT NO. 1) ↑

#### ENB
**Latch Enable Input (Pin 13)**

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on–chip pull–up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

#### OSC$_{in}$, OSC$_{out}$
**Reference Oscillator Input/Output (Pins 19, 18)**

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC$_{in}$ to ground and OSC$_{out}$ to ground. OSC$_{in}$ may also serve as the input for an externally–generated reference signal. This signal is typically AC coupled to OSC$_{in}$, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC$_{out}$.

#### TEST
**Factory Test Input (Pin 16)**

Used in manufacturing. Must be left open or tied to V$_{SS}$.

## OUTPUT PINS

### PDout
**Phase Detector A Output (Pin 6)**

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see $\phi V$ and $\phi R$).

Frequency $f_V > f_R$ or $f_V$ Leading: Negative Pulses
Frequency $f_V < f_R$ or $f_V$ Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

### $\phi R$, $\phi V$
**Phase Detector B Outputs (Pins 4, 3)**

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PDout**).

If frequency $f_V$ is greater than $f_R$ or if the phase of $f_V$ is leading, then error information is provided by $\phi V$ pulsing low. $\phi R$ remains essentially high.

If the frequency $f_V$ is less than $f_R$ or if the phase of $f_V$ is lagging, then error information is provided by $\phi R$ pulsing low. $\phi V$ remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both $\phi V$ and $\phi R$ remain high except for a small minimum time period when both pulse low in phase.

### MC
**Dual–Modulus Prescale Control Output (Pin 8)**

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value ($N_T$) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

### LD
**Lock Detector Output (Pin 9)**

Essentially a high level when loop is locked ($f_R$, $f_V$ of same phase and frequency). LD pulses low when loop is out of lock.

### SW1, SW2
**Band Switch Outputs (Pins 14, 15)**

SW1 and SW2 provide latched open–drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 V, independent of the $V_{DD}$ supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high–impedance state, while a logic 0 causes the output to be low.

### REFout
**Buffered Reference Oscillator Output (Pin 17)**

Buffered output of on–chip reference oscillator or externally provided reference–input signal.

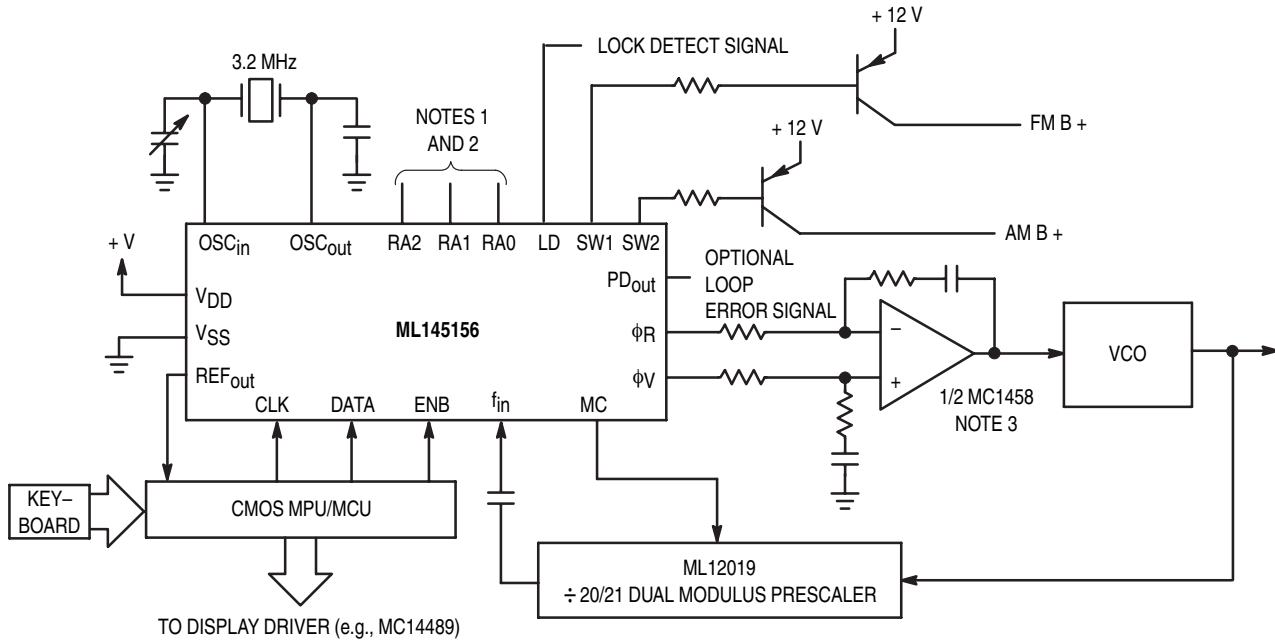## POWER SUPPLY

### VDD
**Positive Power Supply (Pin 5)**

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to $V_{SS}$.

### VSS
**Negative Power Supply (Pin 7)**

The most negative supply potential. This pin is usually ground.

# ML145156
## TYPICAL APPLICATIONS



NOTES:
1. For AM: channel spacing = 5 kHz, $\div R = \div 640$ (code 100).
2. For FM: channel spacing = 25 kHz, $\div R = \div 128$ (code 010).
3. The $\phi_R$ and $\phi_V$ outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop – Low–Pass Filter Design page for additional information. The $\phi_R$ and $\phi_V$ outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

**Figure 1. AM/FM Radio Broadcast Synthesizer**
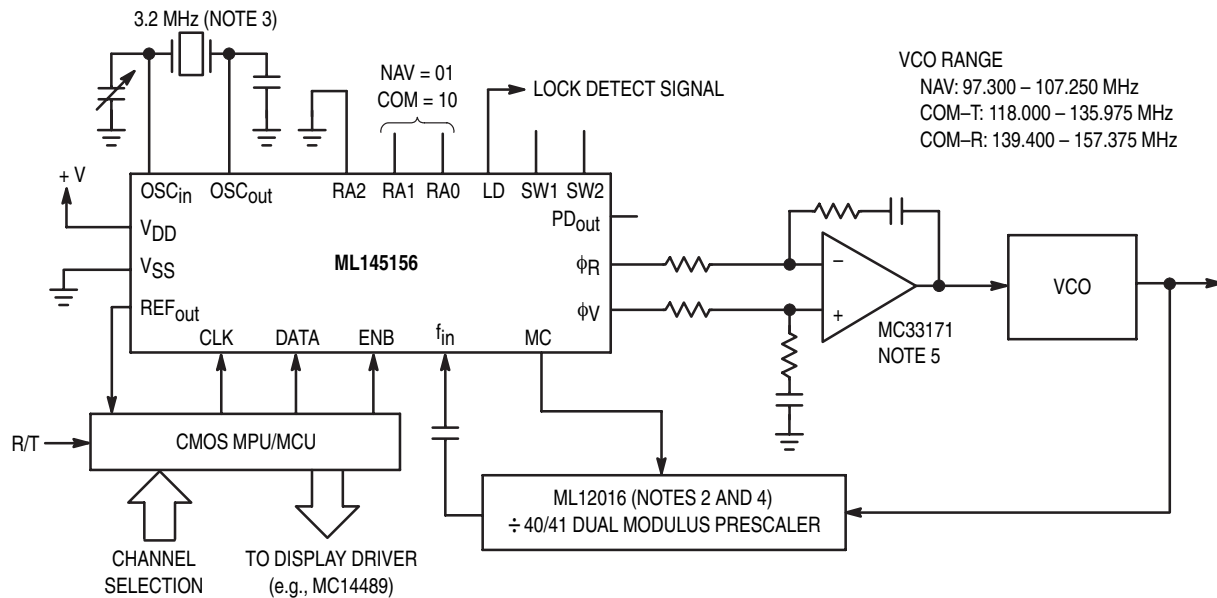


NOTES:
1. For NAV: $f_R$ = 50 kHz, $\div R$ = 64 using 10.7 MHz lowside injection, $N_{total}$ = 1946 – 2145.
   For COM–T: $f_R$ = 25 kHz, $\div R$ = 128, $N_{total}$ = 4720 – 5439.
   For COM–R: $f_R$ = 25 kHz, $\div R$ = 128, using 21.4 MHz highside injection, $N_{total}$ = 5576 – 6295.
2. A $\div 32/33$ dual modulus approach is provided by substituting an ML12015 for the ML12016. The devices are pin equivalent.
3. A 6.4 MHz oscillator crystal can be used by selecting $\div R$ = 128 (code 010) for NAV and $\div R$ = 256 (code 011) for COM.
4. ML12013 + MC10131 combination may also be used to form the $\div 40/41$ prescaler
5. The $\phi_R$ and $\phi_V$ outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop – Low–Pass Filter Design page for additional information. The $\phi_R$ and $\phi_V$ outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

**Figure 2. Avionics Navigation or Communication Synthesizer**

# LANSDALE
## Semiconductor, Inc.

# ML145157
# Serial–Input PLL
# Frequency Synthesizer
## Interfaces with Single–Modulus Prescalers

**Legacy Device:** *Motorola/Freescale MC145157-2*

The ML145157 has a fully programmable 14–bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

- Operating Temperature Range: $T_A$ = – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- $f_V$ and $f_R$ Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates

**P DIP 16 = EP**
PLASTIC DIP
CASE 648

16
1

**SOG 16 = -5P**
SOG PACKAGE
CASE 751G

16
1
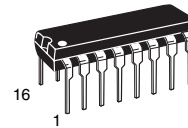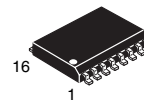
**CROSS REFERENCE/ORDERING INFORMATION**

| PACKAGE | MOTOROLA | LANSDALE |
|---------|----------|----------|
| P DIP 16 | MC145157P2 | ML145157EP |
| SOG 20W | MC145157DW2 | ML145157-5P |

**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

**PIN ASSIGNMENT**

| | | | | |
|---|---|---|---|---|
| $OSC_{in}$ | 1 | | 16 | $\phi R$ |
| $OSC_{out}$ | 2 | | 15 | $\phi V$ |
| $f_V$ | 3 | | 14 | $REF_{out}$ |
| $V_{DD}$ | 4 | | 13 | $f_R$ |
| $PD_{out}$ | 5 | | 12 | $S/R_{out}$ |
| $V_{SS}$ | 6 | | 11 | ENB |
| LD | 7 | | 10 | DATA |
| $f_{in}$ | 8 | | 9 | CLK |

**ML145157 BLOCK DIAGRAM**



## PIN DESCRIPTIONS

**INPUT PINS**

**fin**
**Frequency Input (Pin 8)**

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with AC coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), DC coupling may be used.

**CLK, DATA**
**Shift Clock, Serial Data Inputs (Pins 9, 10)**

Each low–to–high transition of the clock shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ N counter latch. The entry format is as follows:



FIRST DATA BIT INTO SHIFT REGISTER

**ENB**
**Latch Enable Input (Pin 11)**

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

**OSCin, OSCout**
**Reference Oscillator Input/Output (Pins 1, 2)**

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from $OSC_{in}$ to ground and $OSC_{out}$ to ground. $OSC_{in}$ may also serve as the input for an externally–generated reference signal. This signal is typically AC coupled to $OSC_{in}$, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to $OSC_{out}$.

**OUTPUT PINS**

**$PD_{out}$**
**Single–Ended Phase Detector A Output (Pin 5)**

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency fV > fR or fV Leading: Negative Pulses
Frequency fV < fR or fV Lagging: Positive Pulses
Frequency fV = fR and Phase Coincidence:
High–Impedance State

**φR, φV**
**Double–Ended Phase Detector B Outputs (Pins 16, 15)**

These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **$PD_{out}$**).

If frequency $f_V$ is greater than $f_R$ or if the phase of $f_V$ is leading, then error information is provided by $\phi_V$ pulsing low. $\phi_R$ remains essentially high.

If the frequency $f_V$ is less than $f_R$ or if the phase of $f_V$ is lagging, then error information is provided by $\phi_R$ pulsing low. $\phi_V$ remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both $\phi_V$ and $\phi_R$ remain high except for a small minimum time period when both pulse low in phase.

## $f_R$, $f_V$
### RCounter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and $f_{in}$ frequency outputs. The $f_R$ and $f_V$ outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

## LD
### Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked ($f_R$, $f_V$ of same phase and frequency), and pulses low when loop is out of lock.

## REF$_{out}$
### Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

## S/R$_{out}$
### Shift Register Output (Pin 12)

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

## POWER SUPPLY

## V$_{DD}$
### Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from +3 to +9 V with respect to V$_{SS}$.

## V$_{SS}$
### Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

# LANSDALE
## *Semiconductor, Inc.*

# ML145158
# Serial–Input PLL
# Frequency Synthesizer
## Interfaces with Dual–Modulus Prescalers

**Legacy Device:** *Motorola/Freescale MC145158-2*

The ML145158 has a fully programmable 14–bit reference counter, as well as fully programmable ÷ N and ÷ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

- Operating Temperature Range: $T_A = -40$ to $85°C$
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 1023
- Dual Modulus Capability; ÷ A Range = 0 to 127
- $f_V$ and $f_R$ Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates

**P DIP 16 = EP**
PLASTIC DIP
CASE 648

16
1

**SOG 16 = -5P**
SOG PACKAGE
CASE 751G

16
1
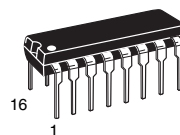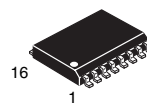
### CROSS REFERENCE/ORDERING INFORMATION

| PACKAGE | MOTOROLA | LANSDALE |
|---|---|---|
| P DIP 16 | MC145158P2 | ML145158EP |
| SOG 16 | MC145158DW2 | ML145158-5P |

**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

### PIN ASSIGNMENT

| | | | | |
|---|---|---|---|---|
| $OSC_{in}$ | 1 ● | | 16 | $\phi R$ |
| $OSC_{out}$ | 2 | | 15 | $\phi V$ |
| $f_V$ | 3 | | 14 | $REF_{out}$ |
| $V_{DD}$ | 4 | | 13 | $f_R$ |
| $PD_{out}$ | 5 | | 12 | MC |
| $V_{SS}$ | 6 | | 11 | ENB |
| LD | 7 | | 10 | DATA |
| $f_{in}$ | 8 | | 9 | CLK |

## ML145158  BLOCK DIAGRAM
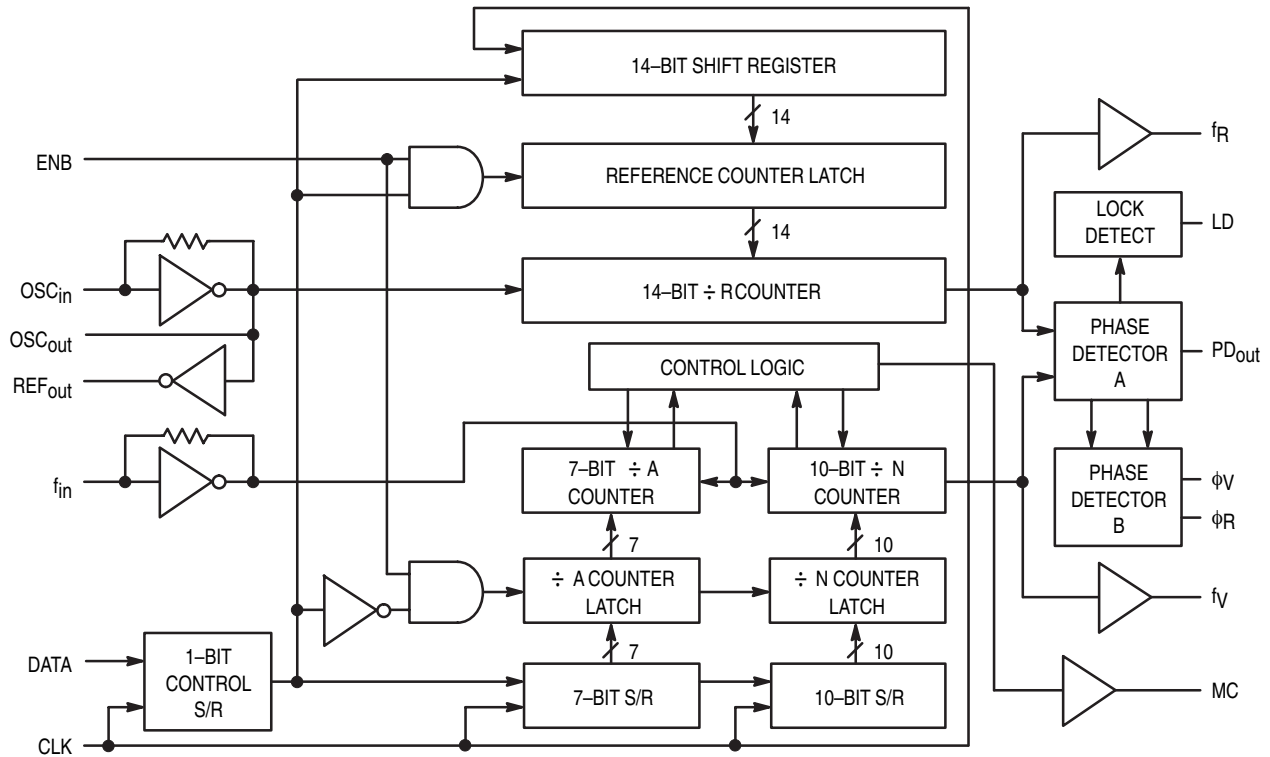


## PIN DESCRIPTIONS
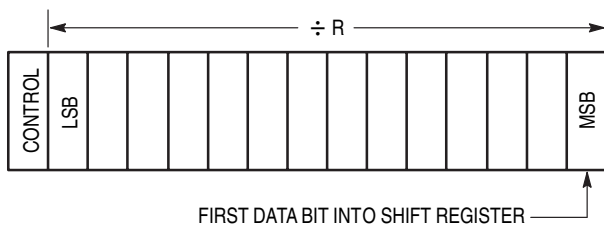
### INPUT PINS
### $f_{in}$ Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with AC coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), DC coupling may be used.

### CLK, DATA
### Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the CLK shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ A, ÷ N counter latch. The data entry format is as follows:
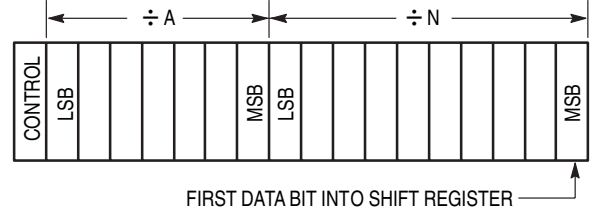


FIRST DATA BIT INTO SHIFT REGISTER



FIRST DATA BIT INTO SHIFT REGISTER

### ENB
### Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

### $OSC_{in}$, $OSC_{out}$
### Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from $OSC_{in}$ to ground and $OSC_{out}$ to ground. $OSC_{in}$ may also serve as the input for an externally–generated reference signal. This signal is typically AC coupled to $OSC_{in}$, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to $OSC_{out}$.

## OUTPUT PINS

### PD$_{out}$
### Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or $f_V$ Leading: Negative Pulses
Frequency $f_V < f_R$ or $f_V$ Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence:
      High–Impedance State

### $\phi$R, $\phi$V
### Phase Detector B Outputs (Pins 16, 15)

Double–ended phase detector outputs. These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD$_{out}$**).

If frequency $f_V$ is greater than $f_R$ or if the phase of $f_V$ is leading, then error information is provided by $\phi_V$ pulsing low. $\phi_R$ remains essentially high.

If the frequency $f_V$ is less than $f_R$ or if the phase of $f_V$ is lagging, then error information is provided by $\phi_R$ pulsing low. $\phi_V$ remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both $\phi_V$ and $\phi_R$ remain high except for a small minimum time period when both pulse low in phase.

### MC
### Dual–Modulus Prescaler Control Output (Pin 12)

This output generates a signal by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value $(N_T) = N \bullet P + A$ where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual–modulus version offers a distinct advantage. The dual–modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

### f$_R$, f$_V$
### R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and fin frequency outputs. The $f_R$ and $f_V$ outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

### LD
### Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked ($f_R$, $f_V$ of same phase and frequency), and pulses low when loop is out of lock.

### REF$_{out}$
### Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

## POWER SUPPLY

### V$_{DD}$
### Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to VSS.

### V$_{SS}$
### Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually-ground.

## ML14515X FAMILY CHARACTERISTICS AND DESCRIPTIONS - CONTINUED

**MAXIMUM RATINGS\*** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | $-0.5$ to $+10.0$ | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage (DC or Transient) except SW1, SW2 | $-0.5$ to $V_{DD} + 0.5$ | V |
| $V_{out}$ | Output Voltage (DC or Transient), SW1, SW2 ($R_{pull-up}$ = 4.7 k$\Omega$) | $-0.5$ to $+15$ | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient), per Pin | $\pm 10$ | mA |
| $I_{DD}$, $I_{SS}$ | Supply Current, $V_{DD}$ or $V_{SS}$ Pins | $\pm 30$ | mA |
| $P_D$ | Power Dissipation, per Package† | 500 | mW |
| $T_{stg}$ | Storage Temperature | $-65$ to $+150$ | C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 seconds | 260 | C |

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
†Power Dissipation Temperature Derating:
   Plastic DIP: $-12$ mW/ C from 65 to 85 C
   SOG Package: $-7$ mW/ C from 65 to 85 C

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS}$ ($V_{in}$ or $V_{out}$) $V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$), except for inputs with pull–up devices. Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Test Condition | $V_{DD}$ V | $-40$ C Min | $-40$ C Max | 25 C Min | 25 C Max | 85 C Min | 85 C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage Range | | $-$ | 3 | 9 | 3 | 9 | 3 | 9 | V |
| $I_{SS}$ | Dynamic Supply Current | $f_{in}$ = $OSC_{in}$ = 10 MHz, 1 V p–p AC coupled sine wave R = 128, A = 32, N = 128 | 3 5 9 | $-$ $-$ $-$ | 3.5 10 30 | $-$ $-$ $-$ | 3 7.5 24 | $-$ $-$ $-$ | 3 7.5 24 | mA |
| $I_{SS}$ | Quiescent Supply Current (not including pull–up current component) | $V_{in}$ = $V_{DD}$ or $V_{SS}$ $I_{out}$ = 0 $\mu$A | 3 5 9 | $-$ $-$ $-$ | 800 1200 1600 | $-$ $-$ $-$ | 800 1200 1600 | $-$ $-$ $-$ | 1600 2400 3200 | $\mu$A |
| $V_{in}$ | Input Voltage – $f_{in}$, $OSC_{in}$ | Input AC coupled sine wave | $-$ | 500 | $-$ | 500 | $-$ | 500 | $-$ | mV p–p |
| $V_{IL}$ | LowLevel Input V oltage – $f_{in}$, $OSC_{in}$ | $V_{out}$ 2.1 V Input DC $V_{out}$ 3.5 V coupled $V_{out}$ 6.3 V square wave | 3 5 9 | $-$ $-$ $-$ | 0 0 0 | $-$ $-$ $-$ | 0 0 0 | $-$ $-$ $-$ | 0 0 0 | V |
| $V_{IH}$ | High–Level Input Voltage – $f_{in}$, $OSC_{in}$ | $V_{out}$ 0.9 V Input DC $V_{out}$ 1.5 V coupled $V_{out}$ 2.7 V square wave | 3 5 9 | 3.0 5.0 9.0 | $-$ $-$ $-$ | 3.0 5.0 9.0 | $-$ $-$ $-$ | 3.0 5.0 9.0 | $-$ $-$ $-$ | V |
| $V_{IL}$ | Low–Level Input Voltage – except $f_{in}$, $OSC_{in}$ | | 3 5 9 | $-$ $-$ $-$ | 0.9 1.5 2.7 | $-$ $-$ $-$ | 0.9 1.5 2.7 | $-$ $-$ $-$ | 0.9 1.5 2.7 | V |
| $V_{IH}$ | High–Level Input Voltage – except $f_{in}$, $OSC_{in}$ | | 3 5 9 | 2.1 3.5 6.3 | $-$ $-$ $-$ | 2.1 3.5 6.3 | $-$ $-$ $-$ | 2.1 3.5 6.3 | $-$ $-$ $-$ | V |
| $I_{in}$ | Input Current ($f_{in}$, $OSC_{in}$) | $V_{in}$ = $V_{DD}$ or $V_{SS}$ | 9 | $\pm 2$ | $\pm 50$ | $\pm 2$ | $\pm 25$ | $\pm 2$ | $\pm 22$ | $\mu$A |
| $I_{IL}$ | Input Leakage Current (Data, CLK, ENB – without pull–ups) | $V_{in}$ = $V_{SS}$ | 9 | $-$ | $-0.3$ | $-$ | $-0.1$ | $-$ | $-1.0$ | $\mu$A |
| $I_{IH}$ | Input Leakage Current (all inputs except $f_{in}$, $OSC_{in}$) | $V_{in}$ = $V_{DD}$ | 9 | $-$ | 0.3 | $-$ | 0.1 | $-$ | 1.0 | $\mu$A |

(continued)

**DC ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Test Condition | $V_{DD}$ V | – 40 C Min | – 40 C Max | 25 C Min | 25 C Max | 85 C Min | 85 C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Pull–up Current (all inputs with pull–ups) | $V_{in} = V_{SS}$ | 9 | – 20 | – 400 | – 20 | – 200 | – 20 | – 170 | μA |
| $C_{in}$ | Input Capacitance | | – | – | 10 | – | 10 | – | 10 | pF |
| $V_{OL}$ | Low–Level Output Voltage – $OSC_{out}$ | $I_{out}$   0 μA $V_{in} = V_{DD}$ | 3 5 9 | – – – | 0.9 1.5 2.7 | – – – | 0.9 1.5 2.7 | – – – | 0.9 1.5 2.7 | V |
| $V_{OH}$ | High–Level Output Voltage – $OSC_{out}$ | $I_{out}$   0 μA $V_{in} = V_{SS}$ | 3 5 9 | 2.1 3.5 6.3 | – – – | 2.1 3.5 6.3 | – – – | 2.1 3.5 6.3 | – – – | V |
| $V_{OL}$ | Low–Level Output Voltage – Other Outputs | $I_{out}$   0 μA | 3 5 9 | – – – | 0.05 0.05 0.05 | – – – | 0.05 0.05 0.05 | – – – | 0.05 0.05 0.05 | V |
| $V_{OH}$ | High–Level Output Voltage – Other Outputs | $I_{out}$   0 μA | 3 5 9 | 2.95 4.95 8.95 | – – – | 2.95 4.95 8.95 | – – – | 2.95 4.95 8.95 | – – – | V |
| $V_{(BR)DSS}$ | Drain–to–Source Breakdown Voltage – SW1, SW2 | $R_{pull–up}$ = 4.7 kΩ | – | 15 | – | 15 | – | 15 | – | V |
| $I_{OL}$ | Low–Level Sinking Current – MC | $V_{out}$ = 0.3 V $V_{out}$ = 0.4 V $V_{out}$ = 0.5 V | 3 5 9 | 1.30 1.90 3.80 | – – – | 1.10 1.70 3.30 | – – – | 0.66 1.08 2.10 | – – – | mA |
| $I_{OH}$ | High–Level Sourcing Current – MC | $V_{out}$ = 2.7 V $V_{out}$ = 4.6 V $V_{out}$ = 8.5 V | 3 5 9 | – 0.60 – 0.90 – 1.50 | – – – | – 0.50 – 0.75 – 1.25 | – – – | – 0.30 – 0.50 – 0.80 | – – – | mA |
| $I_{OL}$ | Low–Level Sinking Current – LD | $V_{out}$ = 0.3 V $V_{out}$ = 0.4 V $V_{out}$ = 0.5 V | 3 5 9 | 0.25 0.64 1.30 | – – – | 0.20 0.51 1.00 | – – – | 0.15 0.36 0.70 | – – – | mA |
| $I_{OH}$ | High–Level Sourcing Current – LD | $V_{out}$ = 2.7 V $V_{out}$ = 4.6 V $V_{out}$ = 8.5 V | 3 5 9 | – 0.25 – 0.64 – 1.30 | – – – | – 0.20 – 0.51 – 1.00 | – – – | – 0.15 – 0.36 – 0.70 | – – – | mA |
| $I_{OL}$ | Low–Level Sinking Current – SW1, SW2 | $V_{out}$ = 0.3 V $V_{out}$ = 0.4 V $V_{out}$ = 0.5 V | 3 5 9 | 0.80 1.50 3.50 | – – – | 0.48 0.90 2.10 | – – – | 0.24 0.45 1.05 | – – – | mA |
| $I_{OL}$ | Low–Level Sinking Current – Other Outputs | $V_{out}$ = 0.3 V $V_{out}$ = 0.4 V $V_{out}$ = 0.5 V | 3 5 9 | 0.44 0.64 1.30 | – – – | 0.35 0.51 1.00 | – – – | 0.22 0.36 0.70 | – – – | mA |
| $I_{OH}$ | High–Level Sourcing Current – Other Outputs | $V_{out}$ = 2.7 V $V_{out}$ = 4.6 V $V_{out}$ = 8.5 V | 3 5 9 | – 0.44 – 0.64 – 1.30 | – – – | – 0.35 – 0.51 – 1.00 | – – – | – 0.22 – 0.36 – 0.70 | – – – | mA |
| $I_{OZ}$ | Output Leakage Current – $PD_{out}$ | $V_{out}$ = $V_{DD}$ or $V_{SS}$ Output in Off State | 9 | – | ± 0.3 | – | ± 0.1 | – | ± 1.0 | μA |
| $I_{OZ}$ | Output Leakage Current – SW1, SW2 | $V_{out}$ = $V_{DD}$ or $V_{SS}$ Output in Off State | 9 | – | ± 0.3 | – | ± 0.1 | – | ± 3.0 | μA |
| $C_{out}$ | Output Capacitance – $PD_{out}$ | $PD_{out}$ – Three–State | – | – | 10 | – | 10 | – | 10 | pF |

## AC ELECTRICAL CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r = t_f$ = 10 ns)

| Symbol | Parameter | $V_{DD}$ V | Guaranteed Limit 25°C | Guaranteed Limit – 40 to 85°C | Unit |
|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, $f_{in}$ to MC (Figures 1 and 4) | 3<br>5<br>9 | 110<br>60<br>35 | 120<br>70<br>40 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, ENB to SW1, SW2 (Figures 1 and 5) | 3<br>5<br>9 | 160<br>80<br>50 | 180<br>95<br>60 | ns |
| $t_W$ | Output Pulse Width, $\phi_R$, $\phi_V$, and LD with $f_R$ in Phase with $f_V$ (Figures 2 and 4) | 3<br>5<br>9 | 25 to 200<br>20 to 100<br>10 to 70 | 25 to 260<br>20 to 125<br>10 to 80 | ns |
| $t_{TLH}$ | Maximum Output Transition Time, MC (Figures 3 and 4) | 3<br>5<br>9 | 115<br>60<br>40 | 115<br>75<br>60 | ns |
| $t_{THL}$ | Maximum Output Transition Time, MC (Figures 3 and 4) | 3<br>5<br>9 | 60<br>34<br>30 | 70<br>45<br>38 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, LD (Figures 3 and 4) | 3<br>5<br>9 | 180<br>90<br>70 | 200<br>120<br>90 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Other Outputs (Figures 3 and 4) | 3<br>5<br>9 | 160<br>80<br>60 | 175<br>100<br>65 | ns |

## SWITCHING WAVEFORMS

**Figure 1.**

**Figure 2.**

* $f_R$ in phase with $f_V$.
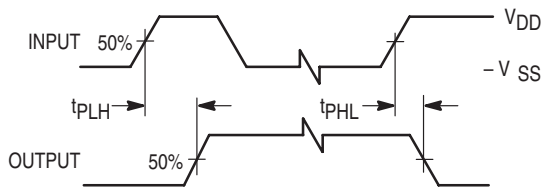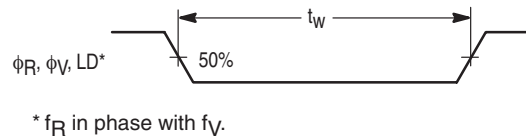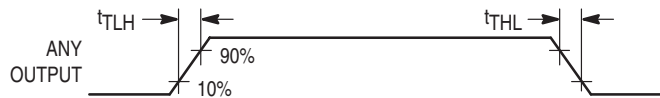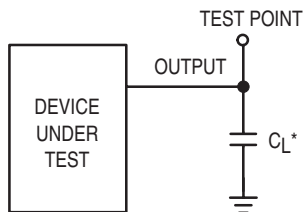
**Figure 3.**

* Includes all probe and fixture capacitance.

**Figure 4. Test Circuit**
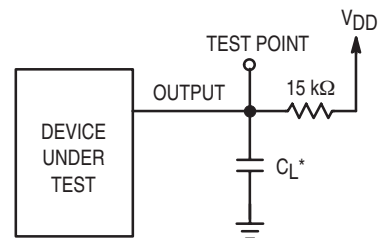
* Includes all probe and fixture capacitance.

**Figure 5. Test Circuit**

**TIMING REQUIREMENTS** (Input $t_r = t_f$ = 10 ns unless otherwise indicated)

| Symbol | Parameter | $V_{DD}$ V | Guaranteed Limit 25 C | Guaranteed Limit – 40 to 85 C | Unit |
|---|---|---|---|---|---|
| $f_{clk}$ | Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 6) | 3 5 9 | DC to 5.0 DC to 7.1 DC to 10 | DC to 3.5 DC to 7.1 DC to 10 | MHz |
| $t_{su}$ | Minimum Setup Time, Data to CLK (Figure 7) | 3 5 9 | 30 20 18 | 30 20 18 | ns |
| $t_h$ | Minimum Hold Time, CLK to Data (Figure 7) | 3 5 9 | 40 20 15 | 40 20 15 | ns |
| $t_{su}$ | Minimum Setup Time, CLK to ENB (Figure 7) | 3 5 9 | 70 32 25 | 70 32 25 | ns |
| $t_{rec}$ | Minimum Recovery Time, ENB to CLK (Figure 7) | 3 5 9 | 5 10 20 | 5 10 20 | ns |
| $t_{w(H)}$ | Minimum Pulse Width, CLK and ENB (Figure 6) | 3 5 9 | 50 35 25 | 70 35 25 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times – Any Input (Figure 8) | 3 5 9 | 5 4 2 | 5 4 2 | µs |

## SWITCHING WAVEFORMS
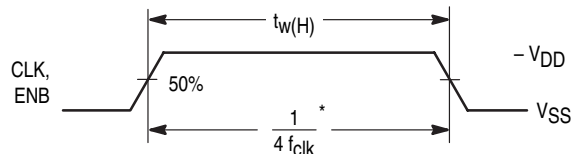


*Assumes 25% Duty Cycle.

**Figure 6.**
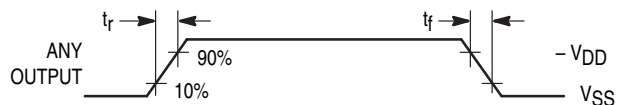


**Figure 8.**
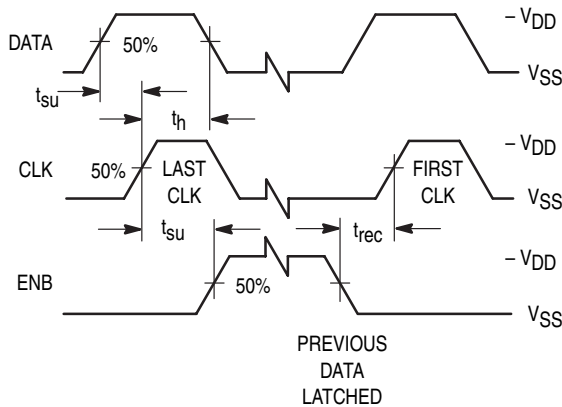


**Figure 7.**

**FREQUENCY CHARACTERISTICS** (Voltages References to $V_{SS}$, $C_L$ = 50 pF, Input $t_r$ = $t_f$ =10 ns unless otherwise indicated)

| Symbol | Parameter | Test Condition | $V_{DD}$ V | – 40 C | | 25 C | | 85 C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $f_i$ | Input Frequency ($f_{in}$, $OSC_{in}$) | R ≥ 8, A ≥ 0, N ≥ 8 $V_{in}$ = 500 mV p–p AC coupled sine wave | 3 5 9 | – – – | 6 15 15 | – – – | 6 15 15 | – – – | 6 15 15 | MHz |
| | | R ≥ 8, A ≥ 0, N ≥ 8 $V_{in}$ = 1 V p–p AC coupled sine wave | 3 5 9 | – – – | 12 22 25 | – – – | 12 20 22 | – – – | 7 20 22 | MHz |
| | | R ≥ 8, A ≥ 0, N ≥ 8 $V_{in}$ = $V_{DD}$ to $V_{SS}$ DC coupled square wave | 3 5 9 | – – – | 13 25 25 | – – – | 12 22 25 | – – – | 8 22 25 | MHz |

NOTE: Usually, the PLL's propagation delay from $f_{in}$ to MC plus the setup time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P / (t_P + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual modulus prescaler ratios, $t_P$ is the $f_{in}$ to MC propagation delay in seconds, and $t_{set}$ is the prescaler setup time in seconds.
For example, with a 5 V supply, the $f_{in}$ to MC delay is 70 ns. If the MC12028A prescaler is used, the setup time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P / (t_P + t_{set}) = 64/(70 + 16) = 744$ MHz.
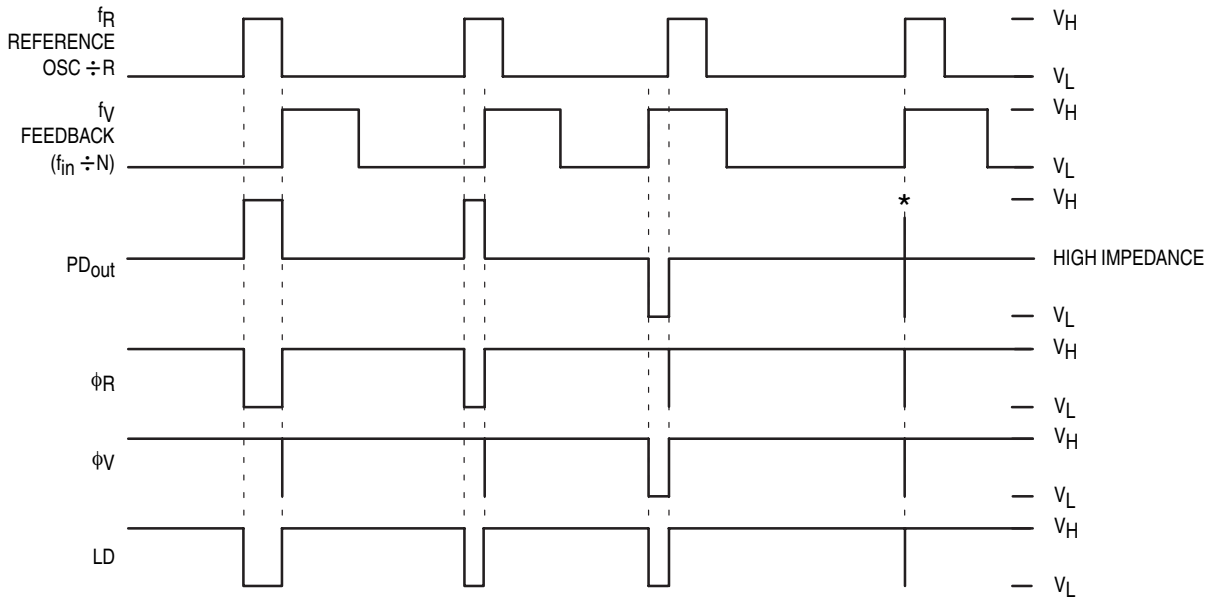


$V_H$  = High Voltage Level.
$V_L$  = Low Voltage Level.
* At this point, when both $f_R$ and $f_V$ are in phase, the output is forced to near mid–supply.
NOTE: The $PD_{out}$ generates error pulses during out–of–lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low–pass filter capacitor.

**Figure 9. Phase Detector/Lock Detector Output Waveforms**

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Issue A

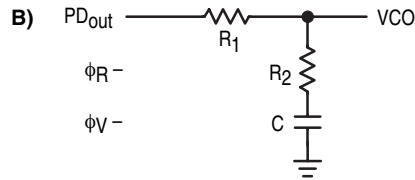## DESIGN CONSIDERATIONS

### PHASE–LOCKED LOOP – LOW–PASS FILTER DESIGN

**A)**
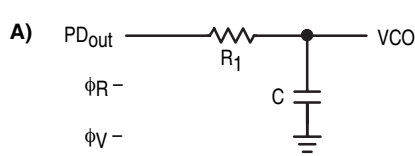


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1 C}}$$
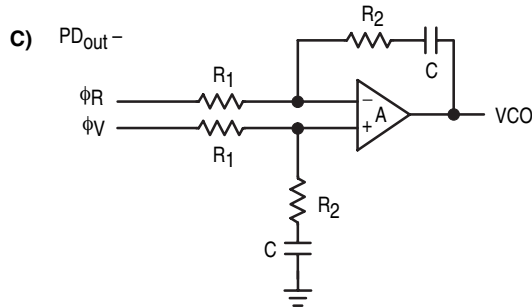
$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1 sC + 1}$$

**B)**



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5 \, \omega_n \left( R_2 C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2 sC + 1}{(R_1 + R_2)sC + 1}$$

**C)**



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE: Sometimes $R_1$ is split into two series resistors, each $R_1 \div 2$. A capacitor $C_C$ is then placed from the midpoint to ground to further filter $\phi_V$ and $\phi_R$. The value of $C_C$ should be such that the corner frequency of this network does not significantly affect $\omega_n$. The $\phi_R$ and $\phi_V$ outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in feedback loop

$K_\phi$ (Phase Detector Gain) = $V_{DD}/4\pi$ for $PD_{out}$

$K_\phi$ (Phase Detector Gain) = $V_{DD}/2\pi$ for $\phi_V$ and $\phi_R$

$K_{VCO}$ (VCO Gain) = $\dfrac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design $w_n$ (Natural Frequency) $\dfrac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design*. New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

## CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's or Lansdale's CMOS frequency synthesizers.

### Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or DC coupled to $OSC_{in}$. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail ($V_{DD}$ to $V_{SS}$) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or AC coupling to $OSC_{in}$ may be used. $OSC_{out}$, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the eem Electronic Engineers Master Catalog, the Gold Book, or similar publications.

### Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the ML12061 MECL device. The reference signal from the MECL device is AC coupled to $OSC_{in}$. For large amplitude signals (standard CMOS logic levels), DC coupling is used. $OSC_{out}$, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

### Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.
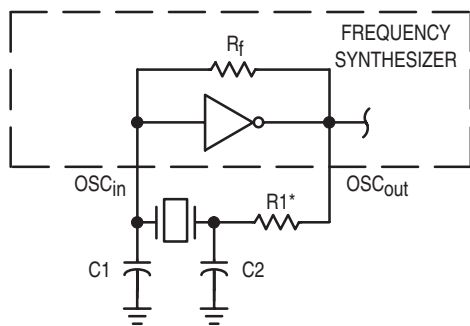


* May be deleted in certain cases. See text.

**Figure 10. Pierce Crystal Oscillator Circuit**

For $V_{DD}$ = 5.0 V, the crystal should be specified for a loading capacitance, $C_L$, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic $C_L$ values. The shunt load capacitance, $C_L$, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1 + C2}$$

where
$C_{in}$ = 5 pF (see Figure 11)
$C_{out}$ = 6 pF (see Figure 11)
$C_a$ = 1 pF (see Figure 11)
$C_O$ = the crystal's holder capacitance (see Figure 12)
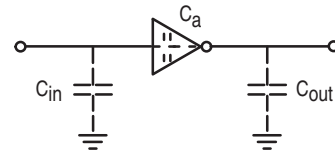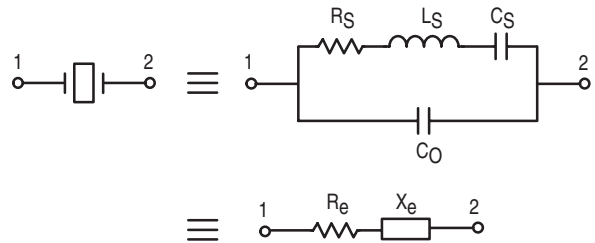C1 and C2 = external capacitors (see Figure 10)



**Figure 11. Parasitic Capacitances of the Amplifier**



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

**Figure 12. Equivalent Crystal Networks**

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the $OSC_{in}$ and $OSC_{out}$ pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for $C_{in}$ and $C_{out}$.

Power is dissipated in the effective series resistance of the crystal, Re, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum DC supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at $OSC_{out}$. (Care should be taken to minimize loading.) The frequency should increase very slightly as the DC supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

**Table 1. Partial List of Crystal Manufacturers**

| United States Crystal Corp. |
|---|
| Crystek Crystal |
| Statek Corp. |
| Fox Electronics |

NOTE: Lansdale and Motorola do not recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

## RECOMMENDED READING

Technical Note TN–24, Statek Corp.
Technical Note TN–7, Statek Corp.
E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2 Feb.,1969.
D. Kemper, L. Rosine, "Quartz Crystals for FrequencyControl", Electro–Technology, June, 1969.
P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

## DUAL–MODULUS PRESCALING

### OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible with out the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Lansdale's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus-prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷4 to ÷128/÷ 129 can be controlled by most Lansdale frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145152 (Motorola), ML145156, or ML145158 are:

| | | |
|---|---|---|
| ML12009 | ÷5/÷6 | 440 MHz |
| ML12011 | ÷8/÷9 | 500 MHz |
| ML12013 | ÷10/÷11 | 500 MHz |
| ML12015 | ÷32/÷33 | 225 MHz |
| ML12016 | ÷40/÷41 | 225 MHz |
| ML12017 | ÷64/÷65 | 225 MHz |
| ML12018 | ÷128/÷129 | 520 MHz |
| MC12028A | ÷32/33 or ÷64/65 | 1.1 GHz |
| MC12034 | ÷32/33 or ÷64/65 | 2.0 GHz |
| MC12038 | ÷127/128 or ÷255/256 | 1.1 GHz |
| ML12052 | ÷64/65 or ÷128/129 | 1.1 GHz |
| ML12054A | ÷64/65 or ÷128/129 | 2.0 GHz |

## DESIGN GUIDELINES

The system total divide value, N total ($N_T$) will be dictated by the application:
N is the number programmed into the ÷ N counter, A is the

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of $N_T$ values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for $N_T$. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint N ≥ A always applies. If $A_{max}$ = P – 1, then $N_{min}$ ≥ P – 1. Then $N_T$ min = (P – 1) P + A or (P – 1) P since A is free to assume the value of 0.

$$N_{T\,max} = N_{max} \cdot P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

For the maximum frequency into the prescaler ($f_{VCOmax}$), the value used for P must be large enough such that:
1. $f_{VCO}$max divided by P may not exceed the frequency capability of $f_{in}$ (input to the ÷ N and ÷ A counters).
2. The period of $f_{VCO}$ divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its MC signal.
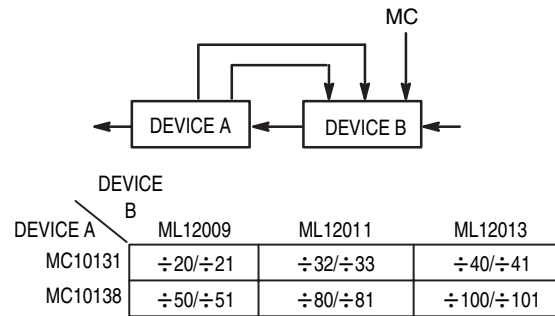   c. Propagation time from $f_{in}$ to the MC output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of $N_T$ results when $N_T$ in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷A counter contains "a" bits where $2^a$ ≥P.

2. Always program all higher order ÷A counter bits above "a" to 0.

3. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, $N_T$, now results when the value of $N_T$ in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable (shown in Figure 13).



| DEVICE A \ DEVICE B | ML12009 | ML12011 | ML12013 |
|---|---|---|---|
| MC10131 | ÷20/÷21 | ÷32/÷33 | ÷40/÷41 |
| MC10138 | ÷50/÷51 | ÷80/÷81 | ÷100/÷101 |

NOTE: ML12009, ML12011, and ML12013 are pin equivalent.
ML12015, ML12016, and ML12017 are pin equivalent.

**Figure 13. Dual–Modulus Values**

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## OUTLINE DIMENSIONS

**P DIP 16 = EP
PLASTIC DIP
CASE 648–08
(ML145157EP, ML145158EP)**
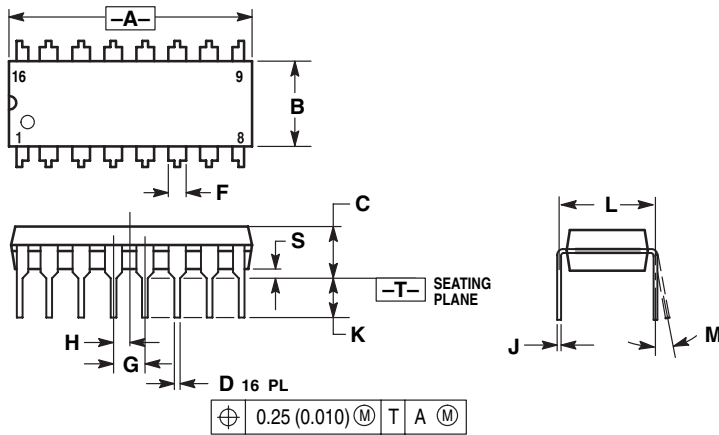


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

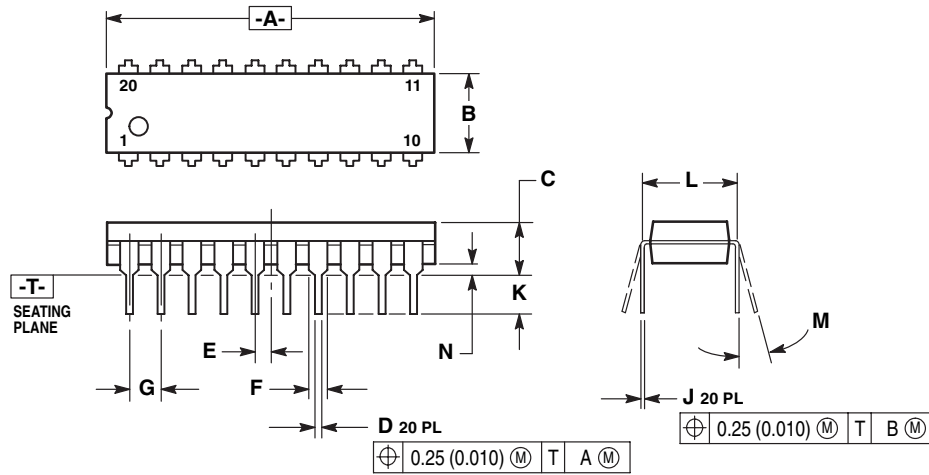| DIM | INCHES | | MILLIMETERS | |
| --- | --- | --- | --- | --- |
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

**P DIP 18 = VP
PLASTIC DIP
CASE 707–02
(ML145155VP)**
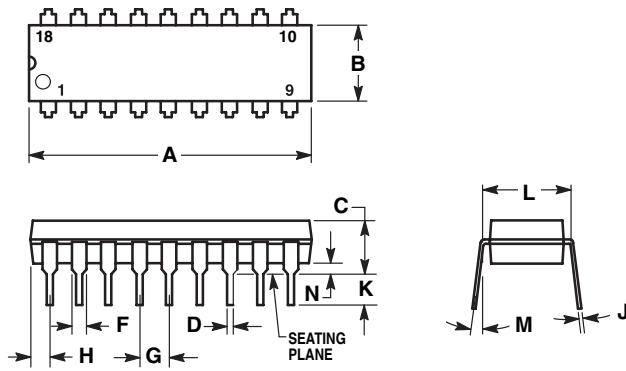


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | MILLIMETERS | | INCHES | |
| --- | --- | --- | --- | --- |
| | MIN | MAX | MIN | MAX |
| A | 22.22 | 23.24 | 0.875 | 0.915 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.56 | 4.57 | 0.140 | 0.180 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.27 | 1.78 | 0.050 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.02 | 1.52 | 0.040 | 0.060 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

# OUTLINE DIMENSIONS

**P DIP 20 = RP**
**PLASTIC DIP**
**CASE 738–03**
**(ML145156RP)**



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|-----|-----|-----|-----|-----|
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**SOG 20 = -6P**
**SOG PACKAGE**
**CASE 751D–04**
**(MC145155-6P, MC145156-6P)**
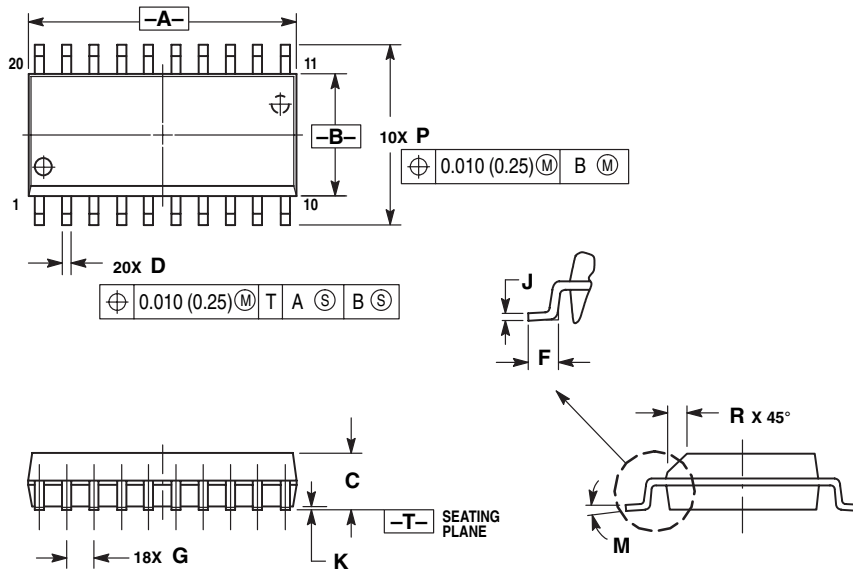


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|-----|-----|-----|-----|-----|
| A | 12.65 | 12.95 | 0.499 | 0.510 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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# OUTLINE DIMENSIONS

**P DIP 28 = YP**
**PLASTIC DIP**
**CASE 710–02**
**(ML145151YP, ML145152YP)**
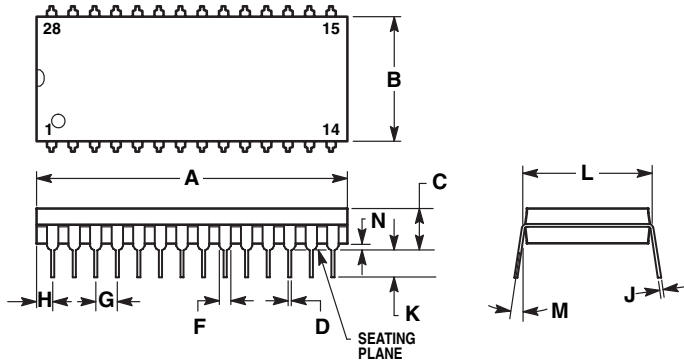
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 36.45 | 37.21 | 1.435 | 1.465 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

**SO 28W = -6P**
**SOG PACKAGE**
**CASE 751F–04**
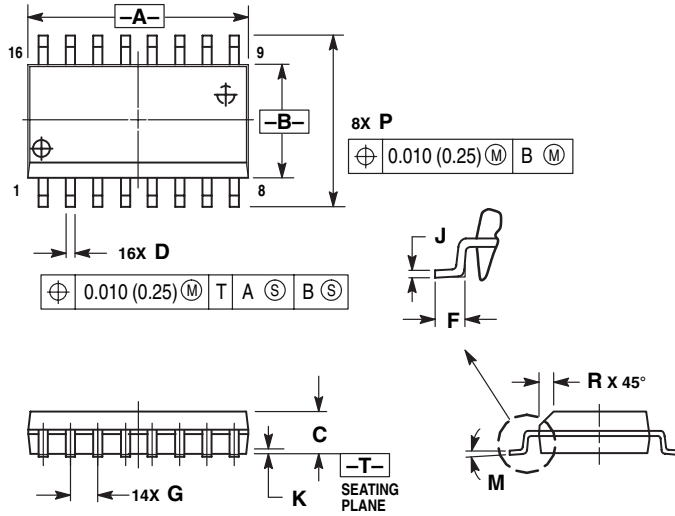**(ML145151-6P, ML145152–6P)**
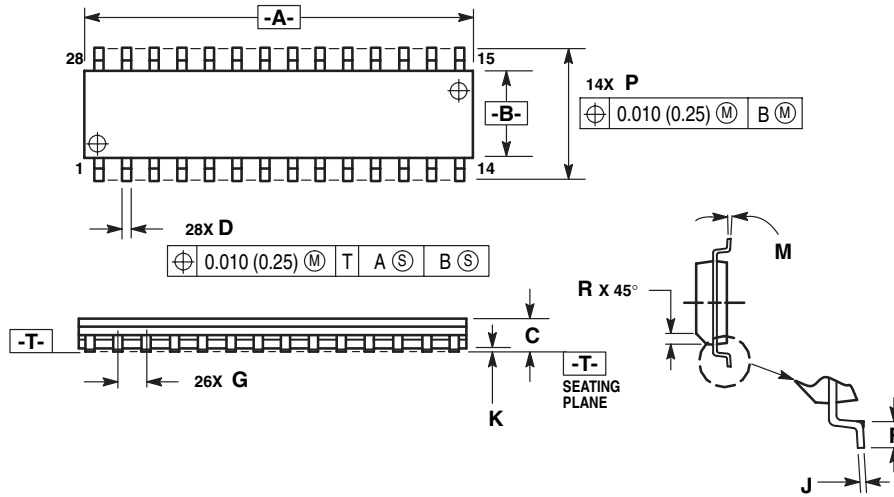
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 17.80 | 18.05 | 0.701 | 0.711 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.41 | 0.90 | 0.016 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.23 | 0.32 | 0.009 | 0.013 |
| K | 0.13 | 0.29 | 0.005 | 0.011 |
| M | 0° | 8° | 0° | 8° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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**OUTLINE DIMENSIONS**

**SOG 20 = -5P**
**SOG PACKAGE**
**CASE 751G–02**
**(ML145157-5P, ML145158-5P)**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|-------|-------|
|     | MIN  | MAX  | MIN   | MAX   |
| A   | 10.15 | 10.45 | 0.400 | 0.411 |
| B   | 7.40  | 7.60  | 0.292 | 0.299 |
| C   | 2.35  | 2.65  | 0.093 | 0.104 |
| D   | 0.35  | 0.49  | 0.014 | 0.019 |
| F   | 0.50  | 0.90  | 0.020 | 0.035 |
| G   | 1.27 BSC | | 0.050 BSC | |
| J   | 0.25  | 0.32  | 0.010 | 0.012 |
| K   | 0.10  | 0.25  | 0.004 | 0.009 |
| M   | 0°    | 7°    | 0°    | 7°    |
| P   | 10.05 | 10.55 | 0.395 | 0.415 |
| R   | 0.25  | 0.75  | 0.010 | 0.029 |

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