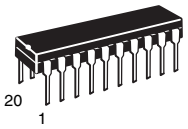
LANSDALE Semiconductor, Inc.

ML145428
Asynchronous–to–Synchronous and Synchronous–to–Asynchronous Converter

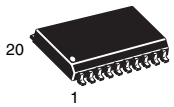
Legacy Device: *Motorola MC145428*

The ML145428 Data Set Interface provides asynchronous-to-synchronous and synchronous-to-asynchronous data conversion. It is ideally suited for voice/data digital telesets supplying an EIA-232 compatible data port into a synchronous transmission link. Other applications include: data multiplexers, concentrators, data-only switching, and PBX-based local area networks. This low-power CMOS device directly interfaces with either the 64 kbps or 8kbps channel of Motorola's MC145422 and MC145426 Universal Digital Loop Transceivers (UDLTs), as well as the MC145421 and MC145425 Second Generation Universal Digital Loop Transceivers (UDLT II).

- Provides the Interface Between Asynchronous Data Ports and Synchronous Transmission Lines
- Up to 128 kbps Asynchronous Data Rate Operation
- Up to 2.1 Mbps Synchronous Data Rate Operation
- On-Board Bit Rate Clock Generator with Pin Selectable Bit Rates of 300, 1200, 1400, 4800, 9600, 19200 and 38400 bps or an Externally Supplied 16 Times Bit Rate Clock
- Accepts Asynchronous Data Words of 8 or 9 Bits in Length
- False Start Detection Provided
- Automatic Sync Insertion and Checking
- Single 5 V Power Supply
- Low Power Consumption of 5 mW Typical
- Application Notes AN943 and AN946
- Operating Temperature Range T_A = –40° to +85°C.



P DIP 20 = RP
PLASTIC
CASE 732



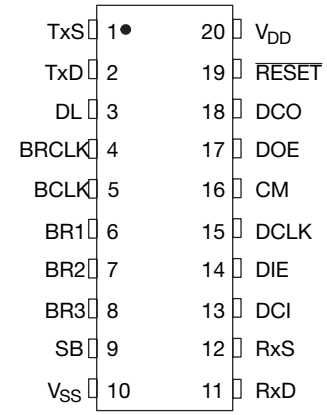
SOG 20 = -6P
PLASTIC
CASE 751D

CROSS REFERENCE/ORDERING INFORMATION

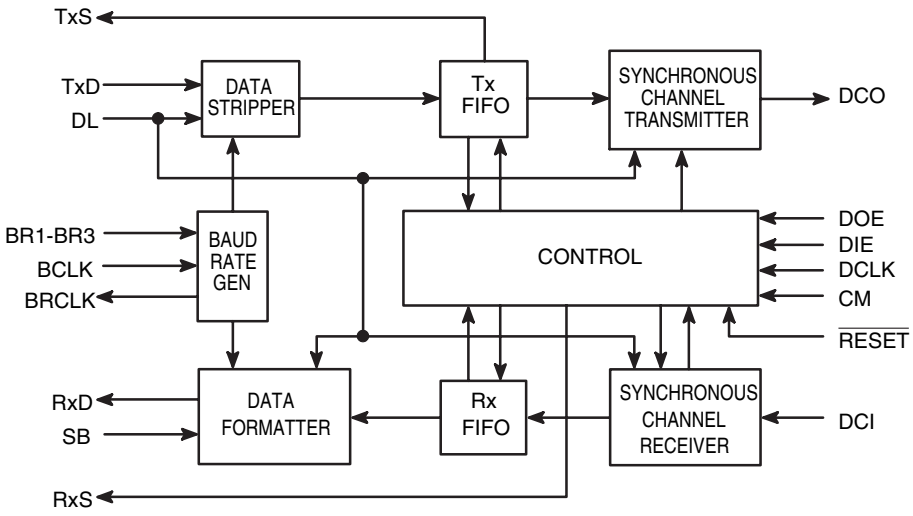
PACKAGE	MOTOROLA	LANSDALE
P DIP 20	MC145428P	ML145428RP
SOG 20	MC145428DW	ML145428-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} - V_{SS}	-0.5 to 6.0	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	+10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-85 to +150	°C

DIGITAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = 0 to 70°C)

Parameter	Symbol	V_{DD}	Min	Max	Unit
Input High Level	V_{IH}	5	3.5	—	V
Input Low Level	V_{IL}	5	—	1.5	V
Input Current	I_{in}	—	—	+1.0	μA
Input Capacitance	C_{in}	—	—	7.5	pF
Output High Current (Source) V_{OH} = 2.5 V V_{OH} = 4.6 V	I_{OH}	 5 5	 -1.7 -0.36	 — —	mA
Output Low Current V_{OL} = 0.4 V V_{OL} = 0.8 V	I_{OL}	 5 5	 0.36 0.8	 — —	mA
Operating Current (DC = 128 kHz, BC = 4.096 MHz)	I_{DD}	5	—	2.0	mA

SWITCHING CHARACTERISTICS (C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C)

Characteristic	Min	Typ	Max	Unit
Baud Clock Bit Rate Input Frequency (BR1, BR2, BR3) = (0,0,0) (BR1, BR2, BR3) = non-zero	 — —	 — —	 2.1 4.1	MHz
Baud Clock Pulse Width	100	—	—	ns
Data Clock Frequency	—	—	2.1	MHz
Data Clock Pulse Width	200	—	—	ns

ML145428 DSI PIN DESCRIPTIONS

V_{DD}. POSITIVE POWER SUPPLY

The most positive power supply pin, normally 5 volts.

V_{SS}. NEGATIVE POWER SUPPLY

The most negative supply pin, normally 0 volts.

TxD. TRANSMIT DATA INPUT

Input for asynchronous data, idle is logic high; break is 11 baud or more of logic low. One stop bit is required

RxD. RECEIVE DATA OUTPUT

Output for asynchronous data. The number of stop bits and the data word length are selected by teh SB and DL pins. Idle is logic high; break is a continuous logic low.

TxS. TRANSMIT STATUS OUTPUT

This pin will go low if the transmit FIFO holds 2 or more data words or if $\overline{\text{RESET}}$ is low.

RxS. RECEIVE STATUS OUTPUT

This pin will go low if framing of the synchronous channel is lost or not established or if $\overline{\text{RESET}}$ is low, or if the receive FIFO is overwritten.

SB, STOP BITS INPUT

This pin controls the number of stop bits the DATA FORMATTER will re–create when outputting data at the RxD asynchronous output. A high on this pin selects two stop bits; a low selects one stop bit.

DL, DATA LENGTH INPUT

This pin instructs the DSI to look for either 8 or 9 bits of data to be input at the TxD asynchronous input between the start and stop bits. The DL input also instructs the DSI's SYNCHRONOUS CHANNEL RECEIVER and SYNCHRONOUS CHANNEL TRANSMITTER to expecct 8 or 9 bit data words and also instructs the DSI's DATA FORMATTER to re–create 8 or 9 data bits between the start and stop bits when outputting data at its RxD asynchronous output. A high on this pin selects a 9 bit data word, a low selects an 8 bit data word length.

ML145428 DSI PIN DESCRIPTIONS – cont'd

BC, BAUD CLOCK INPUT

This pin serves as an input for an externally supplied 16 times data clock. Otherwise, the BC pin expects a 4.096 MHz clock signal which is internally divided to obtain the 16 times clock for the most frequentlly used standard bit rates (see BR1 - BR3 pin description).

BRCLD, 16 TIMES CLOCK INTERNAL OUTPUT

This pin outputs the internal 16 times asynchronous data rate clock.

BR1, BR2, BR3, BIT RATE SELECT INPUTS

These three pins select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the internally supplied bit rates. (See Table 1.)

DCO, DATA CHANNEL OUTPUT

This pin is a three–state output pin. Synchronous data is output when DOE is high. This pin will go high impedance when DOE or RESET are low. When CM is low, synchronous data is output on DCO on the falling edges of DC as long as DOE is high. When CM is high, synchronous data is output on DCO on the rising edges of DC, while DOE is held high. No more than eight data bits can be output during a given DOE high interval when CM = high. This feature allows the DSI to interface directly with the MC145422/26 Universal Digital Loop Transceivers (UDLT's) and PABX time division multiplexed highways.

DOE, DATA OUTPUT ENABLE INPUT

See DCO pin description and the SYNCHRONOUS CHANNEL INTERFACE section.

DIE, DATA INPUT ENABLE OUTPUT

See DCI and DCO pin descriptions and the SYNCHRONOUS CHANNEL INTERFACE section.

CM, CLOCK MODE INPUT

See the SYNCHRONOUS CHANNEL INTERFACE section and the SYNCHRONOUS CLOCKING MODE SUMMARY. (See Table 2.)

$\overline{\text{RESET}}$, RESET INPUT

When held low, this pin clears the internal FIFO's, forces the TxD asynchronous input to appear high to the DSI's internal circuitry, forces TxS and RxS low. When returned high, normal operation results.

When the $\overline{\text{RESET}}$ input is returned high the DSI's SYNCHRONOUS CHANNEL RECEIVER will not accept or transfer any incoming data words on the DCI pin to the Rx FIFO until one "flag" word is input at the DCI pin. (Also see RxS pin description)

DCI, DATA CHANNEL INPUT

Synchronous data is input on this pin on the falling edges of DC when DIE is high.

Table 1. Programmable Baud Rates

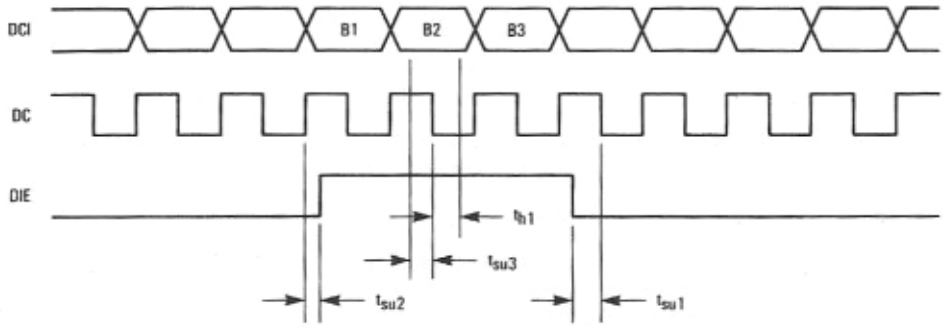
BR3	BR2	BR1	Bit Rate (bps)	BC in MHz	BRCLK
0	0	0	Variable 0 to 128 kbps	0 to 2.1 MHz	0 to 2.1 MHz
0	0	1	38.4 k	4.096	614.4 kHz
0	1	0	19.2 k	4.096	307.2 kHz
0	1	1	9600	4.096	153.6 kHz
1	0	0	4800	4.096	76.8 kHz
1	0	1	2400	4.096	38.4 kHz
1	1	0	1200	4.096	19.2 kHz
1	1	1	300	4.096	4.8 kHz

CM = LOW, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1A)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Fall Before DC Falls	t_{su1}	40	-9	—	ns	1
DIE Rise After Rise of DC	t_{su2}	40	+24	—	ns	2
DCI Data Stable Before DC Falling Edge	t_{su3}	40	-5	—	ns	3
DCI Data Stable After DC Falling Edge	t_{h1}	40	0	—	ns	4

NOTES:
1. Time DIE must fall before DC falls in order to avoid reading the bit after B3.
2. Time DC must be high before DIE rise in order to avoid clocking in the bit before B1. (See Synchronous Channel Interface for further details and see Figure 1A.)
3. Time data must be stable on the DCI pin before falling edge of the data clock DC.
4. Time data must be stable on the DCI pin after the falling edge of the data clock DC.



NOTE: When CM = 0, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL NAND of $\overline{DC}$ and DIE.
i.e. ↓ of $\overline{DC}$ ● DIE

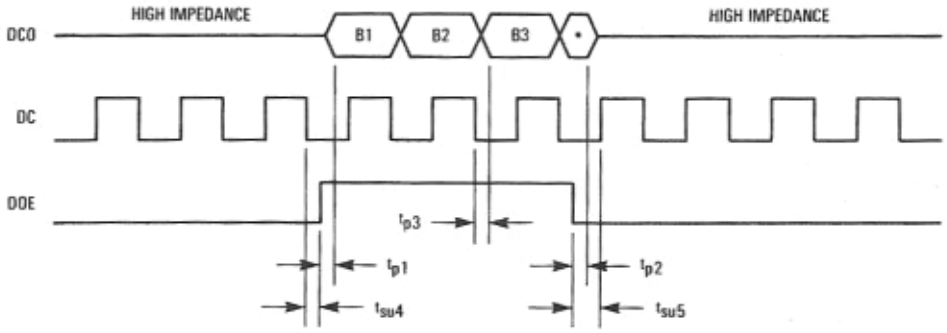
Figure 1A. CM = Low, Synchronous Channel Receiver Input Switching Characteristics

CM = LOW, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1B)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su4}	0	10	—	ns	5
DOE Falling to DC Rising	t_{su5}	40	-5	—	ns	6
DOE Rising to DCO Active	t_{p1}	50	28	—	ns	7
DOE Falling to High-Z of DCO	t_{p2}	50	26	—	ns	8
DC Falling to DCO	t_{p3}	80	71	—	ns	9

NOTES:
5. Time DC must be low before the rising edge of DOE in order to avoid clocking out a data bit before B1. (See Synchronous Channel Interface section for further details and also Figure 1B.)
6. Time DOE must be low before the rising edge of DC in order for the (*) bit to be output in the B1 position in the next cycle.
7. Propagation delay time from the rising edge of DOE to the low output impedance state of the DCO pin.
8. Propagation delay time from the falling edge of DOE to the high output impedance state of the DCO pin.
9. Propagation delay time from the falling edge data of the data clock DC to valid data on the DCO pin.



*This bit will be output in the B1 position on the next cycle of DOE.

NOTE: When CM = Low, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL NAND of DC and DOE. i.e. ↑ of DC ● DOE

Figure 1B. CM = Low, Synchronous Channel Transmitter Output Switching Characteristics

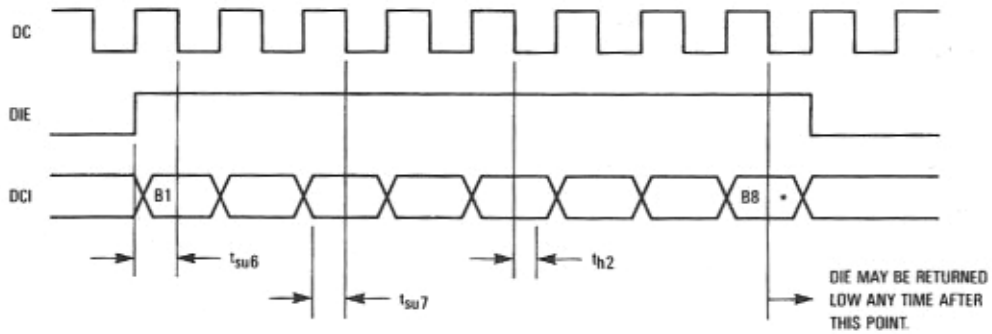
CM = HIGH, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1C)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Rising to DC Falling	t_{su6}	100	76	—	ns	10
DCI to DC Falling	t_{su7}	40	-4	—	ns	11
DC Falling to DCI	t_{h2}	20	0	—	ns	12

NOTES:

10. Time DIE must be high before the falling edge of DC in order for the data bit to be accepted by the synchronous data input of the DSI. (See Synchronous Channel Interface for further details.)
11. Time DCI data must be stable before the falling edge of the data clock DC.
12. Time DCI data must be stable after the falling edge of the data clock DC.



*Last bit accepted.

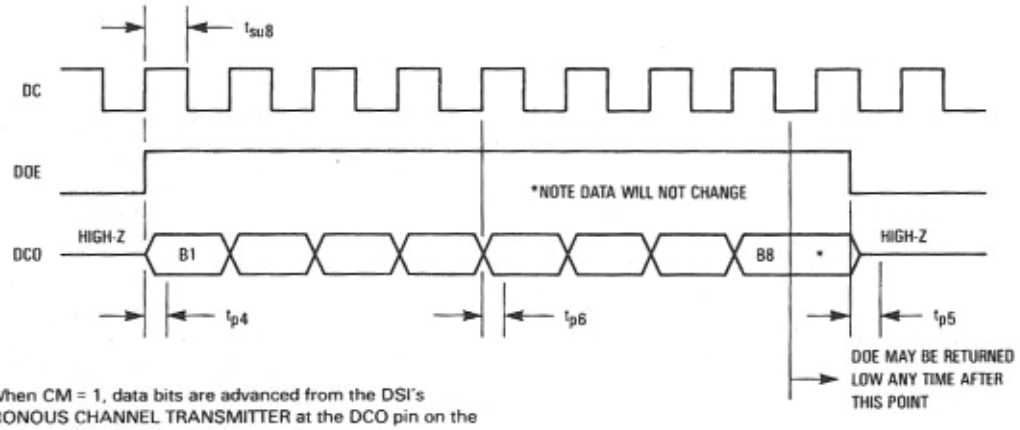
NOTE: When CM = 1, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL AND of DC and DIE. (DC ● DIE)

Figure 1C. CM = High, Synchronous Channel Receiver Input Switching Characteristics

CM = HIGH, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS
(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1D)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su8}	100	82	—	ns	13
DOE Rising to Active Data on DCO	t_{p4}	105	87	—	ns	14
DOE Falling to High-Z on DCO	t_{p5}	50	28	—	ns	15
DC Rising to DCO	t_{p6}	100	74	—	ns	16

NOTES:
13. Time DOE must be high before the falling edge of the data clock DC.
14. Time delay between the rise of the DOE pin and the time the DCO reaches the low impedance state.
15. Time delay between the fall of the DOE pin and the time the DCO pin reaches the high impedance state.
16. Delay from the rising edge of the data clock DC to the valid data on the DCO pin.



NOTE: When CM = 1, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL AND of DC and DOE. (DC ● DOE)

Figure 1D. CM = High, Synchronous Channel Transmitter Output Switching Characteristics

CIRCUIT DESCRIPTION

The ML145428 Data Set Interface provides a means for conversion of an asynchronous (start/stop format) data channel to a synchronous data channel and synchronous to asynchronous data channel conversion. Although primarily intended to facilitate the implementation of RS - 232 compatible asynchronous data ports in digital telephone sets using the MC145422/26 UDLTs, this device is also useful in many applications that require the conversion of synchronous and asynchronous data.

TRANSMIT CIRCUIT

Asynchronous data is input on the TxD pin. This data is expected to consist of a start bit (logic low) followed by eight or nine data bits and one or more stop bits (logic high). The length of the data word is selected by the DL pin. The data baud rate is selected with the BR1, BR1 and BR3 pins to obtain the internal sampling clock. This internal sampling clock is selected to be 16 times the baud rate at the TxD pin. An externally supplied 16 times clock may also be used, in which case the BR1, BR2, and BR3 pins should all be at logic zero and the 16 times sampling clock supplied at the BC pin.

Data input at the TxD pin is stripped of start and stop bits and is loaded into a four–word deep FIFO register. A break condition is also recognized at the TxD pin and this information is relayed to the synchronous channel transmitter which codes this condition so it may be re–created at the remote receiving device.

The synchronous channel transmitter sends one bit at a time under control of the DC, CM and DOE pins. The synchronous channel transmitter transmits one of three possible data patterns based on whether or not the top of the Tx FIFO is full and whether or not a break condition has been recognized by the data stripper. When no data is available at the top of the Tx FIFO for transmission, the synchronous data transmitter sends a special synchronizing flag pattern (011111110). When a break condition is detected by the data stripper and no data is available at the top of the Tx FIFO, the break pattern (111111110) is sent. Figure 2A depicts this operation.

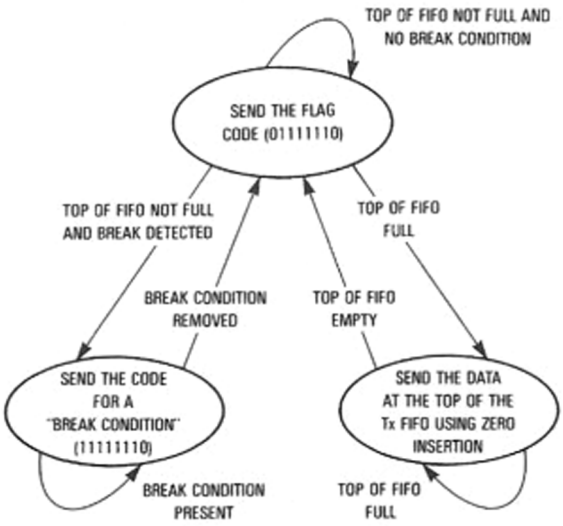


Figure 2A. Synchronous Data Channel Transmitter Operation

When stripped data words reach the top of the Tx FIFO they are loaded into the SYNCHRONOUS CHANNEL TRANSMITTER and are sent using a special zero insertion technique. When stripped data is being transmitted, the synchronous data transmitter will insert a binary 0 after any succession of five continuous 1's of data. Therefore, using this technique, no pattern of (01111110) or (11111110) can occur while sending data. This also allows the DSI to synchronize itself to the incoming synchronous data word boundaries based on the data alone.

The receive section of the DSI (synchronous channel receiver) performs the reverse operation by removing a binary 0 that follows five continuous 1's in order to recover the transmitted data. (note that a binary 1 which follows five continuous 1's is not removed so that flags and breaks may be detected.) Figure 2B shows an example of this process.

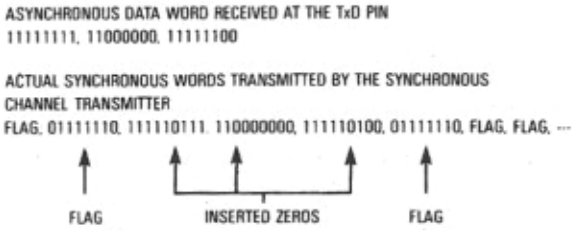


Figure 2B. Data Format Protocol

If the incoming data rate at TxD exceeds the rate at which it is output at DCO, the FIFO will fill. The TxS pin will go low when the FIFO contains two or more words. TxS may, therefore, be used as a local Clear-to-Send control line at the asynchronous interface port to avoid transmit data over-runs.

In order to insure synchronization during the transfer of a continuous stream of data the DSI's synchronous channel transmitter will insert a flag synchronnizing word (01111110) every 61st data word. The DSI's synchronous channel receiver checks for this synchronizing word and if not present, the loss of synchronizaion will be indicated by the RxS pin being latched low until the flag synchronizing word is received. Note that under these conditions the data will continue to output at RxD.

RECEIVE CIRCUIT

Data incoming from the synchronous channel is loaded into the ML145428 at the DCI pin under the control of the DC and DIE pins (see SYNCHRONOUS CHANNEL INTERFACE section). Framing information, break code detection, and data word recovery functions are performed by the SYNCHRONOUS CHANNEL RECEIVER. Recovered data words are loaded into the four word deep Rx FIFO. When the recovered data words reach the top of the Rx FIFO they are taken by the DATA FORMATTER, start and stop bits are re-inserted and the re-constructed asynchronous data is output at the TxD pin at the same baud rate as the transmit side. The number of stop bits and word length are those selected by the SB and DL pins.

Loss of framing, if it occurs, is indicated by the RxS pin going low. Data will continue to be output under these conditions, but RxS will remain low until frame synchronization, i.e., the detection of a framing flag word, is re-established. If the output data rate is less than the data rate of the incoming synchronous data channel, data will be lost at the rate of one word at a time due to the bottom word on the Rx FIFO being overwritten. In order to prevent data loss (in the form of asynchronous terminal to asynchronous terminal over-runs) due to clock slip between remote DSI links, (during long bursts the stop bit which it re-creates at its RxD output by 1/32nd. This action allows the originator of a transmission (of asynchronous data) to be up to 3% faster than the receive device is expecting for any given data rate. This tolerance is well with in the normally expected differences in clock frequencies between remote stations. If the Rx FIFO is overwriting the RxS line will pulse low for one DC clock period following the overwriting of the bottom level of the Rx FIFO.

INITIALIZATION

Initialization is accomplished by use of the RESET pin. When held low, the internal FIFOs are cleared, the TxD input appears high to the data strippers, internal circuitry. DCO is forced to a high impedance state, TxS and RxS are forced low. When brought high normal operation resumes and and the synchronous channel transmitter sends the flag code until data has reached the top of the Tx FIFO. Note that the TxS line will immediately go high after RESET goes high, while RxS will remain low until framing is detected. The synchronous channel

receiver section of the DSI is forced into a "HOLD" state while the RESET line is low. The synchronous channel receiver remains in the "HOLD" state after RESET goes high until a flag code word (01111110) is received at the DCI pin. While in the "HOLD" state no data words can be transferred to the Rx FIFO and, therefore, the DATA FORMATTER and RxD line are hold in the MARK idle state. After receiving the flag code pattern the RxS line goes high and normal operation proceeds. RESET should be held low when power is first applied to the DSI. RESET may be tied high permanently, if a short period of undefined operation at initial power application can be tolerated.

SYNCHRONOUS CHANNEL INTERFACE

The synchronous channel interface is generally operated in one of three basic modes of operation. The first is a continuous mode. A new data bit is clocked out of the DCO pin on each successive falling edge of the DC clock, and a new data bit is accepted by the DSI at its DCI pin on each successive falling edge of the DC clock. In this mode of operation, the CM control line is always low and the DOE and DIE enable control lines are always High. This is the typical setup when interfacing the DSI to the 8 kbps signal bit inputs and outputs of the MC145422/26 UDLTs (See Figures 3A and 4)

The second synchronous clocking mode is one in which 8 bits at a time are clocked out at the SYNCHRONOUS CHANNEL TRANSMITTER, and 8 bits are read by the SYNCHRONOUS CHANNEL RECEIVER at a time. The transferring of these 8 bit groups of data would normally be repeated on some cyclic basis. An example is a time division multiplexed data highway. In this mode (Cm = 1), the rising edge of the enable signal DIE and DOE should be roughly aligned to the rising edge of the DC clock signal. When enabled, the data is clocked out on the rising edge of the DC clock through the DCO pin and clocked in on the falling edge of the DC clock through the DCI pin. A variation of this clocking mode is to transfer less than 8 bits of data into or out of the DSI on a cyclic basis. If less than eight bits are to be transmitted and received, enable pins DIE and DOE should be returned low while the DC clock is low. This is illustrated in Figure 3D where five bits are being locked out of the DSI through the DCO pin and four bits are being input to the DSI through the DCI pin.

This restriction does not apply if eight bits are to be clocked into or out of the synchronous channels of the DSI, i.e., the DSI has internal circuitry to prevent more than eight clocks following the rising edge of the respective enable signal(s). Figure 3B illustrates a timing diagram depicting an eight bit data format. If the DOE enable is held high beyond the eight clock periods the last data bit B8 will remain at the output of the DCO pin until the DOE enable is brought low to reinitialize the sequence. Similarly the DSI's SYNCHRONOUS CHANNEL RECEIVER will read (at its DCI input) a minimum of eight data bits for any given DIE high period.

The CM = high mode, using 8 bits of data, is the typical set up for interfacing the DSI to the 64 kbps channel of the MC145422 or MC145426 Universal Digital Loop Transceivers. (See Figure 3B and Figure 5).

In the third mode of operation, an unlimited variable number of data bits may be clocked into or out of the synchronous side of the DSI at a time. When the CM line is low, any number of data bits may be clocked into or out of the DSI's synchronous channels provided that the respective enable signal is high. Figure 3C illustrates three data bits being clocked out of the DCO pin and three data bits being clocked into the DCI pin.

In the CM = low mode of operation, an internal clock is formed, which is the logical NAND of DC, DOE and CM, (IDC•DOE•CM). It is on the rising edge of this signal that a new data bit is clocked out of the DCO pin. Therefore, the DOE signal should be raised and lowered following the falling edge of the DC clock (i.e., when the DC clock is low).

Also in the CM = low mode of operation another internal clock is formed which is the logical NAND of DC, DIE, and CM (DC•DIE•CM). It is on the falling edge of this signal that a new bit is clocked into the DCI pin. Therefore the DIE signal should be raised or lowered following the rising edge of the DC clock (i.e., when the DC clock is high).

The following table summarizes when data bits are advanced from the synchronous channel transmitter and when data bits are read by the synchronous channel receiver dependent on the CM control line. (Shown below in Table 2.)

Table 2. Synchronous Clocking Mode Summary

Mode	Bits Advanced From The Synchronous Channel Transmitter On;	Bits Read By The Synchronous Channel Receiver On:
CM = 0	The rising edge of an internal clock formed by the logical NAND of DOE and DC. i.e ↑ of $\overline{DOE \bullet DC}$	The falling edge of an internal clock formed by the logical NAND of DIE and $\overline{DC}$. i.e. ↓ of $\overline{DIE \bullet \overline{DC}}$
CM = 1	The rising edge of an internal clock formed by the logical AND of DOE and DC. i.e. ↑ of DOE • DC	The falling edge of an internal clock formed by the logical AND of DIE and DC. i.e. ↓ of DIE • DC

TIMING DIAGRAMS

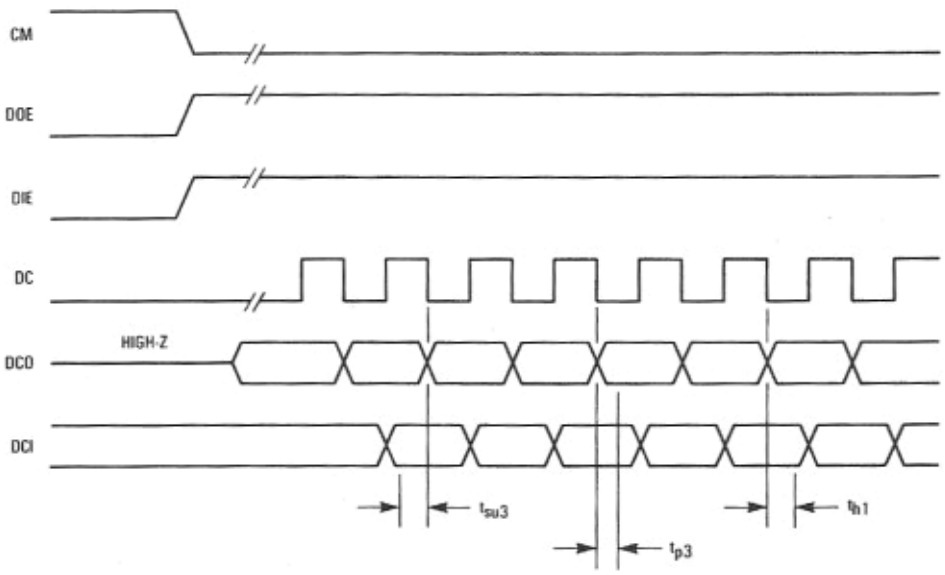


Figure 3A. Synchronous I/O, Continuous Bit Rate, Clock Mode Low

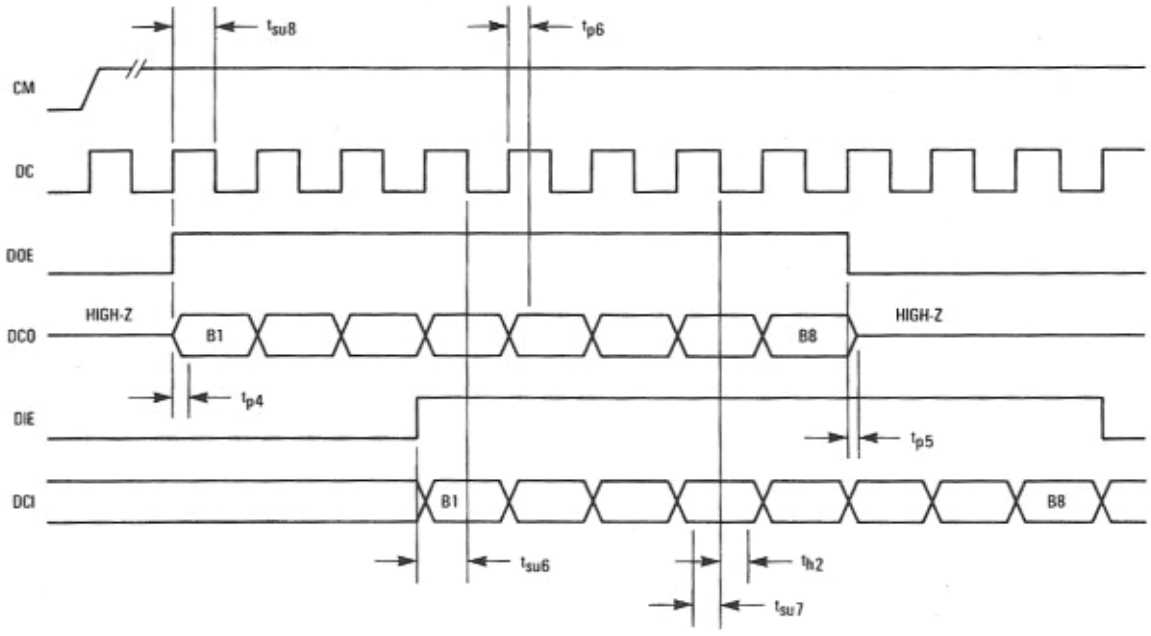


Figure 3B. Synchronous I/O, Eight Bit, Clock Mode High

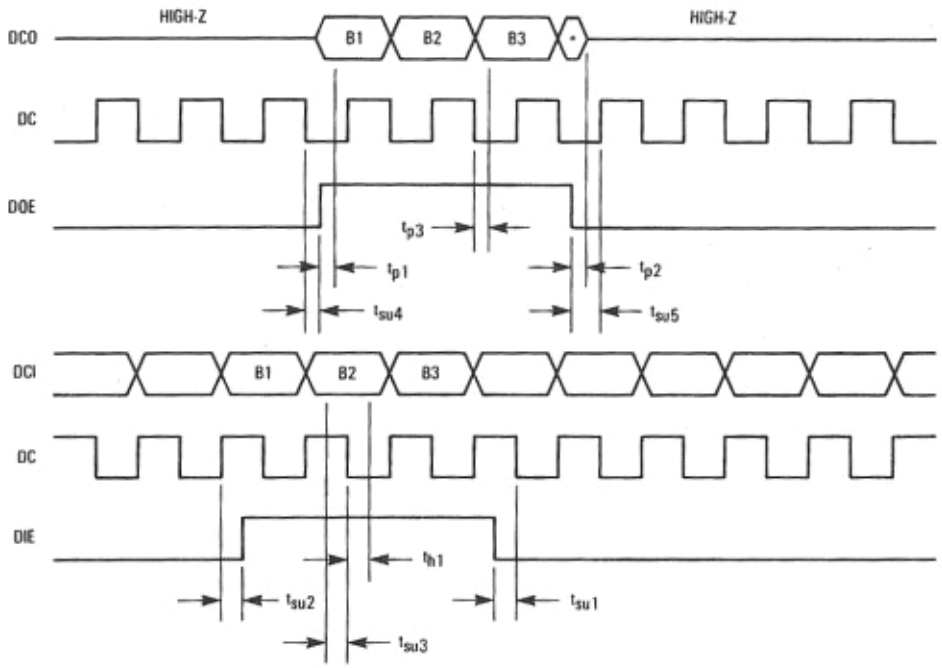


Figure 3C. Synchronous I/O, Variable Bit Length, Clock Mode Low

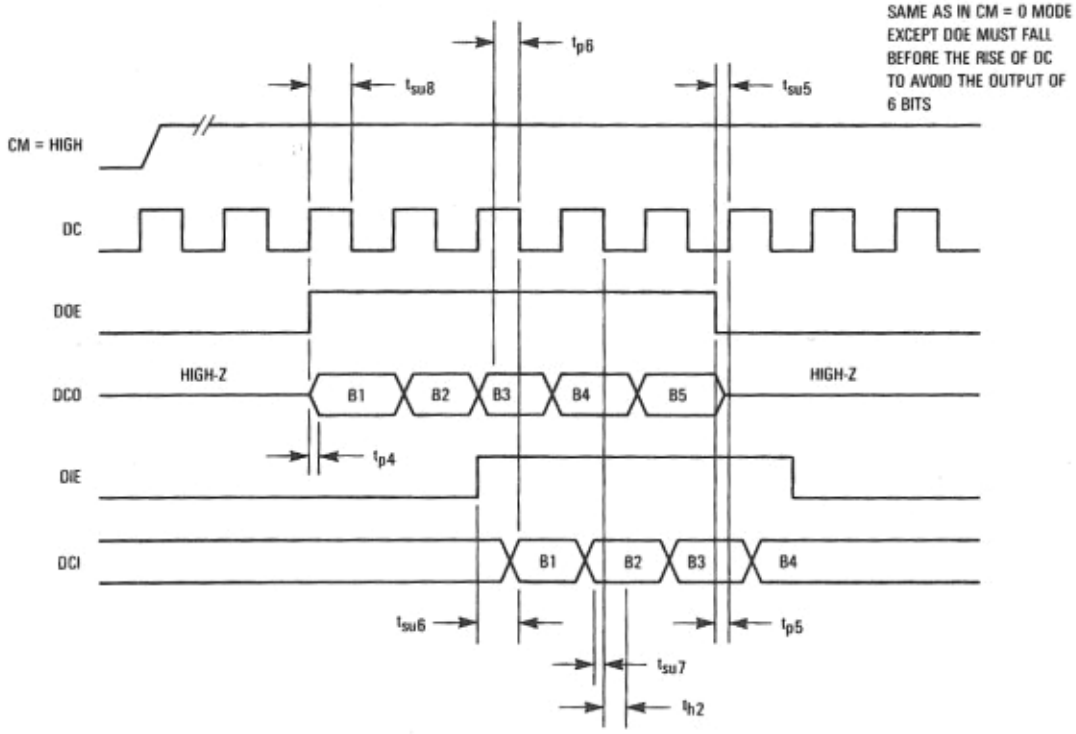
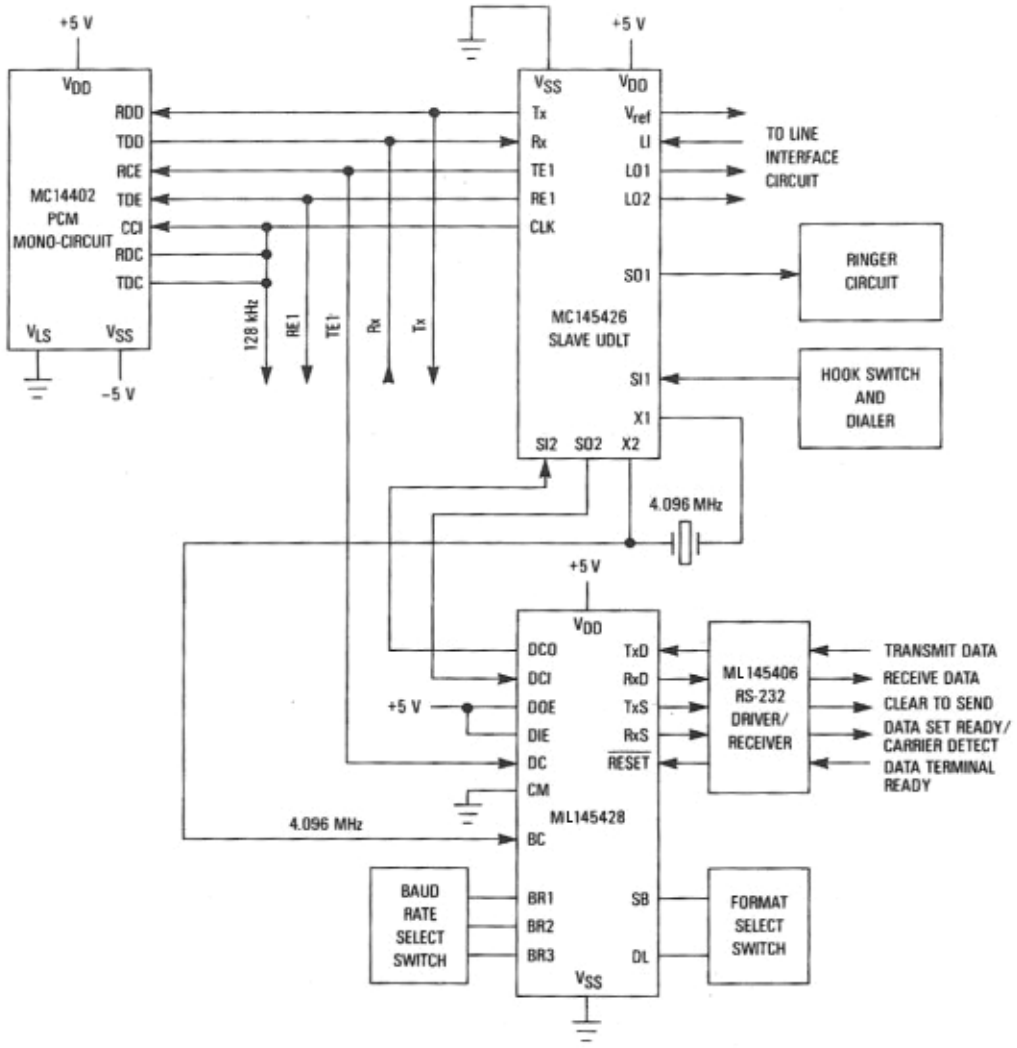
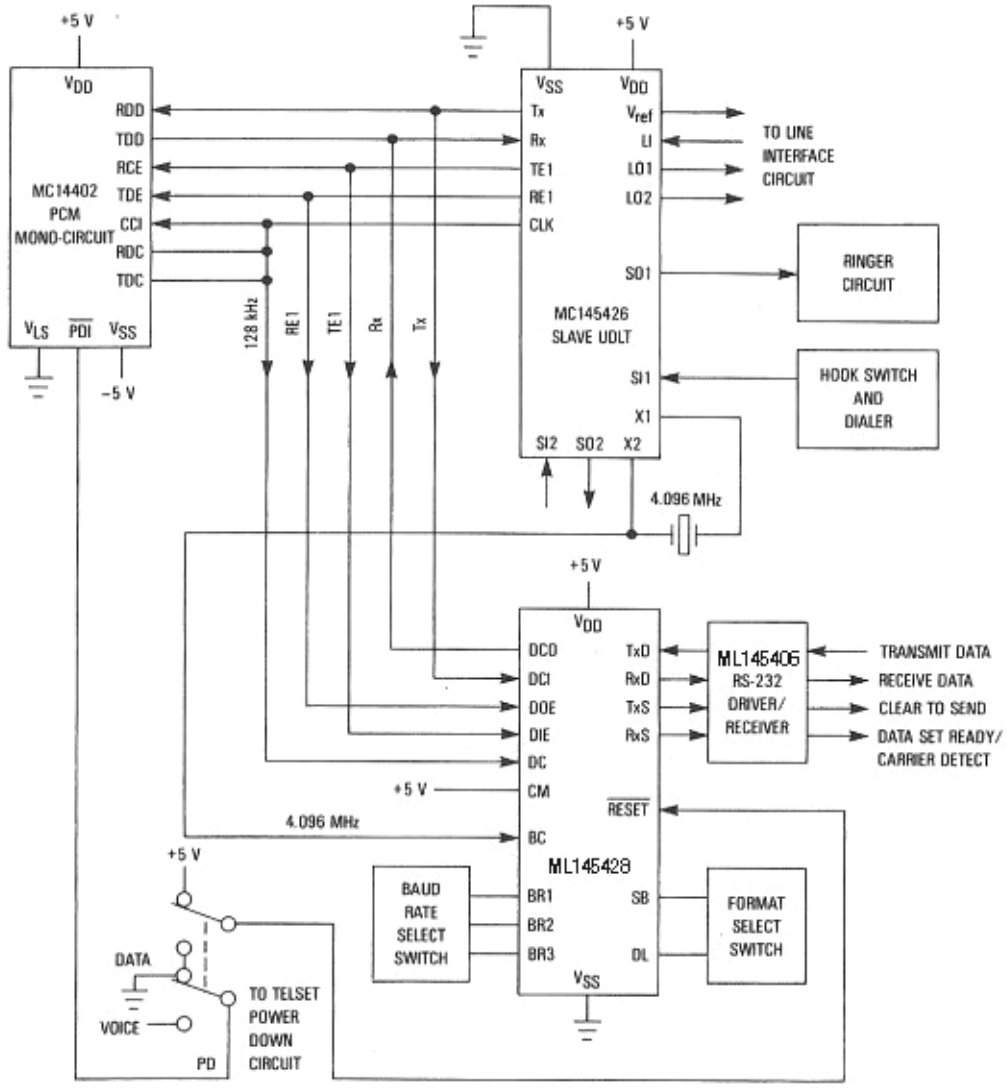


Figure 3D. Synchronous I/O, Variable Bit Length, Clock Mode High



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 4. Digital Telset RS-232 Port Using 8 Kilobits/Second Channel of ML145426



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 5. Digital Telset RS-232 Port Using 64 Kilobits/Second Channel of MC145426 for Voice or Data

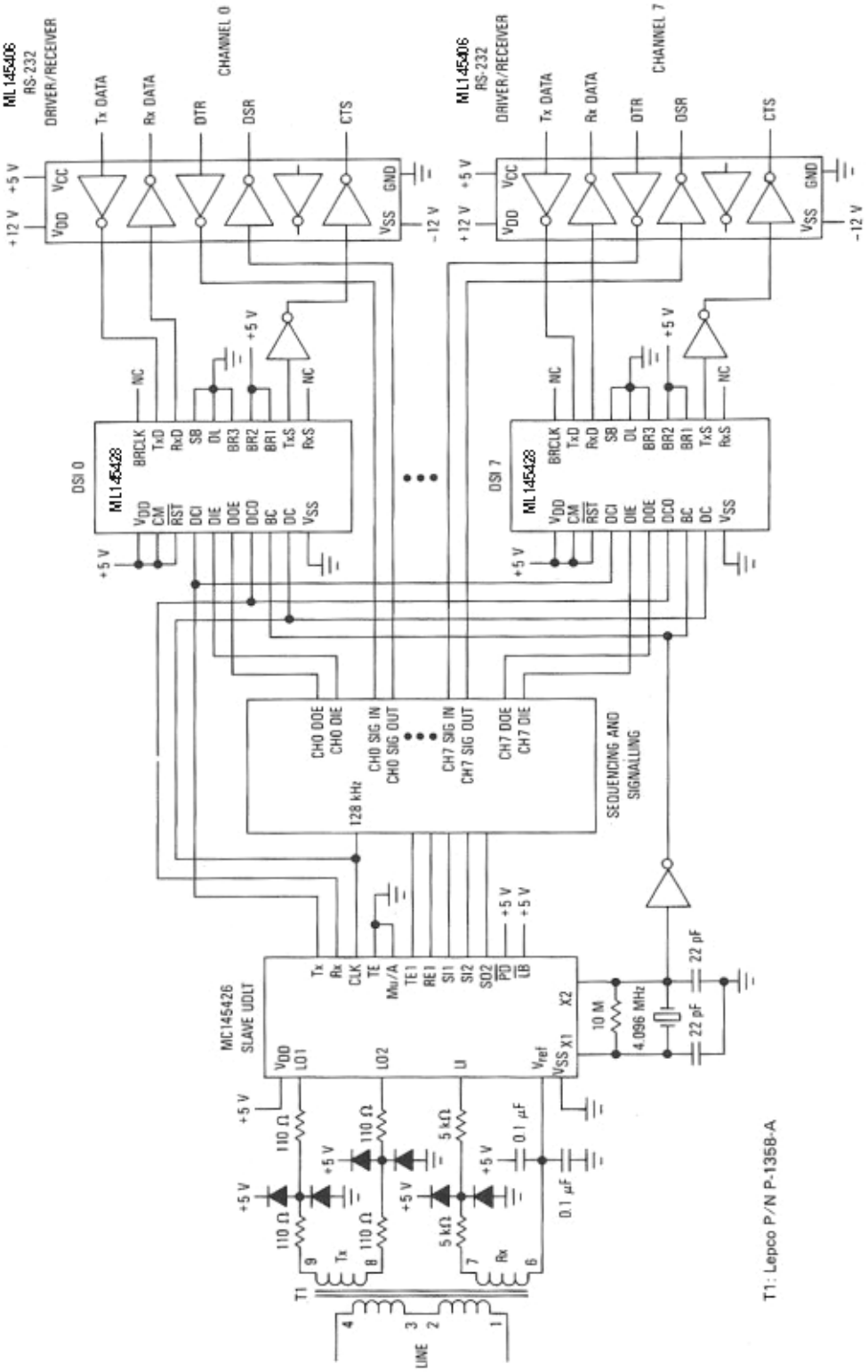
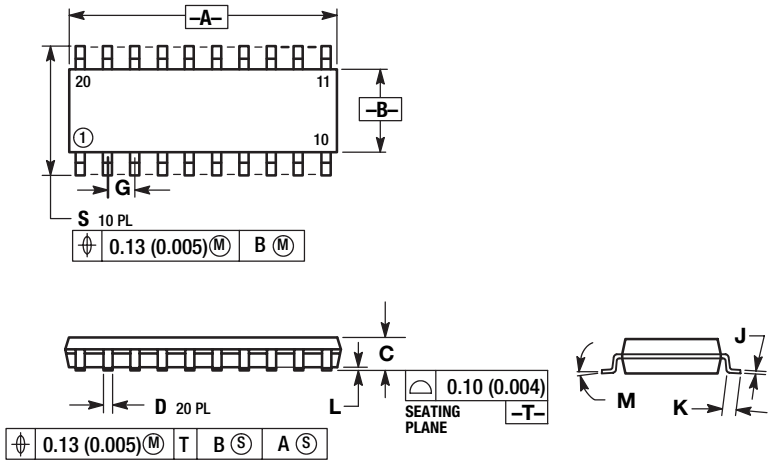


Figure 6. Multiplexing Eight RS-232 Telset Ports Into 64 Kilobits/Second Channel of MC145426

OUTLINE DIMENSIONS

SO 20 = -6P
(ML145428-6P)
CASE 751J-01

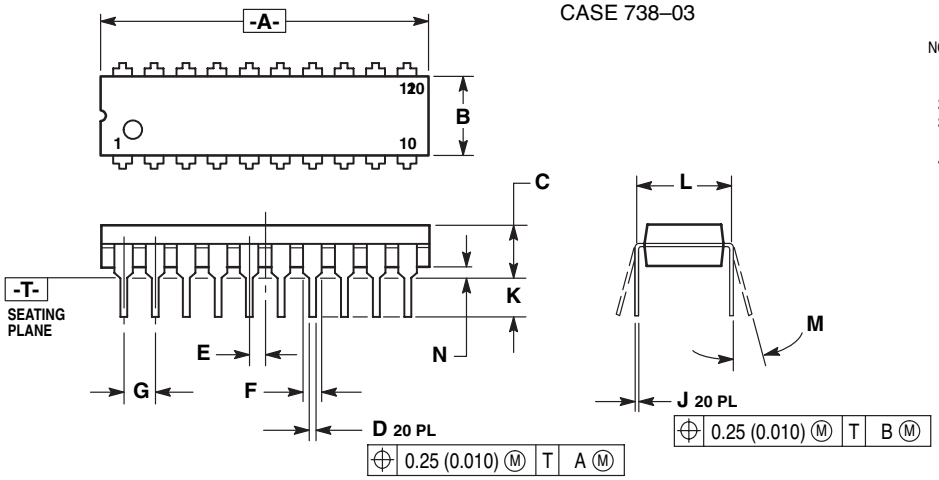


NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y 14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.55	12.80	0.494	0.504
B	5.10	5.40	0.201	0.213
C	–	2.00	–	0.079
D	0.35	0.45	0.014	0.018
G	1.27 BSC		0.050 BSC	
J	0.18	0.23	0.007	0.009
K	0.55	0.85	0.022	0.033
L	0.05	0.20	0.002	0.008
M	0°	7°	0°	7°
S	7.40	8.20	0.291	0.323

OUTLINE DIMENSIONS

PLASTIC DIP 20 = RP
(ML145428RP)
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01