LANSDALE Semiconductor, Inc.

ML145506

PCM Codec–Filter Mono–Circuit

Legacy Device: *Motorola MC145506*

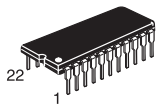
The ML145506 is a per channel codec–filter PCM mono–circuit. This device performs the voice digitization and reconstruction, as well as the band limiting and smoothing required for PCM systems. This device has HCMOS compatible digital outputs and supplements the Lansdale ML145502 – ML145505 series of PCM codec–filters. The ML145506 is functionally similar to the ML145502. It is designed to operate in both synchronous and asynchronous applications and contain an on–chip precision reference voltage. The ML145506 is offered in a 22–pin package and has the capability of selecting from three peak overload voltages (2.5 V, 3.15 V, and 3.78 V).

This device maintains compatibility with Motorola's family of MC3419/MC33120 SLIC products.

The ML1455xx family of PCM codec–filter mono–circuits utilize CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

ML145506 Features

- 22–Pin Package, HCMOS Output Version of ML145502
- Selectable Peak Overload Voltages (2.5 V, 3.15 V, 3.78 V)
- Push–Pull Analog Output with Gain Adjust
- 64 kHz to 4.1 MHz Transmit and/or Receive Data Clock Rate
- Operating Temperature Range T_A = –40° to +85° C



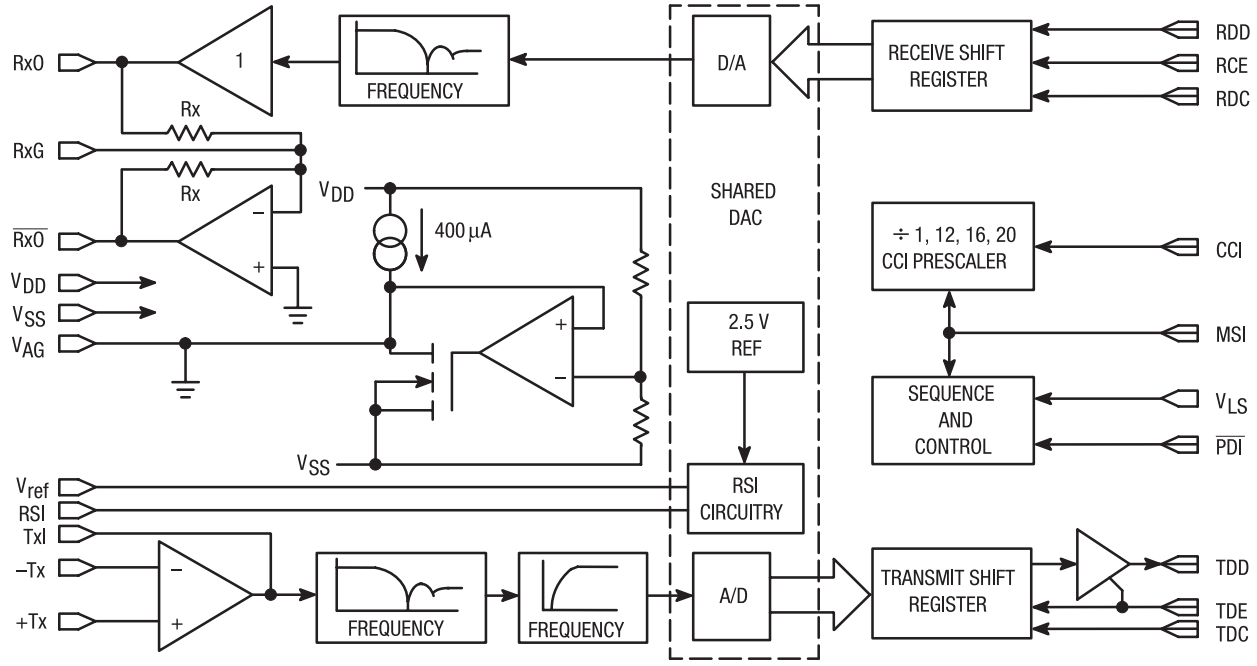
P DIP 22 = WP
PLASTIC DIP
CASE 708

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 22	MC145506P	ML145506WP

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

ML145506 PCM CODEC–FILTER MONO–CIRCUIT BLOCK DIAGRAM

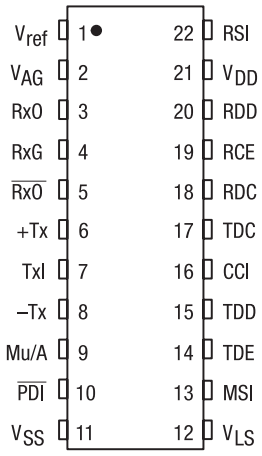


NOTES: ⇦ Controlled by V_{LS}.
Rx ≈ 100 kΩ (internal resistors).

PIN ASSIGNMENTS

(Drawings Do Not Reflect Relative Size)

ML145506



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	–0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	–0.5 to V_{DD} + 0.5	V
DC Drain Per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–85 to 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{SS}, V_{DD}, V_{LS}, or V_{AG}).

RECOMMENDED OPERATING CONDITIONS (T_A = –40° to 85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage					V
Dual Supplies: $V_{DD} = -V_{SS}$ ($V_{AG} = V_{LS} = 0$ V)		4.75	5.0	6.3	
Single Supply: V_{DD} to V_{SS} (V_{AG} is an Output, $V_{LS} = V_{DD}$ or V_{SS})					
Using Internal 3.15 V Reference		8.5	—	12.6	
Using Internal 2.5 V Reference		7.0	—	12.6	
Using Internal 3.78 V Reference		9.5	—	12.6	
Using External 1.5 V Reference, Referenced to V_{AG}		4.75	—	12.6	
Power Dissipation					mW
CMOS Logic Mode (V_{DD} to V_{SS} = 10 V, $V_{LS} = V_{DD}$)		—	40	70	
HCMOS Logic Mode (V_{DD} = 5 V, V_{SS} = –5 V, $V_{LS} = V_{AG}$ = 0 V)		—	50	90	
Power Down Dissipation		—	0.1	1.0	mW
Frame Rate Transmit and Receive		7.5	8.0	8.5	kHz
CCI Clock Rate		—	128	—	kHz
		—	1536	—	
Must Use One of These Frequencies ±2%, Relative to MSI Frequency of 8 kHz		—	1544	—	
		—	2048	—	
		—	2560	—	
Data Rate		64	—	4096	kHz
Full Scale Analog Input and Output Level					V_P
($V_{ref} = V_{SS}$)	RSI = V_{DD}	—	3.78	—	
	RSI = V_{SS}	—	3.15	—	
	RSI = V_{AG}	—	2.5	—	
Using an External Reference Voltage Applied at V_{ref} Pin	RSI = V_{DD}	—	1.51 x V_{ref}	—	
	RSI = V_{SS}	—	1.26 x V_{ref}	—	
	RSI = V_{AG}	—	V_{ref}	—	

DIGITAL LEVELS (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = –40° to 85°C)

Characteristic		Symbol	Min	Max	Unit
Input Voltage Levels (TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI, $\overline{PDI}$)					V
CMOS Mode ($V_{LS} = V_{DD}$, V_{SS} is Digital Ground)	"0"	V_{IL}	—	0.3 x V_{DD}	
	"1"	V_{IH}	0.7 x V_{DD}	—	
HCMOS Mode ($V_{LS} \le V_{DD}$ – 4.0 V, V_{LS} is Digital Ground)	"0"	V_{IL}	—	V_{LS} + 0.8 V	
	"1"	V_{IH}	V_{LS} + 2.0 V	—	
Output Current for TDD (Transmit Digital Data)					mA
CMOS Mode ($V_{LS} = V_{DD}$, V_{SS} = 0 V and is Digital Ground)					
	(V_{DD} = 5 V, V_{out} = 0.4 V)	I_{OL}	1.6	—	
	(V_{DD} = 10 V, V_{out} = 0.5 V)		1.6	—	
	(V_{DD} = 5 V, V_{out} = 4.5 V)	I_{OH}	–1.6	—	
	(V_{DD} = 10 V, V_{out} = 9.5 V)		–1.6	—	
HCMOS Mode ($V_{LS} \le V_{DD}$ – 4.75 V, V_{LS} = 0 V and is Digital Ground)	(V_{OL} = 0.4 V)	I_{OL}	1.6	—	
	($V_{OH} = V_{DD}$ – 0.5 V)	I_{OH}	–1.6	—	

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5%, V_{LS} = V_{AG} = 0 V, V_{ref} = RSI = V_{SS} (Internal 3.15 V Reference),
0 dBm0 = 1.546 Vrms = 6 dBm @ 600 Ω, T_A = –40° to 85°C, TDC = RDC = CCI, TDE = RCE = MSI, Unless Otherwise Noted)

Characteristic		End–to–End Min	End–to–End Max	A/D Min	A/D Max	D/A Min	D/A Max	Unit
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{DD} = 5 V, V_{SS} = –5 V)		—	—	–0.30	0.30	–0.30	0.30	dB
Absolute Gain Variation with Temperature 0° to 70°C		—	—	—	±0.03	—	±0.03	dB
Absolute Gain Variation with Temperature –40° to 85°C		—	—	—	±0.1	—	±0.1	dB
Absolute Gain Variation with Power Supply (V_{DD} = 5 V, V_{SS} = –5 V, 5%)		—	—	—	±0.02	—	±0.02	dB
Gain vs Level Tone (Relative to –10 dBm0, 1.02 kHz)	3 to –40 dBm0	–0.4	0.4	–0.2	0.2	–0.2	0.2	dB
	–40 to –50 dBm0	–0.8	0.8	–0.4	0.4	–0.4	0.4	
	–50 to –55 dBm0	–1.6	1.6	–0.8	0.8	–0.8	0.8	
Gain vs Level Pseudo Noise (A–Law Relative to –10 dBm0)								dB
CCITT G.714	–10 to –40 dBm0	—	—	–0.25	0.25	–0.25	0.25	
	–40 to –50 dBm0	—	—	–0.30	0.30	–0.30	0.30	
	–50 to –55 dBm0	—	—	–0.45	0.45	–0.45	0.45	
Total Distortion – 1.02 kHz Tone (C–Message)	0 to –30 dBm0	35	—	36	—	36	—	dBC
	–40 dBm0	29	—	29	—	30	—	
	–45 dBm0	24	—	24	—	25	—	
Total Distortion With Pseudo Noise (A–Law)	–3 dBm0	27.5	—	28	—	28.5	—	dB
CCITT G.714	–6 to –27 dBm0	35	—	35.5	—	36	—	
	–34 dBm0	33.1	—	33.5	—	34.2	—	
	–40 dBm0	28.2	—	28.5	—	30.0	—	
	–55 dBm0	13.2	—	13.5	—	15.0	—	
Idle Channel Noise (For End–End and A/D, See Note 1)								
	(Mu–Law, C–Message Weighted)	—	15	—	15	—	9	dBrnC0
	(A–Law, Psophometric Weighted)	—	–69	—	–69	—	–78	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0)	15 to 60 Hz	—	–23	—	–23	—	0.15	dB
	300 to 3000 Hz	–0.3	0.3	–0.15	0.15	–0.15	0.15	
	3400 Hz	–1.6	0	–0.8	0	–0.8	0	
	4000 Hz	—	–28	—	–14	—	–14	
	≥4600 Hz	—	–60	—	–32	—	–30	
Inband Spurious (1.02 kHz @ 0 dBm0, Transmit and RxO)		—	—	—	–43	—	–43	dBm0
	300 to 3000 Hz							
Out–of–Band Spurious at RxO (300 – 3400 Hz @ 0 dBm0 In)								dB
	4600 to 7600 Hz	—	–30	—	—	—	–30	
	7600 to 8400 Hz	—	–40	—	—	—	–40	
	8400 to 100,000 Hz	—	–30	—	—	—	–30	
Idle Channel Noise Selective @ 8 kHz, Input = V_{AG}, 30 Hz Bandwidth		—	–70	—	—	—	–70	dBm0
Absolute Delay @ 1020 Hz (TDC = 2.048 MHz, TDE = 8 kHz)								µs
Group Delay Referenced to 1600 Hz (TDC = 2048 kHz,								µs
TDE = 8 kHz)	500 to 600 Hz							
	600 to 800 Hz							
	800 to 1000 Hz							
	1000 to 1600 Hz							
	1600 to 2600 Hz							
	2600 to 2800 Hz							
	2800 to 3000 Hz							
Crosstalk of 1020 Hz @ 0 dBm0 From A/D or D/A (Note 2)		—	—	—	–75	—	–80	dB
Intermodulation Distortion of Two Frequencies of Amplitudes –4 to –21 dBm0 from the Range 300 to 3400 Hz		—	—	—	–41	—	–41	dB

NOTES:
1. Extrapolated from a 1020 Hz @ –50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ –50 dBm0.

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = –V_{SS} = 5 V to 6 V ±5%, T_A = –40° to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	+Tx, –Tx	I_{in}	—	±0.01	±0.2	µA
AC Input Impedance to V_{AG} (1 kHz)	+Tx, –Tx	Z_{in}	5	10	—	MΩ
Input Capacitance	+Tx, –Tx		—	—	10	pF
Input Offset Voltage of TxI Op Amp			—	< ±30	—	mV
Input Common Mode Voltage Range	+Tx, –Tx	V_{ICR}	V_{SS} + 1.0	—	V_{DD} – 2.0	V
Input Common Mode Rejection Ratio	+Tx, –Tx	CMRR	—	70	—	dB
TxI Unity Gain Bandwidth	$R_L \geq 10$ kΩ	BW_p	—	1000	—	kHz
TxI Open Loop Gain	$R_L \geq 10$ kΩ	A_{VOL}	—	75	—	dB
Equivalent Input Noise (C–Message) Between +Tx and –Tx, at TxI			—	–20	—	dBrnC0
Output Load Capacitance for TxI Op Amp			0	—	100	pF
Output Voltage Range TxI Op Amp, RxO or $\overline{RxO}$ R_L = 10 kΩ to V_{AG} R_L = 600 Ω to V_{AG}		V_{out}	 V_{SS} + 0.8 V_{SS} + 1.5	 — —	 V_{DD} – 1.0 V_{DD} – 1.5	V
Output Current TxI, RxO, $\overline{RxO}$	V_{SS} + 1.5 V ≤ V_{out} ≤ V_{DD} – 1.5 V		±5.5	—	—	mA
Output Impedance RxO, $\overline{RxO}$*	0 to 3.4 kHz	Z_{out}	—	3	—	Ω
Output Load Capacitance for RxO and $\overline{RxO}$*			0	—	200	pF
Output dc Offset Voltage Referenced to V_{AG} Pin	RxO $\overline{RxO}$*		— —	— —	±100 ±150	mV
Internal Gainsetting Resistors for RxG to RxO and $\overline{RxO}$			62	100	225	kΩ
External Reference Voltage Applied to V_{ref} (Referenced to V_{AG})			0.5	—	V_{DD} – 1.0	V
V_{ref} Input Current			—	—	20	µA
V_{AG} Output Bias Voltage			—	0.53 V_{DD} + 0.47 V_{SS}	—	V
V_{AG} Output Current	Source Sink	I_{VAG}	0.4 10.0	— —	0.8 —	mA
Output Leakage Current During Power Down for the TxI Op Amp, V_{AG}, RxO, and $\overline{RxO}$			—	—	±30	µA
Positive Power Supply Rejection Ratio, 0 – 100 kHz @ 250 mV, C–Message Weighting	Transmit Receive		45 55	50 65	— —	dBC
Negative Power Supply Rejection Ratio, 0 – 100 kHz @ 250 mV, C–Message Weighting	Transmit Receive		50 50	55 60	— —	dBC

* Assumes that RxG is not connected for gain modifications to $\overline{RxO}$.

MODE CONTROL LOGIC (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = –40° to 85°C)

Characteristic	Min	Typ	Max	Unit
V_{LS} Voltage for HCMOS Mode (HCMOS Logic Levels Referenced to V_{LS})	V_{SS}	—	V_{DD} – 4.0	V
V_{LS} Voltage for CMOS Mode (CMOS Logic Levels of V_{SS} to V_{DD})	V_{DD} – 0.5	—	V_{DD}	V
Mu/A Select Voltage				V
Mu–Law Mode	V_{DD} – 0.5	—	V_{DD}	
Sign Magnitude Mode	V_{AG} – 0.5	—	V_{AG} + 0.5	
A–Law Mode	V_{SS}	—	V_{SS} + 0.5	
RSI Voltage for Reference Select Input				V
3.78 V Mode	V_{DD} – 0.5	—	V_{DD}	
2.5 V Mode	V_{AG} – 0.5	—	V_{AG} + 0.5	
3.15 V Mode	V_{SS}	—	V_{SS} + 0.5	
V_{ref} Voltage for Internal or External Reference				V
Internal Reference Mode	V_{SS}	—	V_{SS} + 0.5	
External Reference Mode	V_{AG} + 0.5	—	V_{DD} – 1.0	
Analog Test Mode Selection Frequency, MS = CCI See Pin Description; Test Modes	—	128	—	kHz

SWITCHING CHARACTERISTICS (V_{SS} to V_{DD} = 9.5 V to 12.6 V, T_A = –40° to 85°C, C_L = 150 pF, CMOS or HCMOS Mode)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Rise Time	TDD	t_{TLH}	—	30	80	ns
Output Fall Time		t_{THL}	—	30	80	
Input Rise Time	TDE, TDC, RCE, RDC, DC, MSI, CCI	t_{TLH}	—	—	4	µs
Input Fall Time		t_{THL}	—	—	4	
Pulse Width	TDE Low, TDC, RCE, RDC, DC, MSI, CCI	t_W	100	—	—	ns
Data Clock Pulse Frequency	TDC, RDC, DC	f_{CL}	64	—	4096	kHz
CCI Clock Pulse Frequency (MSI = 8 kHz)		f_{CL1}	—	128	—	kHz
This Pin Will Accept One of These Discrete Clock Frequencies and		f_{CL2}	—	1536	—	
Will Compensate to Produce Internal Sequencing		f_{CL3}	—	1544	—	
		f_{CL4}	—	2048	—	
		f_{CL5}	—	2560	—	
Propagation Delay Time						ns
TDE Rising to TDD Low Impedance	HCMOS	t_{P1}	—	90	180	
	CMOS		—	90	150	
TDE Falling to TDD High Impedance	HCMOS	t_{P2}	—	—	55	
	CMOS		—	—	40	
TDC Rising Edge to TDD Data, During TDE High	HCMOS	t_{P3}	—	90	180	
	CMOS		—	90	150	
TDE Rising Edge to TDD Data, During TDC High	HCMOS	t_{P4}	—	90	180	
	CMOS		—	90	150	
TDC Falling Edge to TDE Rising Edge Setup Time		t_{su1}	20	—	—	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su2}	100	—	—	ns
TDE Falling Edge to TDC Rising Edge to Preserve the Next TDD Data		t_{su8}	20	—	—	ns
RDC Falling Edge to RCE Rising Edge Setup Time		t_{su3}	20	—	—	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su4}	100	—	—	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su5}	60	—	—	ns
CCI Falling Edge to MSI Rising Edge Setup Time		t_{su6}	20	—	—	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su7}	100	—	—	ns
RDD Hold Time from RDC Falling Edge		t_h	100	—	—	ns
TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI Input Capacitance			—	—	10	pF
TDE,TDC, RCE, RDC, RDD, DC, MSI, CCI Input Current			—	±0.01	±0.2	µA
TDD Capacitance During High Impedance (TDE Low)			—	12	15	pF
TDD Input Current During High Impedance (TDE Low)			—	±0.1	±10.0	µA

DEVICE DESCRIPTIONS

A codec–filter is a device which is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "coder" for the A/D used to digitize voice, and "decoder" for the D/A used for reconstructing voice. A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal to distortion of about 30 dB for a dynamic range of about 40 dB. This may be accomplished with a linear 13–bit A/D and D/A, but will far exceed the required signal to distortion at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13–bit linear scheme to companded 8–bit schemes. These companding schemes follow a segmented or "piecewise–linear" curve formatted as a sign bit, 3 chord bits, and 4 step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the 4 step bits increment and carry to the 3 chord bits which increment. With the chord bits incremented, the step bits double their voltage weighting. This results in an effective resolution of 6 bits (sign + chord + 4 step bits) across a 42 dB dynamic range (7 chords above 0, by 6 dB per chord). There are two companding schemes used; Mu–255 Law specifically in North America, and A–Law specifically in Europe. These companding schemes are accepted world wide. The tables show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a band-width of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling which must be attenuated from the signal by a high–pass filter before the A/D converter. The D/A process reconstructs a staircase version of the desired inband signal which has spectral images of the in-band signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components which need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The ML1455xx series PCM codec–filters have the codec, both presampling and reconstruction filters, a precision voltage reference on chip, and require no external components.

ML145506

The ML145506 PCM codec–filter is the full–featured 22–pin device. It is intended for use in applications requiring maximum flexibility. The ML145506 is intended for bit interleaved or byte interleaved applications with data clock frequencies which are nonstandard or time varying. One of the five standard frequencies (listed in CCI Convert Clock Input section) is applied to the CCI input, and the data clock inputs can be any frequency between 64 kHz and 4.096 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference. The RxG pin accommodates gain adjustments for the inverted analog output. All three pins of the input gain setting operational amplifier are present which provide maximum flexibility for the analog interface.

PIN DESCRIPTIONS

DIGITAL

V_{LS}
Logic Level Select Input and HCMOS Digital Ground

V_{LS} controls the logic levels and digital ground reference for all digital inputs and the digital output. These devices can operate with logic levels from full supply (V_{SS} to V_{DD}) or with TTL logic levels using V_{LS} as digital ground. For $V_{LS} = V_{DD}$, all I/O is full supply (V_{SS} to V_{DD} swing) with CMOS switch points. For $V_{SS} < V_{LS} < (V_{DD} – 4\ V)$, all inputs are TTL compatible with VLS being the digital ground while TDD outputs HCMOS levels from V_{LS} to V_{DD}. The pins controlled by V_{LS} are inputs MSI, CCI, TDE, TDC, RCE, RDC, RDD, $\overline{PDI}$, and output TDD.

MSI
Master Synchronization Input

MSI is used for determining the sample rate of the transmit side and as a time base for selecting the internal prescale divider for the convert clock input (CCI) pin. The MSI pin should be tied to an 8 kHz clock which may be a frame sync or system sync signal. MSI has no relation to transmit or receive data timing, except for determining the internal transmit strobe as described under the TDE pin description. MSI should be derived from the transmit timing in asynchronous applications. In many applications, MSI can be tied to TDE.

CCI
Convert Clock Input

CCI is designed to accept five discrete clock frequencies. These are 128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The duty cycle of CCI is dictated by the minimum pulse width except for 128 kHz, which is used directly for internal sequencing and must have a 40% to 60% duty cycle. In asynchronous applications, CCI should be derived from transmit timing.

TDC
Transmit Data Clock Input

TDC can be any frequency from 64 kHz to 4.096 MHz, and is often tied to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and its rising edges produce successive data bits at TDD. TDE should be derived from this clock.

TDE
Transmit Data Enable Input

TDE serves three major functions. The first TDE rising edge following an MSI rising edge, generates the internal transmit strobe which initiates an A/D conversion. The internal transmit strobe also transfers a new PCM data word into the transmit shift register (sign bit first) ready to be output at TDD. The TDE pin is the high–impedance control for the transmit digital data (TDD) output. As long as this pin is high, the TDD output stays low impedance. This pin also enables the output shift register for clocking out the 8–bit serial PCM word. The logical AND of the TDE pin with the TDC pin, clocks out a new data bit at TDD. TDE should be held high for eight consecutive TDC cycles to clock out a complete PCM word for byte interleaved applications. The transmit shift register feeds back on itself to allow multiple reads of the transmit data. If the PCM word is clocked out once per frame in a byte interleaved system, the MSI pin function is transparent and may be connected to TDE.

The TDE pin may be cycled during a PCM word for bit interleaved applications. TDE controls both the high–impedance state of the TDD output and the internal shift clock. TDE must fall before TDC rises (t_{su8}) to ensure integrity of the next data bit. There must be at least two TDC falling edges between the last TDE rising edge of one frame and the first TDE rising edge of the next frame. MSI must be available separate from TDE for bit interleaved applications.

TDD
Transmit Digital Data Output

The output levels at this pin are controlled by the VLS pin. For V_{LS} connected to V_{DD}, the output levels are from V_{SS} to V_{DD}. For a voltage of V_{LS} between V_{DD} – 4 V and V_{SS}, the output levels are HCMOS compatible with V_{LS} being the digital ground supply and V_{DD} being the positive logic supply. The TDD pin is a three–state output controlled by the TDE pin. The timing of this pin is controlled by TDC and TDE. The data format (Mu–Law, A–Law, or sign magnitude) is controlled by the Mu/A pin.

RDC
Receive Data Clock Input

RDC can be any frequency from 64 kHz to 4.096 MHz. This pin is often tied to the TDC pin for applications that can use a common clock for both transmit and receive data transfers.The receive shift register is controlled by the receive clock enable (RCE) pin to clock data into the receive digital data (RDD) pin on falling RDC edges. These three signals can be asynchronous with all other digital pins.

RCE
Receive Clock Enable Input

The rising edge of RCE should identify the sign bit of a receive PCM word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive PCM word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In asynchronous applications with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 kHz and 8.5 kHz. Two receive PCM words may be decoded and analog summed each transmit frame to allow on–chip conferencing. The two PCM words should be clocked in as two single PCM words, a minimum of 31.25 μs apart, with a receive data clock of 512 kHz or faster.

RDD
Receive Digital Data Input

RDD is the receive digital data input. The timing for this pin is controlled by RDC and RCE. The data format is determined by the Mu/A pin.

Mu/A
Mu/A Select

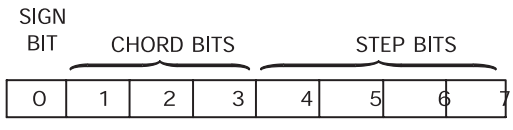
This pin selects the companding law and the data format atTDD and RDD.

Mu/A = V_{DD}; Mu–255 Companding D3 Data Format with Zero Code Suppress

Mu/A = VAG; Mu–255 Companding with Sign Magnitude Data Format

Mu/A = VSS; A–Law Companding with CCITT Data Format Bit Inversions

Code	Sign/ Magnitude	Mu–Law	A–Law (CCITT)
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
– Zero	0000 0000	0111 1111	0101 0101
– Full Scale	0111 1111	0000 0010	0010 1010



NOTE: Starting from sign magnitude, to change format:
To Mu–Law —
MSB is unchanged (sign)
Invert remaining 7 bits
If code is 0000 0000, change to 0000 0010 (for zero code suppression)

To A–Law —
MSB is unchanged (sign)
Invert odd numbered bits
Ignore zero code suppression

$\overline{PDI}$
Power Down Input

The power down input disables the bias circuitry and gates off all clock inputs. This puts the V_{AG}, Txl, RxO, $\overline{RxO}$, and TDD outputs into a high–impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI}$ is a low logic level. The circuit operates normally with $\overline{PDI}$ = V_{DD} or with a logic high as defined by connection at V_{LS}. TDD will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

ANALOG

V_{AG}
Analog Ground Input/Output Pin

V_{AG} is the analog ground power supply input/output. All analog signals into and out of the device use this as their ground reference. Each version of the ML1455xx PCM codec–filter family can provide its own analog ground supply internally. The dc voltage of this internal supply is 6% positive of the midway between V_{DD} and V_{SS}. This supply can sink more than 8 mA but has a current source limited to 400 μA. The output of this supply is internally connected to the analog ground input of the part. The node where this supply and the analog ground are connected is brought out to the V_{AG} pin. In symmetric dual supply systems (±5, ±6, etc.), V_{AG} may be externally tied to the system analog ground supply. When $\overline{RxO}$ or RxO drive low–impedance loads tied to V_{AG}, a pull–up resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground. All analog signals for the part are referenced to V_{AG}, including noise; therefore, decoupling capacitors (0.1 μF) should be used from V_{DD} to V_{AG} and V_{SS} to V_{AG}.

V_{ref}
Positive Voltage Reference Input

The V_{ref} pin allows an external reference voltage to be used for the A/D and D/A conversions. If V_{ref} is tied to V_{SS}, the internal reference is selected. If $V_{ref} > V_{AG}$, then the external mode is selected and the voltage applied to V_{ref} is used for generating the internal converter reference voltage. In either internal or external reference mode, the actual voltage used for conversion is multiplied by the ratio selected by the RSI pin. The RSI pin circuitry is explained under its pin description below. Both the internal and external references are inverted within the PCM codec–filter for negative input voltages such that only one reference is required.

External Mode — In the external reference mode ($V_{ref} > V_{AG}$), a 2.5 V reference like the MC1403 may be connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref} pins and V_{AG} pins from different codec–filters. In special applications, the external reference voltage may be between 0.5 and 5 V. However, the reference voltage gain selection circuitry associated with RSI must be considered to arrive at the desired codec–filter gain.

Internal Mode — In the internal reference mode ($V_{ref} = V_{SS}$), an internal 2.5 V reference supplies the reference voltage for the RSI circuitry.

RSI
Reference Select Input

The RSI input allows the selection of three different overload or full–scale A/D and D/A converter reference voltages independent of the internal or external reference mode. The RSI pin is a digital input that senses three different logic states: V_{SS}, V_{AG}, and V_{DD}. For RSI = V_{AG}, the reference voltage is used directly for the converters. The internal reference is 2.5 V. For RSI = V_{SS}, the reference voltage is multiplied by the ratio of 1.26, which results in an internal converter reference of 3.15 V. For RSI = V_{DD}, the reference voltage is multiplied by 1.51, which results in an internal converter reference of 3.78 V. The device requires a minimum of 1.0 V of headroom between the internal converter reference to V_{DD}. V_{SS} has this same absolute valued minimum, also measured from the V_{AG} pin. The various modes of operation are summarized in Table 2.

RxO, $\overline{RxO}$
Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak–to–peak signal described with the reference. If a 3.15 V reference is used with RSI tied to V_{AG} and a 3 dBm0 sine wave is decoded, the RxO output will be a 6.3 V peak–to–peak signal. $\overline{RxO}$ will also have an inverted signal output of 6.3 V peak–to–peak. External loads may be connected from RxO to $\overline{RxO}$ for a 6 dB push–pull signal gain or from either RxO or $\overline{RxO}$ to V_{AG}. With a 3.15 V reference, each output will drive 600 Ω to 9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to 9 dBm.

RxG
Receive Output Gain Adjust

The purpose of the RxG pin is to allow external gain adjustment for the $\overline{RxO}$ pin. If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{RxO}$. Thus, the push–pull gain to a load from RxO to $\overline{RxO}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{RxO}$ (RG), the gain of $\overline{RxO}$ can be set differently from inverting unity. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{RxO}$ gain is approximately equal to minus RG/RI. The actual gain is determined by taking into account the internal resistors which will be in parallel to these external resistors. The internal resistors have a large tolerance, but they match each other very closely. This matching tends to minimize the effects of their tolerance on external gain configurations. The circuit for RxG and $\overline{RxO}$ is shown in the Block Diagram.

Txl
Transmit Analog Input

TxI is the input to the transmit filter. It is also the output of the transmit gain amplifier. The TxI input has an internal gain

of 1.0, such that a 3 dBm0 signal at TxI corresponds to the peak converter reference voltage as described in the V_{ref} and RSI pin descriptions. For a 3.15 V reference, the 3 dBm0 input should be 6.3 V peak–to–peak.

+Tx/ –Tx
Positive Tx Amplifier Input
Negative Tx Amplifier Input

The Txl pin is the input to the transmit band–pass filter. If +Tx or –Tx is available, then there is an internal amplifier preceding the filter whose pins are +Tx, –Tx, and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 kΩ.

POWER SUPPLIES

V_{DD}
Most Positive Power Supply

V_{DD} is typically 5 V to 12 V.

V_{SS}
Most Negative Power Supply

V_{SS} is typically 10 V to 12 V negative of V_{DD}. For a ±5 V dual–supply system, the typical power supply configuration is V_{DD} = 5 V, V_{SS} = –5 V, V_{LS} = 0 V (digital ground accommodating TTL logic levels), and V_{AG} = 0 V being tied to system analog ground.

For single–supply applications, typical power supply configurations include:

V_{DD} = 10 V to 12 V
V_{SS} = 0 V

V_{AG} generates a mid supply voltage for referencing all analog signals.

V_{LS} controls the logic levels. This pin should be connected to V_{DD} for CMOS logic levels from V_{SS} to V_{DD}. This pin should be connected to digital ground for true TTL logic input levels referenced to V_{LS}, with HCMOS output levels from V_{LS} to V_{DD}.

TESTING CONSIDERATIONS

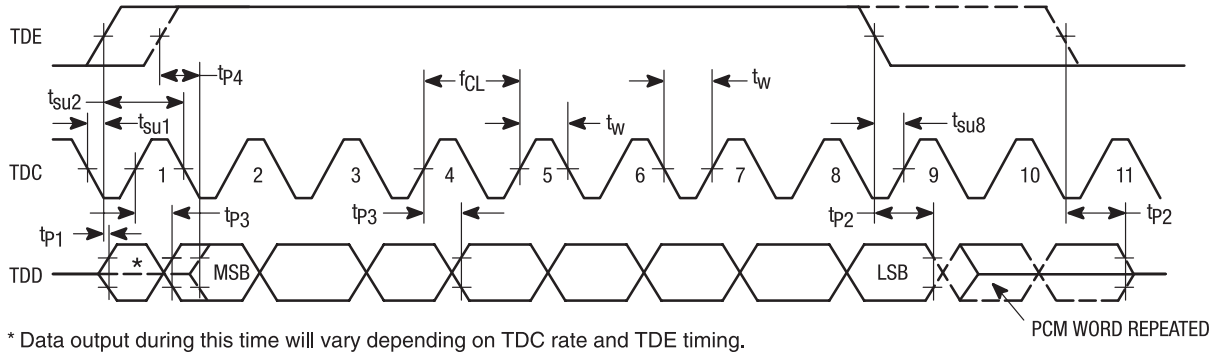
An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the A/D (the output of the Tx filter) is available at the $\overline{PDI}$ pin. This input is direct coupled to the A/D side of the codec. The A/D is a differential design. This results in the gain of this input being effectively attenuated by half. If monitored with a high–impedance buffer, the output of the Tx low–pass filter can also be measured at the $\overline{PDI}$ pin. This test mode allows independent evaluation of the transmit low–pass filter and A/D side of the codec. The transmit and receive channels of these devices are tested with the codec–filter fully functional.

Table 1. ML145506 Options Available by Pin Selection

RSI* Pin Level	V_{ref}* Pin Level	Peak–to–Peak Overload Voltage (TxI, RxO)
V_{DD}	V_{SS}	7.56 Vp–p
V_{DD}	V_{AG} + V_{EXT}	(3.02 x V_{EXT}) Vp–p
V_{AG}	V_{SS}	5 Vp–p
V_{AG}	V_{AG} + V_{EXT}	(2 x V_{EXT}) Vp–p
V_{SS}	V_{SS}	6.3 Vp–p
V_{SS}	V_{AG} + V_{EXT}	(2.52 x V_{EXT}) Vp–p

Table 2. Summary of Operation Conditions User Programmed Through Pins V_{DD}, V_{AG}, and V_{SS}

Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu–Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu–Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Input Levels, V_{AG} Up; HCMOS Output Levels, V_{AG} to V_{DD}
V_{SS}	A–Law Companding Curve and CCITT Digital Format	3.15	TTL Levels, V_{SS} Up; HCMOS Output Levels, V_{SS} to V_{DD}



* Data output during this time will vary depending on TDC rate and TDE timing.

Figure 2. Transmit Timing Diagram

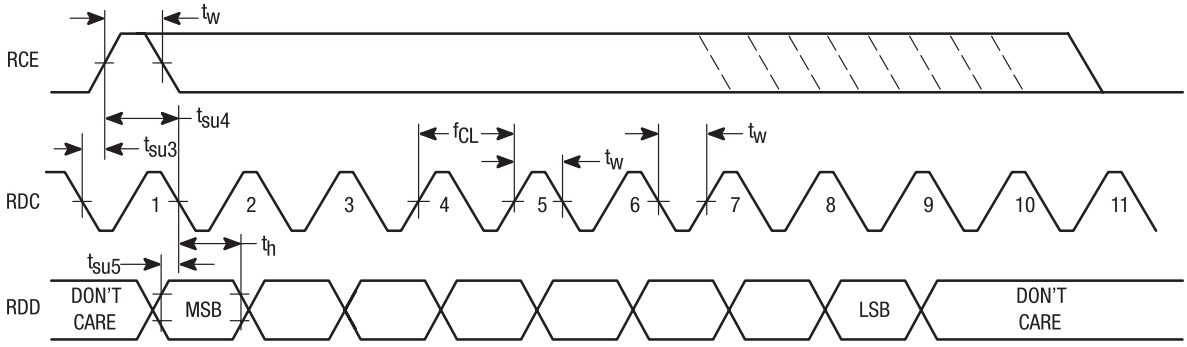


Figure 3. Receive Timing Diagram

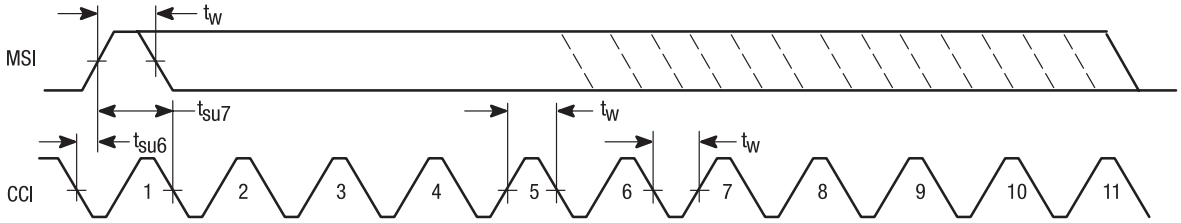


Figure 4. MSI/CCI Timing Diagram

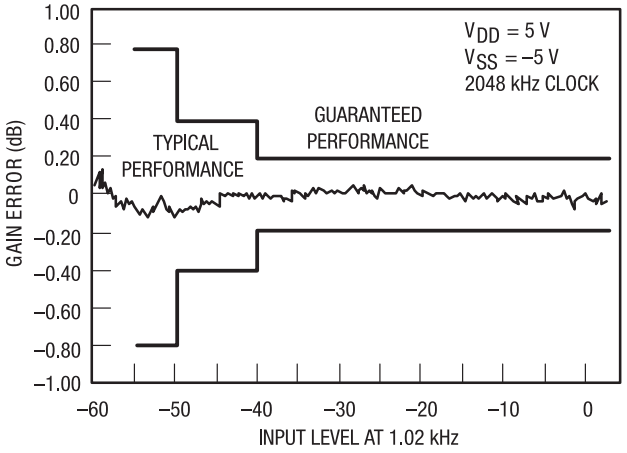


Figure 5. ML145506 Gain vs Level Mu–Law Transmit

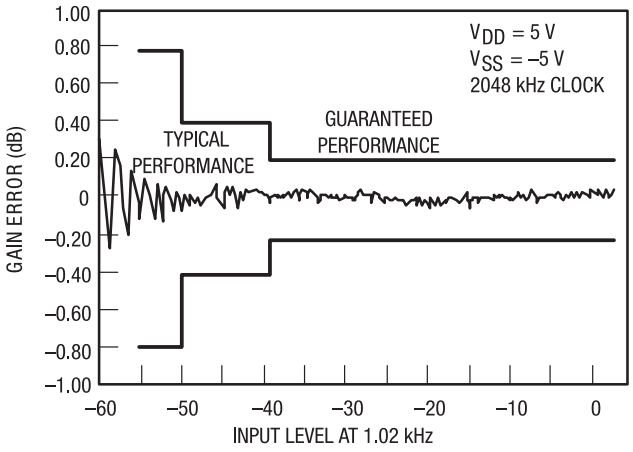


Figure 6. ML145506 Gain vs Level Mu–Law Receive

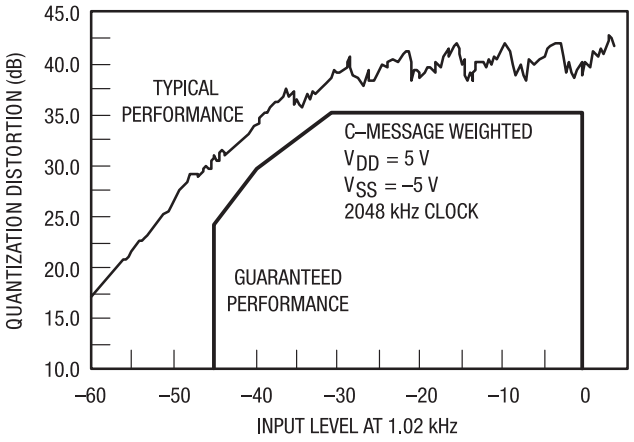


Figure 7. ML145506 Quantization Distortion Mu–Law Transmit

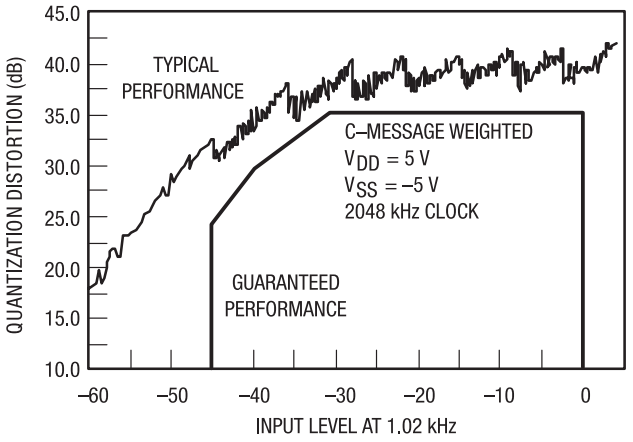


Figure 8. ML145506 Quantization Distortion Mu–Law Receive

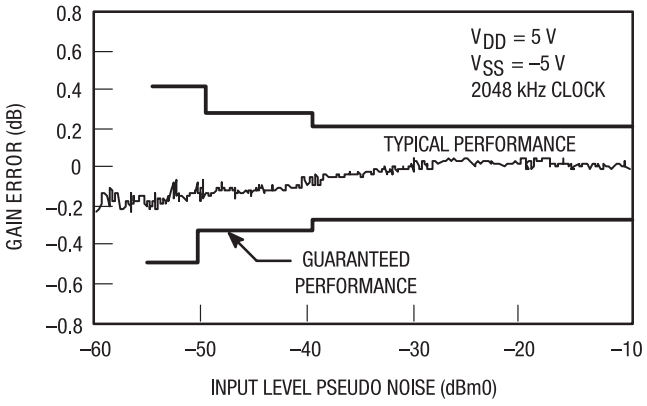


Figure 9. ML145506 Gain vs Level A–Law Transmit

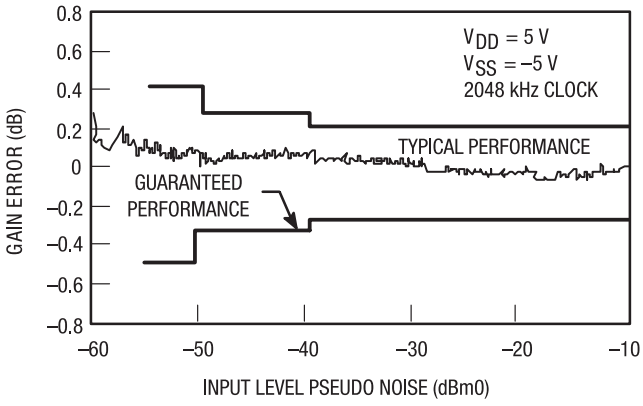


Figure 10. ML145506 Gain vs Level A–Law Receive

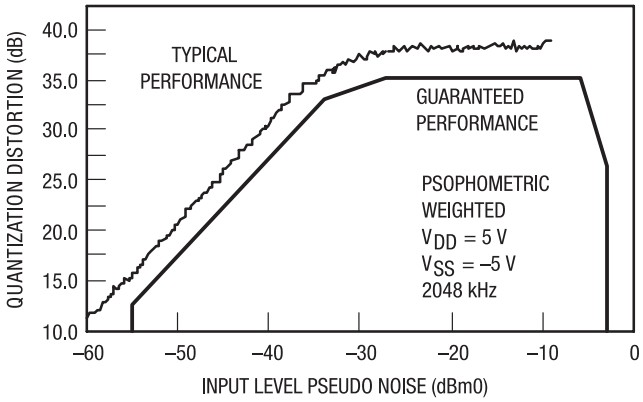


Figure 11. ML145506 Quantization Distortion A–Law Transmit

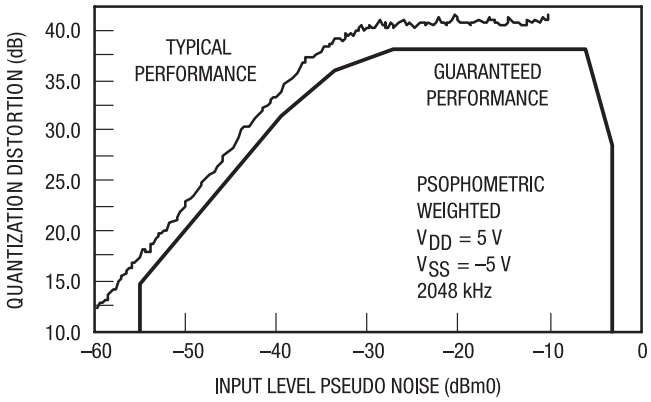


Figure 12. ML145506 Quantization Distortion A–Law Receive

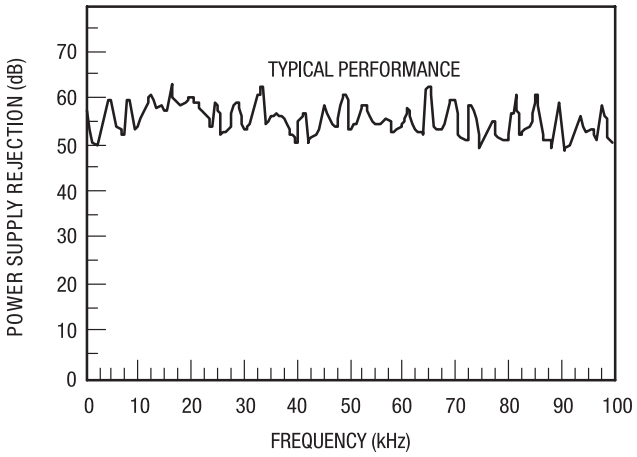


Figure 13. ML145506 Power Supply Rejection Ratio Positive Transmit VAC = 250 mVrms, C–Message Weighted

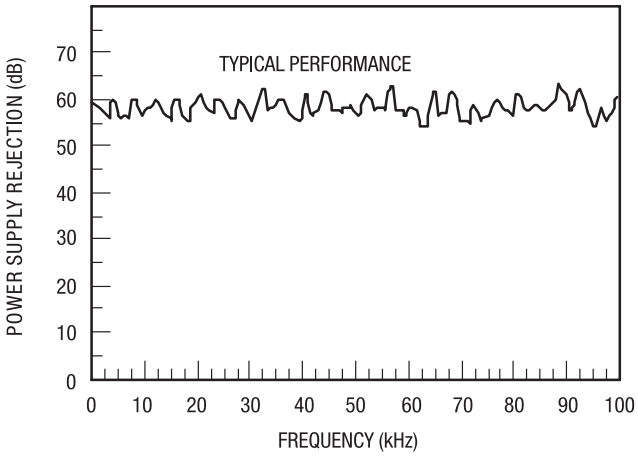


Figure 14. ML145506 Power Supply Rejection Ratio Negative Transmit VAC = 250 mVrms, C–Message Weighted

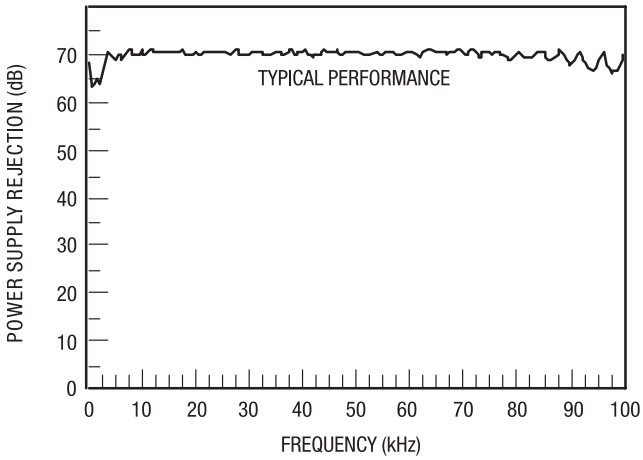


Figure 15. ML145506 Power Supply Rejection Ratio Positive Receive VAC = 250 mVrms, C–Message Weighted

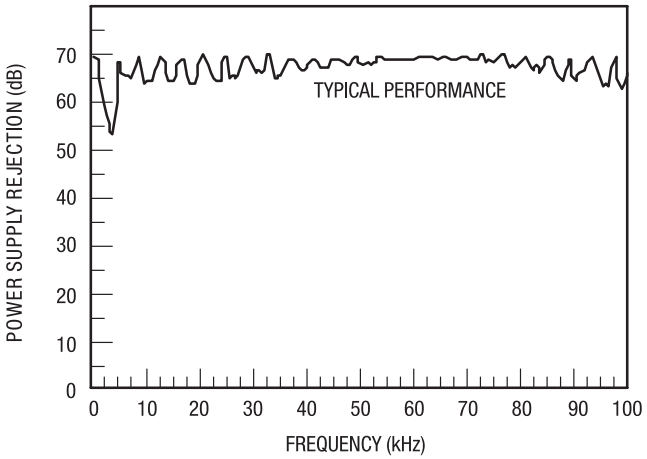


Figure 16. ML145506 Power Supply Rejection Ratio Negative Receive VAC = 250 mVrms, C–Message Weighted

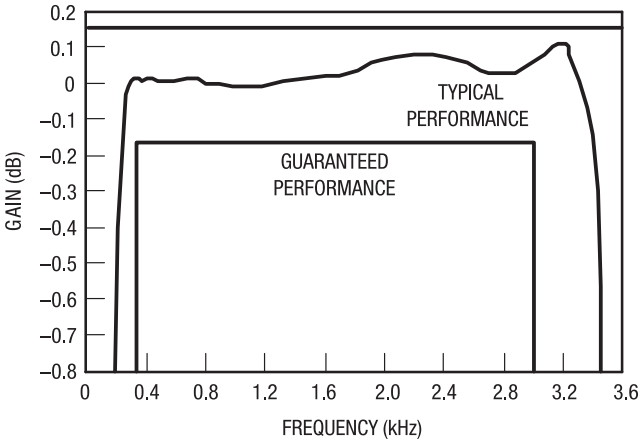


Figure 17. ML145506 Pass–Band Filter Response Transmit

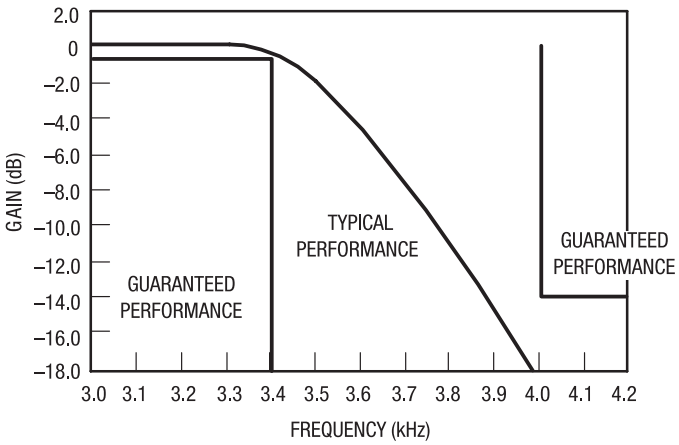


Figure 18. ML145506 Low–Pass Filter Response Transmit

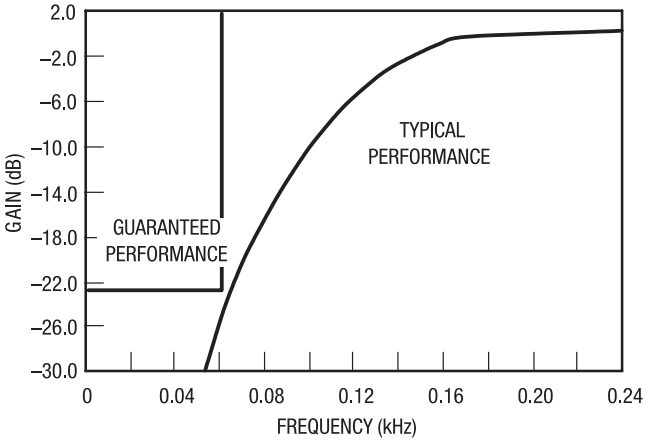


Figure 19. ML145506 High–Pass Filter Response Transmit

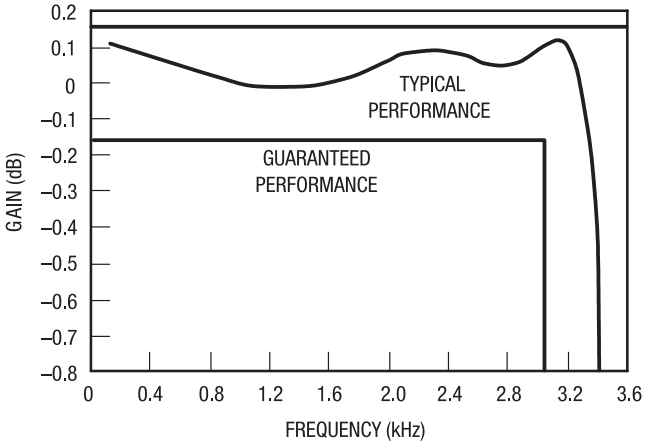


Figure 20. ML145506 Pass–Band Filter Response Receive

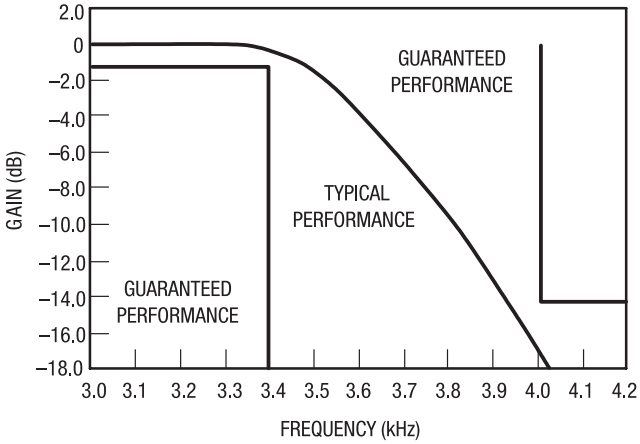


Figure 21. ML145506 Low–Pass Filter Response Receive

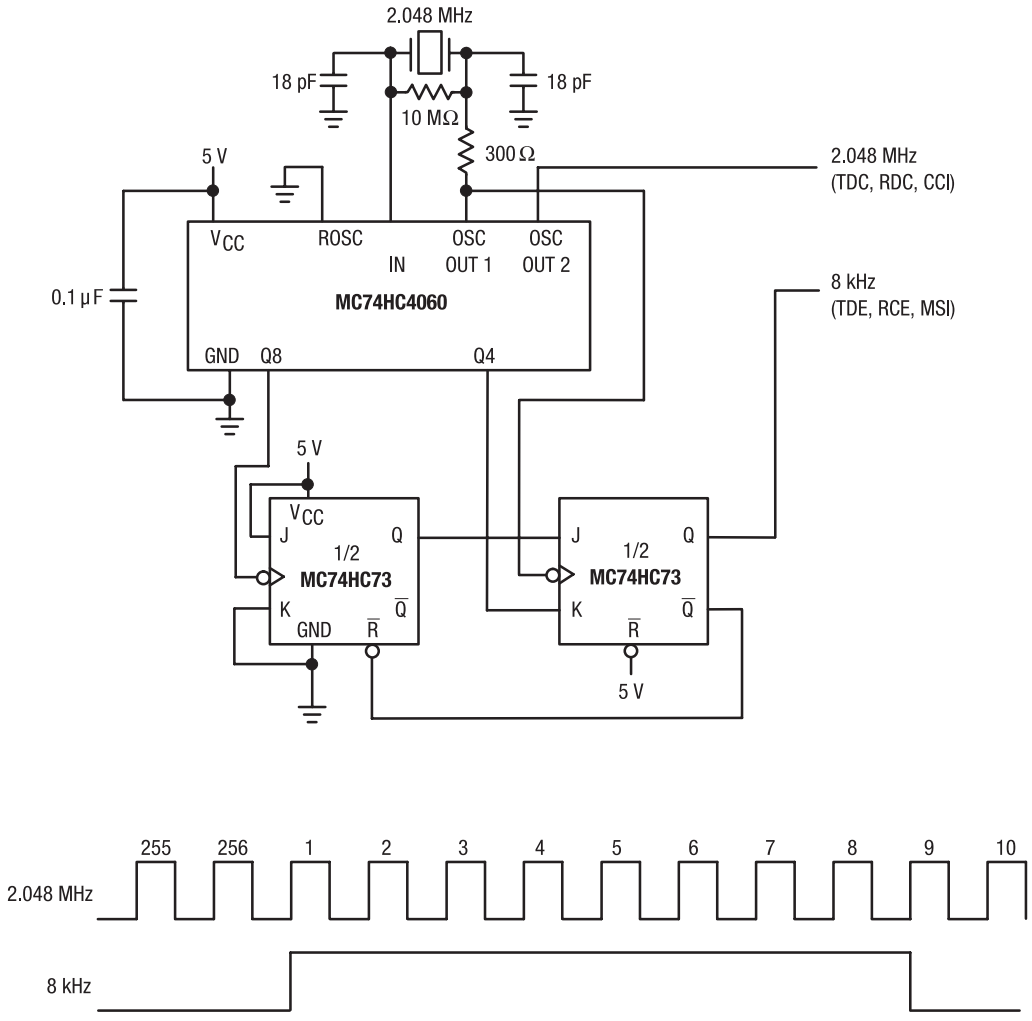
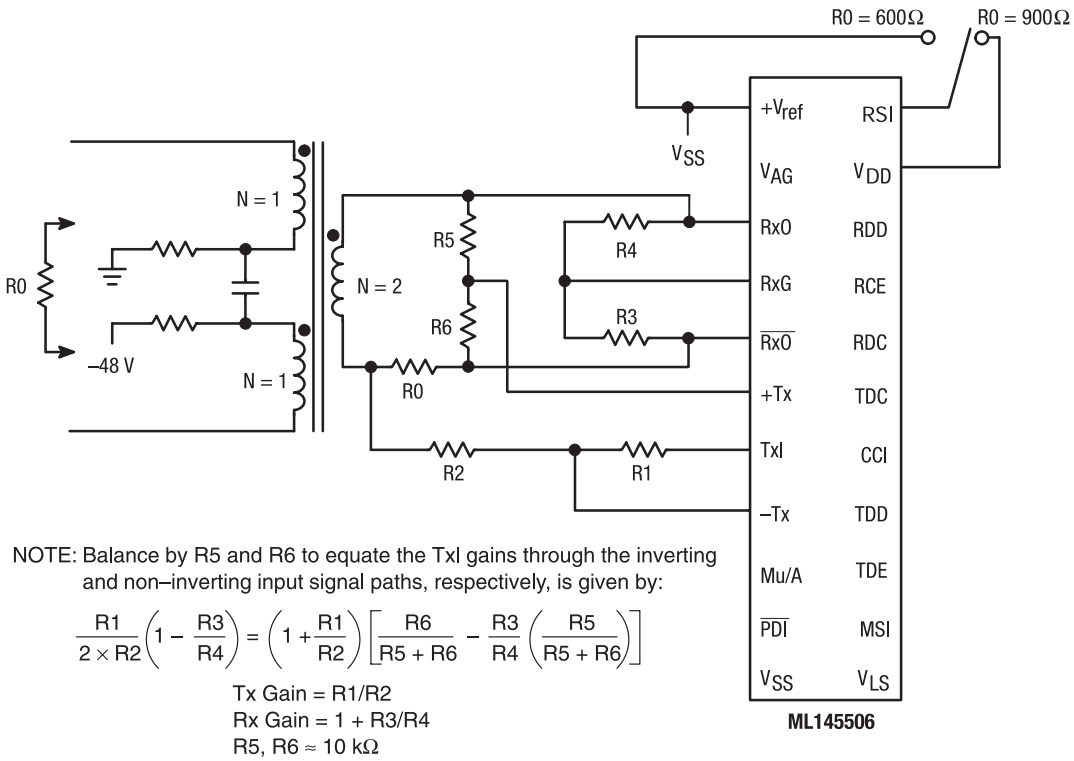


Figure 22. Simple Clock Circuit for Driving ML145506 Codec–Filters

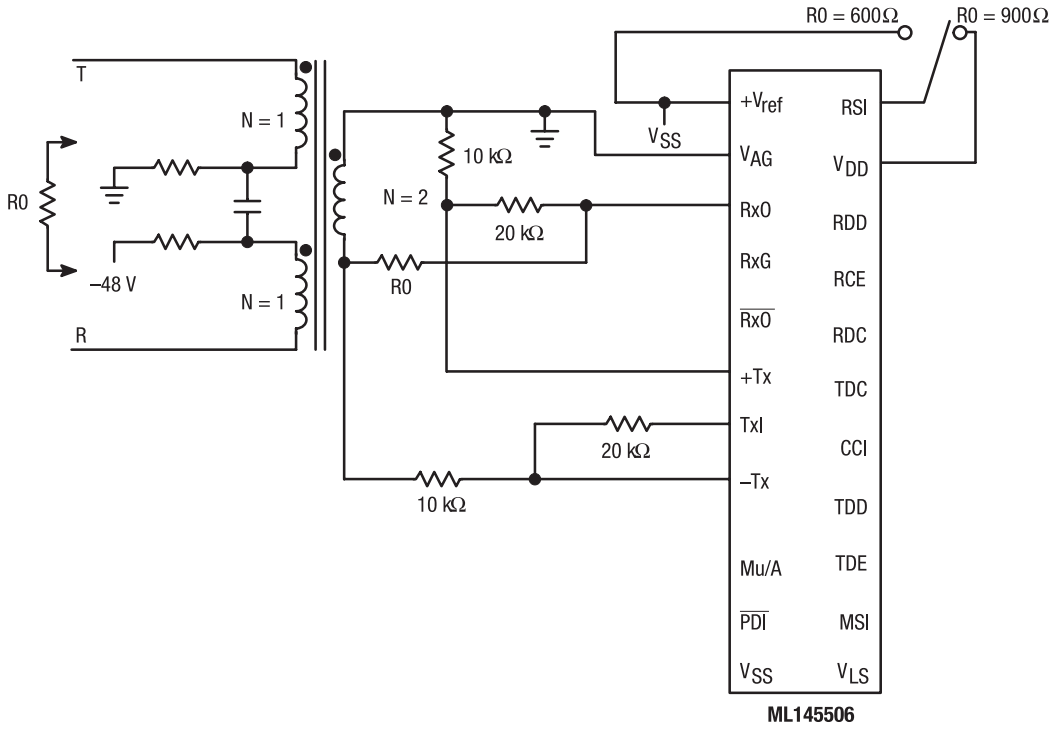


NOTE: Balance by R5 and R6 to equate the TxI gains through the inverting and non–inverting input signal paths, respectively, is given by:

$$\frac{R1}{2 \times R2}\left(1 - \frac{R3}{R4}\right) = \left(1 + \frac{R1}{R2}\right)\left[\frac{R6}{R5 + R6} - \frac{R3}{R4}\left(\frac{R5}{R5 + R6}\right)\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≈ 10 kΩ
Adjust Rx Gain with R3
Adjust Tx Gain with R1

(a) Universal Transformer Hybrid Using ML145506



(b) Single–Ended Hybrid Using ML145506

Figure 24. Hybrid Interfaces to the ML145506 PCM Codec–Filter Mono–Circuit

Table 3. Mu–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
8	16	256		1	0	0	0	0	0	0	0	8031
			7903 ⋮ 4319					⋮				⋮
				1	0	0	0	1	1	1	1	4191
			4063 ⋮					⋮				⋮
7	16	128	2143									
				1	0	0	1	1	1	1	1	2079
			2015 ⋮					⋮				⋮
6	16	64	1055									
				1	0	1	0	1	1	1	1	1023
			991 ⋮					⋮				⋮
5	16	32	511									
				1	0	1	1	1	1	1	1	495
			479 ⋮					⋮				⋮
4	16	16	239									
				1	1	0	0	1	1	1	1	231
			223 ⋮					⋮				⋮
3	16	8	103									
				1	1	0	1	1	1	1	1	99
			95 ⋮					⋮				⋮
2	16	4	35									
				1	1	1	0	1	1	1	1	33
			31 ⋮					⋮				⋮
1	15	2	3									
				1	1	1	1	1	1	1	0	2
	1	1	1									
				1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

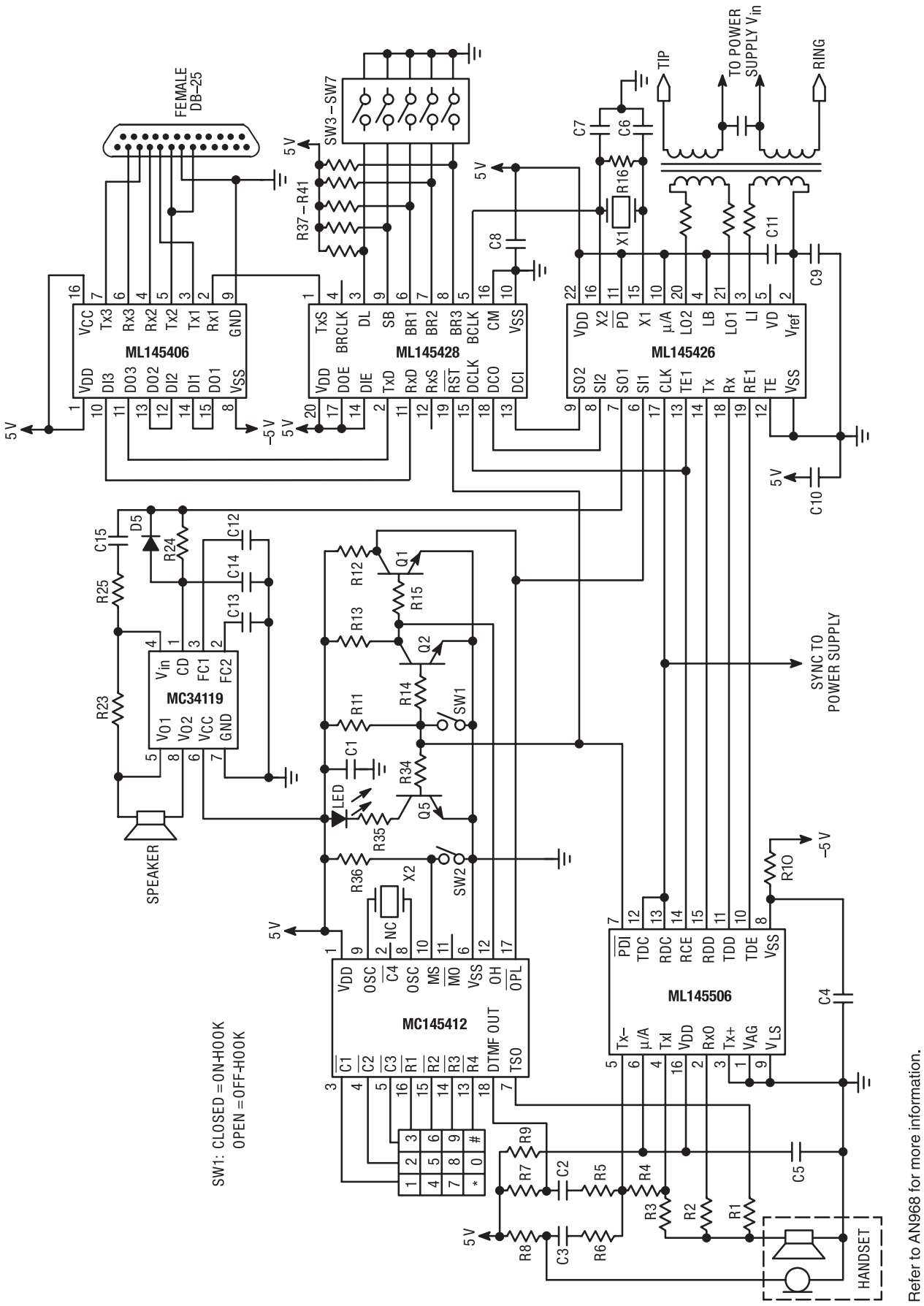


Figure 26. Digital Telephone Schematic

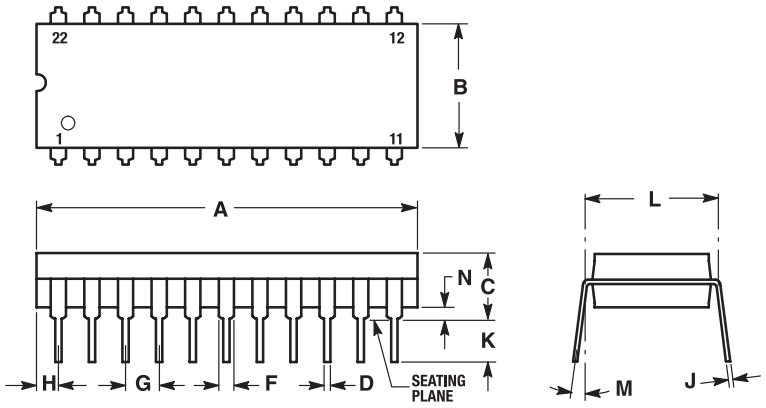
Table 4. A–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
7	16	128	3968	1	0	1	0	1	0	1	0	4032
			⋮					⋮				⋮
			2176	1	0	1	0	0	1	0	1	2112
			2048									
6	16	64	⋮					⋮				⋮
			1088	1	0	1	1	0	1	0	1	1056
			1024									
5	16	32	⋮					⋮				⋮
			544	1	0	0	0	0	1	0	1	528
			512									
4	16	16	⋮					⋮				⋮
			272	1	0	0	1	0	1	0	1	264
			256									
3	16	8	⋮					⋮				⋮
			136	1	1	1	0	0	1	0	1	132
			128									
2	16	4	⋮					⋮				⋮
			68	1	1	1	1	0	1	0	1	66
			64									
1	32	2	⋮					⋮				⋮
			2	1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inversion, as specified by CCITT.

OUTLINE DIMENSIONS

P DIP 22 = WP
(ML145506WP)
PLASTIC DIP
CASE 708–04



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040