LANSDALE Semiconductor, Inc.

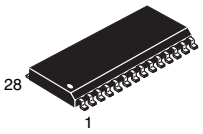
ML145583

3.3 Volt Only Driver/Receiver with an Integrated Standby Mode RS 232/EIA–232–E and CCITT V.28

Legacy Device: *Motorola MC145583*

The ML145583 is a CMOS transceiver composed of three drivers and five receivers that fulfills the electrical specifications of EIA–232–E, EIA–562, and CCITT V.28 while operating from a single + 3.3 or + 5.0 V power supply. This transceiver is a high–performance, low–power consumption device that is equipped with a standby function.

A voltage tripler and inverter converts the + 3.3 V to ± 8.8 V, or a voltage doubler and inverter converts the + 5.0 V to ± 8.8 V. This is accomplished through an on–chip 40 kHz oscillator and five inexpensive external capacitors.



SOIC 28W = -7P
SOG PACKAGE
CASE 751F

PACKAGE	MOTOROLA	LANSDALE
SOIC 28W	MC145583DW	ML145583-7P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

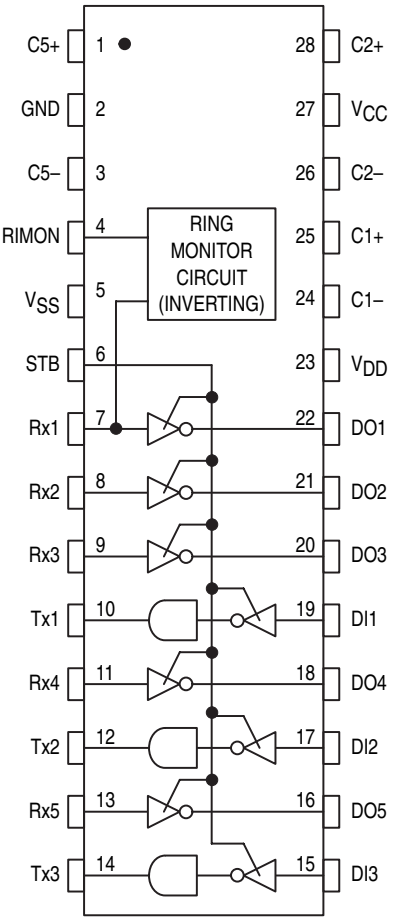
FEATURES

Drivers:
- ± 5 V Minimum Output Swing at 3.3 or 5.0 V Power Supply
- 300 Ω Power–Off Impedance
- Output Current Limiting
- Three–State Outputs During Standby Mode

Receivers:
- ± 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity
- Three–State Outputs During Standby Mode

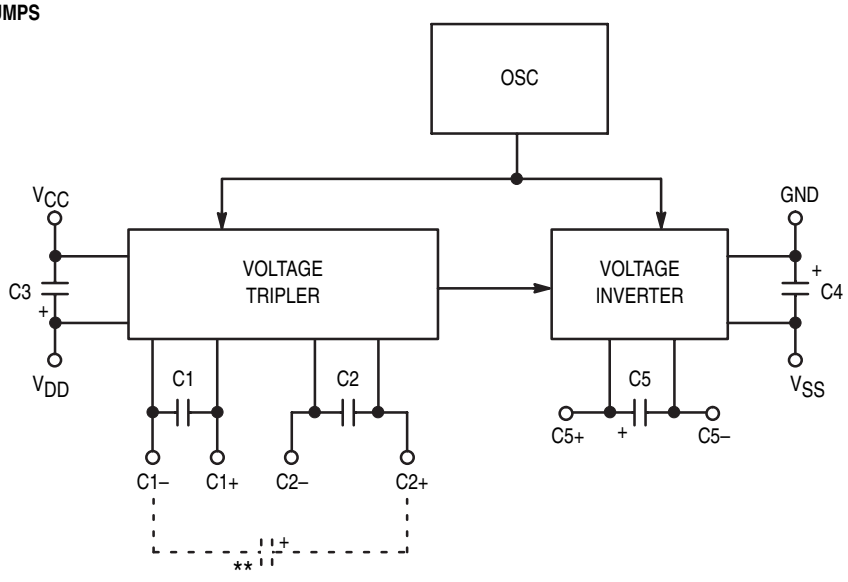
Ring Monitor Circuit:
- Invert the Input Level on Rx1 to Logic Output Level on RIMON at Standby Mode

PIN ASSIGNMENT

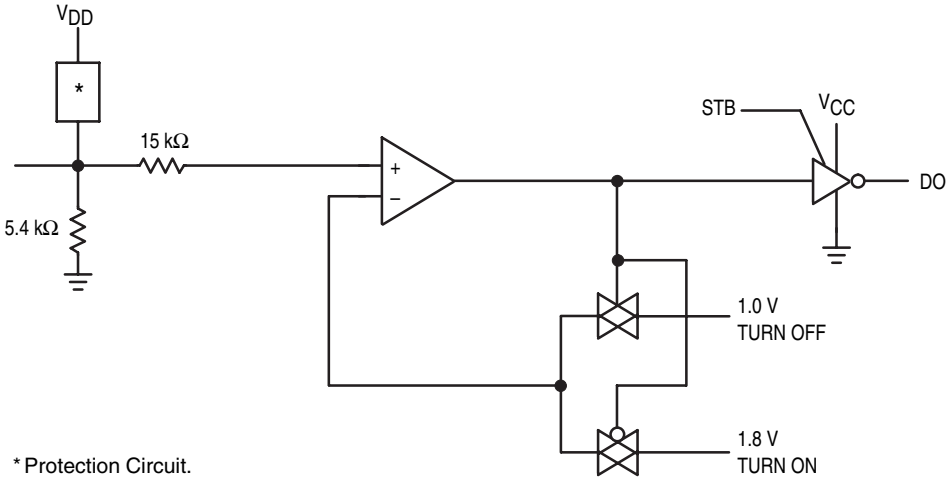


FUNCTION DIAGRAM

CHARGE PUMPS

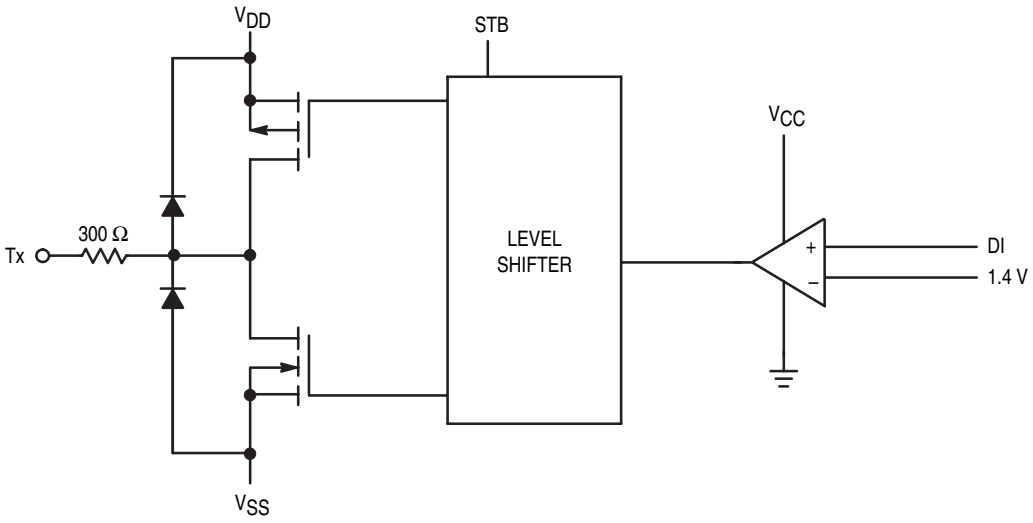


RECEIVER



* Protection Circuit.
** Capacitors C1 and C2 are replaced by a 1 μF capacitor at V_{CC} = 5.0 V supply.

DRIVER



MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to + 6.0	V
Input Voltage Rx1 – Rx5 Inputs DI1 – DI3 Inputs	V_{IR}	V_{SS} – 15 to V_{DD} + 15 – 0.5 to V_{CC} + 0.5	V
DC Current per Pin	I	± 100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that the voltage at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{CC} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the Rx pin should be constrained to (V_{SS} – 15 V) ≤ $V_{Rx1 – Rx5}$ ≤ (V_{DD} + 15 V), and Tx should be constrained to V_{SS} ≤ $V_{Tx1 – Tx3}$ ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC} V_{CC}*	3.0 4.5	3.3 5.0	3.6 5.5	V
Operating Temperature Range	T_A	– 40	—	85	°C

* Capacitors C1 and C2 are replaced by a 1 μF capacitor at V_{CC} = 5 V.

DC ELECTRICAL CHARACTERISTICS (Voltage polarities referenced to GND = 0 V; C1 – C5 = 1 μF; T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supply	V_{CC}	3.0	3.3	3.6	V
Quiescent Supply Current (Output Unloaded, Input Low)	I_{CC}	—	2.8	6.0	mA
Quiescent Supply Current (Standby Mode; STB = 1, Output Unloaded)	$I_{CC(STB)}$	—	< 5	10	μA
Control Signal Input Voltage (STB)	V_{IL} V_{IH}	— V_{CC} – 0.5	— —	0.5 —	V
Control Signal Input Current (STB)	I_{IL} I_{IH}	— —	— —	10 10	μA
Charge Pumps Output Voltage (V_{CC} = 3 V; C1, C2, C3, C4, C5 = 1 μF)					V
Output Voltage (V_{DD}) I_{load} = 0 mA I_{load} = 6 mA	V_{DD}	 8.5 7.5	 8.8 7.9	 — —	
Output Voltage (V_{SS}) I_{load} = 0 mA I_{load} = 6 mA	V_{SS}	— —	– 8.8 – 7.8	– 8.5 – 7.0	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 3.3 V ± 10%; C1 – C5 = 1 μF; T_A = 25°C)

Parameter		Symbol	Min	Typ	Max	Unit
Input Turn–On Threshold ($V_{DO1 – DO5}$ = V_{OL}; Rx1 – Rx5)	3.3 V 5.0 V	V_{on}	1.35 2.00	1.8 2.5	2.35 3.10	V
Input Turn–Off Threshold ($V_{DO1 – DO5}$ = V_{OH}; Rx1 – Rx5)	3.3 V 5.0 V	V_{off}	0.75 1.20	1.0 1.5	1.25 1.80	V
Input Resistance		R_{in}	3	5.4	7	kΩ
High–Level Output Voltage (DO1 – DO5) I_{out} = – 20 μA $V_{Rx1 – Rx5}$ = – 3 to – 25 V I_{out} = – 1 mA		V_{OH}	V_{CC} – 0.1 V_{CC} – 0.6	— 2.7	— —	V
Low–Level Output Voltage (DO1 – DO5) I_{out} = + 20 μA $V_{Rx1 – Rx5}$ = + 3 to + 25 V I_{out} = + 1.6 mA		V_{OL}	— —	0.01 0.5	0.1 0.7	V
Ring Monitor Circuit (Input Threshold)		V_{TH}	—	1.1	—	V
High–Level Output Voltage (RIMON) I_{out} = – 20 μA I_{out} = – 1 mA		V_{OH}	V_{CC} – 0.1 V_{CC} – 0.6	— 2.7	— —	V
Low–Level Output Voltage (RIMON) I_{out} = + 20 μA I_{out} = + 1.6 mA		V_{OL}	— —	0.01 0.5	0.1 0.7	V

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 3.3 V or + 5.0 V ± 10%; C1 – C5 = 1 μF; T_A = 25°C)

Parameter		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI3					V
Logic Low		V_{IL}	—	—	0.7	
Logic High		V_{IH}	1.8	—	—	
Digital Input Current	DI1 – DI3					μA
V_{DI} = GND		I_{IL}	—	7	—	
V_{DI} = V_{CC}		I_{IH}	—	—	± 1.0	
Output High Voltage		V_{OH}				V
Load on All Tx1 – Tx3, R_L = 3 kΩ; C_P = 2500 pF, $V_{DI1 – DI3}$ = Logic Low			5.0	7.0	—	
No Load			8.5	8.8	—	
Output Low Voltage		V_{OL}				V
Load on All Tx1 – Tx3, R_L = 3 kΩ; C_P = 2500 pF, $V_{DI1 – DI3}$ = Logic High			—	– 7.0	– 5.0	
No Load			—	– 8.8	– 8.5	
Ripple (Refer to V_{DD} – V_{SS} Value) ***		V_{RF}	—	—	± 5%	
Off Source Impedance	Tx1 – Tx3	Z_{off}	300	—	—	Ω
Output Short Circuit Current (V_{CC} = 3.3 V or 5.5 V)		I_{SC}				mA
Tx1 – Tx3 Shorted to GND*			—	—	± 60	
Tx1 – Tx3 Shorted to ± 15 V**			—	—	± 100	

* Specification is for one Tx output to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

** This condition could exceed package limitations.

*** Ripple V_{RF} would not exceed ± 5% of (V_{DD} – V_{SS}).

SWITCHING CHARACTERISTICS (V_{CC} = + 3.3 V or + 5 V, ± 10%; C1 – C5 = 1 μF; T_A = 25°C)

Parameter		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1 – Tx3	t_{DPLH}				μs
Low–to–High (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)			—	0.5	1	
High–to–Low (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)		t_{DPHL}	—	0.5	1	
Output Slew Rate (Source R = 300 Ω) Loading: R_L = 3 – 7 kΩ; C_L = 2500 pF	Tx1 – Tx3	SR	± 4	—	± 30	V/μs
Output Disable Time*		t_{DAZ}	—	4	10	μs
Output Enable Time*		t_{DZA}	—	25	50	ms
Receivers						
Propagation Delay Time	DO1 – DO5					μs
Low–to–High		t_{RPLH}	—	—	1	
High–to–Low		t_{RPHL}	—	—	1	
Output Rise Time	DO1 – DO5	t_r	—	120	200	ns
Output Fall Time	DO1 – DO5	t_f	—	40	100	ns
Output Disable Time*		t_{RAZ}	—	4	10	μs
Output Enable Time*		t_{RZA}	—	25	50	ms

* Including the charge pump setup time.

TRUTH TABLES

Drivers

DI	STB	Tx
X	H	Z*
H	L	L
L	L	H

* $V_{SS} \le V_{Tx} \le V_{DD}$ X = Don't Care

Receivers

Rx	STB	DO
X	H	Z*
H	L	L
L	L	H

* GND ≤ V_{DO} ≤ V_{CC} X = Don't Care

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply (Pin 27)

This digital supply pin is connected to the logic power supply. This pin should have a not less than 0.33 µF capacitor GND.

GND
Ground (Pin 2)

Ground return pin is typically connected to the signal ground pin of the EIA–232–E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply (Pin 23)

This is the positive output of the on–chip voltage tripler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply (Pin 5)

This is the negative output of the on–chip voltage tripler/inverter and the negative power supply input of the driver/ receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

RIMON
Ring Monitor Circuit (Pin 4)

The Ring Monitor Circuit will convert the input level on Rx1 pin at standby mode and output on the RIMON pin.

STB
Standby Mode (Pin 6)

The device enters the standby mode while this pin is connected to the logic high level. During the standby mode, driver and receiver output pins become high–impedance state. In this condition, supply current I_{CC} is below 5 µA (typ).

C5+, C5–, C2+, C2–, C1+, C1–
Voltage Tripler and Inverter (Pins 1, 3, 28, 26, 25, 24)

These are the connections to the internal voltage tripler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2, Rx3, Rx4, Rx5
Receive Data Inputs (Pins 7, 8, 9, 11, 13)

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space, and causes the corresponding DO pin to swing to GND (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2, DO3, DO4, DO5
Data Outputs (Pins 22, 21, 20, 18, 16)

These are the receiver digital output pins, which swing from V_{CC} to GND. Output level of these pins is high impedance while in standby mode.

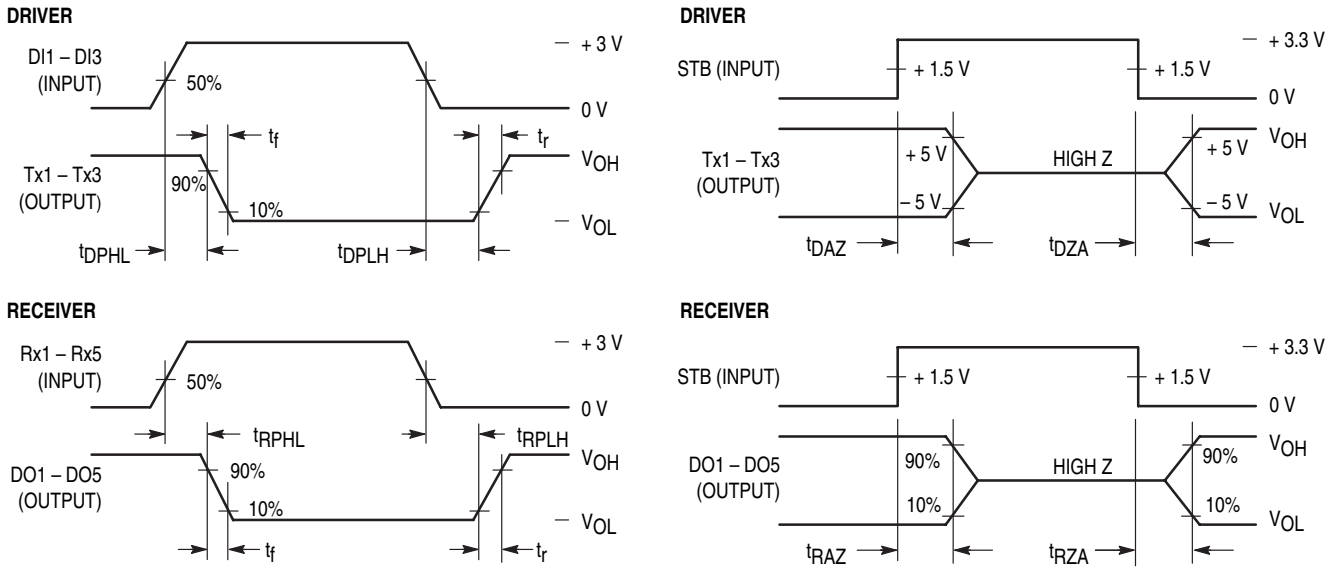
DI1, DI2, DI3
Data Inputs (Pins 19, 17, 15)

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins must be betweenV_{CC} and GND.

Tx1, Tx2, Tx3
Transmit Data Output (Pins 10, 12, 14)

These are the EIA–232–E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. The actual levels and slew rate achieved will depend on the output loading (RL/CL). The minimum output impedance is 300 Ω when turned off.

SWITCHING CHARACTERISTICS



ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes which are designed to do just that. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 1 shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1and C2.

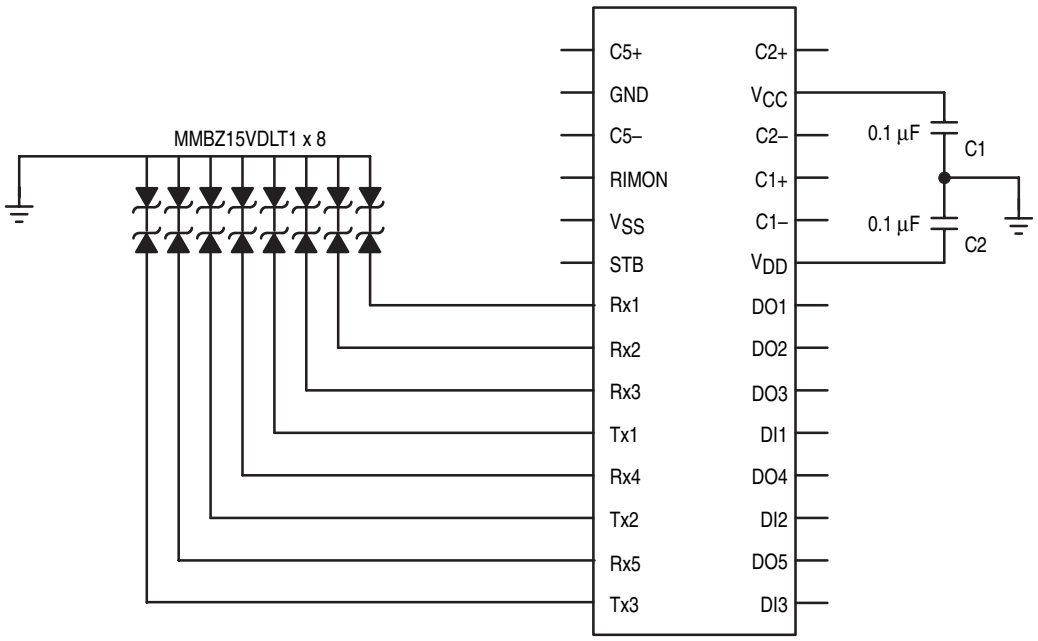
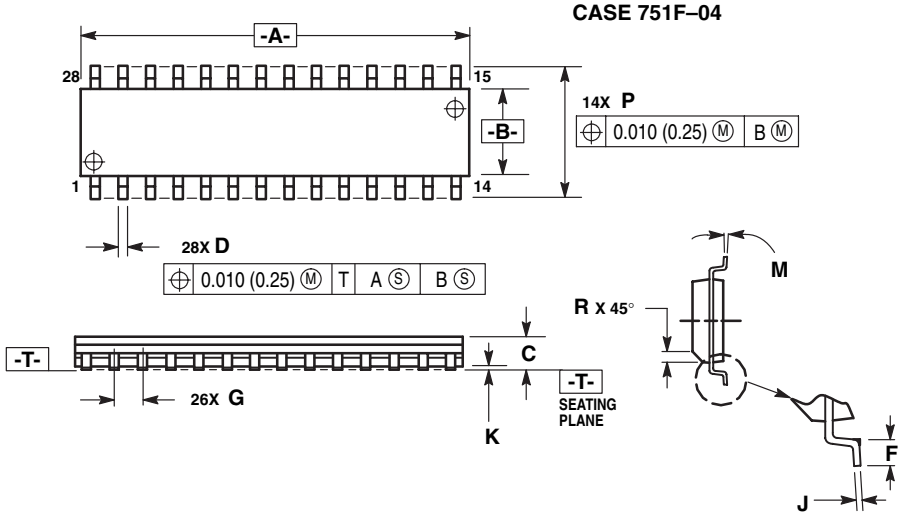


Figure 1. ESD Protection Scheme

OUTLINE DIMENSIONS

SOIC 28W = -7P
(ML145583-7P)
SOG PACKAGE
CASE 751F–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029