ML2200, ML2208

12-Bit Plus Sign Data Acquisition Peripheral

GENERAL DESCRIPTION

The ML2200 and ML2208 Data Acquisition Peripherals (DAP) are monolithic CMOS data acquisition subsystems. These data acquisition peripherals feature an input multiplexer, a programmable gain instrumentation amplifier, a 2.5V bandgap reference, and a 12-bit plus sign A/D converter with built-in sample-and-hold. In addition to a general purpose 8-bit microprocessor interface, the ML2200 and ML2208 include a programmable processor, data buffering, a 16-bit timer, and limit alarms.

The ML2200B and ML2208B self-calibrating algorithmic A/D converters have a maximum non-linearity error over temperature of 0.018% of full-scale, while the ML2200C, ML2200D, ML2208C, and ML2208D have a maximum non-linearity error over temperature of 0.024%.

The ML2200 has a four channel differential input multiplexer and the ML2208 has an eight channel single ended input multiplexer.

The digital interface, with software-alterable configurations, is designed to off-load the microprocessor. Control of the DAP is autonomously handled through the control sequencer which receives its instructions from the instruction RAM.

FEATURES

- Resolution 12-bits + sign
- Conversion time (including S/H acquisition) 31.5µs max
- Sample-and-hold acquisition 2.3µs max
- Non-linearity error ±3/4 LSB and ±1 LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self-calibrating — maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Internal voltage reference 2.5V ± 2%
- Four differential or eight single-ended input channels
- Data buffering (8 word data RAM)
- Programmable limit alarm
- 8-Bit microprocessor interface — interrupt, DMA, or polling
- 16-Bit timer for programmable conversion rates
- Standard hermetic 40-pin DIP

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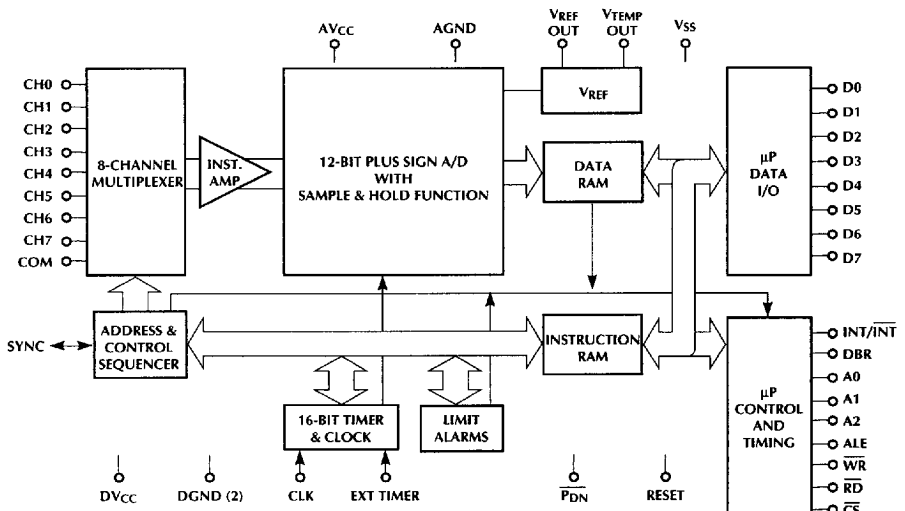
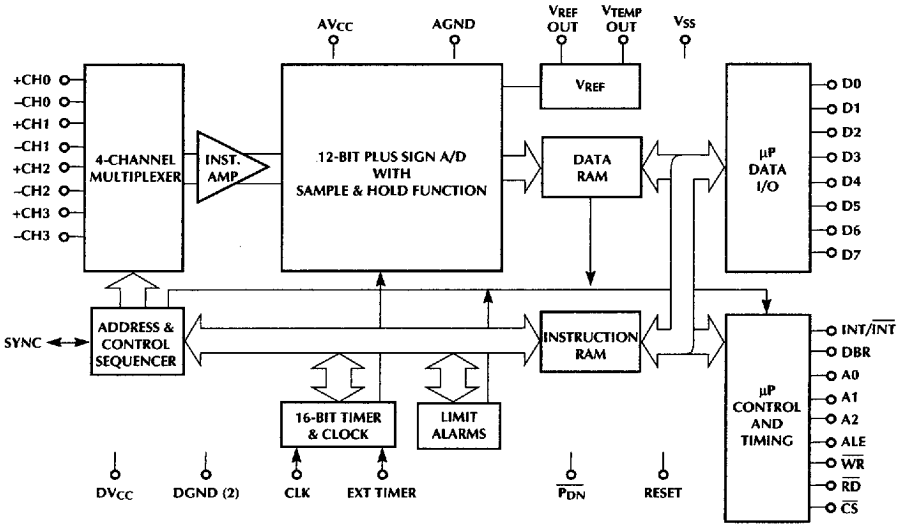
BLOCK DIAGRAM



ML2200 BLOCK DIAGRAM



BLOCK SCHEMATIC DIAGRAM

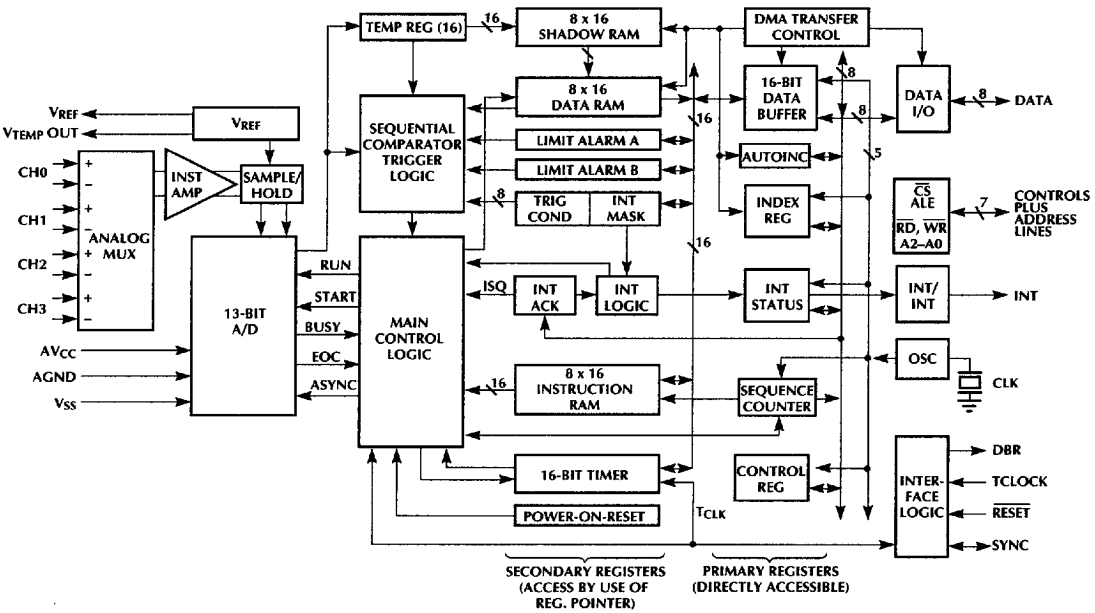


Figure 1. Block Schematic Diagram.

Micro Linear

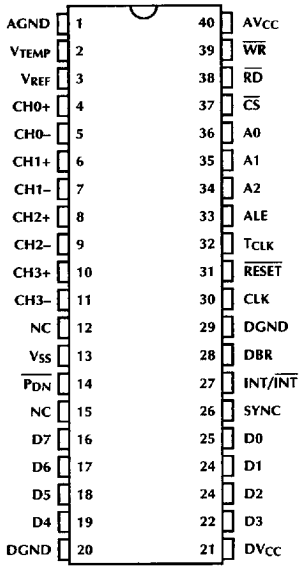
PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	AGND	Analog Ground.
2	V_{TEMP}	Voltage output proportional to the die temperature.
3	V_{REF}	Internal voltage reference output
4-11	CH	Analog Inputs. ML2200 — Positive or negative input of four differential inputs ML2208 — Eight single ended inputs referenced to common pin. Digitally selected by control sequencer.
12	NC COM	ML2200 — No connection. ML2208 — Negative common input for the eight input channels. Tie to analog ground or (V_{SS} +2.5)to (AV_{CC} – 2.5 V)
13	V_{SS}	Negative power supply; decouple to AGND.
14	$\overline{P_{DN}}$	Power-Down Input When $\overline{P_{DN}}$ = 0, device in power-down mode with register contents retained if AV_{CC} >2.0V.
15	NC	No Connection.
16-19	D7, D6, D5, D4	Bidirectional data bits.
20	DGND	Digital Ground.
21	DV_{CC}	Digital power supply. Tie to AV_{CC} from same power supply.
22-25	D3, D2, D1, D0	Bidirectional data bits.
26	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start a conversion. In master mode, SYNC is an output and indicates a conversion has occurred .
27	INT	Interrupt output. A maskable interrupt programmable to be active high or low or will default to active high. INT will not clear until acknowledged in halt mode; not affected by the run or halt state. INT = 0 during reset and inactive during P_{DN}.
28	DBR	Data Buffer Ready output active high indicates that a sequence of operations has completed and data is ready to transfer. DBR is not maskable. It can be used to generate an interrupt in addition to the INT pin when the DBRIE bit in the interrupt mask register has not been enabled. DBR is the DMA request pin when DMA mode is enabled. DBR is not active unless in run mode and at least one sequence of operations has been completed. DBR remains active in the halt mode if not acknowledged; low during reset time and power-down.
29	DGND	Digital Ground.
30	CLK	Clock input. Drive with an external clock or crystal reference to DGND. The crystal must be parallel resonant with minimum capacitive loading (i.e., No bypass caps should be used and leads should be kept short).
31	$\overline{RESET}$	Active low hardware reset with internal pull up resistor of 200K. Tie to system reset line or to grounded capacitor. The capacitor size (usually >6µF) is based on the time the power supplies stabilize, to the time reset voltage reaches 1.4V (>400ms).
32	T_{CLK}	External timer, T_{CLK} is used as external clock input for the 16-bit timer when the T_{CLK} bit in the control register is set to one.
33	ALE	Address latch enable, active low latches information on A0, A1, A2 and $\overline{CS}$. Tie to AV_{CC} to disable use when separate address and data bus are used.
34	A2	Address 2
35	A1	Address 1
36	A0	Address 0
37	$\overline{CS}$	Chip select, active low
38	$\overline{RD}$	Read, active low enables ML2200 or ML2208 to drive data bus.
39	$\overline{WR}$	Write, active low allows writing into the registers.
40	A V_{CC}	Positive analog Power supply. Decouple to AGND. Tie to DV_{CC} from same power supply

PIN CONNECTIONS

ML2200

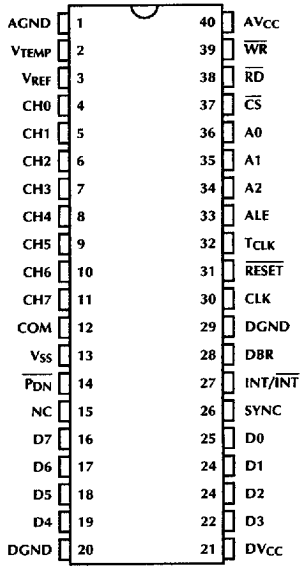
40-PIN DIP



TOP VIEW

ML2208

40-PIN DIP



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... – 6.0V
Voltage at Analog Inputs ..... V_{SS} – 7V to AV_{CC} +7V
Voltage at V_{REF} ..... V_{SS} – 7V to AV_{CC} +7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... – 65°C to +150°C
Package Dissipation @ 25° C 1W
Lead Temperature (Soldering 10 sec.)
Dual-In-Line Package (Plastic) ..... 260°C

OPERATING CONDITIONS

(Note 2)

Temperature Range ..... $T_{MIN} \le T_A \le T_{MAX}$
ML2200BCP, ML2200CCP, ML2200DCP ..... 0°C to 70°C
ML2208BCP, ML2208CCP, ML2208DCP ..... 0°C to 70°C
Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$

ELECTRICAL CHARACTERISTICS

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Converter Characteristics							
	Linearity Error						
	ML2200BCP, ML2208BCP	4	f_{CCLK} = 0.1 ≤ 7MHz			±3/4	LSB
	ML2200CCP, ML2208CCP		f_{CCLK} = 0.1 ≤ 7MHz			±1	LSB
	ML2200DCP, ML2208DCP		f_{CCLK} = 0.1 ≤ 5MHz			±1	LSB
	Unadjusted Zero Error						
	ML2200BCP, ML2208BCP	4				±3/4	LSB
	ML2200CCP, ML2208CCP					±2	LSB
	ML2200DCP, ML2208DCP					±2	LSB
	Unadjusted Positive and Negative Full Scale Error	5				±4	LSB
	Zero Error Temperature Coefficient				0.5		ppm/°C
	Gain Temperature Coefficient		External Reference		3		ppm/°C
	Common-Mode Rejection	13			80		dB
	Analog Input Range	5	All Analog Inputs	V_{SS} – 0.05		AV_{CC} + 0.05	V
	External Source Resistance for Analog Inputs	5	Channel = Analog Input Channel = Voltage Reference			2 0.5	kΩ kΩ
	Differential Analog Input Range		CHX referred to COM for ML2208 CHX+ referred to CHX– for ML2200	$–V_{REF}$		$+V_{REF}$	V
	Off Channel Leakage Current	5, 6	On Chan = 2.5V, Off Chan = –2.5V On Chan =–2.5V Off Chan = 2.5V	–100		 +100	nA
	On Channel Leakage Current	5, 6	On Chan = –2.5V, Off Chan = 2.5V On Chan = 2.5V Off Chan = –2.5V	–100		 +100	nA
	Gain Error		Gain = 2, 4, or 8		0.03		%
Voltage Reference and V_{TEMP} Characteristics							
	V_{REF} Absolute Value	4	Referred to AGND	2.45		2.55	V
	V_{REF} Output Pin						
	Output Resistance	5				300	mΩ
	Minimum Load Resistance	5		1			kΩ
	Maximum Load Resistance	5				50	pF
	Temperature Coefficient				50		ppm/°C
	Line Regulation		4.75 ≤ AV_{CC} ≤ 5.25		1		mV
			–4.75 ≥ V_{SS} ≥ –5.25		1		mV
	Load Regulation		1µA – 2.5mA		1		mV
	Output Noise				100		$µV_{RMS}$
	V_{TEMP} Output Pin				AV_{CC} – 1.5		
	Absolute Value @ 25°C						
	Volts per °C				5		mV/°C

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ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DC Characteristics							
	Power Supply Current						
	AI_{CC}, Analog AV_{CC}	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}		30	50	mA
	DI_{CC}, Digital DV_{CC}	12			10		µA
	I_{SS}, V_{SS}	4			18	30	mA
I_{CC}	Standby Current AI_{CC} + DI_{CC}	4, 9	$\overline{P_{DN}}$ pin = GND		10	1000	µA
I_{SS}	Standby Current				10	1000	µA
	V_{CCPD} Minimum AV_{CC} and DV_{CC} for power-down data retention		$\overline{P_{DN}}$ pin = GND V_{SS} = –5.25 to GND	2			V
	Power Supply Rejection	7					
	AV_{CC}/DV_{CC}		DC		80		dB
			DC to 25kHz, 200mV_{P-P}		50		dB
	V_{SS}		DC		80		dB
			DC to 25kHz, 200mV_{P-P}		50		dB
V_{IL}	Input Low Voltage (except CLK, t_{CLK})	4				0.8	V
V_{IL1}	Input Low Voltage (CLK, t_{CLK})	4				0.8	V
V_{IH}	Input High Voltage (except CLK, t_{CLK})	4		2.0			V
V_{IH1}	Input High Voltage (CLK, t_{CLK})	4		3.5			V
V_{OL}	Output Low Voltage	4	I_{OL} = 2.0mA			0.45	V
V_{OH}	Output High Voltage	5	I_{OH} = –1mA	4.0			V
I_L	Input Leakage Current (except CLK and RESET)	4	GND < V_{IN} < V_{CC}			±10	µA
I_{L1}	Input Leakage Current (CLK)	4	GND < V_{IN} < V_{CC}			±200	µA
I_{L0}	Output Leakage Current (D0 – D7)	4	$\overline{RD}$ = $\overline{CS}$ = V_{IH}			±10	µA
I_{RST}	RESET Pin Source Current	4	$\overline{RESET}$ = 0V	15	50	100	µA
C_I	Input Capacitance (All Digital Inputs)				10		pF
C_O	Output Capacitance (All Outputs and D0 – D7)				20		pF
AC Electrical Characteristics (Note 8)							
t_C	Conversion Time	4, 9	CLK Mode = 0, f_{CLK} = 7.0MHz	31.5			µs
			CLK Mode = 0, f_{CLK} = 5.0MHz	44.0			µs
	Sample and Hold Acquisition	4, 9	CLK Mode = 0, f_{CLK} = 7.0MHz			2.3	µs
			CLK Mode = 0, f_{CLK} = 5.0MHz			3.2	µs
SNR	Signal-to-Noise Ratio		V = 10kHz, 2.5V Sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). Noise is sum of all nonfundamental components up to 1/2 of $f_{SAMPLING}$.		73		dB
THD	Total Harmonic Distortion		V = 10kHz, 2.5V Sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). THD is sum of 2, 3, 4, 5 harmonics relative to fundamental.		–75		dB

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = +5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, AGND = DGND = COM = CHX– = 0V, $T_A = T_{MIN}$ to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
AC Electrical Characteristics (Note 8) (Continued)							
IMD	Intermodulation Distortion		$V_{IN} = f_A + f_B$. f_A = 9kHz 1.25V sine. f_B = 10kHz, 1.25 sine. f_{CLK} = 7MHz ($f_{SAMPLING}$ = 31.8kHz). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A - f_B)$, $(2f_A + f_B)$, $(f_A - 2f_B)$ relative to fundamental.		–75		dB
FR	Frequency Response		V_{IN} = 0 to 10kHz, 2.5V sine relative to 1kHz		0.01		dB
f_{CLK}	CLK Frequency	4	(No crystal)	0.1		7	MHz
f_{CLKX}	CLK Frequency	4	(Crystal)	3		7	MHz
f_{CLKI}	Internal CLK Frequency				1/2		f_{CLK} or f_{CLKX}
f_{CLKT}	CLK Frequency (t_{CLK} only)	4				f_{CLKI}	MHz
f_{CLKW}	Minimum Clock High/Low Width (CLK)	5		50			ns
f_{CLKWT}	Minimum Clock High/Low Width (t_{CLK})	5		75			ns
t_{RF}	Maximum Rise/Fall Times, All Inputs	5				25	ns
t_{RESET}	Minimum Reset Active Time	4, 10		10			f_{CLK} Periods
t_{PDN}	Power-Up Time		Time After $P_{DN} = V_{IH}$		1		ms
Non-Multiplexed Data Bus Timing							
t_{AL}	Address to ALE Setup Time	4		20			ns
t_{LA}	Address Hold Time After ALE	4		20			ns
t_{LC}	Latch to RD or WR Control	4		20			ns
t_{RD}	Valid Data Delay from Read	4				150	ns
t_{AD}	Address Stable to Valid Data	5		150			ns
t_{LL}	ALE Width	4		80			ns
t_{DF}	Data Bus Float After Read	4		10		50	ns
t_{CL}	Read or Write Control to ALE	4		20			ns
t_{CC}	Read or Write Control Width	4		150			ns
t_{DW}	Data Setup Time for Write	4		100			ns
t_{WD}	Data Hold Time for Write	4		0			ns
t_{RV}	Recovery Time Between Two Reads or Writes	4		250			ns
t_{AD}	Address Stable to Valid Data	5		150			ns
t_{AR}	Address Stable Before Read	4		0			ns
t_{RA}	Address Hold Time for Read	4		0			ns
t_{RR}	Read Pulse Width	4		150			ns
t_{RD}	Data Delay from Read	4				150	ns
t_{DF}	Read to Data Float	4		10		50	ns

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply for AV_{CC} = DV_{CC} = +5V ± 5%, V_{SS} = –5V ± 5%, AGND = DGND = COM = CHX– = 0V, T_A = T_{MIN} to T_{MAX} unless otherwise specified. C_L = 100pF for D0–D7, C_L = 50pF for INT, DBR, and SYNC.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
Non-Multiplexed Data Bus Timing							
t_{RV}	Recovery Time Between Two Reads or Writes	4		250			ns
t_{AW}	Address Stable Before Write	4		0			ns
t_{WA}	Address Hold Time for Write	4		0			ns
t_{WW}	Write Pulse Width	4		150			ns
t_{DW}	Data Setup Time for Write	4		100			ns
t_{WD}	Data Hold Time for Write	4		0			ns
DMA Interrupt and SYNC Timings							
t_{CKDBR}	Clock to DBR Assert	11, 4	DMA		120	190	ns
t_{RDD}	Read to DBR Negation on Last Byte	4			110	170	ns
t_{CKDBR}	Clock to DBR or t_{CKINT}, INT Assert	11, 4	Non-DMA		100	180	ns
t_{WRDBR}	Write to DBR or t_{WRINT} INT Negation	11, 4			70	120	ns
t_{CKSYNC}	Clock to SYNC Delay	11, 4	Master Mode		150	220	ns
t_{SYNCN}	SYNC Input Width	5		3			f_{CLKI}
t_{SYNCCK}	SYNC to Clock Setup	4	Slave: Mode 4 Only	50			ns
t_{SYNCO}	Minimum SYNC Output Width	4		4		4	f_{CLKI}

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: 0°C to +70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Leakage current is measured with the clock not switching.
Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.
Note 8: All parameters measured from 0.8V to 2.0V.
Note 9: Power-down current is with power-down pin at GND potential only. Any other level will dissipate more power. Other digital input pins may float but cannot be above VDD or below GND.
Note 10: RESET should be held active for at least 10 internal clocks after power supplies have stabilized to within 5% of 5V.
Note 11: Since the internal master clock is the input clock divided by 2, this number can be either the maximum listed or the maximum listed plus 1/2 the input clock period.
Note 12: When RD = CS = V_{IL}, the current into the DV_{CC} pin depends on the data bus pins D0 – D7.
Note 13: Common-Mode rejection is the ratio of the change in zero error to the change in common-mode input voltage.

TIMING DIAGRAMS

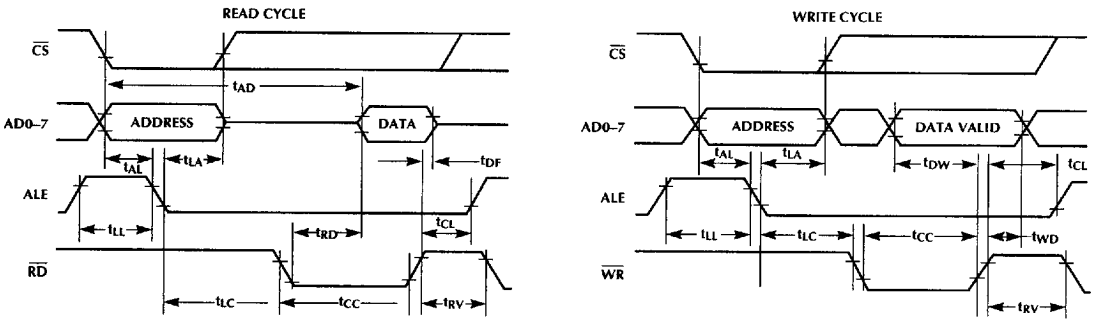


Figure 2. Multiplexed Bus.

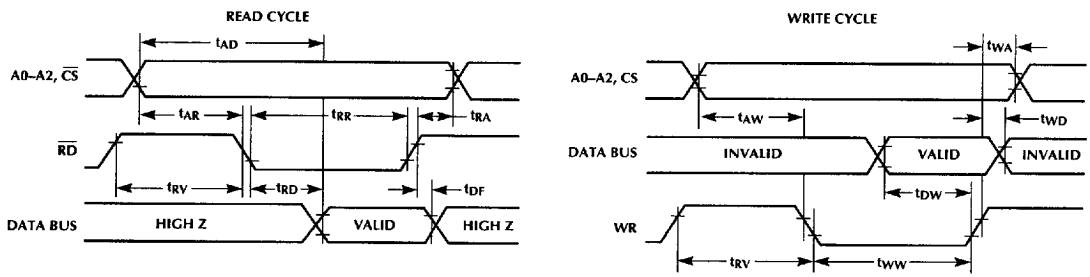
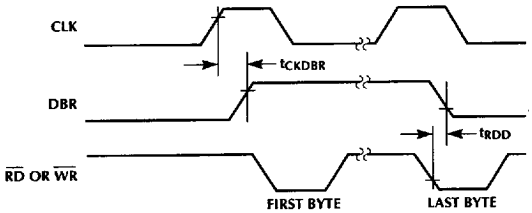


Figure 3. Non-Multiplexed Bus.

TIMING DIAGRAMS (Continued)



Note: There are 2*n Read Operations where n is the number of words to be transferred. DBR is set and cleared by internal circuitry. DMA bit in the control register must be set for this operation.

Figure 4. DMA Mode.

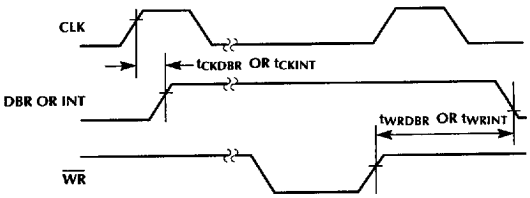


Figure 5. DBR and INT (Non-DMA Mode).

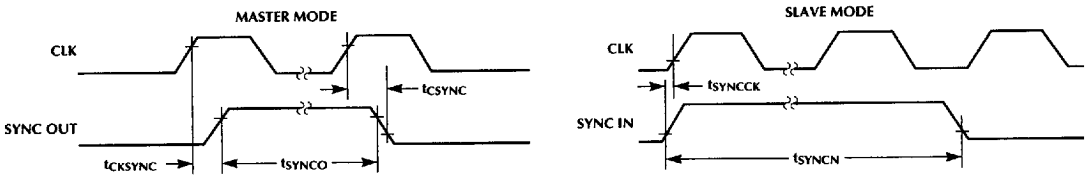


Figure 6. SYNC

1.0 FUNCTIONAL DESCRIPTION

1.1 ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feed back the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

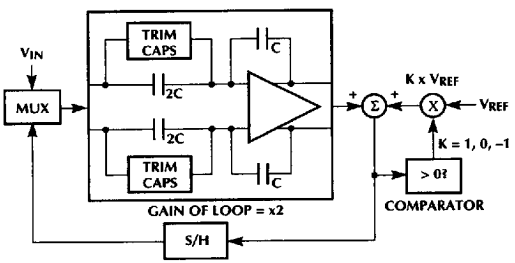


Figure 7. Self Calibrating A/D Converter.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample-and-hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample-and-hold. This process repeats again, however now the sample-and-hold voltage is multiplied by 2.

Self-Calibration

In order to maintain integral and differential linearity to the ½ LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2x amp. The gain of the loop is adjusted using self-calibration .

Self-calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full-scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0" . If the magnitude bits of the resulting conversion are all "1s",

the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13-bit accuracy of 2.

1.2 MULTIPLEXER INPUT

The input voltage is ±2.5V relative to COM of the ML2208 or a CH– of the ML2200. The input voltages under normal operation must not exceed supply voltages by 0.05V. Each channel is selected by the programmable sequencer.

1.3 INTERNAL VOLTAGE REFERENCE AND V_{TEMP}

The internal bandgap voltage reference with a temperature coefficient of 50 ppm /°C has an external use current of 2.5mA.

The voltage reference V_{TEMP} output is directly proportional to the chip temperature.

1.4 CONVERSION TIMES

The following table lists the conversion times which include the sample-and-hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

Operation	Number of Internal Clocks*
8-bit A/D	80
13-bit A/D	110
CALWR	52
CALRD	80

*Internal clock is the external clock divided by two.

1.5 SAMPLE-AND-HOLD TIMING

Figure 8 shows the internal timing for the sample-and-hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks, regardless of the Start Mode. Six internal clocks after the Start of Conversion, the Sample-and-Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the input pins; one on CH+ and one on CH– for the ML2200, and CH and COM for the ML2208. The sample switch is kept in the sample mode for 8 internal clocks (2.3µs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample-and-hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion. SYNC is activated one internal clock cycle before the Start of Conversion and lasts for four internal clocks.

1.6 ANALOG INPUTS DIFFERENTIAL INPUTS AND COMMON-MODE REJECTION

The differential inputs of the ML2200 eliminate the effects of common-mode input noise (60Hz, for example), as CH+ and CH– are sampled at the same time.

Noise

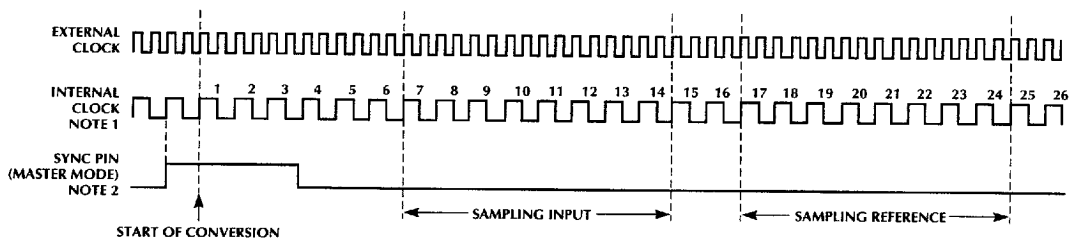
The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

Power Supply Decoupling

Low inductance tantalum capacitors of 1µF or greater and 0.01µF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

2.0 µP HARDWARE INTERFACE

The microprocessor interface is a byte-oriented structure which occupies eight memory or I/O locations in the microprocessor's address space. Each register is readable and writable via the chip select, read and write pins, three address lines, and 8-bit data bus.



Note 1: External clock in phase with internal clock using RESET.
Note 2: Immediate execute mode where start of conversion and start of operation occur at the same time.

Figure 8. Sample-and-Hold Timing.

Interfaces are shown for multiplexed address data bus in Figure 9 and Figure 10. When non-multiplexed interfaces are used, ALE can be tied high. All internal address and chip select latches are transparent.

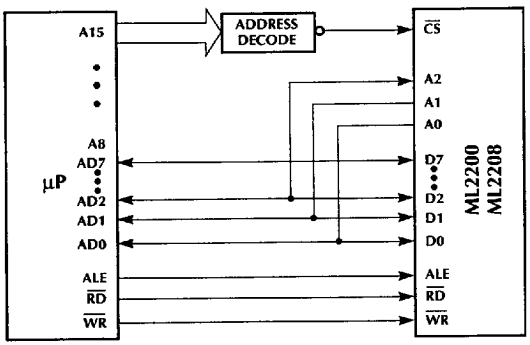


Figure 9. 8-Bit Multiplexed Bus Interface.

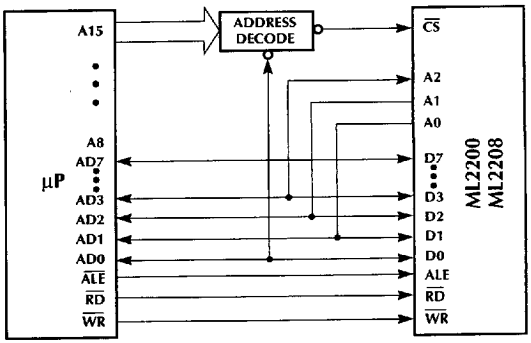


Figure 10. 16-Bit Multiplexed Bus Interface.

2.1 INTERRUPTS

The ML2200 and ML2208 provide two interrupt pins, one for control/status interrupts (INT), and one for data interrupts (DBR). The standard INT pin is maskable via an interrupt mask register while the DBR pin is always enabled to signify that data is available. DBR can be mapped into the INT pin if only one interrupt pin is desired.

The interrupt pin (INT) can be programmed, via the Interrupt Bit Mask register, to be active high, or active low. When programmed for active high, it is driven in both directions. When INT is programmed for active low, it is an open drain output, therefore an external pull-up resistor of 2.5 kΩ or more should be used. The DAP's Status register can be read to determine whether its interrupt is active or not.

2.2 DMA

The separate DBR pin can also serve as a DMA request signal when DMA operation is enabled in the Control register. DBR goes active high when the data buffer is full and ready to be read. DBR remains high until the last byte in the data buffer has been read. This allows back-to-back DMA cycles or single cycle transfers depending on how the DMA controller is programmed. The data for the DMA cycle is transferred over the 8-bit data bus at address 0 (A0 – A2 =0). The ML2200 or ML2208 automatically places both high and low bytes of the 16-bit wide data buffer at address 0 or 1 for the DMA controller to read. The LOBYT bit in the Control register specifies whether the high or low byte is placed on the bus first. Figure 11 shows a block diagram interfacing to the 8237 DMA controller.

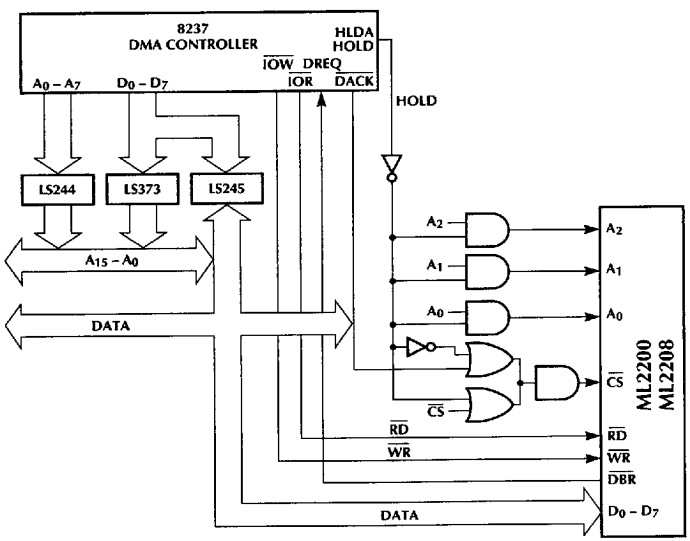


Figure 11. DMA Interface.

Micro Linear

3.0 REGISTER DEFINITIONS

These data acquisition peripherals contain six directly addressable 8-bit registers, and twenty indirectly addressable 16-bit registers. Figure 12 illustrates the register architecture while Figures 13, 14 & 15 illustrate the bit maps and addresses. The first three primary registers (Window Low, Window High, and Index) are used to access the 20 secondary registers. Window Low and Window High provide read /write access to the low and high bytes of the secondary register pointed to by Index.

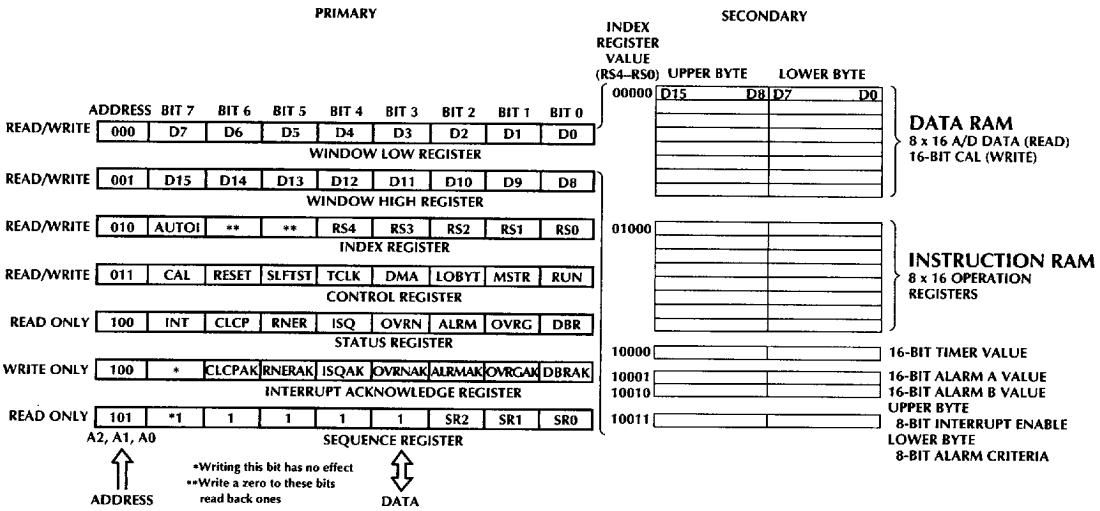


Figure 12. Register Architecture.

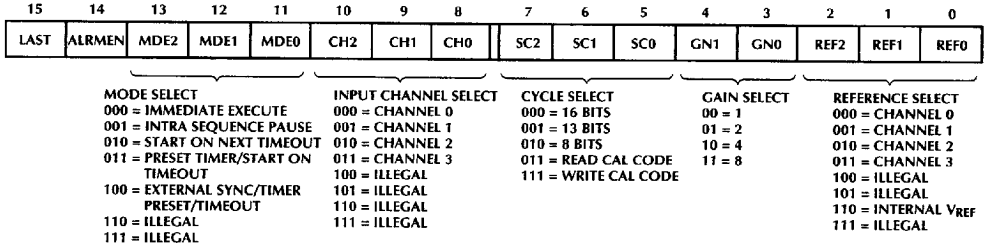


Figure 13. ML2200 Bit Map of Instruction RAM.

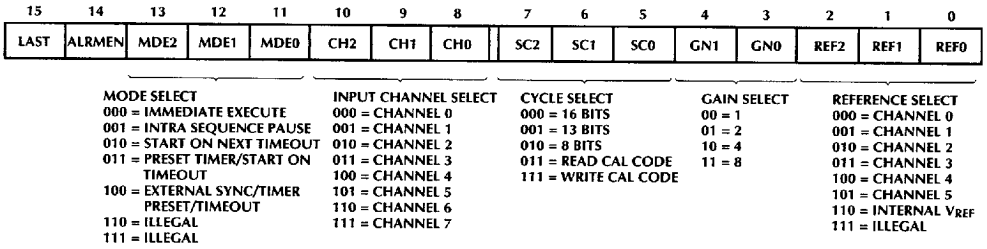


Figure 14. ML2208 Bit Map of Instruction RAM.

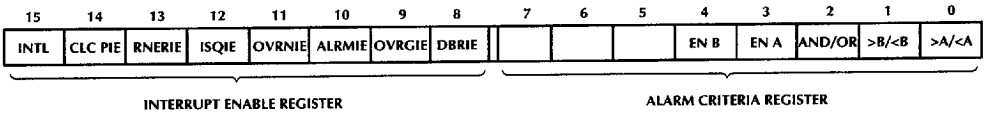


Figure 15. Interrupt Enable and Alarm Criteria Registers.

3.1 Primary Registers

READ/ WRITE

D7	D6	D5	D4	D3	D2	D1	D0

Window Low Register

READ/ WRITE

D15	D14	D13	D12	D11	D10	D9	D8

Window High Register

Window Registers— Registers 0 and 1

These registers form a two-byte window into the secondary registers. Window Low is the low byte of the secondary 16-bit word, and Window High is the high byte. Any one of the 20 words in the secondary register set can be accessed by first setting a 5-bit address in the Index register, then reading from or writing to the Window registers. Sequential access of the secondary registers is also available without writing to the Index register via the AUTOI bit in the Index register.

Index Register — Register 2

READ/ WRITE

AUTOI			RS4	RS3	RS2	RS1	RS0

Index Register

RSX = Secondary Register Address (Bits 0 to 4): The lower five bits of this register (RSO – RS4) define the location within the secondary register set that the window registers are positioned at.

Bits 5 and 6: Undefined. Writing to these bits have no effect, however a zero should be written; always read as ones.

AUTOI = autoincrement (Bit 7): Setting AUTOI signifies that the lower five addressing bits in the Index register are automatically incremented after either the Window Low or Window High register is accessed. Whether the autoincrement occurs when accessing Window Low or Window High register, is based on the LOBYT bit in the Control register.

Interrupt Operation Caution!!! — Using the autoincrement feature with interrupt driven software deserves special attention. A problem can arise when an interrupt service routine accessing the secondary registers, interrupts another routine accessing secondary registers. This problem can be avoided one of two ways: disable the interrupt in the main routine while accessing secondary registers, or reload the index register to its entry value when exiting the interrupt routine.

Note: The Index register is automatically cleared only under two conditions, one is a RESET, the other is when mode is used. This register is reset to 0 in DMA mode just prior to the DMA request (DBR going active). DMA mode uses the index register for operation, so the index register should never be written to when RUN and DMA are set.

Control Register — Register 3

READ/ WRITE

CAL	RESET	SLFTST	t_{CLK}	DMA	LOBYT	MSTR	RUN

Control Register

RUN (Bit 0): Setting this bit to a one will cause the chip to start executing the operations defined in the Instruction RAM, beginning with location 0. This is referred to as the Run mode. Clearing this bit will place the ML2200 in the Halt mode. The run bit is initially cleared on power up or after a hardware or software reset. In order to properly start the chip operation, the RUN bit should be set after setting all other applicable bits in the control register. The act of halting the chip will always reset the sequence pointer to operation 0. Thus, the next time RUN is asserted, the chip starts from operation 0 again. Placing the chip in the Run or Halt mode has no effect on the Interrupt pins (INT and DBR), nor the status bits in the status register. It is recommended that secondary registers only be written to in the Halt mode. Writing to secondary registers in the Run mode will cause the RNER status bit to be set, indicating a run error. All of the status bits in the Status register should be acknowledged (cleared) before entering the Run mode.

MSTR = master (Bit 1): Indicates whether the SYNC pin will be an input or an output. If set the chip will enter the master mode of operation and the SYNC pin will become an output pin which puts out a sync pulse at the beginning of each operation. This serves as a signal for other slave chips that are used in a synchronous operating method. While in master mode, any operation requiring a sync input will not proceed, and the chip will "hang", waiting for a sync that will never come. The chip default is slave mode with the SYNC pin as an input.

LOBYT = low byte first (Bit 2): This bit is used to indicate which byte is accessed first in AUTOI or DMA operation. When this bit is set, the index register is incremented on the read or write of the Window High register. When this bit is clear, the index register is incremented on the read or write of the Window Low register. If DMA operation is specified, then setting this bit will make the low byte be output first, then the high byte, after which the index register is incremented. Conversely, clearing this bit will output the high byte first, then the low byte, then increment the index register. The default is low.

DMA = DMA Mode (Bit 3): When set enables DMA operation. DMA operation proceeds as follows:

1) The DMA bit must be set after defining all other registers (Instruction RAM, Alarm etc.) but prior to setting the RUN bit. The RUN bit is then set.

2) The sequence of operations in the Instruction RAM is executed.

3) At the end of the sequence, the DBR pin goes true, requesting DMA service, and the Index register is automatically cleared, pointing to the first location of the data buffer.

4) Each read of either Window Low or Window High register outputs a byte from the data registers. The DMA controller can read Window Low register, or Window High register, or alternate between Window Low and Window High. The same data is placed in both Window Low and Window High registers, and updated in both of them when either one is read. The data is placed in the Window registers beginning with data word 0 and incrementing on up. The placement of the low byte/ high byte order is based on the LOBYT bit in the Control register. The number of bytes transmitted equals twice the number of operations defined, since the words are 16-bits going over an 8-bit bus. DBR remains asserted until all of the bytes have been transmitted. It is negated on the leading edge of the last byte read pulse. DBR acknowledge (setting the DBRAK bit in the Status register) is not required when transferring bytes via DMA.

The AUTOI bit does not have to be set when in the DMA mode. Setting the DMA bit forces the Index register to be auto-incremented in the Run mode. However if AUTOI is not set, then when in Halt mode autoincrement will not be enabled. If the AUTOI bit and DMA bit are both set, the autoincrement will occur in both the Run mode and the Halt mode.

t_{CLK} = enable external timer clock (Bit 4): When set, will divert the clock input for the internal sixteen bit timer to the t_{CLK} pin. When reset to 0, the timer runs at the internal chip clock frequency, which is ½ of that generated at the CLK pin.

SLFTST = self test (Bit 5): When set, the function of the input multiplexer is modified to enable self test operations. This bit also redefines the Instruction Word, specifically the CHAN field of the instruction word (See Figure 16 for the redefinition of the Instruction Word when SLFTST = 1). With SLFTST set the CHAN bits now specify which of four self tests is to be performed as shown below.

Instruction Word CHAN Field	Function	Description
000	System Offset	Inputs shorted together and shorted to ground
001	Internal Reference	Convert internal V_{REF}, plus side tied to V_{REF}, minus side tied to AGND
010	Minus Internal	Convert internal V_{REF}, Reference minus side tied to V_{REF}, plus side tied to AGND
011	Common Mode	Both inputs of the converter are tied to V_{REF}
100-111	Illegal	

These self-test results are useful for user confidence at power on. The default on reset is 0, normal mode of operation.

RESET = soft reset (Bit 6): Is a software reset of the chip. This bit does not have to be cleared once set. The microprocessor should read this bit back to determine if the reset operation has completed, especially if a slow clock rate is being used. It takes at least 4 internal clocks for the reset bit to clear. Microprocessor communication with the chip should be held off until this bit is read back as cleared. When issuing a hardware reset, communication with the chip should be held off until the $\overline{RESET}$ pin goes inactive. The chip will be in the Halt mode (RUN bit cleared) after a reset. See RESET/Power-On Conditions (Section 4.2) for chip register conditions after a reset.

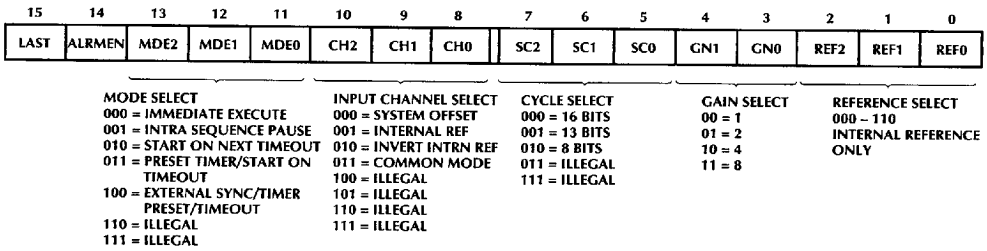


Figure 16. Bit Map of Instruction Word When SLFTST = 1.

CAL = calibration start (Bit 7): When set, a self-calibration of the A/D converter will begin. Reading the CAL bit indicates whether the chip has been calibrated since the last reset or power-on condition. If CAL is a 1, then a calibration of the A/D converter has been performed since the last reset or power-up. When setting CAL, the user should not write a 0 back to clear it. ***Writing a 0 to the CAL bit has no effect;*** this will not clear it if it was previously set. Attempting to set the RUN bit without this bit being set will result in a run error condition, in which the RNER status bit will be set, and an interrupt being generated if it was enabled in the mask register. The amount of time required for calibration is 8,260 internal clocks, or 16,520 external clocks. To determine when a calibration is complete, the microprocessor should enable the calibration complete interrupt (CLCPIE) in the interrupt mask register, and wait for the interrupt to occur. Interrupt servicing of the calibration complete interrupt is done in a normal manner, in which the interrupt is acknowledged by setting the CLCPAK bit in the interrupt acknowledge register. All I /O to the ML2200 should be avoided during calibration (i.e., 16,520 external clocks after the CAL bit is set), because accessing the chip during calibration could adversely affect the calibration. If an interrupt is not desired, the microprocessor can read the Status register to verify completion 16,520 external clocks after the CAL bit is set. When the CAL bit is set, all other bits in the Control register should be cleared. DO NOT set the CAL and RUN bits simultaneously.

Status Register — Register 4

READ ONLY

INT	CLCP	RNER	ISQ	OVRN	ALRM	OVRG	DBR

Status Register

Register 4 serves as the status register of the various conditions that can occur. The bits in the Status register will be updated regardless of the Mask register. The status bits are updated any time within or at the end of a sequence of operations. The bits in the Status register are cleared by setting the corresponding bits in the Interrupt Acknowledge register. The status register can be polled at any time without fear of clearing the status bits. This register is not cleared at HALT time. When entering the Run mode, all of the old status bits should be cleared (acknowledged).

DBR = Data Buffer Ready (Bit 0): Is set when the chip has gone through one complete sequence of operations and has filled the data registers with the converted results. This bit signifies that the microprocessor should read all locations in the data registers that have relevant data. Reading all loaded data locations will clear DBR. If all loaded data locations are not read, DBRAK in the Interrupt Acknowledge register should be set to clear DBR, else OVRN will be set. The DBR pin is logically the same as the DBR status bit. The DBR pin is ALWAYS enabled and cannot be masked out. The DBR status bit is the only condition that can cause the DBR pin to be asserted. The DBR status bit can be enabled to assert the INT pin through the Interrupt Mask register.

OVRG = overrange interrupt (Bit1): Is set at the end of an operation when an underflow or overflow of the A/D converter has occurred (underflow and overflow are the most negative and most positive number, respectively, that is representable in the chip according to the specified cycle length). The overflow and underflow conditions apply to ALL incoming A/D converted data.

ALRM = limit alarm (Bit 2): Is the limit alarm status bit. It is set whenever the alarm criteria specified in the alarm registers is satisfied by a conversion from an operation where the ALRMEN bit is enabled. The limit alarm test only applies to an operation in which the ALRMEN bit is set.

Note that OVRG and ALRM can be enabled without enabling the DBR interrupt so that the microprocessor can be left alone until an overflow/underflow or limit alarm occurs. This is done to search for a limit condition first without taking any data into the microprocessor. Doing this, however, will set the OVRN (overrun error) bit in the status register, indicating that the microprocessor has not read any data from previous sequences.

OVRN = overrun error (Bit 3): The OVRN bit indicates that the microprocessor has missed from one byte to several blocks of data. Even if an overrun error occurs, the ML2200 or ML2208 continues converting the inputs and updating the data registers with the new conversions.

This bit may intentionally become set as a result of searching for the overflow/underflow or limit alarm criteria without reading the data.

The setting of the OVRN bit also occurs in DMA mode if all data has not been read by the completion of the next sequence. (Note: DBRAK should not be set in DMA mode, since DBR is automatically cleared by the chip.) If OVRN occurs in DMA mode, DBR will not be reactivated once all of the data from the sequence which was overrun is read; OVRN automatically disables DBR reactivation. Acknowledging OVRN (setting OVRNAK in the Interrupt Acknowledge register) will re-enable the DBR pin, however the OVRN bit may immediately be set again before the DMA controller can read the entire buffer. Therefore, it is recommended that in DMA mode if OVRN gets set, put the ML2200 or ML2208 in the Halt state, acknowledge the overrun and the DBR, then place the chip back in the Run mode.

ISQ = intra-sequence pause (Bit 4): Indicates that the chip has halted operation within a sequence as a result of choosing the ISQ op code in the mode field of the Instruction word. Setting the ISQAK bit in the interrupt acknowledge register will then restart the operation within the sequence. This lets the microprocessor achieve timing control of individual operations within a sequence.

RNER= run error (Bit 5): Indicates that an error occurred either entering or operating in the Run state. The following operational errors cause the RNER bit to get set

1. Entering the Run state without having performed a self-calibration after the most recent Reset or power-up. The status of whether a calibration was executed or not is indicated by the CAL bit in the control register. If the CAL bit in the Control register is a one, the chip has already been calibrated.
2. Writing to any secondary registers other than the data registers during Run mode. All secondary register locations are readable during Run time.

CLCP = calibration complete (Bit 6): Is set at the end of a calibration sequence. The purpose of this bit is to notify the microprocessor that a self-calibration has completed.

INT = interrupt (Bit 7): Is identical to the state of the INT pin. The INT status bit and pin is an OR of the status bits enabled in the Interrupt Mask register. While the polarity of the INT pin can be defined in the interrupt mask register, this bit is positive true only.

Interrupt Acknowledge Register — Register 4

WRITE ONLY

	CLCPAK	RNERAK	ISQAK	OVRNAK	ALRAK	OVRGAK	DBRAK

Interrupt Acknowledge Register

The status bits in the status register can only be cleared by setting the appropriate bit in this register; writing a zero has no effect. The relative bit positions in the Interrupt Acknowledge register are identical to the Status register except for bit 7, which is valid for reads (see explanation in Status Register) and undefined for writes (user must write a zero to this bit to be software-compatible for possible future redefinitions).

Sequence Register — Register 5

READ ONLY

1	1	1	1	1	SR2	SR1	SR0

Sequence Register

During the RUN mode, this register can be read back to indicate the current operation in progress. This is especially useful for examining interrupts when multiple intra-sequence pauses are specified. Bits 3–7 always reads 1s.

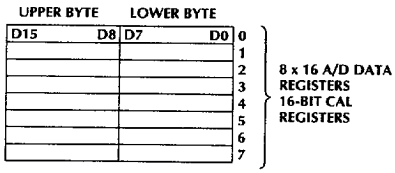
Registers 6 and 7— these registers are reserved for future use.

3.2 SECONDARY REGISTERS

There are twenty 16-bit wide secondary registers containing the Data RAM, Instruction RAM, Timer, Alarms, Alarm Criteria Register, and Interrupt Mask. Except for the Data RAM, the secondary registers should only be accessed on initialization, or when the chip is placed in the Halt mode.

Secondary Registers 0 to 7

Data RAM (read only)
Calibration Holding Register (write only)



The Data RAM consists of eight 16-bit wide registers that hold the output results from the latest conversion sequence. Each word in the Data RAM has a one-for-one correspondence with a word in the Instruction RAM. The Data RAM is also referred to as the data output registers.

The data output registers are double buffered and readable by the microprocessor at any time. The A/ D converter fills a "shadow" bank of registers during conversions, while the microprocessor is free to read the output registers. When the sequence is done, the "shadow" bank information is transferred to the output registers for the microprocessor to read, after which time DBR is asserted. Therefore, the microprocessor has essentially one sequence time to drain the data buffer. This time varies according to the number of operations defined, the system clock frequency, the mode field for each operation, and the cycle length (number of bits to be converted). Refer to Conversion Times for more information.

Data Format

All data is returned from the converter in 16-bit two's complement format, right hand justified, with the sign bit extended across the most significant unused bits.

Cycle	+Max	–Max	Mid-Range
16	7FFF	8000	0000
13	0FFF	F000	0000
8	007F	FF80	0000

Calibration Holding Register —

This register is for diagnostic purposes only. It is one 16-bit wide register mapped into the write only secondary address space 0 to 7 (i.e., a write to any of the secondary addresses 0-7 will load the Calibration Holding register). This register is write only and cannot be read back directly. It is used when the mode field in the Instruction Word is set to CAL Write, and the Instruction is executed. This command takes the contents of the Calibration Holding register and loads it into the Calibration register of the A/D converter. Note that this will change the calibration of the A/D converter, and a calibration of the A/D converter should be done after a CAL Write command is issued.

Instruction RAM — Secondary Registers 8 to 15 (Read/Write)

OP	0	8
OP	1	9
OP	2	10
OP	3	11
OP	4	12
OP	5	13
OP	6	14
OP	7	15

8 x 16 OPERATION REGISTERS

The Instruction RAM, sometimes referred to as the Operation registers, consists of eight 16-bit wide registers broken up into seven different fields (see Figures 10 and 10A). Each Instruction or Operation defines a single conversion, where the converted data result is stored in the corresponding data output register. Note that when the SLFTST bit in the Control register is set, the Instruction Word is redefined for diagnostic mode. Figure 12 illustrates the redefinition when SLFTST is set. The following section defines the seven different fields making up the Instruction word when SLFTST = 0.

D15	D14	D13 – 11	D10 – 8	D7 – 5	D4, 3	D2 – 0
LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF

REF (Bits 2,1, 0 — Voltage Reference Selection) REF specifies the source of the voltage reference used for the A/ D conversion.

GAIN (Bits 4 and 3 — Gain Settings) GAIN defines the gain of the precision instrumentation amplifier. The gain can be either 1, 2, 4, or 8. Each gain factor of 2 adds an additional 4 internal clock cycles (1 /f_{CLKI}) to the conversion time. Therefore a gain of 8 adds an additional 12 internal clock cycles to the conversion time.

CYCLE (Bits 7, 6, 5 — Cycle Select) CYCLE defines one of five different cycles: 8-, 13-, or 16-bit conversions, and READ or WRITE CAL CODE. Choosing 8-, 13- or 16-bit cycles determines how many bits the A/ D converter will convert. However, even though the converter has a 16-bit cycle, it may not have 16-bits of useful resolution. The useful resolution of the converter can be determined from the linearity specs.

Since the algorithmic converter is a successive approximation type of converter, an 8-bit cycle requires the least amount of time to convert, and the 16-bit cycle requires the most. Refer to Sampling Rates and Conversion Times for the exact number of clocks each cycle takes.

READ CAL CODE and WRITE CAL CODE cycles are for diagnostic purposes only. READ CAL CODE reads the Calibration register in the A/D converter and loads it into the corresponding data output register. WRITE CAL CODE transfers the contents of the Calibration Holding register into the A/D converter's Calibration register. The transfer is complete after the operation is executed. Refer to Diagnostics for more information on READ and WRITE CAL CODE.

CHAN (Bits 10, 9, 8 — Input Channel Number) defines the input channel to be converted.

ALRMEN (Bit 14 — Alarm Enable) When this bit is set the alarm criteria for the operation is enabled, otherwise the alarm is disabled for this operation. If ALRMEN is set and the alarm condition is met, the ALRM bit in the Status register will be set at the end of the operation.

LAST (Bit 15 — Last Operation) signifies that this operation is the last operation of the sequence. The chip will return to and begin the first operation of the sequence after execution of the current operation. If all eight operations are specified, the last one MUST have this bit set.

MODE (Bits 13,12,11—Mode Selection) defines the condition that must be met for the operation to proceed. The mode field also has an effect on the Operation Execution Time.

000	Immediate Execute
001	Intra-Sequence Pause
010	Start on Next Time out
011	Preset Timer/Start on Time out
100	External Sync Start
101	External Sync/Timer Preset/Time out
110	ILLEGAL
111	ILLEGAL

Events That Occur Within an Operation

To better understand six modes of the ML2200 or ML2208 one must first understand the events that occur during an operation. This can be aided by referring to Figure 17.

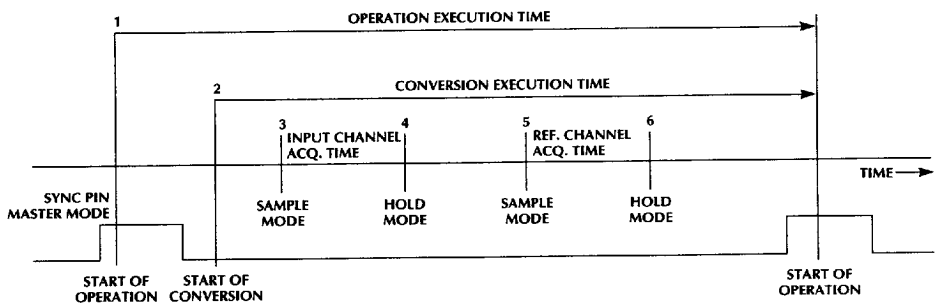


Figure 17. Events Within an Operation.

The first event that occurs in the Operation is the Start of Operation. This may or may not be the beginning of the conversion, depending on the mode selected. The time between the Start of Operation and Start of Conversion is variable. When the conditions of the mode have been met, the Start of Conversion occurs.

The Conversion Execution time includes the input and reference acquisition times, the gain time, and the successive approximation conversion time. Shortly after the Start of Conversion the S/H goes into sample mode acquiring the input channel for eight internal clocks. After the input has been acquired the S/H goes into hold mode, disconnecting the S/H from the input channel, and transferring the charge into the A/D converter. A couple of clocks later the same S/H goes into sample mode on the reference voltage, either the internal V_{REF} or one of the input channels. The reference acquisition time for all six modes is the same; eight internal clocks. After the S/H goes into hold mode the successive approximation A/D conversion begins. When the conversion is complete the next operation begins.

Immediate Execute (000) — The Start of Conversion begins at the Start of Operation. In other words, the conversion begins the instant the operation begins. There is no gating item delaying the conversion. This mode allows the chip to convert at its maximum rate with no unnecessary delays. As an example of calculating the sequence time, if all eight operations used Immediate Execute with a gain of 1 and a 13-bit conversion, the time to execute one sequence (all eight operations) would be 8 x 110 = 880 internal clocks.

Intra-Sequence Pause (001) — This mode provides a way for the microprocessor to initiate conversions, rather than the other modes which either initiate conversions from internal timings or an external pulse. At the Start of Operation the ISQ status bit is set. The microprocessor will recognize the setting of the ISQ status bit either by polling the Status register, or having enabled the ISQ interrupt. The Start of Conversion is delayed until the ISQAK bit in the Interrupt Acknowledge register is set.

Start on Next Time out (010) — After the Start of Operation occurs the Start of Conversion is delayed until the internal timer decrements from 1 to 0. When using this mode the timer will be free-running. This means that the timer is initialized in the Halt mode and left alone to decrement and reload automatically when in the Run mode. This mode can be used to establish a specific sampling rate. Note that the timer value must be greater than the conversion time, therefore this mode can only slow the sampling rate down from its maximum rate. In the case where several operations are used, and only one of them uses this mode, the timer value must be greater than all the other Operation Execution times plus the current operation conversion time.

Preset Timer/Start on Time out (011) — At the Start of Operation the timer is loaded with its pre-programmed count. The delay between the Start of Operation and the Start of Conversion is the pre-programmed count. Execution time of the operation is the pre-programmed timer count plus the conversion time. As opposed to mode 2, the timer can be any value between 2 and 2^{16}; i.e., there is no restriction on the timer value being greater than the conversion time. One application of this mode would be when an external analog event is triggered by the SYNC pulse, and the conversion needs to be delayed by a programmable amount of time.

Using the External SYNC Input — The following description applies to modes 4 and 5, since these two modes use the external SYNC input. These modes should only be used when the SYNC pin is programmed as an input (MSTR bit in Control register is 0). If the external SYNC signal arrives before the Start of Operation, it may be latched depending upon the arrival time. If it arrives 22 clocks after the previous operation's Start of Conversion, external SYNC will be latched; any time before will miss the pulse. Therefore the external SYNC pulse rate should not be any faster than the frequency of the operations which use this mode, otherwise there will be more external SYNC pulses than conversions.

External SYNC Start (100) — After the Start of Operation, the Start of Conversion is delayed until the rising edge of the SYNC pulse and the next rising edge of the internal clock. Unless the rising edge of the external SYNC is synchronized with the internal clock (See t_{SYNCCK} Spec), the aperture uncertainty is one internal clock.

External SYNC/Timer Preset/Time out (101) — For this mode, the external SYNC pulse presets the timer, and when the timer times out the Start of Conversion begins. The timer is preset after the rising edge of the external SYNC and the next rising edge of the internal clock. When the timer transitions from 1 to 0, the Start of Conversion begins. As in the previous mode, unless the rising edge of the external SYNC is synchronized with the internal clock, the aperture uncertainty is one internal clock.

Timer Functions of the Different Modes — The on-chip timer is started when RUN is asserted. It then free-runs, pre-loads and restarts itself at the pre-programmed count unless one of the modes in an operation word specifies a timer preset. If "Start on Next Timeout" mode is selected for all operations, the timer free-runs and subsequently starts conversions on regular intervals, without the inclusion of any variable overhead timing requirements of any specific operation. The "preset timer" function that can be specified in any operation, functions as a "one-shot" time out feature; however it can upset the regularity of conversions. The use of the external SYNC start allows flexibility with asynchronous conditions outside the chip. In addition, the use of time out with external SYNC allows synchronous operation of multiple Micro Linear chips with interleaved operation. If a different rate is desired other than increments of one master clock cycle (½ the CLK pin frequency) or if external events need to be counted before starting an operation, then setting the t_{CLK} bit in the control register will divert the timer to the t_{CLK} pin for all operations.

Timer Holding Register — Secondary Register 16 — This register holds the pre-programmed value of the timer. The value is in 1 internal clock increments, or the period of t_{CLK} if this input is used. The timer is a countdown timer, therefore the realized delay will be the number loaded into the Timer Holding register multiplied by the clock period. The value is written as a 16-bit binary word, and

either high or low bytes can be written first. These registers are both writable and readable, with register writes executed only when the chip is in the Halt mode (RUN bit cleared in the control register). Reading the Timer Holding register will return the preprogrammed value for the timer, it will not provide the actual timer value. Timer Holding register values of 1 or 0 are illegal and will "hang up" the timer when placed in Run mode. Therefore the minimum value that can be loaded into the Timer holding register is 2. The timer is decrementing when in Run mode and idle when in Halt mode. When the chip is placed in Run mode, the timer is automatically loaded with the value in the Timer Holding Register, and begins to count down.

Alarm Registers — Secondary Registers 17, 18 (Read /Write) — These registers specify the alarm criteria against which the converted data of a current operation is compared. The comparison occurs only when the ALRMEN bit is set within the operation. Secondary register 17 is Alarm A and secondary register 18 is Alarm B. These values are written in two's complement format, right justified and sign extended (refer to Data Format for more information).

Alarm Criteria Register— Secondary Register 19 lower byte (Read/Write) — Specifies the compare criteria to be used with alarm registers A and B. Bit 0 specifies whether the comparison of alarm word A is to be greater than (setting the bit) or less than equal to (clearing the bit). Similarly, bit l specifies the same criteria for alarm word B. The criteria of the two groups can be "ANDed" or "ORed" together by clearing (OR) or setting (AND) bit 2. Bits 3 and 4 enable the alarm comparison for words A and B, respectively. Bits 5, 6, and 7 are unused and be can be any value when written, always read as ones. The following table illustrates all of the possible combinations, X signifies don't care.

Bit Number					
4	3	2	1	0	
ENB	ENA	AND	GB	GA	Test Done:
0	0	X	X	X	No Test
0	1	X	X	0	≤ A
0	1	X	X	1	> A
1	0	X	0	X	≤ B
1	0	X	1	X	> B
1	1	0	0	0	≤ B or ≤ A
1	1	0	0	l	≤ B or >A
1	1	0	1	0	> B or ≤ A
1	1	0	1	1	> B or > A
1	1	1	0	0	≤ B and ≤ A
1	1	1	0	1	≤ B and > A
1	1	1	1	0	> B and ≤ A
1	1	1	1	1	> B and > A

Using the various criteria, the chip can discern whether a certain channel is inside or outside a band, or greater than or less than a value. Notifying the microprocessor can be done through an interrupt or by polling the status register.

Interrupt Mask— Secondary Register 19 Upper Byte (Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8
INTL	CLCPIE	RNERIE	ISQIE	IVRNIE	ALRMIE	OVRGIE	DBRIE

This register is used to define which interrupt conditions are capable of setting the hardware interrupt pin and the INT bit of the Status register. The bits in the Interrupt Mask register are interrupt enable bits, meaning when the bits are set they enable the corresponding status bit to activate the hardware interrupt pin as well as the INT bit in the Status register. The INTL bit determines the polarity of the INT pin. If set, the INT pin becomes active low, with an open drain output. If clear, the INT pin becomes active high, with driving capability in both directions.

Secondary Registers 20 to 31 — Undefined
These registers are undefined and will cause unpredictable results if read or written to.

4.0 SAMPLING RATES AND CONVERSION TIMES

To determine the sampling rate, one must first determine the sequence execution time. A sequence is defined as the number of operations or instructions used. Therefore the sequence execution time equals the sum of the individual operation execution times. The simplest case for determining the sampling rate is when only one operation is used in the sequence. Then the sampling period is the operation execution time. If all eight instructions are used in the sequence, the sampling rate would be the sequence rate multiplied by the number of times the channel was sampled in the sequence.

It is possible to sample one channel more frequently than another. For example, if every other operation sampled channel 0, while the remaining operations sampled channels 1, 2, and 3, the sampling rate for channel 0 would be four times the sampling rate of the other channels. If periodic sampling is important, one must be careful when sampling a channel multiple times in a sequence since different operations can have different execution times.

EXAMPLE: SAMPLING FOUR CHANNELS IN A BURST EVERY 10 MS

Using Mode 2 "Start on Next Time out" for Instruction 0 will establish the 10ms sampling rate, once the clock is initialized properly. Instructions 1, 2, and 3 can each use Mode 0 "Immediate Execution." For the ML2200, each instruction can sample a different channel, thus covering all four channels in a burst. For the ML2208, the same holds true except all eight channels can be sampled in a burst, periodically.

Assuming the external clock is 7MHz and each conversion is 13 bits with a gain of 1, the conversion time for each operation will be 110 x 286 ns = 31.4µs. Therefore four instructions will require 4 x 31.4µs = 125.7µs. The execution time is much less than the sampling rate, thus the timer can be used to set the sampling rate. The timer value for a 10 ms sample rate is: 10 ms/286 ns = 35,000 decimal or 88B8H.

OPERATION OR INSTRUCTION EXECUTION TIME

Figure 17 illustrates the Operation Execution Time. The time between the Start of Operation and Start of Conversion is variable and depends on the Mode chosen. For more information on how to determine the time between Start of Operation and Start of Conversion refer to the Secondary registers Mode field description in the Instruction RAM.

The Conversion Execution time depends on the Cycle, the Gain, and the Mode chosen in the instruction word. Modes 0–5 all behave the same way when it comes to Conversion Execution Time. To help determine the Conversion Execution Time the following table gives the number of internal clocks used for Modes 0–5 based on the Cycle chosen.

Cycle	Number of Internal System Clocks Needed ($1/f_{CLKI}$)
16-Bit	128
13-Bit	110
8-Bit	80
Read CAL	80
Write CAL	52

Add 4 extra clocks to the Cycle time for each gain of 2 (including Read CAL and Write CAL). For a gain of 2 add 4 extra clocks, for gain of 4 add 8 extra clocks, for gain of 8 add 12 extra clocks. Example: Modes 0–5, Cycle = 13-bit conversion with a gain of 8. Conversion Execution time is 122 internal clocks.

5.0 MICROPROCESSOR INITIALIZATION PROCEDURE

The following sequence of steps is recommended when initializing the ML2200 from the microprocessor:

1) Keep reset active for at least 10 internal clock cycles after power supplies have stabilized. If a software reset is issued, hold off microprocessor communications with the chip until the RESET bit in the control register is read back as cleared, which takes 4 internal clock cycles.

2) If desired, check the data register path by performing a write and read of the calibration register for all 8 operations. (This step is optional, but does provide user assurance of the integrity of the on-chip data paths.) The calibration register is a full 16-bit data path.

3) Perform a calibration by first enabling the CLCP interrupt in the Interrupt Mask register, then start the calibration by asserting the CAL bit i n the Control register. Alternately, if an interrupt driven system is not desired, the interrupt status register can be polled 8260 internal clocks after the CAL bit has been set. The chip should not be polled during calibration.

4) Upon receiving the CLCP interrupt, acknowledge it. If desired, read back the calibration code to verify a successful calibration. Other diagnostics may be run at this time, however diagnostics are optional and not required.

5) Load the Instruction RAM, alarm criteria, interrupt conditions, and timer. Set the proper data transfer mode up (DMA, interrupt driven or polled mode.) Clear all status bits before setting the RUN bit.

6) Start the chip running by setting the RUN bit in the Control register. This may be done by ORing the RUN bit with the other bits already configured in the Control register; however do not set the CAL bit again or another calibration will take place. Writing a 0 to the CAL bit has no effect; it will still read 1.

5.1 RESET/ POWER-ON CONDITIONS

When applying power to the ML2200, DV_{CC} and AV_{CC} should never be powered-on at different times.

It is OK to assert both $\overline{RD}$ and $\overline{WR}$ during RESET time, but not legal to do so otherwise; this may damage the chip internally.

The following list specifies the affected registers on the chip after a reset is performed. Note that both hardware and software reset of the chip have identical effects.

All registers shown below are cleared (all bits 0):

Primary Registers:
Index register (register 2)
Control register (register 3)
Status register (register 4)
Sequence status (register 5)

Secondary Registers:
Interrupt bit mask (upper half, register 19)
Alarm criteria register (lower half, register 19)

All other registers will have random data in them after power on. If a hardware or software reset is performed later, registers which are not listed above will be unchanged. Re-calibration after a hardware or software reset is not necessary, since the calibration register remains the same after a reset. Only after a power-up is a calibration necessary. However the CAL bit in the Control Register will be cleared after a reset. Setting the RUN bit while the CAL bit is clear will cause the RNER bit to be set. But, if a calibration had been done before the reset, the RNER may be ignored.

5.2 TIMER

If any of the operations require a timer function, (either a one-shot or regular conversion interval) then the timer value must be written. This is done by writing the index register value to 10 hexadecimal and writing the proper 16-bit time value to the window registers. The timer value must be greater than 1. If using mode 2 "Start on Next Time out" the timer value must be greater than the conversion time.

5.3 LIMIT ALARM OPERATION

The chip may be set up to watch for certain data conditions by enabling the proper interrupt bits in the Interrupt Mask register. These conditions include A/D overrange/ underrange and user-defined alarm criteria. In order to use the alarms, the A and B alarm values must be defined. Note that since alarm registers A and B are 16 bits wide, 13-bit two's complement sign extended values must be loaded. (Refer to Data Format for more information). In order to further qualify alarm registers A and B, the Alarm Criteria register must be initialized.

5.4 DEFINING INTERRUPT CONDITIONS

If the chip is used in polled situations, the interrupt mask bits need not be set unless the "OR" of the interrupt conditions, bit 7 in the Status register is used.

If the chip is used in interrupt mode rather than polled mode, the desired interrupt conditions should be considered. In addition to the interrupts specified for data comparison operations, several other interrupts can be defined in the Interrupt Mask register. The DBR bit can be set if the DBR pin is not used. This enables interrupts at the end of sequences for data transfer via the INT pin. The intra-sequence interrupt bit should be enabled if intra-sequence pauses are desired in any of the operations. Overrun error and run-time error bits should be enabled if trapping of these errors is desired.

Note that alarm A and B and overrange interrupts occur at any time within the sequence of operations. Due to the interrupt latency time of the microprocessor, multiple interrupts of this type within a sequence may be indistinguishable from each other. The A and B alarms should generally be used on only one operation so that its source can be determined with no ambiguity. Overrange interrupts can be handled by examining the data in the chip at the end of the sequence.

The INT pin polarity can be defined to be active high (bit 15 cleared in the Interrupt Mask register) or active low (bit 15 set). When active low is chosen, the INT pin is open drain without a pull-up. When active high, the INT pin is driven actively in both directions. The default condition is active high, and the INT pin is actively driven low during reset time.

6.0 METHODS OF DATA TRANSFER TO THE MICROPROCESSOR

There are several ways to handle the data output; polling, interrupt, or DMA. If interrupts are the method chosen, method 5) may be preferable. Method 5) DMA/Interrupt mode, does not require a DMA controller. It simply uses the DMA mode of the ML2200 or ML2208 which can be interfaced to an interrupt controller.

1) Intra-Sequence pause instruction is used when the microprocessor is not going to periodically/continuously read the data, but it will read the data at arbitrary times. The Table 1 below shows the op codes to sample all eight channels.

   Using these instructions the program begins when the RUN bit is set in the control register. Immediately after RUN is set, before the first conversion takes place, the ISQ bit in the status register is set. This indicates that the sequencer has paused. When the microprocessor wants to read a value on one or more of the channels it sets the ISQAK bit in the Interrupt Acknowledge register. The ML2208 then performs eight conversions back-to-back, jumps back to sequence 0, and sets the ISQ and DBR bits in the status register. The data from all eight channels is now available in the Data RAM. The next time a conversion is desired, once again the microprocessor sets ISQAK in the interrupt acknowledge register.

2) Polled mode transfer is done simply by polling the status register and examining the DBR bit to see if a sequence has been completed. The DBRIE interrupt mask bit need not be set, but an acknowledge should be done by setting DBRAK in the Interrupt Acknowledge register, otherwise an overrun error will occur. The CPU can just poll the INT bit in the Status register. Only the bits which are enabled in the Interrupt Mask register will set the INT status bit. When the INT bit is set, the CPU can examine the other status bits to determine which requests are active.

3) Interrupt mode can be implemented using the INT pin and enabling the desired interrupt conditions in the Interrupt Mask register. The polarity of the INT pin can be selected at the same time. If desired, DBR can be used as a second interrupt pin to signify the transfer of data only. This may be useful in systems with multiple and prioritized interrupt structures. If DBR is used, the DBR mask bit in the interrupt mask register should be disabled or cleared.

4) DMA mode can be implemented by setting the DMA enable bit in the control register and selecting high byte or low byte first by setting or clearing the LOBYT bit. The DBR pin is utilized as the DMA request, and will remain asserted until all data from the sequence is read.

5) DMA/Interrupt mode. DMA mode can also be used in non-DMA applications. Although this appears to be unconventional, it may actually be preferred over the interrupt mode because of its convenience and speed. One way to do this would be to use the DBR pin as an interrupt request but enable DMA mode in the DAP. When data is ready DBR interrupts the microprocessor. The microprocessor then reads either window register the required number of times to drain the Data RAM.

TABLE 1. CHANNELS IN AN ML2208 AT ARBITRARY TIMES

	LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF
SEQ0	0	0	Intra Sequence Pause	CH0	13	1	Internal
SEQI	0	0	Immed Execute	CHI	13	1	Internal
SEQ2	0	0	Immed Execute	CH2	13	1	Internal
SEQ3	0	0	Immed Execute	CH3	13	1	Internal
SEQ4	0	0	Immed Execute	CH4	13	1	Internal
SEQ5	0	0	Immed Execute	CH5	13	1	Internal
SEQ6	0	0	Immed Execute	CH6	13	1	Internal
SEQ7	1	0	Immed Execute	CH7	13	1	Internal

Using the DMA mode interrupt method over non-DMA mode interrupt method saves a lot of overhead. For example in non-DMA mode interrupt method (assuming AUTOI is set), the index register would have to be set on entry, and the DBRAK bit would have to be set each service routine. In DMA interrupt mode, neither the Index register nor the DBRAK bit would have to be set. These are handled automatically in DMA mode.

7.0 POWER-DOWN MODE

The chip can be powered-down by asserting the P_{DN} pin. It is advisable to place the chip in HALT mode first by clearing the RUN bit in the control register, however the chip will automatically go into Halt mode when powered-down. All analog circuits are powered-off; digital circuits are left in an idle state. All registers within the chip will retain their values down to a level of 2V between V_{CC} and GND.

Powering-up the chip is done by bringing P_{DN} high. The chip will be in Halt mode upon power-up. Note, however, that the first 10ms of chip operation after a power-up will not be valid due to the settling of quiescent bias conditions within the on-chip's analog circuits. Any data that is returned for this period after power-up should be considered invalid. The user has the choice of either throwing away the first 10ms of data or waiting for 10ms and then setting the chip in RUN mode. The on-chip timer can be used for this purpose, if desired, by defining a sequence of dummy operations that last for the required delay, then rewriting the required operations for normal use.

Acknowledge register. D_{BRAK} should also be set sometime before the next sequence to prevent the OVRN bit from being set, however this is not necessary.

Note that the microprocessor cannot let the ML2200 sequencer run continuously, i.e., SEQ 0 would be changed to Immediate Execute and asynchronously read the Data RAM. The problem in this case would be that the microprocessor may read the data at the same time that the chip is updating it. That is why either polling, interrupt, or DMA transfer is required in a continuous run mode of operation.

APPENDIX A

DIAGNOSTICS

The ML2200 and ML2208 may be run through a diagnostic routine after power-up. The DAP provides software programmable diagnostics so that no external hardware is necessary. Diagnostics are not necessary. They are provided as an option to the user.

SELF-TEST MODE

Setting the SLFTST bit in the Control register redefines the CHAN field in the Instruction Word. This in effect changes the input to the Sample-and-Hold from the multiplexer input channels to internal points within the chip; such as V_{REF} and AGND. Conversions in the Self-Test Mode allow the user to determine how the Sample-and-Hold and A/D converter behave with known input signals. This can be useful as a diagnostic routine for a product in the field, or as a debugging feature during product development. Figure 16 illustrates the redefinition of the instruction word when SLFTST= 1.

1. **System Offset** — The positive and negative inputs to the Sample-and-Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample-and-Hold combination.
2. **Internal Reference** — Connects the positive input of the Sample-and-Hold to V_{REF} and the negative input of the Sample-and-Hold to analog ground. The result of converting in this test mode is a value near positive full scale.
3. **Invert Internal Reference** — Connects the negative input of the Sample-and-Hold to V_{REF} and the positive input of the Sample-and-Hold to analog ground. The result of converting in this test mode is a value near negative full scale.
4. **Common Mode** — Both the positive and negative inputs of the Sample-and-Hold are tied to the internal V_{REF}. The result of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

Since setting the SLFTST bit merely changes the input to the Sample-and-Hold, conversions must be executed in order to read the results. This means placing the chip in the RUN mode and reading the results from the Data RAM. It is possible to run one sequence then halt the sequencer and read the results. The sequencer can be put in a "pause" via the Intra Sequence Pause Mode instruction. The following instructions accomplish this:

	LAST	ALRMEN	MODE	CHAN	CYCLE	GAIN	REF
SEQ 0	0	0	Intra SEQ Pause	System Offset	13	1	0
SEQ 1	0	0	Immed Execute	INT REF	13	1	0
SEQ 2	0	0	Immed Execute	Minus INT REF	13	1	0
SEQ 3	1	0	Immed Execute	Common Mode	13	1	0

After the RUN bit is set, the ISQ bit in the status register is immediately set. Setting the ISQAK bit in the Interrupt Acknowledge register will allow the sequencer to continue. The next time the ISQ bit is set, the results may be read from the Data RAM.

Reading and Writing to the Calibration Register The ML2200 and ML2208 architecture provides a way for the microprocessor to indirectly read and write to the A/D converter; specifically the Calibration register and the A/D's Data register. Figure 18 illustrates this architecture.

The instructions that cause these transfers are READ CAL CODE and WRITE CAL CODE; selected in the Cycle field of the instruction word when SLFTST = 0. WRITE CAL CODE transfers the contents of the Calibration Holding register into the A/D converter's Calibration register. READ CAL CODE transfers the contents of the Calibration Holding register through the A/D's Data register, into the Data Output register with the same location as the operation.

As a result of providing READ and WRITE CAL, it is possible to execute digital loopbacks through the Calibration register, A/D registers, and all 8 Data Output registers. These loopbacks provides user assurance that all of the paths are clear and there are no stuck bits.

Writing to the Calibration register changes the calibration of the A/D converter. Therefore a self calibration should be performed after executing a WRITE CAL CODE to ensure the A/D is properly calibrated.

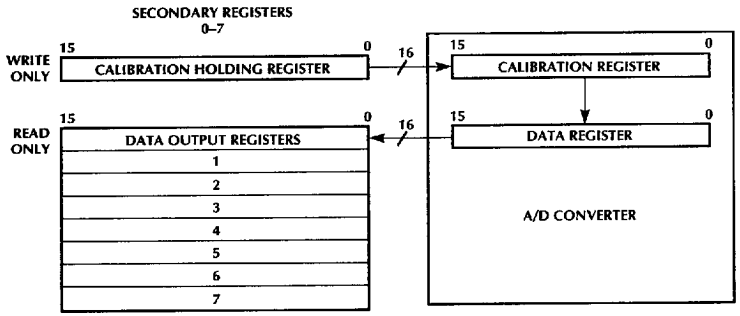


Figure 18. Digital Loopback Architecture.

DIGITAL LOOPBACK ARCHITECTURE

Reading the calibration register provides a way for the microprocessor to determine that the self calibration was successful. The microprocessor configures the DAP to execute a READ CAL CODE after a self calibration has been performed. If the lower byte of data from the READ CAL CODE is anything other than all 1s, then the calibration was successful.

Even though the calibration register itself is a 16-bit register, and is capable of holding a 16-bit result, only the lower 9 bits are significant in determining the calibration code. These 9 bits have a sign magnitude format, in other words the 9th bit (MSB of the 9-bit word) is the sign bit, and the other eight bits are magnitude bits. An easy way to determine whether the calibration has passed or failed is to read the lower data byte after a READ CAL is executed. If it's not all 1s then the calibration was a success.

APPLICATIONS

Utilizing instruction RAM bits 0, 1, and 2, any of the differential input channels of the ML2200 can be programmed to sense the external reference (See Figure 13.) Only single ended channels 0 thru 5 can be used on the ML2208 (See Figure 14.)

Figure 19. Using a 2.5V External Reference.

The system gain errors can be nulled by applying 2.4991 V (the full-scale voltage minus 1.5LSB) to one of the input channels and adjusting R1 until the digital output toggles between 01111 1111 1110 and 01111 1111 1111. If offset is not adjusted the full-scale voltage will be shifted by the amount of this unadjusted offset voltage.

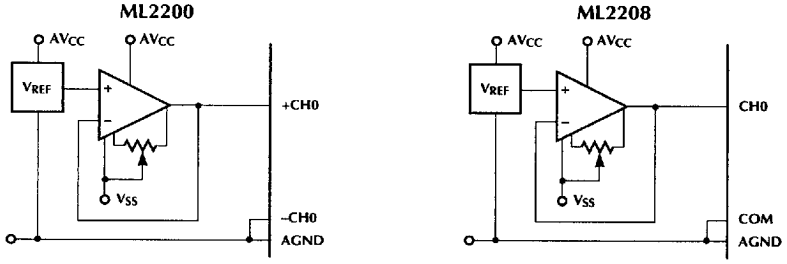


Figure 20. Adjusting Full-Scale Error.

APPLICATIONS (Continued)

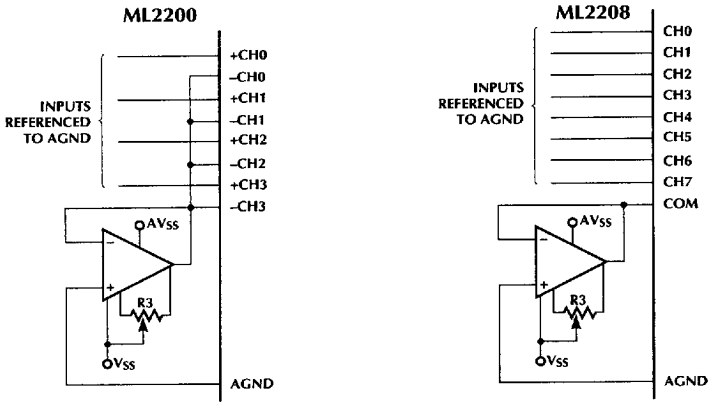


Figure 21. Adjusting Zero Error.

An op amp with an offset adjustment with a range of at least + 1.3 mV is required, like an OP – 27. The Zero Error can be nulled by first applying 305µV to one of the input channels (referenced to AGND.) 305µV is equivalent to ½ LSB which is the ideal input voltage which should cause the digital output to toggle from 0 0000 0000 0000 to 0 0000 0000 0001. Adjust R3 until this occurs.

If an external reference is also being used, it should be referenced to AGND, while the COM or negative inputs are tied to the offset op amp as shown above. In this configuration, the offset adjustment will effect the gain setting and so should be set first.

The Channel to Channel Zero Error and Full-Scale Error are very low and do not need to be adjusted separately. If, however, the input signal sources have their own different offsets, a separate op amp, with an offset adjustment, can be placed at each channel input.

APPLICATIONS (Continued)

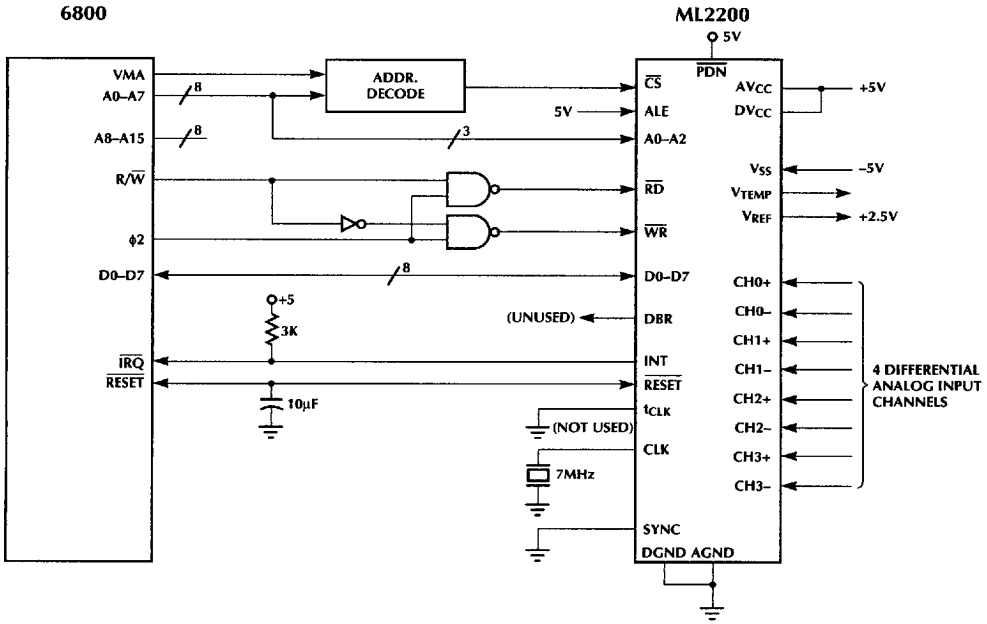


Figure 22. Interfacing ML2200 to 6800 Type Microprocessors.

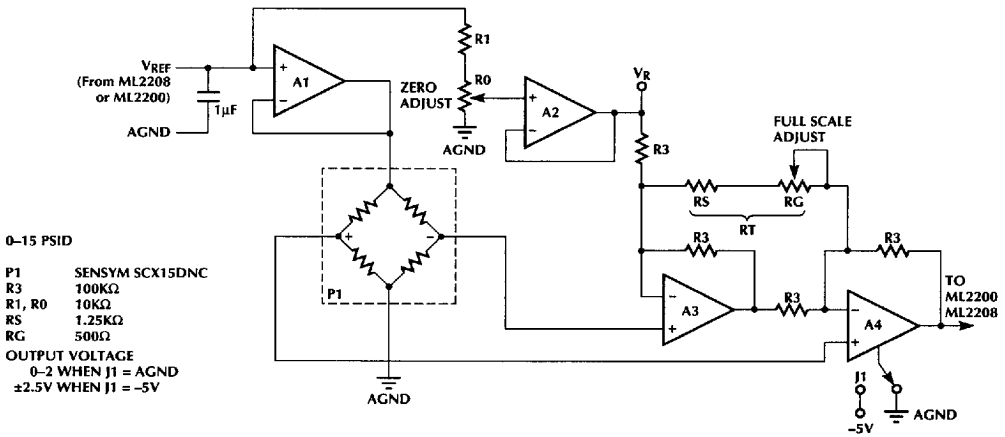


Figure 23. Pressure Sensor Application.

ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	MINIMUM CONVERSION	PACKAGE	TEMPERATURE RANGE
Four Differential Analog Inputs				
ML2200BCP	±3/4 LSB	31.5µs	Plastic DIP (P40)	0°C to +70°C
ML2200CCP	±1 LSB	31.5µs		
ML2200DCP	± LSB	44.0µs		
Eight Single Ended Analog Inputs				
ML2208BCP	±3/4 LSB	31.5µs	Plastic DIP (P40)	0°C to +70°C
ML2208CCP	±1 LSB	31.5µs		