ML5824 2.4GHz to 5.8GHz Frequency Translator

Final Datasheet

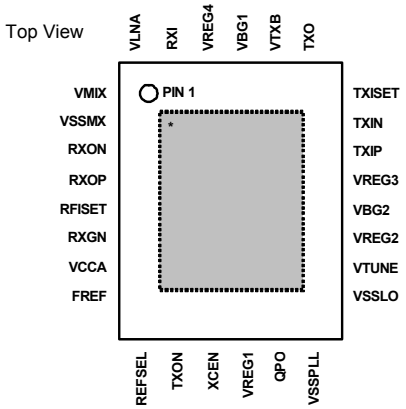
GENERAL DESCRIPTION

The ML5824 is a high integration 2.4GHz - 5.8GHz frequency translator (transverter). It upconverts 2.4GHz signals to 5.8GHz and downconverts received 5.8GHz signals to 2.4GHz. Transmit and receive utilize the same low noise fixed local oscillator (LO). It is intended to be used in conjunction with a 2.4GHz transceiver-based solution to quickly and easily develop a 5.8GHz solution while fully leveraging previous development.

The ML5824 receive chain contains a Low Noise Amplifier (LNA), bandpass filter and image reject down conversion mixer. A digitally controlled 18dB gain step in the receive chain provides an innovative solution for optimizing IIP3 (low gain mode) and Noise Figure (high gain mode). On the transmit side, the ML5824 buffers and upconverts a differential 2.4GHz signal to 5.8GHz, where it is filtered and amplified.

The ML5824's PLL accepts two industry-standard input clock frequencies. The ML5824's low STANDBY MODE current maximizes battery life. Power supply regulation is included in the ML5824, providing circuit isolation and consistent performance over supply voltages between 2.8V-3.6V.

PIN CONFIGURATION



* GROUND/RETURN ON EXPOSED PADDLE

ORDERING INFORMATION

PART NUMBER	TEMP RANGE	PACKAGE	PACK (QTY)
ML5824EM	-10°C to +70°C	28LPCC 4x5x0.9 mm	Antistatic Tray (490)
ML5824EM-T	-10°C to +70°C	28LPCC 4x5x0.9 mm	Tape & Reel (2500)

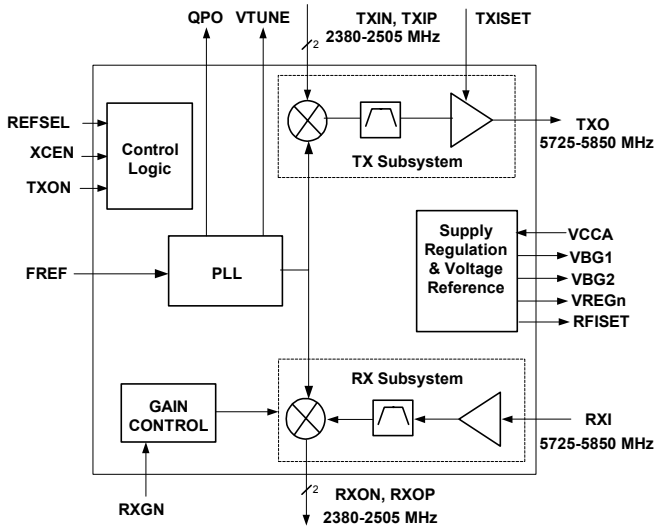
FEATURES

- High Integration 2.4GHz to 5.8GHz Transverter
  - Receive LNA, Image Reject Filter & Mixer
  - Transmit Pre-Driver, Filters & Mixers
  - Fully Integrated PLL-Based Synthesizer
- Selectable Receive Gain Optimizes NF and IIP3
- Interfaces Directly with Many 2.4GHz Transceivers
- 4dB (typ. High Gain Mode) Noise Figure
- -14dBm Input IP3 (Low Gain Mode)
- Selectable Transmit Output Power
- 10µA Standby Mode
- Space-saving 28 pin LPCC package

APPLICATIONS

- 5.8GHz Digital Cordless Telephones
- 5.8GHz Streaming Audio & Video
- Upconverted 2.4GHz Standards
  - o Bluetooth
  - o Zigbee/802.15.4

BLOCK DIAGRAM



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SIMPLIFIED APPLICATIONS DIAGRAM

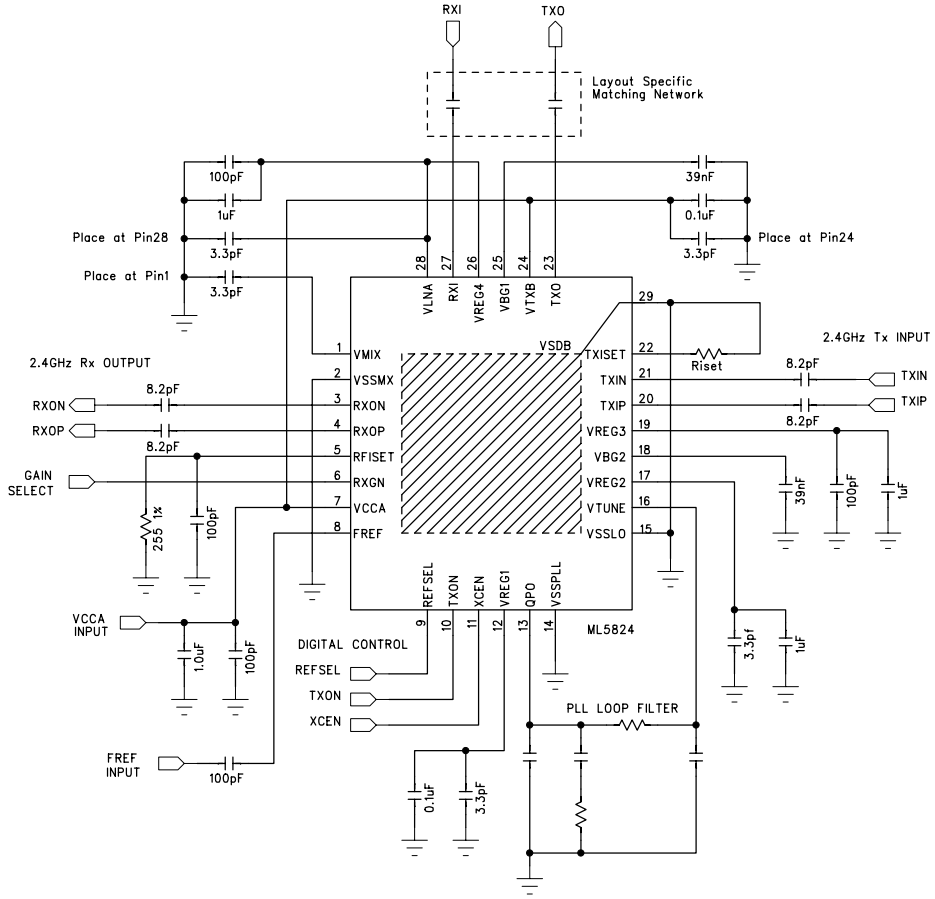


Figure 1: ML5824 Typical Application Schematic

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. Operating the device for any length of time beyond the operating conditions may degrade device performance and/or shorten operating lifetime.

VCCA..... 3.6 V
Maximum Receive RF Input Power..... +13dBm
Maximum Transmit RF Input Power..... +3dBm
Junction Temperature..... 150°C
Storage Temperature Range..... -65°C to 150°C
Lead Temperature (Soldering, 10s)..... 260°C
Thermal Resistance (θ_{JA})..... 39°C/W

OPERATING CONDITIONS

Ambient Temperature Range..... -10°C to 70°C
VCCA Range..... 2.8V to 3.6V

Unless otherwise specified, V_{CCA}=3.2V, T_A=-10ºC to +70ºC, XCEN=V_{IH}, P_{INRX}=-40dBm, P_{INTX}=-3dBm, PLL Loop Filter Bandwidth=40 KHz, and gain control in either state.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
VCCA	Analog supply voltage		2.8	3.2	3.6	V
I_{STBY}	Supply current, STANDBY mode	VCCA=3.6V, XCEN=V_{IL}, TXON= V_{IL} OR V_{IH}			10	µA
I_{RX}	Supply current, RECEIVE mode at -10dBm max RF input	TXON= V_{IL} TXON= V_{IL}, T_A=50ºC TXON= V_{IL}, T_A=25ºC			60 55 50	mA mA mA
I_{TX}	Supply current, TRANSMIT mode	TXON= V_{IH} R_{TXISET}=7.5KΩ R_{TXISET}=5.5KΩ TXON= V_{IH} R_{TXISET}=7.5KΩ, T_A=50ºC R_{TXISET}=5.5KΩ, T_A=50ºC		95 100 95 100	110 115 105 110	mA mA mA mA
SUPPLY REGULATION						
V_{R27}	Regulated Output Voltage	Pins 12, 19, 26		2.7		V
V_{R25}	Regulated Output Voltage	Pin 17		2.5		V
V_{BG}	Bandgap Voltage	Pins 18 & 25		1.25		V
SYNTHESIZER						
f_{LO}	Local Oscillator Frequency	F_{OUT} = F_{IN}+/- F_{LO}		3343.68		MHz
I_P	Charge Pump sink/source current This is a function of V_{TUNE} to compensate for the change in K_V	 V_{TUNE} =0.3V V_{TUNE} =1.2V V_{TUNE} =1.9V	 0.49	 0.90 0.60 0.38	 0.71	 mA mA mA
Φ_N	Phase noise at driver output f_o=10KHz offset from f_c f_o=1.2MHz offset from f_c	400mVp-p sine wave reference		 -65 -115	 -110	 dBc/Hz dBc/Hz
K_V	VCO Tuning sensitivity		100	230	350	MHz/V
F_{PULL}	Frequency pulling	70µs after P_{IN} –50dBm to +12dBm		+/-20		KHz

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
F_{PTR}	Frequency pulling TX to RX and RX to TX	70µs after transition		+/-20		KHz
F_{PUSH}	Frequency pushing	Vary VCCA from 2.9V to 3.6V		<.5		MHz/V
t_{WAKE}	Lock up time from standby	XCEN=V_{IH}, to within 10KHz,			200	µs
f_{FREF}	Reference signal frequency	REFSEL=V_{IL} REFSEL=V_{IH}		10.368 13.824		MHz MHz
V_{FREF}	Reference signal level	AC coupled	400		1200	mVp-p
RECEIVER						
F_{RXI}	Receiver Input Frequency Range			5.725-5.850		GHz
F_{RXO}	Receiver Output Frequency Range			2.380-2.505		GHz
Z_{RIN}	Receiver Input Impedance	Over F_{RXI}		37 + j2		Ω
Z_{RXO}	Receiver Output Impedance	Differential Impedance RXON/RXOP Over F_{RXO}		100		Ω
NF	Input noise figure	High Gain Mode Low Gain Mode		4.0 14	7.0 22	dB dB
G_{RX}	RX Power Gain High Gain Mode High Gain Mode High Gain Mode Low Gain Mode	Pin=-50dBm, T_A=25°C Pin=-50dBm, T_A=50°C Pin=-50dBm Pin=-30dBm	10.5 9.5 8	13 -8		 dB dB
I_{IP3}	Input IP3 High Gain Mode Low Gain Mode	For Pin=-50dBm each tone spaced +/-1MHz from 5800MHz For Pin=-30dBm each tone spaced +/1MHz from 5800MHz	-25	 -14		dBm dBm
P_{1dB}	RX Input 1dB compression	High Gain Mode Low Gain Mode		-35 -25		dBm dBm
P_{RXI}	RX conducted emissions from RF input port	RXI terminated in 50 ohm			-50	dBm
P_{SPUR}	Out of Band Spurious, High Gain Mode Low Gain Mode	Spurs outside Receive Output Frequency Range		 -25 -5		 dBc dBc
IRR	RX Image Rejection	From RXI to RXO, Pin=-50dBm, F_{RXI}= 835-965MHz	20			dB
TRANSMITTER						
F_{TXI}	Transmitter Input Frequency Range			2.380-2.505		GHz
F_{TXO}	Transmitter Output Frequency Range			5.725-5.850		GHz
Z_{TXI}	Transmitter Input Impedance	Differential Impedance TXIN/TXIP Over F_{TXI}		100		Ω
Z_{TXO}	Transmitter Output Impedance	Over F_{TXO}		43 + j88		Ω
P_{OUT}	TX buffer output power at 5.85 GHz Matched into 50 ohms, -10°C<T_A<70°C	R_{TXISET}=7.5KΩ, Pin=-6dBm R_{TXISET}=5.5KΩ, Pin=-3dBm	3.5 5.5			dBm dBm
P_{50C}	TX buffer output power at 5.85 GHz Matched into 50 ohms, -10°C<T_A<50°C	R_{TXISET}=7.5KΩ, Pin=-6dBm R_{TXISET}=5.5KΩ, Pin=-3dBm	5 7			dBm dBm
R_{TXH}	Transmit harmonic output rejection See Note 1	50 Ohm load		<-20		dBc
R_{LO}	Transmit LO feed thru	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}	-30			dBc

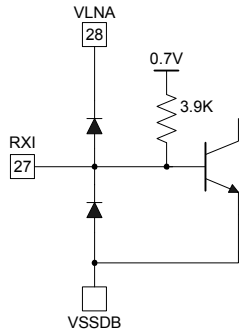
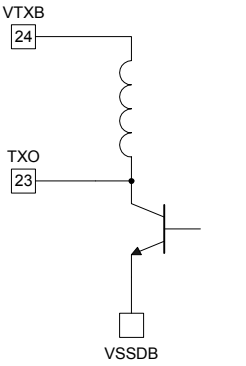
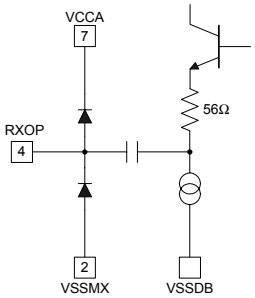
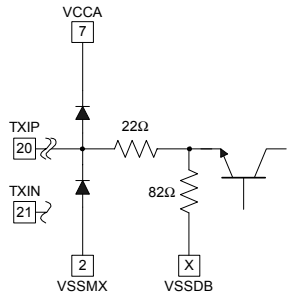
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{RFIF}	Transmit IF feed thru	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}	-30			dBc
R_{2LO}	Transmit 2xLO feed thru See Note 1	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}		<-30		dBc
R_{3LO}	Transmit 3xLO feed thru See Note 1	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}		<-20		dBc
R_{4LO}	Transmit 4xLO feed thru See Note 1	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}		<-20		dBc
R_{TSB}	Transmit lower sideband rejection	From TXI to TXO ports at P_{TXI} for F_{TXO}= 835-960MHz	25			dBc
R_{MXN}	Mixer products rejection at output port See Note 1	From TXI to TXO ports at P_{TXI} for F_{TXO}= 960-970MHz		>55		dBc
INTERFACE LOGIC LEVELS						
Input pins (XCEN, TXON, RXGN, REFSEL)						
V_{IH}	Input high voltage		VCCA*0.7		VCCA+0.4	V
V_{IL}	Input low voltage		-0.4		VCCA*0.3	V
I_B	Input bias current	All states	-5		5	µA
C_{IN}	Input capacitance	1MHz test frequency		4		pF

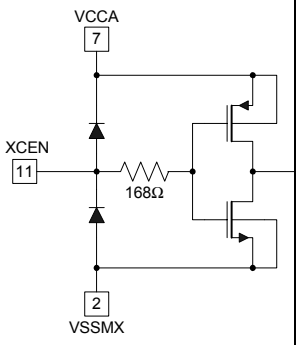
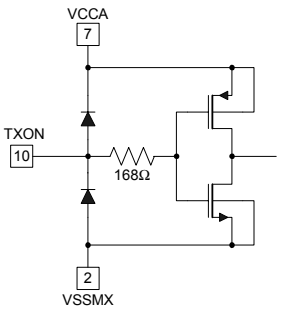
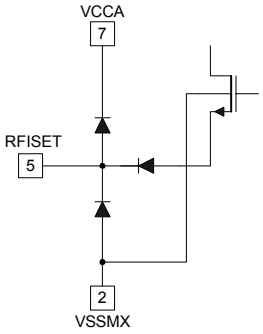
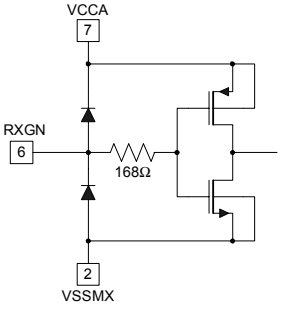
Note 1: Typical specs represent a 3 sigma data point at sample test.

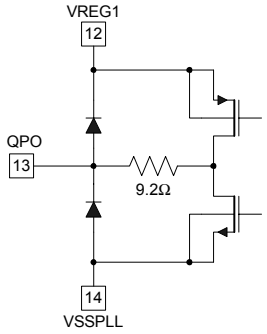
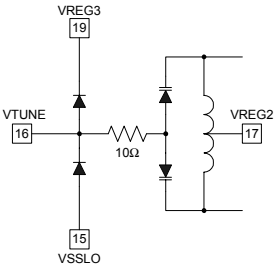
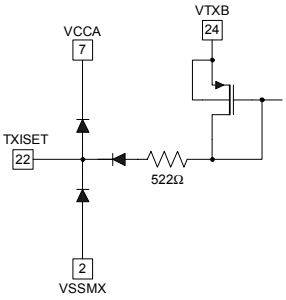
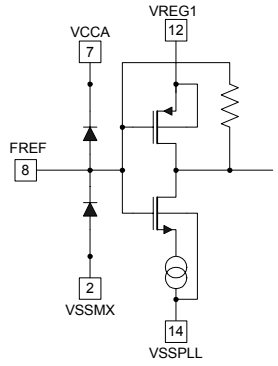
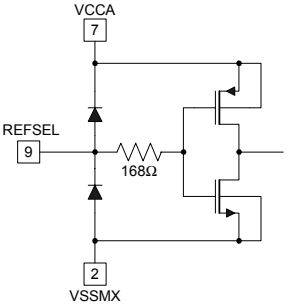
PIN DESCRIPTIONS

PIN	NAME	I/O	FUNCTION	DIAGRAM
POWER & GROUND				
2	VSSMX	GROUND	Mixer Ground	**N/A**
7	VCCA	POWER	Regulated External Supply, Requires Proper Decoupling Components	**N/A**
14	VSSPLL	GROUND	PLL Ground	**N/A**
15	VSSLO	GROUND	VCO and LO Ground	**N/A**
24	VTXB	INPUT	TX Buffer Supply Voltage, Connect to Pin 7	**N/A**
X	VSSDB	GROUND	Exposed Paddle. Ground/Return	**N/A**

SUPPLY REGULATION				
1	VMIX	INPUT	2.7V Supply Decoupling Point, Connect to Pin 26	**N/A**
12	VREG1	OUTPUT	2.7V Regulated Supply Output	**N/A**
17	VREG2	OUTPUT	2.5V Regulated Supply Output	**N/A**
18	VBG2	OUTPUT	1.24V Bandgap2 Supply Decoupling Point	**N/A**
19	VREG3	OUTPUT	2.7V Regulated Supply Decoupling Point	**N/A**
25	VBG1	OUTPUT	1.24V Bandgap1 Supply Decoupling Point	**N/A**
26	VREG4	OUTPUT	2.7V Regulated Supply Output, Connect to Pins 1 and 28	**N/A**
28	VLNA	INPUT	2.7V LNA Supply Decoupling Point, Connect to Pin 26	**N/A**

RF TRANSMIT/RECEIVE DATA				
27	RXI	I (analog)	5.8GHz RX Input. A simple matching network is required for optimum noise figure. This input connects to the base of an NPN transistor and should be AC coupled.	
23	TXO	O (analog)	5.8GHz TX Output into a matched load over the 5725 to 5850 MHz range.	
4 3	RXOP RXON	O (analog)	Differential 2.4GHz RX Output.	
20 21	TXIP TXIN	I (analog)	Differential 2.4GHz TX Input	

RF CONTROL & OTHERS				
11	XCEN	I (CMOS)	Transceiver Enable Input. Enables the bandgap reference and voltage regulators when high. Consumes only leakage current in STANDBY mode when low. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	
10	TXON	I (CMOS)	TX/RX Control Input. Switches the transceiver between TRANSMIT and RECEIVE modes. Circuits are powered up and signal paths reconfigured according to the operating mode. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	
5	RFISET	I (analog)	Connect to a 255Ω +/-1% resistor to ground.	
6	RXGN	I (CMOS)	Gain Step Input Control. Switches the receiver between high gain (when HIGH) and low gain (when LOW). This dual-gain design allows the system designer to achieve low noise figure for low input signals while maintaining a good IIP3 under high input signal conditions. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	

13	QPO	O (analog)	Charge Pump Output. This output is connected to the external PLL loop filter. Sources current when the LO frequency is lower than desired.	
16	VTUNE	I (analog)	VCO Tuning Voltage. This input from the PLL loop filter determines the output frequency and is very sensitive to noise coupling and leakage currents.	
22	TXISET	I (analog)	A resistor between this pin and ground establishes the PA output power compression point by setting a bias current.	
8	FREF	I (analog)	Input Reference Frequency. Depending on the state of the REFSEL pin this input is divided by 3 or 4 to generate the PLL reference frequency.	
9	REFSEL	I (CMOS)	Reference Divider Control. If REFSEL is HIGH, FREF is divided by 4, otherwise FREF is divided by 3. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	

FUNCTIONAL DESCRIPTION

The ML5824 is a monolithic, bilateral 2.4GHz to 5.8GHz frequency translator. It provides a simple and straightforward solution for designers of 2.4GHz products who want to develop advanced products for the relatively interference-free 5.8GHz band, especially digital cordless telephones. The ML5824 can implement “dual band” solutions that use both the 2.4GHz and 5.8GHz bands as well as “hybrid” products where one link (say, basestation transmission) is at 5.8GHz, while the other link (basestation receive) is at 2.4GHz.

5.8GHz signals enter the RXI pin and then are fed to an LNA and bandpass filter. An image-reject downconvert mixer translates the signal to the 2.4GHz ISM band where it is then buffered and sent off chip differentially on RXON/RXOP. The receive signal path can be configured for either a “High Gain” mode (about 14dB) or “Low Gain” mode (-4dB). Gain mode is selected via the RXGN digital input pin. High Gain mode is used for low-level input signals to minimize Noise Figure while Low Gain mode optimizes input IP3 for stronger signals.

2.4GHz signals come into the ML5824 differentially on the TXIP/TXIN pins, where they are upconverted to 5.8GHz, bandpass filtered, and then amplified and exit via TXO. The predriver/buffer output power compression point is programmed by an external resistor that sets the preamp bias level.

A fully integrated phase locked loop (PLL) generates the fixed local oscillator (LO) at 3343.68MHz which is used for upconverting and downconverting the RF signals. The comparison frequency of the PLL is derived from the frequency reference present on the FREF pin and the state of REFSEL as shown in Table 1. The PLL loop filter is external to the ML5824 so that lock time and in-band phase noise can be optimized for the system of interest.

REFSEL	REFERENCE DIVISION	FREF
V_{IL}	3	10.368MHz
V_{IH}	4	13.824MHz

Table 1: ML5824 Frequency References

The ML5824 contains two separate bandgap references and several low dropout (LDO) voltage regulators to insure consistent performance over supply voltage and minimize crosstalk on chip. The device is enabled by bringing XCEN to V_{IH} and is placed in transmit mode by setting TXON to V_{IH}. With XCEN at V_{IL} the ML5824 enters a low power standby mode.

MODES OF OPERATION

The ML5824 has three key modes of operation. The two operational modes are RECEIVE and TRANSMIT, controlled by TXON. XCEN is the chip enable/disable control pin, which sets the device in operational or STANDBY modes. The relationship between the parallel control lines and the mode of operation of the IC is summarized in Table 2.

XCEN	TXON	MODE NAME	FUNCTION
0	X	STANDBY	Standby. All circuits powered down
1	0	RECEIVE	Receive Chain Active
1	1	TRANSMIT	Transmit Chain Active

Table 2: Modes of Operation

STANDBY MODE

In STANDBY mode, the ML5824 transverter is powered down. When exiting STANDBY mode, the transmitter is disabled for 200µs. However, the receive path is not similarly locked out and so will receive invalid data for up to 200µs. Therefore, the system should wait 200µs after exiting STANDBY mode before actively processing signals to allow the PLL to lock. A timing diagram for the ML5824 is shown in Figure 2.

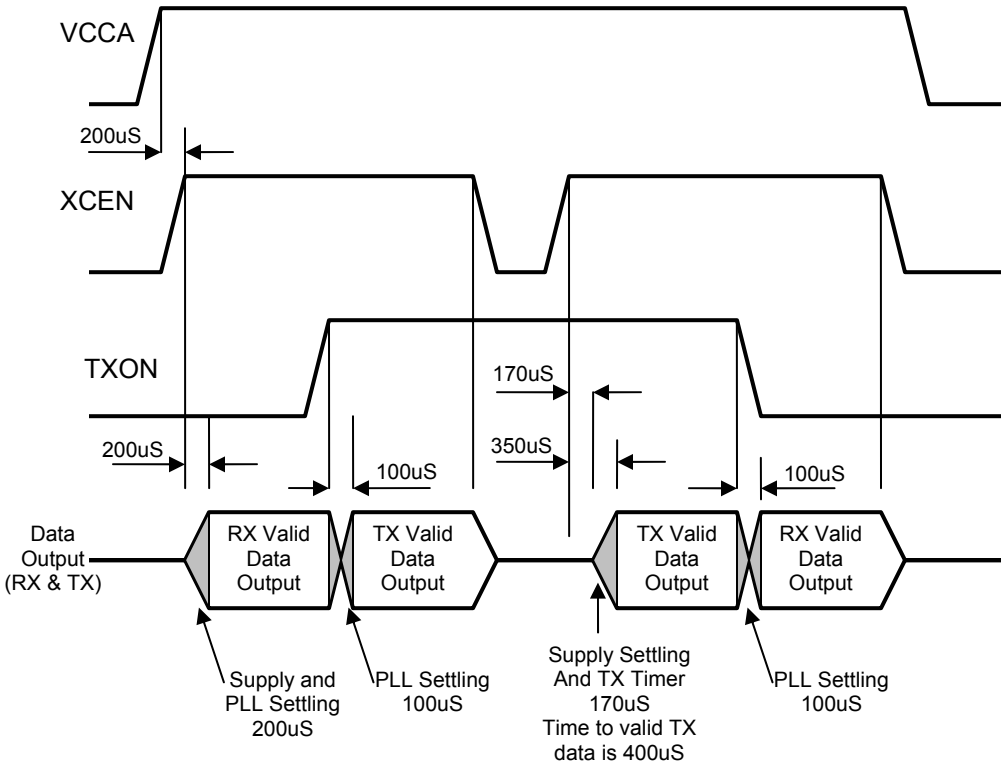


Figure 2: ML5824 Control Timing Diagram, assuming a 40 KHz loop bandwidth.

RECEIVE MODE

In RECEIVE mode, the received signal at 5.8GHz is amplified, filtered, and downconverted to 2.4GHz. The receiver has two gain modes; High Gain (about 14dB) and Low Gain (about -4dB). Gain mode is set via the state of the RXGN input, with High Gain Mode corresponding to a logic “1” on RXGN.

TRANSMIT MODE

In TRANSMIT mode, the transmitted signal at 2.4GHz is upconverted, filtered, and amplified at 5.8GHz. The transmit output power compression point is programmable via an external resistor on the TXISET pin.

PHYSICAL DIMENSIONS

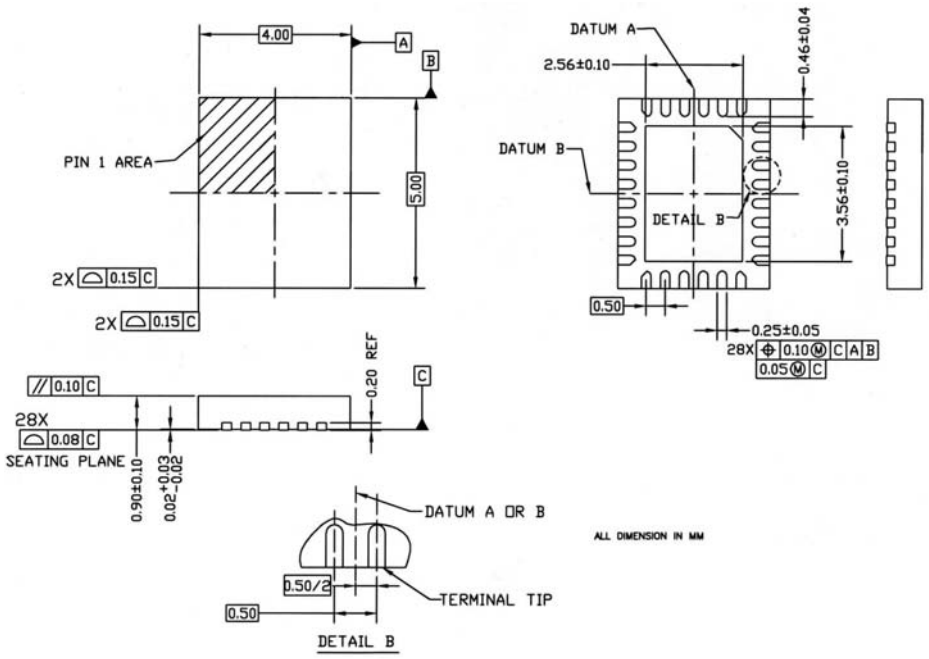


Figure 3: 28 Leadless Plastic Chip Carrier (LPCC) Dimensions

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

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