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# ML610404/ML610405/ML610406

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## 8-bit Microcontroller with a Built-in LCD driver

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### GENERAL DESCRIPTION

ML610404/ML610405/ML610406 is a high-performance 8-bit CMOS microcontroller into which peripheral circuits, such as synchronous serial port, UART, melody driver, RC oscillation type A/D converter, and LCD driver, are incorporated around LAPIS Semiconductor-original 8-bit CPU nX-U8/100. ML610404/ML610405/ML610406 operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.

The short TAT are entertained by offering MTP version ML610Q407/ML610Q408/ML610Q409.

ML610404P/ ML610405P/ML610406P support industrial temperature -40°C to +85°C, are added to the product lineup.

### FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Minimum instruction execution time
    - 30.5  $\mu$ s (@32.768 kHz system clock)
    - 2 $\mu$ s (@500kHz system clock)
    - 0.5 $\mu$ s(@2MHz system clock)
- Internal memory
  - ML610404/5/6 :
    - Internal 8KByte Mask ROM (4K $\times$ 16 bits) (including unusable 128 Byte TEST area)
    - Internal 256Byte Data RAM (256 $\times$ 8 bits)
- Interrupt controller
  - 1 non-maskable interrupt sources
    - Internal source: 1 (Watch dog timer)
  - 27 maskable interrupt sources
    - Internal sources: 14 (Synchronous serial port 0, Synchronous serial port 1, Timer0, Timer1, Timer2, Timer3, UART0, Melody0, RC Oscillation type A/D converter, PWM0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    - External sources: 13 (P00, P01, P02, P03, P04, P50, P51, P52, P53, P54, P55, P56, P57)
    - (One interrupt request is generated from P50 to P57 interrupt sources.)
- Time base counter
  - Low-speed time base counter  $\times$ 1 channel
    - Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter  $\times$ 1 channel
- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s)
- Timers
  - 8 bits  $\times$  4 channels [also available is 16-bit configuration (using Timers 0 and 1, or Timers 2 and 3)  $\times$  2 channels]
  - Clock frequency measurement function mode (16-bit configuration using Timers 2 and 3  $\times$  1 channel only)

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)
- PWM
  - Resolution 16 bits × 1 channel
- Synchronous serial port
  - Master/slave selectable × 2 channel
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator
- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
  - 16-bit counter
  - Time division × 2 channels
- General-purpose ports
  - Input-only port × 5 channels (including secondary functions)
  - Output-only port
    - ML610404: × 12 channels (including secondary functions)
    - ML610405: × 8 channels (including secondary functions)
    - ML610406: × 4 channels (including secondary functions)
  - Input/output port × 22 channels (including secondary functions)
- LCD driver
  - Number of segments
    - ML610404: Up to 105 dots (select among 21 segments x 5 commons, 22 segments x 4 commons, 23 segments x 3 commons, and 24 segments x 2 commons)
    - ML610405: Up to 125 dots (select among 25 segments x 5 commons, 26 segments x 4 commons, 27 segments x 3 commons, and 28 segments x 2 commons)
    - ML610406: Up to 145 dots (select among 29 segments x 5 commons, 30 segments x 4 commons, 31 segments x 3 commons, and 32 segments x 2 commons)
  - 1/1 to 1/5 duty
  - 1/2, 1/3 bias (built-in bias generation circuit)
  - Frame frequency selectable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function
- Reset
  - Reset through the RESET\_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected (Cancellation by a mask option is possible)
  - Reset by the watchdog timer (WDT) overflow

- Clock
  - Low-speed clock (Operation of this LSI is not guaranteed under a condition with no supply of low-speed crystal oscillation clock)
    - Crystal oscillation (32.768 kHz)
  - High-speed clock: Built-in RC oscillation (500 kHz, 2MHz)
  
- Power management
  - HALT mode: Suspends the instruction execution by CPU (peripheral circuits are in operating states)
  - STOP mode: Stops the low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Completely stops the operation of any function block circuit that is not used (resets registers and stops clock)
  
- Guaranteed operating range
  - Operating temperature: -20°C to +70°C (P version: -40°C to +85°C)
  - Operating voltage:  $V_{DD} = 1.25V$  to 3.6V

• Product name – Supported Function

- Chip (Die) -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610404-xxxWA	Yes	Yes	Cancellation by a mask option is possible	-20°C to +70°C	Yes
ML610405-xxxWA	Yes	Yes	Cancellation by a mask option is possible	-20°C to +70°C	Yes
ML610406-xxxWA	Yes	Yes	Cancellation by a mask option is possible	-20°C to +70°C	Yes
ML610404P-xxxWA	Yes	Yes	Cancellation by a mask option is possible	-40°C to +85°C	Yes
ML610405P-xxxWA	Yes	Yes	Cancellation by a mask option is possible	-40°C to +85°C	Yes
ML610406P-xxxWA	Yes	Yes	Cancellation by a mask option is possible	-40°C to +85°C	Yes

-80-pin plastic TQFP -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610404-xxxTB	Yes	Yes	Cancellation by a mask option is possible	-20°C to +70°C	-
ML610405-xxxTB	Yes	Yes	Cancellation by a mask option is possible	-20°C to +70°C	-
ML610406-xxxTB	Yes	Yes	Cancellation by a mask option is possible	-20°C to +70°C	-
ML610404P-xxxTB	Yes	Yes	Cancellation by a mask option is possible	-40°C to +85°C	-
ML610405P-xxxTB	Yes	Yes	Cancellation by a mask option is possible	-40°C to +85°C	-
ML610406P-xxxTB	Yes	Yes	Cancellation by a mask option is possible	-40°C to +85°C	-

xxx: ROM code number (xxx of the blank product is NNN)

Q: MTP version

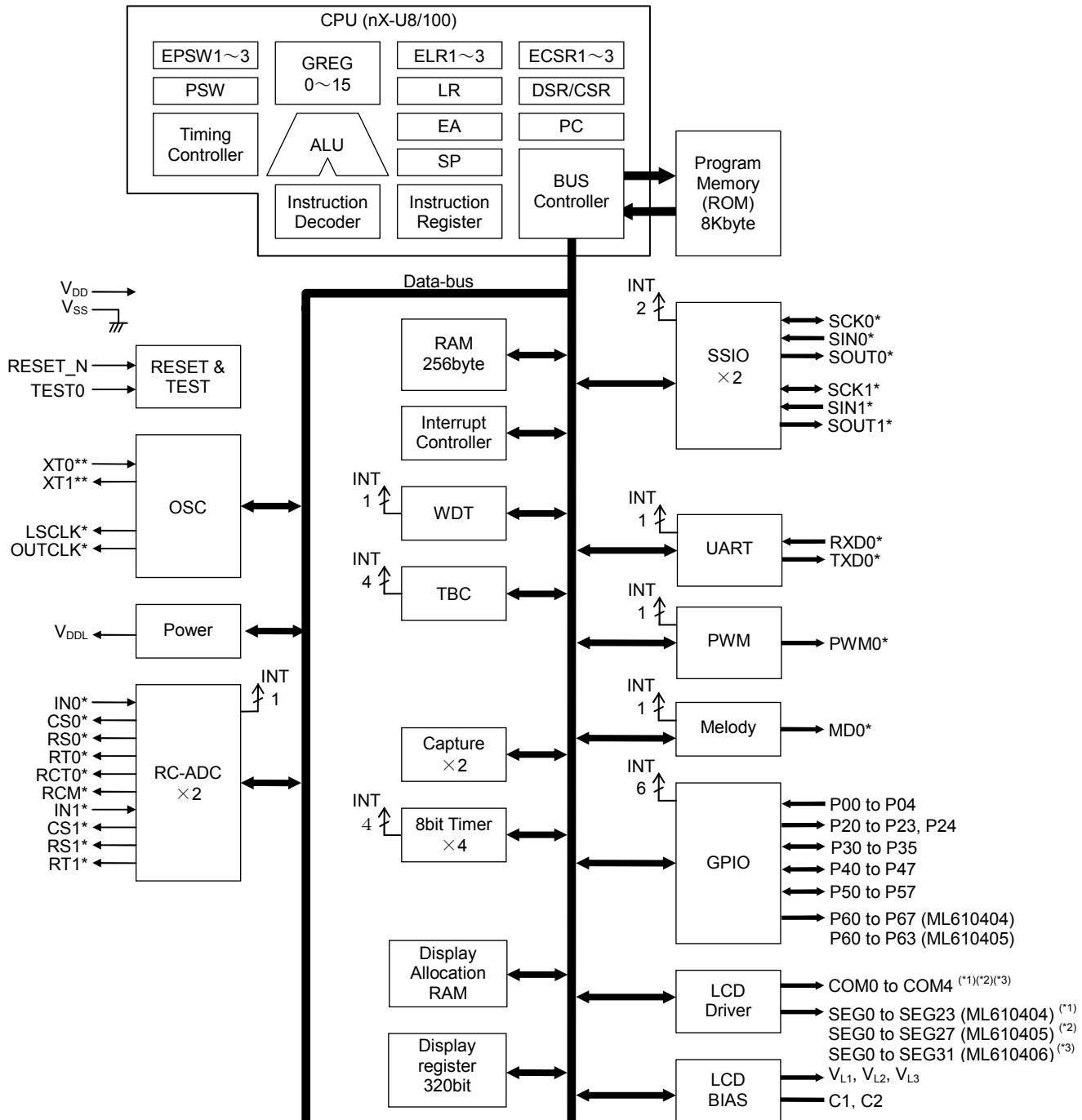
P: Wide range temperature version (P version)

WA: Chip (Die)

TB: TQFP

**BLOCK DIAGRAM**

Block Diagram of ML610404/ML610405/ML610406



\* Secondary function or Tertiary function

“\*1”: Select among 21 segments x 5 commons, 22 segments x 4 commons, 23 segments x 3 commons, and 24 segments x 2 commons with the register

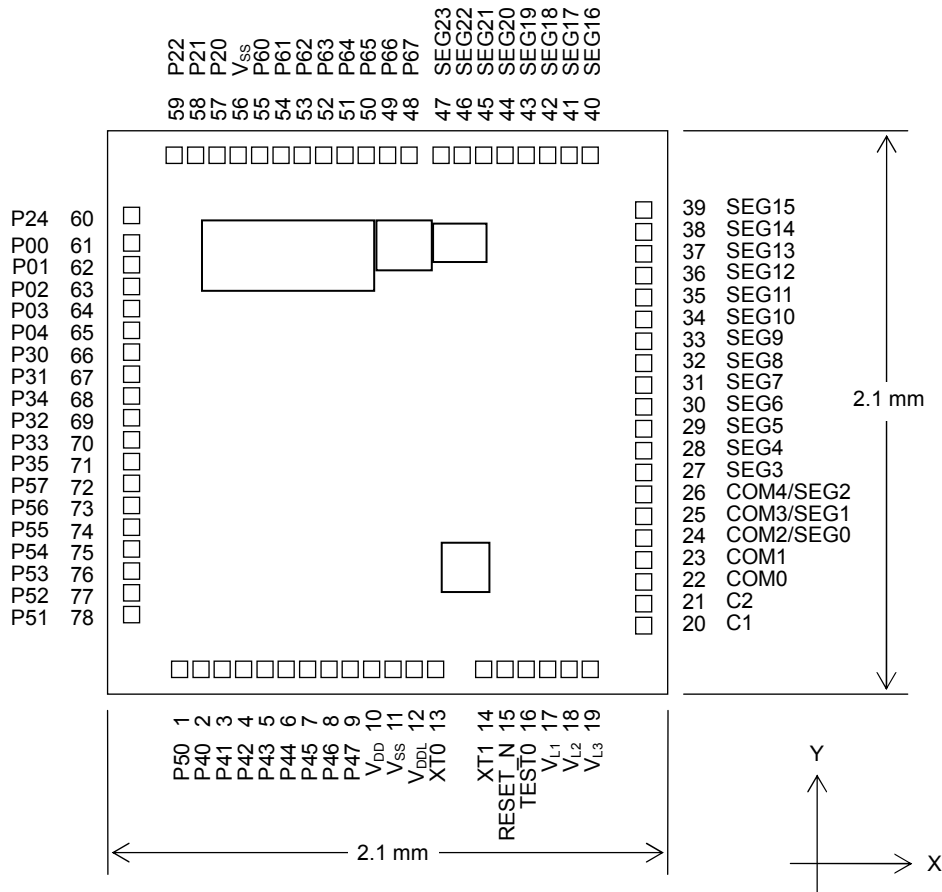
“\*2”: Select among 25 segments x 5 commons, 26 segments x 4 commons, 27 segments x 3 commons, and 28 segments x 2 commons with the register

“\*3”: Select among 29 segments x 5 commons, 30 segments x 4 commons, 31 segments x 3 commons, and 32 segments x 2 commons with the register

Figure 1 Block Diagram of ML610404/ML610405/ML610406

**PIN CONFIGURATION**

**Pin Layout of ML610404 Chip**



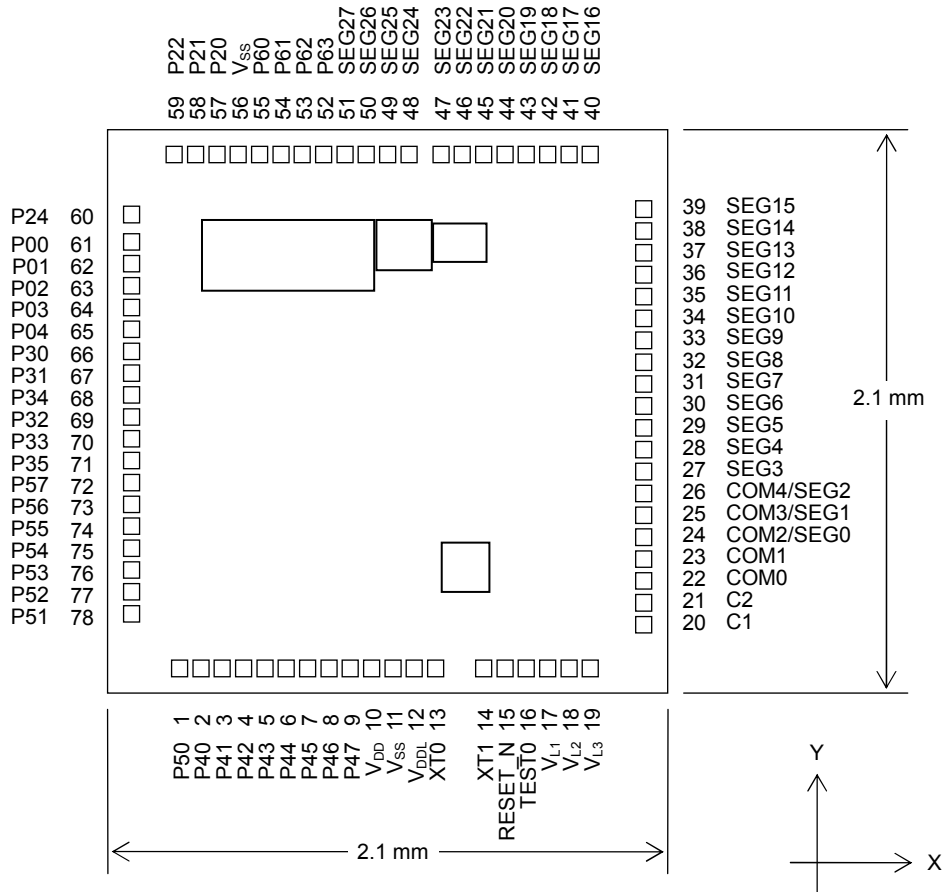
Note:

The assignment of the pads P30 to P35 are not in order.

Chip size: 2.1 mm × 2.1 mm  
 PAD count: 78 pins  
 Minimum PAD pitch: 80μm  
 PAD aperture: 70μm×70μm  
 Chip thickness: 350μm  
 Voltage of the rear side of chip: V<sub>SS</sub> leve

**Figure 2 Dimensions of ML610404 Chip**

**Pin Layout of ML610405 Chip**



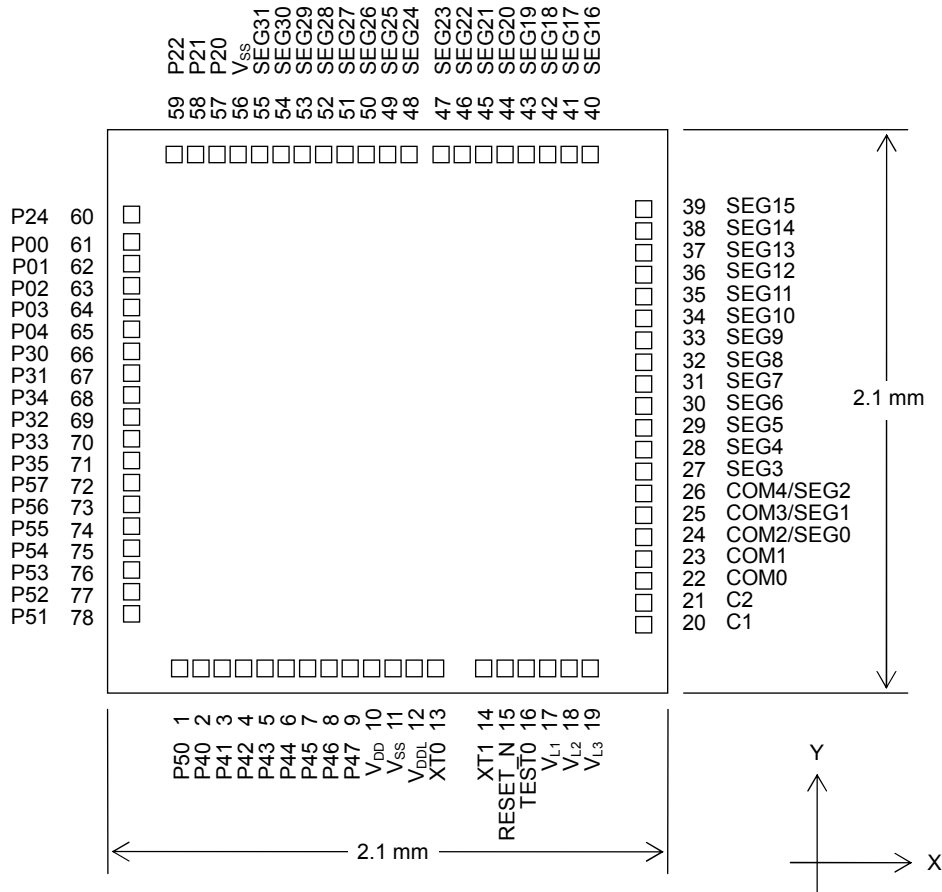
Note:

The assignment of the pads P30 to P35 are not in order.

- Chip size: 2.1 mm × 2.1 mm
- PAD count: 78 pins
- Minimum PAD pitch: 80μm
- PAD aperture: 70μm×70μm
- Chip thickness: 350μm
- Voltage of the rear side of chip: V<sub>SS</sub> level.

**Figure 3 Dimensions of ML610405 Chip**

**Pin Layout of ML610406 Chip**



Note:  
The assignment of the pads P30 to P35 are not in order.

- Chip size: 2.1 mm × 2.1 mm
- PAD count: 78pins
- Minimum PAD pitch: 80 μm
- PAD aperture: 70 μm×70 μm
- Chip thickness: 350 μm
- Voltage of the rear side of chip: V<sub>SS</sub> level.

**Figure 4 Dimensions of ML610406 Chip**



**Pad Coordinates of ML610404/ML610405/M610406 Chip**

**Table 1 Pad Coordinates of ML610404/ML610405/ML610406**

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610404/5/6		PAD No.	Pad Name	ML610404/5/6	
		X (μm)	Y (μm)			X (μm)	Y (μm)
1	P50	-773	-944	44	SEG20	450	944
2	P40	-693	-944	45	SEG21	370	944
3	P41	-613	-944	46	SEG22	290	944
4	P42	-533	-944	47	SEG23	210	944
5	P43	-453	-944	48	P67 <sup>(*)</sup>	115	944
6	P44	-373	-944		SEG24 <sup>(*)</sup> (*)		
7	P45	-293	-944	49	P66 <sup>(*)</sup>	35	944
8	P46	-213	-944		SEG25 <sup>(*)</sup> (*)		
9	P47	-133	-944	50	P65 <sup>(*)</sup>	-45	944
10	V <sub>DD</sub>	-53	-944		SEG26 <sup>(*)</sup> (*)		
11	V <sub>SS</sub>	27	-944	51	P64 <sup>(*)</sup>	-125	944
12	V <sub>DDL</sub>	107	-944		SEG27 <sup>(*)</sup> (*)		
13	XT0	187	-944	52	P63 <sup>(*)</sup> (*)	-205	944
14	XT1	347	-944		SEG28 <sup>(*)</sup>		
15	RESET_N	427	-944	53	P62 <sup>(*)</sup> (*)	-285	944
16	TEST0	507	-944		SEG29 <sup>(*)</sup>		
17	V <sub>L1</sub>	587	-944	54	P61 <sup>(*)</sup> (*)	-365	944
18	V <sub>L2</sub>	667	-944		SEG30 <sup>(*)</sup>		
19	V <sub>L3</sub>	747	-944	55	P60 <sup>(*)</sup> (*)	-445	944
20	C1	944	-810		SEG31 <sup>(*)</sup>		
21	C2	944	-730	56	V <sub>SS</sub>	-525	944
22	COM0	944	-650	57	P20	-605	944
23	COM1	944	-570	58	P21	-685	944
24	COM2/SEG0	944	-490	59	P22	-765	944
25	COM3/SEG1	944	-410	60	P24	-944	717
26	COM4/SEG2	944	-330	61	P00	-944	617
27	SEG3	944	-250	62	P01	-944	537
28	SEG4	944	-170	63	P02	-944	457
29	SEG5	944	-90	64	P03	-944	377
30	SEG6	944	-10	65	P04	-944	297
31	SEG7	944	70	66	P30	-944	217
32	SEG8	944	150	67	P31	-944	137
33	SEG9	944	230	68	P34	-944	57
34	SEG10	944	310	69	P32	-944	-23
35	SEG11	944	390	70	P33	-944	-103
36	SEG12	944	470	71	P35	-944	-183
37	SEG13	944	550	72	P57	-944	-263
38	SEG14	944	630	73	P56	-944	-343
39	SEG15	944	710	74	P55	-944	-423
40	SEG16	770	944	75	P54	-944	-503
41	SEG17	690	944	76	P53	-944	-583
42	SEG18	610	944	77	P52	-944	-663
43	SEG19	530	944	78	P51	-944	-743

(\*) Pad for ML610404. (\*\*) Pad for ML610405. (\*\*\*) Pad for ML610406

**List of Pins**

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
11,57	11,56	V <sub>SS</sub>	—	Negative power supply pin	—	—	—	—
10	10	V <sub>DD</sub>	—	Positive power supply pin	—	—	—	—
12	12	V <sub>DDL</sub>	—	Power supply pin for internal logic (internally generated)	—	—	—	—
18	17	V <sub>L1</sub>	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin) <sup>(*)</sup>	—	—	—	—
19	18	V <sub>L2</sub>	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin) <sup>(*)</sup>	—	—	—	—
20	19	V <sub>L3</sub>	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin) <sup>(*)</sup>	—	—	—	—
21	20	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—
22	21	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—
17	16	TEST0	I/O	Test input pin	—	—	—	—
16	15	RESET_N	I	Reset input pin	—	—	—	—
14	13	XT0	I	Low-speed clock oscillation pin	—	—	—	—
15	14	XT1	O	Low-speed clock oscillation pin	—	—	—	—
62	61	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—	—
63	62	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—	—
64	63	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 received data	—	—	—	—
65	64	P03/EXI3	I	Input port, External interrupt	—	—	—	—
66	65	P04/EXI4/ T02P0CK	I	Input port, Timer 0/Timer 2/PWM0 external clock input External interrupt	—	—	—	—
58	57	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
59	58	P21/LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
60	59	P22/LED2	O	Output port	Secondary	MD0	O	Melody 0 output
61	60	P24/LED4	O	Output port	Secondary	PWM0	O	PWM0 output
67	66	P30	I/O	Input/output port	Secondary	IN0	I	RC type ADC0 oscillation input pin
68	67	P31	I/O	Input/output port	Secondary	CS0	O	RC type ADC0 reference capacitor connection pin
69	68	P34	I/O	Input/output port	Secondary	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
70	69	P32	I/O	Input/output port	Secondary	RS0	O	RC type ADC0 reference resistor connection pin
71	70	P33	I/O	Input/output port	Secondary	RT0	O	RC type ADC0 measurement resistor sensor connection pin
72	71	P35	I/O	Input/output port	Secondary	RCM	O	RC type ADC oscillation monitor

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
2	2	P40	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SIN0	I	SSIO0 data input
3	3	P41	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
4	4	P42	I/O	Input/output port	Secondary	RXD0	I	UART data input
					Tertiary	SOUT0	O	SSIO0 data output
5	5	P43	I/O	Input/output port	Secondary	TXD0	O	UART data output
					Tertiary	PWM0	O	PWM0 output
6	6	P44/ T02POCK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	Secondary	IN1	I	RC type ADC1 oscillation input pin
					Tertiary	SIN0	I	SSIO0 data input
7	7	P45/T13CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	Secondary	CS1	O	RC type ADC1 reference capacitor connection pin
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
8	8	P46	I/O	Input/output port	Secondary	RS1	O	RC type ADC1 reference resistor connection pin
					Tertiary	SOUT0	O	SSIO0 data output
9	9	P47	I/O	Input/output port	Secondary	RT1	O	RC type ADC1 measurement resistor sensor connection pin
1	1	P50/EX18	I/O	Input/output port, External interrupt	Secondary	MD0	O	Melody 0 output
					Tertiary	SIN1	I	SSIO1 data input
79	78	P51/EX18	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
78	77	P52/EX18	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
77	76	P53/EX18	I/O	Input/output port, External interrupt	—	—	—	—
76	75	P54/EX18	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SIN1	I	SSIO1 data input
75	74	P55/EX18	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
74	73	P56/EX18	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
73	72	P57/EX18	I/O	Input/output port, External interrupt	—	—	—	—

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary/Tertiary	Pin name	I/O	Function
23	22	COM0	O	LCD common pin	—	—	—	—
24	23	COM1	O	LCD common pin	—	—	—	—
25	24	COM2/ SEG0	O	LCD common/segment pin	—	—	—	—
26	25	COM3/ SEG1	O	LCD common/segment pin	—	—	—	—
27	26	COM4/ SEG2	O	LCD common/segment pin	—	—	—	—
28	27	SEG3	O	LCD segment pin	—	—	—	—
29	28	SEG4	O	LCD segment pin	—	—	—	—
30	29	SEG5	O	LCD segment pin	—	—	—	—
31	30	SEG6	O	LCD segment pin	—	—	—	—
32	31	SEG7	O	LCD segment pin	—	—	—	—
33	32	SEG8	O	LCD segment pin	—	—	—	—
34	33	SEG9	O	LCD segment pin	—	—	—	—
35	34	SEG10	O	LCD segment pin	—	—	—	—
36	35	SEG11	O	LCD segment pin	—	—	—	—
37	36	SEG12	O	LCD segment pin	—	—	—	—
38	37	SEG13	O	LCD segment pin	—	—	—	—
39	38	SEG14	O	LCD segment pin	—	—	—	—
40	39	SEG15	O	LCD segment pin	—	—	—	—
41	40	SEG16	O	LCD segment pin	—	—	—	—
42	41	SEG17	O	LCD segment pin	—	—	—	—
43	42	SEG18	O	LCD segment pin	—	—	—	—
44	43	SEG19	O	LCD segment pin	—	—	—	—
45	44	SEG20	O	LCD segment pin	—	—	—	—
46	45	SEG21	O	LCD segment pin	—	—	—	—
47	46	SEG22	O	LCD segment pin	—	—	—	—
48	47	SEG23	O	LCD segment pin	—	—	—	—
49	48	P67 <sup>(2)</sup>	O	Output port	—	—	—	—
		SEG24 <sup>(3)</sup>	O	LCD segment pin	—	—	—	—
50	49	P66 <sup>(2)</sup>	O	Output port	—	—	—	—
		SEG25 <sup>(3)</sup>	O	LCD segment pin	—	—	—	—
51	50	P65 <sup>(2)</sup>	O	Output port	—	—	—	—
		SEG26 <sup>(3)</sup>	O	LCD segment pin	—	—	—	—
52	51	P64 <sup>(2)</sup>	O	Output port	—	—	—	—
		SEG27 <sup>(3)</sup>	O	LCD segment pin	—	—	—	—
53	52	P63 <sup>(4)</sup>	O	Output port	—	—	—	—
		SEG28 <sup>(5)</sup>	O	LCD segment pin	—	—	—	—
54	53	P62 <sup>(4)</sup>	O	Output port	—	—	—	—
		SEG29 <sup>(5)</sup>	O	LCD segment pin	—	—	—	—
55	54	P61 <sup>(4)</sup>	O	Output port	—	—	—	—
		SEG30 <sup>(5)</sup>	O	LCD segment pin	—	—	—	—
56	55	P60 <sup>(4)</sup>	O	Output port	—	—	—	—
		SEG31 <sup>(5)</sup>	O	LCD segment pin	—	—	—	—

(\*<sup>1</sup>) Internally generated, or connect to either positive power supply pin (V<sub>DD</sub>) or power supply pin for internal logic (V<sub>DDL</sub>). For details, see user's manual.

(\*<sup>2</sup>) Pin for ML610404

(\*<sup>3</sup>) Pin for ML610405/ML610406

(\*<sup>4</sup>) Pin for ML610404/ML610405

(\*<sup>5</sup>) Pin for ML610406

**PIN DESCRIPTION**

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
<b>System</b>				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal resonator is connected to this pin. Capacitors C <sub>DL</sub> and C <sub>GL</sub> are connected across this pin and V <sub>SS</sub> . (see measuring circuit 1) .	—	—
LSCLK	O	Low-speed clock output. Assigned to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
<b>General-purpose input port</b>				
P00 to P04	I	General-purpose input port.	Primary	Positive
<b>General-purpose output port</b>				
P20 to P22, P24	O	General-purpose output port. This cannot be used as the general output port when used as the secondary function.	Primary	Positive
<b>General-purpose input/output port</b>				
P30 to P35	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P40 to P47	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary or tertiary function.	Primary	Positive
P50 to P57	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P60 to P63	O	General-purpose output port. Incorporated only into ML610404/ML610405, and not into ML610406.	Primary	Positive
P64 to P67	O	General-purpose output port. Incorporated only into ML610404, and not into ML610405/ ML610406.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
<b>UART</b>				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
<b>Synchronous serial (SSIO)</b>				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Assigned to the tertiary function of the P51 pin and P55 pin.	Tertiary	—
SIN1	I	Synchronous serial data input pin. Assigned to the tertiary function of the P50 pin and P54 pin.	Tertiary	Positive
SOUT1	O	Synchronous serial data output pin. Assigned to the tertiary function of the P52 pin and P56 pin.	Tertiary	Positive
<b>PWM</b>				
PWM0	O	PWM0 output pin. This pin is used as the secondary function of the P24 and tertiary function of the P43 pin.	Secondary Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P04 pin and P44 pin.	Primary	—
<b>External interrupt</b>				
EXI0-4	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00 to P04 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. Assigned to the primary function of the P50 to P57 pins.	Primary	Positive/ negative
<b>Capture</b>				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software.	Primary	Positive/ negative
CAP1	I	These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
<b>Timer</b>				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. This pin is used as the primary function of the P04 pin and P44 pin.	Primary	—
T13CK	I	External clock input pin used for both Timer 1 and Timer 3. This pin is used as the primary function of the P45 pin.	Primary	—
<b>Melody</b>				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 and P50 pins.	Secondary	Positive/ negative
<b>LED drive</b>				
LED0 to LED2, LED4	O	N-channel open drain output pins to drive LED. This pin is used as the primary function of the P20 to P22 and P24 pins.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
<b>RC oscillation type A/D converter</b>				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
<b>LCD drive signal</b>				
COM0 to COM4	O	Common output pins. COM2, COM3, and COM4 can be switched to SEG0, SEG1, and SEG2, respectively, through the register setting. To change the setting, switch between COM4 and SEG2 for one pin and switch between COM3, COM4 and SEG1, SEG2 for two pins.	—	—
SEG0 to SEG23	O	Segment output pin. The SEG0, SEG1, and SEG2 pins are for switching the register setting with the COM2, COM3, and COM4.	—	—
SEG24 to SEG27	O	Segment output pin. Incorporated into ML610405/ML610406, not into ML610404.	—	—
SEG28 to SEG31	O	Segment output pin. Incorporated into ML610406, not into ML610404/ML610405.	—	—
<b>LCD driver power supply</b>				
V <sub>L1</sub>	—	Power supply pin for LCD bias (internally generated) or power supply connection pin. Depending on LCD Bias setting and V <sub>DD</sub> voltage level, V <sub>DD</sub> or V <sub>DDL</sub> or capacitor is connected.	—	—
V <sub>L2</sub>	—		—	—
V <sub>L3</sub>	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitor C <sub>12</sub> (see measuring circuit 1) is connected between C1 and C2.	—	—
C2	—		—	—
<b>For testing</b>				
TEST0	I/O	Pin for testing. A pull-down resistor is internally connected.	—	Positive
<b>Power supply</b>				
V <sub>SS</sub>	—	Negative power supply pin.	—	—
V <sub>DD</sub>	—	Positive power supply pin.	—	—
V <sub>DDL</sub>	—	Positive power supply pin (internally generated) for internal logic. Capacitor C <sub>L</sub> (see measuring circuit 1) is connected between this pin and V <sub>SS</sub> .	—	—

## TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

**Table 3 Termination of Unused Pins**

Pin	Recommended pin handling
VL1	Open
VL2	Open
VL3	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
P00 to P04	VDD or VSS
P20 to P22, P24	Open
P30 to P35	Open
P40 to P47	Open
P50 to P57	Open
P60 to P67	Open
COM0 to COM4	Open
SEG0 to SEG31	Open

**Note:**

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.



**ELECTRICAL CHARACTERISTICS**

**ABSOLUTE MAXIMUM RATINGS**

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V <sub>DD</sub>	Ta = 25°C	-0.3 to +4.6	V
Power supply voltage 2	V <sub>DDL</sub>	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 3	V <sub>L1</sub>	Ta = 25°C	-0.3 to +2.0	V
Power supply voltage 4	V <sub>L2</sub>	Ta = 25°C	-0.3 to +4.0	V
Power supply voltage 5	V <sub>L3</sub>	Ta = 25°C	-0.3 to +6.0	V
Input voltage	V <sub>IN</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>OUT</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output current 1	I <sub>OUT1</sub>	Port 3 to 6, Ta = 25°C	-12 to +11	mA
Output current 2	I <sub>OUT2</sub>	Port 2, Ta = 25°C	-12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T <sub>STG</sub>	—	-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T <sub>OP</sub>	without P version	-20 to +70	°C
		P version	-40 to +85	
Operating voltage	V <sub>DD</sub>	f <sub>OP</sub> = 30k to 625kHz	1.25 to 3.6	V
		f <sub>OP</sub> = 30k to 2.5MHz	1.8 to 3.6	
Operating frequency (CPU)	f <sub>OP</sub>	V <sub>DD</sub> = 1.25 to 3.6V	30k to 625k	Hz
		V <sub>DD</sub> = 1.8 to 3.6V	30k to 2.5M	
V <sub>DD</sub> pin external capacitance	C <sub>V</sub>	—	1.0±30% to 2.2±30%* <sup>1</sup>	μF
V <sub>DDL</sub> pin external capacitance	C <sub>L</sub>	—	0.47±30% to 2.2±30%* <sup>2</sup>	μF
V <sub>L1, 2, or 3</sub> pin external capacitance	C <sub>a, b, c</sub>	—	0.1±30%	μF
Pin-to-pin (C1 to C2) external capacitance	C <sub>12</sub>	—	0.47±30%	μF

\*<sup>1</sup>: Please select as C<sub>V</sub> is larger than C<sub>L</sub> or same as C<sub>L</sub>.

\*<sup>2</sup>: When the load of V<sub>DD</sub> is small and the power rise time is too short, it may happen that the power-on reset is not generated. In this case please select C<sub>L</sub> with larger capacitance

**CLOCK GENERATION CIRCUIT OPERATING CONDITIONS**

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f <sub>XTL</sub>	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R <sub>L</sub>	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor	C <sub>DL</sub> /C <sub>GL</sub>	C <sub>L</sub> =6pF of crystal oscillation	—	12	—	pF
		C <sub>L</sub> =9pF of crystal oscillation	—	18	—	
		C <sub>L</sub> =12pF of crystal oscillation	—	24	—	

**DC CHARACTERISTICS (1/5)**

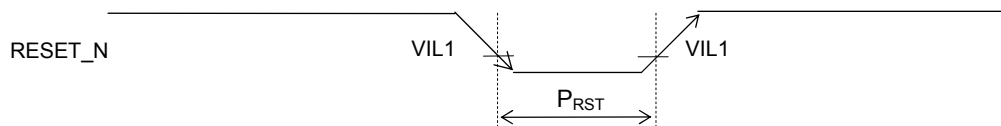
(V<sub>DD</sub>=1.25 to 3.6V, V<sub>SS</sub>=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
500kHz/2MHz RC oscillation frequency	f <sub>RC</sub>	V <sub>DD</sub> = 1.25 to 3.6V	Ta = 25°C	Typ. -10%	500	Typ. +10%	kHz	1
			*3	Typ. -25%	500	Typ. +25%		
		V <sub>DD</sub> = 1.80 to 3.6V	Ta = 25°C	Typ. -10%	2.0	Typ. +10%	MHz	
			*3	Typ. -25%	2.0	Typ. +25%		
Low-speed crystal oscillation start time*2	T <sub>XTL</sub>	—		—	0.6	2	s	
500kHz/2MHz RC oscillation start time	T <sub>RC</sub>	—		—	—	3	μs	
Low-speed oscillation stop detect time*1	T <sub>STOP</sub>	—		12	16.4	41	ms	
Reset pulse width	P <sub>RST</sub>	—		200	—	—	μs	
Reset noise elimination pulse width	P <sub>NRST</sub>	—		—	—	0.3		
Power-on reset generated power rise time	T <sub>POR</sub>	—		—	—	10	ms	

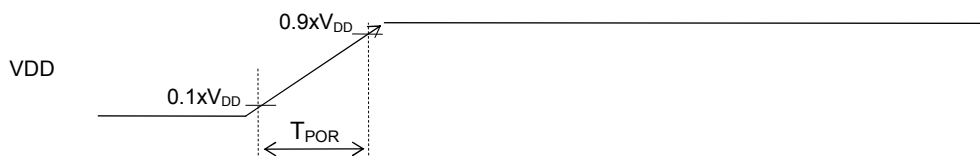
\*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

\*2: 32.768KHz Crystal resonator DT-26 (Load Capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C<sub>GL</sub>=C<sub>DL</sub>=6pF)

\*3: Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)



**Reset pulse width (P<sub>RST</sub>)**



**Power-on reset activation power rise time (T<sub>POR</sub>)**

**DC CHARACTERISTICS (2/5)**

( $V_{DD}=1.25$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a=-20$  to  $+70^{\circ}C$ ,  $T_a=-40$  to  $+85^{\circ}C$  for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
V <sub>DDL</sub> voltage	V <sub>DDL</sub>	f <sub>OP</sub> = 30k to 625kHz	1.1	1.2	1.3	V	1
		f <sub>OP</sub> = 30k to 2.5MHz	1.35	1.5	1.65		
V <sub>DDL</sub> temperature deviation *1	ΔV <sub>DDL</sub>	V <sub>DD</sub> = 3.0V	—	-1	—	mV/°C	
V <sub>DDL</sub> voltage dependency *1	ΔV <sub>DDL</sub>	—	—	5	20	mV/V	

\*1: The maximum V<sub>DDL</sub> voltage becomes the V<sub>DD</sub> voltage level when the V<sub>DDL</sub> voltage determined by the temperature and voltage deviations mathematically exceeds the V<sub>DD</sub> voltage.

**DC CHARACTERISTICS (3/5)**

(V<sub>DD</sub>=3.0V, V<sub>SS</sub>=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit	
			Min.	Typ.	Max.			
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta= 25°C	—	0.4	0.8	μA	1
			*5	—	—	6.5		
Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating). <sup>*3,*4</sup> High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. <sup>*6</sup>	Ta= 25°C	—	0.9	1.8	μA	
			*5	—	—	7.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state. <sup>*1,*3</sup> High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. <sup>*2</sup>	Ta= 25°C	—	4.0	7.5	μA	
			*5	—	—	11.0		
Supply current 4-1	IDD4-1	CPU: In 500kHz RC operating state. LCD/BIAS circuits: Operating. <sup>*2</sup>	Ta= 25°C	—	60	80	μA	
			*5	—	—	90		
Supply current 4-2	IDD4-2	CPU: In 2MHz RC operating state. LCD/BIAS circuits: Operating. <sup>*2</sup>	Ta= 25°C	—	240	300	μA	
			*5	—	—	320		

\*1: When the CPU operating rate is 100% (No HALT state).

\*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

\*3: 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C<sub>GL</sub>=C<sub>DL</sub>=6pF).

\*4: Significant bits of BLKCON0 to BLKCON4 registers are all "1" except DLCD bit on BLKCON4.

\*5: Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)

\*6: LCD stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

**DC CHARACTERISTICS (4/5)**

( $V_{DD}=1.25$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a=-20$  to  $+70^{\circ}C$ ,  $T_a=-40$  to  $+85^{\circ}C$  for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit		
			Min.	Typ.	Max.				
Output voltage 1 (P20 to P22,P24 (N-channel open drain output mode is not selected)) (P30 to P35) (P40 to P47) (P50 to P57) (P60 to P63) <sup>*2</sup> (P60 to P67) <sup>*1</sup>	VOH1	IOH1 = -0.5mA, $V_{DD} = 1.8$ to $3.6V$	$V_{DD}$ -0.5	—	—	V	2		
		IOH1 = -0.03mA, $V_{DD} = 1.25$ to $3.6V$	$V_{DD}$ -0.3	—	—				
	VOL1	IOL1 = +0.5mA, $V_{DD} = 1.8$ to $3.6V$	—	—	0.5				
		IOL1 = +0.1mA, $V_{DD} = 1.25$ to $3.6V$	—	—	0.3				
Output voltage 2 (P20 to P22,P24 (N-channel open drain output mode is not selected))	VOL2	IOL2 = +5mA, $V_{DD} = 1.8$ to $3.6V$	—	—	0.5			V	2
Output voltage 3 (COM0 to 4) (SEG0 to 23) <sup>*1</sup> (SEG0 to 27) <sup>*2</sup> (SEG0 to 31) <sup>*3</sup>	VOH3	IOH3 = -0.05mA, $V_{L1}=1.2V$	$V_{L3}$ -0.2	—	—				
	VOML3	IOML3 = +0.05mA, $V_{L1}=1.2V$	—	—	$V_{L2}$ +0.2				
	VOML3S	IOML3S = -0.05mA, $V_{L1}=1.2V$	$V_{L2}$ -0.2	—	—				
	VOLM3	IOLM3 = +0.05mA, $V_{L1}=1.2V$	—	—	$V_{L1}$ +0.2				
	VOLM3S	IOLM3S = -0.05mA, $V_{L1}=1.2V$	$V_{L1}$ -0.2	—	—				
	VOL3	IOL3 = +0.05mA, $V_{L1}=1.2V$	—	—	0.2				
Output leakage (P20 to P22,P24) (P30 to P35) (P40 to P47) (P50 to P57) (P60 to P63) <sup>*2</sup> (P60 to P67) <sup>*1</sup>	IOOH	VOH = $V_{DD}$ (in high-impedance state)	—	—	1	$\mu A$	3		
	IOOL	VOL = $V_{SS}$ (in high-impedance state)	-1	—	—				
Input current 1 (RESET_N)	I IH1	$V_{IH1} = V_{DD}$	—	—	1	$\mu A$	4		
	I IL1	$V_{IL1} = V_{SS}$	-600	-300	-2				
Input current 2 (TEST0)	I IH2	$V_{IH2} = V_{DD}$	2	300	600				
	I IL2	$V_{IL2} = V_{SS}$	-1	—	—				
Input current 3 (P00 to P04) (P30 to P35) (P40 to P47) (P50 to P57)	I IH3	$V_{IH3} = V_{DD}$ , $V_{DD} = 1.8$ to $3.6V$ (when pulled-down)	2	30	200				
		$V_{IH3} = V_{DD}$ , $V_{DD} = 1.25$ to $3.6V$ (when pulled-down)	0.01	30	200				
	I IL3	$V_{IL3} = V_{SS}$ , $V_{DD} = 1.8$ to $3.6V$ (when pulled-up)	-200	-30	-2				
		$V_{IL3} = V_{SS}$ , $V_{DD} = 1.25$ to $3.6V$ (when pulled-up)	-200	-30	-0.01				
	I IH3Z	$V_{IH3} = V_{DD}$ (in high-impedance state)	—	—	1				
	I IL3Z	$V_{IL3} = V_{SS}$ (in high-impedance state)	-1	—	—				

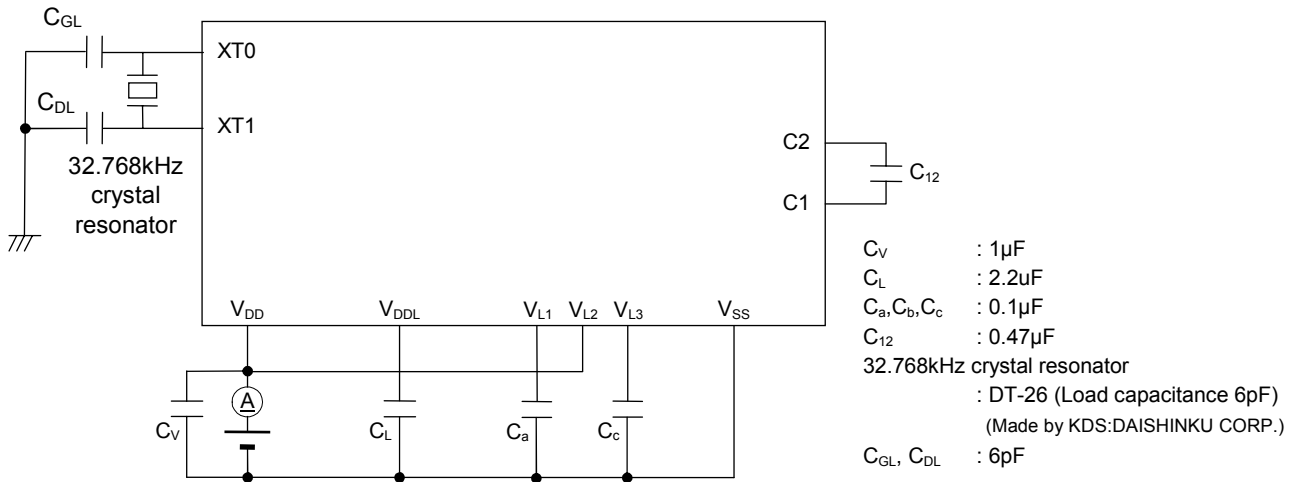
\*1: Characteristics for ML610404  
\*2: Characteristics for ML610405  
\*3: Characteristics for ML610406

**DC CHARACTERISTICS (5/5)**

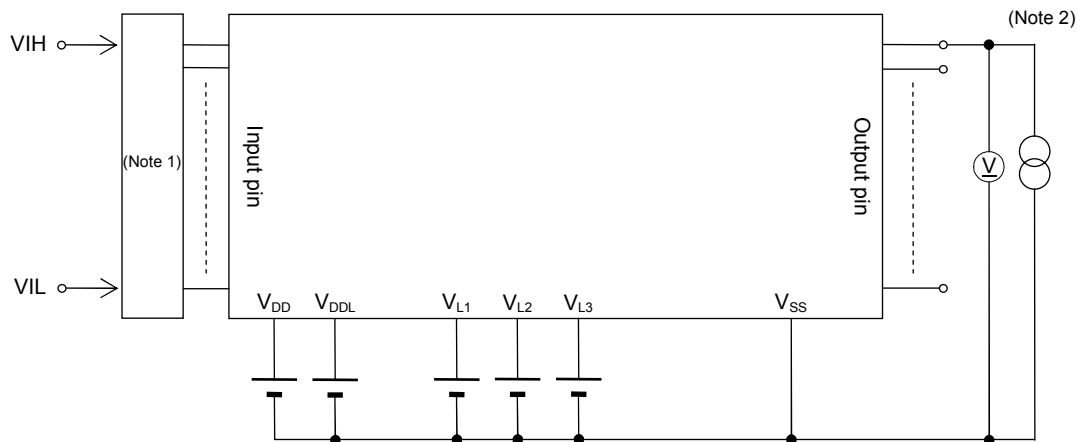
( $V_{DD}=1.25$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a=-20$  to  $+70^{\circ}C$ ,  $T_a=-40$  to  $+85^{\circ}C$  for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (P00 to P04) (P30 to P35) (P40 to P47) (P50 to P57)	VIH1	—	0.7 $\times V_{DD}$	—	$V_{DD}$	V	5
	VIL1	$V_{DD} = 1.8$ to $3.6V$	0	—	0.3 $\times V_{DD}$		
		$V_{DD} = 1.25$ to $3.6V$	0	—	0.2 $\times V_{DD}$		
Input pin capacitance (P00 to P04) (P30 to P35) (P40 to P47) (P50 to P57)	CIN	f = 10kHz $V_{rms} = 50mV$ $T_a = 25^{\circ}C$	—	—	5	pF	—

**MEASURING CIRCUITS**

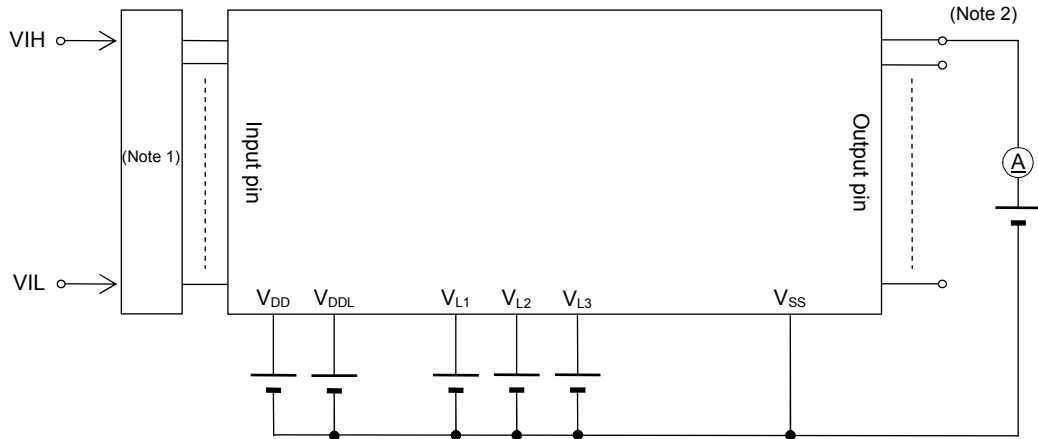


**MEASURING CIRCUIT 2**



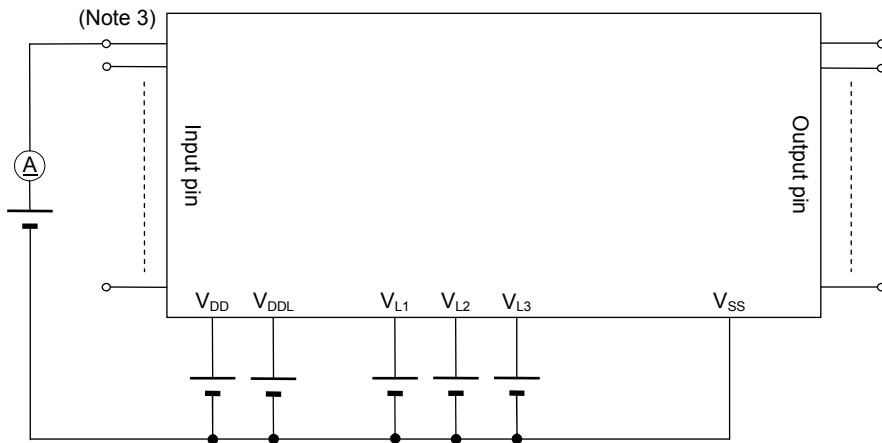
(Note 1) Input logic circuit to determine the specified measuring conditions.  
 (Note 2) Repeats for the specified output pin

**MEASURING CIRCUIT 3**



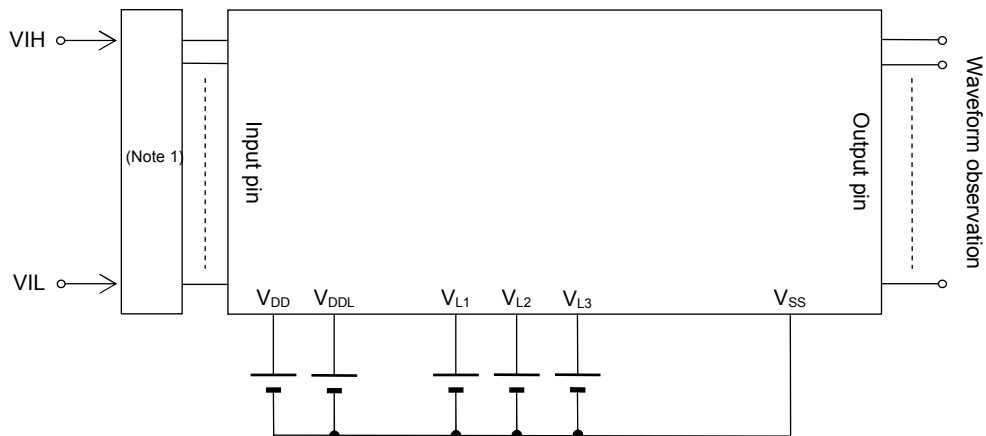
(Note 1) Input logic circuit to determine the specified measuring conditions.  
(Note 2) Repeats for the specified output pin

**MEASURING CIRCUIT 4**



(Note 3) Repeats for the specified input pin

**MEASURING CIRCUIT 5**



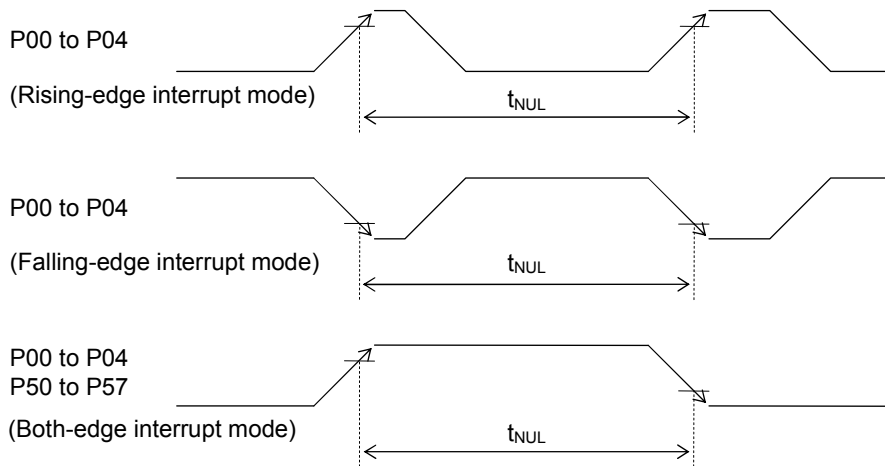
(Note 1) Input logic circuit to determine the specified measuring conditions.



**AC CHARACTERISTICS (External Interrupt)**

(V<sub>DD</sub>=1.25 to 3.6V, V<sub>SS</sub>=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T <sub>NUL</sub>	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

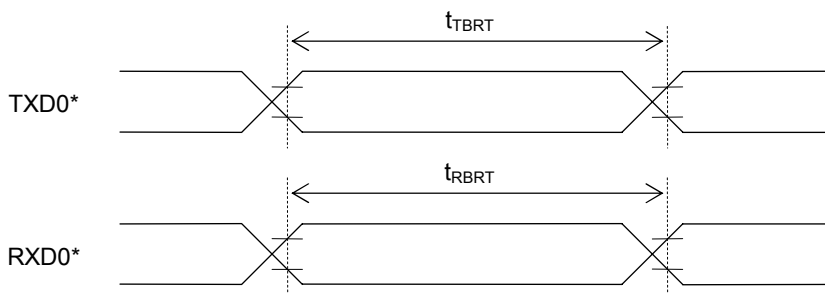


**AC CHARACTERISTICS (UART)**

(V<sub>DD</sub>=1.25 to 3.6V, V<sub>SS</sub>=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t <sub>TBRT</sub>	—	—	BRT* <sup>1</sup>	—	s
Receive baud rate	t <sub>RBRT</sub>	—	BRT* <sup>1</sup> -3%	BRT* <sup>1</sup>	BRT* <sup>1</sup> +3%	s

\*1: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



\*: Indicates the secondary function of the port.

**AC CHARACTERISTICS (Synchronous Serial Port)**

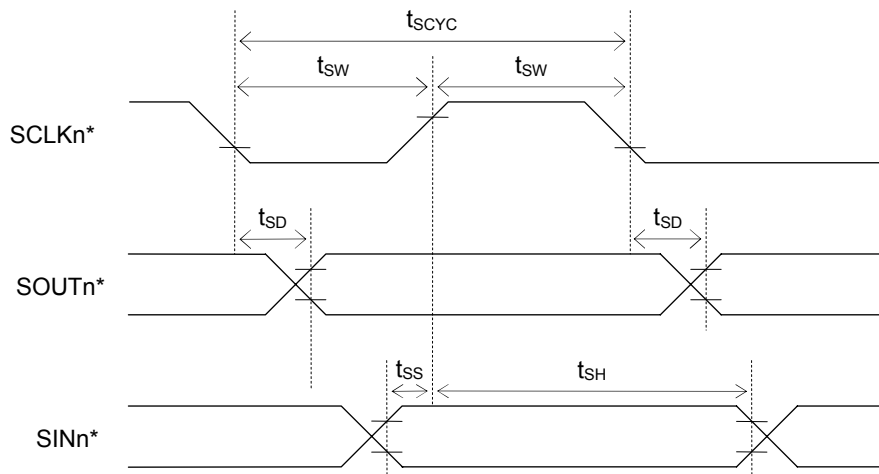
( $V_{DD}=1.25$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a=-20$  to  $+70^{\circ}C$ ,  $T_a=-40$  to  $+85^{\circ}C$  for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	$t_{SCYC}$	In the 500kHz oscillation mode* <sup>2</sup>	10	—	—	$\mu s$
		In the 2MHz oscillation mode* <sup>3</sup> $V_{DD}=1.8$ to $3.6V$	1	—	—	$\mu s$
SCLK output cycle (master mode)	$t_{SCYC}$	—	—	SCLK* <sup>1</sup>	—	s
SCLK input pulse width (slave mode)	$t_{SW}$	In the 500kHz oscillation mode* <sup>2</sup>	4	—	—	$\mu s$
		In the 2MHz oscillation mode* <sup>3</sup> $V_{DD}=1.8$ to $3.6V$	0.4	—	—	$\mu s$
SCLK output pulse width (master mode)	$t_{SW}$	—	SCLK* <sup>1</sup> $\times 0.4$	SCLK* <sup>1</sup> $\times 0.5$	SCLK* <sup>1</sup> $\times 0.6$	s
SOUT output delay time (slave mode)	$t_{SD}$	In the 500kHz oscillation mode* <sup>2</sup> Output load 10pF	—	—	500	ns
		In the 2MHz oscillation mode* <sup>3</sup> Output load 10pF	—	—	240	
SOUT output delay time (master mode)	$t_{SD}$	In the 500kHz oscillation mode* <sup>2</sup> Output load 10pF	—	—	500	ns
		In the 2MHz oscillation mode* <sup>3</sup> Output load 10pF, $V_{DD}=1.8$ to $3.6V$	—	—	240	
SIN input setup time (slave mode)	$t_{SS}$	—	80	—	—	ns
SIN input setup time (master mode)	$t_{SS}$	In the 500kHz oscillation mode* <sup>2</sup>	500	—	—	ns
		In the 2MHz oscillation mode* <sup>3</sup> $V_{DD}=1.8$ to $3.6V$	240	—	—	
SIN input hold time	$t_{SH}$	In the 500kHz oscillation mode* <sup>2</sup>	300	—	—	ns
		In the 2MHz oscillation mode* <sup>3</sup> $V_{DD}=1.8$ to $3.6V$	80	—	—	

\*<sup>1</sup>: Clock cycle selected with SnCK2–0 of the serial port n mode register (SIO nMOD1) (n= 0, 1)

\*<sup>2</sup>: When 500kHz oscillation is selected with OSCM2 of the frequency control register 0 (FCON0)

\*<sup>3</sup>: When 2MHz oscillation is selected with OSCM2 of the frequency control register 0 (FCON0)



\*: Indicates the tertiary function of the port (n= 0,1)

**AC CHARACTERISTICS (RC Oscillation A/D Converter)**

Condition for  $V_{DD}=1.8$  to  $3.6V$

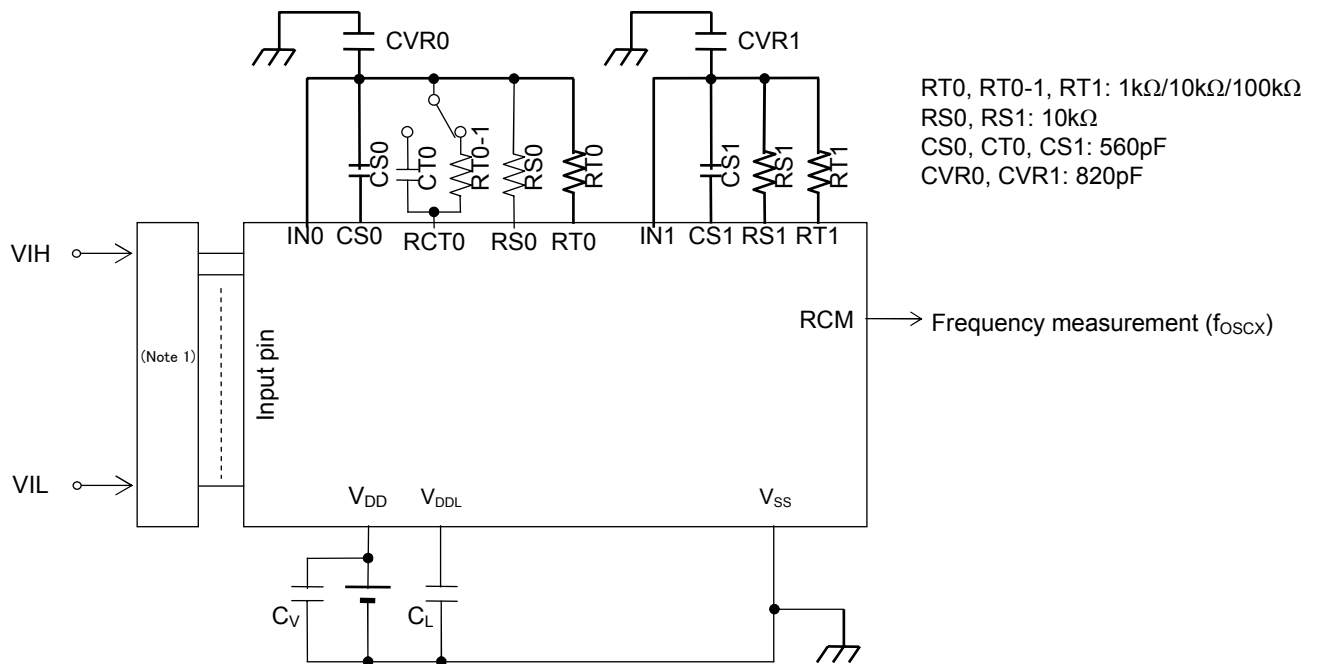
( $V_{DD}=1.8$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a=-20$  to  $+70^\circ C$ ,  $T_a=-40$  to  $+85^\circ C$  for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1 $\geq$ 740pF	1	—	—	k $\Omega$
Oscillation frequency $V_{DD} = 3.0V$	$f_{OSC1}$	Resistor for oscillation=1k $\Omega$	457.3	525.2	575.1	kHz
	$f_{OSC2}$	Resistor for oscillation=10k $\Omega$	53.48	58.18	62.43	kHz
	$f_{OSC3}$	Resistor for oscillation=100k $\Omega$	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio <sup>*1</sup> $V_{DD} = 3.0V$	Kf1	RT0, RT0-1, RT1=1k $\Omega$	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1, RT1=10k $\Omega$	0.981	1	1.019	—
	Kf3	RT0, RT0-1, RT1=100k $\Omega$	0.099	0.101	0.104	—

\*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{oscx}(RT0-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \frac{f_{oscx}(RT0-1-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \frac{f_{oscx}(RT1-CS1 \text{ oscillation})}{f_{oscx}(RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)



\*1: Input logic circuit to determine the specified measuring conditions.



**Revision History**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610406-01	Dec.15,2011	–	–	Final edition
FEDL610406-02	Dec.5,2012	15	15	Remove the word "appendixC" in the table.
		17	17	Correct the symbol of capacitor at $V_{DDL}$ .
		19	19	The notes about $C_V$ , $C_L$ were added.
		19,25	19,25	The value of capacitor $C_L$ was changed to 2.2uF.
FEDL610406-03	Feb.21,2014	All	All	Change header and footer
		3	4	Change from "Shipment" to " Product name – Supported Function "
		20	18	Correct minimum time of Power-on reset generated power rise time
		3,5,6,7,31	4	Delete package products
FEDL610406-04	Apr.18,2014	4	4	Correct the "Product name – Supported Function"
FEDL610406-05	May.23,2014	-	17	Add Clock Generation Circuit Operating Conditions
		18	18	Change "RESET" to " Reset pulse width ( $P_{RST}$ )" and " Power-on reset activation power rise time ( $T_{POR}$ )".
		18	18	Correct minimum time of Power-on reset generated power rise time
		18	18	Correct the $C_{GL}$ 's value and the $C_{DL}$ 's value of DC CHARACTERISTICS (1/5)'s note No.2

NOTES

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