ML610421

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), melody driver, battery level detect circuit, RC oscillation type A/D converter, 12-bit successive approximation type A/D converter, and LCD driver, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel procesing. This LSI operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    0.24 4μs (@4.096 MHz system clock)

- Internal memory
  - Internal 32KBbyte mask ROM (16K×16 bits) (including unusable 1KByte TEST area)
  - Internal 1KByte Data RAM (1024×8 bits), 1KByte Display Allocation RAM (1024 x 8bit)
  - Internal 100Byte RAM for display

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 20 maskable interrupt sources (Internal sources: 16, External sources: 4)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- 1 kHz timer
  – 10 Hz/1 Hz interrupt function

- Capture
  – Time base capture × 2 channels (4096 Hz to 32 Hz)

- PWM
  – Resolution 16 bits × 1 channel

- Synchronous serial port
  – Master/slave selectable
  – LSB first/MSB first selectable
  – 8-bit length/16-bit length selectable

- UART
  – TXD/RXD × 1 channel
  – Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  – Positive logic/negative logic selectable
  – Built-in baud rate generator

- I^2C bus interface
  – Master function only
  – Fast mode (400 kbps@4MHz), standard mode (100 kbps@1MHz, 50kbps@500kHz)

- Melody driver
  – Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  – Tone length: 63 types
  – Tempo: 15 types
  – Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  – 24-bit counter
  – Time division × 2 channels

- Successive approximation type A/D converter
  – 12-bit A/D converter
  – Input × 2 channels

- General-purpose ports
  – Non-maskable interrupt input port × 1 channel
  – Input-only port × 6 channels (including secondary functions)
  – Output-only port × 3 channels (including secondary functions)
  – Input/output port
    ML610421: 22 channels (including secondary functions)

- LCD driver
  - Dot matrix can be supported.
    ML610421: 400 dots max. (50 seg × 8 com), 1/1 to 1/8 duty
  - 1/3 or 1/4 bias (built-in bias generation circuit)
  - Frame frequency selecable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function (available only when 1/1~1/8 duty is selected)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  - Operating temperature: –20°C to 70°C (P version: –40°C to +85°C)
  - Operating voltage: V_{DD} = 1.1V to 3.6V, AV_{DD} = 2.2V to 3.6V

- Product name – Supported Function
  The line-up of the ML610421 is below.

- Chip (Die) -	ROM type	Operating temperature	Product availability
ML610421-xxxWA	Mask ROM	-20°C to +70°C	Yes
ML610422-xxxWA	Mask ROM	-20°C to +70°C	-
ML610421P-xxxWA	Mask ROM	-40°C to +85°C	-
ML610422P-xxxWA	Mask ROM	-40°C to +85°C	-

-120-pin plastic TQFP -	ROM type	Operating temperature	Product availability
ML610421-xxxTB	Mask ROM	-20°C to +70°C	-
ML610422-xxxTB	Mask ROM	-20°C to +70°C	-
ML610421P-xxxTB	Mask ROM	-40°C to +85°C	-
ML610422P-xxxTB	Mask ROM	-40°C to +85°C	-

xxx: ROM code number (xxx of the blank product is NNN)
Q: Flash ROM version
P: Wide range temperature version (P version)
WA: Chip (Die),
TB: TQFP

BLOCK DIAGRAM

ML610421 Block Diagram

Figure 1 show the block diagram of the ML610421.
"*" indicates the secondary function of each port.

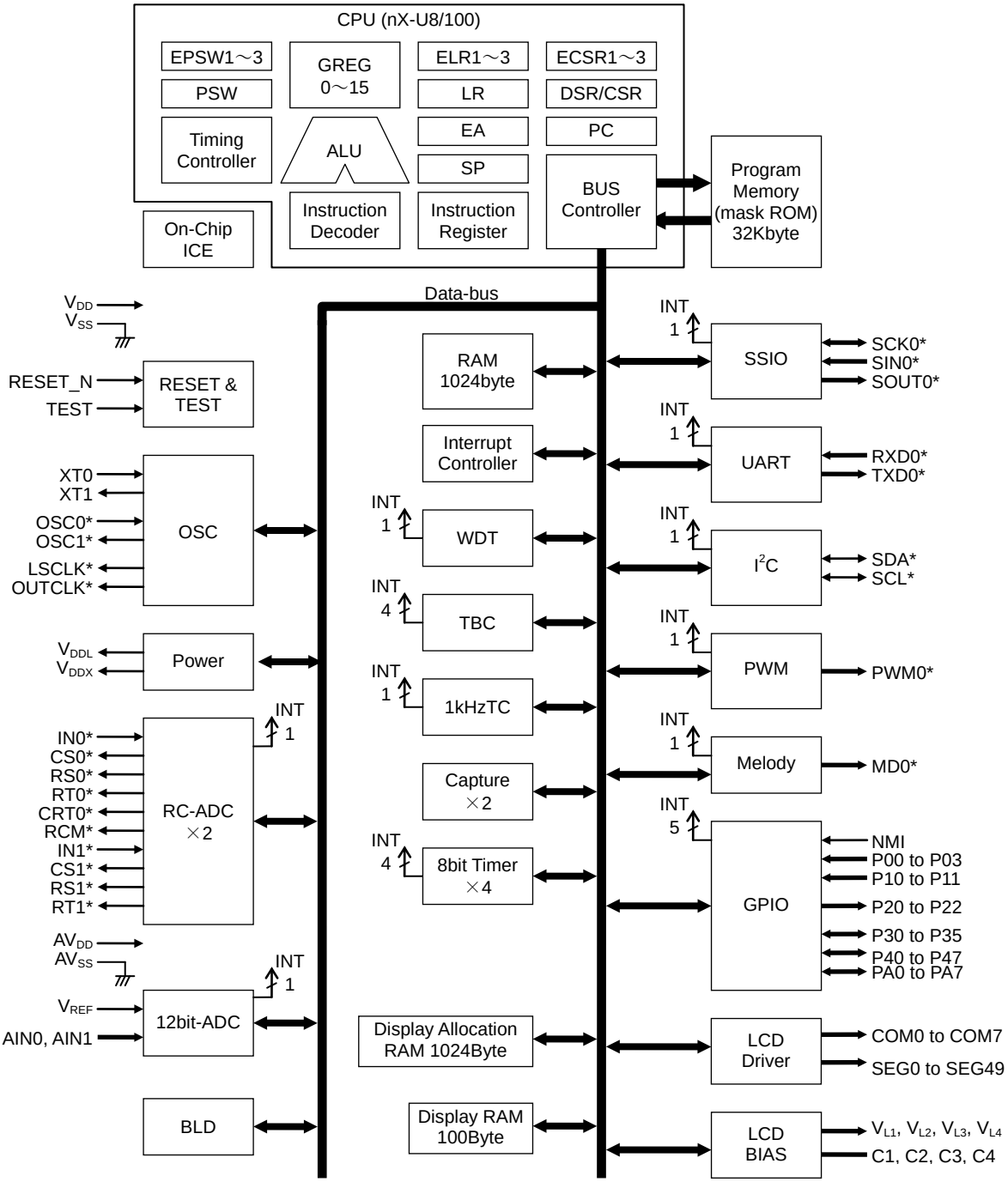
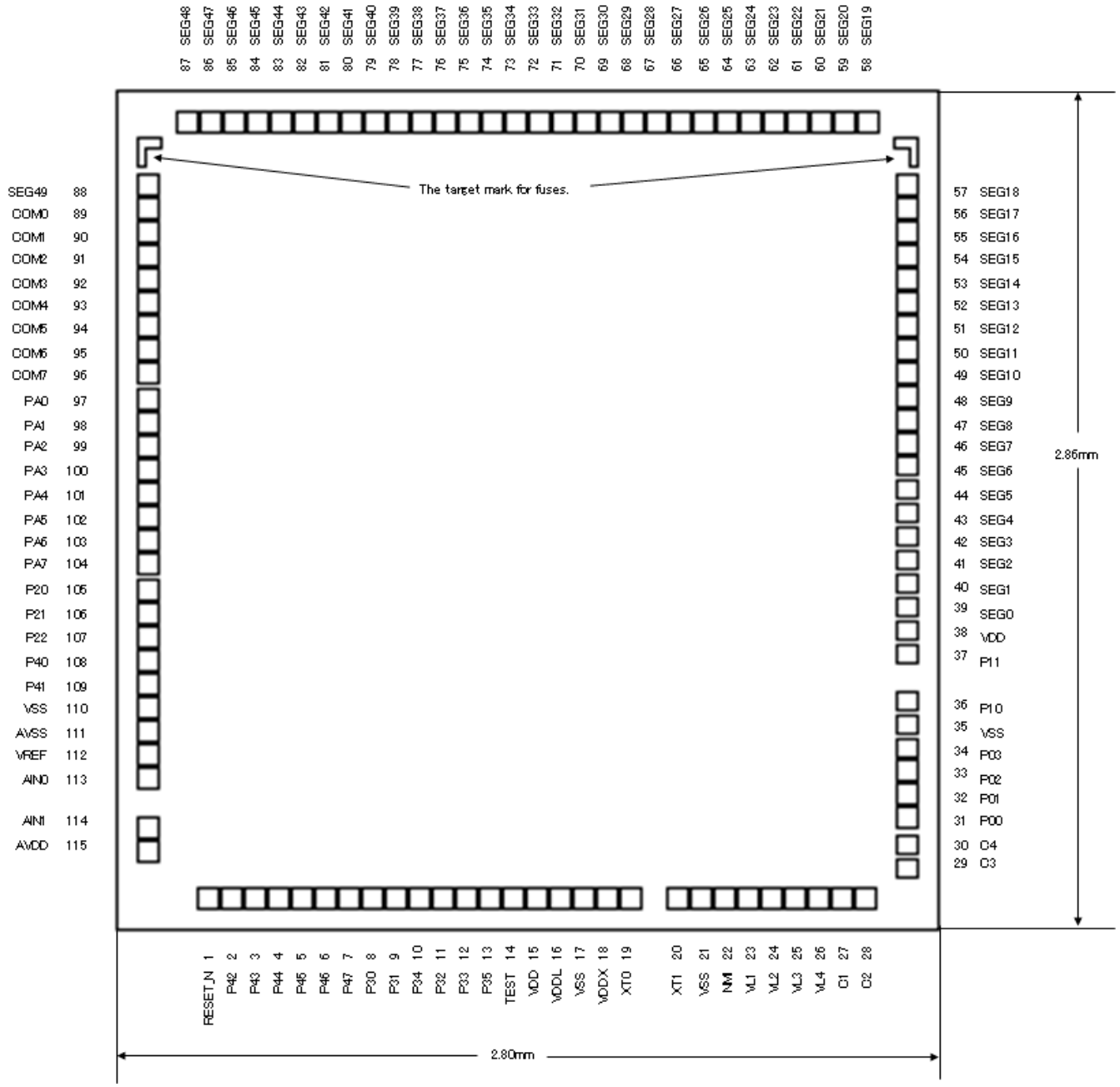


Figure 1 ML610421 Block Diagram

ML610421 Chip Pin Layout & Dimension



Note:

The assignment of the pads P30 to P35 are not in order.

Chip size:	2.80 mm × 2.86 mm
PAD count:	115 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 2 ML610421 Chip Layout & Dimension

PAD COORDINATES

ML610421 Pad Coordinates

Table 1 ML610421 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	RESET_N	-1090	-1324	51	SEG12	1294	630	101	PA4	-1294	60
2	P42	-1010	-1324	52	SEG13	1294	710	102	PA5	-1294	-20
3	P43	-930	-1324	53	SEG14	1294	790	103	PA6	-1294	-100
4	P44	-850	-1324	54	SEG15	1294	870	104	PA7	-1294	-180
5	P45	-770	-1324	55	SEG16	1294	950	105	P20	-1294	-270
6	P46	-690	-1324	56	SEG17	1294	1030	106	P21	-1294	-350
7	P47	-610	-1324	57	SEG18	1294	1110	107	P22	-1294	-430
8	P30	-530	-1324	58	SEG19	1160	1324	108	P40	-1294	-510
9	P31	-450	-1324	59	SEG20	1080	1324	109	P41	-1294	-590
10	P34	-370	-1324	60	SEG21	1000	1324	110	Vss	-1294	-670
11	P32	-290	-1324	61	SEG22	920	1324	111	AVss	-1294	-750
12	P33	-210	-1324	62	SEG23	840	1324	112	VREF	-1294	-830
13	P35	-130	-1324	63	SEG24	760	1324	113	AIN0	-1294	-910
14	TEST	-50	-1324	64	SEG25	680	1324	114	AIN1	-1294	-1082
15	VDD	30	-1324	65	SEG26	600	1324	115	AVDD	-1294	-1162
16	VDDL	110	-1324	66	SEG27	520	1324				
17	Vss	190	-1324	67	SEG28	440	1324				
18	VDDX	270	-1324	68	SEG29	360	1324				
19	XT0	350	-1324	69	SEG30	280	1324				
20	XT1	510	-1324	70	SEG31	200	1324				
21	Vss	590	-1324	71	SEG32	120	1324				
22	NMI	670	-1324	72	SEG33	40	1324				
23	VL1	750	-1324	73	SEG34	-40	1324				
24	VL2	830	-1324	74	SEG35	-120	1324				
25	VL3	910	-1324	75	SEG36	-200	1324				
26	VL4	990	-1324	76	SEG37	-280	1324				
27	C1	1070	-1324	77	SEG38	-360	1324				
28	C2	1150	-1324	78	SEG39	-440	1324				
29	C3	1294	-1220	79	SEG40	-520	1324				
30	C4	1294	-1140	80	SEG41	-600	1324				
31	P00	1294	-1050	81	SEG42	-680	1324				
32	P01	1294	-970	82	SEG43	-760	1324				
33	P02	1294	-890	83	SEG44	-840	1324				
34	P03	1294	-810	84	SEG45	-920	1324				
35	Vss	1294	-730	85	SEG46	-1000	1324				
36	P10	1294	-650	86	SEG47	-1080	1324				
37	P11	1294	-490	87	SEG48	-1160	1324				
38	VDD	1294	-410	88	SEG49	-1294	1110				
39	SEG0	1294	-330	89	COM0	-1294	1030				
40	SEG1	1294	-250	90	COM1	-1294	950				
41	SEG2	1294	-170	91	COM2	-1294	870				
42	SEG3	1294	-90	92	COM3	-1294	790				
43	SEG4	1294	-10	93	COM4	-1294	710				
44	SEG5	1294	70	94	COM5	-1294	630				
45	SEG6	1294	150	95	COM6	-1294	550				
46	SEG7	1294	230	96	COM7	-1294	470				
47	SEG8	1294	310	97	PA0	-1294	380				
48	SEG9	1294	390	98	PA1	-1294	300				
49	SEG10	1294	470	99	PA2	-1294	220				
50	SEG11	1294	550	100	PA3	-1294	140				

PIN LIST

PAD NO.	Primary function			Secondary function			Tertiary function		
421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
17,21, 35,110	Vss	—	Negative power supply pin	—	—	—	—	—	—
15,38	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
16	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
18	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
111	AV_{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
115	AV_{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
23	V_{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
24	V_{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
25	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
26	V_{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
27	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
28	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
29	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
30	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
14	TEST	I	Input pin for testing	—	—	—	—	—	—
1	RESET_N	I	Reset input pin	—	—	—	—	—	—
19	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
20	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
112	V_{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—
113	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
114	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—

PAD NO.	Primary function			Secondary function			Tertiary function		
421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
22	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
31	P00/ EXI0/ CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
32	P01/ EXI1/ CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
33	P02/ EXI2/ RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
34	P03/ EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
36	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
37	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
105	P20/ LED0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
106	P21/ LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
107	P22/ LED2	O	Output port	MD0	O	Melody output	—	—	—
8	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
9	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
10	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
11	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
12	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
13	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
108	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO data input
109	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO synchronous clock
2	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	I	SSIO data output
3	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
4	P44/ T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
5	P45/ T13P1CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
6	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
7	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
97	PA0	I/O	Input/output port	—	—	—	—	—	—
98	PA1	I/O	Input/output port	—	—	—	—	—	—
99	PA2	I/O	Input/output port	—	—	—	—	—	—
100	PA3	I/O	Input/output port	—	—	—	—	—	—
101	PA4	I/O	Input/output port	—	—	—	—	—	—
102	PA5	I/O	Input/output port	—	—	—	—	—	—
103	PA6	I/O	Input/output port	—	—	—	—	—	—
104	PA7	I/O	Input/output port	—	—	—	—	—	—
89	COM0	O	LCD common pin	—	—	—	—	—	—
90	COM1	O	LCD common pin	—	—	—	—	—	—
91	COM2	O	LCD common pin	—	—	—	—	—	—

PAD NO.	Primary function			Secondary function			Tertiary function		
421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
92	COM3	O	LCD common pin	—	—	—	—	—	—
93	COM4	O	LCD common pin	—	—	—	—	—	—
94	COM5	O	LCD common pin	—	—	—	—	—	—
95	COM6	O	LCD common pin	—	—	—	—	—	—
96	COM7	O	LCD common pin	—	—	—	—	—	—
—	COM8	O	LCD common pin	—	—	—	—	—	—
—	COM9	O	LCD common pin	—	—	—	—	—	—
—	COM10	O	LCD common pin	—	—	—	—	—	—
—	COM11	O	LCD common pin	—	—	—	—	—	—
—	COM12	O	LCD common pin	—	—	—	—	—	—
—	COM13	O	LCD common pin	—	—	—	—	—	—
—	COM14	O	LCD common pin	—	—	—	—	—	—
—	COM15	O	LCD common pin	—	—	—	—	—	—
39	SEG0	O	LCD segment pin	—	—	—	—	—	—
40	SEG1	O	LCD segment pin	—	—	—	—	—	—
41	SEG2	O	LCD segment pin	—	—	—	—	—	—
42	SEG3	O	LCD segment pin	—	—	—	—	—	—
43	SEG4	O	LCD segment pin	—	—	—	—	—	—
44	SEG5	O	LCD segment pin	—	—	—	—	—	—
45	SEG6	O	LCD segment pin	—	—	—	—	—	—
46	SEG7	O	LCD segment pin	—	—	—	—	—	—
47	SEG8	O	LCD segment pin	—	—	—	—	—	—
48	SEG9	O	LCD segment pin	—	—	—	—	—	—
49	SEG10	O	LCD segment pin	—	—	—	—	—	—
50	SEG11	O	LCD segment pin	—	—	—	—	—	—
51	SEG12	O	LCD segment pin	—	—	—	—	—	—
52	SEG13	O	LCD segment pin	—	—	—	—	—	—
53	SEG14	O	LCD segment pin	—	—	—	—	—	—
54	SEG15	O	LCD segment pin	—	—	—	—	—	—
55	SEG16	O	LCD segment pin	—	—	—	—	—	—
56	SEG17	O	LCD segment pin	—	—	—	—	—	—
57	SEG18	O	LCD segment pin	—	—	—	—	—	—
58	SEG19	O	LCD segment pin	—	—	—	—	—	—
59	SEG20	O	LCD segment pin	—	—	—	—	—	—
60	SEG21	O	LCD segment pin	—	—	—	—	—	—
61	SEG22	O	LCD segment pin	—	—	—	—	—	—
62	SEG23	O	LCD segment pin	—	—	—	—	—	—
63	SEG24	O	LCD segment pin	—	—	—	—	—	—
64	SEG25	O	LCD segment pin	—	—	—	—	—	—
65	SEG26	O	LCD segment pin	—	—	—	—	—	—
66	SEG27	O	LCD segment pin	—	—	—	—	—	—
67	SEG28	O	LCD segment pin	—	—	—	—	—	—
68	SEG29	O	LCD segment pin	—	—	—	—	—	—
69	SEG30	O	LCD segment pin	—	—	—	—	—	—
70	SEG31	O	LCD segment pin	—	—	—	—	—	—
71	SEG32	O	LCD segment pin	—	—	—	—	—	—
72	SEG33	O	LCD segment pin	—	—	—	—	—	—
73	SEG34	O	LCD segment pin	—	—	—	—	—	—
74	SEG35	O	LCD segment pin	—	—	—	—	—	—
75	SEG36	O	LCD segment pin	—	—	—	—	—	—
76	SEG37	O	LCD segment pin	—	—	—	—	—	—
77	SEG38	O	LCD segment pin	—	—	—	—	—	—
78	SEG39	O	LCD segment pin	—	—	—	—	—	—
79	SEG40	O	LCD segment pin	—	—	—	—	—	—
80	SEG41	O	LCD segment pin	—	—	—	—	—	—

PAD NO.	Primary function			Secondary function			Tertiary function		
421	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
81	SEG42	O	LCD segment pin	—	—	—	—	—	—
82	SEG43	O	LCD segment pin	—	—	—	—	—	—
83	SEG44	O	LCD segment pin	—	—	—	—	—	—
84	SEG45	O	LCD segment pin	—	—	—	—	—	—
85	SEG46	O	LCD segment pin	—	—	—	—	—	—
86	SEG47	O	LCD segment pin	—	—	—	—	—	—
87	SEG48	O	LCD segment pin	—	—	—	—	—	—
88	SEG49	O	LCD segment pin	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
XT1	O		—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock. A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V_{SS}. This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
OSC1	O		Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0-2	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
Successive approximation type A/D converter				
AV_{SS}	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV_{DD}	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V_{REF}	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
LCD drive signal				
COM0-7	O	Common output pins.	—	—
COM8-15	O	Common output pins. These pins are for the ML610422, but are not provided in the ML610421.	—	—
SEG0-49	O	Segment output pin.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, Cc, and Cd (see measuring circuit 1) are connected between V_{SS} and V_{L1}, V_{L2}, V_{L3}, and V_{L4}, respectively.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
V_{L4}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 and C34 (see measuring circuit 1) are connected between C1 and C2 and between C3 and C4, respectively.	—	—
C2	—		—	—
C3	—		—	—
C4	—		—	—
For testing				
TEST	I	Input pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{DDX}	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor Cx (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
AV_{DD}	V_{SS}
AV_{SS}	V_{SS}
V_{REF}	V_{SS}
AIN0, AIN1	Open
V_{L1}, V_{L2}, V_{L3}, V_{L4}	Open
C1, C2, C3, C4	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V_{DD} or V_{SS}
P10 to P11	V_{DD}
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7	Open
COM0 to 15	Open
SEG0 to 49	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	AV_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 4	V_{DDX}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 5	V_{L1}	Ta = 25°C	–0.3 to +1.75	V
Power supply voltage 6	V_{L2}	Ta = 25°C	–0.3 to +3.5	V
Power supply voltage 7	V_{L3}	Ta = 25°C	–0.3 to +5.25	V
Power supply voltage 8	V_{L4}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–A, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.25	W
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	ML610421	–20 to +70	°C
Operating voltage	V_{DD}	—	1.1 to 3.6	V
	AV_{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V_{DD} = 1.3 to 3.6V	30k to 650k	
		V_{DD} = 1.8 to 3.6V	30k to 4.2M	
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	1.0±30%	µF
	C_{L1}	—	0.1±30%	
Capacitor externally connected to V_{DDX} pin	C_X	—	0.1±30%	µF
Capacitors externally connected to $V_{L1, 2, 3, 4}$ pins	$C_{a, b, c, d}$	—	1.0±30%	µF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C_{12}, C_{34}	—	1.0±30%	µF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor [*1]	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation [*2]	—	0	—	pF
		C_L=9pF of crystal oscillation	—	6	—	
		C_L=12pF of crystal oscillation	—	12	—	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	—	4.0M / 4.096M	—	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	—	24	—	pF
	C_{GH}	—	—	24	—	

[*1]: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.

[*2]: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

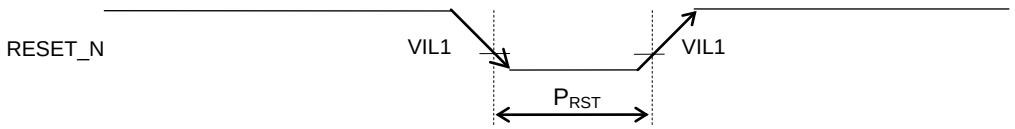
DC CHARACTERISTICS (1/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified) (1/5)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
500kHz RC oscillation frequency	f_{RC}	V_{DD} = 1.3 to 3.6V	Ta = 25°C	Typ. −10%	500	Typ. +10%	kHz	1
			Ta = −20 to +70°C	Typ. −25%	500	Typ. +25%	kHz	
PLL oscillation frequency*4	f_{PLL}	LSCLK = 32.768kHz V_{DD} = 1.8 to 3.6V		-2.5%	8.192	+2.5%	MHz	
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.3	2	s	
500kHz RC oscillation start time	T_{RC}	—		—	50	500	μs	
High-speed crystal oscillation start time*3	T_{XTH}	V_{DD} = 1.8 to 3.6V		—	2	20	ms	
PLL oscillation start time	T_{PLL}	V_{DD} = 1.8 to 3.6V		—	1	10		
Low-speed oscillation stop detect time*1	T_{STOP}	—		0.2	3	20		
Reset pulse width	P_{RST}	—		200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

*1 : When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.
*2 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*3 : Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).
*4 : 1024 clock average.

[Reset pulse width]



Reset pulse width (P_{RST})

[Power-on reset activation power rise time]

Power-on reset activation power rise time (T_{POR})

DC CHARACTERISTICS (2/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (2/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L1} voltage	V_{L1}	V_{DD} = 3.0V, Tj = 25°C	CN4–0 = 00H	0.89	0.94	0.99	V	1
			CN4–0 = 01H	0.91	0.96	1.01		
			CN4–0 = 02H	0.93	0.98	1.03		
			CN4–0 = 03H	0.95	1.00	1.05		
			CN4–0 = 04H	0.97	1.02	1.07		
			CN4–0 = 05H	0.99	1.04	1.09		
			CN4–0 = 06H	1.01	1.06	1.11		
			CN4–0 = 07H	1.03	1.08	1.13		
			CN4–0 = 08H	1.05	1.10	1.15		
			CN4–0 = 09H	1.07	1.12	1.17		
			CN4–0 = 0AH	1.09	1.14	1.19		
			CN4–0 = 0BH	1.11	1.16	1.21		
			CN4–0 = 0CH	1.13	1.18	1.23		
			CN4–0 = 0DH	1.15	1.20	1.25		
			CN4–0 = 0EH	1.17	1.22	1.27		
			CN4–0 = 0FH	1.19	1.24	1.29		
			CN4–0 = 10H	1.21	1.26	1.31		
			CN4–0 = 11H	1.23	1.28	1.33		
			CN4–0 = 12H	1.25	1.30	1.35		
			CN4–0 = 13H	1.27	1.32	1.37		
			CN4–0 = 14H *1	1.29	1.34	1.39		
			CN4–0 = 15H *1	1.31	1.36	1.41		
			CN4–0 = 16H *1	1.33	1.38	1.43		
			CN4–0 = 17H *1	1.35	1.40	1.45		
			CN4–0 = 18H *1	1.37	1.42	1.47		
			CN4–0 = 19H *1	1.39	1.44	1.49		
			CN4–0 = 1AH *1	1.41	1.46	1.51		
			CN4–0 = 1BH *1	1.43	1.48	1.53		
			CN4–0 = 1CH *1	1.45	1.50	1.55		
			CN4–0 = 1DH *1	1.47	1.52	1.57		
			CN4–0 = 1EH *1	1.49	1.54	1.59		
			CN4–0 = 1FH *1	1.51	1.56	1.61		
V_{L1} temperature deviation	ΔV_{L1}	V_{DD} = 3.0V		—	–1.5	—	mV/°C	
V_{L1} voltage dependency	ΔV_{L1}	V_{DD} = 1.3 to 3.6V		—	5	20	mV/V	
V_{L2} voltage*2	V_{L2}	V_{DD} = 3.0V, Tj = 25°C, 500kΩ load (V_{L4}–V_{SS})		Typ. –10%	V_{L1}×2	Typ. +4%	V	
V_{L3} voltage*2	V_{L3}	V_{DD} = 3.0V, Tj = 25°C, 500kΩ load (V_{L4}–V_{SS})	1/3 bias	Typ. –10%	V_{L1}×2	Typ. +4%		
			1/4 bias		V_{L1}×3			
V_{L4} voltage*2	V_{L4}		1/3 bias	Typ. –10%	V_{L1}×3	Typ. +5%		
			1/4 bias		V_{L1}×4			
LCD bias voltage generation time	T_{BIAS}	—		—	—	600	ms	

*1: When using 1/4 bias, the V_{L1} voltage is set to typ. 1.32 V (same voltage as in CN4–0 = 13H).
*2: Boost clock is 2kHz(initial) for the bias generation. C12=C34=1uF.

DC CHARACTERISTICS (3/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	V_{DD} = 1.35 to 3.6V	LD2–0 = 0H	Typ. –2%	1.35	Typ. +2%	V	
			LD2–0 = 1H		1.4			
			LD2–0 = 2H		1.45			
			LD2–0 = 3H		1.5			
			LD2–0 = 4H		1.6			
			LD2–0 = 5H		1.7			
			LD2–0 = 6H		1.8			
			LD2–0 = 7H		1.9			
			LD2–0 = 8H		2.0			
			LD2–0 = 9H		2.1			
			LD2–0 = 0AH		2.2			
			LD2–0 = 0BH		2.3			
			LD2–0 = 0CH		2.4			
			LD2–0 = 0DH		2.5			
			LD2–0 = 0EH		2.7			
			LD2–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	V_{DD} = 1.35 to 3.6V		—	0	—	%/°C	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.15	0.50	μA	1
			Ta = -20 to +70°C	—	—	2.50		
Supply current 2	IDD2	CPU: In HALT state (LTBC, WDT: Operating*3*5). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	Ta = 25°C	—	0.5	1.3	μA	
			Ta = -20 to +70°C	—	—	3.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed oscillation: Stopped. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	5	7	μA	
			Ta = -20 to +70°C	—	—	12		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	70	85	μA	
			Ta = -20 to +70°C	—	—	100		
Supply current 5	IDD5	CPU: In 4.096MHz operating state.*2*3 PLL: In oscillating state. LCD/BIAS circuits: Operating. *2 V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.8	1.0	mA	
			Ta = -20 to +70°C	—	—	1.2		
Supply current 6	IDD6	CPU: In 4.096MHz operating state.*2 PLL: In oscillating state. *3*4 A/D: In operating state. LCD/BIAS circuits: Operating. *2 V_{DD} = AV_{DD} = 3.0V	Ta = 25°C	—	1.5	1.6	mA	
			Ta = -20 to +70°C	—	—	2.5		

*1 : When the CPU operating rate is 100% (No HALT state).
*2 : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*4 : Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).
*5 : Significant bits of BLKCON0~BLKCON4 registers are all “1”.

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C,unless otherwise specified) (4/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P22/2nd function is selected) (P30–P35) (P40–P47) (PA0–PA7)*1	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V	V_{DD} –0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V	V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V	V_{DD} –0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.3 to 3.6V	—	—	0.5		
		IOL1 = +0.03mA, V_{DD} = 1.1 to 3.6V	—	—	0.3		
Output voltage 2 (P20–P22/2nd function is Not selected)	VOH2	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V	V_{DD} –0.5	—	—		
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V	V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V	V_{DD} –0.3	—	—		
	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)	—	—	0.4		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA7)*1	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	–1	—	—		

*1: ML610421 only

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (4/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	V_{DD} = 1.8 to 3.6V	–600	–300	–20		
			V_{DD} = 1.3 to 3.6V	–600	–300	-10		
			V_{DD} = 1.1 to 3.6V	–600	–300	-2		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD}	V_{DD} = 1.8 to 3.6V	20	300	600		
			V_{DD} = 1.3 to 3.6V	10	300	600		
			V_{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V_{ss}		-1	—	—		
Input current 2 (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7)*1	IIH2	VIH2 = V_{DD} (when pulled-down)	V_{DD} = 1.8 to 3.6V	2	30	200		
			V_{DD} = 1.3 to 3.6V	0.2	30	200		
			V_{DD} = 1.1 to 3.6V	0.01	30	200		
	IIL2	VIL2 = V_{SS} (when pulled-up)	V_{DD} = 1.8 to 3.6V	–200	–30	–2		
			V_{DD} = 1.3 to 3.6V	–200	–30	-0.2		
			V_{DD} = 1.1 to 3.6V	–200	–30	-0.01		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		–1	—	—		

*1: ML610421 only

DC CHARACTERISTICS (5/5)

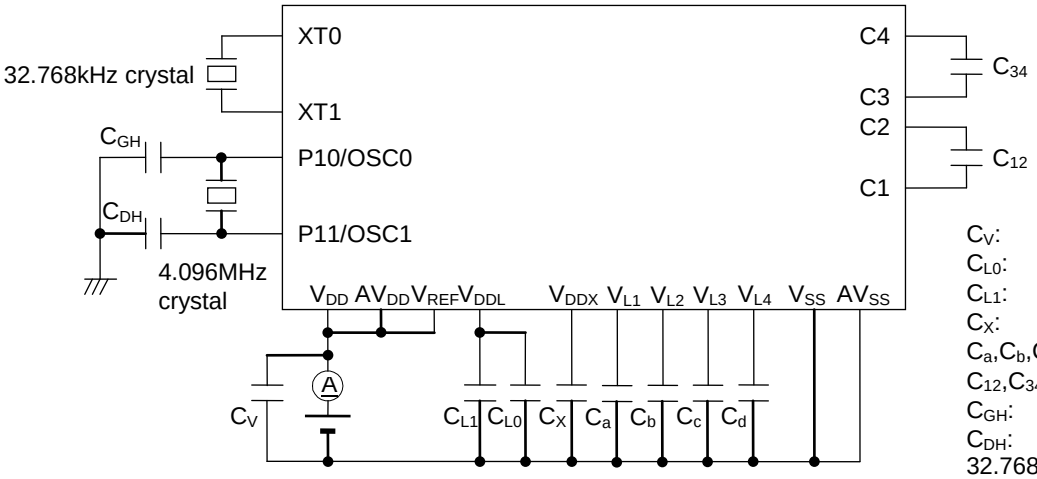
(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, Ta = –40 to +85°C for P version, unless otherwise specified) (5/5)

Parameter	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)*1	VIH1	V_{DD} = 1.3 to 3.6V	0.7 ×V_{DD}	—	V_{DD}	V	5
		V_{DD} = 1.1 to 3.6V	0.7 ×V_{DD}	—	V_{DD}		
	VIL1	V_{DD} = 1.3 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0	—	0.2 ×V_{DD}		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7)*1	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

*1: ML610421 only

MEASURING CIRCUITS

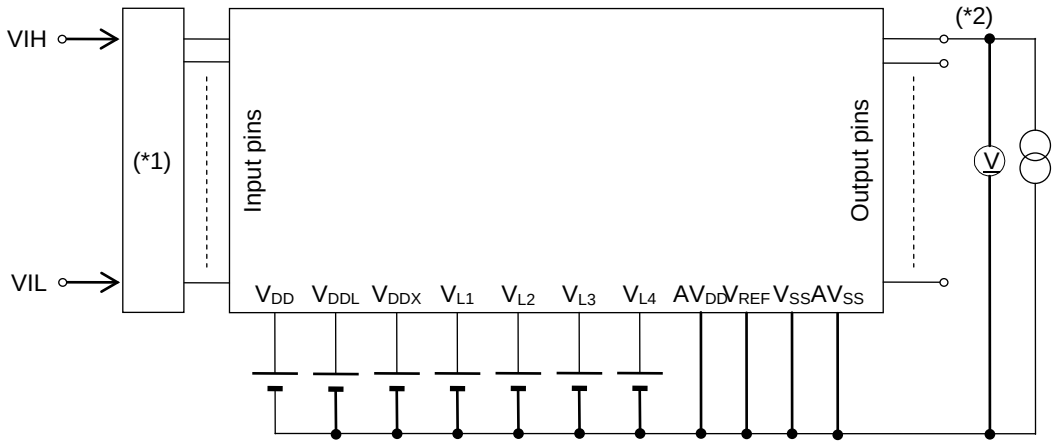
MEASURING CIRCUIT 1



C_V:	1µF
C_{L0}:	1µF
C_{L1}:	0.1µF
C_X:	0.1µF
C_a,C_b,C_c,C_d:	1µF
C_{12},C_{34}:	1µF
C_{GH}:	24pF
C_{DH}:	24pF

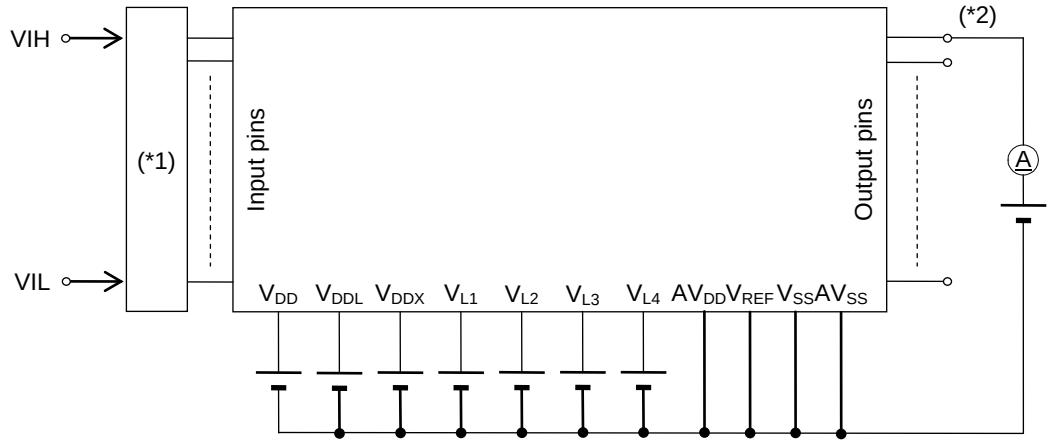
32.768kHz crystal:
C-001R (Epson Toyocom)
4.096MHz crystal:
HC49SFWB (Kyocera)

MEASURING CIRCUIT 2



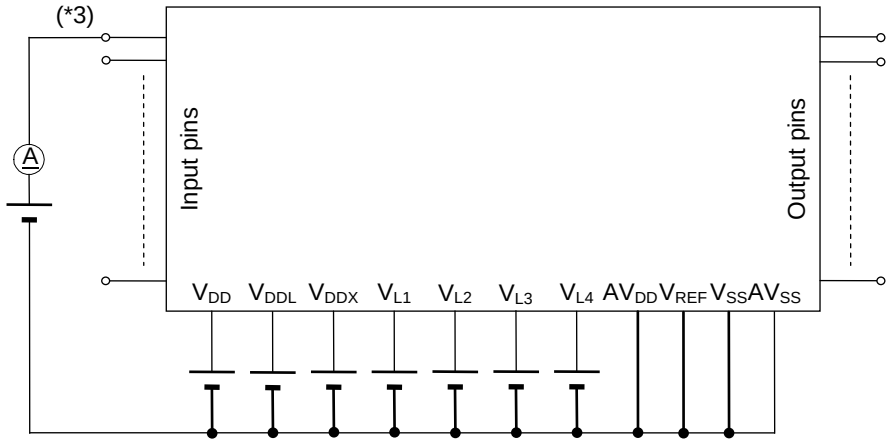
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



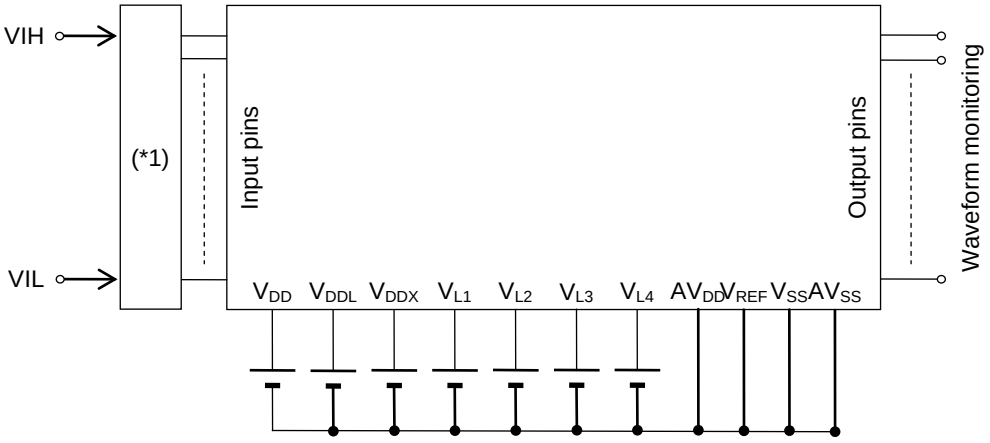
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

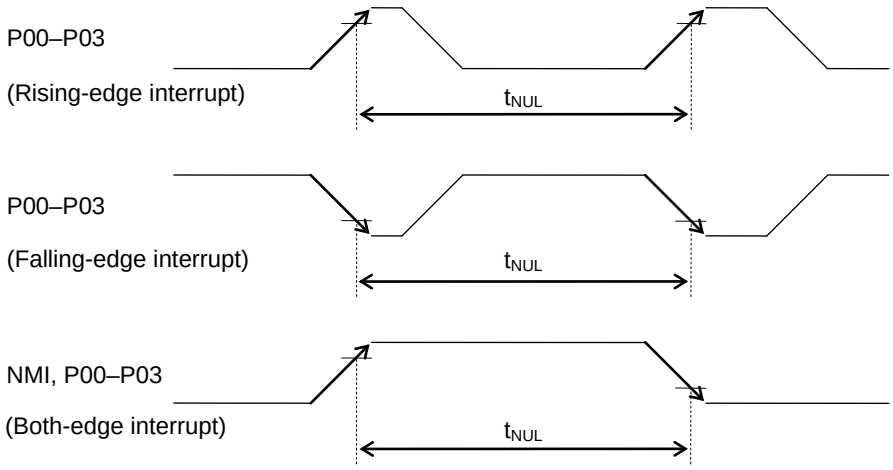


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	µs

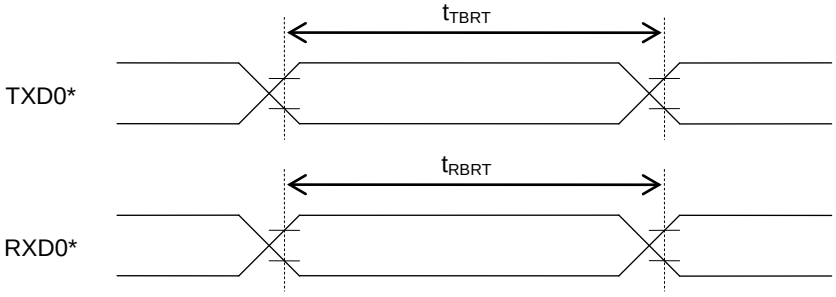


AC CHARACTERISTICS (UART)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] –3%	BRT*[1]	BRT*[1] +3%	s

*[1]: Baud rate period (including the error of the clock frequency selected) set with the UART0 baud rate register (UA0BRTL,H) and the UART0 mode register 0 (UA0MOD0).



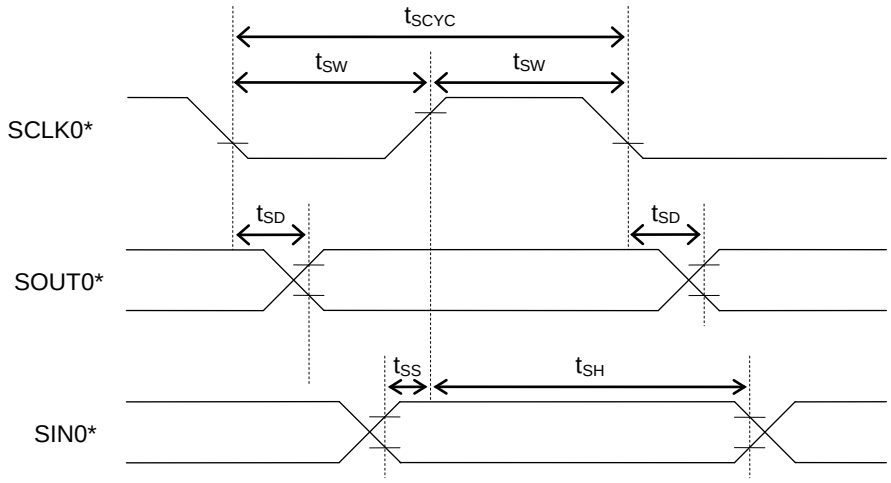
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	10	—	—	µs
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	1	—	—	µs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*1	—	s
SCLK input pulse width (slave mode)	t_{SW}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	4	—	—	µs
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	0.4	—	—	µs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	—	—	240	
SOUT output delay time (master mode)	t_{SD}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	—	—	240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	500	—	—	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	240	—	—	
SIN input hold time	t_{SH}	When RC oscillation is active*2 (V_{DD} = 1.3 to 3.6V)	300	—	—	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	80	—	—	

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)
*2: When RC oscillation is selected with OSCM1–0 of the frequency control register (FCON0)
*3: When Crystal/ceramic oscillation, built-in PLL oscillation, or external clock input is selected with OSCM1–0 of the frequency control register (FCON0)



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I^2C Bus Interface: Standard Mode 100kHz)

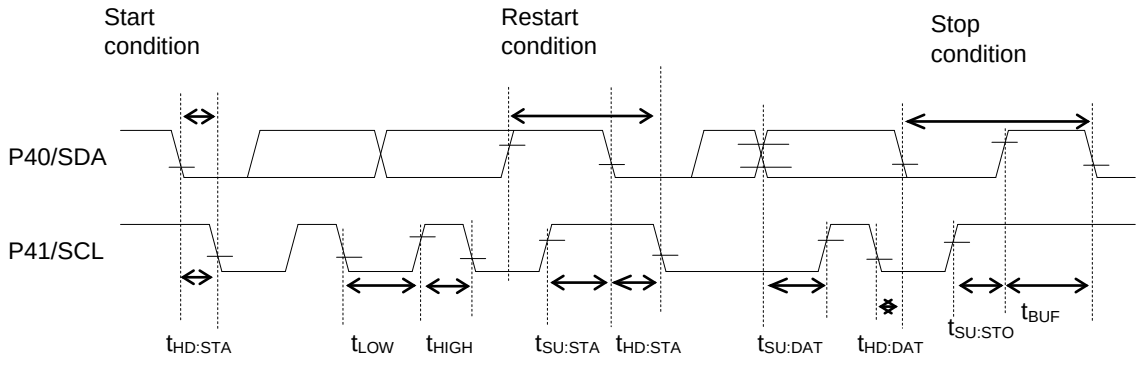
(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC CHARACTERISTICS (I2C Bus Interface: Fast Mode 400kHz)

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



AC CHARACTERISTICS (RC Oscillation A/D Converter)

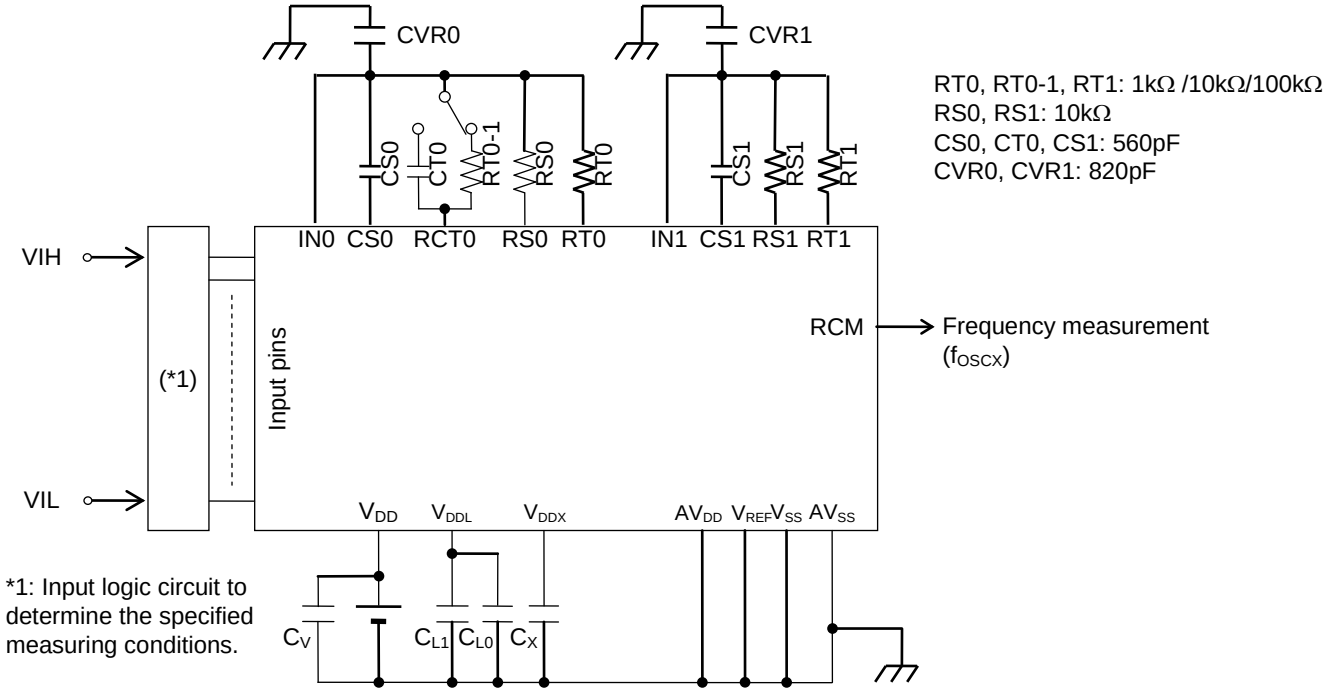
(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resistors for oscillation	RS0, RS1, RT0, RT0-1,RT1	CS0, CT0, CS1 ≥ 740pF	1	—	—	kΩ
Oscillation frequency VDD = 1.5V	f_{OSC1}	Resistor for oscillation = 1kΩ	209.4	330.6	435.1	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	41.29	55.27	64.16	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	4.71	5.97	7.06	kHz
RS to RT oscillation frequency ratio *1 VDD = 1.5V	Kf1	RT0, RT0-1, RT1 = 1kHz	5.567	5.982	6.225	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.104	0.108	0.118	—
Oscillation frequency VDD = 3.0V	f_{OSC1}	Resistor for oscillation = 1kΩ	407.3	486.7	594.6	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	49.76	59.28	72.76	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	5.04	5.993	7.04	kHz
RS to RT oscillation frequency ratio *1 VDD = 3.0V	Kf1	RT0, RT0-1, RT1 = 1kHz	8.006	8.210	8.416	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.100	0.108	0.115	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCX}(RT0–CS0\ oscillation)}{f_{OSCX}(RS0–CS0\ oscillation)}, \frac{f_{OSCX}(RT0\text{-}1–CS0\ oscillation)}{f_{OSCX}(RS0–CS0\ oscillation)}, \frac{f_{OSCX}(RT1–CS1\ oscillation)}{f_{OSCX}(RS1–CS1\ oscillation)}$$

(x = 1, 2, 3)



Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.

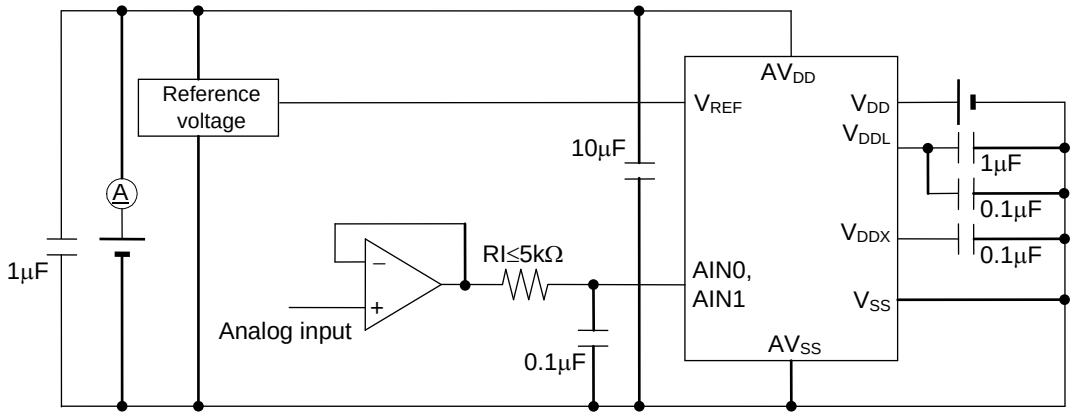
- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 3.6V	–4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	–3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	SACK = 0 (HSCLK = 375kHz to 625kHz)	—	25	—	ϕ/CH
		SACK = 1 (HSCLK = 1.5MHz to 4.2MHz)	—	112	—	

ϕ: Period of high-speed clock (HSCLK)



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610421-01	Apr. 12, 2011	–	–	Final edition 1
FEDL610421-02	Feb. 9, 2015	All	All	Change header
		1 to 4, 6,8,10, 12 to 16, 21, 25 to 26	1 to 4 8 to 11 16 21 to 22	Delete ML610422 Mask ROM Version
		4,7,8,34	4	Delete ML610421 Mask ROM TQFP Package Version
		3,4	3,4	Delete Low-speed clock oscillation stop detection reset un-carrying version (B) version
		1,4 21 to 26, 29 to 33	1,4 16 to 21 25 to 29	Delete Wide range temperature version (P version)
		4	4	Change from "Shipment" to " Product name – Supported Function "
		-	17	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		22	18	Change "RESET" to " Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".
		36	31	Change description in Note.

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