FEDL610Q359-01
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ML610Q359/ML610Q360

8-bit Microcontroller with Voice Output Function

GENERAL DESCRIPTION

Equipped with a 8-bit CPU nX-U8/100, the ML610Q359 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as, 12-bit A/D converter, timer, synchronous serial port, UART, and voice output function. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture.
In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set:Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    Approx 30.5 μs (at 32.768kHz system clock)
    Approx 0.125 μs (at 8MHz system clock)@DV_{DD} = 2.2 to 3.6V
    Approx 0.250 μs (at 4MHz system clock)@DV_{DD} = 2.0 to 3.6V

- Internal memory
  – Has 160-Kbyte flash ROM(80K × 16-bit) built in. (544 byte of test domain that it cannot be used is included)
  – Has 3-Kbyte flash ROM built in. (area in which self rewriting is possible.512Byte×6)
  – Has 2-Kbyte RAM (2048 × 8 bits) built in.
  – Has 16-Mbit P2ROM built in. (only ML610Q360)

- Interrupt controller
  – 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  – 25 maskable interrupt sources (Internal source: 19, External source: 6)

- Time base counter
  – Low-speed time base counter × 1 channel
  – High-speed time base counter × 1 channel

- Watchdog timer
  – Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  – Free running
  – Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  – 8 bits × 8ch (16-bit configuration available)

ROHM SEMICONDUCTOR

- Voice output function
  - Voice synthesis method: 4-bit ADPCM2 / non-linear PCM / straight 8-bit PCM / straight 16-bit PCM
  - Sampling frequency: 8/16/32 kHz; 10.7/21.3 kHz; 6.4/12.8/25.6 kHz

- D/A converter
  - 12-bit D/A converter

- Speaker amplifier output power
  - 0.5W(at 3.0V)
  - Thermal detection circuit
  - Disconnection detection circuit

- Synchronous serial port
  - 2ch
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-duplex × 2ch or half-duplex × 1ch + full-duplex × 1ch
  - TXD / RXD
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Successive approximation type A/D converter
  - 12-bit A/D converter
  - Input: 4ch (ch0-2:External input
    ch3: A regulator output (V_{DDR}) or a temperature sensor output (TEMPO)
  - Conversion time: 20 μs per channel at 8MHz $AV_{DD} \geqq 2.5V$
  - Conversion time: 28 μs per channel at 8MHz $AV_{DD} \geqq 2.2V$

- Temperature sensor
  - Measuring range : –40°C to +85°C

- Regulator output (V_{DDR})
  - 1.5V±50mV(at –40°C to +85°C and when a V_{DDR} pin is no-load)
  - 1.5V / 0V / HiZ selectable

- General-purpose ports
  - Non-maskable interrupt input port × 1ch
  - Input-only port × 7ch
  - Output-only port × 3ch (including secondary functions)
  - Input/output × 29ch (including secondary functions)

- Supply voltage supervisor circuit
  - Judgment accuracy: ±1.5% (Typ.)
  - Judgment Voltage: A binary to selection is possible
  - This function can be used as supply voltage supervisor reset.

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - Reset when oscillation stop of the low-speed clock is detected
  - Voltage level supervisor reset

- Clock
  - Low-speed clock (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock
    Built-in oscillation (8.192MHz), external clock

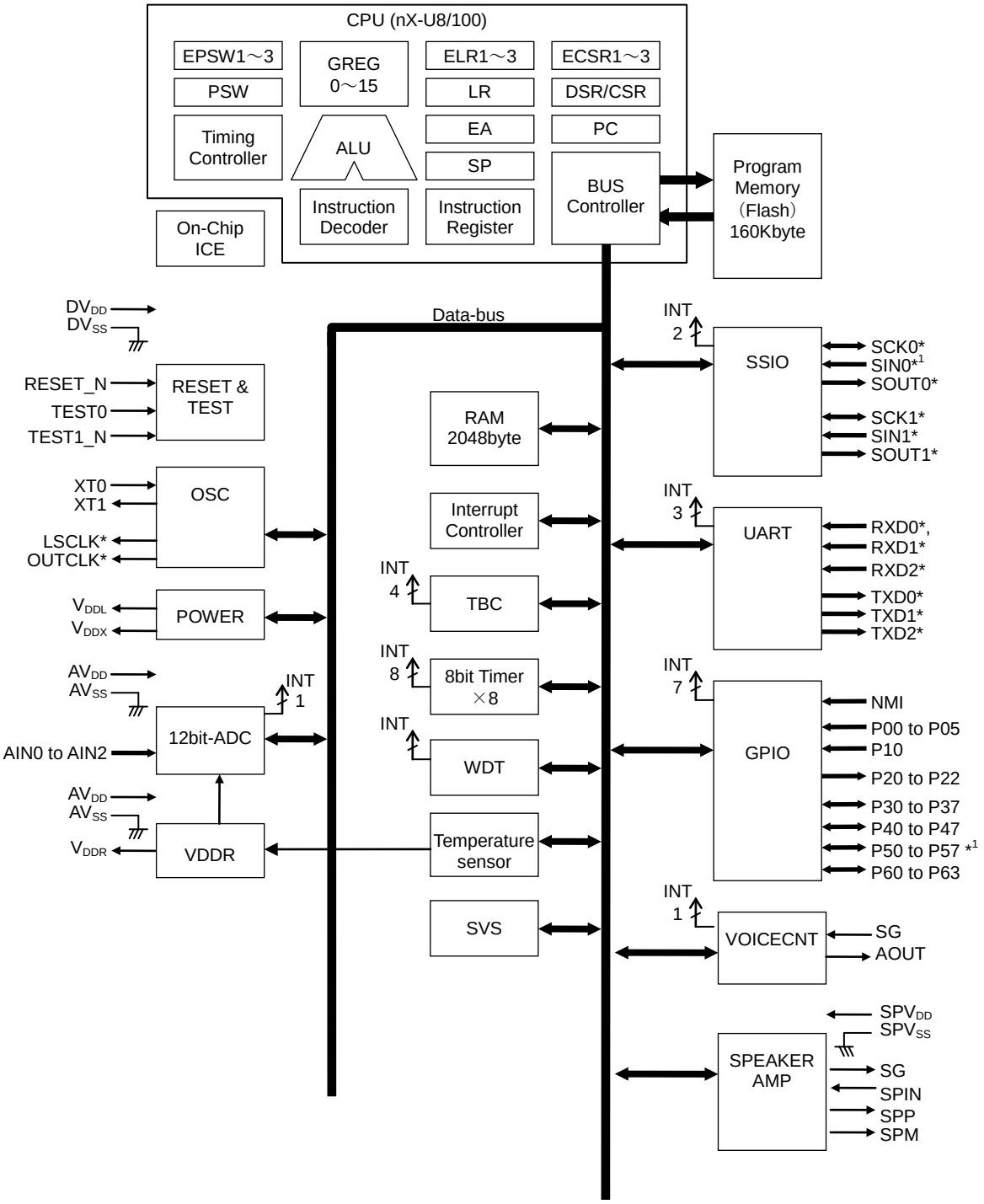
- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

- Shipment
  - 64-pin TQFP
    ML610Q359-xxxTB (blank product: ML610Q359-NNNTB)
    ML610Q360-xxxTB (blank product: ML610Q360-NNNTB)
    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: –40°C to 85°C(for ML610Q359)
    : –10°C to 65°C(P2ROM movment of ML610Q360)
  - Operating voltage: DV_{DD} = 2.0V to 3.6V, SPV_{DD} = 2.2V to 3.6V, AV_{DD} = 2.2V to 3.6V

BLOCK DIAGRAM

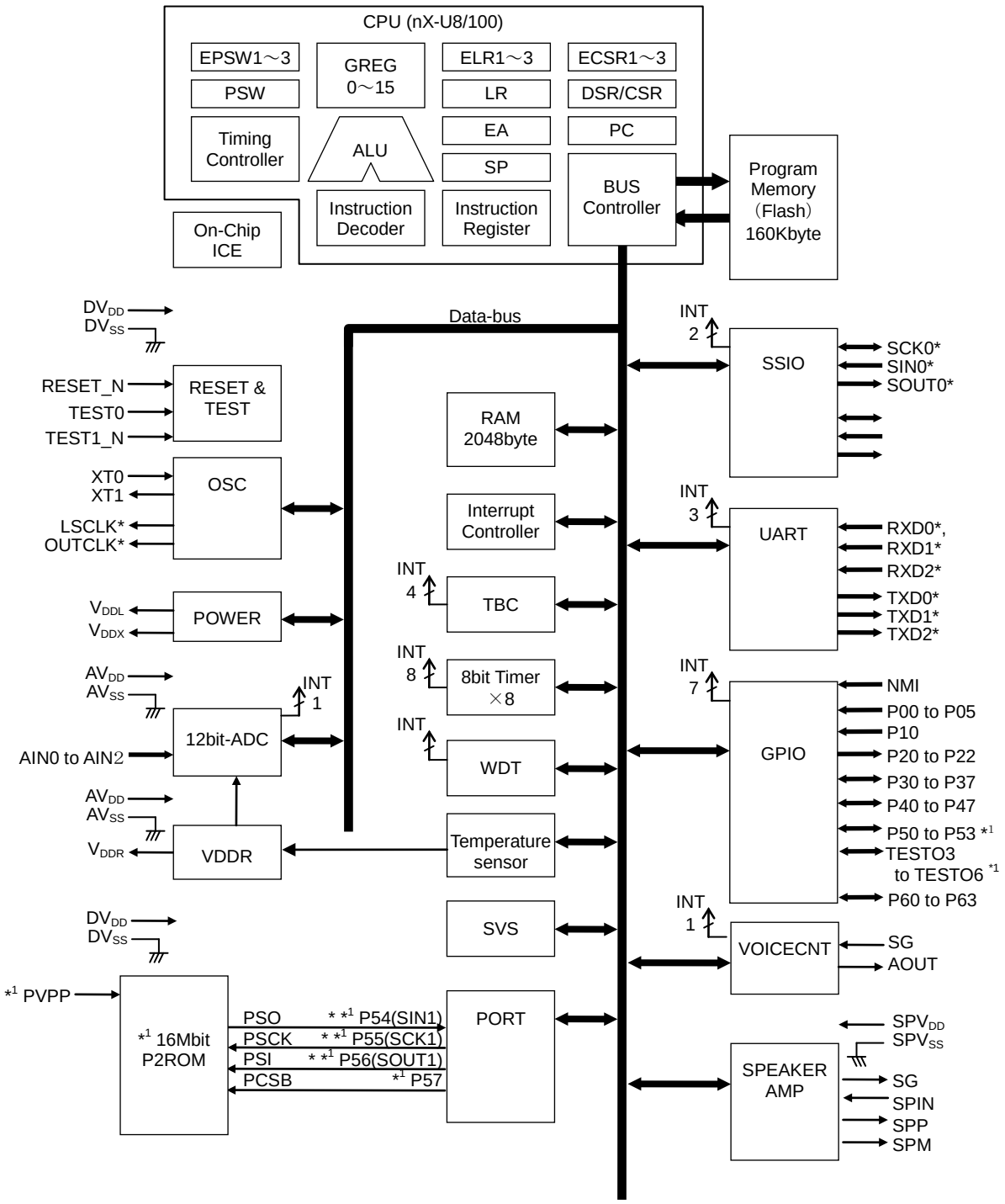
Block Diagram of ML610Q359



* : Secondary or tertiary or fourthly function
*1: It is the point with the difference in ML610Q359 and ML610Q360

Figure 1 Block Diagram of ML610Q359

Block Diagram of ML610Q360

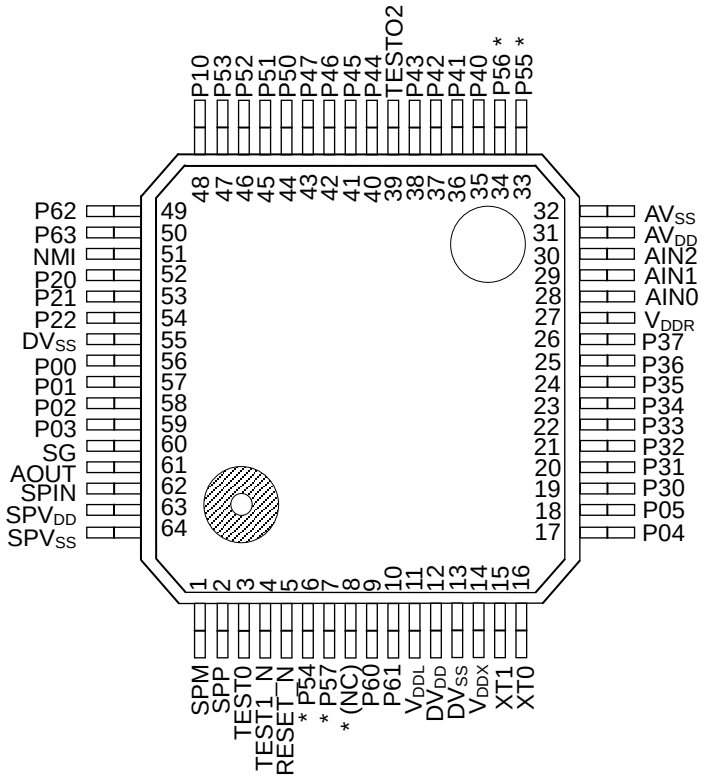


* : Secondary or tertiary or fourthly function
*1: It is the point with the difference in ML610Q359 and ML610Q360

Figure 2 Block Diagram of ML610Q360

PIN CONFIGURATION

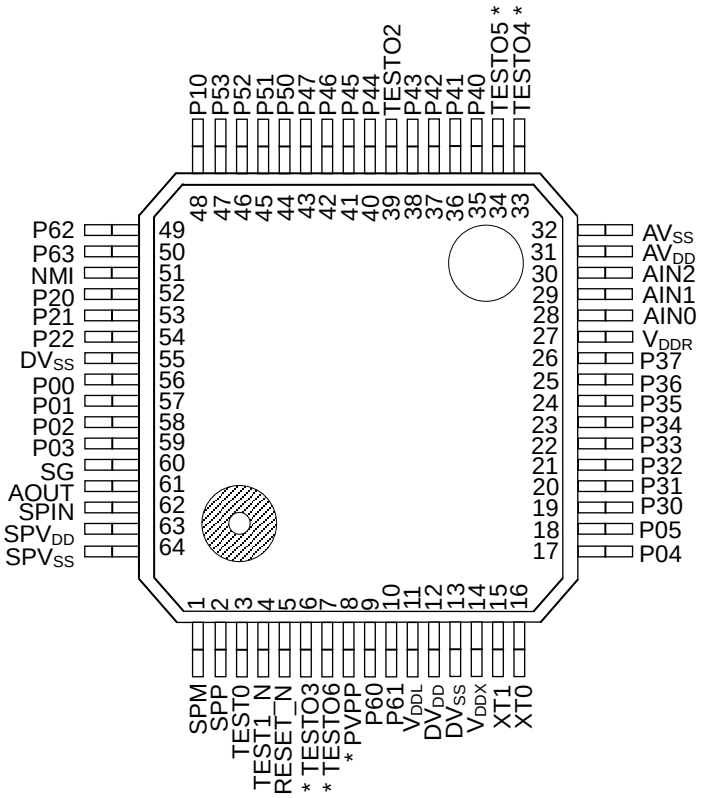
ML610Q359 TQFP package product



*: It is the point with the difference in ML610Q359 and ML610Q360
(NC): No Connection

Figure 3 Pin Configuration of ML610Q359 Package Product

ML610Q360 TQFP package product



*: It is the point with the difference in ML610Q359 and ML610Q360

Figure 4 Pin Configuration of ML610Q360 Package Product

LIST OF PINS

Pin No		Primary function			Secondary function			Tertiary function		
Q359	Q360	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
13,55	13,55	DV_{SS}	—	Negative power supply pin	—	—	—	—	—	—
12	12	DV_{DD}	—	Positive power supply pin	—	—	—	—	—	—
11	11	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—
14	14	V_{DDX}	—	Power supply pin for oscillation (internally generated)						
27	27	V_{DDR}	—	Reference voltage output of 1.5V	—	—	—	—	—	—
64	64	SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—	—	—	—	—
63	63	SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—	—	—	—	—
32	32	AV_{SS}	—	Negative power supply pin for successive-approximation type ADC/OP-amp	—	—	—	—	—	—
31	31	AV_{DD}	—	Positive power supply pin for successive-approximation type ADC/OP-amp	—	—	—	—	—	—
—	8	PVPP	—	High voltage power supply pin of data to building P2ROM	—	—	—	—	—	—
3	3	TEST0	I/O	Input/output pin for testing	—	—	—	—	—	—
4	4	TEST1_N	I	Input pin for testing	—	—	—	—	—	—
39	39	TESTO2	—	Output pin for testing	—	—	—	—	—	—
5	5	RESET_N	I	Reset input pin	—	—	—	—	—	—
16	16	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
15	15	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
61	61	AOUT	O	LINE output	—	—	—	—	—	—
62	62	SPIN	I	Analog input to the built-in speaker amplifier	—	—	—	—	—	—
60	60	SG	O	Reference power supply pin of the built-in speaker amplifier	—	—	—	—	—	—
2	2	SPP	O	Positive output pin of the built-in speaker amplifier	—	—	—	—	—	—
1	1	SPM	O	Negative output pin of the built-in speaker amplifier	—	—	—	—	—	—
28	28	AIN0	I	Successive-approximation type ADC input	—	—	—	—	—	—
29	29	AIN1	I	Successive-approximation type ADC input	—	—	—	—	—	—
30	30	AIN2	I	Successive-approximation type ADC input	—	—	—	—	—	—

Pin No		Primary function			Secondary function			Tertiary function			Fourthly function		
Q359	Q360	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
51	51	NMI	I	Input port, non-maskable interrupt	—	—	—	—	—	—	—	—	—
56	56	P00/EXI0	I	Input port / External	—	—	—	—	—	—	—	—	—
57	57	P01/EXI1	I	Input port / External	—	—	—	—	—	—	—	—	—
58	58	P02/EXI2 / RXD0 / RXD2	I	Input port / External interrupt / UART0 data input / UART2 data input	—	—	—	—	—	—	—	—	—
59	59	P03/EXI3 / RXD1	I	Input port / External interrupt / UART1 data input	—	—	—	—	—	—	—	—	—
17	17	P04/EXI4/ T02P0CK	I	Input port / External interrupt / Timer0,2 external clock input	—	—	—	—	—	—	—	—	—
18	18	P05/EXI5/ T13P0CK	I	Input port / External interrupt / Timer1,3 external clock input	—	—	—	—	—	—	—	—	—
48	48	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—	—	—	—
52	52	P20/ LED0	O	Output port / LED drive	LSCLK	O	Low-speed clock output	—	—	—	—	—	—
53	53	P21/ LED1	O	Output port / LED drive	OUTCLK	O	high-speed clock output	—	—	—	—	—	—
54	54	P22/ LED2	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
19	19	P30	I/O	Input/output port	—	—	—	—	—	—	—	—	—
20	20	P31	I/O	Input/output port	—	—	—	—	—	—	—	—	—
21	21	P32	I/O	Input/output port	—	—	—	—	—	—	—	—	—
22	22	P33	I/O	Input/output port	—	—	—	—	—	—	—	—	—
23	23	P34	I/O	Input/output port	—	—	—	—	—	—	—	—	—
24	24	P35	I/O	Input/output port	—	—	—	—	—	—	—	—	—
25	25	P36	I/O	Input/output port	—	—	—	—	—	—	—	—	—

Pin No		Primary function			Secondary function			Tertiary function			Fourthly function		
Q359	Q360	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
35	35	P40	I/O	Input/output port	—	—	—	SIN0	I	SSIO0 data input	—	—	—
36	36	P41	I/O	Input/output port	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
37	37	P42	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	RXD2	I	UART2 data input
38	38	P43	I/O	Input/output port	TXD0	O	UART0 data output	—	—	—	TXD2	O	UART2 data output
40	40	P44	I/O	Input/output port	—	—	—	SIN0	I	SSIO0 data input	—	—	—
41	41	P45	I/O	Input/output port	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
42	42	P46	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
43	43	P47	I/O	Input/output port	—	—	—	—	—	—	—	—	—
44	44	P50	I/O	Input/output port	—	—	—	SIN1	I	SSIO1 data input	—	—	—
45	45	P51	I/O	Input/output port	—	—	—	SCK1	I/O	SSIO1 synchronous clock input/output	—	—	—
46	46	P52	I/O	Input/output port	RXD1	I	UART1 data input	SOUT1	O	SSIO1 data output	—	—	—
47	47	P53	I/O	Input/output port	TXD1	O	UART1 data output	—	—	—	TXD2	O	UART2 data output
6	—	P54/ TESTO3	I/O	Input/output port	—	—	—	SIN1	I	SSIO1 data input	—	—	—
33	—	P55/ TESTO4	I/O	Input/output port	—	—	—	SCK1	I/O	SSIO1 synchronous clock input/output	—	—	—
34	—	P56/ TESTO5	I/O	Input/output port	—	—	—	SOUT1	O	SSIO1 data output	—	—	—
7	—	P57/ TESTO6	I/O	Input/output port	—	—	—	—	—	—	—	—	—
9	9	P60	I/O	Input/output port	—	—	—	—	—	—	—	—	—
10	10	P61	I/O	Input/output port	—	—	—	—	—	—	—	—	—
49	49	P62	I/O	Input/output port	—	—	—	—	—	—	—	—	—
50	50	P63	I/O	Input/output port	—	—	—	—	—	—	—	—	—

Note:
The function which has not been chosen is lost when it is chosen any of a secondary function, the Tertiary function, and the fourthly function they are. However, when using it as an input, it is possible to read input data with a port-n data register.

Complement: It is only ML610Q360. ML610Q359 does not correspond.
P54-P57 are connected with built-in P2ROM inside the chip, and each function exists. An external terminator name is set to TESTO3-TESTO6. Please make the external terminator open. The content of contact with P2ROM is shown below.

The terminator of built-in P2ROM	Explanation
PSO	serial data output It connects with P54/SIN1(tertiary functional use) inside.
PSCK	serial clock input It connects with P55/SCK1(tertiary functional use) inside.
PSI	serial data input It connects with P56/SOUT1(tertiary functional use) inside.
PCSB	chip select input It connects with P57(primary functional use) inside.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary	Logic
Power supply				
DV_{SS}	—	Negative power supply pin	—	—
DV_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated) Connect capacitors (C_L) (see Measuring Circuit 1) between this pin and DV_{SS} .	—	—
V_{DDX}	—	Power supply pin for oscillation (internally generated). Capacitors C_X(see measuring circuit 1) are connected between this pin and DV_{SS}.	—	—
V_{DDR}	—	Reference voltage output. Capacitors C_R(see measuring circuit 1) are connected between this pin and DV_{SS}.	—	—
SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—
SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—
AV_{SS}	—	Negative power supply pin for successive-approximation type ADC/op-amp	—	—
AV_{DD}	—	Positive power supply pin for successive-approximation type ADC/op-amp	—	—
PVPP		High voltage power supply pin of the data write to building P2ROM into. Besides, fix at the V_{SS} level.	—	—
Test				
TEST0	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
TEST1_N	I	Input pin for testing. Has a pull-up resistor built in.	—	Negative
TESTO2	—	Output pin for testing	—	—
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a “H” level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
XT0	I		—	Positive
XT1	O		—	Negative
OSC0	I		Secondary	Positive
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P05	I	General-purpose input ports.	Primary	Positive
P10	I	General-purpose input/output ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Fourthly	Logic
General-output input port				
P20 to P22	O	General-purpose output ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30 to P37 P40 to P47 P50 to P57 P60 to P63	I/O	General-purpose input/output ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART0 data input pin. Allocated to the primary function of the P02 pin and the secondary function of the P42 pin.	Secondary	Positive
TXD1	O	UART1 data output pin. Allocated to the secondary function of the P53 pin.	Secondary	Positive
RXD1	I	UART1 data input pin. Allocated to the primary function of the P03 pin and the secondary function of the P52 pin.	Secondary	Positive
TXD2	O	UART0 data output pin. Allocated to the fourthly function of the P43 pin and the fourthly function of the P53 pin.	Fourthly	Positive
RXD2	I	UART0 data input pin. Allocated to the primary function of the P02 pin and the fourthly function of the P42 pin.	Fourthly	Positive
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin and the tertiary function of the P44 pin.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 pin and the tertiary function of the P45 pin.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 pin and the tertiary function of the P46 pin.	Tertiary	Positive
SIN1	I	Synchronous serial data input pin. Allocated to the tertiary function of the P50 pin and the tertiary function of the P54 pin .	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P51 pin and the tertiary function of the P55 pin.	Tertiary	—
SOUT1	O	Synchronous serial data output pin. Allocated to the tertiary function of the P52 pin and the tertiary function of the P56 pin.	Tertiary	Positive
External interrupt				
NMI	I	External non-maskable interrupt input pin. The interrupt occurs on both the rising and falling edges.	Primary	Positive/ Negative
EXI0–EXI5	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P00–P05 pins.	Primary	Positive/ Negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Fourthly	Logic
LED drive				
LED0–LED2	O	Pins for LED driving. Allocated to the primary function of the P20 to P22 pins.	Primary	Positive/ Negative
Voice output function				
AOUT	O	LINE output pin. The case of built-in speaker amplifier use, connect capacitors (C_{AOSP}) between this pin and the SPIN pin.	—	—
SPIN	I	Analog input pin of the internal speaker amplifier.	—	—
SG	O	Reference voltage output pin of the internal speaker amplifier.	—	—
SPP	O	Positive output pin of the internal speaker amplifier.	—	—
SPM	O	Negative output pin of the internal speaker amplifier.	—	—
Successive-approximation type A/D converter				
AIN0–AIN2	I	Analog inputs to Ch0–Ch2 of the successive-approximation type A/D converter.	—	—

TERMINATION OF UNUSED PINS

How to Terminate Unused Pins

Pin	Recommended pin termination
RESET_N	Open
TEST0	Open
TEST1_N	Open
TESTO2	Open
AVDD	Connect to DVDD
AVSS	Connect to DVSS
AIN0 to AIN2	Open
SPVDD	Connect to DVDD
SPVSS	Connect to DVSS
PVPP	Open
AOUT	Open
SPIN	Open
SG	Open
SPP	Open
SPM	Open
P00 to P05	Connect to DVDD or DVSS
P10	Connect to DVDD or DVSS
P20 to P22	Open
P30 to P37	Open
P40 to P47	Open
P50 to P57	Open
TESTO3 to TESTO6	Open
P60 to P63	Open
VDDR	Open

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(DV_{SS} = AV_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	DV_{DD}	Ta=25°C	–0.3 to +7.0	V
Power supply voltage 2	AV_{DD}	Ta=25°C	–0.3 to +7.0	V
Power supply voltage 3	SPV_{DD}	Ta=25°C	–0.3 to +7.0	V
Power supply voltage 4	V_{DDL}	Ta=25°C	–0.3 to +3.6	V
Power supply voltage 5	V_{DDX}	Ta=25°C	–0.3 to +3.6	V
Power supply voltage 6	V_{DDR}	Ta=25°C	–0.3 to +3.6	V
Power supply voltage 7	TESTO2	Ta=25°C	–0.3 to +9.5	V
Input voltage	V_{IN}	Ta=25°C	–0.3 to DV_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	–0.3 to DV_{DD}+0.3	V
Output current 1	I_{OUT1}	Port 3, 4, 5, 6 Ta=25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port 2, Ta=25°C	–12 to +60	mA
Power dissipation	PD	ML610Q359 Ta=25°C	472	mW
		ML610Q360	562	mW
Storage temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions

(DV_{SS} = AV_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–40 to +85	°C
Operating voltage	DV_{DD}	—	2.0 to 3.6	V
	SPV_{DD}	—	2.2 to 3.6	
	AV_{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f_{OP}	DV_{DD} =2.2V to 3.6V	3.8k to 8.4M	Hz
		DV_{DD} =2.0V to 3.6V	3.8k to 4.2M	
Low speed clock oscillation frequency	f_{XTL}	—	32.768k	Hz
Low speed clock oscillation Capacitor externally connected to Low speed clock oscillation pin	C_{DL}	MC-146 (EPSON TOYOCOM)	14	pF
	C_{GL}		14	
Capacitor externally connected to V_{DDL} pin	C_L	—	10±30%	µF
Capacitor externally connected to V_{DDX} pin	C_X	—	0.1±30%	µF
Capacitor externally connected to V_{DDR} pin	C_R	—	1±30%	µF
Capacitor externally connected to AOUT pin – SPIN pin	C_{AOSP}	—	0.022±30%	µF
Capacitor externally connected to SG pin	C_{SG}	—	0.1±30%	µF

Flash Memory Operating Conditions

(DV_{SS} = AV_{SS} = SPV_{SS} = 0V)

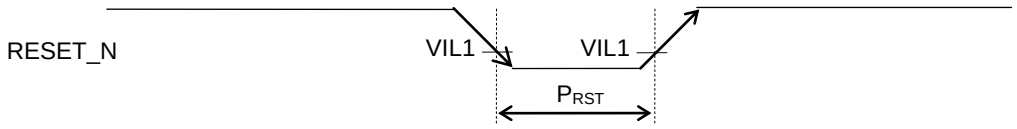
Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	-20 to +75	°C
Operating voltage	DV_{DD}	At write/erase	2.2 to 3.6	V
Maximum rewrite count	C_{EPD}	Data area(1024B)	6000	times
	C_{EPP}	Program area	100	
Data retention period	Y_{DR}	—	10	years

DC Characteristics (1 of 5)

(DV_{DD}= AV_{DD}=SPV_{DD}= 2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
High-speed oscillation start time	T_{XTH}	—	—	1	3	ms	1
Low-speed crystal oscillation start time	T_{XTL}	—	—	—	2	s	
High-speed oscillator frequency	f_{HPLL}	LSCLK=32.768kHz	typ -2.5%	8.192M	typ +2.5%	Hz	
Reset pulse width	P_{RST}	—	100	—	—	μs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.3		
Time from power-on reset to power-up	T_{POR}	—	—	—	10	ms	

Reset



Reset by RESET_N pin

Power-on reset

DC Characteristics (2 of 5)

(DV_{DD}=AV_{DD}=SPV_{DD}= 2.3 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
LINE amplifier output voltage range	V_{AD}	At 10kΩ load for DV_{SS}	SPV_{DD}×1/6	—	SPV_{DD}×5/6	V	1
SG output voltage	V_{SG}	—	0.95 × SPV_{DD}/2	SPV_{DD}/2	1.05 × SPV_{DD}/2	V	
SG output resistance	R_{SG}	—	57	96	135	kΩ	
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω	
Speaker amplifier output power	P_{SPO1}	SPV_{DD} = 3.0V, f = 1kHz, RSPO = 8Ω, THD ≥ 17% At SPIN Input	—	0.5	—	W	
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPV_{DD}=3.0V, SPIN – SPM, Gain = +6dB With a load of 8Ω	−30	—	+30	mV	

DC Characteristics (3 of 5)

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped	Ta ≦ +50°C	—	0.5	2.5	μA	1
			Ta ≦ +85°C	—	0.5	8		
Supply current 2	IDD2	CPU: In HALT state (LTBC, WDT: Operating*2) High-speed oscillation:Stopped	Ta ≦ +50°C	—	1.7	3.5		
			Ta ≦ +85°C	—	1.7	10		
Supply current 3	IDD3	CPU: Running at 32.768 kHz*1 High-speed oscillation: Stopped		—	16	25		
Supply current 4	IDD4	CPU: Running at 8.192MHz High-speed oscillation:Stopped	DV_{DD} = SPV_{DD} = 3.0V	—	4.5	10	mA	

*1: Case when the CPU operating rate is 100% (with no HALT state)
*2 : Significant bits of BLKCON0 to BLKCON4 registers are all “1”.

Supply-voltage supervisor circuit

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
VLS judging voltage	V_{SVS1}	Ta = 25°C	DV_{DD} falling	Typ. -1.5%	2.05	Typ. +1.5%	V	1
			DV_{DD} rising		2.13			
	V_{SVS2}	Ta = 25°C	DV_{DD} falling	Typ. -1.5%	2.25	Typ. +1.5%		
			DV_{DD} rising		2.33			
VLS self-consumption current	I_{SVS}	—		—	10	—	μA	

Temperature sensor

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
TEMPO output voltage	V_{TEMPO}	Ta = 25°C	0.95	1.3	1.6	V	1
TEMPO temperature inclination	Δ_{TEMPO}	Ta=-40℃ to +25℃	—	-3.9	—	mV/℃	
		Ta=+25℃ to +85℃	—	-4.1	—		

Regulator output

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
V_{DDR} output voltage	V_{DDR}	No load	1.45	1.5	1.55	V	1

DC Characteristics (4 of 5)

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit

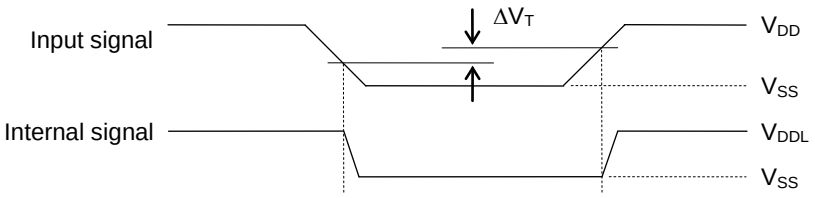
Output voltage 1 (P20 to P22) (P30 to P37) (P40 to P47) (P50 to P57) (P60 to P63)	VOH1	IOH1 = −0.5mA		DV_{DD} −0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20 to P22)	VOL2	When LED drive mode is selected	IOL2=+20mA DV_{DD}≧2.5V	—	—	0.5		
出力リーク (P20 to P22) (P30 to P37) (P40 to P47) (P50 to P57) (P60 to P63)	IOOH	VOH = DV_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = DV_{SS} (in high-impedance state)		−1	—	—		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = DV_{DD}		0	—	−1	μA	4
	IIL1	VIL1 = DV_{SS}		−1500	−300	−20		
Input current 2 (NMI) (P00 to P05) (P10) (P30 to P37) (P40 to P47) (P50 to P57) (P60 to P63)	IIH2	VIH2 = DV_{DD} (when pulled down)		2	30	250		
	IIL2	VIL2 = DV_{SS} (when pulled up)		−250	−30	−2		
	IIH2Z	VIH2 = DV_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = DV_{SS} (in high-impedance state)		-1	—	—		
Input current 3 (TEST0)	IIH3	VIH3=DV_{DD}		20	300	1500		
	IIL3	VIL3=DV_{SS}		-1	—	—		

DC Characteristics (5 of 5)

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

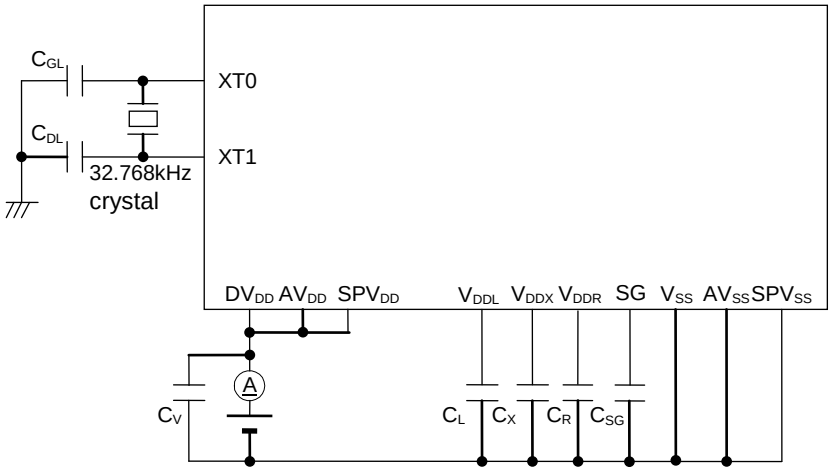
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST0) (TEST1_N) (NMI) (P00 to P05) (P10) (P30 to P37) (P40 to P47) (P50 to P57) (P60 to P63)	VIH1	—	0.7× DV_{DD}	—	DV_{DD}	V	5
	VIL1	—	0	—	0.3× DV_{DD}		
Hysteresis width (RESET_N) (TEST0) (TEST1_N) (NMI) (P00 to P05) (P10) (P30 to P37) (P40 to P47) (P50 to P57) (P60 to P63)	ΔVT	—	0.05× DV_{DD}	—	0.4× DV_{DD}		
Input pin capacitance (NMI) (P00 to P05) (P10) (P30 to P37) (P40 to P47) (P50 to P57) (P60 to P63)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

Hysteresis Width



Measuring Circuits

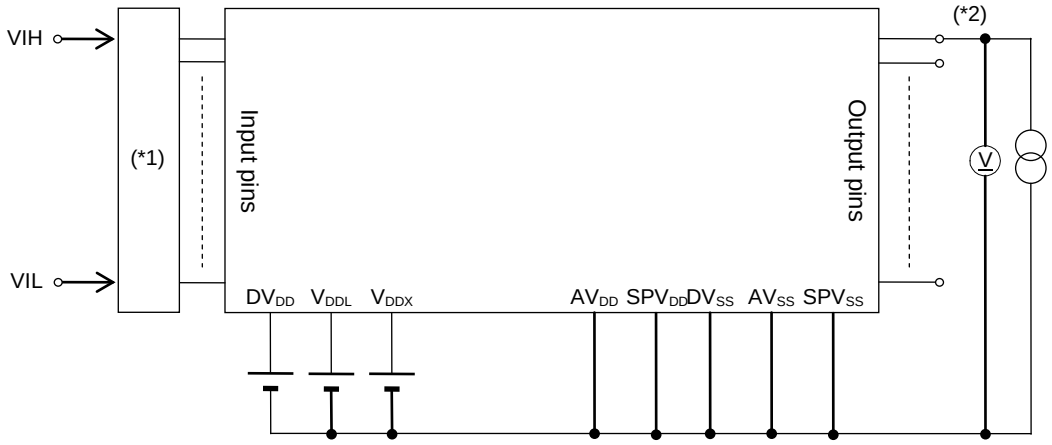
Measuring circuit 1



C_V	: 10µF
C_L	: 10µF
C_X	: 0.1µF
C_R	: 1µF
C_{SG}	: 0.1µF
C_{GL}	: 14pF
C_{DL}	: 14pF

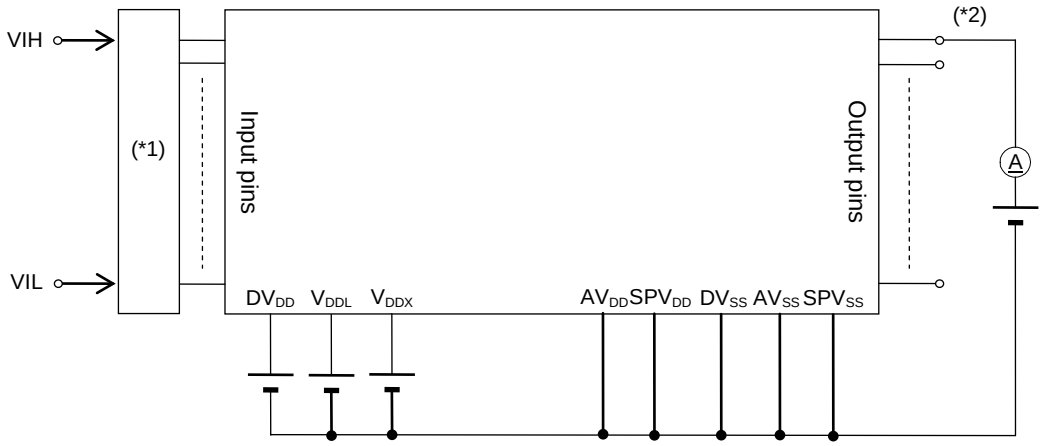
CPTiming

Measuring circuit 2



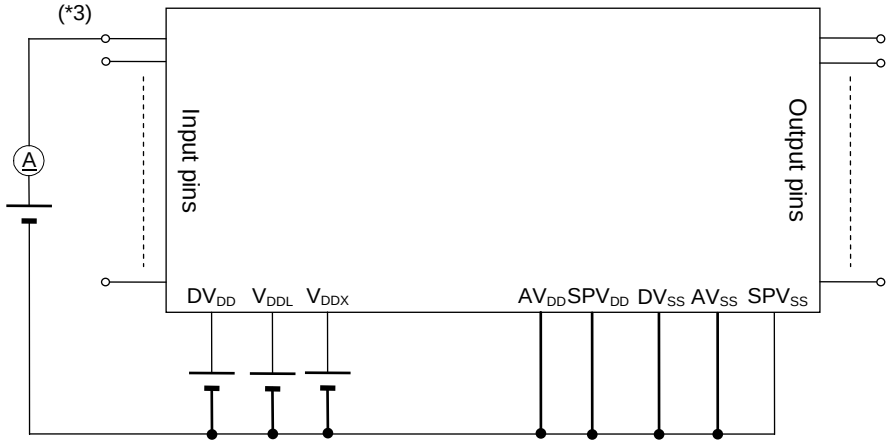
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 3



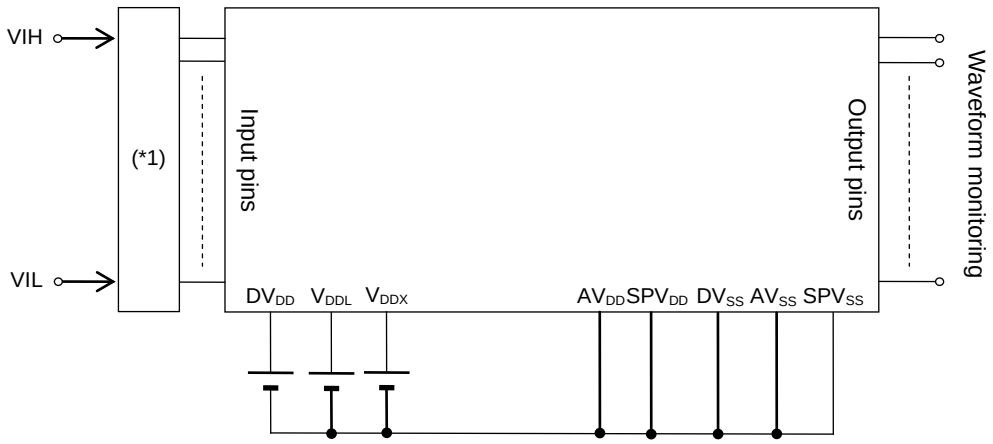
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 4



*3: Measured at the specified input pins.

Measuring circuit 5

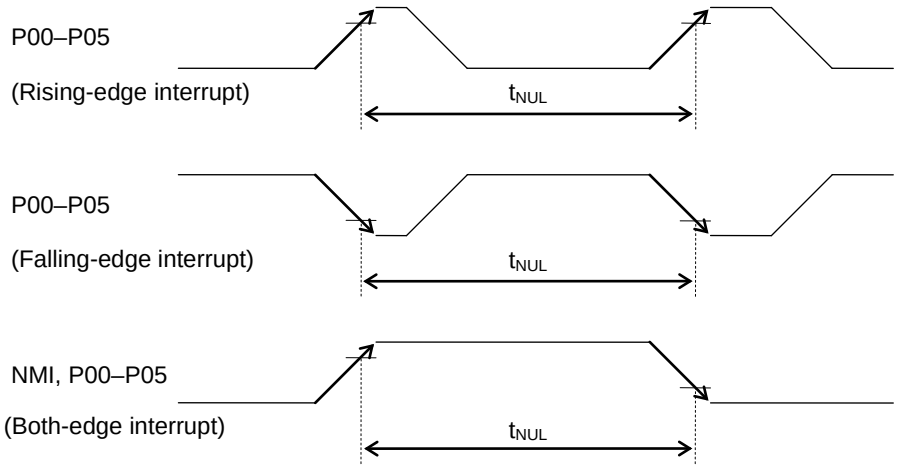


*1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5× sysclk	—	3.5× sysclk	μs

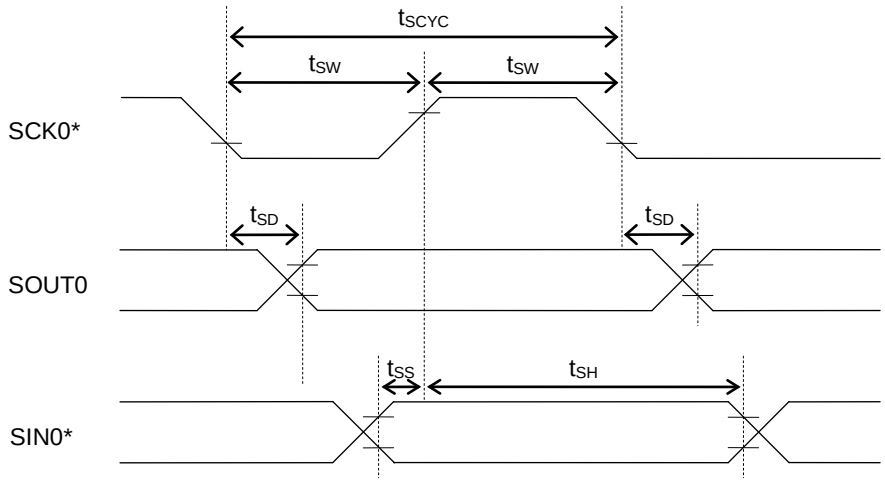


AC Characteristics (Synchronous Serial Port)

(DV_{DD}=AV_{DD}=SPV_{DD}=2.0 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	µs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	s
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	µs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected by S0CK3–0 of the serial port 0 mode register (SIO0MOD1)



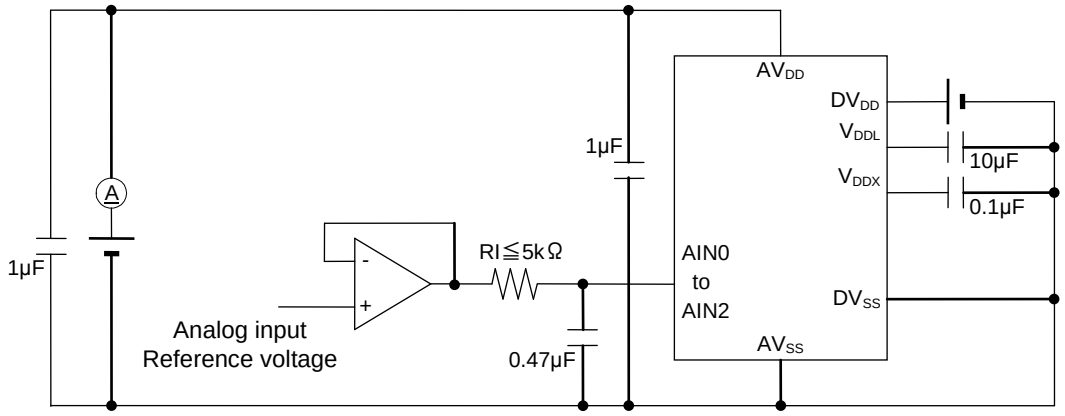
*: Indicates the tertiary function of the corresponding port.

Electrical Characteristics of Successive Approximation Type A/D Converter

(DV_{DD}=SPV_{DD}=2.0 to 3.6V, AV_{DD}=2.2 to 3.6V, DV_{SS}=AV_{SS}=SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V≦V_{REF}≦3.6V	–4	—	+4	LSB
		2.2V≦V_{REF}≦2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V≦V_{REF}≦3.6V	–3	—	+3	
		2.2V≦V_{REF}≦2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Input impedance	Z_I	—	—	—	5k	Ω
Conversion time	t_{CONV}	SACK=0 (HSCLK=3M to 4.2MHz) 2.2≦AV_{DD}	—	224	—	φ/CH
		SACK=1 (HSCLK=3M to 8.4MHz) 2.5≦AV_{DD}	—	160	—	

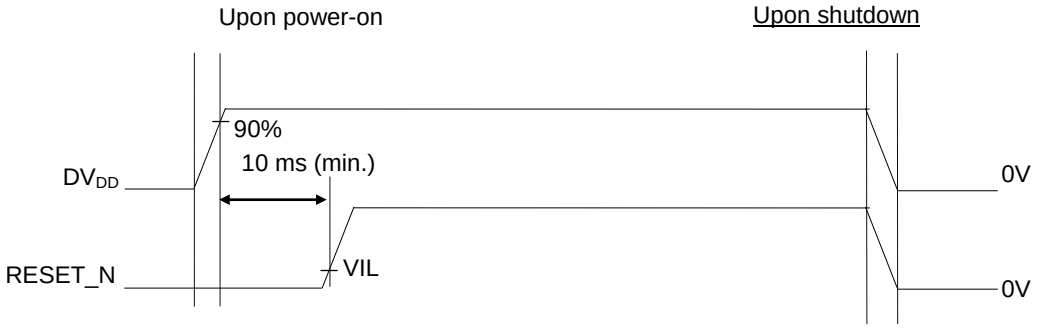
φ: Period of high-speed clock (HSCLK)



Power-on/Shutdown Sequence

■ When the power rise time is 10 ms or less

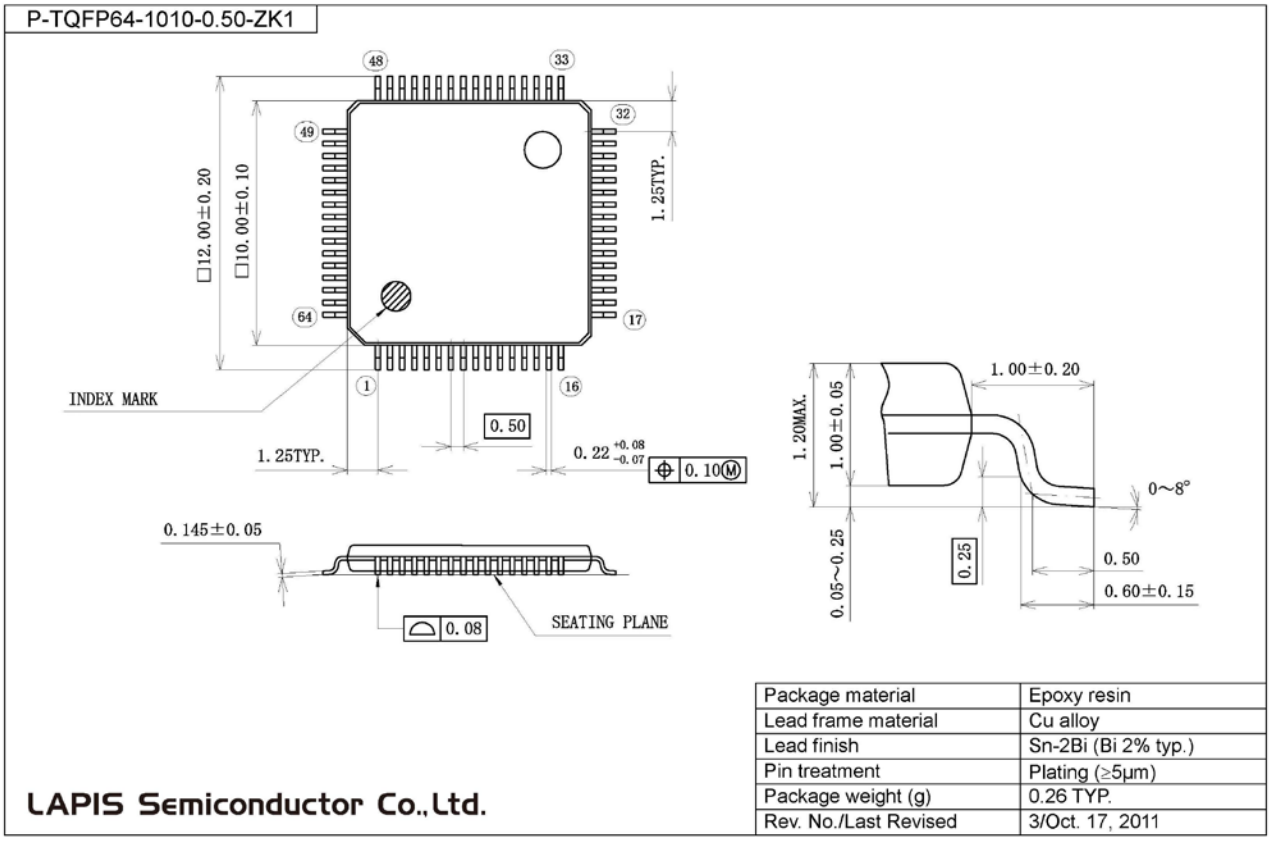
■ When the power rise time is more than 10 ms



When DV_{DD} becomes less than 2.0V, please set DV_{DD} to 0V, and repeat a Power-on Sequence.
Please supply voltage to AV_{DD} simultaneous with DV_{DD} or After DV_{DD} rises.

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Plating (≥5μm)
Package weight (g)	0.26 TYP.
Rev. No./Last Revised	3/Oct. 17, 2011

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

Condition	Example 1 (EIA/JESD51)	Example 2
PCB	W/L/t= 76.2 / 114.5 / 1.6(mm)	W/L/t= 50 / 50 / 1.6(mm)
PCB Layer	2Layers	2Layers
Cu thickness	40(um)	30(um)
Cu density	60% / 60% (Two-Sided)	80% / 60% (Two-Sided)
Air cooling conditions	Calm(0m/sec)	Calm(0m/sec)
Heat resistance(θJa)	41.3[℃/W]	46.1[℃/W]
Power consumption of Chip PMax at OutputPower 0.5W (3.6V)	0.472[W] (ML610Q359) 0.562[W] (ML610Q360)	

TjMax of this LSI is 125℃. TjMax is expressed with the following formulas.
TjMax = TaMax + θJa × PMax

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q359-01	Jul 31, 2015	–	–	Final edition 1

Notes

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