FEDL610Q461-03
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ML610Q461/ML610Q462/ML610Q463

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which peripheral circuits, such as synchronous serial port, UART, RC oscillation type A/D converter, and LCD driver, are incorporated around LAPIS Semiconductor-original 8-bit CPU nX-U8/100. ML610Q461 /ML610Q462/ML610Q463 operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    2μs (@500kHz system clock)
    0.5μs(@2MHz system clock)

- Internal memory
  - Internal 16KByte Flash ROM (8K×16 bits) (including unusable 1K Byte TEST area)
  - Internal 1KByte Data RAM (1024×8 bits)

- Interrupt controller
  - 1 non-maskable interrupt sources
    Internal source: 1 (Watch dog timer)
  - 17 maskable interrupt sources
    Internal sources: 12 (SSIO0, Timer0, Timer1, Timer2, Timer3, UART0, RC-A/D converter, PWM0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    External sources: 5 (P00, P01, P02, P03, P04)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  – 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  – Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- Capture
  – Time base capture × 2 channels (4096 Hz to 32 Hz)

- PWM
  – Resolution 16 bits × 1 channel

- Synchronous serial port
  – Master/slave selectable × 1 channel
  – LSB first/MSB first selectable
  – 8-bit length/16-bit length selectable

- UART
  – Half-Duplex Communication
  – TXD/RXD × 1 channel
  – Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  – Positive logic/negative logic selectable
  – Built-in baud rate generator

- RC oscillation type A/D converter
  – 16-bit counter
  – Time division × 2 channels

- General-purpose ports
  – Input-only port × 5 channels (including secondary functions)
  – Output-only port
    ML610Q461 : 10 channels (including secondary functions)
    ML610Q462 : 6 channels (including secondary functions)
    ML610Q463 : 2 channels (including secondary functions)
  – Input/output port × 14 channels (including secondary functions)

- LCD driver
  – The number of segments
    ML610Q461 : 64 dots max. (16seg×4com)
    ML610Q462 : 80 dots max. (20seg×4com)
    ML610Q463 : 96 dots max. (24seg×4com)
  – 1/1 to 1/4 duty
  – 1/2, 1/3 bias (built-in bias generation circuit)
  – Frame frequency selecable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
  – Bias voltage multiplying clock selectable (8 types)
  – LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Reset
  – Reset through the RESET_N pin
  – Power-on reset generation when powered on
  – Reset when oscillation stop of the low-speed clock is detected
  – Reset by the watchdog timer (WDT) overflow

- Clock
  – Low-speed clock: Crystal oscillation (32.768 kHz)
    (This LSI can not guarantee the operation withoug low-speed crystal oscillation clock)
  – High-speed clock: Built-in RC oscillation (500 kHz, 2MHz)

- Power management
  – HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  – STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  – High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
  – Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Guaranteed operating range
  – Operating temperature: –20°C to +70°C
  – Operating voltage: V_{DD} = 1.25V to 3.6V

- Product name －Supported Function
  The line-up of the ML610Q461 ,the ML610Q462 and the ML610Q463 are below.

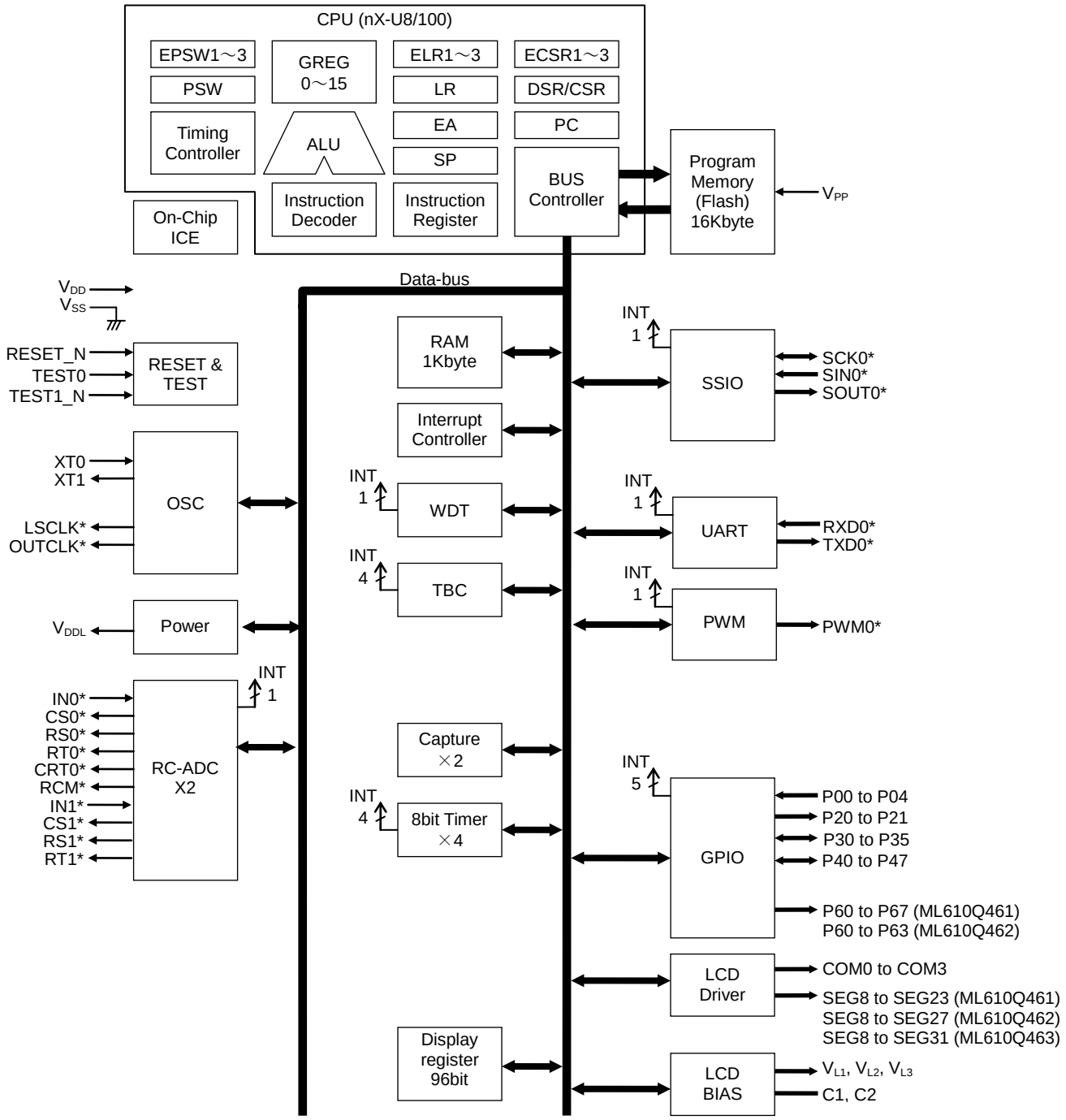
- 64-Pin plastic TQFP -	ROM type	Operating temperature	Product availability
ML610Q461-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q462-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q463-xxxTB	Flash ROM	-20°C to +70°C	Yes

xxx：ROM code number (xxx of the blank product is NNN)
Q：Flash ROM version
TB：TQFP

BLOCK DIAGRAM

Block Diagram of ML610Q461/ML610Q462/ML610Q463

Figure 1 show the block diagram of the ML610Q461/ML610Q462/ML610Q463.

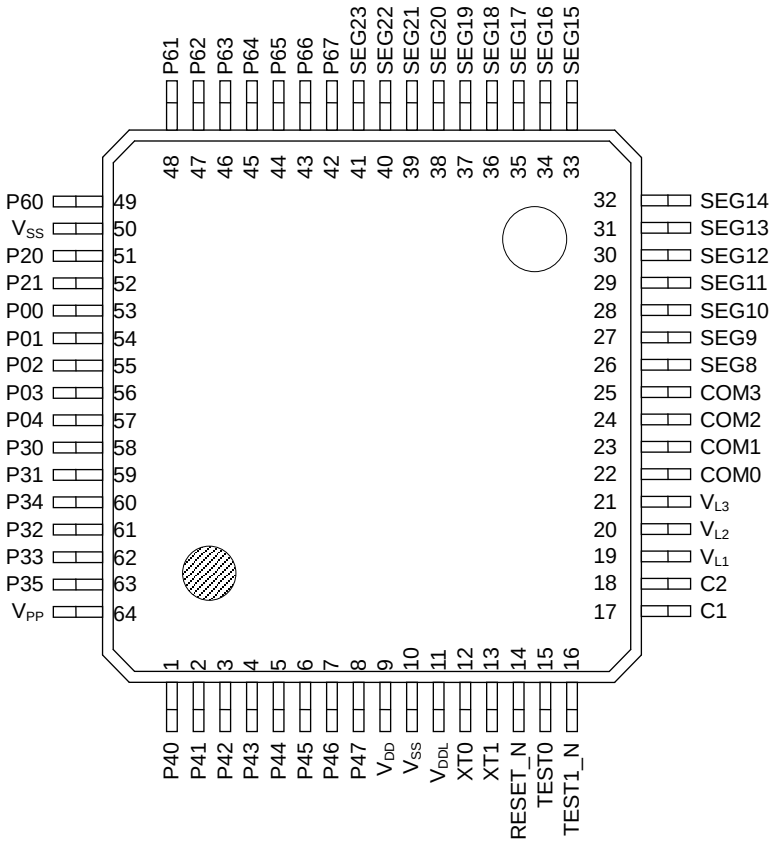


"*" indicates the secondary or tertiary function of each port.

Figure 1 ML610Q461/ML610Q462/ML610Q463 Block Diagram

PIN CONFIGURATION

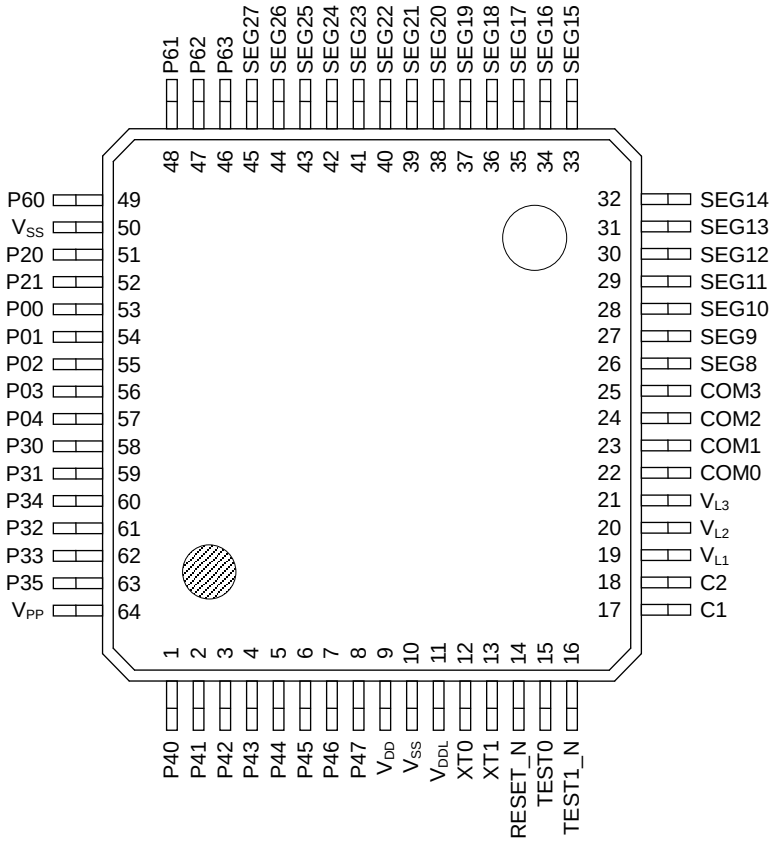
ML610Q461 TQFP64 Pin Layout



Note: The assignment of the P30 to P35 are not in order.

Figure 2 ML610Q461 TQFP64 Pin Configuration

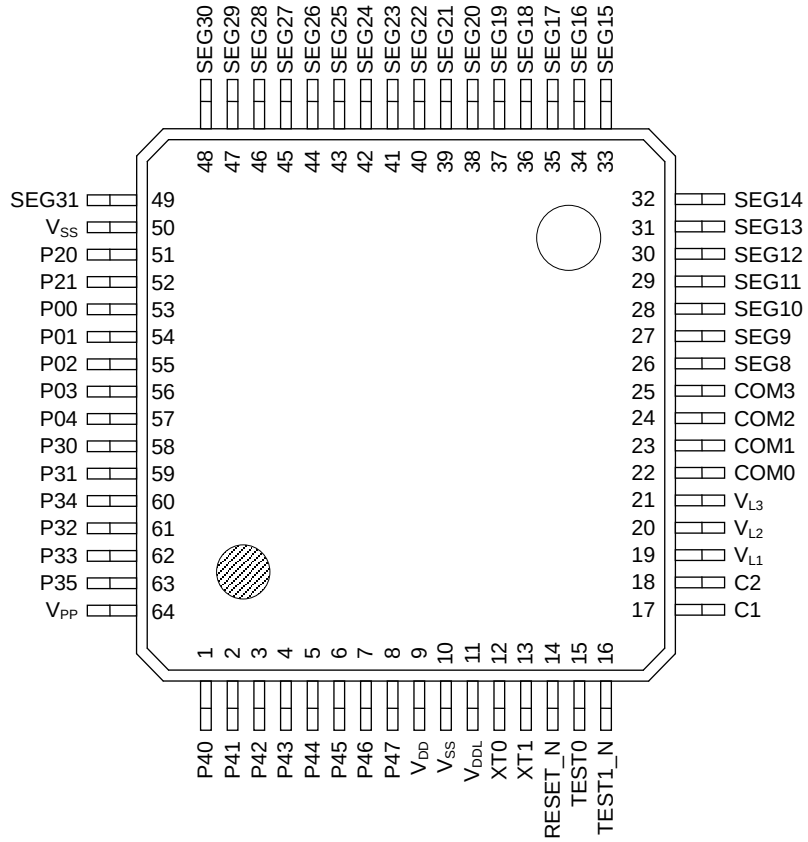
ML610Q462 TQFP64 Pin Layout



Note: The assignment of the P30 to P35 are not in order.

Figure 3 ML610Q462 TQFP64 Pin Configuration

ML610Q463 TQFP64 Pin Layout



Note: The assignment of the P30 to P35 are not in order.

Figure 4 ML610Q463 TQFP64 Pin Configuration

PIN LIST

PIN No.	Primary function			Secondary function or Tertiary function			
	Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
10 50	Vss	—	Negative power supply pin	—	—	—	—
9	V_{DD}	—	Positive power supply pin	—	—	—	—
11	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—
64	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—
19	V_{L1}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*1)	—	—	—	—
20	V_{L2}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*1)	—	—	—	—
21	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
17	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—
18	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—
15	TEST0	I/O	Test pin	—	—	—	—
16	TEST1_N	I	Test pin	—	—	—	—
14	RESET_N	I	Reset input pin	—	—	—	—
12	XT0	I	Low-speed clock oscillation pin	—	—	—	—
13	XT1	O	Low-speed clock oscillation pin	—	—	—	—
53	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—	—
54	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—	—
55	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 received data	—	—	—	—
56	P03/EXI3	I	Input port, External interrupt	—	—	—	—
57	P04/EXI4/ T02P0CK	I	Input port, Timer 0/Timer 2/PWM0 external clock input External interrupt	—	—	—	—
51	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
52	P21/LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
58	P30	I/O	Input/output port	Secondary	IN0	I	RC type ADC0 oscillation input pin
59	P31	I/O	Input/output port	Secondary	CS0	O	RC type ADC0 reference capacitor connection pin
60	P34	I/O	Input/output port	Secondary	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
61	P32	I/O	Input/output port	Secondary	RS0	O	RC type ADC0 reference resistor connection pin
62	P33	I/O	Input/output port	Secondary	RT0	O	RC type ADC0 measurement resistor sensor connection pin
63	P35	I/O	Input/output port	Secondary	RCM	O	RC type ADC oscillation monitor

PIN No.	Primary function			Secondary function or Tertiary function			
	Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
1	P40	I/O	Input/output port	Secondary	—	—	—
				Tertiary	SIN0	I	SSIO0 data input
2	P41	I/O	Input/output port	Secondary	—	—	—
				Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
3	P42	I/O	Input/output port	Secondary	RXD0	I	UART data input
				Tertiary	SOUT0	O	SSIO0 data output
4	P43	I/O	Input/output port	Secondary	TXD0	O	UART data output
				Tertiary	PWM0	O	PWM0 output
5	P44/ T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	Secondary	IN1	I	RC type ADC1 oscillation input pin
				Tertiary	SIN0	I	SSIO0 data input
6	P45/T13CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	Secondary	CS1	O	RC type ADC1 reference capacitor connection pin
				Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
7	P46	I/O	Input/output port	Secondary	RS1	O	RC type ADC1 reference resistor connection pin
				Tertiary	SOUT0	O	SSIO0 data output
8	P47	I/O	Input/output port	Secondary	RT1	O	RC type ADC1 measurement resistor sensor connection pin

PIN No.	Primary function			Secondary function or Tertiary function			
	Pin name	I/O	Function	Secondary/ Tertiary	Pin name	I/O	Function
22	COM0	O	LCD common pin	—	—	—	—
23	COM1	O	LCD common pin	—	—	—	—
24	COM2	O	LCD common pin	—	—	—	—
25	COM3	O	LCD common pin	—	—	—	—
26	SEG8	O	LCD segment pin	—	—	—	—
27	SEG9	O	LCD segment pin	—	—	—	—
28	SEG10	O	LCD segment pin	—	—	—	—
29	SEG11	O	LCD segment pin	—	—	—	—
30	SEG12	O	LCD segment pin	—	—	—	—
31	SEG13	O	LCD segment pin	—	—	—	—
32	SEG14	O	LCD segment pin	—	—	—	—
33	SEG15	O	LCD segment pin	—	—	—	—
34	SEG16	O	LCD segment pin	—	—	—	—
35	SEG17	O	LCD segment pin	—	—	—	—
36	SEG18	O	LCD segment pin	—	—	—	—
37	SEG19	O	LCD segment pin	—	—	—	—
38	SEG20	O	LCD segment pin	—	—	—	—
39	SEG21	O	LCD segment pin	—	—	—	—
40	SEG22	O	LCD segment pin	—	—	—	—
41	SEG23	O	LCD segment pin	—	—	—	—
42	P67(*2)	O	Output port	—	—	—	—
	SEG24(*3) (*4)	O	LCD segment pin	—	—	—	—
43	P66(*2)	O	Output port	—	—	—	—
	SEG25(*3) (*4)	O	LCD segment pin	—	—	—	—
44	P65(*2)	O	Output port	—	—	—	—
	SEG26(*3) (*4)	O	LCD segment pin	—	—	—	—
45	P64(*2)	O	Output port	—	—	—	—
	SEG27(*3) (*4)	O	LCD segment pin	—	—	—	—
46	P63(*2) (*3)	O	Output port	—	—	—	—
	SEG28(*4)	O	LCD segment pin	—	—	—	—
47	P62(*2) (*3)	O	Output port	—	—	—	—
	SEG29(*4)	O	LCD segment pin	—	—	—	—
48	P61(*2) (*3)	O	Output port	—	—	—	—
	SEG30(*4)	O	LCD segment pin	—	—	—	—
49	P60(*2) (*3)	O	Output port	—	—	—	—
	SEG31(*4)	O	LCD segment pin	—	—	—	—

(*1) Internally generated, or connect to either positive power supply pin (V_{DD}) or power supply pin for internal logic (V_{DDL}). For details, see “Chapter 20 LCD Drivers. In the user’s manual”
(*2) For ML610Q461. (*3) For ML610Q462. (*4) For ML610Q463.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} .	—	—
XT1	O		—	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P04	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P21	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P60-P63	O	General-purpose output port. Incorporated only into ML610Q461/ML610Q462, and not into ML610Q463.	Primary	Positive
P64-P67	O	General-purpose output port. Incorporated only into ML610Q461, and not into ML610Q462/ ML610Q463.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
External interrupt				
EXI0-4	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P04 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
LED drive				
LED0-1	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0-3	O	Common output pins.	—	—
SEG8-23	O	Segment output pins.	—	—
SEG24-27	O	Segment output pins. Incorporated into ML610Q462/ML610Q463, not into ML610Q461.	—	—
SEG28-31	O	Segment output pins. Incorporated into ML610Q463, not into ML610Q461/ML610Q462.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated or positive power supply pin connected). Depending on LCD Bias setting and V_{DD} voltage level, V_{DD} or V_{DDL} or capacitor is connected. For details of the connection method, see user's manual.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST0	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
TEST1_N	I	Input pin for testing. A pull-up resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitor CL (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
V_{L1}, V_{L2}, V_{L3}	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
TEST1_N	Open
P00 to P04	V_{DD} or V_{SS}
P20 to P21	Open
P30 to P35	Open
P40 to P47	Open
P60 to P67	Open
COM0 to 3	Open
SEG8 to 31	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 4	V_{L1}	Ta = 25°C	–0.3 to +2.0	V
Power supply voltage 5	V_{L2}	Ta = 25°C	–0.3 to +4.0	V
Power supply voltage 6	V_{L3}	Ta = 25°C	–0.3 to +6.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–6, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–20 to +70	°C
Operating voltage	V_{DD}	f_{OP} = 30k to 625kHz	1.25 to 3.6	V
		f_{OP} = 30k to 2.5MHz	1.8 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.25 to 3.6V	30k to 625k	Hz
		V_{DD} = 1.8 to 3.6V	30k to 2.5M	
Capacitor externally connected to V_{DDL} pin	C_L	—	0.47±30%	μF
Capacitors externally connected to $V_{L1, 2, 3}$ pins	$C_{a, b, c}$	—	0.1±30%	μF
Capacitors externally connected across C1 and C2 pins	C_{12}	—	0.47±30%	μF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation	—	12	—	pF
		C_L=9pF of crystal oscillation	—	18	—	

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase*1	2.75 to 3.6	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase*1	7.7 to 8.3	
erase/program cycles	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

*1: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM. V_{PP} pin has an internal pulldown resister.

DC CHARACTERISTICS (1/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified)

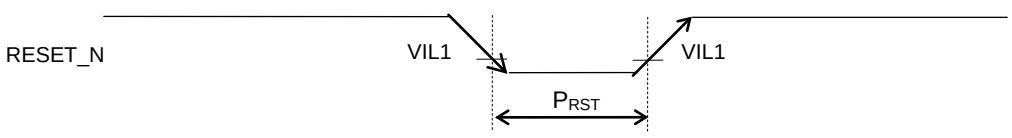
Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
500kHz/2MHz RC oscillation frequency	f_{RC}	V_{DD} = 1.25 to 3.6V	Ta = 25°C	Typ. −10%	500	Typ. +10%	kHz	1
			*3	Typ. −25%	500	Typ. +25%		
		V_{DD} = 1.80 to 3.6V	Ta = 25°C	Typ. −10%	2.0	Typ. +10%	MHz	
			*3	Typ. −25%	2.0	Typ. +25%		
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.6	2	s	
500kHz/2MHz RC oscillation start time	T_{RC}	—		—	—	0.3	μs	
Low-speed oscillation stop detect time*1	T_{STOP}	—		12	16.4	41	ms	
Reset pulse width	P_{RST}	—		200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

*2 : Use 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=12pF).

*3 : Recommended operating temperature (Ta = −20 to +70°C)

[Reset pulse width]



Reset pulse width (P_{RST})

[Power-on reset activation power rise time]

Power-on reset activation power rise time (T_{POR})

DC CHARACTERISTICS (2/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
V_{DDL} voltage	V_{DDL}	f_{OP} = 30k to 625kHz	1.1	1.2	1.3		1
		f_{OP} = 30k to 2.5MHz	1.35	1.5	1.65		
V_{DDL} temperature deviation *1	ΔV_{DDL}	V_{DD} = 3.0V	—	-1	—	mV/°C	
V_{DDL} voltage dependency *1	ΔV_{DDL}	—	—	5	20	mV/V	

*1:V_{DDL} can not exceed V_{DD} level. The maximum V_{DDL} becomes V_{DD} level when the V_{DDL} calculated by the temperature deviation and voltage dependency is going to exceed the V_{DD} level.

DC CHARACTERISTICS (3/5)

(V_{DD} = 3.0V, V_{SS} = 0V, Ta = −20 to +70°C)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz/2MHz oscillation: stopped.	Ta= 25°C	—	0.4	0.8	μA	1
			*5	—	—	8		
Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating).*3*4 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *6	Ta= 25°C	—	0.9	1.8	μA	
			*5	—	—	9		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	5	8	μA	
			*5	—	—	15		
Supply current 4-1	IDD4-1	CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	70	100	μA	
			*5	—	—	120		
Supply current 4-2	IDD4-2	CPU: In RC 2MHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	280	350	μA	
			*5	—	—	400		

*1: When the CPU operating rate is 100% (No HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)
*4 : Significant bits of BLKCON0~BLKCON4 registers except DLCD bit on BLKCON4 are all “1”.
*5 : Recommended operating temperature (Ta = −20 to +70°C)
*6: LCD Stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P21 Nch open drain mode is Not selected) (P30–P35) (P40–P47) (P60–P67)	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V	V_{DD} –0.5	—	—	V	2
		IOH1 = -0.03mA, V_{DD} = 1.25 to 3.6V	V_{DD} –0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20–P21 Nch open drain mode is selected)	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0 to 3) (SEG8 to 23)*1 (SEG8 to 27)*2 (SEG8 to 31)*3	VOH3	IOH4 = –0.05mA, VL1=1.2V	V_{L3} –0.2	—	—		
	VOML3	IOMH4 = +0.05mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOML3S	IOM4S = –0.05mA, VL1=1.2V	V_{L2} –0.2	—	—		
	VOLM3	IOML4 = +0.05mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOLM3S	IOML4S = –0.05mA, VL1=1.2V	V_{L1} –0.2	—	—		
	VOL3	IOL4 = +0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20–P21) (P30–P35) (P40–P47) (P60–P67)	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	–1	—	—		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V_{DD}	0	—	1	µA	4
	IIL1	VIL1 = V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH1 = V_{DD}	2	300	600		
	IIL2	VIL1 = V_{ss}	-1	—	—		
Input current 3 (P00-P04) (P30-P35) (P40-P47)	IIH3	VIH3 = V_{DD} ,V_{DD} = 1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3 = V_{DD} ,V_{DD} = 1.25 to 3.6V (when pulled-down)					
	IIL3	VIL3 = V_{SS} , V_{DD} = 1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3 = V_{SS} , V_{DD} = 1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3 = V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3 = V_{SS} (in high-impedance state)	–1	—	—		

*1: Characteristics for ML610Q461.
*2: Characteristics for ML610Q462.
*3: Characteristics for ML610Q463.

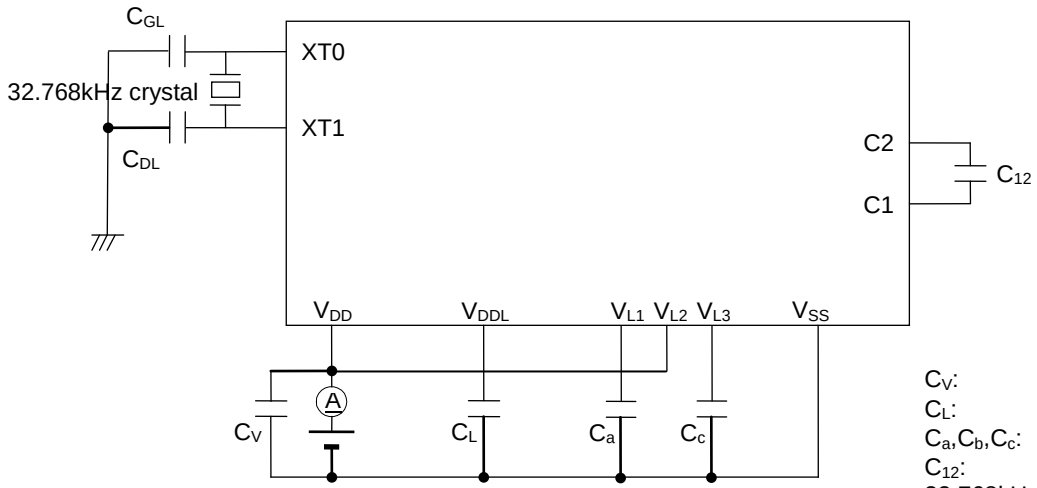
DC CHARACTERISTICS (5/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0, TEST1_N) (P00–P04) (P30–P35) (P40–P47)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD} = 1.8 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00–P04) (P30–P35) (P40–P47)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

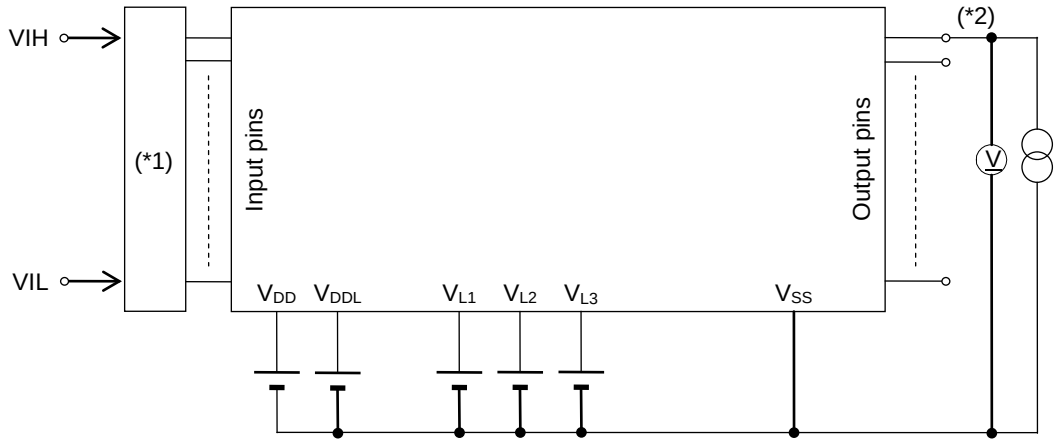
MEASURING CIRCUITS

MEASURING CIRCUIT 1



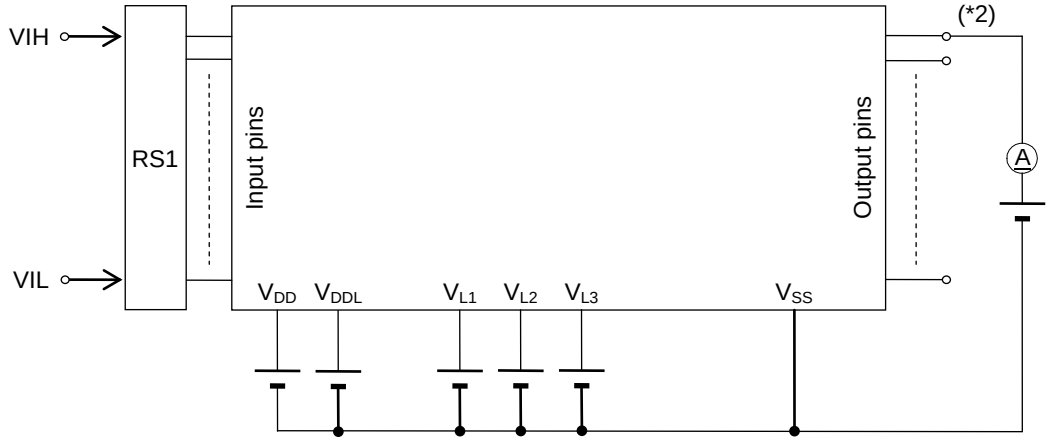
C_V: 1µF
C_L: 0.47µF
C_a,C_b,C_c: 0.1µF
C_{12}: 0.47µF
32.768kHz crystal: DT-26 (Load capacitance 6pF)
(made by KDS:DAISHINKU CORP.)
C_{GL}, C_{DL}: 6pF

MEASURING CIRCUIT 2



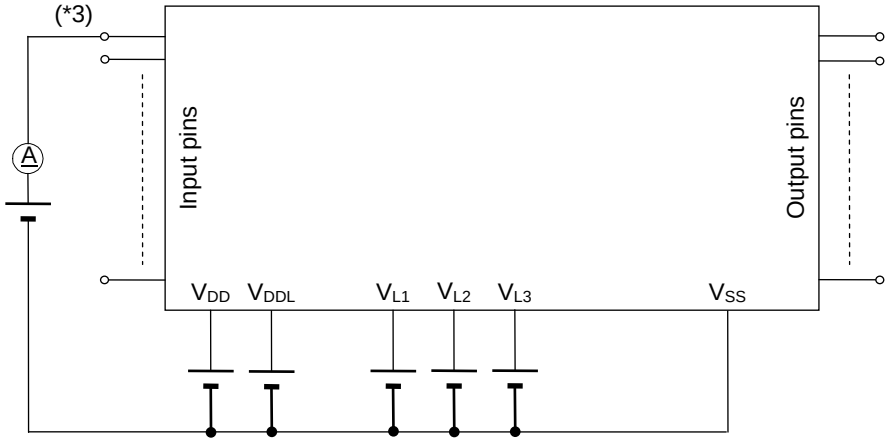
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



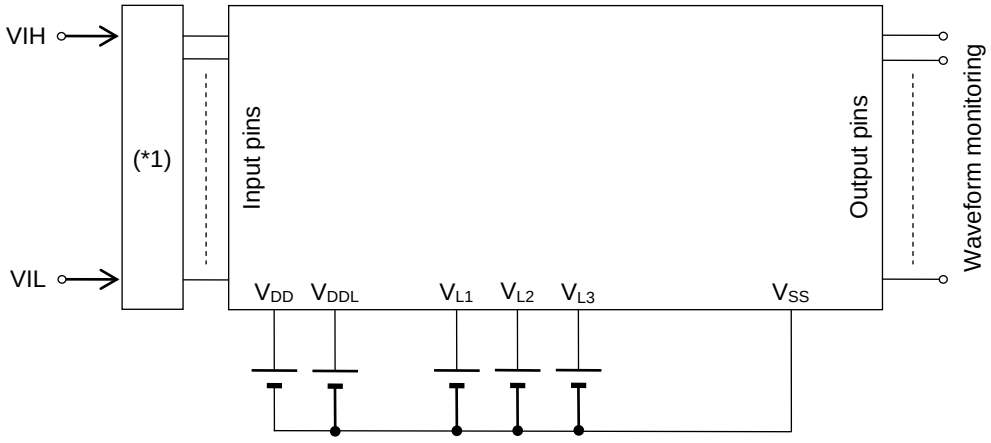
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

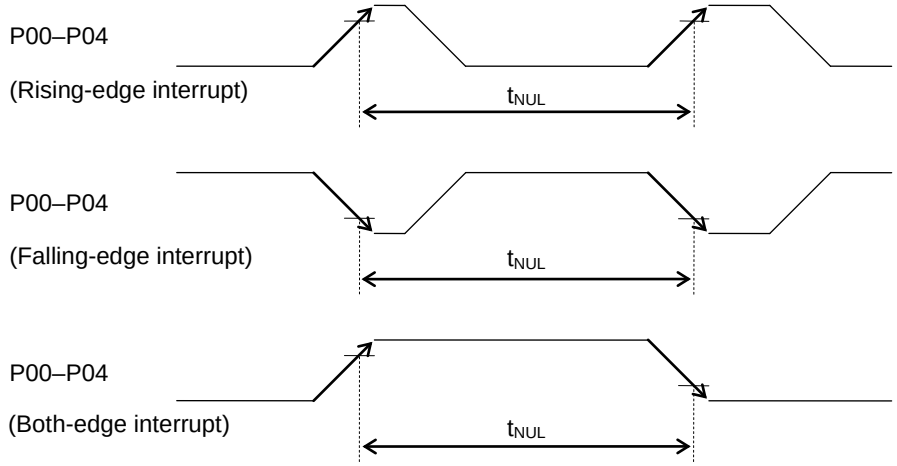


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

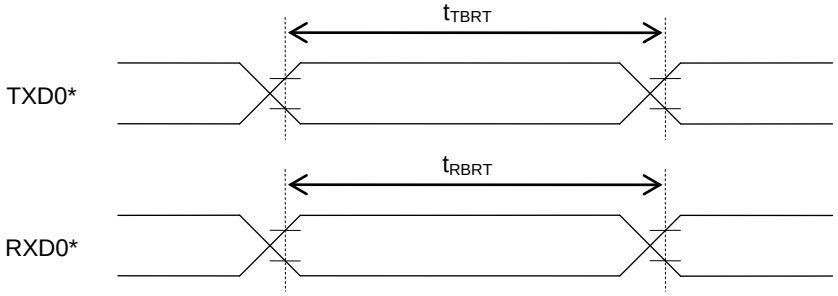


AC CHARACTERISTICS (Serial Port)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*1	—	s
Receive baud rate	t_{RBRT}	—	BRT*1 –3%	BRT*1	BRT*1 +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

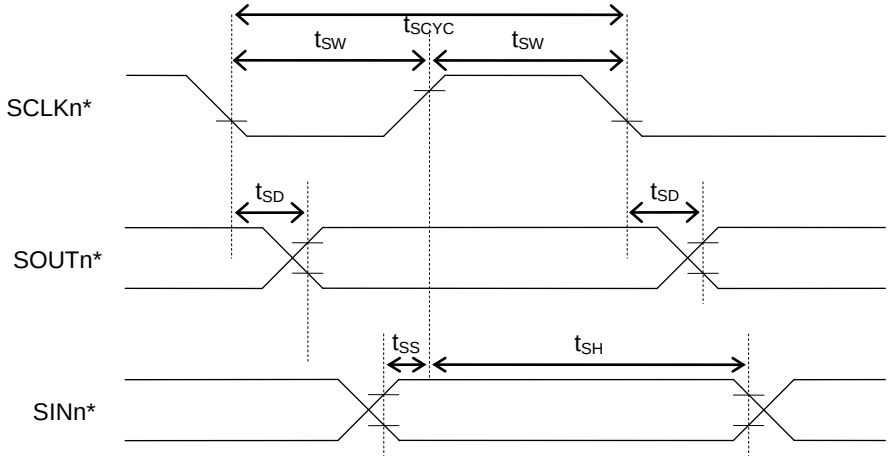
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLKn input cycle (slave mode)	t_{SCYC}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	10	—	—	µs
		When RC oscillation is 2MHz *3 (V_{DD} = 1.8 to 3.6V)	2	—	—	
SCLKn output cycle (master mode)	t_{SCYC}	—	—	SCLKn*1	—	s
SCLKn input pulse width (slave mode)	t_{SW}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	4	—	—	µs
		When RC oscillation is 2MHz *3 (V_{DD} = 1.8 to 3.6V)	04	—	—	
SCLKn output pulse width (master mode)	t_{SW}	—	SCLKn*1 ×0.4	SCLKn*1 ×0.5	SCLKn*1 ×0.6	s
SOUTn output delay time (slave mode)	t_{SD}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V) output load 10pF	—	—	500	ns
		When RC oscillation is 2MHz *3 (V_{DD} = 1.8 to 3.6V) output load 10pF	—	—	240	
SOUTn output delay time (master mode)	t_{SD}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V) output load 10pF	—	—	500	ns
		When RC oscillation is 2MHz *3 (V_{DD} = 1.8 to 3.6V) output load 10pF	—	—	240	
SINn input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SINn input setup time (master mode)	t_{SS}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	500	—	—	ns
		When RC oscillation is 2MHz *3 (V_{DD} = 1.8 to 3.6V)	240	—	—	
SINn input hold time	t_{SH}	When RC oscillation is 500kHz *2 (V_{DD} = 1.25 to 3.6V)	300	—	—	ns
		When RC oscillation is 2MHz *3 (V_{DD} = 1.8 to 3.6V)	80	—	—	

n= 0,1

*1: Clock period selected with SnCK3–0 of the serial port n mode register (SIOnMOD1)

*2: When 500kHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)

*3: When 2MHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)



*: Indicates the secondary function of the port (n= 0,1)

AC CHARACTERISTICS (RC Oscillation A/D Converter)

Condition for V_{DD}=1.8 to 3.6V

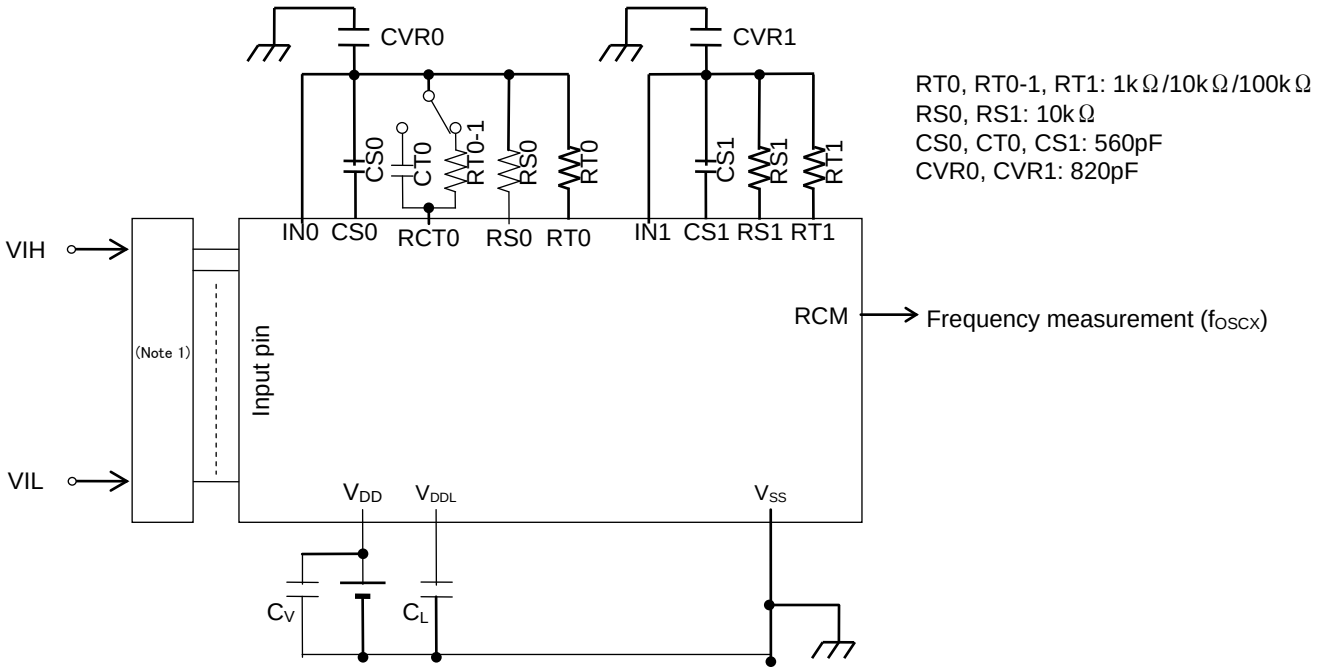
(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=1kΩ	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10kΩ	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100kΩ	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1 =1kΩ	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1, RT1 =10kΩ	0.981	1	1.019	—
	Kf3	RT0, RT0-1, RT1 =100kΩ	0.099	0.101	0.104	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCX}(\text{RT0-CS0 oscillation})}{f_{OSCX}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCX}(\text{RT0-1-CS0 oscillation})}{f_{OSCX}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCX}(\text{RT1-CS1 oscillation})}{f_{OSCX}(\text{RS1-CS1 oscillation})}$$

(x = 1, 2, 3)



*1: Input logic circuit to determine the specified measuring conditions.

Condition for V_{DD}=1.25 to 3.6V

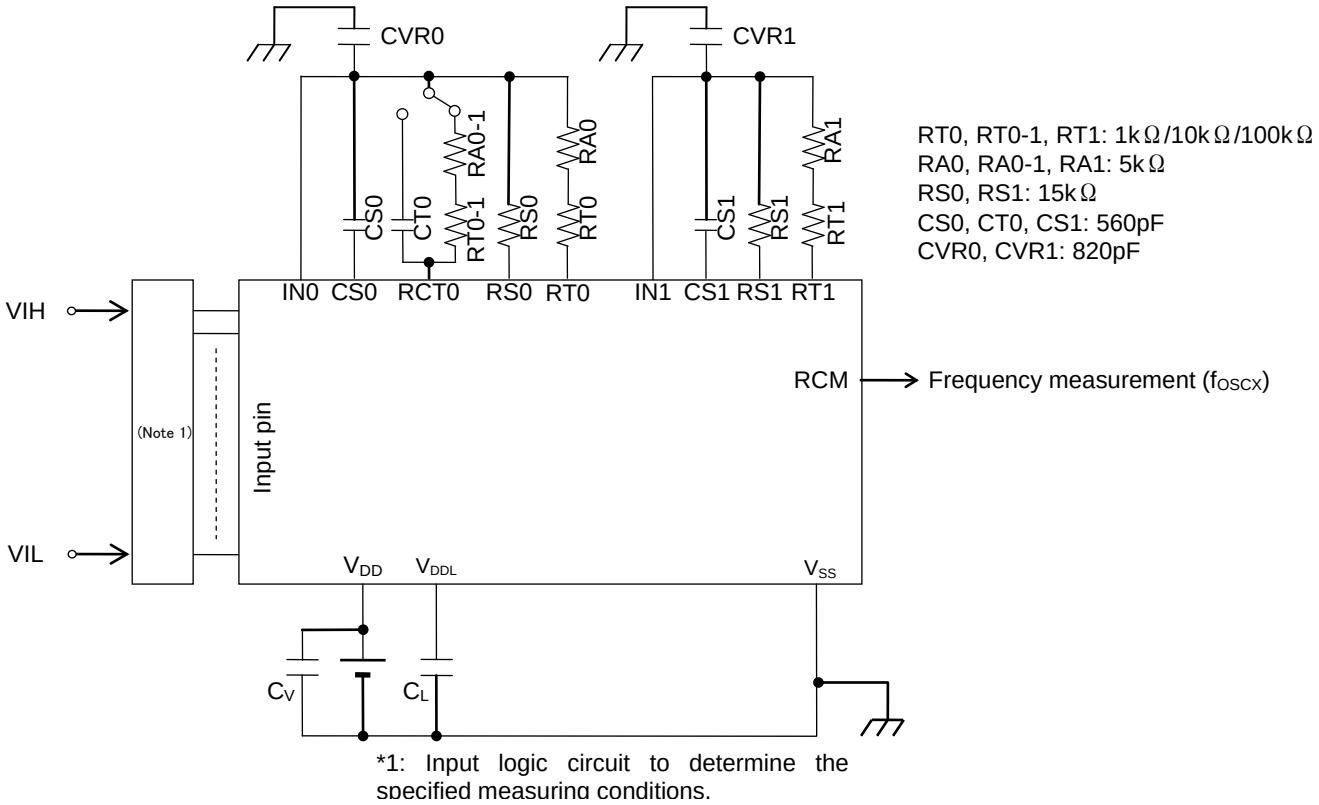
(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 1.5V	f_{OSC1}	Resistor for oscillation=6kΩ	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 1.5V	Kf1	RT0, RT0-1, RT1 =1kΩ	2.139	2.381	2.632	—
	Kf2	RT0, RT0-1, RT1 =10kΩ	0.973	1	1.028	—
	Kf3	RT0, RT0-1, RT1 =100kΩ	0.142	0.147	0.152	—
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=6kΩ	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1 =1kΩ	2.227	2.432	2.626	—
	Kf2	RT0, RT0-1, RT1 =10kΩ	0.982	1	1.018	—
	Kf3	RT0, RT0-1, RT1 =100kΩ	0.141	0.145	0.149	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCX}(\text{RT0-CS0 oscillation})}{f_{OSCX}(\text{RS0-CS0 oscillation})} , \frac{f_{OSCX}(\text{RT0-1-CS0 oscillation})}{f_{OSCX}(\text{RS0-CS0 oscillation})} , \frac{f_{OSCX}(\text{RT1-CS1 oscillation})}{f_{OSCX}(\text{RS1-CS1 oscillation})}$$

(x = 1, 2, 3)



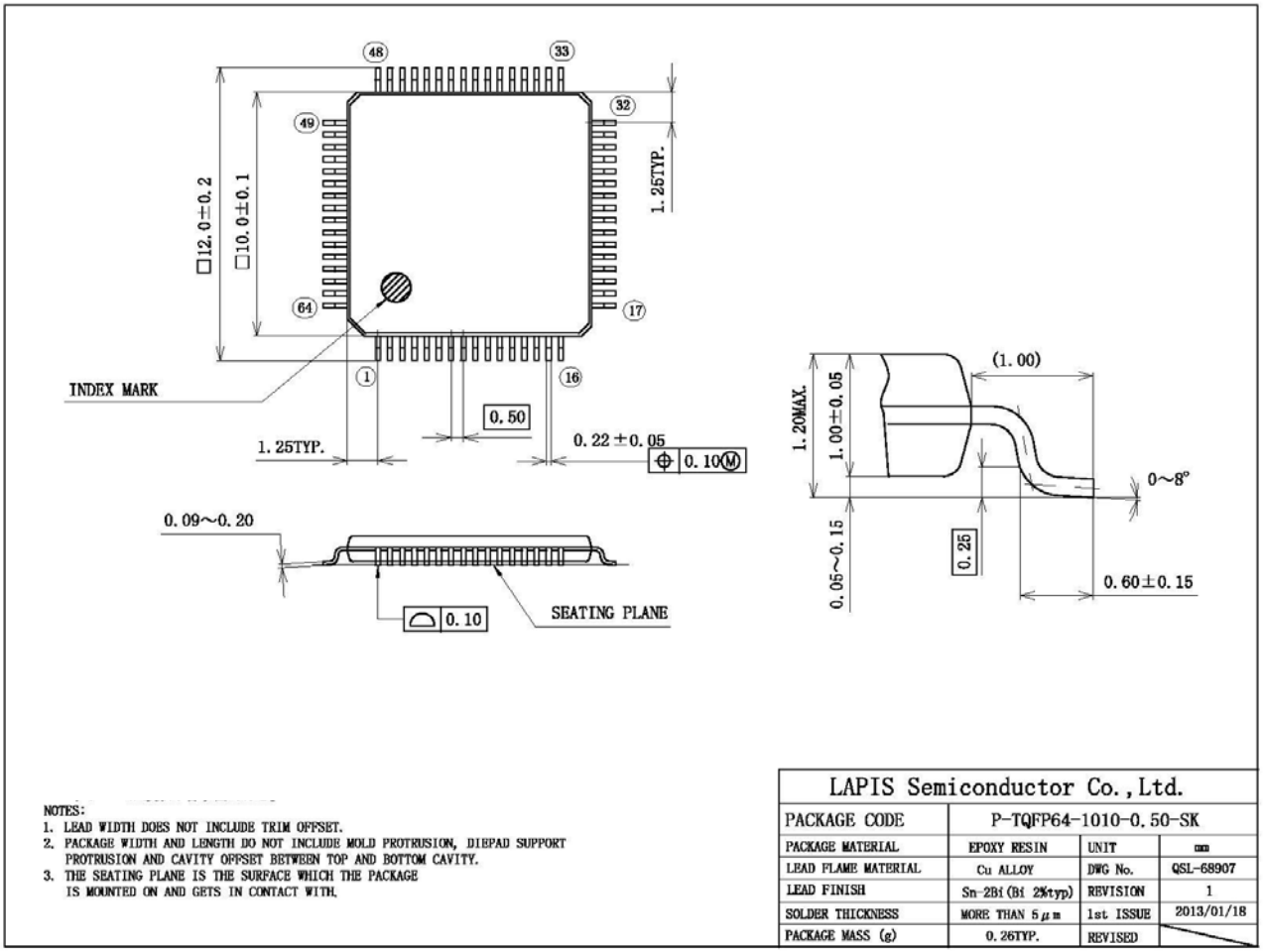
*1: Input logic circuit to determine the specified measuring conditions.

Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Package Dimensions

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q461-01	Oct.10,2013	–	–	Final edition 1
FEDL610Q461-02	Apr. 14, 2015	All	All	Change header and footer.
		1-4 6-11 14 15 17	1-4 8 9 11	Delete ML610Q462 and ML610Q463
		1 3 19-24 27-30	1 3 15-20 23-26	Delete wide range temperature version (P version)
		3	3	Change from "Shipment" to "Product name – Supported Function"
		–	13	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		20	14	Change "RESET" to "Reset pulse width (P_{RST}) " and "Power-on reset activation power rise time (T_{POR}) ".
		25	25	Change in the Package figure
		34	27	Change description in Notes.
FEDL610Q461-03	July.28,2015	All	All	Change header.
		1-4 8-9 11	1-4 6-7 10-11 13	Add ML610Q462 and ML610Q463

Notes

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