

# ML620Q151B/2B/3B/4B/5B/6B/7B/8B/9B

16-bit micro controller

## GENERAL DESCRIPTION

This LSI is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as 10-bit A/D converter, timer, PWM, synchronous serial port, UART, I2C bus interface (master), Low level detect circuit, are incorporated around 16-bit CPU nX-U16/100.

The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. and, this LSI has a data flash-memory fill area by a software which can be written in. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

## FEATURES

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time  
 Approx 30.5  $\mu$ s (at 32.768kHz system clock)  
 Approx 0.122  $\mu$ s (at 8.192MHz system clock)

- Internal memory
  - Flash-memory

Product	Program area	Rewrite cycle
ML620Q151B/ML620Q154B/ML620Q157B	32-Kbyte* (16K $\times$ 16-bit)	100
ML620Q152B/ML620Q155B/ML620Q158B	48-Kbyte* (24K $\times$ 16-bit)	
ML620Q153B/ML620Q156B/ML620Q159B	64-Kbyte* (32K $\times$ 16-bit)	

\* including unusable 1KByte TEST area

Internal 2-Kbyte Data Flash (1-Kbyte  $\times$  2) Rewrite cycle: 10,000 times

- SRAM: Internal 2-Kbyte RAM (2-Kbyte  $\times$  8 -bits)

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: BACK-UP CLOCK, WDT)
  - maskable interrupt

Product	Interrupt source
ML620Q151B/ML620Q154B/ML620Q157B	27 (Internal source: 20, External source: 7)
ML620Q152B/ML620Q155B/ML620Q158B	28 (Internal source: 20, External source: 8)
ML620Q153B/ML620Q156B/ML620Q159B	28 (Internal source: 20, External source: 8)

- 4 steps of interrupt level, and a mask function



- Time base counter
  - Low-speed time base counter × 1 channel
- Watchdog timer
  - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s @32.768kHz)
- Timers
  - 8 bits × 2ch (16-bits configuration available × 1ch)
  - 16 bits × 4ch
- PWM
  - 16bits × 4ch
  - The auto reload timer mode / PWM mode
  - Timer start-stop function by the software and an external trigger.
  - A pulse width can be measured using an external-trigger input.
  - An external event can be selected as the counter clock.
  - Complement synchronous PWM
- Synchronous serial port
  - 1ch
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
- UART
  - Full-duplex × 1ch ( Half-duplex × 2ch )
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator
- I<sup>2</sup>C bus interface
  - Master function only
  - Fast mode (400kbit/s), Standard mode (100kbit/s)
- Successive approximation type A/D converter
  - 10-bit A/D converter
  - Input: 12ch (Maximum)
  - Conversion time: 43 $\mu$ s, 13.5 $\mu$ s per channel (conversion-time is selectable)
- Analog Comparator
  - 1ch
  - Edge for the interrupt and sampling function is selectable.

- General-purpose ports (including secondary functions)

- Input-only ports

Product	Input-only ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151B/ML620Q152B/ML620Q153B	6ch	5ch
ML620Q154B/ML620Q155B/ML620Q156B	7ch	6ch
ML620Q157B/ML620Q158B/ML620Q159B	7ch	6ch

- Output-only ports : 4ch

- Input/output ports

Product	Input/output ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151B/ML620Q152B/ML620Q153B	31ch	30ch
ML620Q154B/ML620Q155B/ML620Q156B	34ch	33ch
ML620Q157B/ML620Q158B/ML620Q159B	46ch	45ch

- Reset

- Reset through the RESET\_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - Reset by the Low Level Detector (LLD)

- Low Level detect function

- Threshold voltages: 4values (1.9V/2.55V/3.7V/4.2V)  
A threshold voltage is selected as Code-Option.
  - LLD is a ready as a supply-voltage supervisory reset.  
Reset or an interrupt output is selectable as Code-Option.

- Clock

- Low-speed clock (This LSI can not guarantee the operation without low-speed clock)  
Crystal oscillation (32.768 kHz) or Built-in RC oscillation (32.768kHz)  
Crystal oscillation or Built-in RC oscillation is selectable as Code-Option.
  - High-speed clock  
Built-in RC oscillation (2.097MHz) or Built-in PLL oscillation (8.192MHz)

- Power management

- HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Operation of an intact functional block circuit is powered down. (register reset and clock stop)

- Package

Product	Package
ML620Q151B/ML620Q152B/ML620Q153B	48pinTQFP (P-TQFP48-0707-0.50-QK)
ML620Q154B/ML620Q155B/ML620Q156B	52pinTQFP (P-TQFP52-1010-0.65-TK)
ML620Q157B/ML620Q158B/ML620Q159B	64pinQFP (P-QFP64-1414-0.80-UK)
	64pinTQFP (P-TQFP64-1010-0.50-ZK6)

- Guaranteed operating range

- Operating temperature:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- Operating voltage:  $V_{\text{DD}} = 1.8\text{V}$  to  $5.5\text{V}$

The difference point of this LSI is shown below.

function	ML620Q151B/152B/153B	ML620Q154B/155B/156B	ML620Q157B/158B/159B
Shipment	48pinTQFP	52pinTQFP	64pinQFP/TQFP
flash capacity (program area)	32Kbyte(ML620Q151B) 48Kbyte(ML620Q152B) 52Kbyte(ML620Q153B)	32Kbyte(ML620Q154B) 48Kbyte(ML620Q155B) 52Kbyte(ML620Q156B)	32Kbyte(ML620Q157B) 48Kbyte(ML620Q158B) 52Kbyte(ML620Q159B)
maskable interrupt	27	28	28
Input-only port (At the case of crystal unused)	6	7	7
P05 port	–	Available	Available
Input/output port (At the case of crystal unused)	31	34	46
P36,P53,P64 ports	–	Available	Available
P37 port	–	–	Available
P50~P52 ports	–	–	Available
P65~P67 ports	–	–	Available
P70~P74 ports	–	–	Available

– :none

BLOCK DIAGRAM

Block Diagram of ML620Q151B/ML620Q152B/ML620Q153B(TQFP48)

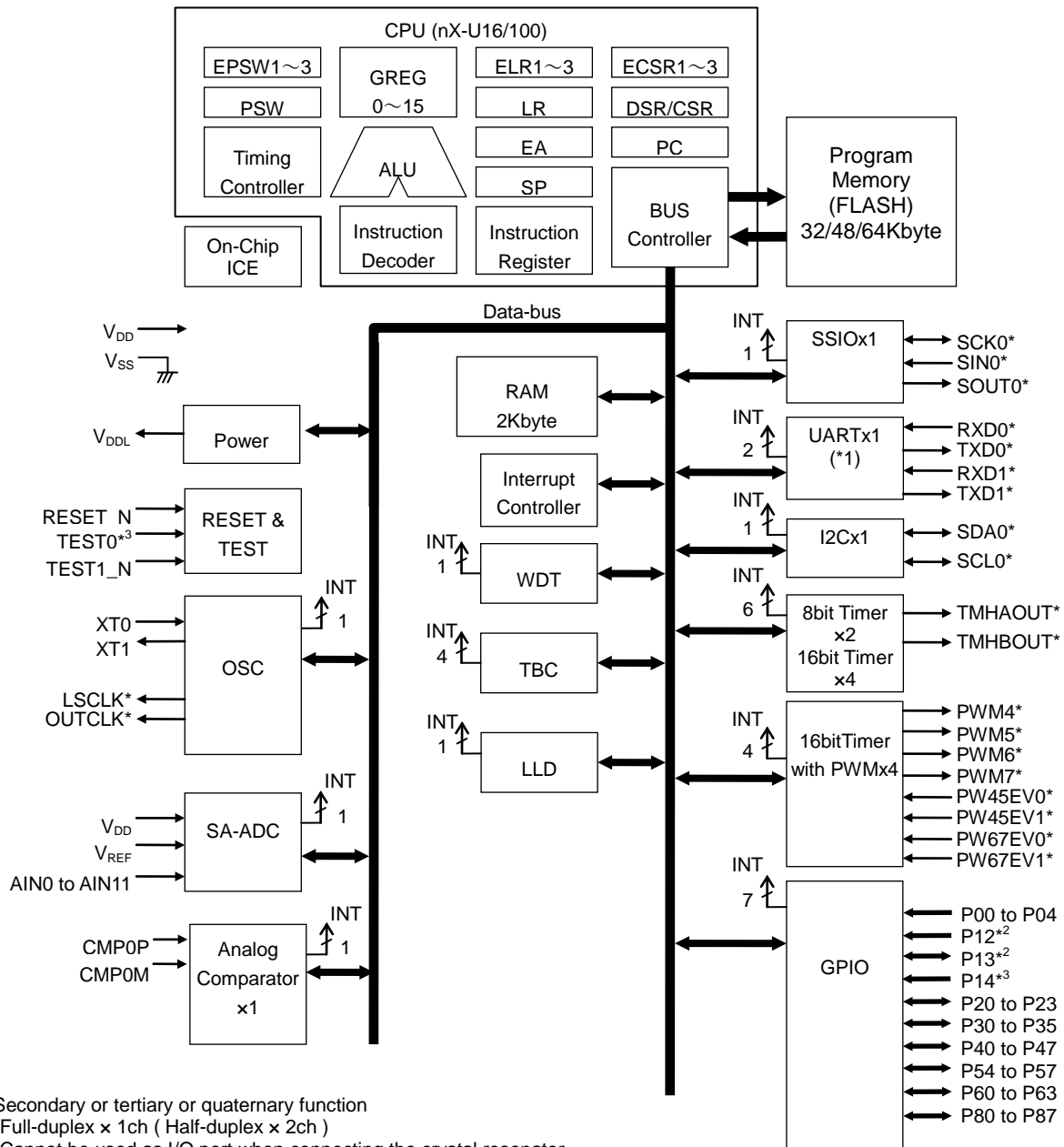
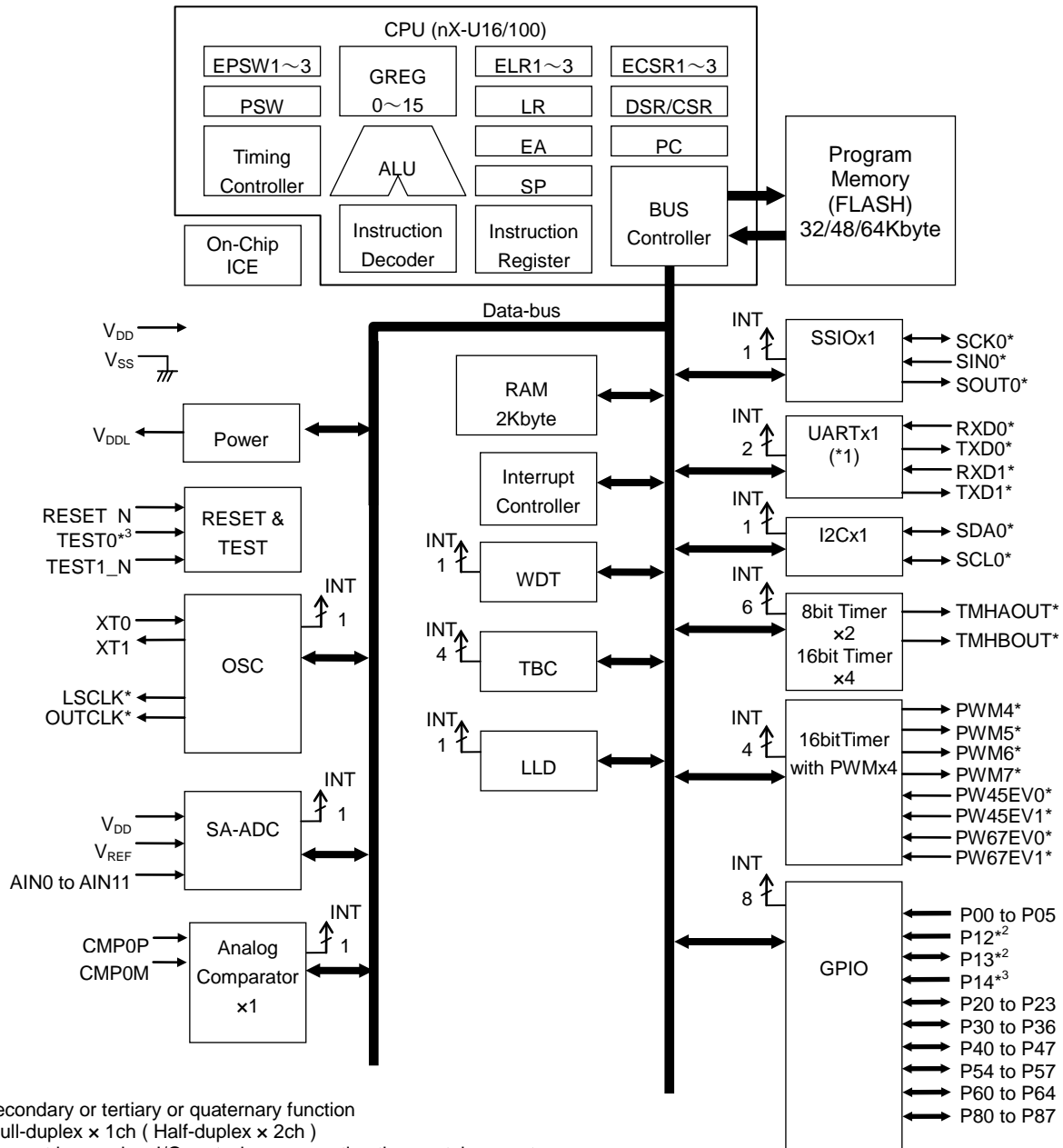


Figure 1-1 Block Diagram of ML620Q151B/ML620Q152B/ML620Q153B(TQFP48)

Block Diagram of ML620Q154B/ML620Q155B/ML620Q156B(TQFP52)



\* Secondary or tertiary or quaternary function

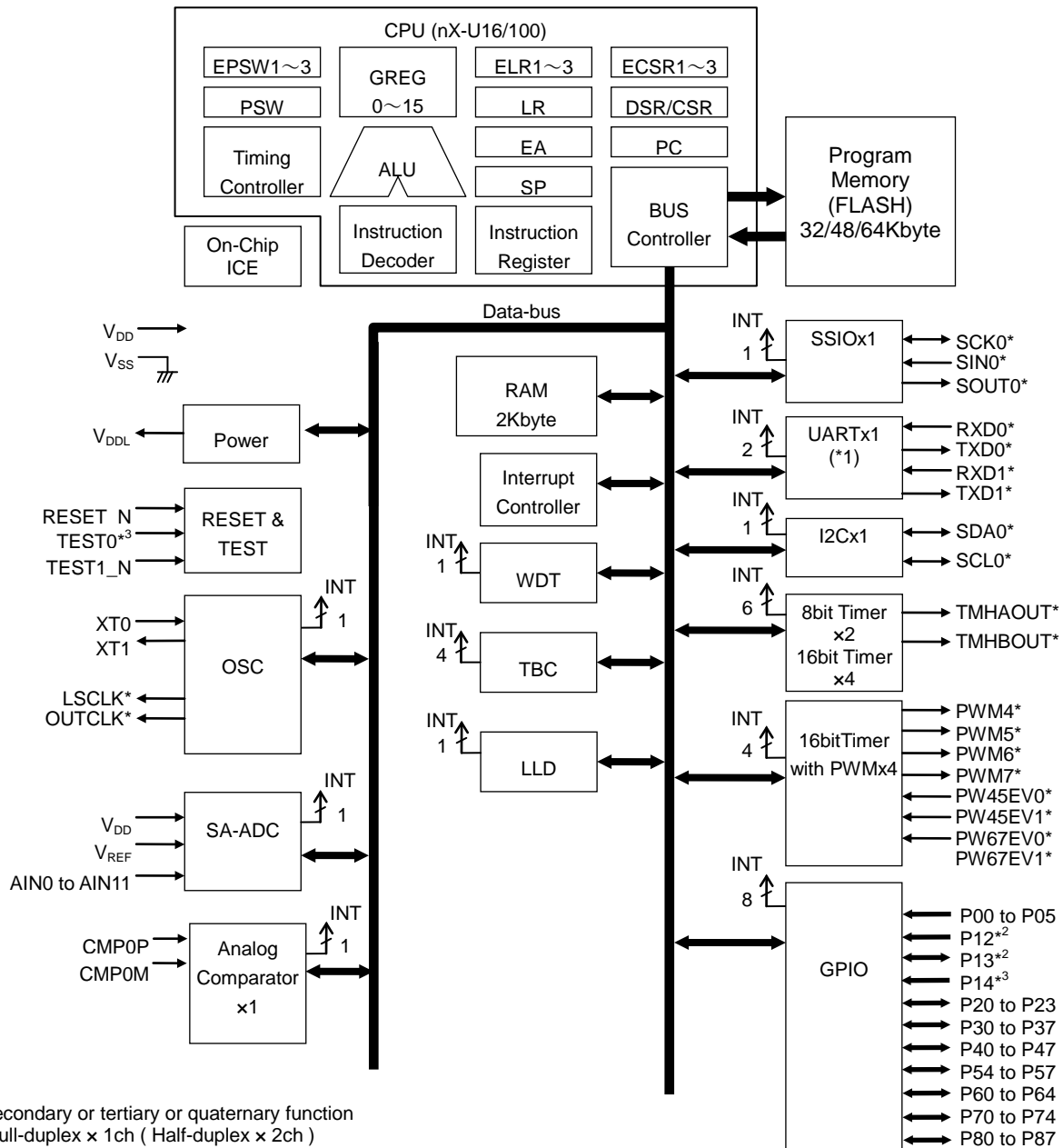
\*1 Full-duplex x 1ch ( Half-duplex x 2ch )

\*2 Cannot be used as I/O port when connecting the crystal resonator

\*3 Cannot be used as I/O port when connecting the uEASE(On-chip debug emulator)

Figure 1-2 Block Diagram of ML620Q154B/ML620Q155B/ML620Q156B(TQFP52)

Block Diagram of ML620Q157B/ML620Q158B/ML620Q159B(QFP64/TQFP64)



\* Secondary or tertiary or quaternary function

\*1 Full-duplex x 1ch ( Half-duplex x 2ch )

\*2 Cannot be used as I/O port when connecting the crystal resonator

\*3 Cannot be used as I/O port when connecting the uEASE(On-chip debug emulator)

Figure 1-3 Block Diagram of ML620Q157B/ML620Q158B/ML620Q159B(QFP64)

PIN CONFIGURATION

ML620Q151B/ML620Q152B/ML620Q153B TQFP48 package product

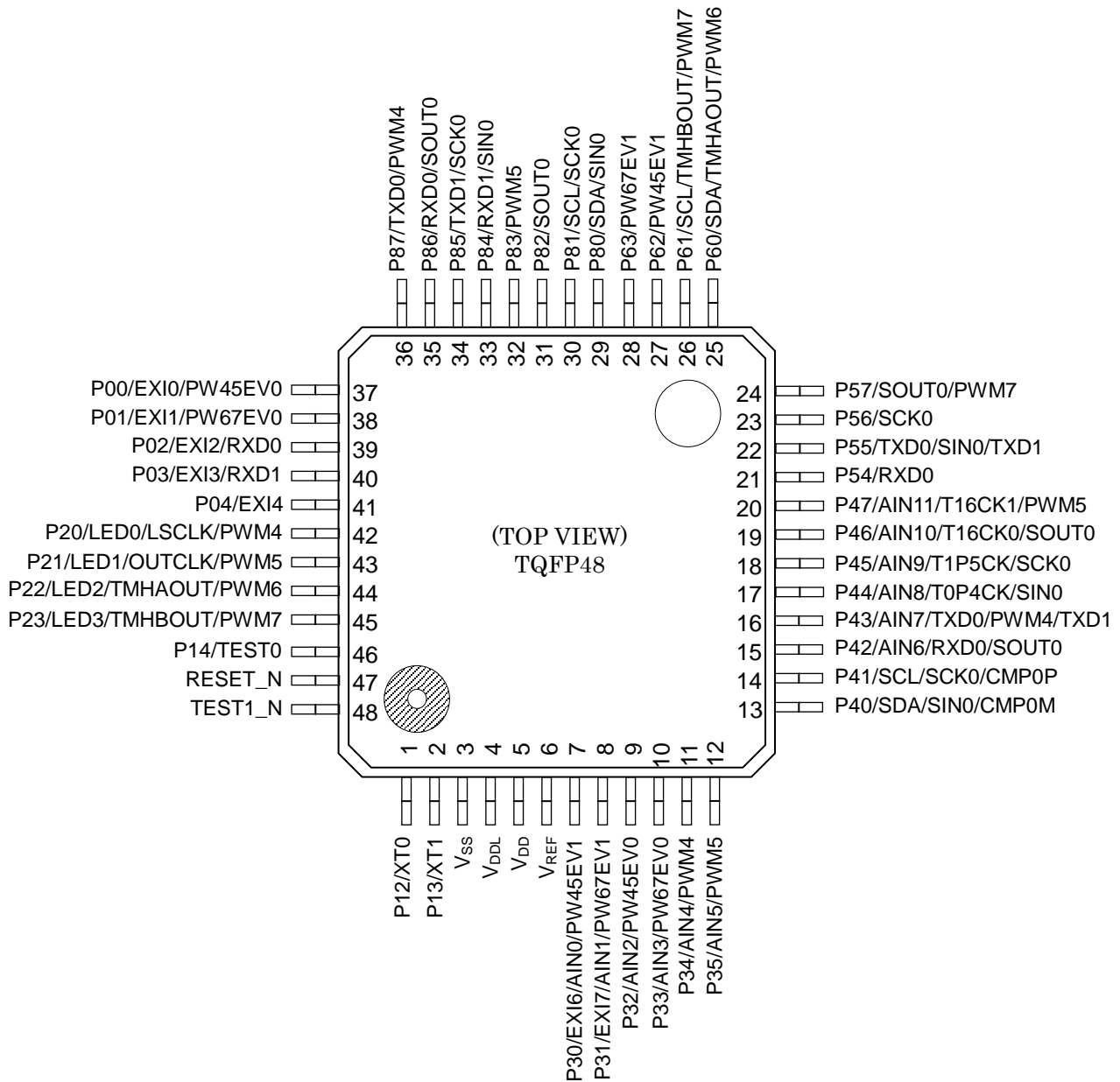


Figure 1-4 Pin Layout of ML620Q151B/ML620Q152B/ML620Q153B TQFP48 Package



ML620Q154B/ML620Q155B/ML620Q156B TQFP52 package product

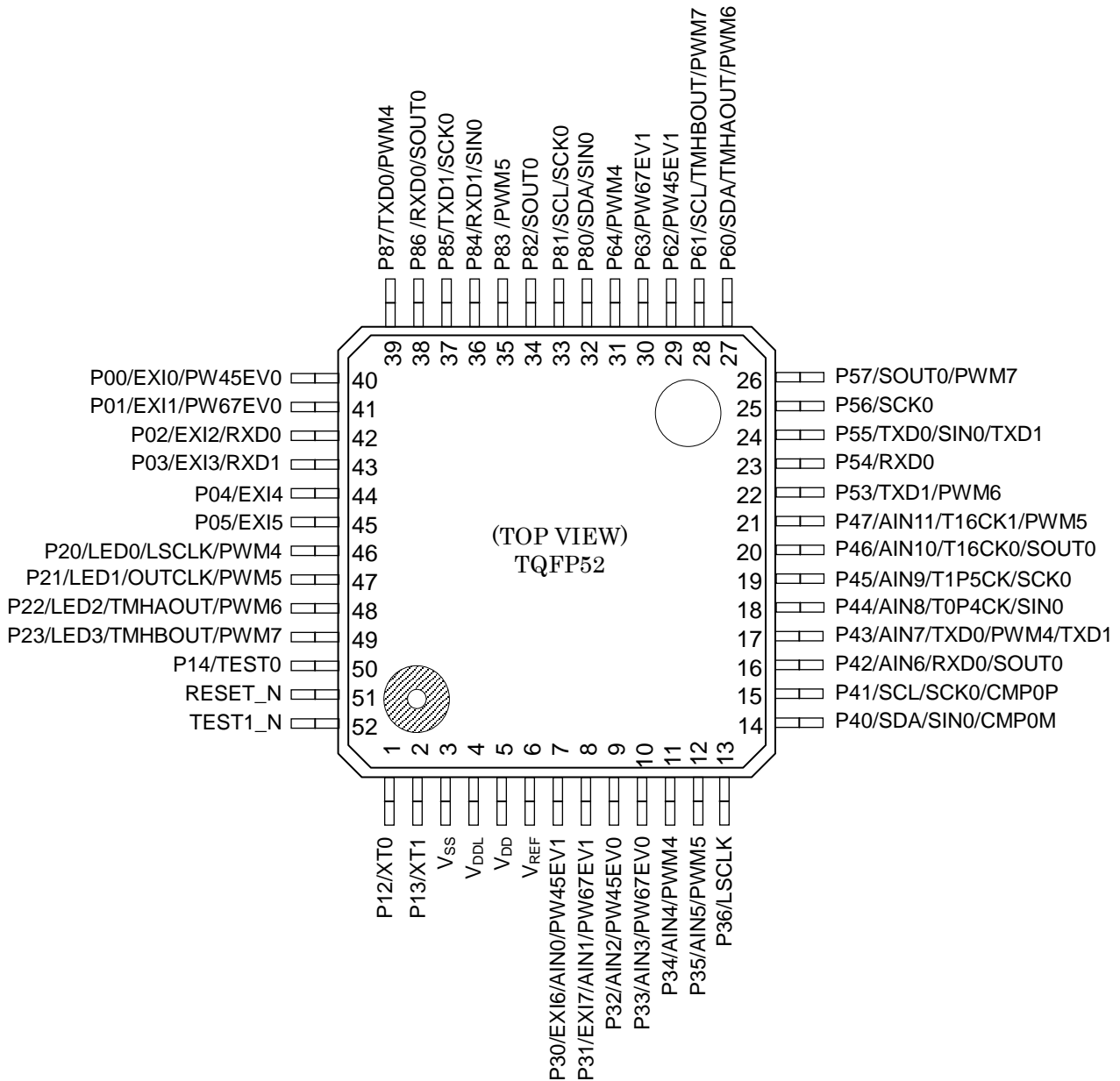


Figure 1-5 Pin Layout of ML620Q154B/ML620Q155B/ML620Q156B TQFP52 Package

ML620Q157B/ML620Q158B/ML620Q159B QFP64/TQFP64 package product

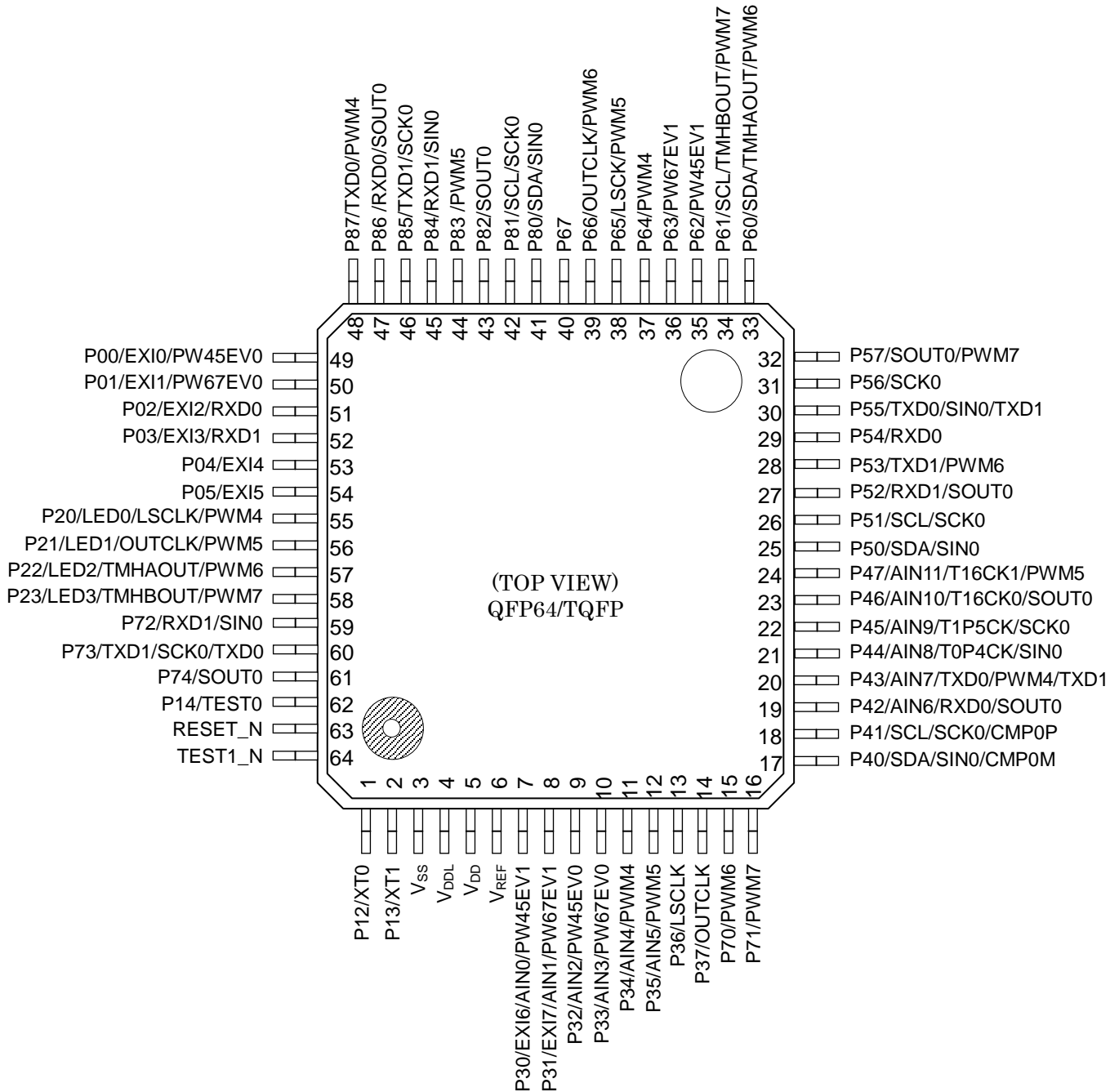


Figure 1-6 Pin Layout of ML620Q157B/ML620Q158B/ML620Q159B QFP64/TQFP Package

## List of Pins

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De- scription	Pin name	I/O	De- scription	Pin name	I/O	De- scription
3	3	3	V <sub>SS</sub>	—	Negative power supply pin	—	—	—	—	—	—	—	—	—
5	5	5	V <sub>DD</sub>	—	Positive power supply pin	—	—	—	—	—	—	—	—	—
4	4	4	V <sub>DDL</sub>	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—	—	—	—
46	50	62	P14/ TEST0	I	Input port/ Input pin for testing	—	—	—	—	—	—	—	—	—
47	51	63	RESET_N	I	Reset input pin	—	—	—	—	—	—	—	—	—
48	52	64	TEST1_N	I	Input pin for testing	—	—	—	—	—	—	—	—	—
1	1	1	P12/ XT0	I	Input port/ Low-speed clock oscillation pin	—	—	—	—	—	—	—	—	—
2	2	2	P13/ XT1	I/O	Input/output port/ Low-speed clock oscillation pin	—	—	—	—	—	—	—	—	—
6	6	6	V <sub>REF</sub>	—	Reference power supply pin of Successive-approximation type ADC	—	—	—	—	—	—	—	—	—
37	40	49	P00/EXI0/ PW45EV0	I	Input port / External interrupt / PW45EV0 input	—	—	—	—	—	—	—	—	—
38	41	50	P01/EXI1/ PW67EV0	I	Input port / External interrupt / PW67EV0 input	—	—	—	—	—	—	—	—	—
39	42	51	P02/EXI2/ RXD0	I	Input port / External interrupt UART0 data input	—	—	—	—	—	—	—	—	—
40	43	52	P03/EXI3/ RXD1	I	Input port / External interrupt UART1 data input	—	—	—	—	—	—	—	—	—
41	44	53	P04/EXI4	I	Input port / External interrupt	—	—	—	—	—	—	—	—	—
—	45	54	P05/EXI5	I	Input port / External interrupt	—	—	—	—	—	—	—	—	—
42	46	55	P20/ LED0/	O	Output port / LED drive	LSCLK	O	Low-speed clock output	PWM4	O	PWM4 output	—	—	—
43	47	56	P21/ LED1/	O	Output port / LED drive	OUTCLK	O	Low-speed clock output	PWM5	O	PWM5 output	—	—	—
44	48	57	P22/ LED2/	O	Output port / LED drive	—	—	—	TMHAOUT	O	TimerA output	PWM6	O	PWM6 output
45	49	58	P23/ LED3/	O	Output port / LED drive	—	—	—	TMHBOUT	O	TimerB output	PWM7	O	PWM7 output
7	7	7	P30/EXI6 PW45EV1 / AIN0	I/O	Input/output port / PW45EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
8	8	8	P31/EXI7 PW67EV1 / AIN1	I/O	Input/output port / PW67EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
9	9	9	P32/ PW45EV0 / AIN2	I/O	Input/output port / PW45EV0 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
10	10	10	P33/	I/O	Input/output port /	—	—	—	—	—	—	—	—	—

## ML620Q151B/2B/3B/4B/5B/6B/7B/8B/9B

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De- scription	Pin name	I/O	De- scription	Pin name	I/O	De- scription
			PW67EV0 / AIN3		PW67EV0 input / Successive approximation type ADC input									
11	11	11	P34/ AIN4/	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM4	O	PWM4 output	—	—	—
12	12	12	P35/ AIN5/	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output	—	—	—
—	13	13	P36	I/O	Input/output port	LSCL K	O	Low-spe ed clock output	—	—	—	—	—	—
—	—	14	P37	I/O	Input/output port	OUTC LK	O	Low-spe ed clock output	—	—	—	—	—	—
13	14	17	P40/ CMP0M	I/O	Input/output port / Comparator0 inverting input	SDA	I/O	I <sup>2</sup> C data input/out put	SIN0	I	SSIO0 data input	—	—	—
14	15	18	P41/ CMP0P	I/O	Input/output port / Comparator0 non-inverting input	SCL	I/O	I <sup>2</sup> C clock input/out put	SCK0	I/O	SSIO0 synchro nous clock input/out put	—	—	—
15	16	19	P42/ AIN6	I/O	Input/output port / Successive approximation type ADC input	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
16	17	20	P43/ AIN7	I/O	Input/output port / Successive approximation type ADC input	TXD0	O	UART0 data output	PWM4	O	PWM4 output	TXD1	O	UART1 data output
17	18	21	P44/ TOP4CK/ AIN8	I/O	Input/output port / PWM4 external clock input/ Successive approximation type ADC input	—	—	—	SIN0	I	SSIO0 data input	—	—	—
18	19	22	P45/ T1P5CK/ AIN9	I/O	Input/output port / PWM5 external clock input/ Successive approximation type ADC input	—	—	—	SCK0	I/O	SSIO0 synchro nous clock input/out put	—	—	—
19	20	23	P46/ T16CK0/ AIN10	I/O	Input/output port / Timer8,A / PWM6 external clock input / Successive approximation type ADC input	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
20	21	24	P47/ T16CK1/ AIN11	I/O	Input/output port / Timer9,B / PWM7 external clock input / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output	—	—	—
—	—	25	P50	I/O	Input/output port	SDA	I/O	I <sup>2</sup> C data input/out put	SIN0	I	SSIO0 data input			
—	—	26	P51	I/O	Input/output port	SCL	I/O	I <sup>2</sup> C clock input/out put	SCK0	I/O	SSIO0 synchro nous clock input/out put			

## ML620Q151B/2B/3B/4B/5B/6B/7B/8B/9B

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De- scription	Pin name	I/O	De- scription	Pin name	I/O	De- scription
—	—	27	P52	I/O	Input/output port	RXD1	I	UART1 data input	SOUT0	O	SSIO0 data output			
—	22	28	P53	I/O	Input/output port	TXD1	O	UART1 data output	PWM6	O	PWM6 output	—	—	—
21	23	29	P54	I/O	Input/output port	RXD0	I	UART0 data input	—	—	—	—	—	—
22	24	30	P55	I/O	Input/output port	TXD0	O	UART0 data output	SIN0	I	SSIO0 data input	TXD1	O	UART1 data output
23	25	31	P56	I/O	Input/output port	—	—	—	SCK0	I/O	SSIO0 synchro nous clock input/out put	—	—	—
24	26	32	P57	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	PWM7	O	PWM7 output
25	27	33	P60	I/O	Input/output port	SDA	I/O	I <sup>2</sup> C data input/out put	TMHAO UT	O	TimerA output	PWM6	O	PWM6 output
26	28	34	P61	I/O	Input/output port	SCL	I/O	I <sup>2</sup> C clock input/out put	TMHBO UT	O	TimerB output	PWM7	O	PWM7 output
27	29	35	P62/ PW45EV1	I/O	Input/output port / PW45EV1 input	—	—	—	—	—	—	—	—	—
28	30	36	P63/ PW67EV1	I/O	Input/output port / PW67EV1 input	—	—	—	—	—	—	—	—	—
—	31	37	P64	I/O	Input/output port	—	—	—	PWM4	O	PWM4 output	—	—	—
—	—	38	P65	I/O	Input/output port	LCLK	O	Low-spe ed clock output	PWM5	O	PWM5 output	—	—	—
—	—	39	P66	I/O	Input/output port	OUT LK	O	Low-spe ed clock output	PWM6	O	PWM6 output	—	—	—
—	—	40	P67	I/O	Input/output port	—	—	—	—	—	—	—	—	—
—	—	15	P70	I/O	Input/output port	—	—	—	PWM6	O	PWM6 output	—	—	—
—	—	16	P71	I/O	Input/output port	—	—	—	PWM7	O	PWM7 output	—	—	—
—	—	59	P72	I/O	Input/output port	RXD1	I	UART1 data input	SIN0	I	SSIO0 data input	—	—	—
—	—	60	P73	I/O	Input/output port	TXD1	O	UART1 data output	SCK0	I/O	SSIO0 synchro nous clock input/out put	TXD0	O	UART0 data output
—	—	61	P74	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
29	32	41	P80	I/O	Input/output port	SDA	I/O	I <sup>2</sup> C data input/out put	SIN0	I	SSIO0 data input	—	—	—
30	33	42	P81	I/O	Input/output port	SCL	I/O	I <sup>2</sup> C clock input/out put	SCK0	I/O	SSIO0 synchro nous clock input/out put	—	—	—
31	34	43	P82	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	—	—	—

## ML620Q151B/2B/3B/4B/5B/6B/7B/8B/9B

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De- scription	Pin name	I/O	De- scription	Pin name	I/O	De- scription
32	35	44	P83	I/O	Input/output port	—	—	—	PWM5	O	PWM5 output	—	—	—
33	36	45	P84	I/O	Input/output port	RXD1	I	UART1 data input	SIN0	I	SSIO0 data input	—	—	—
34	37	46	P85	I/O	Input/output port	TXD1	O	UART1 data output	SCK0	I/O	SSIO0 synchro nous clock input/out put	—	—	—
35	38	47	P86	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
36	39	48	P87	I/O	Input/output port	TXD0	O	UART0 data output	PWM4	O	PWM4 output	—	—	—

## PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
Power supply				
V <sub>SS</sub>	—	Negative power supply pin	—	—
V <sub>DD</sub>	—	Positive power supply pin	—	—
V <sub>DDL</sub>	—	Positive power supply pin for internal logic (internally generated). Connect capacitors (C <sub>L</sub> ) (see Measuring Circuit 1) between this pin and V <sub>SS</sub> .	—	—
Test				
TEST0	I	Input/output pin for testing.	—	Positive
TEST1_N	I	Input/output pin for testing. This pin has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a “H” level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V <sub>SS</sub> as required.	—	—
XT1	O		—	—
LSCLK*	O	Low-speed clock output. This function is allocated to the secondary function of the P20/P36/P65 pin.	Secondary	—
OUTCLK*	O	High-speed clock output. This function is allocated to the secondary function of the P21/P37/P66 pin.	Secondary	—
General-purpose input port				
P00 to P05*	I	General-purpose input or output ports.	Primary	Positive
P12	I			
P13	I/O			
P14	I			
General-purpose output port				
P20 to P23	O	General-purpose output ports. Provided with a secondary or tertiary or quaternary function for each port. Cannot be used as ports if their secondary functions or tertiary or quaternary are used.	Secondary/ Tertiary/ Quaternary	Positive
General-purpose input/output port				
P30 to P37*	I/O	General-purpose output ports. Provided with a secondary or tertiary or quaternary function for each port. Cannot be used as ports if their secondary functions or tertiary or quaternary are used.	Secondary/ Tertiary/ Quaternary	Positive
P40 to P47				
P50 to P57*				
P60 to P67*				
P70 to P74*				
P80 to P87				

\*:ML620Q151B/ML620Q152B/ML620Q153B/ML620Q154B/ML620Q155B/ML620Q156B/ML620Q157B/ML620Q158B/ ML620Q159B have a different pin configuration for each package. See “LIST OF PINS” for more details.

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
UART				
TXD0*	O	UART0 data output pin. Allocated to the secondary function of the P43, P55, P87 and the fourthly function of the P73.	Secondary Quaternary	Positive
RXD0*	I	UART0 data input pin. Allocated to the secondary function of the P02, P42, P54 and P86.	Secondary	Positive
TXD1*	O	UART1 data output pin. Allocated to the secondary function of the P53, P73, P85, and the fourthly function of the P43, P55.	Secondary Quaternary	Positive
RXD1*	I	UART1 data input pin. Allocated to the secondary function of the P03, P52, P72 and P84.	Secondary	Positive
I <sup>2</sup> C bus interface				
SDA*	I/O	I <sup>2</sup> C data input/output pin. This pin is used as the secondary function of the P40, P50, P60 and P80. This pin has an NMOS open drain output. When using this pin as a function of the I <sup>2</sup> C, externally connect a pull-up resistor.	Secondary	Positive
SCL*	I/O	I <sup>2</sup> C clock output pin. This pin is used as the secondary function of the P41, P51, P61 and P81. This pin has an NMOS open drain output. When using this pin as a function of the I <sup>2</sup> C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0*	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40, P44, P50, P55, P72, P80 and P84.	Tertiary	Positive
SCK0*	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41, P45, P51, P56, P73, P81 and P85.	Tertiary	—
SOUT0*	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42, P46, P52, P57, P74, P82 and P86.	Tertiary	Positive
PWM				
PWM4*	O	PWM4 output pin. Allocated to the tertiary function of the P34, P43, P64 and P87.	Tertiary	Positive
PWM5*	O	PWM5 output pin. Allocated to the tertiary function of the P35, P47, P65 and P83.	Tertiary	Positive
PWM6*	O	PWM6 output pin. Allocated to the tertiary function of the P53, P66, P70 and fourthly function of the P22 and P60.	Tertiary Quaternary	Positive
PWM7*	O	PWM7 output pin. Allocated to the tertiary function of the P71 and fourthly function of the P23, P57, and P61.	Tertiary Quaternary	Positive
PW45EV0 PW45EV1	I	Control start /stop/clear for PWM4 and PWM5. Allocated to the primary function of the P00, P30, P32 and P62.	Primary	—
PW67EV0 PW67EV1	I	Control start /stop/clear pin for PWM6 and PWM7. Allocated to the primary function of the P01, P31, P33, and P63.	Primary	—
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—

\*:ML620Q151B/ML620Q152B/ML620Q153B/ML620Q154B/ML620Q155B/ML620Q156B/ML620Q157B/ML620Q158B/ ML620Q159B have a different pin configuration for each package. See "LIST OF PINS" for more details.



**ML620Q151B/2B/3B/4B/5B/6B/7B/8B/9B**

Pin name	I/O	Description	Primary/ Secondary	Logic
External interrupt				
EXI0~7*	I	External maskable interrupt input pins. The interrupt is enabled and interrupt edge is selectable by the software for each bit. Allocated to the primary function of the P00 to P05 and P30 to P31.	Primary	Positive/ Negative
Timer				
T16CK0	I	External clock input pin for 16bit timer 8, timer A and PWM6. Allocated to the primary function of the P46 pin.	Primary	—
T16CK1	I	External clock input pin for 16bit timer 9, timer B and PWM7. Allocated to the primary function of the P47 pin.	Primary	—
TMHAOUT	O	16bit timer A output pin. Allocated to the tertiary function of the P22 andn P60.	Tertiary	Positive
TMHBOUT	O	16bit timer B output pin. Allocated to the tertiary function of the P23 and P61.	Tertiary	Positive
LED drive				
LED0 to LED3	O	Pins for LED driving. Allocated to the primary function of the P20 to P23 pins.	Primary	Positive/ Negative
Successive-approximation type A/D converter				
V <sub>REF</sub>	I	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0 to AIN11	I	Analog inputs to Ch0–Ch11 of the successive-approximation type A/D converter. Allocated to the secondary function of the P30 to P35 and P42 to P47 pins.	—	—
Analog Comparator				
CMP0P	I	Non-inverting input for comparator0. This pin is used as the primary function of the P41 pin.	—	—
CMP0M	I	Inverting input for comparator0. This pin is used as the primary function of the P40 pin.	—	—

\*:ML620Q151B/ML620Q152B/ML620Q153B/ML620Q154B/ML620Q155B/ML620Q156B/ML620Q157B/ML620Q158B/ ML620Q159B have a different pin configuration for each package. See "LIST OF PINS" for more details.

**TERMINATION OF UNUSED PINS**

## How to Terminate Unused Pins

Pin	Recommended pin termination
RESET_N	open
P14/TEST0	open
TEST1_N	open
V <sub>REF</sub>	Connect to V <sub>DD</sub>
P00 to P05* <sup>1</sup>	Connect V <sub>DD</sub> or V <sub>SS</sub>
P12* <sup>2</sup>	Connect V <sub>DD</sub> or V <sub>SS</sub>
P13* <sup>2</sup>	open
P20 to P23	open
P30 to P37* <sup>1</sup>	open
P40 to P47	open
P50 to P57* <sup>1</sup>	open
P60 to P67* <sup>1</sup>	open
P70 to P74* <sup>1</sup>	open
P80 to P87	open

\*<sup>1</sup>: ML620Q151B/ML620Q152B/ML620Q153B/ML620Q154B/ML620Q155B/ML620Q156B/ML620Q157B/ML620Q158B/ ML620Q159B have a different pin configuration for each package. See "LIST OF PINS" for more details.

\*<sup>2</sup>: Handling in the case a crystal resonator is not connected.

**Note:**

For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

## ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V <sub>DD</sub>	Ta = 25°C	-0.3 to +6.5	V
Power supply voltage 2	V <sub>DDL</sub>	Ta = 25°C	-0.3 to +2.0	V
Reference voltage	V <sub>REF</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Analog input voltage	V <sub>AI</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Input voltage	V <sub>IN</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>OUT</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Output current 1	I <sub>OUT1</sub>	Port3,4,5,6,7,8 Ta = 25°C	-12 to +11	mA
Output current 2 (P20 to P23)	I <sub>OUT2</sub>	Port2 Ta = 25°C When N-channel open drain output is selected	-12 to +20	mA
Power dissipation	PD	Ta = 25°C	1	W
Storage temperature	T <sub>STG</sub>	—	-55 to +150	°C

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T <sub>OP</sub>	—	-40 to +105	°C
Operating voltage	V <sub>DD</sub>	—	1.8 to 5.5	V
Reference voltage	V <sub>REF</sub>	—	1.8 to V <sub>DD</sub>	V
Analog input voltage	V <sub>AI</sub>	—	V <sub>SS</sub> to V <sub>REF</sub>	V
Operating frequency (CPU)	f <sub>OP</sub>	—	30k to 8.4M	Hz
Low-speed crystal oscillation frequency	f <sub>XTL</sub>	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C <sub>DL</sub>	Use 32.768KHz Crystal Oscillator DT-26 (DAISHINKU CORP.)	12 to 25	pF
	C <sub>GL</sub>		12 to 25	
Capacitor externally connected to V <sub>DD</sub> pin	C <sub>V</sub>	—	2.2±30% or more	μF
Capacitor externally connected to V <sub>DDL</sub> pin	C <sub>L</sub>	—	2.2±30%	μF

## Flash Memory Operating Conditions

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Condition	Range	Unit	
Operating temperature	T <sub>OP</sub>	Data flash memory, At write/erase	-40 to +105	°C	
		Flash ROM, At write/erase	0 to +40		
Operating voltage	V <sub>DD</sub>	At write/erase	1.8 to 5.5	V	
Maximum rewrite count *1	C <sub>EPD</sub>	Data Flash	10,000	times	
	C <sub>EPP</sub>	Program Flash	100		
Erase unit	—	Chip erase	All area	—	
	—	Block erase	Program Flash	8	KB
			Data Flash	2	KB
	—	Sector erase (Data Flash only)	1	KB	
Erase time	—	Chip erase, Block erase, Sector erase	100	ms	
Write unit	—	—	1 word (2 Bytes)	—	
Write time (Max.)	—	1 word (2 Bytes)	40	μs	
Data retention period	Y <sub>DR</sub>	—	15	years	

\*1: One rewrite cycle includes both one time erase and one time write, it counts as one even if the erase is aborted.

## DC Characteristics (IDD)

(V<sub>DD</sub>=1.8 to 5.5V, V<sub>SS</sub>=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit	
Supply current 1	IDD1	CPU is in STOP state. Low-speed/high-speed oscillation is stopped. V <sub>DD</sub> =3.0V	-40 to +35°C	—	1.0	6	μA	1
			-40 to +105°C	—	1.0	22		
Supply current 2	IDD2	Crystal Oscillating. CPU is in HALT state (LTBC,WBC: Operating <sup>*1</sup> ). High-speed oscillation is stopped. V <sub>DD</sub> =3.0V	-40 to +35°C	—	2.5	7		
			-40 to +105°C	—	2.5	24		
			Internal RC Oscillating. CPU is in HALT state (LTBC,WBC: Operating <sup>*1</sup> ). High-speed oscillation is stopped. V <sub>DD</sub> =3.0V	-40 to +35°C	—	3.5		
-40 to +105°C	—	3.5		26				
Supply current 3	IDD3	CPU: Running at 32kHz <sup>*2</sup> High-speed oscillation is stopped. V <sub>DD</sub> =3.0V	-40 to +35°C	—	13	20		
			-40 to +105°C	—	13	42		
Supply current 4	IDD4	CPU: Running at 2MHz RC oscillating mode <sup>*2</sup> V <sub>DD</sub> =5.0V	—	0.64	2.0	mA		
Supply current 5	IDD5	CPU: Running at 8.192MHz PLL oscillating mode <sup>*2</sup> V <sub>DD</sub> =5.0V	—	5	8			

\*1: Significant bits of BLKCON0, BLKCON2 to BLKCON4, BLKCON6 and BLKCON7 registers are all "1".

\*2: Case when the CPU operating rate is 100% (with no HALT state)

## ML620Q151B/2B/3B/4B/5B/6B/7B/8B/9B

## DC Characteristics (VOHL, IOHL)

(V<sub>DD</sub>=1.8 to 5.5V, V<sub>SS</sub>=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P23) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	VOH1	IOH1 = -0.5mA 1 pin output		V <sub>DD</sub> -0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA 1 pin output		—	—	0.5		
Output voltage 2 (P20-P23)	VOL2	When N-channel open drain output is selected	IOL2 = +10mA V <sub>DD</sub> ≥ 5.0V 1 pin output	—	—	0.5	V	2
			IOL2 = +8mA V <sub>DD</sub> ≥ 3.0V 1 pin output	—	—	0.5		
Output voltage 3 (P40 to P41) (P50 to P51)* (P60 to P61)* (P80 to P81)	VOL3	When I <sup>2</sup> C mode is selected	IOL3 = +3mA V <sub>DD</sub> ≥ 2.0V 1 pin output	—	—	0.4	V	2
			IOL3 = +2mA 2.0V > V <sub>DD</sub> ≥ 1.8V 1 pin output	—	—	V <sub>DD</sub> * 0.2		
Output leakage current (P20 to P23) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	IOOH	VOH = V <sub>DD</sub> (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V <sub>SS</sub> (in high-impedance state)		-1	—	—		

\*:ML620Q151B/ML620Q152B/ML620Q153B/ML620Q154B/ML620Q155B/ML620Q156B/ML620Q157B/  
ML620Q158B/ ML620Q159B have a different pin configuration for each package. See "LIST OF PINS" for more details.

## DC Characteristics (IIHL)

(V<sub>DD</sub>=1.8 to 5.5V, V<sub>SS</sub>=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V <sub>DD</sub>		0	—	1	μA	4
	IIL1	VIL1 = V <sub>SS</sub>		-1500	-300	-20		
Input current 2 (P00 to P05)* (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	IIH2	VIH2 = V <sub>DD</sub> (when pulled down)		2	30	250	μA	4
	IIL2	VIL2 = V <sub>SS</sub> (when pulled up)		-250	-30	-2		
	IIH2Z	VIH2 = V <sub>DD</sub> (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V <sub>SS</sub> (in high-impedance state)		-1	—	—		

\*:ML620Q151B/ML620Q152B/ML620Q153B/ML620Q154B/ML620Q155B/ML620Q156B/ML620Q157B/  
ML620Q158B/ ML620Q159B have a different pin configuration for each package. See "LIST OF PINS" for more details.

## DC Characteristics (VIHL)

(V<sub>DD</sub>=1.8 to 5.5V, V<sub>SS</sub>=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (P14/TEST0) (TEST1_N) (P00 to P05)* (P12, P13) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	VIH1	—	0.7× V <sub>DD</sub>	—	V <sub>DD</sub>	V	5
	VIL1	—	0	—	0.3× V <sub>DD</sub>		
Input pin capacitance (RESET_N) (P14/TEST0) (TEST1_N) (P00 to P05)* (P12, P13) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	CIN	f = 10kHz V <sub>rms</sub> = 50mV Ta = 25°C	—	—	10	pF	—

\*:ML620Q151B/ML620Q152B/ML620Q153B/ML620Q154B/ML620Q155B/ML620Q156B/ML620Q157B/  
ML620Q158B/ ML620Q159B have a different pin configuration for each package. See "LIST OF PINS" for more details.

## DC Characteristics (LLD)

(V<sub>DD</sub>=2.2 to 5.5V, V<sub>SS</sub>=0V, Ta=-40 to +105°C, unless otherwise specified)

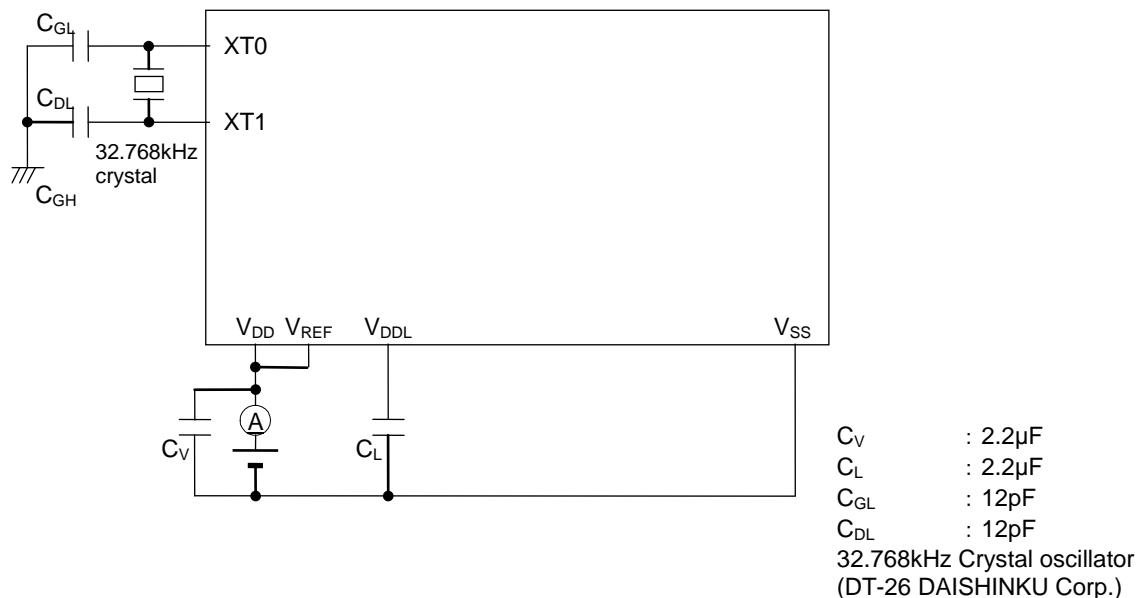
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
LLD threshold voltage	V <sub>D-</sub>	LD1 to 0 = 0H	When power rising	1.85	1.98	2.1	V	1
			When power falling	1.8	1.9	2		
	LD1 to 0 = 1H	When power rising	2.5	2.63	2.75			
		When power falling	2.45	2.55	2.65			
	V <sub>D+</sub>	LD1 to 0 = 2H	When power rising	3.65	3.78	3.9		
			When power falling	3.6	3.7	3.8		
LD1 to 0 = 3H	When power rising	4.15	4.28	4.4				
	When power falling	4.1	4.2	4.3				
Hysteresis	V <sub>hys</sub>	—	—	—	80	—	mV	mA

## DC Characteristics (Analog Comparator)

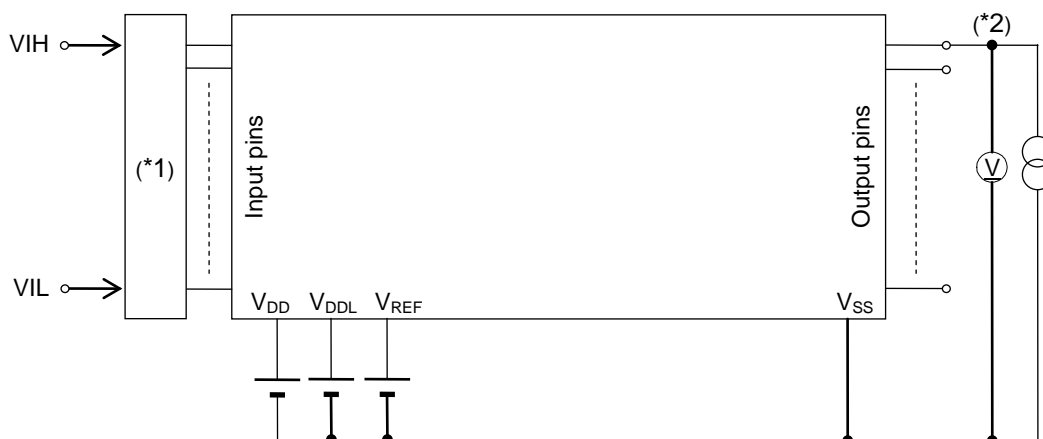
(V<sub>DD</sub>=2.2 to 5.5V, V<sub>SS</sub>=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Common mode Input voltage	CMPnM V <sub>IN</sub>	—	0	—	V <sub>DD</sub> -1.4	V	1
	CMPnP V <sub>IN</sub>	—	0	—	V <sub>DD</sub>		
Input offset voltage	V <sub>CMPOF</sub>	—	—	5	100	mV	
Response time	T <sub>CMP</sub>	CMPnP = CMPnM ± 100mV	—	—	1	μS	

Measuring circuit 1



Measuring circuit 2

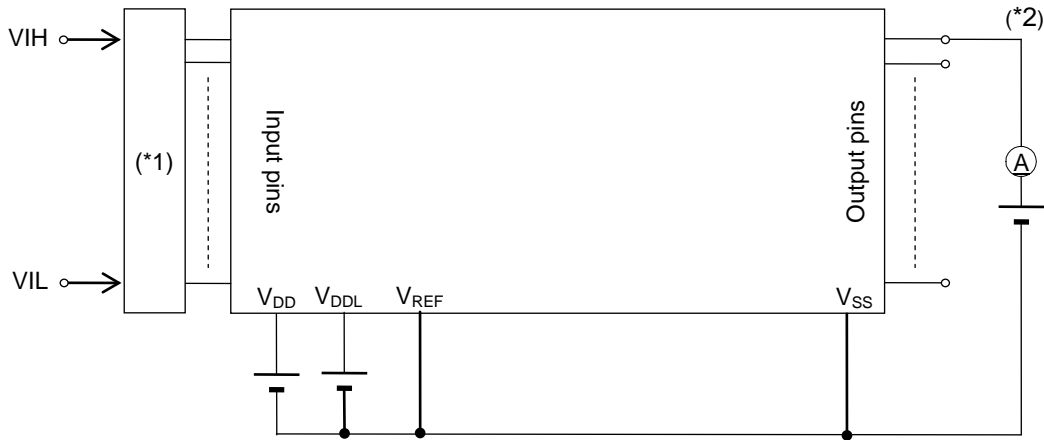


(\*1) Input logic circuit to determine the specified measuring conditions.

(\*2) Measured at the specified output pins.

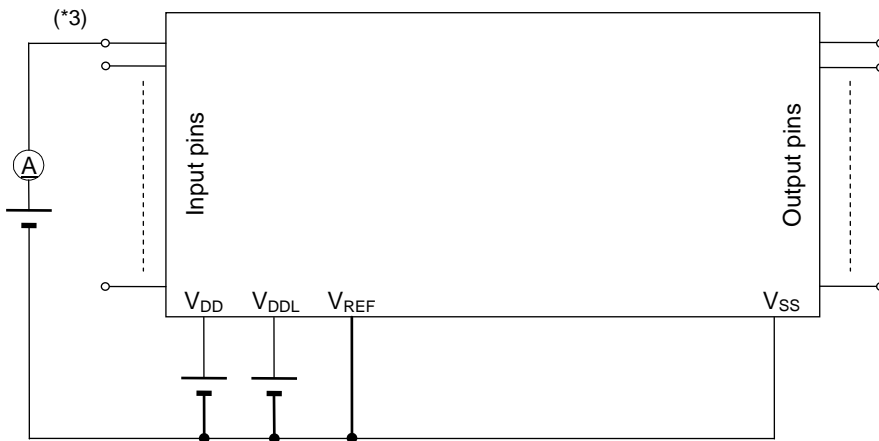


Measuring circuit 3



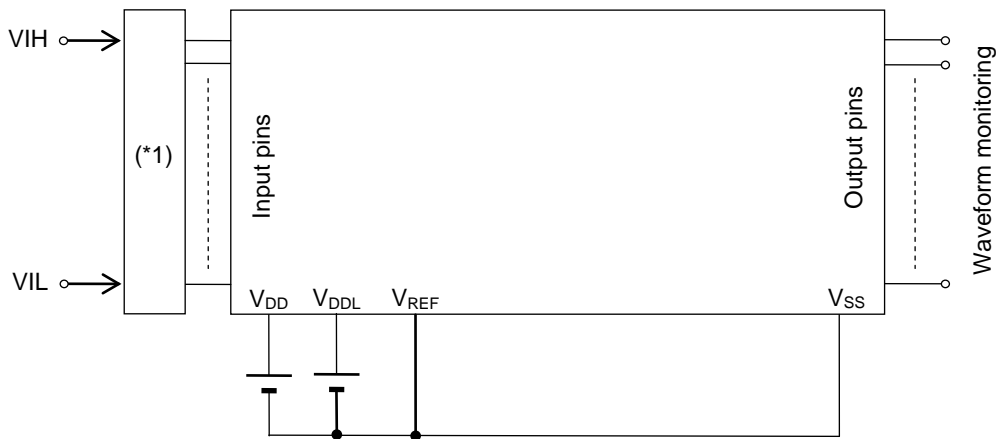
(\*1) Input logic circuit to determine the specified measuring conditions.  
 (\*2) Measured at the specified output pins.

Measuring circuit 4



\*3: Measured at the specified input pins.

Measuring circuit 5



\*1: Input logic circuit to determine the specified measuring conditions.

**AC Characteristics (Oscillation Circuit)**

( $V_{DD}=1.8$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed crystal oscillation start time*1	$T_{XTL}$	—	—	0.6	2	s	1
Low-speed RC oscillator frequency	$f_{LCR}$	$T_a=+25^{\circ}C$	Typ -1%	32.768k	Typ +1%	Hz	
		$T_a=-40$ to $85^{\circ}C$	Typ -2.5%	32.768k	Typ +2.5%	Hz	
		$T_a=-40$ to $105^{\circ}C$	Typ -3%	32.768k	Typ +3%	Hz	
High-speed RC oscillator frequency	$f_{HCR}$	$T_a=+25^{\circ}C$	Typ -5%	2.097	Typ +5%	MHz	
		$T_a=-40^{\circ}C$ to $+105^{\circ}C$	Typ -15%	2.097	Typ +15%	MHz	
PLL oscillation frequency	$f_{PLL}$	LSCLK=32.768kHz 2,048 clock average	Typ -1%	8.192	Typ +1%	MHz	

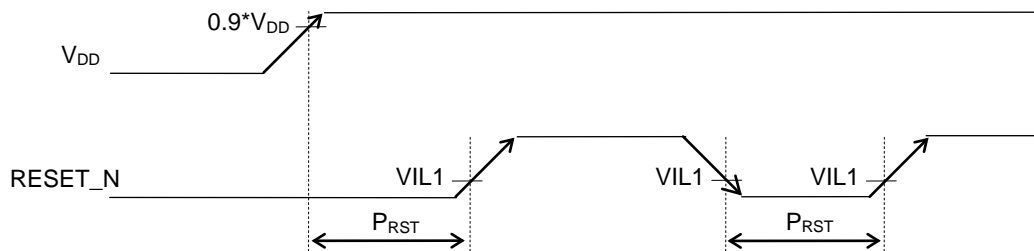
\*1: Use 32.768KHz Crystal Oscillator DT-26 (Daishinku) with capacitance  $C_{GL}/C_{DL}=12pF$ .

**AC Characteristics (Power On Reset Sequence)**

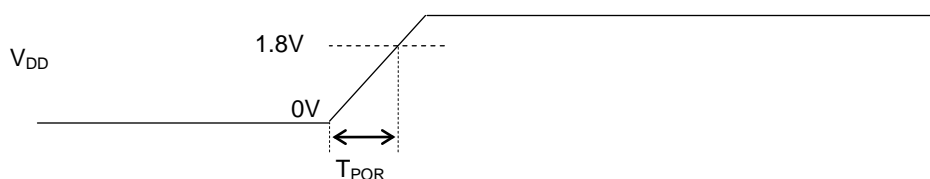
( $V_{DD}=1.8$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Reset pulse width	$P_{RST}$	—	100	—	—	$\mu s$	1
Reset noise rejection pulse width	$P_{NRST}$	—	—	—	0.4		
Power On Reset rising time	$T_{POR}$	—	—	—	10	ms	

**When using RESET\_N pin**



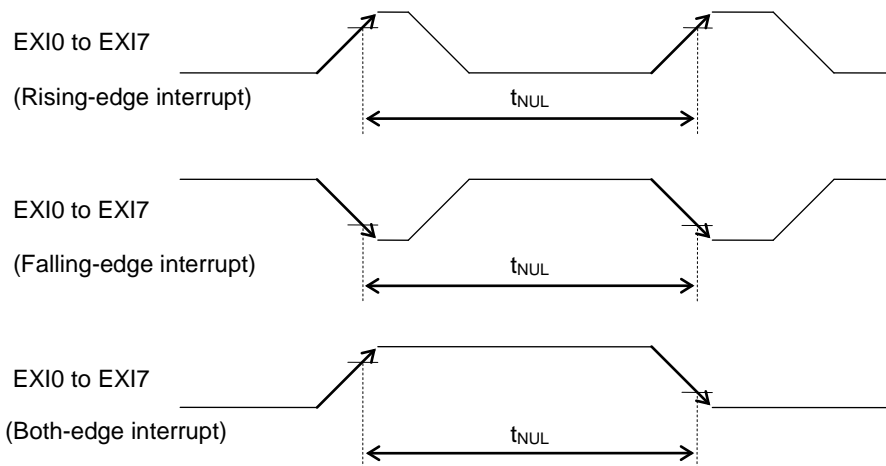
**When using power on reset**



AC Characteristics (External Interrupt)

( $V_{DD}=1.8$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	$T_{NUL}$	Interrupt: Enabled (MIE = 1), CPU: NOP operation	$2.5 \times$ LSCLK	—	$3.5 \times$ LSCLK	$\mu s$

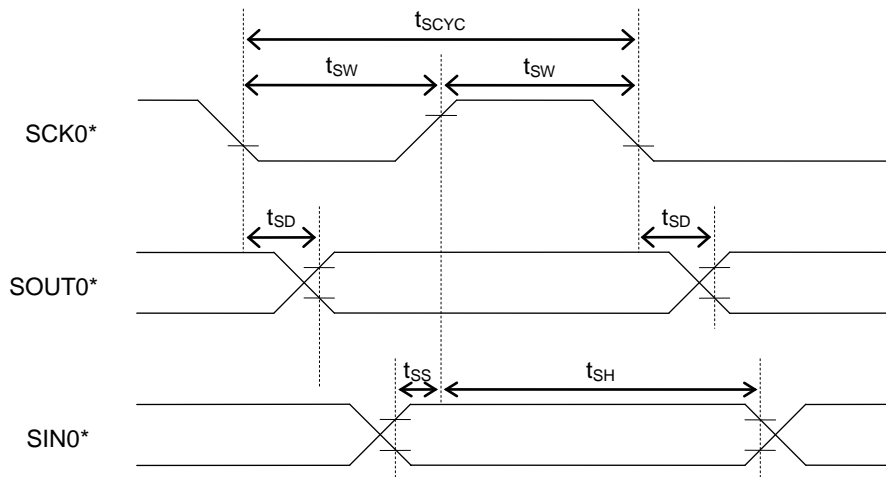


AC Characteristics (Synchronous Serial Port)

( $V_{DD}=1.8$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	$t_{SCYC}$	High-speed oscillation stopped	10	—	—	$\mu s$
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	$t_{SCYC}$	—	—	$SCK^{(*)}$	—	sec
SCK input pulse width (slave mode)	$t_{SW}$	High-speed oscillation stopped	4	—	—	$\mu s$
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	$t_{SW}$	—	$SCK^{(*)} \times 0.4$	$SCK^{(*)} \times 0.5$	$SCK^{(*)} \times 0.6$	sec
SOUT output delay time (slave mode)	$t_{SD}$	—	—	—	180	ns
SOUT output delay time (master mode)	$t_{SD}$	—	—	—	80	ns
SIN input setup time (slave mode)	$t_{SS}$	—	80	—	—	ns
SIN input setup time (Master mode)	$t_{SS}$	—	240	—	—	ns
SIN input hold time	$t_{SH}$	—	80	—	—	ns

\*1: Clock period selected by SnCK3–0 of the serial port n mode register (SIO nMOD1)



\*: Indicates the secondary function of the corresponding port.

**AC Characteristics (I2C Bus Interface: Standard Mode 100kHz)**

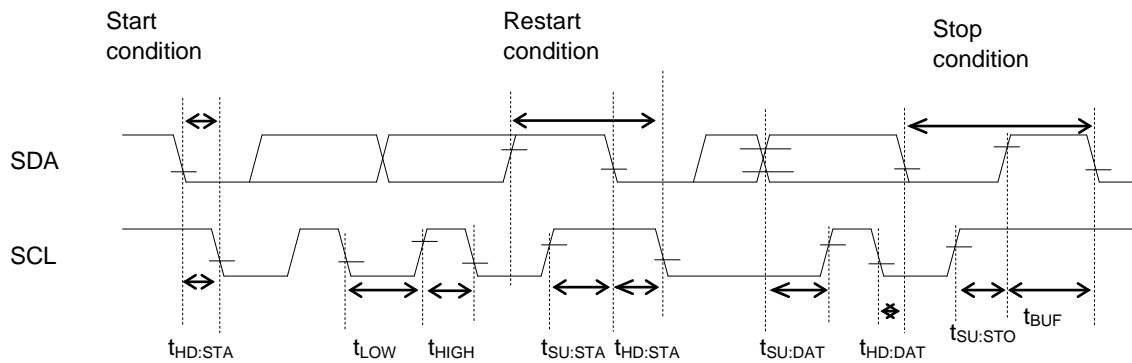
( $V_{DD}=1.8$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	$f_{SCL}$	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	$\mu s$
SCL "L" level time	$t_{LOW}$	—	4.7	—	—	$\mu s$
SCL "H" level time	$t_{HIGH}$	—	4.0	—	—	$\mu s$
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	$\mu s$
SDA hold time	$t_{HD:DAT}$	—	0	—	—	$\mu s$
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	$\mu s$
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	$\mu s$
Bus-free time	$t_{BUF}$	—	4.7	—	—	$\mu s$

**AC Characteristics (I2C Bus Interface: Fast Mode 400kHz)**

( $V_{DD}=1.8$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	$f_{SCL}$	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	$\mu s$
SCL "L" level time	$t_{LOW}$	—	1.3	—	—	$\mu s$
SCL "H" level time	$t_{HIGH}$	—	0.6	—	—	$\mu s$
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	$\mu s$
SDA hold time	$t_{HD:DAT}$	—	0	—	—	$\mu s$
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	$\mu s$
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	$\mu s$
Bus-free time	$t_{BUF}$	—	1.3	—	—	$\mu s$

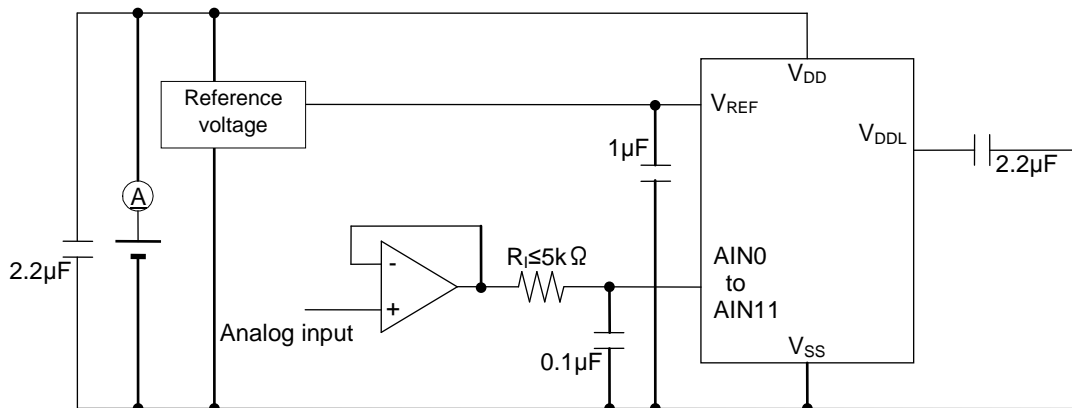


Characteristics of Successive Approximation Type A/D Converter

( $V_{DD}=1.8$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$ , unless otherwise specified)

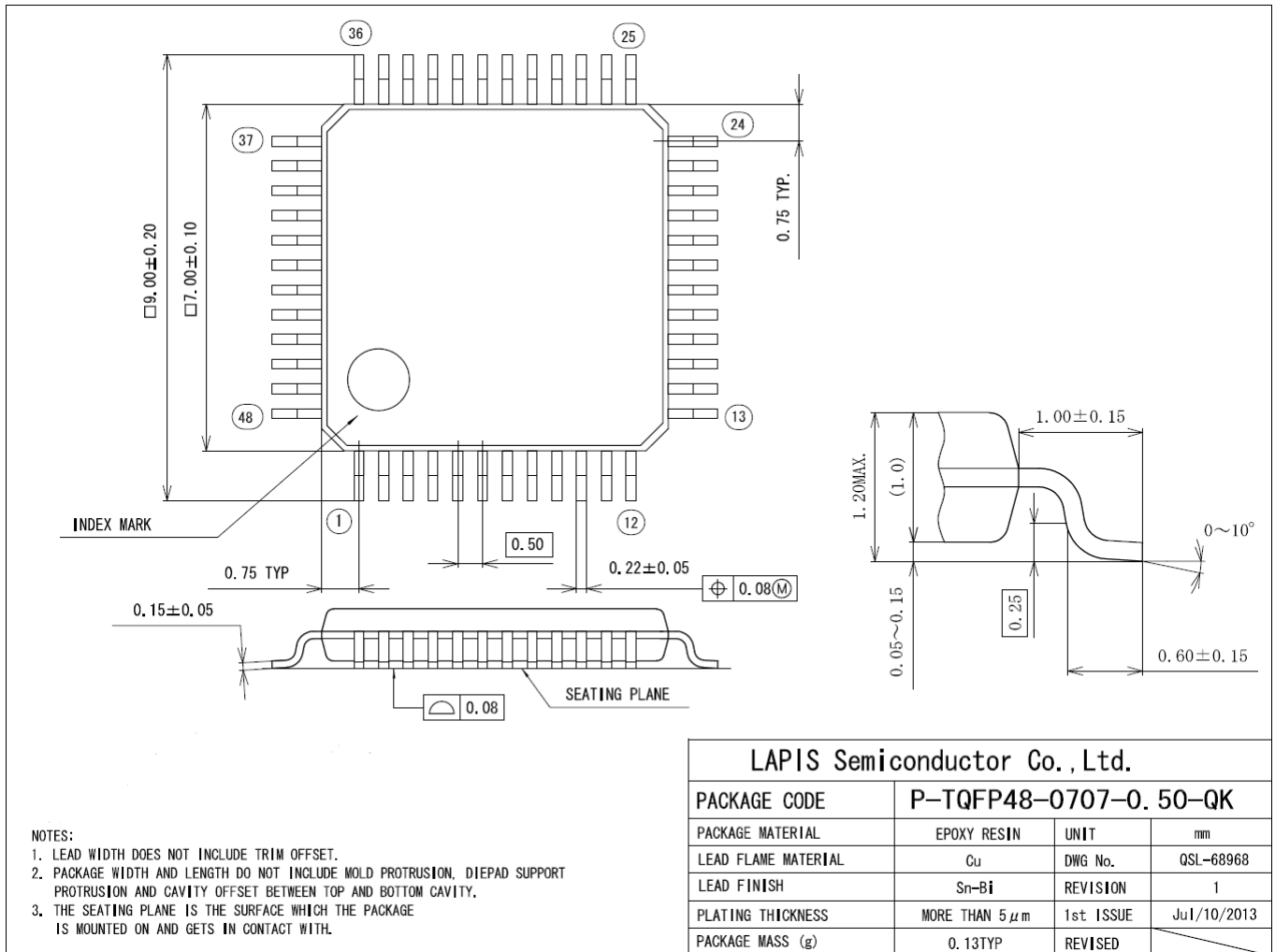
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
Resolution	n	—	—	—	10	bits	
Integral non-linearity error	INL	$2.7V \leq V_{REF} \leq 5.5V$	-4	—	+4	LSB	
		$2.2V \leq V_{REF} < 2.7V$	-6	—	+6		
		$1.8V \leq V_{REF} < 2.2V$ SACK bit *1 = 1	-10	—	+10		
Differential non-linearity error	DNL	$2.7V \leq V_{REF} \leq 5.5V$	-3	—	+3	LSB	
		$2.2V \leq V_{REF} < 2.7V$	-5	—	+5		
		$1.8V \leq V_{REF} < 2.2V$ SACK bit *1 = 1	-9	—	+9		
Zero-scale error	$V_{OFF}$	$R_I \leq 5k\Omega$	-6	—	+6		
Full-scale error	FSE	$R_I \leq 5k\Omega$	-6	—	+6		
Input impedance	$R_I$	—	—	—	5k	$\Omega$	
A/D operating voltage	$V_{REF}$	$V_{REF} \leq V_{DD}$	2.7	—	5.5	V	
Conversion time	$t_{CONV}$	PLL oscillation mode	SACK bit *1 = 0	—	13.5	—	$\mu s$
			SACK bit *1 = 1	—	43	—	
		High-speed RC oscillation mode	SACK bit *1 = 0	—	16	—	
			SACK bit *1 = 1	—	44	—	

\*1: Bit 1 of SA-ADC control register 0 (SADCON0)



PACKAGE DIMENSIONS

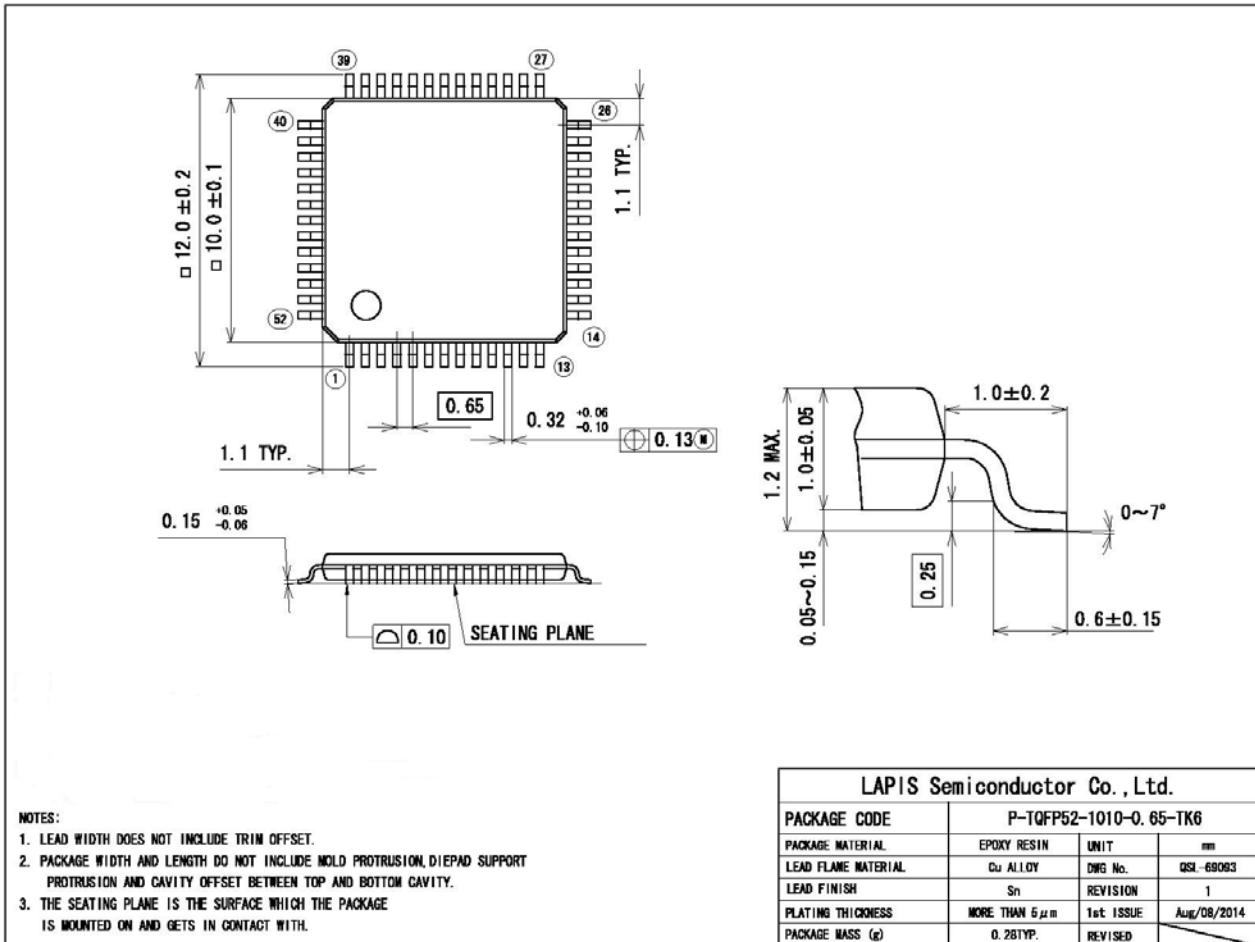
ML620Q151B/ML620Q152B/ML620Q153B Package Dimension (48pin TQFP)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML620Q154B/ML620Q155B/ML620Q156B Package Dimension (52pin TQFP)



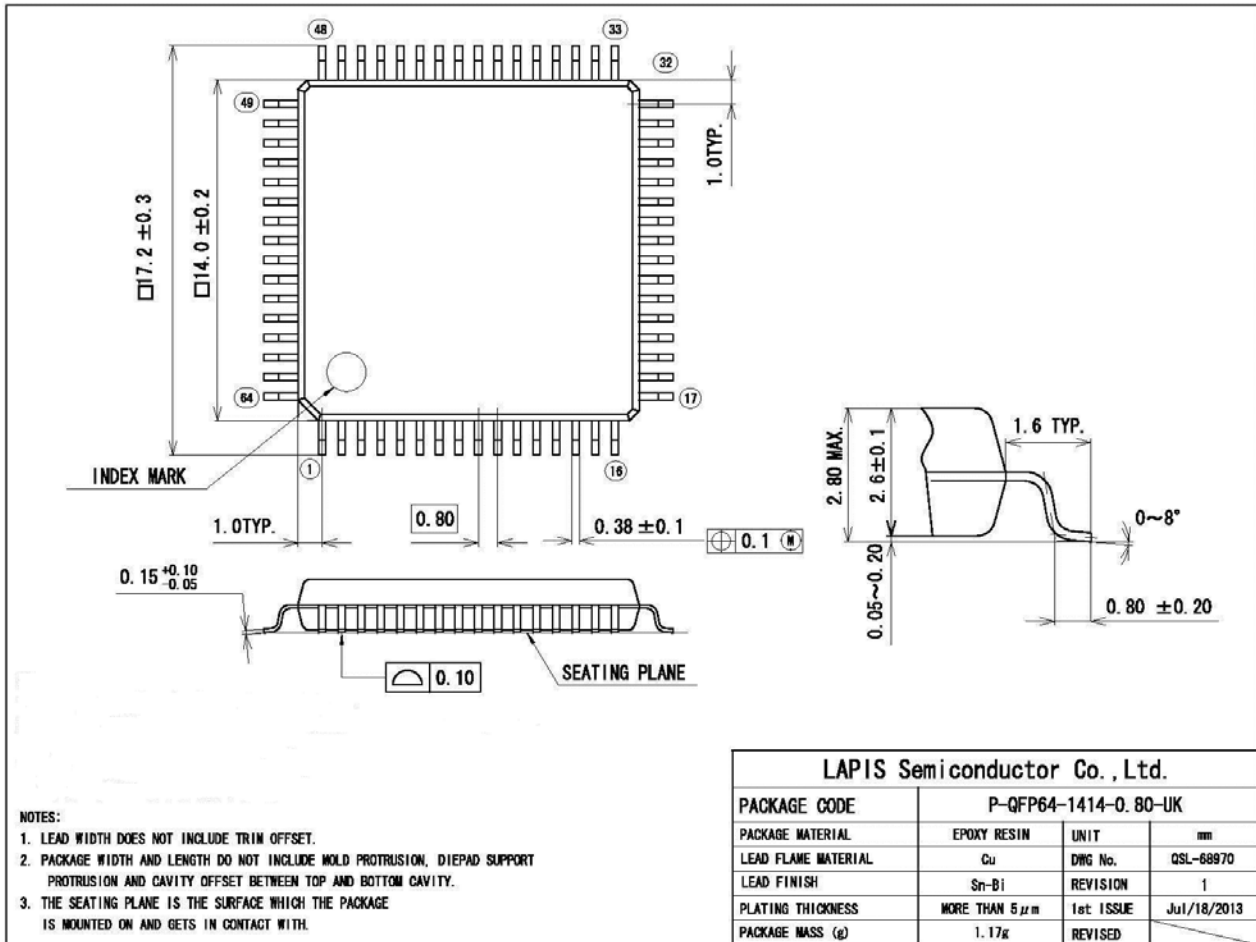
- NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
  2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
  3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



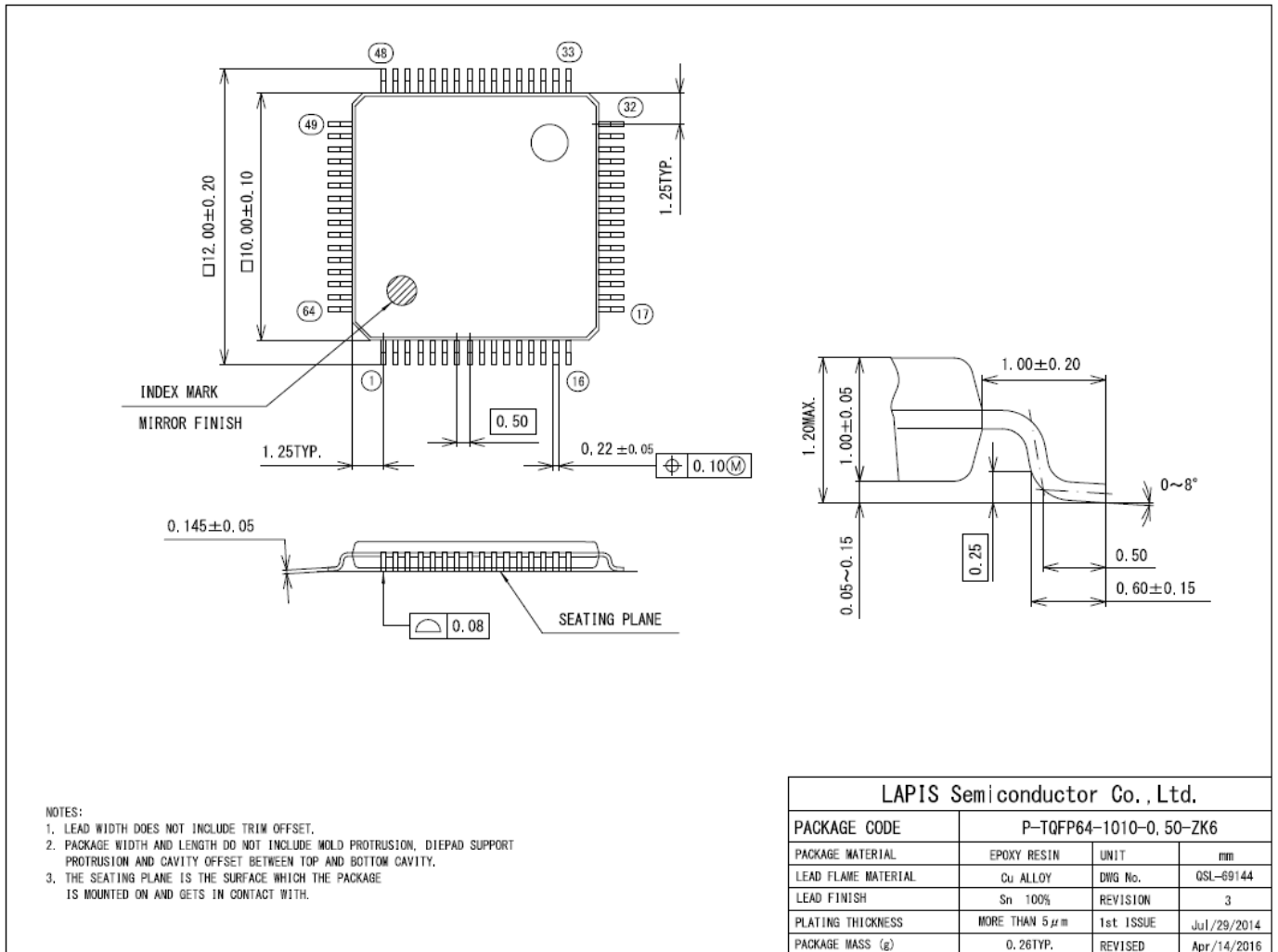
ML620Q157B/ML620Q158B/ML620Q159B Package Dimension (64pin QFP)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML620Q157B/ML620Q158B/ML620Q159B Package Dimension (64pin TQFP)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL620Q150B-01	Mar 30, 2017	-	-	First Edition

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