Discontinued Product

8. Sep, 1998
ML63326

PRELIMINARY

OKI Semiconductor

# ML63326

4-Bit Microcontroller with built-in Voice Synthesis and 1024-Dot LCD Drivers

## GENERAL DESCRIPTION

The ML63326 is a low power 4-bit microcontroller which incorporates the OKI original CPU core nX-4/250 and provides a minimum instruction execution time of 1µs (@2MHz).
It contains 24K-word program memory, 1536-nibble data memory, 4-bit input port, four 4-bit output ports, five 4-bit and 2-bit input-output ports, shift register, LCD driver for up to 1024 segments, and voice synthesis, including 1 megabit mask ROM for speech data, a 12-bit D/A converter and low-pass filter internally. Speech ROM size can be expanded externally with further 4 megabits. The ML63326 is suitable for applications such as games, toys, clocks etc. which use an LCD display and voice synthesis.

## FEATURES

- Rich instruction set

  439 instructions
  Transfer, rotate, increment, decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, branch, conditional branch, call/return, control.
- Rich selection of addressing modes

  Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
  Data memory bank internal direct addressing mode.
- Processing speed

  Two clocks per machine cycle, with most instructions executed in one machine cycle.
  Minimum instruction execution time : 61µs ( @32.768kHz system clock )
  1µs ( @2MHz system clock: 1/2 of high-speed clock )
- Clock generation circuit

  Low-speed clock: : 32.768kHz crystal oscillator,
  or 32kHz ±40% (@1MΩ±10%), RC oscillator (by mask option)
  High-speed clock: : 4MHz (max.) crystal oscillator,
  or 2MHz ±40% (@20kΩ±5%) RC oscillator (by software selection)
- Program memory space

  24K words
  Basic instruction length is 16 bits / 1 word
- Data memory space

  1536 nibbles
- External data memory space

  64kbyte ( expandable )
- Stack level

  Call stack level : 16 levels
  Register stack level : 16 levels

- I/O ports

  Input ports: Selectable as input with pull-up resistance/ input with pull-down resistor / high-impedance input
  Output ports: Selectable as P-channel open drain output / N-channel open drain output / CMOS output / high-impedance output
  Input-output ports: Selectable as input with pull-up resistance / input with pull-down resistance / high-impedance input
  Selectable as P-channel open drain output / N-channel open drain output / CMOS output / high-impedance output
  Can be interfaced with external peripherals that use a different power supply than this device uses.
  Number of ports:
  Input ports : 1 port × 4 bits
  Output port : 4 ports × 4 its
  Input-output port : 5 ports × 4 bits and 1 port × 2 bits

- Voice synthesis

  Algorithm : 4-bit ADPCM / Oki non-linear 8-bit PCM / 8-bit PCM
  Voice synthesis data memory:
  Internal ROM : 1 Mbit mask ROM (128k bytes)
  External ROM : 4 Mbit ROM (512k bytes max.)
  Sampling frequencies (at clock frequency 4.096MHz)
  4.0kHz, 5.3kHz, 6.4kHz, 8.0kHz, 10.7kHz, 12.8kHz, 16.0kHz
  12-bit D/A converter
  Low-pass filter

- Melody output function

  Two systems (one is in voice synthesis portion, the other is in microcontoroller portion)
  MD, MDB output ports are selected from two systems
  Melody output in voice synthesis portion can put out to AOUT/AOUTB output ports

- LCD driver

  Number of segments : 1024 Max. (64SEG × 16COM)
  1/1 to 1/16 duty
  1/4 or 1/5 bias (regulator built-in)
  Selectable as all-on mode/ all-off mode/ power down mode/ normal display mode
  Adjustable contrast

- Reset function

  Reset through RESET pin
  Power-on reset
  Reset to low-speed oscillation halt

- Battery check

  Low-voltage supply check
  Criterion voltage : Can be selected as 2.40 ±0.20V

- Timers and Counters

  8-bit timer × 4
  Selectable to auto-reload mode/ capture mode/ clock frequency measurement mode
  Watchdog timer × 1
  100Hz timer × 1
  15-bit time-base counter × 1
  1, 2, 4, 8, 16, 32, 64, and 128Hz signals can be read

- Shift register

  Shift clock : 1 × or 1/2 × system clock, external clock
  Data length : 8 bits

- Interrupt sources

  External interrupt : 3
  Internal interrupt : 12 (watchdog timer × 1, time base × 4, 100Hz timer × 1, timer × 4, shift-register x 1, melody × 1), (watchdog timer interrupt is a nonmaskable interrupt )

- Operating voltage

  +2.0 to 5.5V

- Package

  Chip : ( Product name : ML63326 - xxx )
  xxx indicates a code number.

  Chip size : TBA
  Chip thickness : 350 µm (typ.)

  Fig.1 shows PAD layout image.
  Minimum pad pitch : xxx µm (a)
  Bonding pad size : 100µm × 100µm (b × c)
  Pad size : 110µm × 110µm (d × e)

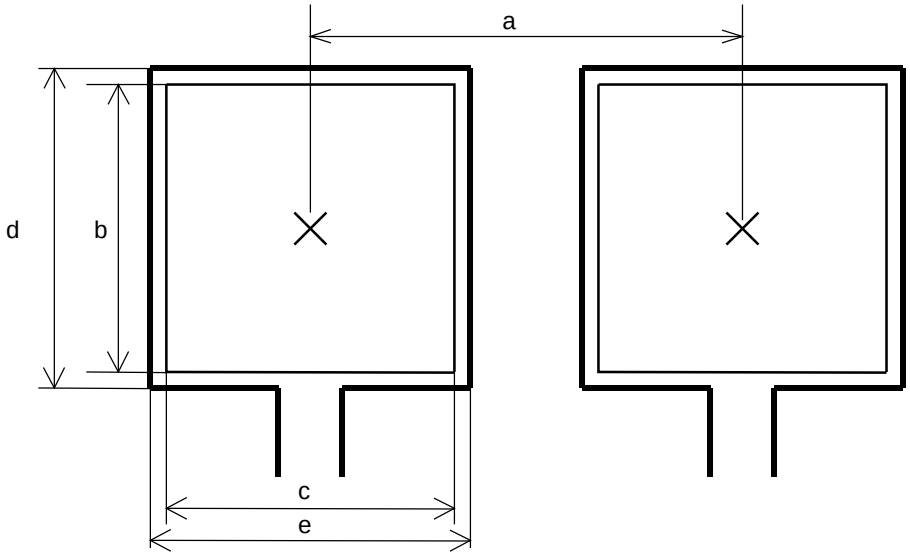


Fig.1 PAD layout

## BLOCK DIAGRAM

An asterisk (*) indicates the port secondary function. ⬚ indicates that the power is supplied to the circuits corresponding to the signal names inside ⬚ from $V_{DDI}$ ( power supply for interface ) .