OKI Semiconductor

PEDL67Q5250-01
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ML67Q5250 Preliminary

DFT Based Fingerprint Authentication LSI

GENERAL DESCRIPTION

The ML67Q5250 is a single chip LSI that executes fingerprint authentication without external memory by using the embedded fingerprint authentication accelerator. This fingerprint authentication accelerator uses DFT(Discrete Fourier Transform) based algorithm licensed from Precise Biometrics, and supports AuthenTec's slide sensors and certain touch sensors from several sensor manufacturers. Besides the ML67Q5250 has the secure circuit to protect enrolled fingerprint data from unauthorized access. Thus this LSI helps customers quickly design new products that offer convenient security as far as high performance fingerprint authentication, low cost and high level of security.

FEATURES

- Fingerprint authentication
  - DTF (Discrete Fourier Transform) based algorithm licensed from Precise Biometrics
    This DFT based algorithm achieves a lower FTE (False To Enrollment rate) and a higher authentication accuracy especially when a slide sensor is used, as compared to the minutiae algorithm.
  - Easy-to-use
    The fingerprint authentication is performaed by the fingerprint authentication accelerator, which does not ask customers for so complicated control.
  - No external memory
    Customer's application program and up to 15 fingerprint data can be stored in the embedded Flash memory on the ML67Q5250. No external memory is required, when a slide sensor is used. External memory is required when a touch sensor is used.
  - High-speed authentication, besides low power consumption
    The highly optimized fingerprint authentication accelerator achieves high-speed authentication using a low speed clock.
    Authentication : < 0.8 seconds (1:1 authentication)
    < 1.8 seconds (1:15 authentication)
    Enrollment : < 2 seconds/finger
  - Applicable fingerprint sensor
    Slide sensor : AuthenTec AES1510 (128 × 8 pixels)
    AuthenTec AES2510 (192 × 16 pixels)
    Touch sensor : Any vendor's touch sensor as far as 256 × 360 pixels max., 8 bits/pixel and 500±8 dpi

- CPU
  - 32-bit RISC CPU (ARM7TDMI)
  - Little endian format
  - Instruction system: A high-density 32-bit instruction and a 16-bit instruction of high-object efficiency, which is the subset of the 32-bit instruction, can be executed in mixed mode.
  - General-purpose register: 32 bits x 31 registers
  - Built-in barrel shifter (ALU and barrel shift operation can be executed by one instruction)
  - Built-in debugging function (JTAG interface)
    The JTAG interface pin is shared with GPIO.

• Internal RAM
- Working RAM for CPU : 16 Kbytes
- Fingerprint authentication RAM : 39 Kbytes
  This RAM can be used as working RAM for CPU while fingerprint authentication is not performed.

• Internal Flash ROM
- 128 Kbyte Flash ROM
- Program ROM : 64 Kbytes
  This program ROM includes drivers for fingerprint authentication and peripherals.
  Erase/rewrite times : 100 max.
- Data ROM for storing fingerprint data : 64 Kbytes
  Erase/rewrite times : 10,000 max. (when enrolling one fingerprint data)

• External memory controller
- ROM/Flash
  • 1 bank x 4 Mbytes
  • Supports 16-bit devices
  • Bootable from external ROM/Flash
    This function can not be used during security function being activated.
- SRAM
  • 1 bank × 4 Mbytes
  • Supports 16-bit devices
- External I/O
  • 2-bank × 4 Mbytes
  • Supports 8-bit/16-bit devices
  • Enable to set address setup, RW/WE pulse, and data off timing in system clock cycle unit
  • Supports an access wait function by wait signal

• Interrupt control
- FIQ: 1 interrupt source
- IRQ: 22 interrupt sources
  7 priority levels can be set for each source.

• DMA controller (DMAC)
- 2 channels
- Enable to allocate multiple DMA transfer request sources for each channel.
- Channel priority: fixed mode/round robin mode
- DMA transfer mode: cycle steal mode/burst mode
- DMA request type: software requests/hardware requests
- Maximum transfer count : 65,536
- Data transfer size: 8 bits/16 bits/32 bits
- Transfer request source: CPU, SPI, Synchronous SIO, Smartcard IF

- GPIO
  - 13 bits × 1 channel, 14 bits × 1 channel, and 16 bits × 1 channel
  - Enable to setting input mode or output mode for each bit
  - Enable to setting as interruption source for each bit
  - Interruption mode: level/edge and positive logic/negative logic

- System timer
  - 16-bit auto reload timer × 1 channel

- Flexible timer (FTM)
  - 16-bit timer × 3 channels
  - Operating mode
    Auto reload timer (ART) /Compare Out (CMO) /pulse width modulation (PWM) /capture (CAP) mode.

- Watch dog timer (WDT)
  - 16-bits timer
  - 8.389 seconds max. (when CPU operating frequency is 32 MHz)
  - Enables generation of interrupt or reset by setting

- SIO (UART)
  - Full-duplex asynchronous mode
  - Built-in baud rate generator

- SPI
  - 2 channels of full-duplex serial peripheral interfaces
  - Operating mode: master mode/slave mode
  - Data transfer size: 8 bits (byte) / 16 bits (word)
  - Built-in 16-byte/16-word FIFO on the transmission side and the reception side
  - Supports DMA transfer (master/slave mode)

- Synchronous SIO (SSIO)
  - 8-bit clock synchronous serial port × 1 channel
  - Selectable clock polarity
  - Selectable LSB first or MSB first
  - Operation mode: master mode/slave mode
  - Supports DMAC transfer (in master mode only)

- Smart Card interface (Smartcard IF)
  - ISO UART × 1 channel
  - Built-in 16-byte FIFO
  - Built-in parity error counter in receive mode and transmit mode at automatic retransmission
  - Supports asynchronous protocol of T = 0 and T = 1 according to ISO7816 and EMV
  - Built-in error detection code generation and error detection functions by hardware
  - Supports DMA transfer

- USB2.0 full-speed device
  - Compliant with Universal Serial Bus (USB) 2.0
  - Full speed (12 Mbps) × 1 port.
  - End points: 5 or 6
  - Supports all data transfer types (control transfer, bulk transfer, interrupt transfer, isochronous transfer).
  - Built-in SOF generation and CRC5/16 generation functions
  - Access size to data transfer FIFOs: 8 bits/16 bits/32 bits

- Random number generator (RANDOM)
  - Generates 8-bit random numbers

- Clock
  - Input clock: 12 MHz (oscillator connected)
  - System clock (CPU operating clock): 32 MHz
    System clock is generated by PLL using 12MHz clock.
  - Output clock: 6/12 MHz for fingerprint sensor

- Power management
  - Power saving mode
    - Individual module clock stop mode:
      Clock operation/stop can be set for each functional block.
    - Sensor interrupt wait mode:
      Start /stop of finger sensor clock output and internal PLL are selectable.
    - STOP mode:
      Start /stop of internal PLL and OSC oscillator circuit are selectable.

- Package
  - 144-pin LFBGA (P-LFBGA144-1111-0.80)

BLOCK DIAGRAM

Figure 1 shows a block diagram of this LSI.

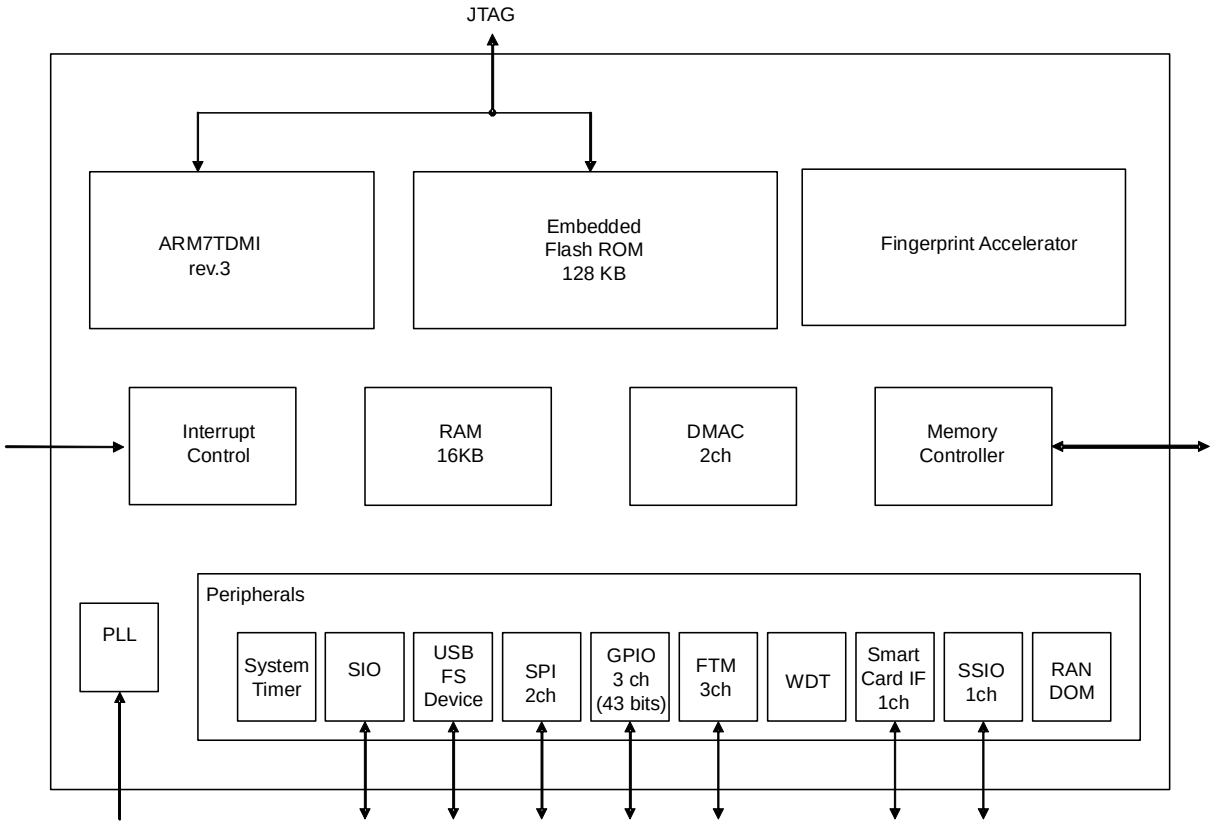


Figure 1 Block Diagram

PINS

Pin Layout

TEST0	GNDIO	PB07	PB05	PB03T	VDDIO	PB00X	VDD CORE	XD08	XD07	XD06	TEST1	TESTF	13
XBNS0	XBSN1	PB06	GND CORE	XD15	XD14	GNDIO	XD10	XD09	GND CORE	PC13	PC12	PC11	12
VDDIO	XIO1 CSN	PB08	VDD CORE	PB04	PB02	XD13	XD12	VDDIO	PC14	PC10	PC08	XD05	11
PB09	PB10	XIO0 CSN	XWAIT 0N	XWAIT 1N	JTAGE	PB01	XD11	PC15	GNDIO	PC09	XD03	XD04	10
XREN	XROM CSN	XWEN	GNDIO						XD01	VDDIO	XD00	XD02	9
XRAM CSN	PB11	GND CORE	PB12						TEST2	PC06	PC07	GNDIO	8
VDDIO	XA01	VDD CORE	XA00	P-LFBGA-144-1111-0.80 (Bottom View)					PC04	VDDIO	PC05	PC03	7
XA04	GNDIO	XA02	XA03						PC02	TEST3	PC01	PC00	6
VDDIO	XA05	XA08	XA06						PA13	GND CORE	GNDIO	PA12	5
XA09	XA07	XA11	XA16	PA01	XA21	PA05	PA06	XI	N.C.	VDDIO	VDD CORE	DM	4
XA12	XA10	GNDIO	XA18	XA19	N.C.	PA04	BOOTP	PLL VDD	PA08	VDD CORE	N.C.	DP	3
XA13	XA14	VDD CORE	PA00	VDDIO	XA20	N.C.	PA07	XO	PLL GND	GND CORE	GNDIO	PUCTL	2
VDDIO	GND CORE	XA15	XA17	GNDIO	PA02	PA03	GNDIO	VDDIO	RESET N	PA09	PA10	PA11	1
N	M	L	K	J	H	G	F	E	D	C	B	A	

Pin List

Pin No.	Pin name	I/O	Polarity (*2)	Description		Schmitt	PU/PD (*1)	Drive capability	5V Tolerant	Initial direction	Initial value
				Primary function	Secondary function						
	Clock										
E4	XI	—	—	Oscillation pin	—	—	—	—	—	I	—
E2	XO	—	—	Oscillation pin	—	—	—	—	—	O	—
	Reset										
D1	RESETN	I	N	System reset input	—	S	PU	4mA	—	I	—
	JTAG										
H10	JTAGE	I	P	JTAG enable	—	S	PD	4mA	—	I	—
	GPIO										
D5	PA13	I/O	P	General-purpose port A13	External interrupt input (Interrupt No. 30)	S	PD	4mA	—	I	—
A5	PA12	I/O	P	General-purpose port A12	Clock output (for sensor)	—	PD	4mA	—	I	—
A1	PA11	I	P	General-purpose port A11	External interrupt input (USB VBUS interrupt)	S	—	—	○	I	—
B1	PA10	I/O	P	General-purpose port A10	External interrupt input (Interrupt No. 28)	S	PD	4mA	—	I	—
C1	PA09	I/O	P	General-purpose port A9	External interrupt input (Interrupt No. 26)	S	PD	4mA	—	I	—
D3	PA08	I/O	P	General-purpose port A8	External FIQ interrupt input	S	PD	4mA	—	I	—
F2	PA07	I/O	P	General-purpose port A7	—	—	PD	4mA	—	I	—
F4	PA06	I/O	P	General-purpose port A6	Smartcard IF clock	—	PD	4mA	—	I	—
G4	PA05	I/O	P	General-purpose port A5	Smartcard IF reset	—	PD	4mA	—	I	—
G3	PA04	I/O	P	General-purpose port A4	Smartcard IF serial data	—	PD	4mA	—	I	—
G1	PA03	I/O	P	General-purpose port A3	Smartcard IF power control	—	PD	4mA	—	I	—
H1	PA02	I/O	P	General-purpose port A2	Smartcard IF voltage control 1	—	PD	4mA	—	I	—
J4	PA01	I/O	P	General-purpose port A1	Smartcard IF voltage control 0	—	PD	4mA	—	I	—
K2	PA00	I/O	P	General-purpose port A0	Smartcard IF card detection	—	PD	4mA	—	I	—
K8	PB12	I/O	P	General-purpose port B12	SIO receive data input	—	PD	4mA	—	I	—
M8	PB11	I/O	P	General-purpose port B11	SIO transmit data output	—	PD	4mA	—	I	—
M10	PB10	I/O	P	General-purpose port B10	FTM2 FTMIN[2]/FTMOUT[2] INOUT	—	PD	4mA	—	I	—
N10	PB09	I/O	P	General-purpose port B09	FTM1 FTMCLK[1] IN/FTMIN[1]/FTMOUT[1] INOUT	—	PD	4mA	—	I	—
L11	PB08	I/O	P	General-purpose port B08	FTM0 FTMCLK[0] IN/FTMIN[0]/FTMOUT[0] INOUT	—	PD	4mA	—	I	—
L13	PB07	I/O	P	General-purpose port B07	JTAG clock	S	PD	4mA	—	I	—

Pin No.	Pin name	I/O	Polarity	Description		Schmitt	PU/PD (*1)	Drive capability	5V Tolerant	Initial direction	Initial value
				Primary function	Secondary function						
L12	PB06	I/O	P	General-purpose port B06	JTAG mode setting	S	PD	4mA	—	I	—
K13	PB05	I/O	P	General-purpose port B05	JTAG data input	S	PD	4mA	—	I	—
J11	PB04	I/O	P	General-purpose port B04	JTAG data output	—	PD	4mA	—	I	—
J13	PB03	I/O	P	General-purpose port B03	JTAG reset	S	PD	4mA	—	I	—
H11	PB02	I/O	P	General-purpose port B02	SSIO communication clock input/output	S	PD	4mA	—	I	—
G10	PB01	I/O	P	General-purpose port B01	SSIO receive data input	—	PD	4mA	—	I	—
G13	PB00	I/O	P	General-purpose port B00	SSIO transmit data output	—	PD	4mA	—	I	—
E10	PC15	I/O	P	General-purpose port C15	—	—	—	4mA	—	I	—
D11	PC14	I/O	P	General-purpose port C14	—	—	—	4mA	—	I	—
C12	PC13	I/O	P	General-purpose port C13	—	—	—	4mA	—	I	—
B12	PC12	I/O	P	General-purpose port C12	—	—	—	4mA	—	I	
A12	PC11	I/O	P	General-purpose port C11	—	—	PD	4mA	—	I	
C11	PC10	I/O	P	General-purpose port C10	—	—	PD	4mA	—	I	
C10	PC09	I/O	P	General-purpose port C9	—	—	PD	4mA	—	I	
B11	PC08	I/O	P	General-purpose port C8	—	—	PD	4mA	—	I	
B8	PC07	I/O	P	General-purpose port C7	SPI ch1 transmit/receive clock	S	PD	4mA	—	I	
C8	PC06	I/O	P	General-purpose port C6	SPI ch1 slave select	S	PD	4mA	—	I	
B7	PC05	I/O	P	General-purpose port C5	SPI ch1 master input/slave output	—	PD	4mA	—	I	
D7	PC04	I/O	P	General-purpose port C4	SPI ch1 master output/slave input	—	PD	4mA	—	I	
A7	PC03	I/O	P	General-purpose port C3	SPI ch0 transmit/receive clock	S	PD	4mA	—	I	
D6	PC02	I/O	P	General-purpose port C2	SPI ch0 slave select	S	PD	4mA	—	I	
B6	PC01	I/O	P	General-purpose port C1	SPI ch0 master input/slave output	—	PD	4mA	—	I	
A6	PC00	I/O	P	General-purpose port C0	SPI ch0 master output/slave input	—	PD	4mA	—	I	
	USB FS Device										
A4	DM	I/O	P	USB dev D-	—	—	—	—	—		
A3	DP	I/O	P	USB dev D+	—	—	—	—	—		
A2	PUCTL	O	P	USB dev pull-up control	—	—	—	4mA	—		
	External Memory Bus										
H4	XA21	O	P	External bus address signal	—	—	—	4mA	—	O	
H2	XA20	O	P	External bus address signal	—	—	—	4mA	—	O	
J3	XA19	O	P	External bus address signal	—	—	—	4mA	—	O	
K3	XA18	O	P	External bus address signal	—	—	—	4mA	—	O	
K1	XA17	O	P	External bus address signal	—	—	—	4mA	—	O	
K4	XA16	O	P	External bus address signal	—	—	—	4mA	—	O	
L1	XA15	O	P	External bus address signal	—	—	—	4mA	—	O	
M2	XA14	O	P	External bus address signal	—	—	—	4mA	—	O	
N2	XA13	O	P	External bus address signal	—	—	—	4mA	—	O	

Pin No.	Pin name	I/O	Polarity	Description		Schmitt	PU/PD (*1)	Drive capability	5V Tolerant	Initial direction	Initial value
				Primary function	Secondary function						
N3	XA12	O	P	External bus address signal	—	—	—	4mA	—	O	0
L4	XA11	O	P	External bus address signal	—	—	—	4mA	—	O	0
M3	XA10	O	P	External bus address signal	—	—	—	4mA	—	O	0
N4	XA09	O	P	External bus address signal	—	—	—	4mA	—	O	0
L5	XA08	O	P	External bus address signal	—	—	—	4mA	—	O	0
M4	XA07	O	P	External bus address signal	—	—	—	4mA	—	O	0
K5	XA06	O	P	External bus address signal	—	—	—	4mA	—	O	0
M5	XA05	O	P	External bus address signal	—	—	—	4mA	—	O	0
N6	XA04	O	P	External bus address signal	—	—	—	4mA	—	O	0
K6	XA03	O	P	External bus address signal	—	—	—	4mA	—	O	0
L6	XA02	O	P	External bus address signal	—	—	—	4mA	—	O	0
M7	XA01	O	P	External bus address signal	—	—	—	4mA	—	O	0
K7	XA00	O	P	External bus address signal	—	—	—	4mA	—	O	0
J12	XD15	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
H12	XD14	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
G11	XD13	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
F11	XD12	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
F10	XD11	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
F12	XD10	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
E12	XD09	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
E13	XD08	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
D13	XD07	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
C13	XD06	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
A11	XD05	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
A10	XD04	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
B10	XD03	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
A9	XD02	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
D9	XD01	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
B9	XD00	I/O	P	External bus data signal	—	S	PU	4mA	—	I	—
M9	XROMCSN	O	N	External ROM chip select	—	—	—	4mA	—	O	1
N8	XRAMCSN	O	N	External RAM chip select	—	—	—	4mA	—	O	1
L10	XIO0CSN	O	N	External IO0 chip select	—	—	—	4mA	—	O	1
M11	XIO1CSN	O	N	External IO1 chip select	—	—	—	4mA	—	O	1
N9	XREN	O	N	External memory read enable	—	—	—	4mA	—	O	1
L9	XWEN	O	N	External memory write enable	—	—	—	4mA	—	O	1
M12	XBSN1	O	N	External memory byte select	—	—	—	4mA	—	O	1
N12	XBSN0	O	N	External memory byte select	—	—	—	4mA	—	O	1
K10	XWAIT0N	I	N	External IO0 access wait	—	S	PU	4mA	—	I	—
J10	XWAIT1N	I	N	External IO1 access wait	—	S	PU	4mA	—	I	—

Pin No.	Pin name	I/O	Polarity	Description		Schmitt	PU/PD (*1)	Drive capability	5V Tolerant	Initial direction	Initial value
				Primary function	Secondary function						
	For System										
F3	BOOTP	I	P	Boot device select 1	—	S	PU	4mA	—	I	—
	For Testing										
A13	TESTF	I	P	Test pin	—	—	—	—	—	I	—
N13	TEST0	I	P	Test mode select signal 0	—	S	PD	4mA	—	I	—
B13	TEST1	I	P	Test mode select signal 1	—	S	PD	4mA	—	I	—
D8	TEST2	I	P	Test mode select signal 2	—	S	PD	4mA	—	I	—
C6	TEST3	I	P	Test mode select signal 3	—	S	PD	4mA	—	I	—

*1: PU/PD column:
PU: Pulled up with a built-in resistor
PD: Pulled down with a built-in resistor
*2: Polarity column:
P: Positive
N: Negative

Other Pins (Power supply pins, Unused pins)

Pin name	Description	Pin No.	Pin count
VDDCORE	Core power supply	C3, L2, L7, K11, F13, B4	6
GNDCORE	Core GND	C2, M1, L8, K12, D12, C5	6
VDDIO	Core power supply	E1, J2, N1, N5, N7, N11, H13, E11, C9, C7, C4	11
GNDIO	Core GND	F1, J1, L3, M6, K9, M13, G12, D10, A8, B5, B2	11
PLLVDD	PLL power supply	E3	1
PLLGND	PLL GND	D2	1
N.C.	Unused pin	G2, H3, B3, D4	4

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage CORE (2.5V)	V_{DD_CORE}	—	–0.3 to +3.6	V
Digital power supply voltage I/O (3.3V)	V_{DD_IO}		–0.3 to +4.6	
Input voltage (normal buffer)	V_I		–0.3 to V_{DD_IO}+0.3	
Input voltage (5 V tolerant)		V_{DD_IO} = 3.0 V to 3.6 V	–0.3 to 6.0	
		V_{DD_IO} < 3.0 V	–0.3 to V_{DD_IO}+0.3	
Output voltage (normal buffer)	V_O		–0.3 to V_{DD_IO}+0.3	
Output voltage (5 V tolerant)		V_{DD_IO} = 3.0 V to 3.6 V	–0.3 to 6.0	
		V_{DD_IO} < 3.0 V	–0.3 to V_{DD_IO}+0.3	
PLL power supply voltage (PLL)	V_{DD_PLL}	—	–0.3 to +3.6	
Input allowable current	I_I		–10 to +10	mA
"H" output allowable current	I_{OH}		+14	
"L" output allowable current	I_{OL}		–14	
Power dissipation	P_D	Ta = 85°C (per package)	600	mW
Storage temperature	T_{STG}	—	–50 to 150	°C

Note:
The values in the table above are preliminary and are subject to change without notice.

Guaranteed Operating Ranges

(GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply voltage (CORE)	V_{DD_CORE}	—	2.25	2.5	2.75	V
Digital power supply voltage (I/O)	V_{DD_IO}		3.0	3.3	3.6	
PLL power supply voltage (PLL)	V_{DD_PLL}		2.25	2.5	2.75	
CPU operating frequency	f_{OSC}	—	—	32	—	MHz
Ambient temperature	Ta	Other than below	–40	25	85	°C
	T_{aflw}	- When enrolling fingerprints - When rewriting Flash memory	–40	25	70	°C

– Internal Flash ROM

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Guaranteed ambient temperature for write operations	$T_{a\_flwrite}$	—	–40	25	70	°C
Guaranteed ambient temperature for read operations	T_{a_flread}	—	–40	25	85	
Flash write count	C_{WR_CODE}	Program code rewrite $T_{a\_flwrite}$ = –40 to +70°C	—	—	100	—
	C_{WR_DATA01}	Fingerprint template data rewrite (for 1-finger enrollment) $T_{a\_flwrite}$ = –40 to +70°C	—	—	10,000	—
	C_{WR_DATA15}	Fingerprint template data rewrite (for 15-finger enrollment) $T_{a\_flwrite}$ = –40 to +70°C	—	—	1,000	—

Note:
The values in the table above are preliminary and are subject to change without notice.

DC Characteristics

– DC characteristics (Core/IO)

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	2.0	—	V_{DD_IO} +0.3	V
"L" input voltage	V_{IL}	—	–0.3	—	0.8	V
Schmitt trigger input threshold voltage	V_{T+}	—	—	—	$V_{DD\_IO}\times 0.7$	V
Schmitt trigger input threshold voltage	V_{T-}	—	$V_{DD\_IO}\times 0.2$	—	—	V
Schmitt trigger input threshold voltage (3.3 V)	ΔV_T	$V_{T+} - V_{T-}$	$V_{DD\_IO}\times 0.1$	—	—	V
Schmitt trigger input threshold voltage	V_{T+}	—	—	—	$V_{DD\_IO}\times 0.7$	V
Schmitt trigger input threshold voltage	V_{T-}	—	$V_{DD\_IO}\times 0.2$	—	—	V
Schmitt trigger input threshold voltage (5 V tolerant)	Δ_{VT}	$V_{T+} - V_{T-}$	$V_{DD\_IO}\times 0.1$	—	—	V
"H" output voltage	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
High level input current (*1)	I_{IH}	$V_{IH} = V_{DD\_IO}$	—	—	10	µA
High level input current (*1)	I_{IH}	$V_{IH} = V_{DD\_IO}$, 50 kΩ pull-down	10	66	200	µA
High level input current (*2)	I_{IH}	$V_{IH} = V_{DD\_IO}$	—	—	10	µA
High level input current (*2)	I_{IH}	V_{IH} = 5.5 V	—	—	10	µA
Low level input current (*1)	I_{IL}	V_{IL} = 0 V	–10	—	—	µA
Low level input current (*1)	I_{IL}	50 kΩ pull-up	–200	–66	–10	µA
Low level input current (*2)	I_{IL}	V_{IL} = 0 V	–10	—	—	µA
3-state output leakage current	I_{OZH}	$V_{OH} = V_{DD\_IO}$	—	—	10	µA
3-state output leakage current	I_{OZH}	50 kΩ pull-down	10	66	200	µA
3-state output leakage current	I_{OZL}	V_{OL} = 0 V	–10	—	—	µA
3-state output leakage current	I_{OZL}	50 kΩ pull-up	–200	–66	–10	µA
Supply current (during STOP) (*4)	I_{DDS1_CORE}	V_{DD_CORE} = 2.75 V, Ta = 85°C	—	—	1000	µA
Supply current (during STOP) (*4)	I_{DDS1_CORE}	V_{DD_CORE} = 2.5 V, Ta = 25°C	—	25	—	µA
Supply current (during STOP) (*4)	I_{DDS1_IO}	V_{DD_IO} = 3.6 V (*3), Ta = 85°C	—	—	200	µA
Supply current (during STOP) (*4)	I_{DDS1_IO}	V_{DD_IO} = 3.3 V (*3), Ta = 25°C	—	4	—	µA
Supply current (during STOP) (*4)	I_{DDS1_PLL}	V_{DD_PLL} = 2.75 V, Ta = 85°C	—	—	50	µA
Supply current (during STOP) (*4)	I_{DDS1_PLL}	V_{DD_PLL} = 2.5 V, Ta = 25°C	—	1	—	µA
Supply current (during fingerprint authentication)	I_{DDO_CORE}	f_{OSC} = 32.0 MHz , no load	—	100	150	mA
Supply current (during fingerprint authentication)	I_{DDO_IO}	f_{OSC} = 32.0 MHz , no load	—	20	40	mA
Supply current (during fingerprint authentication)	I_{DDO_PLL}	f_{OSC} = 32.0 MHz , no load	—	7.0	14	mA

* 1: Pins other than 5 V tolerant pins
* 2: 5 V tolerant pins
* 3: Input ports: V_{DD_IO} or 0V
  Other ports: No load excluding the current flowing in pull-up/pull-down resistors
* 4: LSI supply current when going into LSI stop mode by stopping clock oscillation, PLL operation, and random number generator operation and setting USB power-down mode.

– DC characteristics (USB)

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ. (*1)	Max.	Unit
Differential input sensitivity	V_{DI}	¦ (YB) - (YBN) ¦	0.2	—	—	V
Differential common mode range	V_{CM}	Includes VDI range	0.8	—	2.5	V
Single end input threshold voltage	V_{SE}		0.8	—	2.0	V
High level output voltage	V_{OH}	15K W RL is connected to GND	2.8	—	3.6	V
Low level output voltage	V_{OL}	1.5K W RL to 3.6 V	0.0	—	0.3	V
Hi-Z state input/output leakage current	I_{LO}	0 V < VIN < 3.3 V	–10		10	µA
Driver output resistance (*2)	Z_{DRV}	Steady state	28		44	Ω

*1: "Typ.": V_{DD_IO} = 3.3 V, V_{DD_CORE} = 2.5 V, Tj = 25°C

*2: ZDRV includes the resistance of external serial resistors (24Ω±1%).

Note:
The values in the table above are preliminary and are subject to change without notice.

AC Characteristics

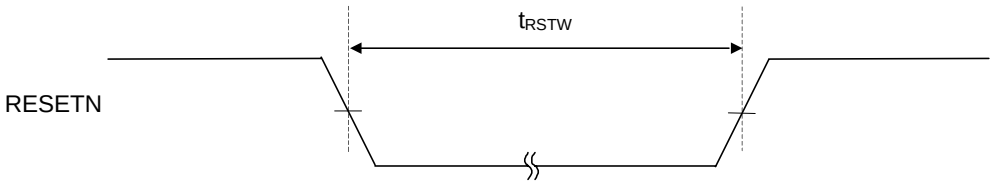
– Reset Timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset pulse width	t_{RSTW}	—	6.0	—	—	ms

Note:
The values in the table above are preliminary and are subject to change without notice.

○ Reset timing



– Main Clock Timing

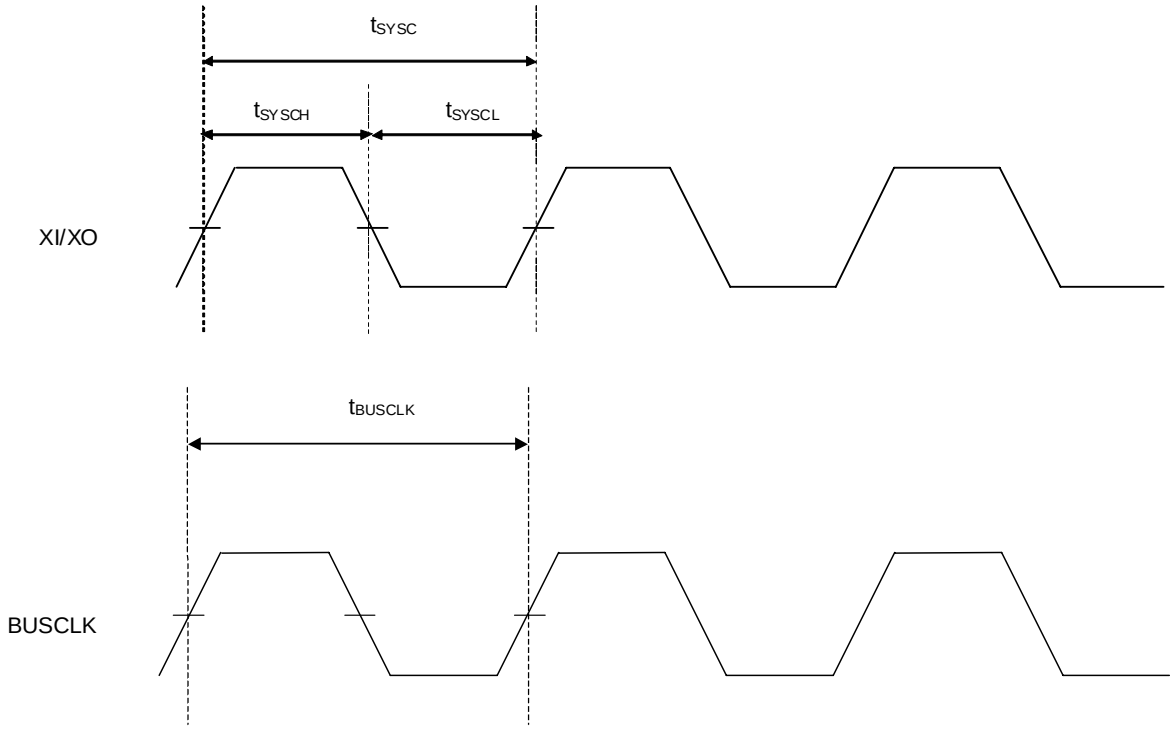
(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Main clock (XI/XO) frequency	f_{SYSC}	—	12 × 0.9975	12	12 × 1.0025	MHz
Main clock (XI/XO) cycle	t_{SYSC}	—	83.33 × 0.9975	83.33	83.33 × 1.0025	ns
Main clock (XI/XO) H pulse width	t_{SYSCH}	—	0.45 × t_{SYSC}	—	0.55 × t_{SYSC}	ns
Main clock (XI/XO) L pulse width	t_{SYSCL}	—	0.45 × t_{SYSC}	—	0.55 × t_{SYSC}	ns
Bus clock cycle (*1)	t_{BUSCLK}	—	—	31.25	—	ns

* 1: Main system bus clock within the LSI and operating clocks of CPU, DMA, etc.

Note:
The values in the table above are preliminary and are subject to change without notice.

○ Main clock timing



– External ROM/RAM Timing

○ Access from CPU

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XROMCSN, XRAMCSN output delay time 1	t_{XCSD1}	CL = 15 pF	—	—	3	ns
XROMCSN, XRAMCSN output delay time 2	t_{XCSD2}		—	—	$0.5*t_{BUSCLK}$ +3	
XROMCSN, XRAMCSN output hold time 1	t_{XCSH1}		–5	—	—	
XROMCSN, XRAMCSN output hold time 2	t_{XCSH2}		$0.5*t_{BUSCLK}$ –5	—	—	
XA output delay time 1	t_{XAD1}		—	—	3	
XA output delay time 2	t_{XAD2}		—	—	$0.5*t_{BUSCLK}$ +3	
XA output hold time 1	t_{XAH1}		–5	—	—	
XA output hold time 2	t_{XAH2}		$0.5*t_{BUSCLK}$ –5	—	—	
XA pulse width 1	t_{XAW1}		t_{RWIDTH} –7	—	t_{RWIDTH} +7	
XBSn output delay time 1	t_{XBSD1}		—	—	3	
XBSn output delay time 2	t_{XBSD2}		—	—	$0.5*t_{BUSCLK}$ +3	
XBSn output hold time 1	t_{XBSH1}		–5	—	—	
XBSn output hold time 2	t_{XBSH2}		$0.5*t_{BUSCLK}$ –5	—	—	
XBSn pulse width 1	t_{XBSW1}		t_{RWIDTH} –7	—	t_{RWIDTH} +7	
XWEN pulse width 1	t_{XWEW1}		t_{WWIDTH} –7	—	t_{WWIDTH} +7	
XD input setup time 1	t_{XDIS1}		25	—	—	
XD input setup time 2	t_{XDIS2}		25	—	—	
XD input hold time 1	t_{XDIH1}		0	—	—	
XD input hold time 2	t_{XDIH2}		0	—	—	
XD output delay time 1	t_{XDOD1}		—	—	$0.5*t_{BUSCLK}$ +5	
XD output hold time 1	t_{XDOH1}		$0.5*t_{BUSCLK}$ –5	—	—	

t_{RWIDTH}: RE pulse width (set by register)
t_{WWIDTH}: WE pulse width (set by register)

Note:
The values in the table above are preliminary and are subject to change without notice.

○ Access by DMA

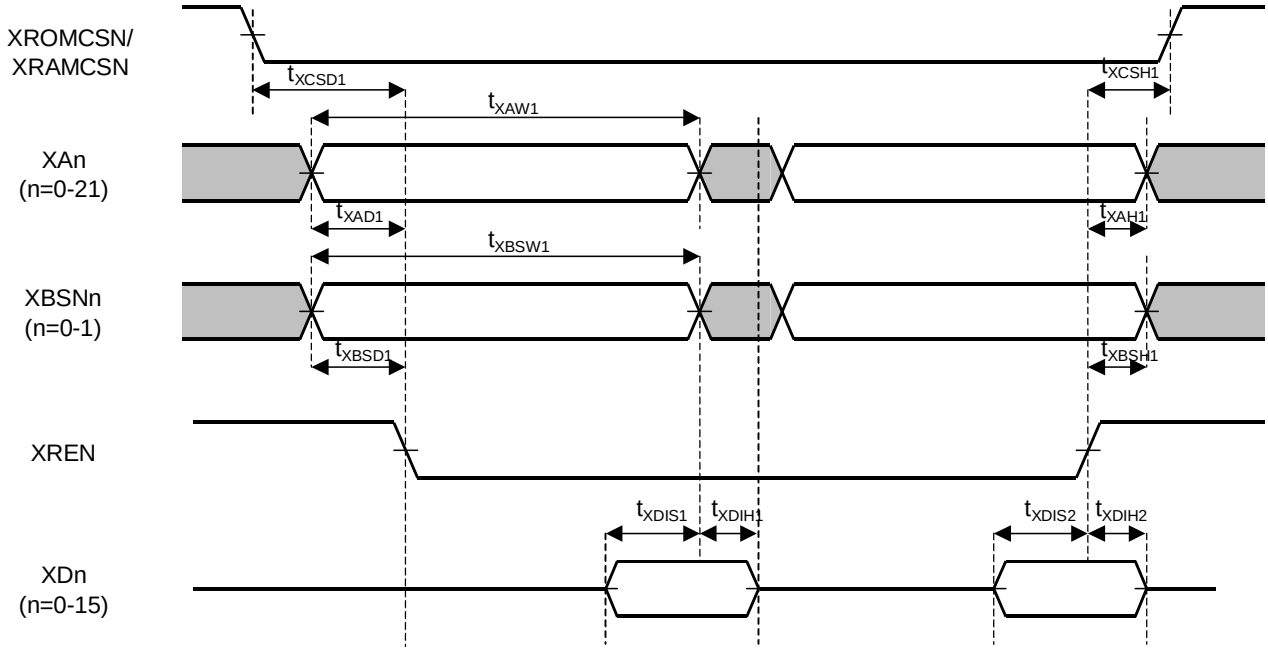
(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XROMCSN, XRAMCSN output delay time 1	t_{XCSD1}	CL = 15 pF	—	—	$1*t_{BUSCLK}$ +3	ns
XROMCSN, XRAMCSN output delay time 2	t_{XCSD2}		—	—	$0.5*t_{BUSCLK}$ +3	
XROMCSN, XRAMCSN output hold time 1	t_{XCSH1}		$1*t_{BUSCLK}$ –5	—	—	
XROMCSN, XRAMCSN output hold time 2	t_{XCSH2}		$0.5*t_{BUSCLK}$ –5	—	—	
XA output delay time 1	t_{XAD1}		—	—	$1*t_{BUSCLK}$ +3	
XA output delay time 2	t_{XAD2}		—	—	$1.5*t_{BUSCLK}$ +3	
XA output hold time 1	t_{XAH1}		$1*t_{BUSCLK}$ –5	—	—	
XA output hold time 2	t_{XAH2}		$0.5*t_{BUSCLK}$ –5	—	—	
XA pulse width 1	t_{XAW1}		t_{RWIDTH} –7	—	t_{RWIDTH} +7	
XBSn output delay time 1	t_{XBSD1}		—	—	$1*t_{BUSCLK}$ +3	
XBSn output delay time 2	t_{XBSD2}		—	—	$1.5*t_{BUSCLK}$ +3	
XBSn output hold time 1	t_{XBSH1}		$1*t_{BUSCLK}$ –5	—	—	
XBSn output hold time 2	t_{XBSH2}		$0.5*t_{BUSCLK}$ –5	—	—	
XBSn pulse width 1	t_{XBSW1}		t_{RWIDTH} –7	—	t_{RWIDTH} +7	
XWEN pulse width 1	t_{XWEW1}		t_{WWIDTH} –7	—	t_{WWIDTH} +7	
XD input setup time 1	t_{XDIS1}		25	—	—-	
XD input setup time 2	t_{XDIS2}		25	—	—	
XD input hold time 1	t_{XDIH1}		0	—-	—	
XD input hold time 2	t_{XDIH2}		0	—	—-	
XD output delay time 1	t_{XDOD1}		—	—	$1.5*t_{BUSCLK}$ +5	
XD output hold time 1	t_{XDOH1}		$0.5*t_{BUSCLK}$ –5	—	—-	

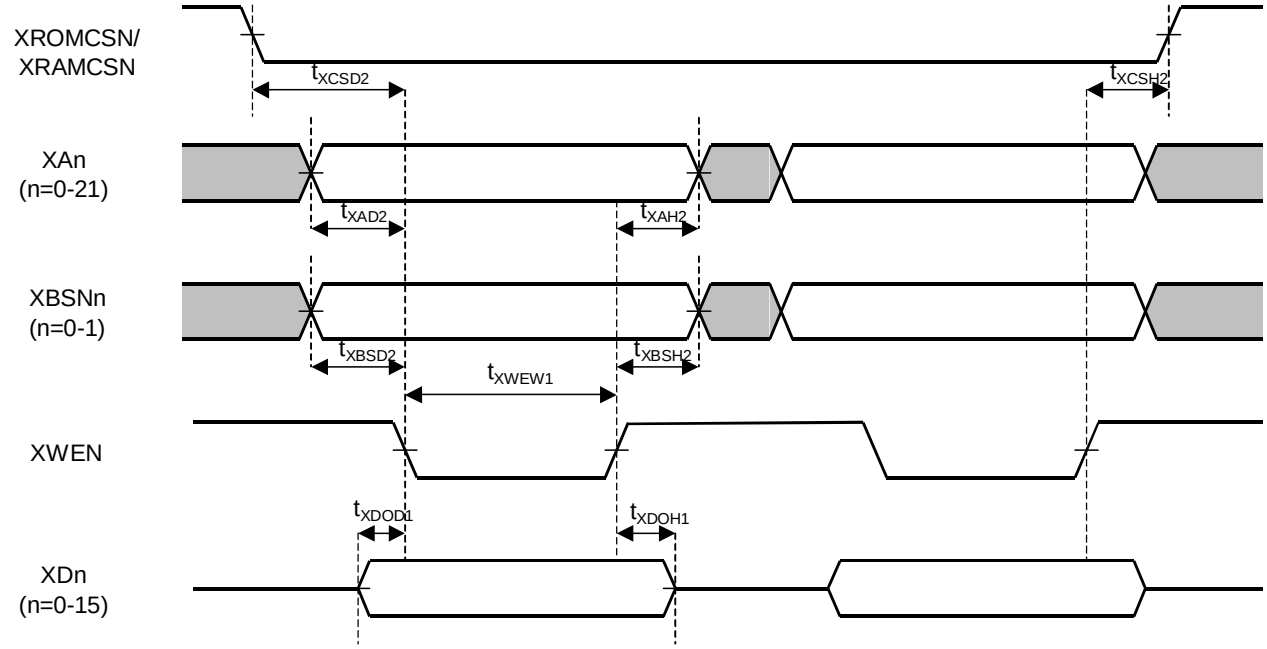
t_{RWIDTH}: RE pulse width (set by register)
t_{WWIDTH}: WE pulse width (set by register)

Note:
The values in the table above are preliminary and are subject to change without notice.

○ External ROM/RAM read timing



○ External ROM/RAM write timing



– External IO0, 1 Timing

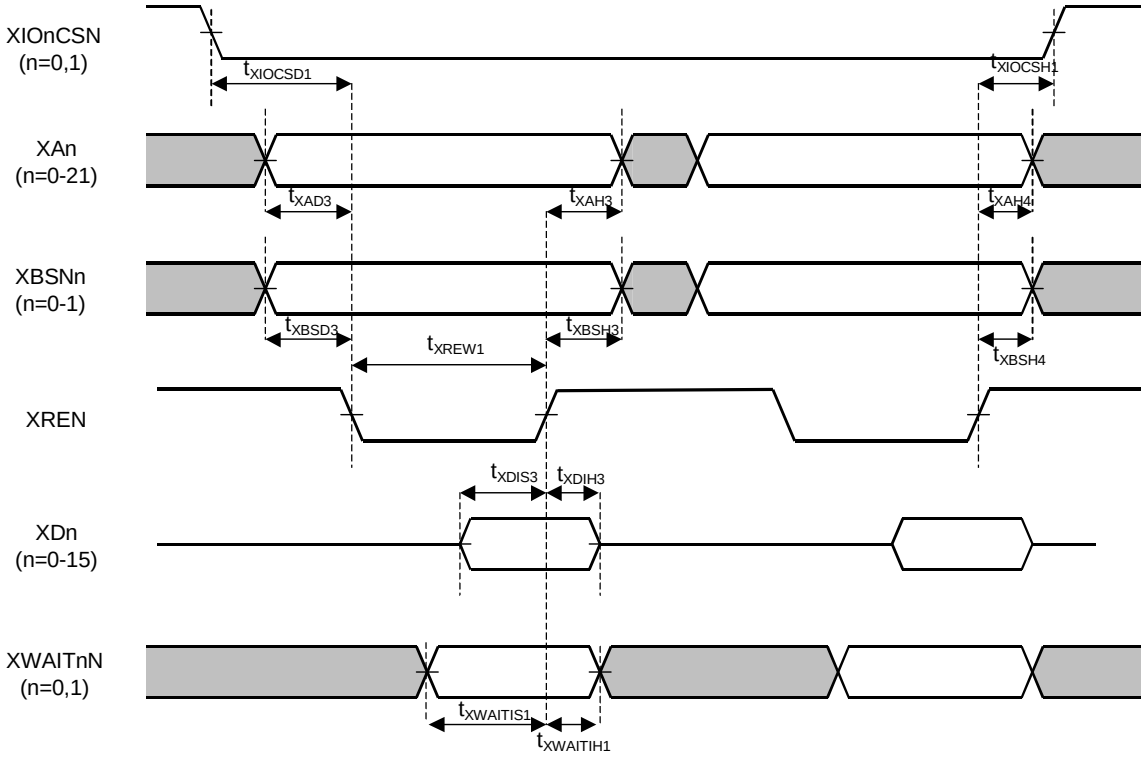
(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
XIOnCSN (n = 0,1) output delay time 1	$t_{XIOCSD1}$	CL = 15 pF	—	—	t_{IOAS} +5	ns
XIOnCSN (n = 0,1) output delay time 2	$t_{XIOCSD2}$		—	—	1*t_{BUSCLK} + t_{IOAS} +5	
XIOnCSN (n=0,1) output hold time 1	$t_{XIOCSH1}$		1*t_{BUSCLK} –5	—	—	
XIOnCSN (n = 0,1) output hold time 2	$t_{XIOCSH2}$		1*t_{BUSCLK} –5	—	—	
XA output delay time 3	t_{XAD3}		—	—	t_{IOAS} + 5	
XA output delay time 4	t_{XAD4}		—	—	1*t_{BUSCLK} + t_{IOAS} +5	
XA output hold time 3	t_{XAH3}		–5	—	—	
XA output hold time 4	t_{XAH4}		1*t_{BUSCLK} –5	—	—	
XA output hold time 5	t_{XAH5}		1*t_{BUSCLK} –5	—	—	
XBSn output delay time 3	t_{XBSD3}		—	—	t_{IOAS} + 5	
XBSn output delay time 4	t_{XBSD4}		—	—	1*t_{BUSCLK} + t_{IOAS} +5	
XBSn output hold time 3	t_{XBSH3}		–5	—	—	
XBSn output hold time 4	t_{XBSH4}		1*t_{BUSCLK} –5	—	—	
XBSn output hold time 5	t_{XBSH5}		1*t_{BUSCLK} –5	—	—	
XREN pulse width 1	t_{XREW1}		$t_{IORWIDTH}$ –5	—	$t_{IORWIDTH}$ +5	
XWEN pulse width 2	t_{XWEW2}		$t_{IOWWIDTH}$ –5	—	$t_{IOWWIDTH}$ +5	
XD input setup time 3	t_{XDIS3}		20	—	—	
XD input hold time 3	t_{XDIH3}		0	—	—	
XD output delay time 2	t_{XDOD2}		—	—	t_{IOAS} +5	
XD output hold time 2	t_{XDOH2}		1*t_{BUSCLK} –5	—	—	
XWAITn (n = 0,1) input setup time 1	$t_{XWAITIS1}$		1*t_{BUSCLK} + 20	—	—	
XWAITn (n = 0,1) input setup time 2	$t_{XWAITIS2}$		1*t_{BUSCLK} + 20	—	—	
XWAITn (n = 0,1) input hold time 1	$t_{XWAITIH1}$		5 –1*t_{BUSCLK}	—	—	
XWAITn (n = 0,1) input hold time 2	$t_{XWAITIH2}$		5 –1*t_{BUSCLK}	—	—	

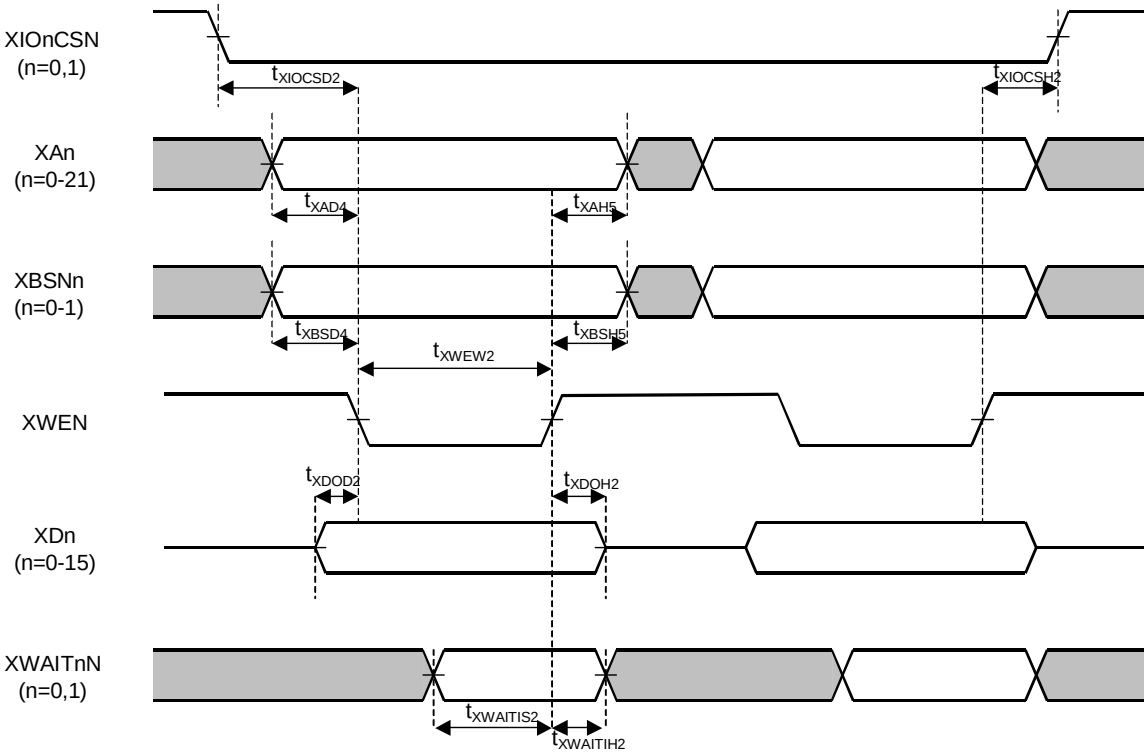
t_{IOAS}: Address setup cycle (set by register)
$t_{IORWIDTH}$: RE pulse width (set by register)
$t_{IOWWIDTH}$: WE pulse width (set by register)

Note:
The values in the table above are preliminary and are subject to change without notice.

○ External IO0, 1 read timing



○ External IO0, 1 write timing



– USB Access Timing (Full-Speed)

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied pin
Rise time (*1)	T_R	CL = 50 pF	4	—	20	ns	D+, D–
Fall time (*1)	T_F	CL = 50 pF	4	—	20	ns	
Output signal crossover voltage	V_{CRS}	CL = 50 pF	1.3	—	2	V	
Data rate	T_{DRATE}	Average bit rate (12Mbps ±0.25%)	11.97	—	12.03	Mbps	

* 1: T_R and T_F: Rise time and fall time between 10% and 90% of the pulse amplitude, respectively

Note:
The values in the table above are preliminary and are subject to change without notice.

– SPI Access Timing

Characteristics of master mode timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial clock cycle time	t_{SCK}		2	—	2046	t_{BUSCLK}
Serial clock High/Low time	t_{WSCK}		1	—	1023	t_{BUSCLK}
Data delay time (output)	t_{DD}		—	—	25	ns
Data setup time (input)	t_{SD}	CL = 30 pF	25	—	—	ns
Data hold time (input)	t_{HD}		0 (*1)	—	—	ns
SSN-SCK lead time	t_{LEAD}		0.5	—	1.5	t_{sck}
SCK-SSN lag time	t_{LAG}		0.5	—	1.5	t_{sck}
SSN H min. guaranteed time	t_{WSSH}		1	—	511	t_{sck}
SPI bus input/output rise/fall time	t_R, t_F		—	—	25	ns

* 1: Although actual values may become negative depending on the external load, input the serial data so that the data hold time can be guaranteed.

Note:
The values in the table above are preliminary and are subject to change without notice.

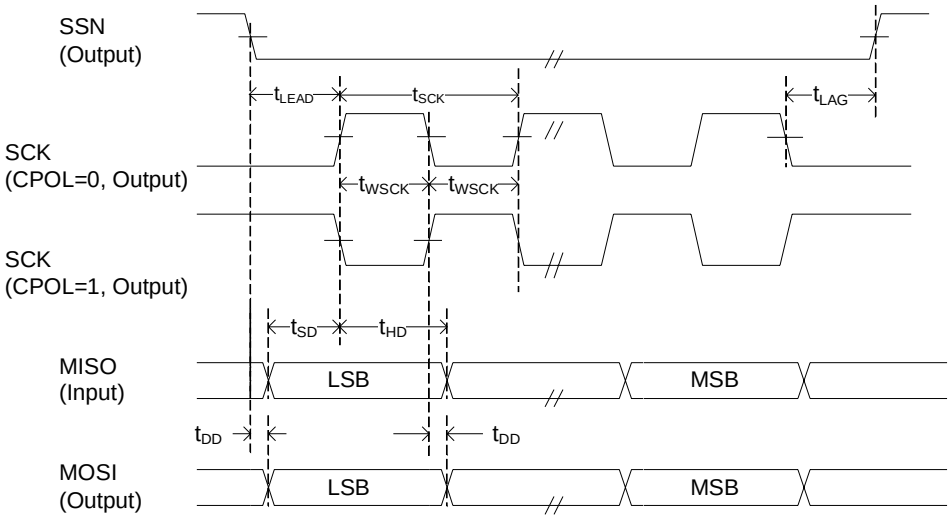
Characteristics of slave mode timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

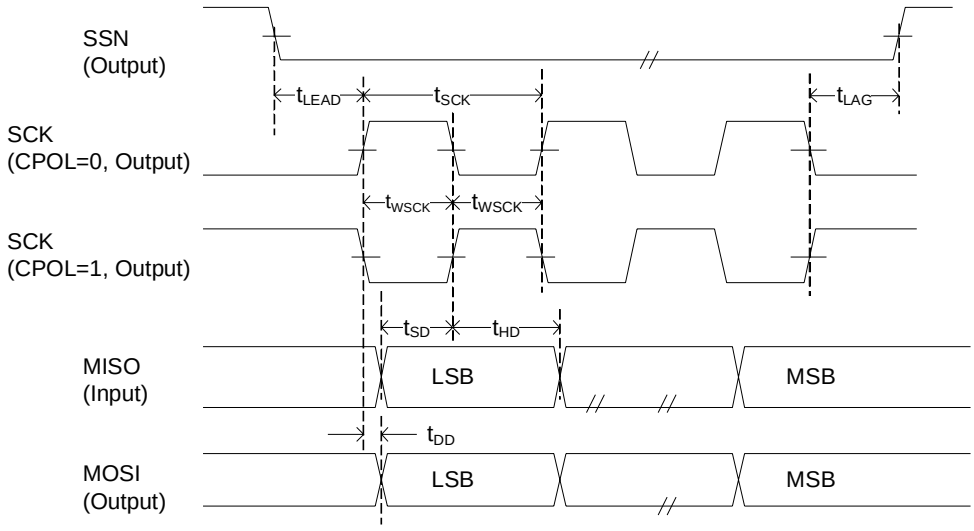
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial clock cycle time	t_{SCK}	—	2	—	—	t_{BUSCLK}
Serial clock High/Low time	t_{WSCK}	—	1	—	—	t_{BUSCLK}
Data delay time (output)	t_{DD}	—	—	—	25	ns
Data setup time (input)	t_{SD}	—	25	—	—	ns
Data hold time (input)	t_{HD}	—	25	—	—	ns
SSN-SCK lead time	t_{LEAD}	—	25	—	—	ns
SCK-SSN lag time	t_{LAG}	—	25	—	—	ns
Slave data invalid time	t_{DIS}	—	—	—	25	ns
SPI bus input/output rise/fall time	t_R, t_F	—	—	—	25	ns

Note:
The values in the table above are preliminary and are subject to change without notice.

○ SPI master mode timing (CPHA = 0)

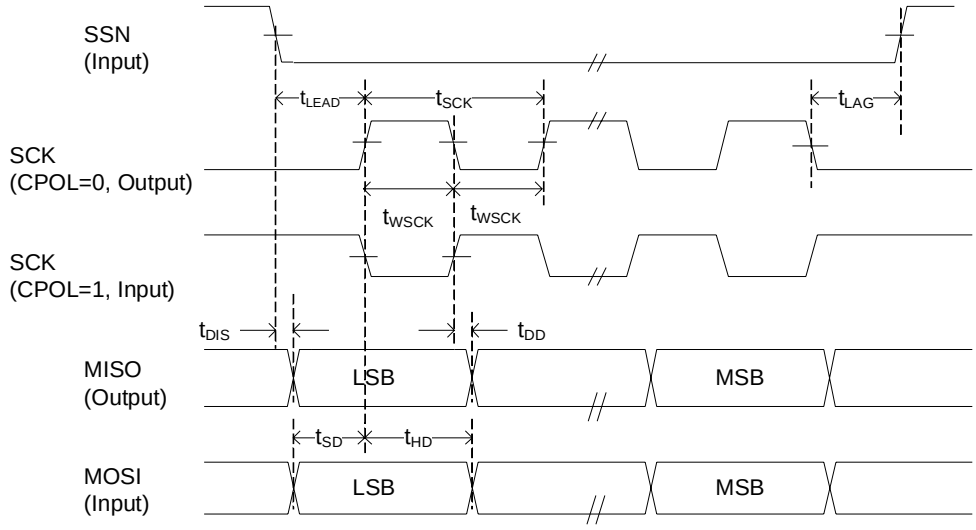


○ SPI master mode timing (CPHA = 1)

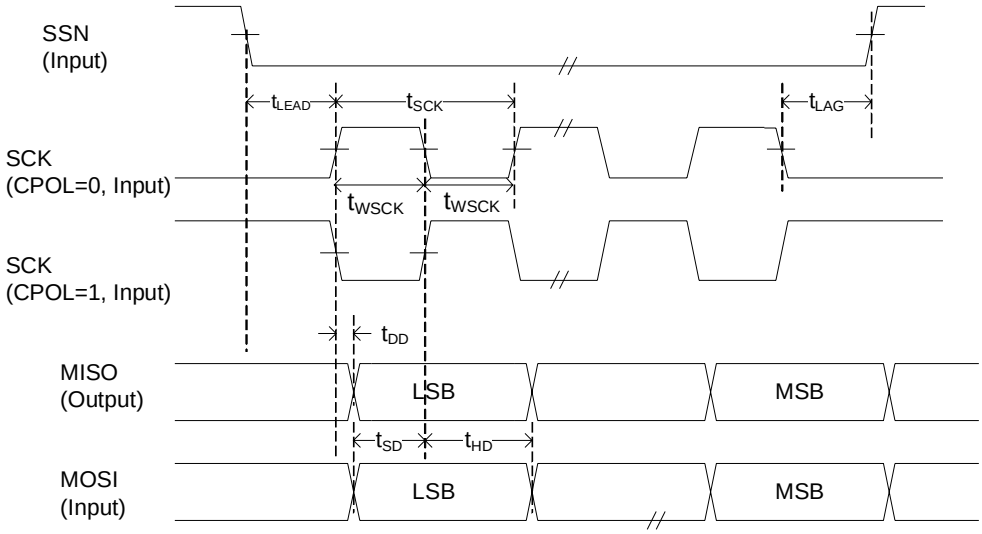


Note:
For CPHA and CPOL, see Section 14.4.1, “SPI Control Registers”, in the ML67Q5250 User’s Manual.

○ SPI slave mode timing (CPHA = 0)



○ SPI slave mode timing (CPHA = 1)



Note:
For CPHA and CPOL, see Section 14.4.1, “SPI Control Registers”, in the ML67Q5250 User’s Manual.

– Synchronous SIO Access Timing

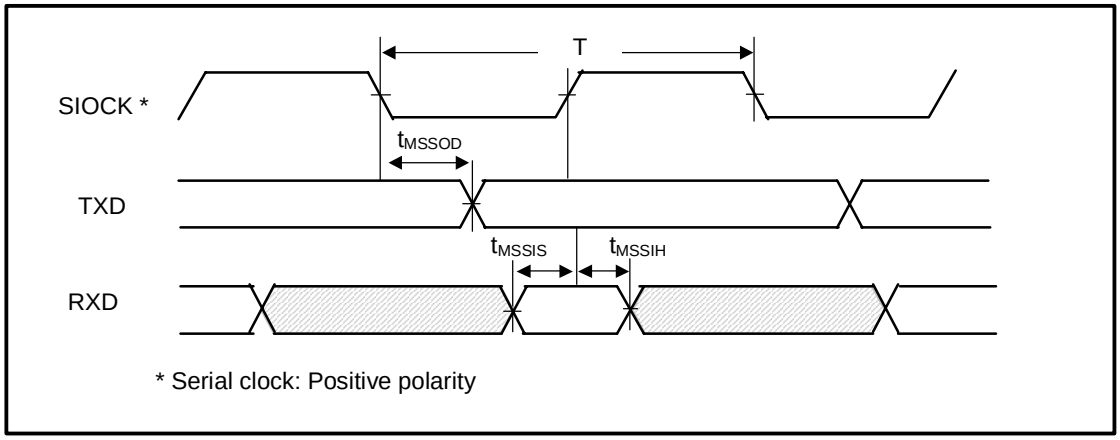
Switching between master mode and slave mode can be set for this synchronous SIO by the software register setting. Serial clock polarity can be switched.
When clock polarity is set to positive, data is transmitted (shifted out) on the falling edge of the clock and is received (shifted in) on the rising edge of the clock. At completion of 8-bit data transmission/reception, the clock stops at a high level and the last data is retained for data output.
When clock polarity is set to negative, data is transmitted (shifted out) on the rising edge of the clock and is received (shifted in) on the falling edge of the clock. At completion of 8-bit data transmission/reception, the clock stops at a low level and the last data is retained for data output.
The following waveforms show the cases where the clock polarity is positive.

• Maste mode

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit	Remarks
Serial clock cycle	T	CL = 50 pF	62.5	—	ns	
Output data delay time	t_{MSSOD}		—	20		
Input data setting time	t_{MSSIS}		40	—		
Input data retained time	t_{MSSIH}		0	—		

Note:
The values in the table above are preliminary and are subject to change without notice.

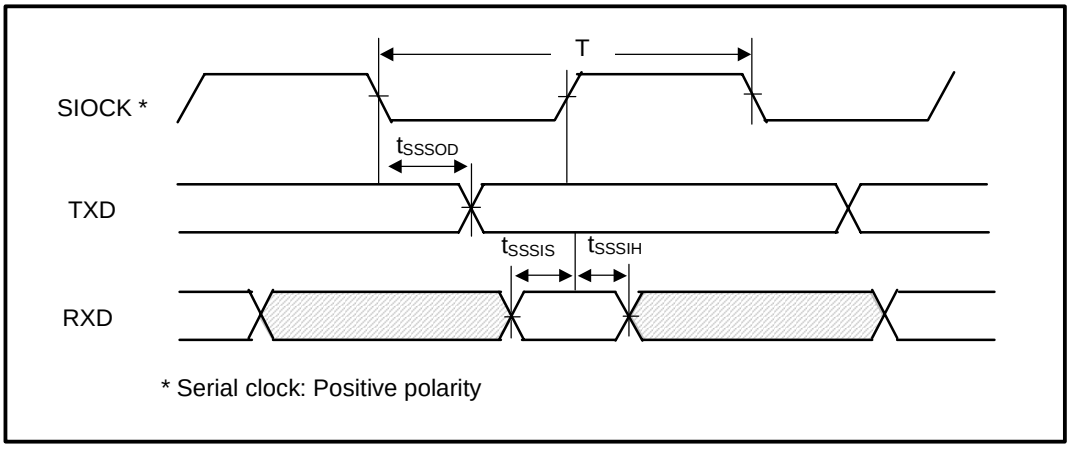


• Slave mode

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit	Remarks
Serial clock cycle	T	CL = 50 pF	62.5	—	ns	
Output data delay time	t_{SSSOD}		—	40		
Input data setting time	t_{SSSIS}		20	—		
Input data retained time	t_{SSSIH}		20	—		

Note:
The values in the table above are preliminary and are subject to change without notice.



– FTM Access Timing

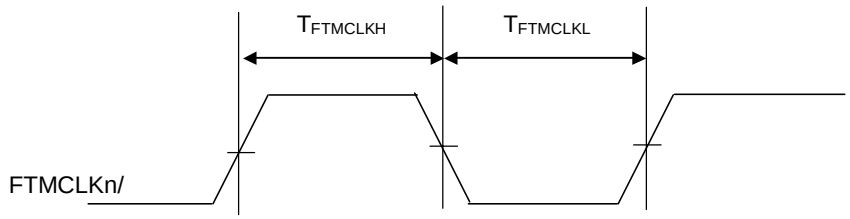
(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FTMCLKn input H duration	$T_{FTMCLKH}$	—	t_{BUSCLK} ×2	—	—	ns
FTMCLKn input L duration	$T_{FTMCLKL}$	—	t_{BUSCLK} ×2	—	—	ns

Note 1: n = 0 to 2

Note:
The values in the table above are preliminary and are subject to change without notice.

○ FTMCLKn input timing (n = 0 to 2)



– GPIO (PA, PB, PC) Access Timing

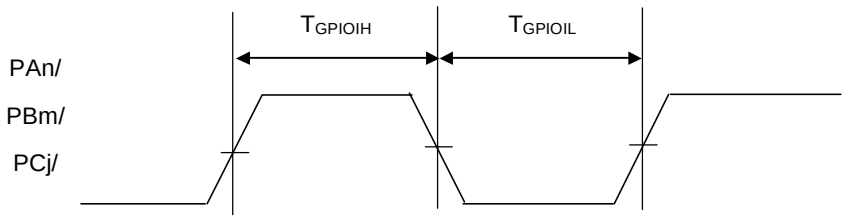
(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PAn, PBm, PCj input H duration	T_{GPIOIH}	—	t_{BUSCLK} ×2	—	—	ns
PAn, PBm, PCj input L duration	T_{GPIOIL}	—	t_{BUSCLK} ×2	—	—	ns

Note 1: n = 12 to 0, m13 to 0, j = 15 to 0

Note:
The values in the table above are preliminary and are subject to change without notice.

○ PAn,PBm,PCj input timing (n = 12 to 0, m = 13 to 0, j = 15 to 0)



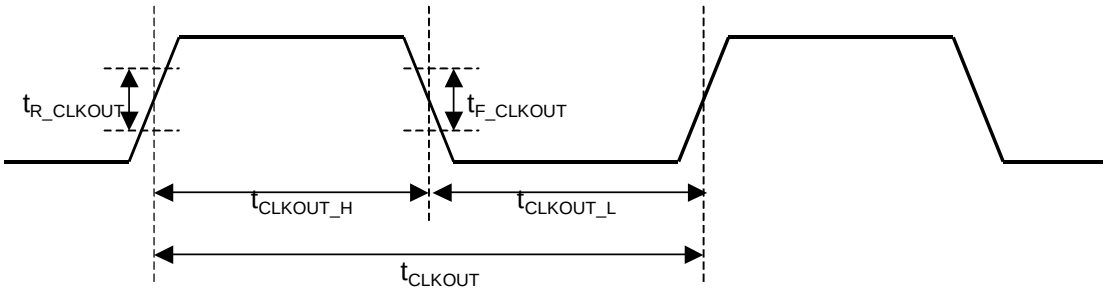
– Clock Output (Secondary Function of PA12 Pin) Timing

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock output cycle	t_{CLKOUT}	6 MHz selected	166.67 – 1%	166.67	166.67 + 1%	ns
		12 MHz selected	83.33 – 1%	83.33	83.33 + 1%	ns
Clock output High duration	t_{CLKOUT_H}	—	45% * t_{CLKOUT}	50% * t_{CLKOUT}	55% * t_{CLKOUT}	ns
Clock output Low duration	t_{CLKOUT_L}	—	45% * t_{CLKOUT}	50% * t_{CLKOUT}	55% * t_{CLKOUT}	ns
Rise time	t_{R_CLKOUT}	CL = 10 pF			3	ns
Fall time	t_{F_CLKOUT}	CL = 10 pF			3	ns

Note:
The values in the table above are preliminary and are subject to change without notice.

○ Clock output (secondary function of PA12 pin) timing



POWER ON/OFF SEQUENCE

Turn on the following powers in this order or turn on all the following powers at the same time.

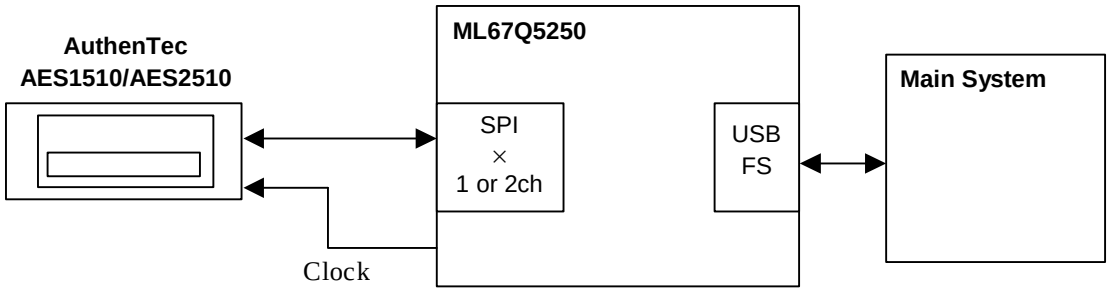
1. VDDIO
2. VDDCORE, PLLVDD

Turn off the following powers in this order or turn off all the following powers at the same time.

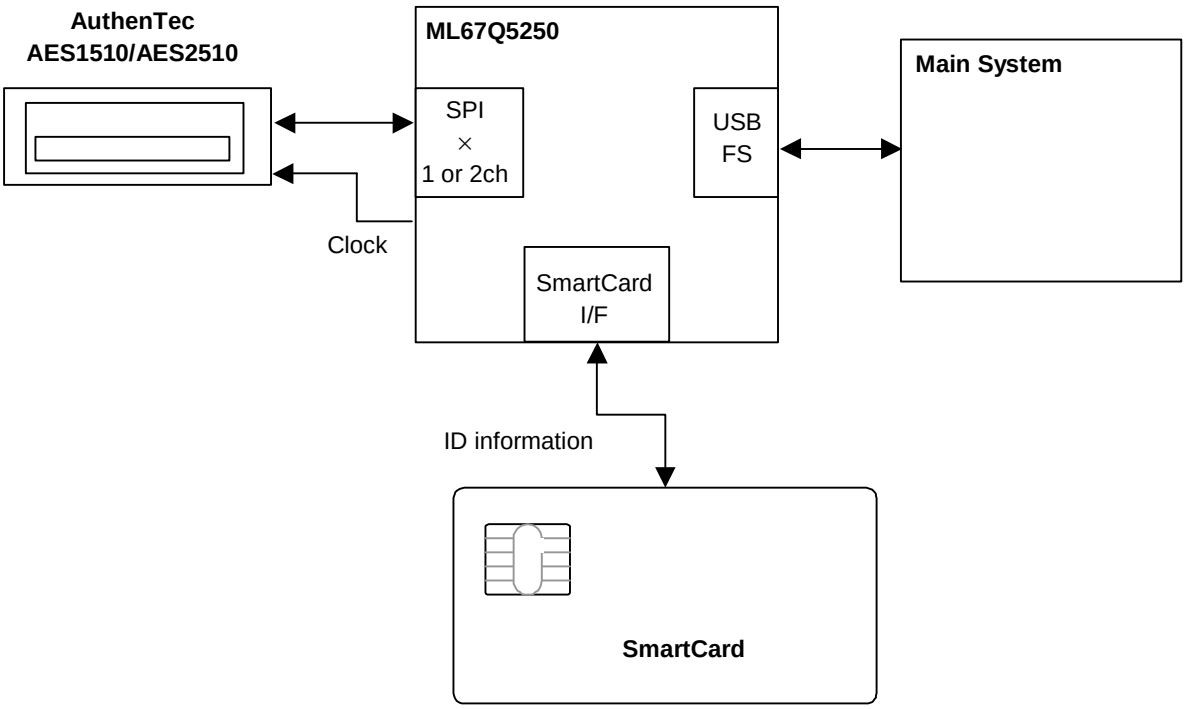
1. VDDCORE, PLLVDD
2. VDDIO

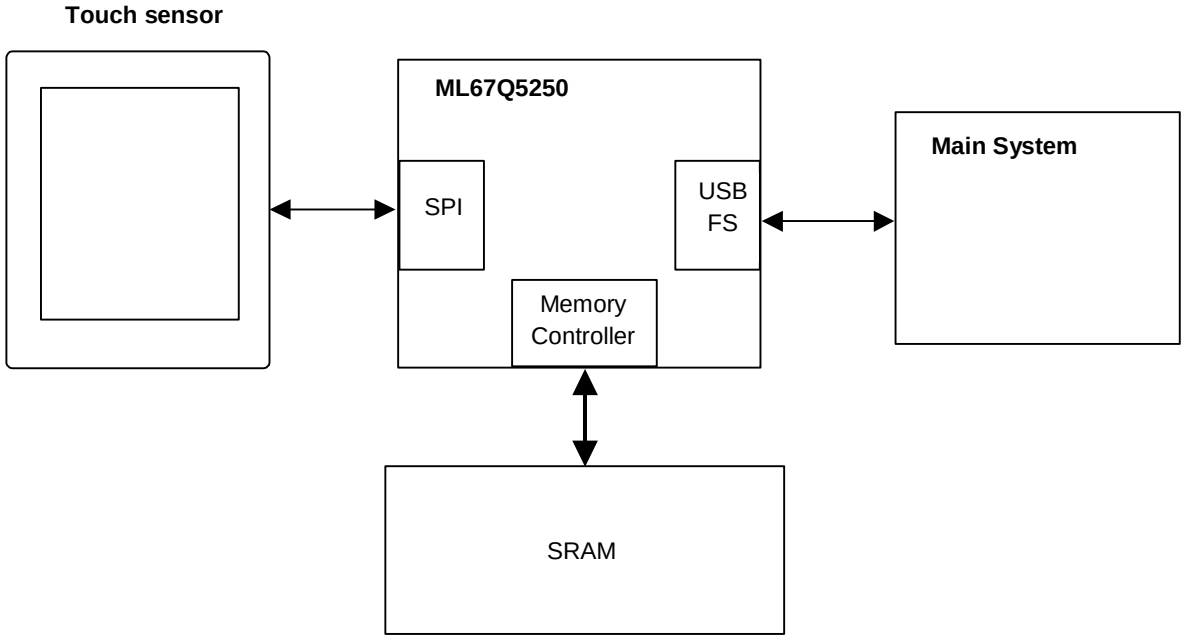
EXAMPLES OF APPLICATION

- Notebook PC
- USB token
etc…



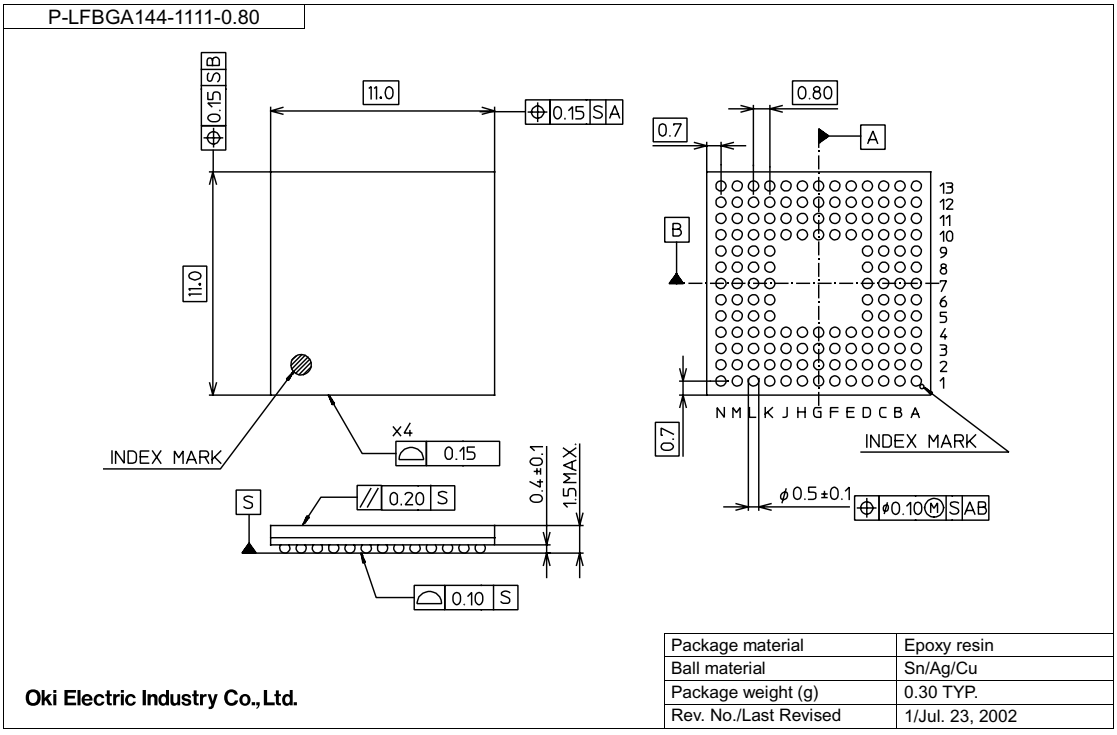
- Gate system
- Printer
etc…




Touch sensor
ML67Q5250
SPI
USB
FS
Memory
Controller
Main System
SRAM

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Ball material	Sn/Ag/Cu
Package weight (g)	0.30 TYP.
Rev. No./Last Revised	1/Jul. 23, 2002

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL67Q5250-1	Nov. 9, 2007	–	–	Preliminary edition 1

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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