ML7037-003

Dual Echo Canceler & Noise Canceler with Dual Codec for Hands-Free

GENERAL DESCRIPTION

The ML7037-003 is an IC device developed for portable, handsfree communication with built-in line echo canceler, acoustic echo canceler, and transmission signal noise canceler. Built-in to the voice signal interface is a PCM CODEC for the analog interface on the acoustic-side, and another PCM CODEC for the analog interface on the line-side. On the line-side, in addition to the analog interface, there is also a μ-law PCM/16-bit linear digital interface.
Equipped with gain and mute controls for data transmission and reception, a μ-law PCM/16-bit linear digital interface for memo recording and message output, and transfer clock and sync clock generators for digital communication, this device is ideally suited for a handsfree system.

FEATURES

• Single 3.3 V Power Supply Operation (3.0 to 3.6 V) [with built-in regulator to generate internal power supply]
• Built-in 2-channel (line and acoustic) echo canceler
  Echo attenuation : 35 dB (typ.) for white noise
  Cancelable echo delay time :
    Single echo canceler mode (only an acoustic echo canceler is enabled)
      Tacoud= 64 ms (max)
    Dual echo canceler mode (both of an acoustic and line echo cancelers are enabled)
      Tacoud = 64 ms Tlined = 20 ms
• Built-in transmission signal noise canceler
  Noise attenuation : 13 dB (typ.) for white noise
• Built-in 2-channel CODEC's
• Analog input gain amp's (Acoustic side = 2 stages; Line-side = 1 stage)
• Analog output configuration: Push-pull drive (can drive a 2.0 kΩ load)
• Receive-side ALC (Auto Level Controler)
• Programmable Gain/Mute
• A slope filter on transmit side
• 16 GPI's and 8 GPO's
• Speech digital interface coding formats : μ-law PCM (G.711 [64kbps]), 16-bit linear (2's complement)
• Speech digital interface sync formats : Long-frame-sync, short-frame-sync
• PCM shift clocks (BCLK)
  Clock slave mode : 64kHz to 2.048MHz (μ-law PCM) / 128kHz to 2.048MHz (16bit Linear PCM)
  Clock master mode : 64kHz (μ-law PCM) / 128kHz (16bit Linear PCM)
• Master clock frequency : 12.288 MHz (crystal unit the ML7037's built-in driving circuit for a crystal unit or a crystal oscillator)
• Transmission signal equalizer
• Package : 64-pin plastic TQFP (TQFP64-P-1010-0.50-K) (ML7037-003TB)

BLOCK DIAGRAM

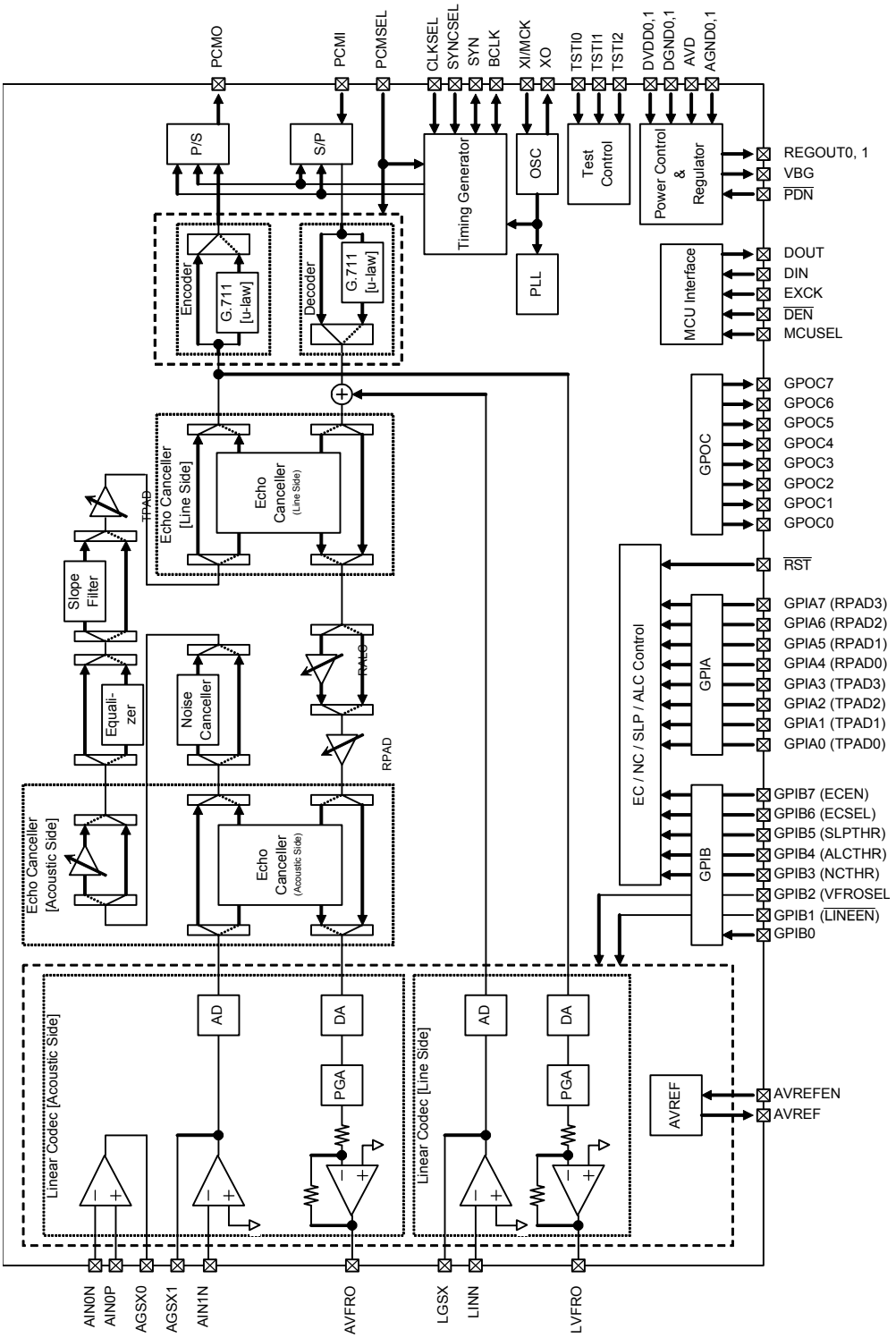


Figure 1

PIN CONFIGURATION (TOP VIEW)

64-Pin Plastic TQFP

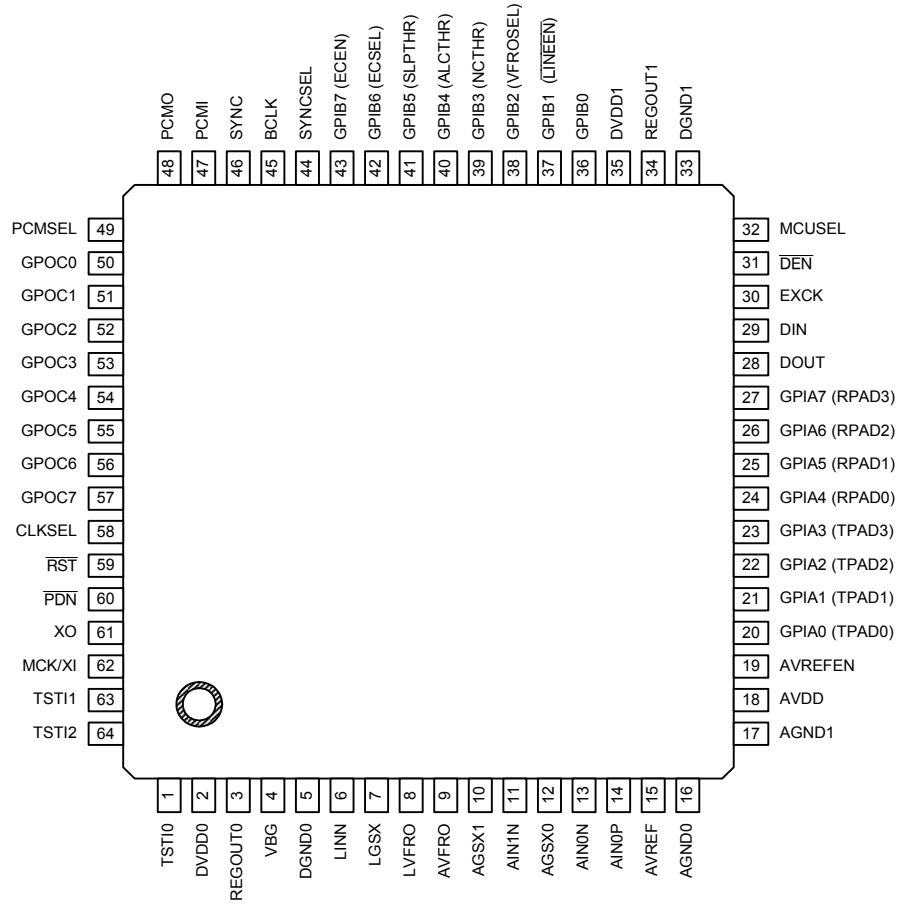


Figure 2

PIN OVERVIEW

Pin Number	Pin Name	I/O	PDN="0"	Descriptions
1	TSTI0	I	I	Test pin0
2	DVDD0	-	-	Digital power supply pin
3	REGOUT0	-	-	Regulatoroutput pin
4	VBG	-	-	Regulatorreference voltage output pin
5	DGND0	-	-	Digital ground pin
6	LINN	I	I	Line-sideanalog input pin (reversed input pin for an analog input amplifier)
7	LGSX	O	Hi-Z	Line-sideanalog output pin (output pin from an analog input amplifier)
8	LVFRO	O	L (*1) 1.4V apporx(*2)	Line-sideanalog output pin
9	AVFRO	O	L (*1) 1.4V apporx(*2)	Acoustic-sideanalog output pin
10	AGSX1	O	Hi-Z	Acoustic-sideanalog output pin (output pin from an analog input amplifier)
11	AIN1N	I	I	Acoustic-sideanalog input pin (reversed input pin for an analog input amplifier)
12	AGSX0	O	Hi-Z	Acoustic-sideanalog output pin (output pin from an analog input amplifier)
13	AIN0N	I	I	Acoustic-sideanalog input pin (reversed input pin for an analog input amplifier)
14	AIN0P	I	I	Acoustic-sideanalog input pin (reversed input pin for an analog input amplifier)
15	AVREF	O	L (*1) 1.4V apporx(*2)	Output pin for analog signal ground level
16	AGND0	-	-	Analog ground pin
17	AGND1	-	-	Analog ground pin
18	AVDD	-	-	Analog power supply pin
19	AVREFEN	I	I	Input pin to switch enabling/disabling AVREF during power-down
20	GPIA0 (TPAD0)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals
21	GPIA1 (TPAD1)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals
22	GPIA2 (TPAD2)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals

（Note）

(*1):Shows the output state when the AVREFEN pin is logic '0'.

(*2):Shows the output state when the AVREFEN pin is logic '1'.

Pin Number	Pin Name	I/O	PDN="0"	Descriptions
23	GPIA3 (TPAD3)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of transmit speech signals
24	GPIA4 (RPAD0)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
25	GPIA5 (RPAD1)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
26	GPIA6 (RPAD2)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
27	GPIA7 (RPAD3)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to tune volume of receive speech signals
28	DOUT	O	Hi-Z	Data output pin for MCU interface
29	DIN	I	I	Data input pin for MCU interface
30	EXCK	I	I	Clock input pin for MCU interface
31	DEN	I	I	Data enable input pin for MCU interface
32	MCUSEL	I	I	Input pin to switch between MCU interface enabled and disabled
33	DGND1	-	-	Digital ground pin
34	REGOUT1	-	-	Regulatoroutput pin
35	DVDD1	-	-	Digital power supply pin
36	GPIB0	I	I	General-purpose input port pin
37	GPIB1 (LINEEN)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to switch between enabling and disabling of line-side analog interface
38	GPIB2 (VFROSEL)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to select output signals from AVFRO/LVFRO
39	GPIB3 (NCTHR)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to select noise canceler mode between normal mode and through mode

Pin Number	Pin Name	I/O	PDN="0"	Descriptions
40	GPIB4 (ALCTHR)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to select ALC mode between normal mode and through mode
41	GPIB5 (SLPTHR)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to select slope filter mode between normal mode and through mode
42	GPIB6 (ECSEL)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to select echo canceler mode between single echo canceler mode and dual echo canceler mode
43	GPIB7 (ECEN)	I	I	General-purpose input port pin ＜Primary function＞ General-purpose input port pin ＜Secondary function＞ Input pin to switch between disabling and enabling echo canceler
44	SYNCSEL	I	I	Input pin to select between long frame sync and short frame sync
45	BCLK	I/O	L (*1) I (*2)	Shift clock input pin for PCM interface
46	SYNC	I/O	L (*1) I (*2)	Sync clock input pin for PCM interface
47	PCMI	I	I	line-side PCM data input pin
48	PCMO	O	Hi-Z	line-side PCMdata output pin
49	PCMSEL	I	I	Input pin to select speech digital interface coding format between 16bit Linear PCM and μ-law PCM
50	GPOC0	O	L	General-purpose output port pin
51	GPOC1	O	L	General-purpose output port pin
52	GPOC2	O	L	General-purpose output port pin
53	GPOC3	O	L	General-purpose output port pin

（Note）
(*1):Shows the output state when the CLKSEL-pin is logic '0'.
(*2):Shows the output state when the CLKSEL-pin is logic '1'.

Pin Number	Pin Name	I/O	PDN="0"	Descriptions
54	GPOC4	O	L	General-purpose output port pin
55	GPOC5	O	L	General-purpose output port pin
56	GPOC6	O	L	General-purpose output port pin
57	GPOC7	O	L	General-purpose output port pin
58	CLKSEL	I	I	Input pin to select between clock slave mode and clock master mode for PCM interface
59	RST	I	I	Reset pin
60	PDN	I	I	Power-down pin
61	XO	O	H	Ouput pin to connect a crystal unit for master clock
62	MCK/XI	I	I	Input pin to connect a crystal unit for master clock Master clock input pin
63	TSTI1	I	I	Test pin1
64	TSTI2	I	I	Test pin2

PIN FUNCTIONAL DESCRIPTION

AIN0N, AIN0P, AGSX0, AIN1N, AGSX1

These are the acoustic analog input and level tuning pins. The AIN0N pin and the AIN1N pin are connected to the inverting input of the internal amp (AMP2、AMP1), and the AIN0P pin is connected to the non-inverting input of the internal amp (AMP2). The AGSX0 pin and the AGSX1 pin are connected to the internal amp (AMP2、AMP1). For the way to tune the level, refer to Figure 3 Analog Interface.

During power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1'), the AGSX0 pin and the AGSX1 pin go to a high impedance state.

(Note) When the acoustic side LSI-internal amplifier (AMP2) is not used, connect the AIN0P pin and the AVREF pin and short the AIN0N pin and the AGSX0 pin.

(Note) Please refer to the application circuit example when the acoustic side LSI-internal amplifier (AMP2) is used as a single-end input.

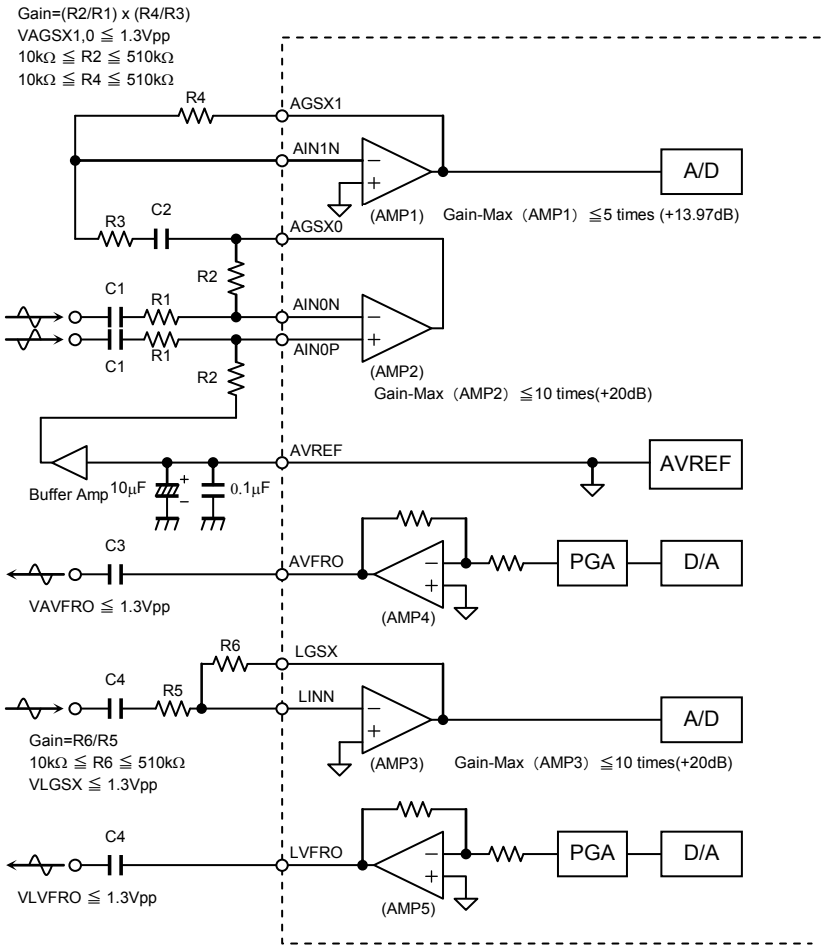


Figure 3 Analog Interface

LINN, LGSX
These are the line analog input and level tuning pins. The LINN pin is connected to the inverting input of the internal amp (AMP3) and the LGSX pin is connected to the output of the amp (AMP3). For level tuning, refer to Figure 3 Analog Interface.
During power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1'), the LGSX pin goes to a high impedance state.

(Note) When the line side analog interface is not used, set the secondary function of the GPIB1 pin (LINEEN) to logic '1' or set the LINEEN-bit [CR0-B5] to '1', and short the LINN pin and the LGSX pin.

AVFRO, LVFRO
These are analog output pins respectively for acoustic-side and line-side. The AVFRO is connected to the output of the internal amp (AMP4), and the LVFRO is connected to the output of the internal amp (AMP5).
The output state of the AVFRO pin and the LVFRO pin can be selected between speech signal output and the AVREF level output (1.4V approx.) by the VFROSEL pin or by the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0]. When the concerned pin or the concerned bit is logic '1', the AVFRO and/or the LVFRO pin outputs speech signals; when the concerned pin and the concerned bit is logic '0', the AVFRO pin and/or the LVFRO pin outputs the AVREF level (1.4V approx.).
During power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1'), if the AVREFEN pin and the AVREFEN-bit [CR16-B7] are logic '0', the AVFRO pin and the LVFRO pin go to a high impedance state; and, if the AVREFEN pin or the AVREFEN-bit [CR16-B7] are logic '1', the pins output 1.4V approx..
(Note) If the AVREFEN pin and the AVREFEN-bit [CR16-B7] are logic '0', pop noises may occur on release and execution of power-down. If the AVREFEN pin and the AVREFEN-bit [CR16-B7] need to be logic '0' and still the pop noises have to be eliminated, it has to be fixed outside of this LSI.
To avoid the pop noises, set the AVREFEN pin or the AVREFEN-bit [CR16-B7] to logic '1' and let the AVREF and the analog output amps alive. Furthermore, the power-down should be released and executed having the output state of the AVFRO pin and the LVFRO pin the AVREF level.
In concrete, the power-down should be released while keeping the VFROSEL pin and by the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0] to logic '0', and then change the VFROSEL pin or the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0] to logic '1'.
And, the VFROSEL pin and the AVFROSEL-bit [CR16-B1] and the LVFROSEL-bit [CR16-B0] should be changed to logic '0' before the power-down execution.
Please note that the power supply current during the power-down would be I_{SS2} compliant (Please refer to the specification under the DC Characteristics to come in a later section.) if the AVREFEN pin or the AVREFEN-bit [CR16-B7] are logic '1'.

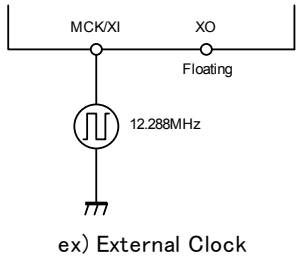
AVREF
This is the output pin for the analog signal ground level. The output voltage is approximately 1.4 V.
Insert a 10 μF bypass capacitor (a tantalum capacitor [recommendation] or an aluminum electrolytic capacitor) and a 0.1 μF capacitor (laminating ceramic type) in parallel between this pin and the AGND0 pin.
During power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') with the AVREFEN pin and the AVREFEN-bit [CR16-B7] to be logic '0', the AVREF pin outputs 0.0V.
During power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') with the AVREFEN pin or the AVREFEN-bit [CR16-B7] to be logic '1', the AVREF pin outputs 1.4V approx..
(Note) If you make use of the AVREF pin output externally in your system, it must be via a buffer amp.

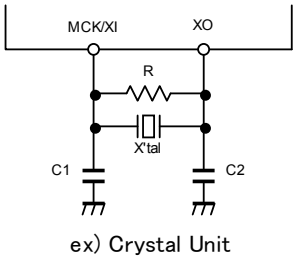
AVREFEN
This is to select disabling and enabling the AVREF output during power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1').
When this is logic '0', the AVREF pin is disabled (power-down state).
When this is logic '1', the AVREF pin is enabled, and the outputs of the AVREF, the AVFRO and the LVFRO become 1.4V approx..
This pin control is valid only during power-down.

GPIB1 (LINEEN)
This is a general-purpose input port pin.
This also works as a power-down control over the line-side analog interface as the secondary function.
When this pin is logic '0', the line-side analog interface is enabled; and, when this pin is logic '1', the line-side analog interface is powered-down (excluding the LVFRO output amp).
During power-down, the LVFRO outputs 1.4V approx..
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB1-bit [GPCR1-B1].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) In an application where the line-side codec is never enabled, the LINN pin and the LGSX pin must be shorted.
(Note) The change of the enabled/disabled state of the line-side codec must be made during power-down state (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

GPIB2 (VFROSEL)
This is a general-purpose input port pin.
This also works as the output state control over the AVFRO pin and the LVFRO pin as the secondary function.
When this pin is logic '0', they output the AVREF level (1.4V apporx.); and, when this pin is logic '1', they output speech signals.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB2-bit [GPCR1-B2].
(Note) When, during a call, the output state is changed or the reset is made, minor noises could happen due to an interruption at an arbitrary point in a sequence of PCM codes so that this output state selection and the reset are recommended to be made before a call as long as it is application-wise allowed.
(Note) The power-down execution and its release are recommended to be made when the AVFRO pin and the LVFRO pin are selected to output the AVREF level.
(Note) When this pin is not used, set this pin to logic '0'.

MCK/X1, XO
These are pins to connect a crystal unit, and the former is used as the master clock input pin as well. The clock frequency is 12.288 MHz.
During power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1'), oscillation of the connected crystal unit is stopped.
After the release of the power-down, the connected crystal unit starts being oscillated, but the master clocks start being utilized within this LSI only after the steady oscillation waiting time (28ms approx.).
Refer to Figure 4 for an example application with an external clock and that with a crystal unit.





X'tal (12.288MHz)	R	C1	C2
HC-49/U-S	1MΩ	10pF	10pF

Figure 4 Examples of external clock and crystal unit as a master clock

(Note) When a crystal unit is used, connect the unit and a feedback resistor of 1MΩ (R) between the MCK/XI and the XO. The appropriate values of capacitors (C1, C2) to be connected between the MCK/XI and GND and between the XO and GND are influenced by load capacitance of a crystal unit and PCB patterns so that they are recommended to be determined by asking a crystal unit vendor for a matching test.

SYNC
This is the 8 kHz sync clcok I/O pin for PCM interface. When the internal clock mode is selected by the CLKSEL pin = logic '0', this pin outputs 8kHz sync clocks synchronizing with the BCLK. When the external clock mode is selected by the CLKSEL pin = logic '1', input 8kHz clocks to this pin in synchronization with the BCLK.
When the SYNCSEL pin is logic '0', this pin outputs/expects to have sync clocks in a long frame sync timing; whereas, when the SYNCSEL pin is logic '1', this pin outputs/expects to have sync clocks in a short frame sync timing.

BCLK
This is the shift clock I/O pin for PCM interface. When the internal clock mode is selected by the CLKSEL pin = logic '0', this pin outputs 64kHz in μ-law PCM mode or 128kHz in 16-bit linear PCM mode. When the external clock mode is selected by the CLKSEL pin = logic '1', input shift clocks to this pin in synchronization with the SYNC. The input frequency must be between 64 kHz and 2048 kHz in μ-law PCM mode and 128 kHz and 2048 kHz in 16-bit linear PCM mode.

CLKSEL
This pin selects internal or external clock modes for PCM interface.
A logic '0' selects the internal clock mode where the SYNC pin and the BCLK pin output clocks so that this LSI could works as a clock master device in your system.
A logic '1' selects the external clock mode where this LSI needs the SYNC and the BCLK externally so that this LSI could works as a clock slave device in your system.
If PCM digital interface is not used, set this pin to a logic '0' to select internal clock mode.
(Note) The change of the input state of this pin must be made during power-down state (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

SYNCSEL
This is the frame sync timing selection pin for PCM interface.
A logic "0" selects long frame sync timing, and a logic "1" selects short frame sync timing.
Refer Figure 5 to Figure8 for the timing.
(Note) The change of the input state of this pin must be made during power-down state (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

PCMSEL
This is the coding format selection pin for PCM interface for the PCMO-pin output and the PCMI-pin input signal.
A logic '0' selects 16-bit linear PCM (2's complement) coding format, and a logic '1' selects μ-law PCM coding format.
The full scale table for both formats are shown below;

16bit Linear PCM (2's complement) Full Scale Table

Level	MSB															LSB
+ Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
+1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
- Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

μ-law PCM Full Scale Table

Level	MSB							LSB
+ Full Scale	1	0	0	0	0	0	0	0
+0	1	1	1	1	1	1	1	1
-0	0	1	1	1	1	1	1	1
- Full Scale	0	0	0	0	0	0	0	0

(Note) If PCM interface is not used, set this pin to a logic '0'.
(Note) The change of the input state of this pin must be made during power-down state (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

PCMI

This is the receive PCM data input pin on the line-side. This input data is shifted at the falling edge of the BCLK. The PCM coding format can be selected between 16-bit linear PCM (2's complement) coding format and μ-law PCM coding format with the PCMSEL pin or the PCMSEL-bit [CR0-B4].

The PCM frame sync timing can be selected between a long frame sync and a short frame sync with the SYNCSEL pin.

Refer Figure 5 to Figure8 for the timing.

(Note) If this pin is not used, set this pin to a logic '0'.

(Note) The change of the input state of this pin must be made during power-down state (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.

PCMO

This is the receive PCM data output pin on the line-side. This output data is shifted at the rising edge of the BCLK. During power-down mode (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') and initial mode or while effective PCM data bits are not being output, this pin goes to a high impedance state.

The PCM coding format can be selected between 16-bit linear PCM (2's complement) coding format and μ-law PCM coding format with the PCMSEL pin or the PCMSEL-bit [CR0-B4].

The PCM frame sync timing can be selected between a long frame sync and a short frame sync with the SYNCSEL pin.

Refer Figure 5 to Figure8 for the timing.

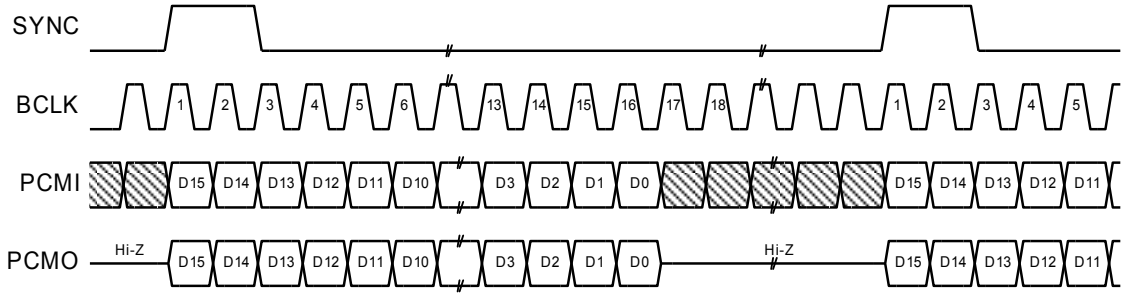


Figure 5 16-bit linear PCM timing chart (long frame sync)

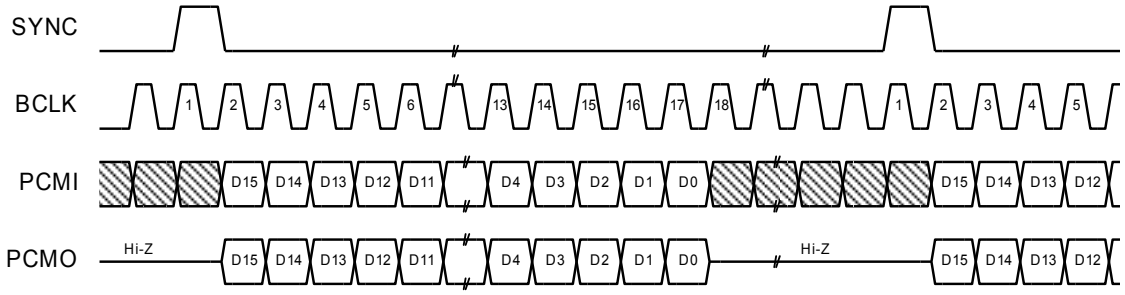


Figure 6 16-bit linear PCM timing chart (short frame sync)

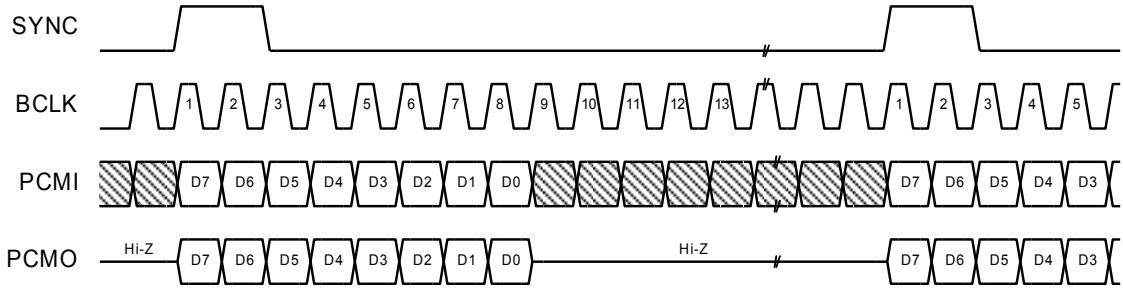


Figure 7 μ-law PCM timing chart (long frame sync)

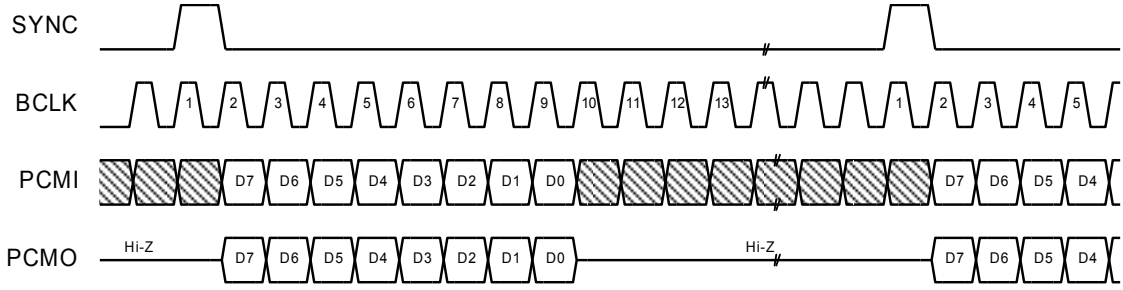


Figure 8 μ-law PCM timing chart (short frame sync)

GPIB3 (NCTHR)
This is a general-purpose input port pin.
This also works as a through-mode control pin over the noise canceller as the secondary function.
A logic '0' enables the noise canceller, and a logic '1' disables the noise canceller and the speech data by-passes the noise canceller.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB3-bit [GPCR1-B3].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) For 24ms approx. after the state change from a noise canceller enabling mode to a through-mode, the speech signals may not be ordinarily processed and be got mute or attenuated. The state change, if needed, is recommended to be made before a call.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB4 (ALCTHR)
This is a general-purpose input port pin.
This also works as a through-mode control pin over the automatic level controller (ALC) as the secondary function.
A logic '0' enables the ALC, and a logic '1' disables the ALC and the speech data by-passes the ALC.
The ALC is a function to mainly aim to absorb the difference in speech volume with handsets to connect to a hands-free. For the functional details, please refer to descriptions under the RALCTHR-bit [CR2-B4].
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB4-bit [GPCR1-B4].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB5 (SLPTHR)
This is a general-purpose input port pin.
This also works as a through-mode control pin over the slope filter as the secondary function.
A logic '0' enables the slope filter, and a logic '1' disables the slope filter and the speech data by-passes the slope filter.
The slope filter has frequency characteristics to suppress low frequency range and gain high frequency range so that it helps to relax near-end ambient noises usually dominant in low frequency range and to emphasize speech consonants mostly dominant in high frequency range. For the functional details, please refer to the slope filter characteristics under Reference Data.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB5-bit [GPCR1-B5].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB6 (ECSEL)
This is a general-purpose input port pin.
This also works as an echo canceller selection as the secondary function.
A logic '0' selects single echo canceller mode (enables only acoustic echo canceller), and a logic '1' selects dual echo canceller mode (enables both of acoustic and line echo cancellers).
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB6-bit [GPCR1-B6].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) The single echo canceller mode should be selected in an environment where no line echoes exist.
(Note) The change of the input state of this pin must be made during power-down state (PDN pin = logic '0' or SPDN-bit [CR0-B7] = '1') or during initial mode.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIB7 (ECEN)
This is a general-purpose input port pin.
This also works as an enabling/disabling selection for echo cancellers as the secondary function.
A logic '0' disables echo cancellers and their auxiliary functions (ATTrA/ATTrL, ASIPAD/LPAL, ASOPAD/LSOPAD, ATTsA/ATTrA, Center Clip), and a logic '1' enables them.
When the MCUSEL pin is logic '1', this pin is automatically assigned with its secondary function.
When the MCUSEL pin is logic '0', this pin's function assignment follows the state of GPFB7-bit [GPCR1-B7].
(Note) The change of the input state to this pin is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) If this pin is not used, set this pin to a logic '0'.

GPIA0 (TPAD0), GPIA1 (TPAD1), GPIA2 (TPAD2), GPIA3 (TPAD3)
These are general-purpose input port pins.
These also work as transmit-side volume control as the secondary function.
For the setting, please refer to Table 1.
When the MCUSEL pin is logic '1', these pins are automatically assigned with their secondary function.
When the MCUSEL pin is logic '0', these pins' function assignment follows the state of GPFA3-0-bits [GPCR0-B3,2,1,0].
(Note) The change of the input state these pins is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) If these pins are not used, set them to a logic '0'.

GPIA4(RPAD0), GPIA5(RPAD1), GPIA6(RPAD2), GPIA7(RPAD3)
These are general-purpose input port pins.
These also work as receive-side volume control as the secondary function.
For the setting, please refer to Table 1.
When the MCUSEL pin is logic '1', these pins are automatically assigned with their secondary function.
When the MCUSEL pin is logic '0', these pins' function assignment follows the state of GPFA7-4-bits [GPCR0-B7,6,5,4].
(Note) The change of the input state to these pins is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) If these pins are not used, set them to a logic '0'.

Table 1 Receive-/Transmit-Side Volume Control

GPIA7 (RPAD3)	GPIA6 (RPAD2)	GPIA5 (RPAD1)	GPIA4 (RPAD0)	GPIA3 (TPAD3)	GPIA2 (TPAD2)	GPIA1 (TPAD1)	GPIA0 (TPAD0)	Level
0	1	1	1	0	1	1	1	+21dB
0	1	1	0	0	1	1	0	+18dB
0	1	0	1	0	1	0	1	+15dB
0	1	0	0	0	1	0	0	+12dB
0	0	1	1	0	0	1	1	+9dB
0	0	1	0	0	0	1	0	+6dB
0	0	0	1	0	0	0	1	+3dB
0	0	0	0	0	0	0	0	0dB
1	1	1	1	1	1	1	1	-3dB
1	1	1	0	1	1	1	0	-6dB
1	1	0	1	1	1	0	1	-9dB
1	1	0	0	1	1	0	0	-12dB
1	0	1	1	1	0	1	1	-15dB
1	0	1	0	1	0	1	0	-18dB
1	0	0	1	1	0	0	1	-21dB
1	0	0	0	1	0	0	0	MUTE

MCUSEL
This pin selects whether the microcontroller interface is used or unused.
When the microcontroller interface is used, set this pin to a logic '0'.
When the microcontroller interface is not used, set this pin to a logic "1".
A logic '1' with this pin automatically determines general-purpose input port pins to work as their secondary functions.
This pin is OR'ed with OPE_STAT-bit [CR0-B0].
Refer to NOTE ON USE.

DEN, EXCK, DIN, DOUT
These are serial control ports for the microcontroller interface.
This LSI has 32 bytes control registers, and the data read and write between the registers and the microcontroller are made via these pins.
The DEN pin is a data read/write enabling signal input pin, the EXCK pin is a clock signal input pin for data shifting, the DIN pin is an address and data input pin, the DOUT pin is a data output pin. If the mirrocontroller interface is not used, set the DEN pin to a logic "1", the EXCK pin and DIN pins to a logic "0", and the MCUSEL pin to logic '1'.
Figure 9-12 shows the input/output timing.

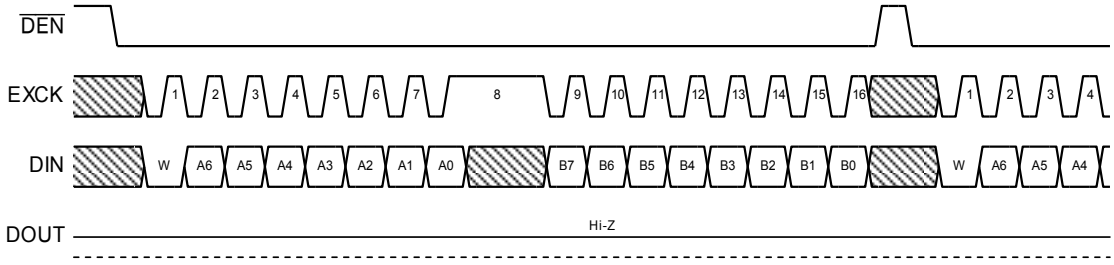


Figure 9 MCU Interface Input/Output Timing (Data Write with 8-bit MCU)

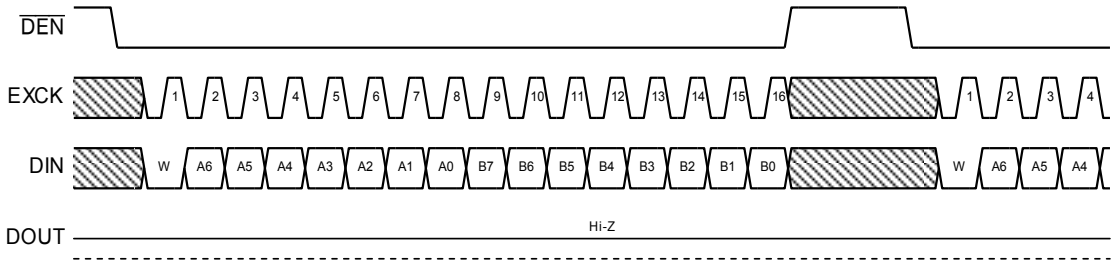


Figure 10 MCU Interface Input/Output Timing (Data Write with 16-bit MCU)

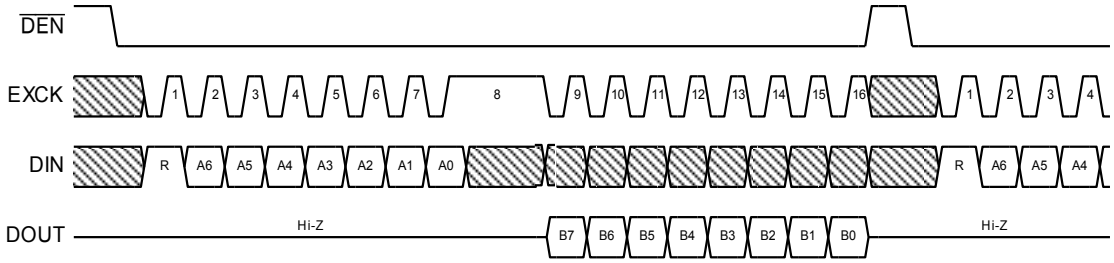


Figure 11 MCU Interface Input/Output Timing (Data Read with 8-bit MCU)

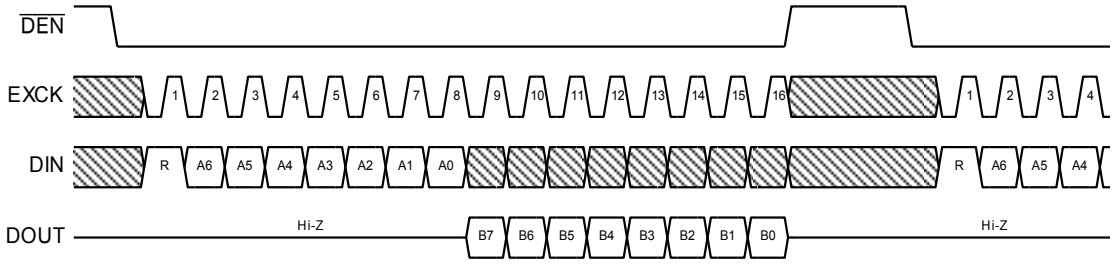


Figure 12 MCU Interface Input/Output Timing (Data Read with 16-bit MCU)

GPIB0
This is a general-purpose input port pin.
(Note) If this pin is not used, set this pin to a logic '0'.

GPOC0, GPOC1, GPOC2, GPOC3, GPOC4, GPOC5, GPOC6, GPOC7
These are general-purpose output port pins.
(Note) If these pins are not used, leave these pins floating.

DVDD0, DVDD1, AVDD
These are power supply pins. The DVDD0 and the DVDD1 are connected to digital circuits and the AVDD is connected to analog circuits in this LSI via the built-in regulator.
Connect them common in the shortest distance, and insert a 10 μF bypass capacitor (a tantalum capacitor [recommendation] or an aluminum electrolytic capacitor) and a 0.1 μF capacitor (laminating ceramic type) in parallel between these pins and the DGND0, 1 pins and the AGND0, 1 pins respectively.

DGND0, DGND1, AGND0, AGND1
These are ground pins. The DGND0 pin and the DGND1 pin are connected to the ground of digital circuits in this LSI. The AGND0 pin and the AGND1 pin are connected to the ground of analog circuits in this LSI. Connect them common in the shortest distance

REGOUT0, REGOUT 1
These are the built-in regulator output pins (2.6V approx.).
Insert a 10 μF capacitor (a tantalum capacitor [recommendation] or an aluminum electrolytic capacitor) and a 0.1 μF capacitor (laminating ceramic type) in parallel between the REGOUT0 pin and the DGND0 pin.
Insert a 0.1 μF capacitor (laminating ceramic type) in parallel between the REGOUT1 pin and the DGND1 pin.

VBG
This is an output pin for a reference voltage of the built-in regulator (1.2V approx.).
Insert a 150 pF (approx.) laminating ceramic capacitor between the this pin and the DGND0.

PDN
This is the power-down reset control input pin.
A logic '0' executes the power-down reset.
When a logic '1' is input to this pin, this LSI is in a normal operation.
This execution also initializes all of this LSI including the control registers, the internal data memories, the filter coefficients of the echo cancellers and those of the noise cancellers.
(Note) The negative logic of this pin is ORed with the SPDN-bit [CR0-B7].
(Note) To avoid unstable operations, right after the power-up, execute the power-down rest with this pin (not with the SPDN-bit [CR0-B7]). The master clock input to the XI pin and the REGOUT output higher than 90% of the normal state are prerequisite to secure the power-down reset.
(Note) When an ORed logic of the AVREFEN pin and the AVREFEN-bit [CR16-B7] are logic '1', the AVREF and analog output amps keep powered up even during the power-down state.

RST
This is an input pin to initialize the filter coefficients of the echo cancellers and the noise canceller and the ALC acquired gain..
A logic '0' executes the initialization. For a normal operation, give this pin a logic '1'.
During the reset state, no speech signals are output. Control registers are preserved.
Execute the initialization in cases where the echo path changes (due to line switching during a telephone conversation, etc.), or for another call.
(Note) The negative logic of this pin is ORed with the RST-bit [CR0-B6].
(Note) The change of the input state to these pins is detected at the rising edge of the SYNC clock so that the change of the input state to this pin less than 250 μs may not be reflected as the LSI behavior.
(Note) The execution of this reset during a call may cause minor noises due to interruption at an arbitrary point in a sequence of PCM codes so that an execution of the reset is recommended to be made in a silent state.

TSTI0, TSTI1, TSTI2
These are LSI manufacturer's test input pins. Set these pins to a logic "0".

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Analog power supply voltage	AV_{DD}	—	–0.3 to +4.6	V
Digital power supply voltage	DV_{DD}	—	–0.3 to +4.6	V
Input voltage	V_{AIN}	Analog pins	–0.3 to AV_{DD}+0.3	V
	V_{DIN}	Digital pins	–0.3 to DV_{DD}+0.3	V
Short-circuit output current	I_{OS}	—	–20 to +20	mA
Power dissipation	P_D	Ta = 85 °C, per package	350	mW
Storage Temperature	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITION (1)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog power supply voltage (*1)	AV_{DD}	AVDD	3.0	3.3	3.6	V
Digital power supply voltage (*1)	DV_{DD}	DVDD0, DVDD1	3.0	3.3	3.6	V
Operating temperature	T_a	—	-40	—	85	°C
High-level input voltage	V_{IH1}	MCK/XI	DVDD x 0.75	—	DVDD + 0.3	V
	V_{IH2}	Normal digital pins	DVDD x 0.75	—	DVDD + 0.3	V
Low-level input voltage	V_{IL1}	MCK/XI	0.0	—	DVDD x 0.19	V
	V_{IL2}	Normal digital pins	0.0	—	DVDD x 0.19	V
Digital input rise time	t_{IR}	Digital pins	-	2	20	ns
Digital input fall time	t_{IF}	Digital pins	-	2	20	ns
Master clock frequency	f_{MCK}	MCK/XI	12.2867712 (-0.01%)	12.288	12.2892288 (+0.01%)	MHz
Master Clock Duty Ratio	d_{MCK}	MCK/XI	40	50	60	%

Note

*1 Turn on and off the analog power supply and digital power supply simultaneously, or turn on digital power supply prior to analog power supply and turn off analog power supply prior to digital power supply.

RECOMMENDED OPERATING CONDITION (2)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit clock frequency	f_{BCLK1}	BCLK (*1) μ-law PCM	64	—-	2048	kHz
	f_{BCLK2}	BCLK (*1) 16bit Linear PCM	128	—	2048	KHz
Bit clock duty ratio	d_{BCLK}	BCLK (*1)	40	50	60	%
Synchronous Signal Frequency	f_{SYNC}	SYNC (*1)	7.992 (-0.1%)	8.0	8.008 (+0.1%)	kHz
Synchronous Signal Width	f_{WS}	SYNC (*1)	1BCLK	—	100	μs
Transmit/Receive Sync Signal Setting Time	t_{BS}	BCLK to SYNC (*1)	100	—	—	ns
	t_{SB}	SYNC to BCLK (*1)	100	—	—-	ns
Digital output load resistance	C_{DL}	Digital pins	—	—	50	pF
Bypass capacitor for AVREF	C_{AVREF}	AVREF - AGND0	—	10+0.1	—	μF
Bypass capacitor for VBG	C_{VBG}	VBG-DGND0	—	150	—	pF
Bypass capacitor for REGOUT	$C_{REGOUT1}$	REGOUT0-DGND0	—	10+0.1	—	μF
	$C_{REGOUT2}$	REGOUT1-DGND1	—	0.1	—	μF

Note
*1 In external clock mode (CLKSEL = logic “1’)

ELECTRICAL CHARACTERISTICS

DC Characteristics

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{SS1}	Stand-by state (1) PDN="0", AVREFEN="0", AVDD=DVDD0,1=3.30V	—	100	500	μA
	I_{SS2}	Stand-by state (2) PDN="0", AVREFEN="1", AVDD=DVDD0,1=3.30V	—	3.5	7.0	mA
	I_{DD1}	Operating state MCK/XI, XO 12.288MHz crystal connected Inpu signal : none AVDD=DVDD0,1=3.30V, T_a=25°C	—	50	60	mA
Digital input pin input leak current	I_{IH1}	V_{IN}=DVDD	—	0.02	10	μA
	I_{IL1}	V_{IN}=0.0V	-10	-0.02	—	μA
Digital I/O pin input leak current	I_{OZH}	V_{IN}=DVDD	—	0.02	10	μA
	I_{OZL}	V_{IN}=0.0V	-10	-0.02	—	μA
High-level output voltage	V_{OH1}	Digital output pins Digital I/O pins I_{OH}=4.0mA	0.78 x DVDD	—	—	V
	V_{OH2}	XO pin I_{OH}=0.5mA	0.78 x DVDD	—	—	V
Low-level output voltage	V_{OL1}	Digital output pins Digital I/O pins I_{OL}=-4.0mA	—	—	0.4	V
	V_{OL2}	XO pin I_{OL}=-0.5mA	—	—	0.4	V
Input capacitance	C_{IN}	Input pins, I/O pins	—	6.0	—	pF

Analog Interface

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input resistance	R_{IN}	Analog input pins (*2)	10	—	—	MΩ
Output load resistance	R_{L1}	AGSX0, AGSX1, LGSX	10	—	—	kΩ
	R_{L2}	AVFRO, LVFRO	2	—	—	kΩ
Output load capacitance	C_L	Analog output pins (*3)	—	—	50	pF
Offset voltage	V_{OF}	Analog output pins (*3)	-40	—	40	mV
Output voltage level (*1)	V_O	LVFRO, AVFRO RL=10kΩ, Input=+3dBm0	1.158	1.3	1.458	V_{PP}

Note

*1 -7.7dBm(600Ω)=0dBm0, +3dBm0=1.3Vpp

*2 Analog input pins (AIN0P, AIN0N, AIN1N, LINN)

*3 Analog output pins (AGSX0, AGSX1, LGSX, AVFRO, LVFRO)

PDN, XO, AVREF Timing

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AVDD supply start delay time	t_{AVDDS}	AVDD	0	—	—	ns
DVDD supply cease delay time	t_{DVDDE}	DVDD0,1	0	—	—	ns
Power-down reset start latency	t_{RSTS}	PDN	—	—	100	ns
Power-dwon reset signal pulse width	t_{RSTW}		1.0	—	—	µs
Power-down reset release latency	t_{RSTE}		—	—	250	ms
Oscillation activation time	t_{SXO}	crystal unit (*1)	—	—	28	ms

Note

*1 Crystal unit (HC-49/U-S), R=1MΩ, C1=C2=10pF

Timing Chart (PDN, XO, AVREF timing)

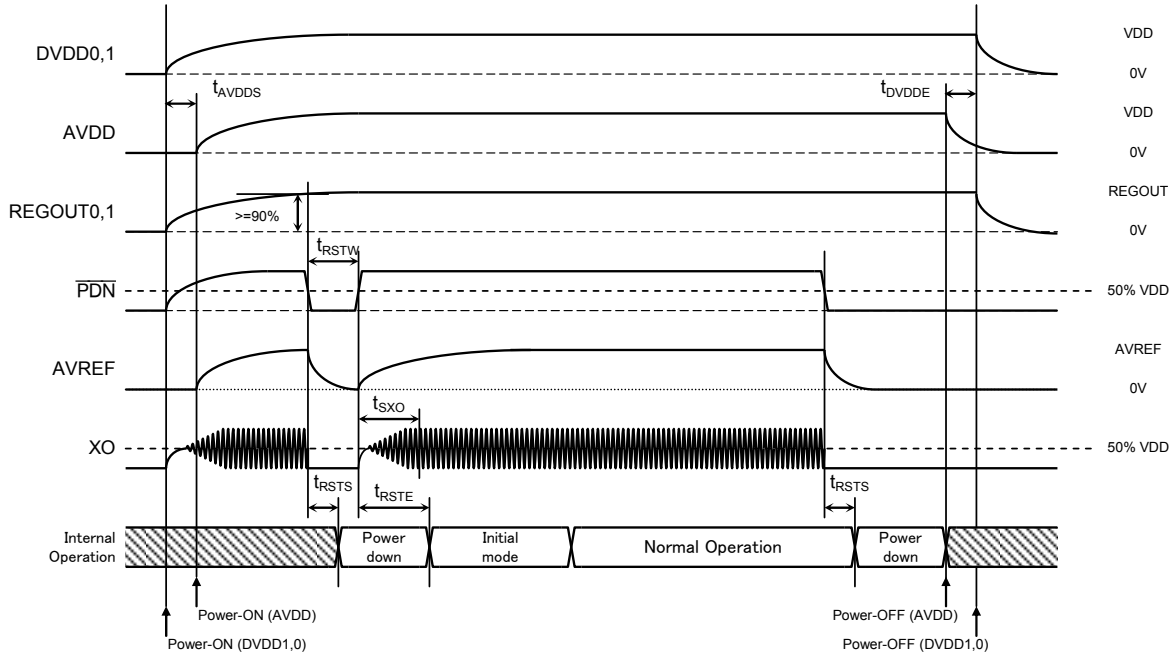


Figure 13 PDN, XO, AVREF Timing

Digital Interface (Pin control, general port timing)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Pin control latency (Low to High)	t_{PARD}	*1	—	—	250	µs
Pin control pulse width	t_{PARW}		250	—	—	µs
Pin control latency (High to Low)	t_{PARH}		—	—	250	µs
General purpose output port output delay time	t_{GPOD}	*2	—	—	100	ns
General output port hold time	t_{GPOH}		—	—	100	ns

Note

*1 GPIA7-4 (RPAD3-0), GPIA3-0 (TPAD3-0), GPIB7 (ECEN), GPIB6 (ECSEL), GPIB5 (SLPTHR), GPIB4 (ALCTHR), GPIB3 (NCTHR), GPIB2 (VFROSEL), GPIB1 (LINEEN), GPIB0, RST, PCMSEL, CLKSEL

*2 GPOC7-0

Timing Chart (Pin Control, General Ports)

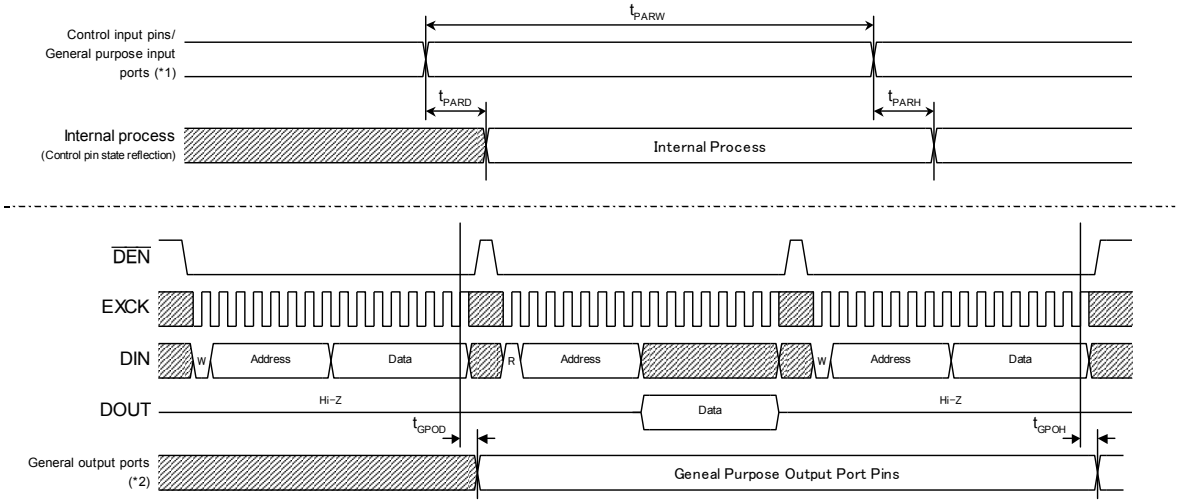


Figure 14 Control Input Pin and General Purpose Output Port Pin Timing

PCM Interface

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit clock frequency	f_{BCLK1}	μ-law PCM mode (*1, *2, *3)	63.36	64	64.64	kHz
	f_{BCLK2}	16bit Linear PCM mode (*1, *2, *3)	126.72	128	129.28	kHz
Bit clock duty ratio	d_{BCLK}	(*1, *2, *3)	40	50	60	%
Sync signal frequency	f_{SYNC}	(*1, *2, *3)	7.92	8.0	8.08	kHz
Sync signal duty ratio	d_{SYNC1}	μ-law PCM mode (*1, *2, *3) Long frame sync mode (*1, *2, *3)	24.85	25	25.15	%
	d_{SYNC2}	16bit Linear PCM mode Long frame sync mode (*1, *2, *3)	12.35	12.5	12.65	%
	d_{SYNC3}	μ-law PCM mode (*1, *2, *3) Short frame sync mode (*1, *2, *3)	12.35	12.5	12.65	%
	d_{SYNC4}	16bit Linear PCM mode Short frame sync mode (*1, *2, *3)	6.10	6.25	6.40	%
Transmit/Receive Sync signal timing	t_{SB}	SYNC to BCLK (*3)	100	—	—	ns
	t_{BS}	BCLK to SYNC (*3)	100	—	—	ns
Input setup time	t_{DS}	—	100	—	—	ns
Input hold time	t_{DH}	—	100	—	—	ns
Digital output delay time	t_{SDX}	C_{DL}=50pF	—	—	100	ns
	t_{XD1}	C_{DL}=50pF	—	—	100	ns
Digital output hold time	t_{XD2}	C_{DL}=50pF	—	—	100	ns
	t_{XD3}	C_{DL}=50pF	—	—	100	ns

Note
*1 C_{DL}=20pF
*2 MCK/XI=12.288MHz
*3 In internal clock mode (CLKSEL = logic “0’)

Timing Chart (PCM Interface)

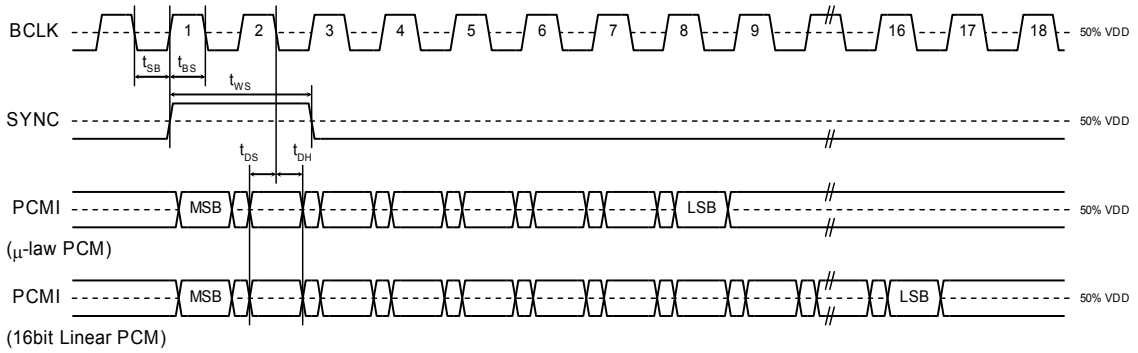


Figure 15 PCM Input Timing (Long Frame Sync)

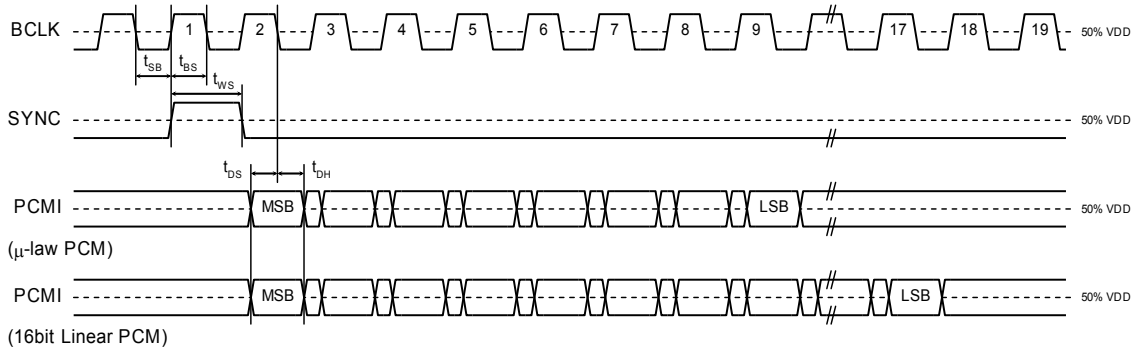


Figure 16 PCM Input Timing (Short Frame Sync)

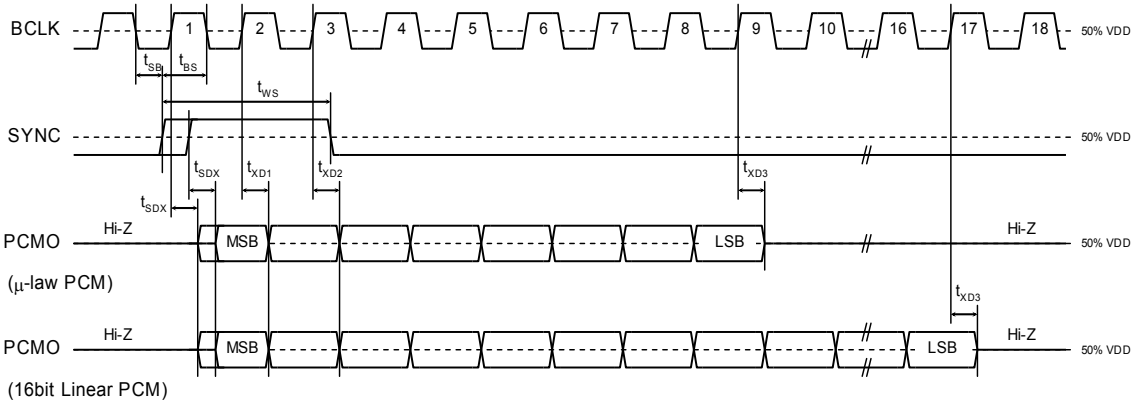


Figure 17 PCM Output Timing (Long Frame Sync)

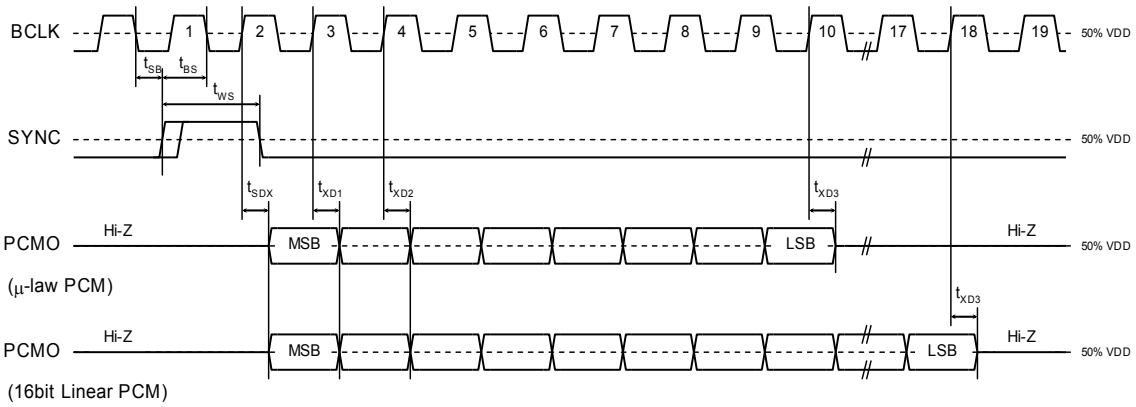


Figure 18 PCM Output Timing (Short Frame Sync)

Microcontroller Interface (Serial Interface)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital input/output timing	t_{M1}	C_{DL}=50pF	20	—	—	ns
	t_{M2}		20	—	—	ns
	t_{M3}		50	—	—	ns
	t_{M4}		100	—	—	ns
	t_{M5}		50	—	—	ns
	t_{M6}		50	—	—	ns
	t_{M7}		—	—	30	ns
	t_{M8}		0	—	—	ns
	t_{M9}		50	—	—	ns
	t_{M10}		—	—	30	ns
	t_{M11}		100	—	—	ns
EXCK clock frequency	f_{EXCK}	—	—	—	10	MHz

Timing Chart (Microcontroller Serial Interface)

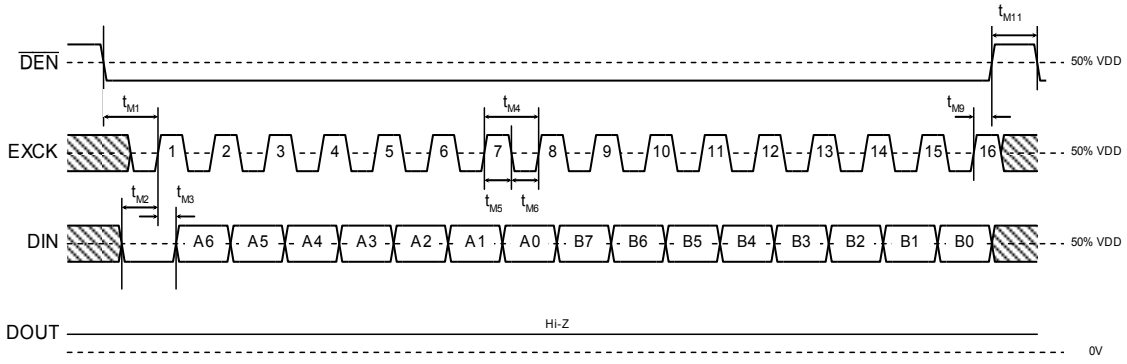


Figure 19 Write Timing

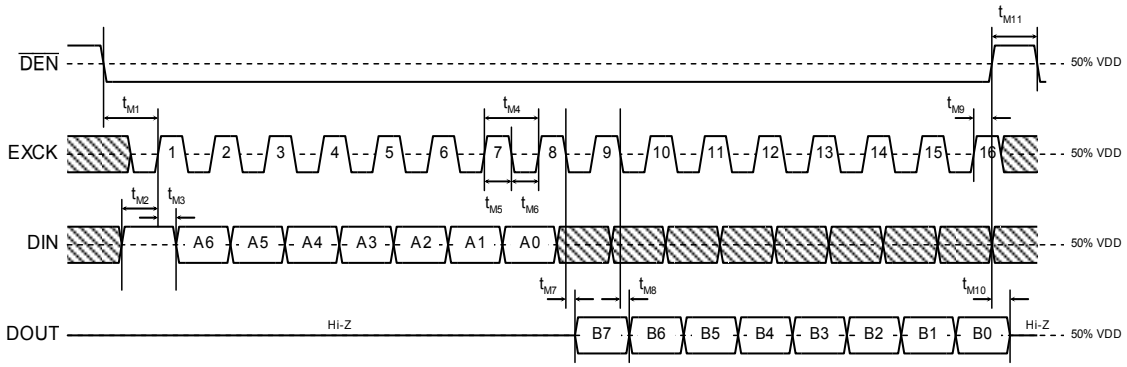


Figure 20 Read Timing

AC Characteristics (Codec Characteristics)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)	Others				
Transmit frequency response	LossT1	0 to 60	0	*1, *2	25	—	—	dB
	LossT2	300 to 3000			-0.15	—	0.25	dB
	LossT3	1020			Reference			—
	LossT4	3300			-0.15	—	0.8	dB
	LossT5	3400			0	—	0.8	dB
	LossT6	3968.75			13	—	-	dB
Receive frequency response	LossR1	0 to 3000	0	*1, *2	-0.15	—	0.2	dB
	LossR2	1020			Reference			—
	LossR3	3300			-0.15	—	0.8	dB
	LossR4	3400			-0.15	—	0.8	dB
	LossR5	3968.75			13	—	—	dB
Transmit signal to distortion ratio	SDT1	1020	+3	*1, *2, *3	35	—	—	dB
	SDT2		0		35	—	—	dB
	SDT3		-30		35	—	—	dB
	SDT4		-40		28	—	—	dB
	SDT5		-45		23	—	—	dB
Receive signal to distortion ratio	SDR1	1020	+3	*1, *2, *3	35	—	—	dB
	SDR2		0		35	—	—	dB
	SDR3		-30		35	—	—	dB
	SDR4		-40		28	—	—	dB
	SDR5		-45		23	—	—	dB
Transmit gain tracking	GTT1	1020	+3	*1, *2, *3	-0.2	—	0.2	dB
	GTT2		-10		Reference			—
	GTT3		-40		-0.2	—	0.2	dB
	GTT4		-50		-0.5	—	0.5	dB
	GTT5		-55		-1.2	—	1.2	dB
Receive gain tracking	GTR1	1020	+3	*1, *2, *3	-0.2	—	0.2	dB
	GTR2		-10		Reference			—
	GTR3		-40		-0.2	—	0.2	dB
	GTR4		-50		-0.5	—	0.5	dB
	GTR5		-55		-1.2	—	1.2	dB
Idle channel noise	$N_{IDL}T$	—	—	*1, *2, *3 *5	—	—	-68	dBm0p
	$N_{IDL}R$	—	—		—	—	-72	dBm0p
Absolute signal level (*4)	AVT	1020	0	*1, *2	0.285	0.32	0.359	Vrms
	AVR		0		0.285	0.32	0.359	Vrms

Note

*1 Echo cancellers, Noise canceller, slope filter, ALC = off
Programmable gain = 0dB

*2 Analog and digital gain = 1

*3 with a psophometric filter

*4 0.32Vrms = 0dBm0 = -7.7dBm (600Ω)

*5 Input signals = Idle pattern

AC Characteristics (Programmable Gain Characteristics)

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Receive gain accuracy	G_{AC1}	against a set gain (*1)	-1.0	—	+1.0	dB
	G_{AC2}	against an adjacent gain step (*2)	-1.0	—	+1.0	dB

Note *1 TPAD, RPAD

*2 Acoustic-side PGA's（Programmable Gain Amp's）, Line-side PGA

Noise Canceller Characteristics

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Noise attenuation	N_{RES}	with white noise for voice band noise attenuation setting = default	—	13	—	dB

[Measurement System Block Diagram]

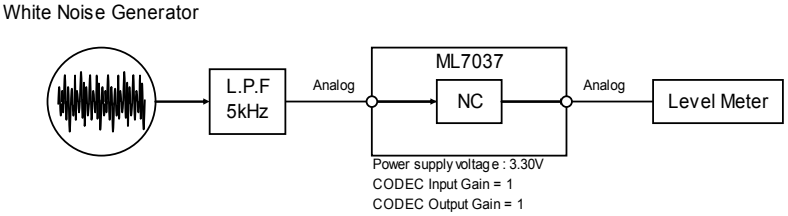


Figure 21 Measurements (Noise Attenuation)

Echo Canceller Characteristics

DVDD0,1=3.00V to 3.60V, AVDD=3.00V to 3.60V, DGND0,1=0.0V, AGND0,1=0.0V, Ta=-40°C to +85°C (otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo attenuation	E_{RES}	Acoustic-side, Line-side *3 (Analog interface or 16bit Linear PCM mode)	—	35	—	dB
		Line-side (μ-law PCM mode)	—	30	—	dB
Cancellable echo delay time	T_{ACOUD}	Acoustic-side	—	—	64	ms
	T_{LINED}	Line-side *3	—	—	20	ms

Note *3 Only in dual echo canceller mode

[Measurement System Block Diagram]

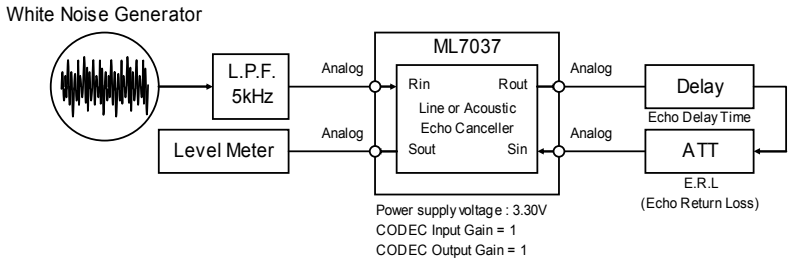


Figure 22 Measurements (Echo Attenuation)

FUNCTIONAL DESCRIPTION

Control Register

The control register map and the general-purpose port control register map are shown as Table 2 and Table3 respectively.

Table 2-1 Control Register Map

Register Name	Address	Data								R/W
		B7	B6	B5	B4	B3	B2	B1	B0	
CR0	00h	SPDN	RST	LINEEN	PCMSEL	CLKEN	PCMEN	ECSEL	OPE_STAT (MCUSEL)	R/W
		/E	/E	I/	I/	I/	I/	I/	I/	
CR1	01h	DMWR	#	#	#	#	#	#	#	R/W
		I/E	-	-	-	-	-	-	-	
CR2	02h	#	#	#	RALCTHR	RPAD3	RPAD2	RPAD1	RPAD0	R/W
		-	-	-	I/E	I/E	I/E	I/E	I/E	
CR3	03h	#	#	#	#	TPAD3	TPAD2	TPAD1	TPAD0	R/W
		-	-	-	-	I/E	I/E	I/E	I/E	
CR4	04h	#	#	#	APGA4	APGA3	APGA2	APGA1	APGA0	R/W
		-	-	-	I/E	I/E	I/E	I/E	I/E	
CR5	05h	#	#	#	LPGA4	LPGA3	LPGA2	LPGA1	LPGA0	R/W
		-	-	-	I/E	I/E	I/E	I/E	I/E	
CR6	06h	A15	A14	A13	A12	A11	A10	A9	A8	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR7	07h	A7	A6	A5	A4	A3	A2	A1	A0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR8	08h	D15	D14	D13	D12	D11	D10	D9	D8	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR9	09h	D7	D6	D5	D4	D3	D2	D1	D0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR10	0Ah	READY	#	#	#	#	#	#	#	R/
		-	-	-	-	-	-	-	-	
CR11	0Bh	LTHR	LECEN	LHLD	#	LCLP	LSLC	LATT	#	R/W
		I/E	I/E	I/E	-	I/E	I/	I/E	-	
CR12	0Ch	ATHR	AECEN	AHLD	#	ACLP	ASLC	AATT	#	R/W
		I/E	I/E	I/E	-	I/E	I/	I/E	-	
CR13	0Dh	ASOPAD1	ASOPAD0	ASIPAD1	ASIPAD0	LSOPAD1	LSOPAD0	LSIPAD1	LSIPAD0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR14	0Eh	SLPTHR	#	#	#	NCTHR	#	#	#	R/W
		I/E	-	-	-	I/E	-	-	-	

Table 2-2 Control Register Map

Register Name	Address	Data								R/W
		B7	B6	B5	B4	B3	B2	B1	B0	
CR15	0Fh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR16	10h	AVREFEN	#	#	#	#	#	AVFROSEL	LVFROSEL	R/W
		I/E	-	-	-	-	-	I/E	I/E	
CR17	11h	#	#	#	#	#	#	AATTMODE1	AATTMODE0	R/W
		-	-	-	-	-	-	I/E	I/E	
CR18	12h	#	#	#	#	#	#	LATTMODE1	LATTMODE0	R/W
		-	-	-	-	-	-	I/E	I/E	
CR19	13h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR20	14h	#	#	#	#	EQL_EN	EQL_2	EQL_1	EQL_0	R/W
		-	-	-	-	I/E	I/E	I/E	I/E	
CR21	15h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR22	16h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR23	17h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR24	18h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR25	19h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR26	1Ah	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR27	1Bh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR28	1Ch	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR29	1Dh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR30	1Eh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
CR31	1Fh	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	

Table 3 General-Purpose Port Control Register Map

Register Name	Address	Data								R/W
		B7	B6	B5	B4	B3	B2	B1	B0	
GPCR0	20h	GPFA7	GPFA6	GPFA5	GPFA4	GPFA3	GPFA2	GPFA1	GPFA0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR1	21h	GPFB7	GPFB6	GPFB5	GPFB4	GPFB3	GPFB2	GPFB1	#	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	-	
GPCR2	22h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
GPCR3	23h	GPDA7	GPDA6	GPDA5	GPDA4	GPDA3	GPDA2	GPDA1	GPDA0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR4	24h	GPDB7	GPDB6	GPDB5	GPDB4	GPDB3	GPDB2	GPDB1	GPDB0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR5	25h	GPDC7	GPDC6	GPDC5	GPDC4	GPDC3	GPDC2	GPDC1	GPDC0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GPCR6	26h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
GPCR7	27h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	
GPCR8	28h	$	$	$	$	$	$	$	$	/
		-	-	-	-	-	-	-	-	

Symbols for register name
- # : Reserved bits
- $: Don't read nor write

Symbols to show when it can be altered (When to alter)
- I/E : both in the initial mode and in normal operation
- I/ : only in the initial mode
- /E : only in normal operation
- - : Don't change

Symbols to show Read or Write
- R/W : Both for Read and Write
- R/ : Read only
- /W : Write only
- / : Both read and write prohibited

(Note) The change of control registers (including the control registers for general-purpose ports) is detected with SYNC signals (8kHz) so that the change of the control registers less than 250 ms may not be reflected as the LSI behavior.

(Note) When you write a control register in any other mode than the initial mode, SYNC signals (8kHz) must be supplied unless the ML7037-003 is in the internal clock mode (the CLKSEL pin = logic 0').

(Note) Refer to descriptions under Internal Data Memory Access for a way to set CR6, CR7, CR8 and CR9.

(1) CR0

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	SPDN	RST	LINEEN	PCMSEL	CLKEN	PCMEN	ECSEL	OPE_STAT (MCUSEL)
When to alter	/E	/E	I/	I/	I/	I/	I/	I/
Initial value (*1)	0	0	0	0	0	0	0	0

*1: The initial value refers to the control register bit data that is set when this LSI is reset by the PDN pin. (Also when reset by SPDN of B7, the bits other than CR0-B7 and CR16-B7 are set to their initial value.)

B7 : Software Power-Down Control Register
0 : Normal operation
1 : Software power-down reset

During the software power-down reset, this device enters the power-down state. In this state, the control registers, the internal data memories, the filter coefficients of the echo cancellers and those of the noise cancellers and the ALC acquired gain. To go out of the software power-down, write a logic '0'. Then, this LSI goes into the initial mode approx. 250ms after the release of the software power-down.
This function is determined by an ORed result of this bit and the negative logic of the PDN pin. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when the PDN pin is set to a logic 0.
For more details, refer to "Pin Control and Control Registers".
(Note) When an ORed logic of the AVREFEN pin and the AVREFEN-bit [CR16-B7] are logic '1', the AVREF and analog output amps keep powered up even during the power-down state.

B6 : Reset Control Register for the Filter Coefficients of Echo Cancellers and Noise Canceller
0 : Normal operation
1 : Reset

An execution of reset initializes the filter coefficients of echo cancellers and a noise canceller and the ALC acquired gain are initialized.
During the reset state, no speech signals are output. Control registers are preserved.
Execute the initialization in cases where the echo path changes (due to line switching during a telephone conversation, etc.), or for another call.
This function is determined by an ORed result of this bit and the negative logic of the RST pin. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when the RST pin is set to a logic 0.
For more details, refer to "Pin Control and Control Registers".
(Note) The execution of this reset during a call may cause minor noises due to interruption at an arbitrary point in a sequence of PCM codes so that an execution of the reset is recommended to be made in a silent state.

B5 : Line-Side Analog Interface Power-Down Control Register
0 : Normal operation
1 : Power-down

During the power-down, the line-side analog interface is powered-down (excluding the LVFRO output amp). Inputs from input pins are processed as idle patterns, and the LVFRO pin outputs approx. 1.4V.
This function is determined by an ORed result of this bit and the secondary function (LINEEN) of the GPIB1 pin. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

B4 : Coding Format Selection Register for PCM Interface
0 : 16bit linear PCM
1 : μ-law PCM

This is the coding format selection register for PCM interface for the PCMO-pin output and the PCMI-pin input signal. This function is determined by an ORed result of this bit and the PCMSEL pin. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

B3 : BCLK, SYNC Clock Output On/Off Selection Register
0 : On (outputs clocks)
1 : Off (outputs no clocks)

This control is valid only when the CLKSEL pin is a logic '0' (internal clock mode).
When OFF, the SYNC and BCLK output pins are in the high impedance state.

B2 : PCM I/O Control Register
0 : PCM interface enabled
1 : PCM interface disabled

When the PCM interface is disabled, the input from the PCMI pin is internally processed as idle patterns, and the PCMO pin goes to a high impedance state.

B1 : Echo Canceller Mode Selection Register
0 : Single echo canceller mode
1 : Dual echo canceller mode

In the single echo canceller mode, only the acoustic echo canceller is enabled. The 64ms cancelable echo delay time is give to the acoustic echo canceller.
In the dual echo canceller mode, both of the acoustic and line echo cancellers are enabled, and the 64ms and the 20ms cancelable delay time are given respectively.
This function is determined by an ORed result of this bit and the secondary function (ECSEL) of the GPIB6 pin. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin configured as its secondary function is set to a logic 1.For more details, refer to "Pin Control and Control Registers". For more details, refer to "Pin Control and Control Registers".

B0 : Operation Mode Selection Register
0 : Initial mode
1 : Normal operation

(Initial mode)
This LSI transits into the initial mode approx. 250ms after the release of power-down reset.
A logic '1' in the initial mode status flag register (READY) shows that this LSI is in the initial mode. After confirming the device is in the initial mode, start writing control registers (including the control registers for general-purpose ports) and the internal data memories.
In this mode, all the following functions are disabled;
- Output pins of the PCM interface go to a high impedance state
- Speech signal inputs are internally processed as idle patterns
- Echo cancellers, a noise canceller, a slope filter, programmable gains (TPAD, RPAD), and the ALC are disabled.

A logic '1' with the MCUSEL pin skips this initial mode after the release of the power-down reset.

(Normal operation)
A logic '1'in this register automatically alters the READY bit [CR10-B7] to a logic '0', and lets the device start the normal operation.
Control over echo cancellers, a noise canceller, a slope filter, programmable gains (TPAD, RPAD), and the ALC with their relevant control registers are possible.
(Note) Acoustic and line echo cancellers are disabled and outputs of the AVFRO pin and the LVFRO pin in their default states. In order to enable echo cancellers and to get speech outputs, the following registers are required to altered from their initial values;
- Acoustic echo canceller enable control register (AECEN-bit [CR12-B6])
- Line echo canceller enable control register (LECEN-bit [CR11-B6])
- Acoustic-side analog output selection register (AVFROSEL-bit [CR16-B1])
- Line-side analog output selection register (LVFROSEL-bit [CR16-B0])

(2) CR1

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	DMWR	#	#	#	#	#	#	#
When to alter	I/E	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7 : Internal Data Memory Write Execution Register
0 : Write inhibited
1 : Write

A logic '1' in this register transfers the data specified by the CR8 (D15-D8) and the CR9 (D7-D0) into the internal data memory address specified by the CR6 (D15-D8) and the CR7 (D7-D0). After the completion of the data transfer, this register bit is automatically cleared to a logic '0'.
Confirm if this register bit turns to a logic '0' before another internal data memory write is made.
For more details, refer to descriptions under Internal Data Memory Access.

B6-B0 : Reserved bits … Do not alter the initial values.

(3) CR2

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	#	#	#	RALCTHR	RPAD3	RPAD2	RPAD1	RPAD0
When to alter	-	-	-	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

B7-5 : Reserved bits ⋯ Do not alter the initial values.

B4 : Receive-Side ALC Through Mode Selection Register
0 : Normal mode (ALC enabled)
1 : Through mode

The ALC is to automatically amplify and attenuate its input signal to the target output level (-10dBm0) mainly for a purpose to absorb difference in handset speech output level varying from a handset to a handset. The maximum gain with the ALC is +27dB. In the through mode, the ALC outputs its given input as it is, and the internal state of the ALC is initialized.
The maximum gain could be altered via internal data memory access. For more details, refer to descriptions under Internal Data Memory Access.
This function is determined by an ORed result of this bit and the secondary function (ALCTHR) of the GPIB4 pin. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

B3-0 : Receive-Side Volume Control Register
A combination of these bits determines the gain setting (including mute) for the receive-side speech signals.
This function is determined by an ORed result of these bits and the secondary functions (RPAD3-0) of the GPIA7-4 pins. Also, each of these bit registers is designed to contain the ORed value automatically so that these bits show a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

Table 4 Receive-Side Volume Control

B3 (RPAD3)	B2 (RPAD2)	B1 (RPAD1)	B0 (RPAD0)	Level
0	1	1	1	+21dB
0	1	1	0	+18dB
0	1	0	1	+15dB
0	1	0	0	+12dB
0	0	1	1	+9dB
0	0	1	0	+6dB
0	0	0	1	+3dB
0	0	0	0	0dB
1	1	1	1	-3dB
1	1	1	0	-6dB
1	1	0	1	-9dB
1	1	0	0	-12dB
1	0	1	1	-15dB
1	0	1	0	-18dB
1	0	0	1	-21dB
1	0	0	0	MUTE

(4) CR3

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	#	#	#	#	TPAD3	TPAD2	TPAD1	TPAD0
When to alter	-	-	-	-	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

B7-4 : Reserved bits ⋯ Do not alter the initial values.

B3-0 : Transmit-Side Volume Control Register
A combination of these bits determines the gain setting (including mute) for the transmit-side speech signals. This function is determined by an ORed result of these bits and the secondary functions (TPAD3-0) of the GPIA3-0 pins. Also, each of these bit registers is designed to contain the ORed value automatically so that these bits show a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

Table 5 Transmit-Side Volume Control

B3 (TPAD3)	B2 (TPAD2)	B1 (TPAD1)	B0 (TPAD0)	Level
0	1	1	1	+21dB
0	1	1	0	+18dB
0	1	0	1	+15dB
0	1	0	0	+12dB
0	0	1	1	+9dB
0	0	1	0	+6dB
0	0	0	1	+3dB
0	0	0	0	0dB
1	1	1	1	-3dB
1	1	1	0	-6dB
1	1	0	1	-9dB
1	1	0	0	-12dB
1	0	1	1	-15dB
1	0	1	0	-18dB
1	0	0	1	-21dB
1	0	0	0	MUTE

(5) CR4

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	#	#	#	APGA4	APGA3	APGA2	APGA1	APGA0
When to alter	-	-	-	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

B7-5 : Reserved bits … Do not alter the initial values.

B4-0 : Acoustic Side PGA Gain Level Tuning Registers
A combination of these bits determines the gain level of acoustic side PGA. Refer to Table 6.
(Note) Tune acoustic side PGA gain level only during the reset state by the RST pin or the RST-bit [CR0-B6] or in the initial mode.

Table 6 Acoustic Side PGA Gain Level

B4 (APGA4)	B3 (APGA3)	B2 (APGA2)	B1 (APGA1)	B0 (APGA0)	Level
0	1	1	1	1	(inhibited for use)
0	1	1	1	0	(inhibited for use)
0	1	1	0	1	(inhibited for use)
0	1	1	0	0	(inhibited for use)
0	1	0	1	1	(inhibited for use)
0	1	0	1	0	+20dB
0	1	0	0	1	+18dB
0	1	0	0	0	+16dB
0	0	1	1	1	+14dB
0	0	1	1	0	+12dB
0	0	1	0	1	+10dB
0	0	1	0	0	+8dB
0	0	0	1	1	+6dB
0	0	0	1	0	+4dB
0	0	0	0	1	+2dB
0	0	0	0	0	0dB
1	1	1	1	1	-2dB
1	1	1	1	0	-4dB
1	1	1	0	1	-6dB
1	1	1	0	0	-8dB
1	1	0	1	1	-10dB
1	1	0	1	0	-12dB
1	1	0	0	1	-14dB
1	1	0	0	0	-16dB
1	0	1	1	1	-18dB
1	0	1	1	0	-20dB
1	0	1	0	1	(inhibited for use)
1	0	1	0	0	(inhibited for use)
1	0	0	1	1	(inhibited for use)
1	0	0	1	0	(inhibited for use)
1	0	0	0	1	(inhibited for use)
1	0	0	0	0	(inhibited for use)

(6) CR5

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	#	#	#	LPGA4	LPGA3	LPGA2	LPGA1	LPGA0
When to alter	-	-	-	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

B7-5 : Reserved bits ··· Do not alter the initial values.

B4-0 : Line-Side PGA Gain Level Tuning Registers
A combination of these bits determines the gain level of line-side PGA. Refer to Table 7.
(Note) Tune line-side PGA gain level only during the reset state by the RST pin or the RST-bit [CR0-B6] or in the initial mode.

Table 7 Line-Side PGA Gain Level

B4 (LPGA4)	B3 (LPGA3)	B2 (LPGA2)	B1 (LPGA1)	B0 (LPGA0)	Level
0	1	1	1	1	(inhibited for use)
0	1	1	1	0	(inhibited for use)
0	1	1	0	1	(inhibited for use)
0	1	1	0	0	(inhibited for use)
0	1	0	1	1	(inhibited for use)
0	1	0	1	0	+20dB
0	1	0	0	1	+18dB
0	1	0	0	0	+16dB
0	0	1	1	1	+14dB
0	0	1	1	0	+12dB
0	0	1	0	1	+10dB
0	0	1	0	0	+8dB
0	0	0	1	1	+6dB
0	0	0	1	0	+4dB
0	0	0	0	1	+2dB
0	0	0	0	0	0dB
1	1	1	1	1	-2dB
1	1	1	1	0	-4dB
1	1	1	0	1	-6dB
1	1	1	0	0	-8dB
1	1	0	1	1	-10dB
1	1	0	1	0	-12dB
1	1	0	0	1	-14dB
1	1	0	0	0	-16dB
1	0	1	1	1	-18dB
1	0	1	1	0	-20dB
1	0	1	0	1	(inhibited for use)
1	0	1	0	0	(inhibited for use)
1	0	0	1	1	(inhibited for use)
1	0	0	1	0	(inhibited for use)
1	0	0	0	1	(inhibited for use)
1	0	0	0	0	(inhibited for use)

(7) CR6

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	A15	A14	A13	A12	A11	A10	A9	A8
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	1	1	1	0	0	0	0

B7-0 : Internal Data Memory Upper Address Specifying Register
For a way to access to the internal data memory, please refer to descriptions under Internal Data Memory Access in later section.
The initial values of CR6-CR9 indicate the version number.

(8) CR7

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	A7	A6	A5	A4	A3	A2	A1	A0
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	1	1	0	1	1	1

B7-0 : Internal Data Memory Lower Address Specifying Register

For a way to access to the internal data memory, please refer to descriptions under Internal Data Memory Access in later section.
The initial values of CR6-CR9 indicate the version number.

(9) CR8

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	D15	D14	D13	D12	D11	D10	D9	D8
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	1	1

B7-0 : Internal Data Memory Upper Data Specifying Register

For a way to access to the internal data memory, please refer to descriptions under Internal Data Memory Access in later section.
The initial values of CR6-CR9 indicate the version number.

(10) CR9

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	D7	D6	D5	D4	D3	D2	D1	D0
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	1

B7-0 : Internal Data Memory Lower Data Specifying Register

For a way to access to the internal data memory, please refer to descriptions under Internal Data Memory Access in later section.
The initial values of CR6-CR9 indicate the version number.

(11) CR10

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	READY	#	#	#	#	#	#	#
When to alter	-	-	-	-	-	-	-	-
Initial value	1	0	0	0	0	0	0	0

B7 : Initial Mode Status Flag Register
0 : Not in the initial mode
1 : In the initial mode

This LSI automatically transits into the initial mode approx. 250ms after a release of the power-down reset. During the initial mode, this register shows a logic '1' to indicate that it's ready for the internal data memory access. The alternation of the OPE_STAT bit [CR0-B0] to a logic '1'let this device transit to normal operation out of the initial mode, and this register automatically returns to logic '0'. By reading this register, it could be known if this device is in the initial mode or not.

B6-0 : Reserved bits ··· Do not alter the initial values.

(12) CR11

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	LTHR	LECEN	LHLD	#	LCLP	LSLC	LATT	#
When to alter	I/E	I/E	I/E	-	I/E	I/	I/E	-
Initial value	0	0	0	0	0	1	0	0

This register byte gets valid only in the dual echo canceller mode specified with ECSEL-bit [CR0-B1] (Echo Canceller Mode Selection Register) or the secondary function (ECSEL) if theGPIB6 pin.

B7 : Line Echo Canceller Through Mode Selection Register
0 : Normal mode
1 : Through mode

When the through mode is selected, speech data at the RinL and the SinL are output to the RoutL and the SoutL respectively as they are.
In the through mode, the filter coefficients of the line echo canceller are preserved, not reset, and the functions of the LHLD, the LCLP, the LATT, and the LSLC are disabled.
The line echo canceller functional block diagram is shown in Figure 23.

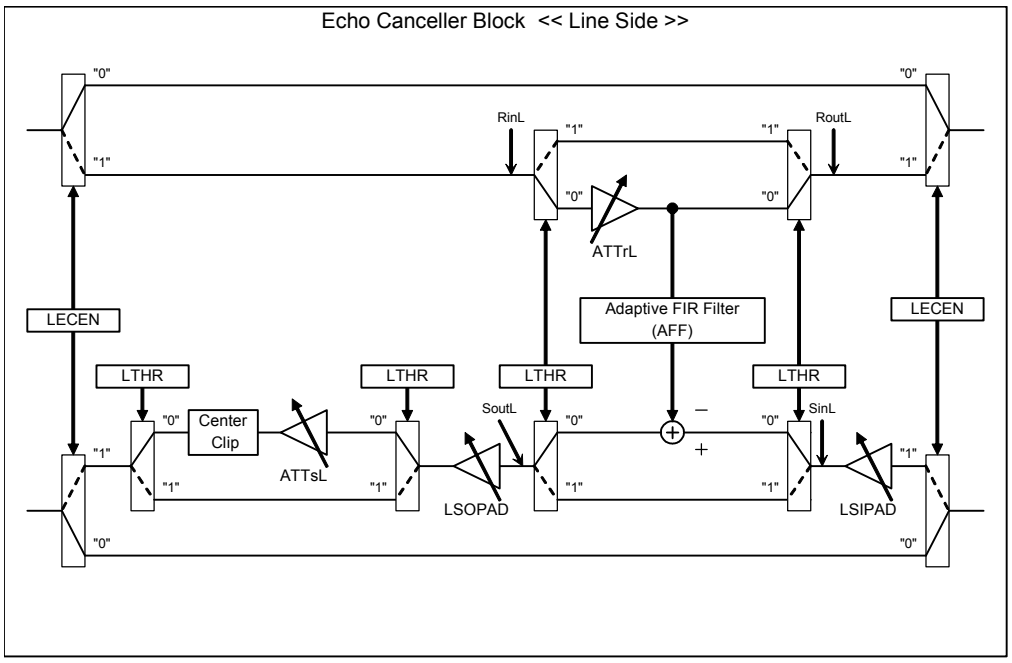


Figure 23 Line Echo Canceller Functional Block Diagram

B6 : Line Echo Canceller Enable Register
0 : Disabled
1 : Enabled

When the line echo canceller is disabled, the functions of the LHLD, the LCLP, the LSLC, the LATT, the LSOPAD0, the LSOPAD1, the LSIPAD0, and the LSIPAD1 are invalid, and the filter coefficients of the line echo canceller are initialized.
This function is determined by an ORed result of this bit and the secondary functions (ECEN) of the GPIB7 pins. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

B5 : Line Echo Canceller Filter Coefficients Update Suspension Register
0 : Allows updates
1 : Update suspended

The update suspension may be helpful for an application where the upper system can detect the RinL signals to be tones with which the coefficient convergence may not be so appropriate.
This control is valid when the LTHR-bit [CR11-B7] is logic '0' and the ORed logic of the LECEN-bit [CR11-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.

B4 : Reserved bits ··· Do not alter the initial values.

B3 : Line Echo Canceller Center Clip On/Off Register
0 : Off
1 : On

When the input to this functional block is not more than the Center Clip Operating Threshold or less, the center clip function forcibly sets it to the zero PCM code (or the positive zero μ-law PCM code). The initial value of the threshold is approx. -53dBm0.
This control is valid when the LTHR-bit [CR11-B7] is logic '0' and the ORed logic of the LECEN-bit [CR11-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.
The Center Clip Operating Threshold and the Center Clip Attenuation Level can be altered through the internal data memory access. Refer to descriptions under Internal Data Memory Address Map in the later section.

B2 : Line Echo Canceller Automatic SinL Level Control Register
0 : Off
1 : On

This is a function to automatically tune the SinL input level and to recover the level decrease at the SoutL to maintain the level diagram flat. The echo attenuation of the echo canceller would decrease when the Echo Return Loss (E.R.L. = RoutL − SinL) is positive. With this function enabled, the degree of the decrease in echo attenuation is relieved.
This control is valid when the LTHR-bit [CR11-B7] is logic '0' and the ORed logic of the LECEN-bit [CR11-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.
(Note) When this register is set to a logic '1', the gains with the LSOPAD and the LSIPAD must be set to 0dB (initial value).

B1 : Line Echo Canceller ATT On/Off Register
0 : On
1 : Off

This bit turns on or off the ATT function to complement echo cancellation by the line echo canceller's adaptive FIR filter and to suppress howling by means of attenuators (ATTsL, ATTrL) provided in the RinL input and SoutL output of the line echo canceler.
When only a speaker on the RinL-side speaks, the ATTsL works.
When a speaker on the RinL-side is silent or when both of speakers on the RinL-side and the SinL-side speak, the ATTrL works.
The initial values of the ATTrL and the ATTsL are 0dB and 6dB (approx.) respectively. The attenuation level of the ATTrL and the ATTsL can be altered by the internal data memory. Refer to descriptions under Internal Data Memory Address Map in the later section.
This control is valid when the LTHR-bit [CR11-B7] is logic '0' and the ORed logic of the LECEN-bit [CR11-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.

B0 : A reserved bit ··· Do not alter the initial value...

(13) CR12

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	ATHR	AECEN	AHLD	#	ACLP	ASLC	AATT	#
When to alter	I/E	I/E	I/E	-	I/E	I/	I/E	-
Initial value	0	0	0	0	0	1	0	0

B7 : Acoustic Echo Canceller Through Mode Selection Register
0 : Normal mode
1 : Through mode

When the through mode is selected, speech data at the RinA and the SinA are output to the RoutA and the SoutA respectively as they are.
In the through mode, the filter coefficients of the acoustic echo canceller are preserved, not reset, and the functions of the AHLD, the AHD, the AATT, ACLP, and the ASLC are disabled.
The acoustic echo canceller functional block diagram is shown in Figure 24.

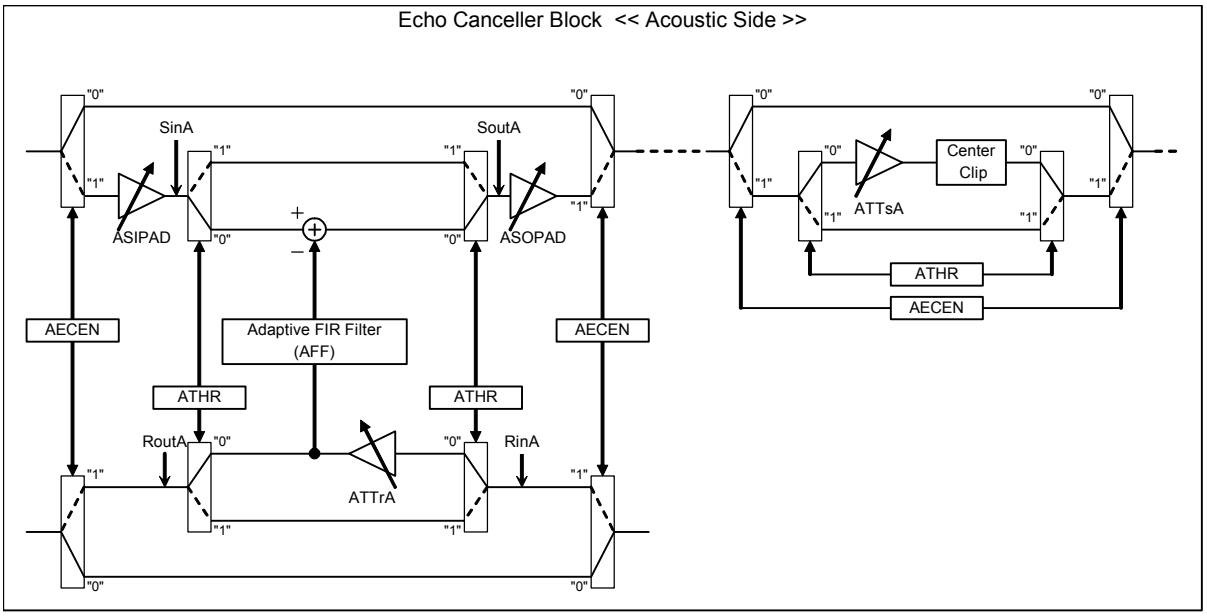


Figure 24 Acoustic Echo Canceller Functional Block Diagram

B6 : Acoustic Echo Canceller Enable Register
0 : Disabled
1 : Enabled

When the line echo canceller is disabled, the functions of the AHLD, the AATT, the ACLP, the ASLC, the ASOPAD0, the ASOPAD1, the ASIPAD0, and the ASIPAD1 are invalid, and the filter coefficients of the acoustic echo canceller are initialized.
This function is determined by an ORed result of this bit and the secondary functions (ECEN) of the GPIB7 pins. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

B5 : Acoustic Echo Canceller Filter Coefficients Update Suspension Register
0 : Allows updates
1 : Update suspended

The update suspension may be helpful for an application where the upper system can detect the RinS signals to be tones with which the coefficient convergence may not be so appropriate.
This control is valid when the ATHR-bit [CR12-B7] is logic '0' and the ORed logic of the AECEN-bit [CR12-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.

B4 : A reserved bit ··· Do not alter the initial value.

B3 : Acoustic Echo Canceller Center Clip On/Off Register
0 : Off
1 : On

When the input to this functional block is not more than the Center Clip Operating Threshold or less, the center clip function forcibly sets it to the zero PCM code (or the positive zero μ-law PCM code). The initial value of the threshold is approx. -53dBm0.
This control is valid when the ATHR-bit [CR12-B7] is logic '0' and the ORed logic of the AECEN-bit [CR12-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.
The Center Clip Operating Threshold and the Center Clip Attenuation Level can be altered through the internal data memory access. Refer to descriptions under Internal Data Memory Address Map in the later section.

B2 : Acoustic Echo Canceller Automatic SinA Level Control Register
0 : Off
1 : On

This is a function to automatically tune the SinA input level and to recover the level decrease at the SoutA to maintain the level diagram flat. The echo attenuation of the echo canceller would decrease when the Echo Return Loss (E.R.L. = RoutA − SinA) is positive. With this function enabled, the degree of the decrease in echo attenuation is relieved.
This control is valid when the ATHR-bit [CR12-B7] is logic '0' and the ORed logic of the AECEN-bit [CR12-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.
(Note) When this register is set to a logic '1', the gains with the ASOPAD and the ASIPAD must be set to 0dB (initial value).

B1 : Acoustic Echo Canceller ATT On/Off Register
0 : On
1 : Off

This bit turns on or off the ATT function to complement echo cancellation by the acoustic echo canceller's adaptive FIR filter and to suppress howling by means of attenuators (ATTsA, ATTrA) provided in the RinA input and SoutA output of the line echo canceler. When only a speaker on the RinA-side speaks, the ATTsA works. When both of speakers on the RinA-side and the SinA-side speak, the ATTrA works.
The initial values of the ATTrA and the ATTsA are 6dB (approx.) and 36dB (approx.) respectively. The attenuation level of the ATTrA and the ATTsA can be altered by the internal data memory. Refer to descriptions under Internal Data Memory Address Map in the later section.
This control is valid when the ATHR-bit [CR12-B7] is logic '0' and the ORed logic of the AECEN-bit [CR12-B6] and the secondary function (ECEN) of the GPIB7 pin is logic '1'.

B0 : A reserved bit ··· Do not alter the initial value.

(14) CR13

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	ASOPAD1	ASOPAD0	ASIPAD1	ASIPAD0	LSOPAD1	LSOPAD0	LSIPAD1	LSIPAD0
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

B7-6 : Acoustic Echo Canceller SoutA Gain Level Control Registers
B5-4 : Acoustic Echo Canceller SinA Loss Level Control Registers

The echo attenuation of the echo canceller would decrease when the Echo Return Loss (E.R.L. = RoutA − SinA) is positive (SinA > RoutA). A combination of the ASIPAD1 and the ASIPAD0 determines a loss level with the ASIPAD to tune the Echo Return Loss adequate for the acoustic echo canceller. A combination of the ASOPAD1 and the ASOPAD0 determines a gain level with the ASOPAD so that the loss by the ASIPAD could be recovered and the level diagram could be kept flat, if needed.
The ASIPAD is a signal processing to narrower the dynamic range so that the loss level is recommended to be 0dB when the Echo Return Loss is known to be negative (SinA < RoutA).
Refer to Table 8 and Table 9.

Table 8 Acoustic Echo Canceller SoutA Gain Level (ASOPAD)

B7 (ASOPAD1)	B6 (ASOPAD0)	Level
0	0	0dB
0	1	+6dB
1	0	+12dB
1	1	+18dB

Table 9 Acoustic Echo Canceller SinA Loss Level (ASIPAD)

B5 (ASIPAD1)	B4 (ASIPAD0)	Level
0	0	0dB
0	1	-6dB
1	0	-12dB
1	1	-18dB

(Note) When Acoustic Echo Canceller Automatic SinA Level Control is enabled (ASLC-bit [CR12-B2] = '1'), Set all of the ASOPAD1, the ASOPAD0, the ASIPAD1, and the ASIPAD0 to logic '0' (initial value).
(Note) The alternation of the setting with these bits must be made either in the initial mode or while the RST pin is a logic '0' or the RST-bit [CR0-B6] is a logic '1'.

B3-2 : Line Echo Canceller SoutL Gain Level Control Registers
B1-0: Line Echo Canceller SinL Loss Level Control Registers

The echo attenuation of the echo canceller would decrease when the Echo Return Loss (E.R.L. = RoutL − SinL) is positive (SinL > RoutL). A combination of the LSIPAD1 and the LSIPAD0 determines a loss level with the LSIPAD to tune the Echo Return Loss adequate for the line echo canceller. A combination of the LSOPAD1 and the LSOPAD0 determines a gain level with the LSOPAD so that the loss by the LSIPAD could be recovered and the level diagram could be kept flat, if needed.
The LSIPAD is a signal processing to narrower the dynamic range so that the loss level is recommended to be 0dB when the Echo Return Loss is known to be negative (SinL < RoutL).
Refer to Table 10 and Table 11.

Table 10 Line Echo Canceller SoutL Gain Level (LSOPAD)

B3 (LSOPAD1)	B2 (LSOPAD0)	Level
0	0	0dB
0	1	+6dB
1	0	+12dB
1	1	+18dB

Table 11 Line Echo Canceller SinL Loss Level (LSIPAD)

B1 (LSIPAD1)	B0 (LSIPAD0)	Level
0	0	0dB
0	1	-6dB
1	0	-12dB
1	1	-18dB

(Note) When Line Echo Canceller Automatic SinL Level Control is enabled (LSLC-bit [CR11-B2] = '1'), Set all of the LSOPAD1, the LSOPAD0, the LSIPAD1, and the LSIPAD0 to logic '0' (initial value).
(Note) The alternation of the setting with these bits must be made either in the initial mode or while the RST pin is a logic '0' or the RST-bit [CR0-B6] is a logic '1'.

(15) CR14

	B7	B6	B5	B4	B3	B2	B1	B0
CR14	SLPTHR	#	#	#	NCTHR	#	#	#
When to alter	I/E	-	-	-	I/E	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7 : Slope Filter Through Mode Selection Register
0 : Normal mode
1 : Through mode

The slope filter has frequency characteristics to suppress low frequency range and gain high frequency range so that it helps to relax near-end ambient noises usually dominant in low frequency range and to emphasize speech consonants mostly dominant in high frequency range.
This function is determined by an ORed result of this bit and the secondary functions (SLPTHR) of the GPIB5 pins. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

B6-4 : Reserved bits ··· Do not alter the initial values.

B3 : Noise Canceller Through Mode Selection Register
0 : Normal Mode (enabled)
1 : Through Mode

In the though mode, input signals to the noise canceller functional block are output as they are. In the normal mode, the noise canceller works. The initial attenuation level setting for the noise canceller is 13dB (approx.). The noise attenuation level setting could be altered through the internal data memory access. Refer to descriptions under Internal Data Memory Address Map in the later section.
This function is determined by an ORed result of this bit and the secondary functions (NCTHR) of the GPIB3 pins. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin configured as its secondary function is set to a logic 1. For more details, refer to "Pin Control and Control Registers".

B2-0 : Reserved bits ··· Do not alter the initial values.

(16) CR15

	B7	B6	B5	B4	B3	B2	B1	B0
CR15	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	1	0	0	0	0	0	0	0

B7-0:Reserved bits … Do not alter the initial values.

(17) CR16

	B7	B6	B5	B4	B3	B2	B1	B0
CR16	AVREFEN	#	#	#	#	#	AVFROSEL	LVFROSEL
When to alter	I/E	-	-	-	-	-	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

B7 : Power-Down State AVREF/Analog Output Amps Control Register
0 : Powered down during power-down mode
1 : Powered up even during power-down mode

This bit specifies the power-down or the power-up with the AVREF and analog output amps in the power-down state with the PDN pin to be a logic '0' or with the SPDN-bit [CR0-B7] to be a logic '1'.
When this is logic '0', the AVREF and the analog output amps are also powered down in the power-down mode.
When this is logic '1', the AVREF and the analog output amps are powered up even in the power-down mode, and the AVREF pin, the AVFRO pin and the LVFRO pin output 1.4V (approx.).
By keeping the AVREF and analog output amps kept powered up, pop noises which may occur on release and execution of power-down could be relaxed.
This function is determined by an ORed result of this bit and the AVREFEN pin. Also, this bit register is designed to contain the ORed value automatically so that this bit shows a logic '1' when its concerned pin is set to a logic 1.
For more details, refer to "Pin Control and Control Registers".
(Note) This control is valid only during power-down.
(Note) "Analog output amps" here refer to the AVFRO output amp and the LVFRO output amp.

B6-B2 : Reserved bits ··· Do not alter the initial values.

B1 : Acoustic Side Analog Output Selection Register
0 : AVREF (1.4V approx.)
1 : Speech signals

B1 : Line- Side Analog Output Selection Register
0 : AVREF (1.4V approx.)
1 : Speech signals

(18) CR17

	B7	B6	B5	B4	B3	B2	B1	B0
CR17	#	#	#	#	#	#	AATTMODE 1	AATTMODE 0
When to alter	-	-	-	-	-	-	I/E	I/E
Initial value	0	0	0	0	0	0	1	0

B7-2 : Reserved bits ⋯ Do not alter the initial values.

B1-0 : ATTsA Operation Mode Selection Register

The acoustic echo canceller's transmit-side attenuator (ATTsA) helps to further suppress echoes left over by the adaptive FIR filter and to reduce residual echoes; whereas it attributes half-duplexity perceived by a far-end speaker. A combination of these bits determines the balance between the two characteristics out of the 4 modes below;

Table 12 ATTsA Operation Mode

AATTMODE1	AATTMODE0	Operation Mode	Echo Suppress	Full Duplexity
1	1	Type A	Modest	More
1	0	Type B*	:	:
0	1	Type C	:	:
0	0	Type D	Aggressive	Less

* Initial setting = Type B

(19) CR18

	B7	B6	B5	B4	B3	B2	B1	B0
CR18	#	#	#	#	#	#	LATTMODE 1	LATTMODE 0
When to alter	-	-	-	-	-	-	I/E	I/E
Initial value	0	0	0	0	0	0	1	0

B7-2 : Reserved bits ⋯ Do not alter the initial values.

B1-0 : ATTsL Operation Mode Selection Register

The acoustic echo canceller's transmit-side attenuator (ATTsL) helps to further suppress echoes left over by the adaptive FIR filter and to reduce residual echoes; whereas it attributes half-duplexity perceived by a far-end speaker. A combination of these bits determines the balance between the two characteristics out of the 4 modes below;

Table 12 ATTsL Operation Mode

LATTMODE1	LATTMODE0	Operation Mode	Echo Suppress	Full Duplexity
1	1	Type A	Modest	More
1	0	Type B*	:	:
0	1	Type C	:	:
0	0	Type D	Aggressive	Less

* Initial setting = Type B

(20) CR19

	B7	B6	B5	B4	B3	B2	B1	B0
CR19	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(21) CR20

	B7	B6	B5	B4	B3	B2	B1	B0
CR20	#	#	#	#	EQL_EN	EQL_2	EQL_1	EQL_0
When to alter	-	-	-	-	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

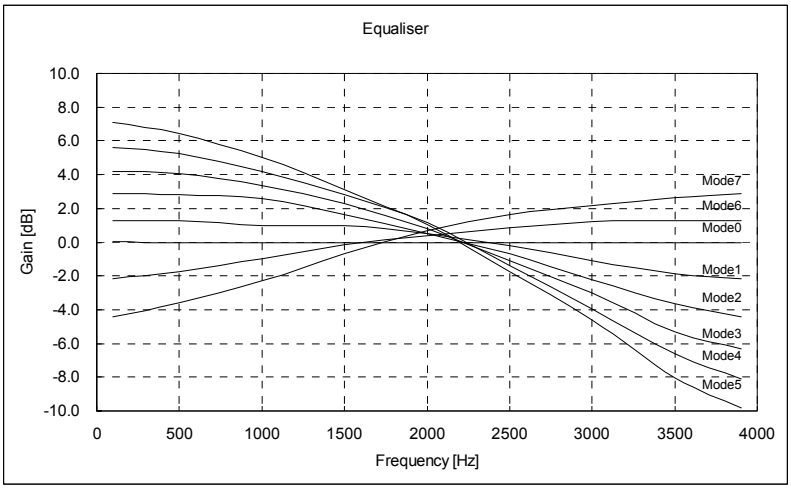
B7-4 : Reserved bits ⋯ Do not alter the initial values.

B3 : Equalizer On/Off Register
0 : Off
1 : On

B2-0 : Equalizer mode selection register

The equalizer modes and their frequency characteristics are shown below;

EQL_2	EQL_1	EQL_0	Mode	Note
0	0	0	Mode 0	Through mode
0	0	1	Mode1	High frequency attenuated ; low frequency amplified
0	1	0	Mode 2	
0	1	1	Mode 3	
1	0	0	Mode 4	
1	0	1	Mode 5	
1	1	0	Mode 6	High frequency amplified ; low frequency attenuated
1	1	1	Mode 7	



Equalizer Filter Characteristics

(22) CR21

	B7	B6	B5	B4	B3	B2	B1	B0
CR21	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(23) CR22

	B7	B6	B5	B4	B3	B2	B1	B0
CR22	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(24) CR23

	B7	B6	B5	B4	B3	B2	B1	B0
CR23	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(25) CR24

	B7	B6	B5	B4	B3	B2	B1	B0
CR24	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(26) CR25

	B7	B6	B5	B4	B3	B2	B1	B0
CR25	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(27) CR26

	B7	B6	B5	B4	B3	B2	B1	B0
CR26	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(28) CR27

	B7	B6	B5	B4	B3	B2	B1	B0
CR27	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(29) CR28

	B7	B6	B5	B4	B3	B2	B1	B0
CR28	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(30) CR29

	B7	B6	B5	B4	B3	B2	B1	B0
CR29	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(31) CR30

	B7	B6	B5	B4	B3	B2	B1	B0
CR30	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(32) CR31

	B7	B6	B5	B4	B3	B2	B1	B0
CR31	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(33) GPCR0

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR0	GPFA7	GPFA6	GPFA5	GPFA4	GPFA3	GPFA2	GPFA1	GPFA0
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

This register byte selects the primary or the secondary function of the GPIA7-0 pins (general-purpose input port pins).

B7 : GPIA7 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) RPAD3

B6 : GPIA6 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) RPAD2

B5 : GPIA5 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) RPAD1

B4 : GPIA4 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) RPAD0

B3 : GPIA3 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) TPAD3

B2 : GPIA2 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) TPAD2

B1 : GPIA1 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) TPAD1

B0 : GPIA0 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) TPAD0

(34) GPCR1

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR1	GPFB7	GPFB6	GPFB5	GPFB4	GPFB3	GPFB2	GPFB1	#
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	-
Initial value	0	0	0	0	0	0	0	0

This register byte selects the primary or the secondary function of the GPIB7-0 pins (general-purpose input port pins).

B7 : GPIB7 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) ECEN

B6 : GPIB6 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) ECSEL

B5 : GPIB5 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) SLPTHR

B4 : GPIB4 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) ALCTHR

B3 : GPIB3 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) NCTHR

B2 : GPIB2 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) VFROSEL

B1 : GPIB1 Primary/Secondary Function Selection Register
0 : (Primary function) General-purpose port
1 : (Secondary function) LINEEN

B0 : A reserved bit ⋯ Do not alter the initial value.

(35) GPCR2

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR2	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(36) GPCR3

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR3	GPDA7	GPDA6	GPDA5	GPDA4	GPDA3	GPDA2	GPDA1	GPDA0
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

These are the input status flag registers for the general-purpose input port pins (the GPIA7-0). By reading these registers, the input status of the concerned pins is known.

B7 : GPIA7 pin Input Status Flag Register

GPFA7-bit	GPIA7 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	RPAD3	shows the input status	does not influence to the pin status

B6 : GPIA6 pin Input Status Flag Register

GPFA6-bit	GPIA6 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	RPAD2	shows the input status	does not influence to the pin status

B5 : GPIA5 pin Input Status Flag Register

GPFA5-bit	GPIA5 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	RPAD1	shows the input status	does not influence to the pin status

B4 : GPIA4 pin Input Status Flag Register

GPFA4-bit	GPIA4 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	RPAD0	shows the input status	does not influence to the pin status

B3 : GPIA3 pin Input Status Flag Register

GPFA3-bit	GPIA3 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	TPAD3	shows the input status	does not influence to the pin status

B2 : GPIA2 pin Input Status Flag Register

GPFA2-bit	GPIA2 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	TPAD2	shows the input status	does not influence to the pin status

B1 : GPIA1 pin Input Status Flag Register

GPFA1-bit	GPIA1 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	TPAD1	shows the input status	does not influence to the pin status

B0 : GPIA0 pin Input Status Flag Register

GPFA0-bit	GPIA0 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	TPAD0	shows the input status	does not influence to the pin status

(37) GPCR4

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR4	GPDB7	GPDB6	GPDB5	GPDB4	GPDB3	GPDB2	GPDB1	GPDB0
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

These are the input status flag registers for the general-purpose input port pins (the GPIB7-0). By reading these registers, the input status of the concerned pins is known.

B7 : GPIB7 pin Input Status Flag Register

GPBF7-bit	GPIB7 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	ECEN	shows the input status	does not influence to the pin status

B6 : GPIB6 pin Input Status Flag Register

GPBF6-bit	GPIB6 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	ECSEL	shows the input status	does not influence to the pin status

B5 : GPIB5 pin Input Status Flag Register

GPBF5-bit	GPIB5 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	SLPTHR	shows the input status	does not influence to the pin status

B4 : GPIB4 pin Input Status Flag Register

GPBF4-bit	GPIB4 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	ALCTHR	shows the input status	does not influence to the pin status

B3 : GPIB3 pin Input Status Flag Register

GPBF3-bit	GPIB3 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	NCTHR	shows the input status	does not influence to the pin status

B2 : GPIB2 pin Input Status Flag Register

GPBF2-bit	GPIB2 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	VFROSEL	shows the input status	does not influence to the pin status

B1 : GPIB1 pin Input Status Flag Register

GPBF1-bit	GPIB1 pin Function	Read	Write
0	General input port	shows the input status	does not influence to the pin status
1	LINEEN	shows the input status	does not influence to the pin status

B0 : GPIB0 pin Input Status Flag Register

GPIB0 pin Function	Read	Write
General input port	shows the input status	does not influence to the pin status

(38) GPCR5

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR5	GPDC7	GPDC6	GPDC5	GPDC4	GPDC3	GPDC2	GPDC1	GPDC0
When to alter	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E
Initial value	0	0	0	0	0	0	0	0

These determine the output status for the general-purpose output port pins (the GPOC7-0). By reading these registers, the output status of the concerned pins is known.

B7 : GPOC7 Output Specifying Register

Read	Write
GPOC7 register value	Specifies the output status of the GPOC7 pin

B6 : GPOC6 Output Specifying Register

Read	Write
GPOC6 register value	Specifies the output status of the GPOC6 pin

B5 : GPOC5 Output Specifying Register

Read	Write
GPOC5 register value	Specifies the output status of the GPOC5 pin

B4 : GPOC4 Output Specifying Register

Read	Write
GPOC4 register value	Specifies the output status of the GPOC4 pin

B3 : GPOC3 Output Specifying Register

Read	Write
GPOC3 register value	Specifies the output status of the GPOC3 pin

B2 : GPOC2 Output Specifying Register

Read	Write
GPOC2 register value	Specifies the output status of the GPOC2 pin

B1 : GPOC1 Output Specifying Register

Read	Write
GPOC1 register value	Specifies the output status of the GPOC1 pin

B0 : GPOC0 Output Specifying Register

Read	Write
GPOC0 register value	Specifies the output status of the GPOC0 pin

(39) GPCR6

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR6	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(40) GPCR7

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR7	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

B7-0 : Reserved bits ··· Do not alter the initial values.

(41) GPCR8

	B7	B6	B5	B4	B3	B2	B1	B0
GPCR8	$	$	$	$	$	$	$	$
When to alter	-	-	-	-	-	-	-	-
Initial value	1	1	1	1	1	1	1	1

B7-0 : Reserved bits ··· Do not alter the initial values.

MICRO CONTROLLER INTERFACE

A way to use the micro controller interface is shown herebelow;

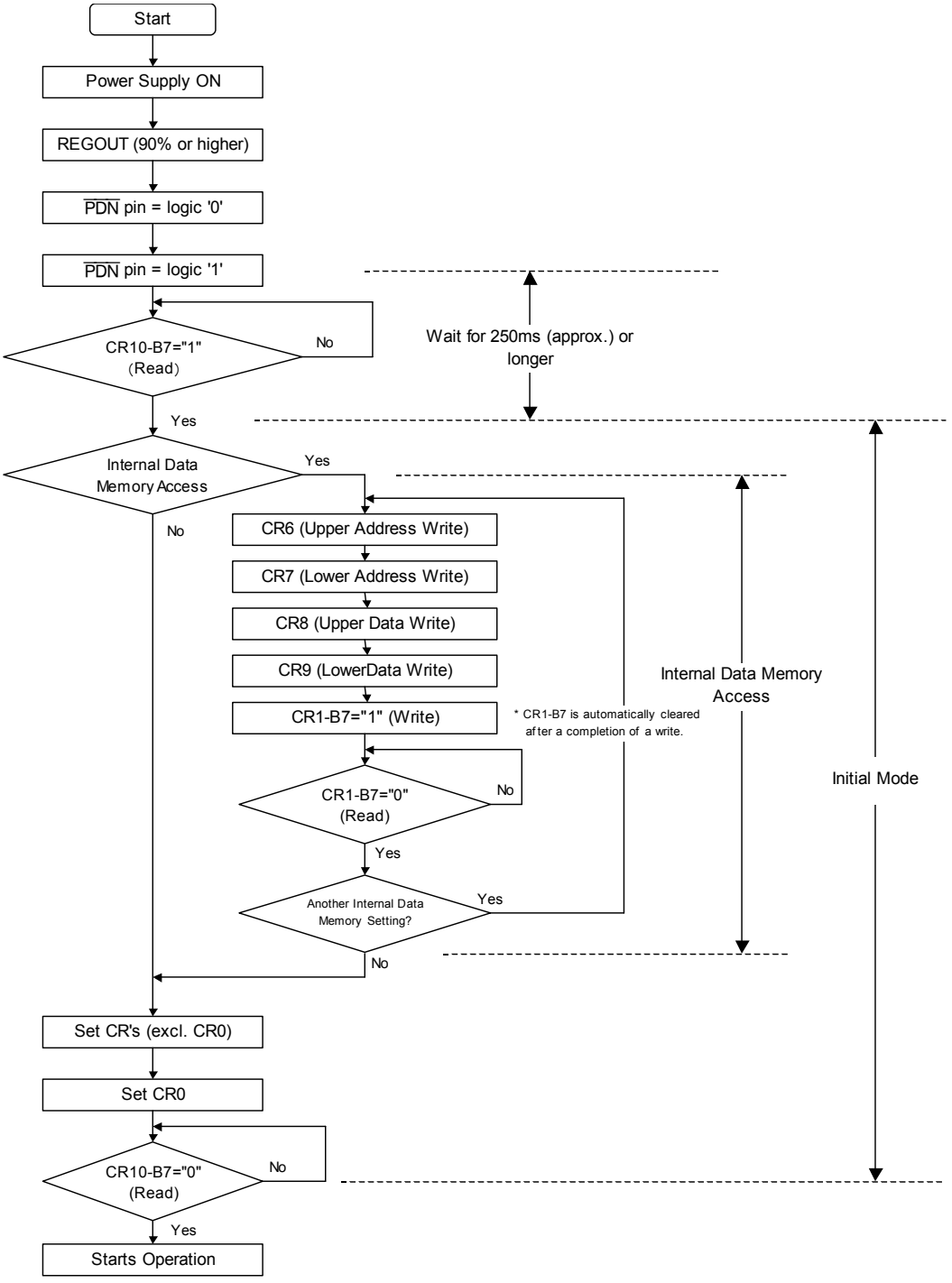


Figure 25 Micro Controller Interface Flow Chart

INTERNAL DATA MEMORY ACCESS

The ML7037-003 has an area called the internal data memories (16-bit wide address and 16-bit wide data), and operates reading variables such as coefficients and thresholds retained therein. By alternating the data in the given memory addresses, the default state could be customized.

How to Write into the Internal Data Memory

The CR6 (A15-A8) and the CR7 (A7-A0) are registers to specify the address of the internal data memory to alter. The CR8 (D15-D8) and the CR9 (D7-D0) are registers to store the data to write into the internal data memory to alter.
When the MCUSEL pin is given a logic '0', the ML7037-003 automatically transits into the initial mode 250ms (approx.) after a release of power-down reset by the PDN pin or the SPDN-bit [CR0-B7], and the READY-bit [CR10-B7] turns to be a logic '1' which shows the ML7037-003 has got ready for the control register access.
During this initial mode, specify both the 16-bit wide address by the CR6-CR7 and the 16-bit wide data by the CR8-CR9 first, and then write a logic '1' into the DMWR-bit [CR1-B7], which executes alternation of the internal data memory in the given address. After the internal data memory alternation, the DMWR-bit [CR1-B7] automatically is cleared to be a logic '0'. The flow of this internal data memory access is shown in Figure 26.
When more than an internal data memory, repeat the procedure above. A change of the OPE_STAT-bit [CR0-B0] to a logic '1' let the ML7037-003 out of the initial mode, and it starts normal operation.

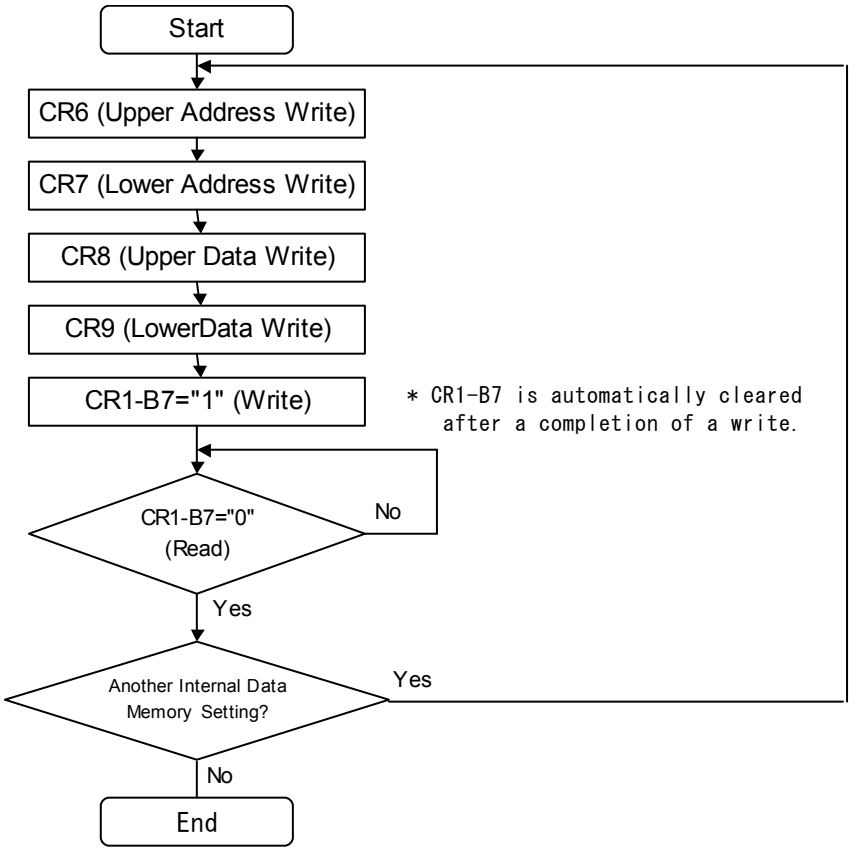


Figure 26 Internal Data Memory Access Flow Chart

PIN CONTROL AND CONTROL REGISTERS

Some of functions and states with the ML7037-003 could be determined either by input state of certain pins (their secondary functions, if the pins are general-purpose input port pins) and/or the control registers. In such cases, the functions and states are determined by ORed logics between them. Hence, when a function or a state is determined (called as "State Control") by the concerned pin input, it is required to be careful with the concerned register setting; and visa versa.
Table 13 shows such pins and the relevant control registers.
All the values to be set in the relevant control registers are the initial values set on a release of power-down reset by the PDN pin or the SPDN-bit [CR0-B7].

Function	Pin input to make when State Control is made by the control register	Pin	Control register value to set when State Control is made by the pin	Control Register
Power-down reset	logic '1'	PDN	logic '0'	SPDN
Reset	logic '1'	RST	logic '0'	RST
PCM Coding Format Selection	logic '0'	PCMSEL	logic '0'	PCMSEL
Micro Control Interface Enable/Disable Selection	logic '0'	MCUSEL	logic '0'	OPE_STAT
Transmit-Side Volume Control	logic '0'	GPIA[3-0] (TPAD[3-0]) *1	logic '0'	TPAD[3-0]
Receive-Side Volume Control	logic '0'	GPIA[4-7] (RPAD[3-0]) *1	logic '0'	RPAD[3-0]
Line-Side Analog Interface Power-Down Control	logic '0'	GPIB1 (LINEEN) *1	logic '0'	LINEEN
Analog Output Selection	logic '0'	GPIB2 (VFROSEL) *1	logic '0'	AVFROSEL LVFROSEL
Noise Canceller Through Mode Selection	logic '0'	GPIB3 (NCTHR) *1	logic '0'	NCTHR
Receive-Side ALC Through Mode Selection	logic '0'	GPIB4 (ALCTHR) *1	logic '0'	RALCTHR
Slope Filter Through Mode Selection	logic '0'	GPIB5 (SLPTHR) *1	logic '0'	SLPTHR
Echo Canceller Mode Selection Register	logic '0'	GPIB6 (ECSEL) *1	logic '0'	ECSEL
Acoustic Echo Canceller Enable Control	logic '0'	GPIB7 (ECEN) *1	logic '0'	LECEN AECEN

*1 : A name in (bracket) shows the pin name when the secondary function is assigned.

Table 13 Relevant Input Pins And Control Registers

INTERNAL DATA MEMORY ADDRESS MAP

Functional Block	What to Determine	Address	Initial Value		When allowed to alter		
			Data	Operation Definition	Initial Mode*1	On Halt*2	On Operation*3
ALC	Maximum Gain (Data 1)	0F11h	1400h	27dB	Yes	Yes	No
	Maximum Gain (Data 2)	0F0Ah	0B49h		Yes	Yes	No
	Maximum Gain (Data 3)	0F0Bh	07FDh		Yes	Yes	No
	Maximum Gain (Data 4)	0F0Ch	0401h		Yes	Yes	No
	Maximum Gain (Data 5)	0F14h	08F4h		Yes	Yes	No
	Maximum Gain (Data 6)	0F15h	00E4h		Yes	Yes	No
Noise Canceller	Noise Attenuation Level (Data1)	01B5h	199Ah	13dB	Yes	Yes	No
	Noise Attenuation Level (Data2)	01ACh	1400h		Yes	Yes	No
Line Echo Canceller	ATTsL Attenuation	0788h	4027h	6dB	Yes	Yes	No
	ATTrL Attenuation (Data1)	0AA2h	7FFFh	6dB	Yes	Yes	No
	ATTrL Attenuation (Data2)	0AA0h	0000h		Yes	Yes	No
	ATTrL Attenuation (Data3)	0AA1h	0000h		Yes	Yes	No
	Center Clip Operational Threshold	07B2h	0020h	-53dBm0 (approx.)	Yes	Yes	No
	Center Clip Attenuation Level	07B3h	0000h	MUTE	Yes	Yes	No
	Echo Cancellable Delay Time	0AA4h	00A0h	20ms	Yes	No	No
Acoustic Echo Canceller	ATTsA Attenuation	076Bh	0207h	36dB	Yes	Yes	No
	ATTsA On-to-Off Transition (Data1)	077Dh	0140h	Mode	Yes	Yes	No
	ATTsA On-to-Off Transition (Data2)	0777h	00A0h		Yes	Yes	No
	ATTrA Attenuation	0ABBh	3FFFh	6dB	Yes	Yes	No
	Center Clip Operational Threshold	07ABh	0020h	-53dBm0 (approx.)	Yes	Yes	No
	Center Clip Attenuation Level	07ACh	0000h	MUTE	Yes	Yes	No
	Speech/Silence Judging Threshold on Receive-Side	0AC0h	0200h	-29 dBm0 (approx.)	Yes	Yes	No
	Echo Cancellable Delay Time	0ABDh	0200h	64ms	Yes	No	No

*1 Initial Mode : A state the ML7037-003 enters after a release of power-down reset when the MCUSEL pin is set to a logic '0'.
*2 Halt : When the concerned function is disabled or set in the through mode
*3 On Operation : When the concerned function is enabled and operational

Table 14 Relevant Input Pins and Control Registers

Automatic Level Controller (Maximum Gain)

The default maximum gain could be altered through the internal data memory.
Though the ALC could automatically gain its received signals when the received signals are weak, it amplifies not only speech but also noises such as a far-end speaker's background noises when the ALC gets gain. When such a trade-off is unwanted or when system noise level with your hands-free is relatively high, the maximum gain is recommended to be relaxed.

Noise Maximum Gain [dB]	Address (0F11h)	Address (0F0Ah)	Address (0F0Bh)	Address (0F0Ch)	Address (0F14h)	Address (0F15h)
	Data	Data	Data	Data	Data	Data
0	0200h	1944h	11E3h	08F7h	0400h	0200h
3	0200h	11E3h	0CAAh	0658h	05A6h	016Ah
6	0200h	0CAAh	08F7h	047Eh	07FBh	0100h
9	0284h	0B49h	07FDh	0401h	08F4h	00E4h
12	038Eh	0B49h	07FDh	0401h	08F4h	00E4h
15	0506h	0B49h	07FDh	0401h	08F4h	00E4h
18	0718h	0B49h	07FDh	0401h	08F4h	00E4h
21	0A06h	0B49h	07FDh	0401h	08F4h	00E4h
24	0E28h	0B49h	07FDh	0401h	08F4h	00E4h
27*	1400h	0B49h	07FDh	0401h	08F4h	00E4h

* The initial values.

Noise Canceller (Noise Attenuation Level)

The default noise attenuation level could be altered through the internal data memory.
There is a trade-off between noise attenuation and sound quality. In other words, increasing the noise attenuation deteriorates sound quality, and decreasing the noise attenuation improves sound quality.

Noise Attenuation Level [dB]	Address (01B5h)	Address (01ACh)
	Data1	Data2
6	3D71h	1400h*
9	28F6h	1400h*
13	199Ah*	1400h*
18	0E14h	2000h

* The initial values.

ATTsL Attenuation

The default ATTsL Attenuation level could be altered through the internal data memory.

Attenuation [dB]	Address (0788h) Data
0	7FFFh
3	5A9Dh
6*	4027h*
9	2D6Ah
12	2027h

* The default and the initial value

ATTrL Attenuation

The default ATTrL Attenuation level could be altered through the internal data memory.

Attenuation [dB]	Address (0AA2h) Data1	Address (0AA0h) Data2	Address (0AA1h) Data3
0*	7FFFh*	0000h*	0000h*
6	3FFFh	0040h	FF80h

* The default and the initial value

ATTsA Attenuation

The default ATTsA Attenuation level could be altered through the internal data memory.

Attenuation [dB]	Address (076Bh) Data
3	5A9Eh
6	4027h
9	2D6Bh
12	2027h
15	16C3h
18	101Dh
21	0B68h
24	0814h
27	05B8h
30	040Ch
33	02DEh
36*	0207h*

* The default and the initial value

ATTsA On-to-Off Transition

The default mode of ATTsA On-to-Off transition could be altered through the internal data memory.
Basically full duplexity and a degree of non-linear echo suppression is in a relationship of a trade-off. This balance is primarily determined by selecting among Type A, B, C and D using CR17-B1, B0 (AATTMODE1-bit, AATTMODE0-bit).
After you choose an appropriate AATTMODE, you may be able to minorly relax the half-duplexity by fastening On-to-Off transition of ATTsA.

Mode	Address (077Dh) Data1	Address (0777h) Data2	Transition	Echo Suppress	Full Duplexity
Mode 0*	0140h*	00A0h*	Slow	Aggressive	Less
Mode 1	0050h	00A0h	:	:	:
Mode 2	0000h	0050h	Fast	Modest	More

* The default and the initial value

ATTrA Attenuation

The default ATTrA Attenuation level could be altered through the internal data memory.

Attenuation [dB]	Address（0ABBh） Data
0	7FFFh
3	5A9Dh
6*	3FFFh*
9	2D6Ah
12	2026h

* The default and the initial value

Line Echo Canceller's Center Clip's (LCLP's) Operational Threshold and Attenuation Level

The default of the line echo canceller's center clip's (LCLP's) operational threshold and the attenuation level could be altered through the internal data memory.
It may help to further suppress near-end ambient noises to complement.

Threshold	Address（07B2h）
	Data
-29dBm0	01FDh
-32dBm0	0169h
-35dBm0	00FFh
-38dBm0	00B5h
-41dBm0	0080h
-44dBm0	005Bh
-47dBm0	0040h
-50dBm0	002Dh
-53dBm0*	0020h*

* The default and the initial value

(Note) The thresholds above are applicable when the input signals are tones. The threshold against verbal speeches or noises may be a bit higher than them.

It's possible to make use of this function not only to mute the output when the input to this functional block is below the given operational threshold but also to attenuate the input by a given loss by altering the internal data memory.

Attenuation [dB]	Address（07B3h）
	Data
3	2D4Eh
6	2000h
9	16B5h
MUTE*	0000h*

* The default and the initial value

(Note) The threshold inadequately high may affect the transmit speech quality or increase the half-duplexity.

Acoustic Echo Canceller's Center Clip's (ACLP's) Operational Threshold and Attenuation Level

The default of the acoustic echo canceller's center clip's (ACLP's) operational threshold and the attenuation level could be altered through the internal data memory.
It may help to further suppress near-end ambient noises to complement.

Threshold	Address（07ABh）
	Data
-29dBm0	01FDh
-32dBm0	0169h
-35dBm0	00FFh
-38dBm0	00B5h
-41dBm0	0080h
-44dBm0	005Bh
-47dBm0	0040h
-50dBm0	002Dh
-53dBm0*	0020h*

* The default and the initial value

(Note) The thresholds above are applicable when the input signals are tones. The threshold against verbal speeches or noises may be a bit higher than them.

It's possible to make use of this function not only to mute the output when the input to this functional block is below the given operational threshold but also to attenuate the input by a given loss by altering the internal data memory.

Attenuation [dB]	Address（07ACh）
	Data
3	2D4Eh
6	2000h
9	16B5h
MUTE*	0000h*

* The default and the initial value

(Note) The threshold inadequately high may affect the transmit speech quality or increase the half-duplexity.

Silence Threshold of Receive Signals with Acoustic Echo Canceller

The default silence threshold of receive signals with the acoustic echo canceller could be altered by writing a given data in a given memory address.
Tuning this threshold might be effective such as when the setting with the RPAD is extremely high.
When changing this threshold, the Data below should be altered.

Threshold	Address（0AC0h）
	Data
-47dBm0	0040h
-41dBm0	0080h
-35dBm0	0100h
-29dBm0*	0200h*

* The initial values

(Note) The thresholds above are applicable when the input signals are tones. The threshold against verbal speeches or noises may be a bit higher than them.

Cancellable Echo Delay Time

Cancellable echo delay time could be altered through internal data memory access.
In principle, the longer the cancellable echo delay time is, the less the echo attenuation is, though the difference is not so major. Therefore, in an environment where the echo delay time is known to be shorter than the LSI default, it is advantageous to shorten the cancellable echo delay time.

(1) Line Echo Canceller's Cancellable Echo Delay Time

Address : 0AA4h
Initial Value (20ms) : 00A0h

A data in 0236h address to set cancellable echo delay time (X) can be calculated by the following formula;
Formula : X [ms] x 8
Upper Limit (20ms) : 00A0h
Lower Limit (0.5ms) : 0004h
Example (15ms) : 15 x 8 = 120d = 0078h

(Note) The minimum alternation step for cancellable echo delay time is 0.25ms. Cancellable echo delay time cannot be defined in finer step than 0.25ms.
The cancellable delay time for line echo canceller can be defined only in the Dual Echo Canceller Mode, and 0236h address must not be accessed in the Single Echo Canceller Mode.

(2) Acoustic Echo Canceller's Cancellable Echo Delay Time

Address : 0ABDh
Initial Value (64ms) : 0200h

A data in 0237h address to set cancellable echo delay time (X) can be calculated by the following formula;
Formula : X [ms] x 8
Upper Limit (64ms) : 0200h
Lower Limit (0.5ms) : 0004h
Example (50ms) : 50 x 8 = 400d = 0190h

(Note) The minimum alternation step for cancellable echo delay time is 0.25ms. Cancellable echo delay time cannot be defined in finer step than 0.25ms.

DIFFERENCE BETWEEN THE ML7037-002 AND THE ML7037-003

1. Difference in Pin Assignment

   No difference.

2. Difference in Control Registers

Control Register		ML7037-002		ML7037-003	
		Name	Initial Value	Name	Initial Value
CR8	B1	D9	1	D9	1
CR8	B0	D8	0	D8	1
CR11	B3	N/A	0	LCLP	0
CR11	B2	N/A	0	LSLC	0
CR13	B[7:6]	GPADA[1:0]	0	ASOPAD[1:0]	0
CR13	B[5:4]	LPADA[1:0]	0	ASIPAD[1:0]	0
CR13	B[3:2]	GPADL[1:0]	0	LSOPAD[1:0]	0
CR13	B[1:0]	LPADL[1:0]	0	LSIPAD[1:0]	0
CR17	B7	FILLER	1	N/A	0
CR17	B1	AATTMODE1	0	AATTMODE1	1
CR18	B1	N/A	0	LATTMODE1	1
CR18	B0	N/A	0	LATTMODE0	0
CR20	B3	N/A	0	EQL_EN	0
CR20	B[2:0]	N/A	0	EQL_[2:0]	0

3. Difference in Functions

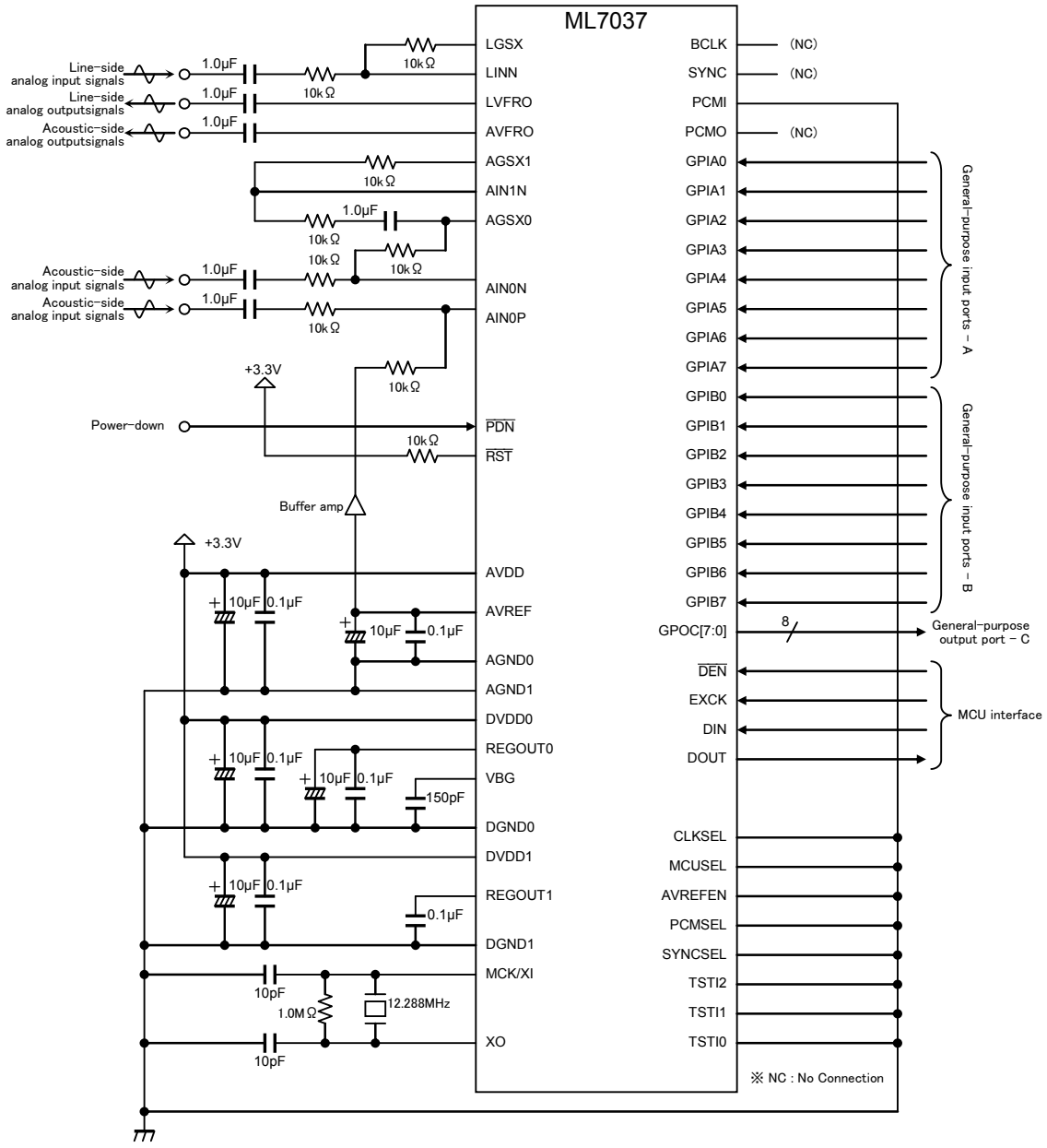
Item	ML7037-002	ML7037-003
Line Echo Canceller's Center Clip	N/A	LCLP
Line Echo Canceller Automatic SinL Level Control	N/A	LSLC
ATTrL Attenuation	-6dB	0dB
Acoustic Echo Canceller In/Out Level Control	GPADA[1:0] / LPADA[1:0]	Re-named (ASOPAD[1:0] / ASIPAD[1:0])
Line Echo Canceller In/Out Level Control	GPADL[1:0] / LPADL[1:0]	Re-named (LSOPAD[1:0] / LSIPAD[1:0])
ALC's Maximum Gain (default)	+20dB	+27dB
ATT FILLER	FILLER	N/A
ATTsL Operational Mode	N/A	Mode Selection (Type A ~ D) LATTMODE[1:0]
Equalizer	N/A	CR20

4. Difference in Internal Data Memory Address Map

Function	Name of Internal Data Memory	ML7037-002 Internal Data Memory Address	ML7037-003 Internal Data Memory Address
ALC	Maximum Gain (Data 1)	N/A	0F11h
ALC	Maximum Gain (Data 2)	N/A	0F0A
ALC	Maximum Gain (Data 3)	N/A	0F0B
ALC	Maximum Gain (Data 4)	N/A	0F0C
ALC	Maximum Gain (Data 5)	N/A	0F14
ALC	Maximum Gain (Data 6)	N/A	0F15
NC	Noise Canceller Attenuation (Data3)	0302h	N/A
LEC	ATTsL Attenuation	025Ch	0788h
LEC	ATTrL Attenuation (Data1)	025Fh	0AA2h
LEC	ATTrL Attenuation (Data2)	N/A	0AA0h
LEC	ATTrL Attenuation (Data3)	N/A	0AA1h
LEC	Center Clip's (LCLP's) Operational Threshold	N/A	07B2h
LEC	Center Clip's (LCLP's) Attenuation	N/A	07B3h
AEC	ATTsA Attenuation	0314h	076Bh
AEC	ATTsA On-to-Off Transition (Data1)	N/A	077Dh
AEC	ATTsA On-to-Off Transition (Data2)	N/A	0777h
AEC	ATTrA Attenuation	0262h	0ABBh
AEC	ATTrA Attenuation	0303h	N/A
AEC	Center Clip's (ACLP's) Operational Threshold	0336h	07ABh
AEC	Center Clip's (ACLP's) Attenuation	0337h	07ACh
AEC	Silence Threshold of Receive Signals	0252h	0AC0h
		0309h	N/A
AEC	ATTsA Operational Mode Intermediate Type Setting	0321h	N/A
LEC	Cancellable Echo Delay Time	0236h	0AA4h
AEC	Cancellable Echo Delay Time	0237h	0ABDh
Miscelaneous		031Ch	N/A
		0243h	N/A
		0244h	N/A
		0323h	N/A

Abbreviations : AEC = Acoustic Echo Canceller
LEC = Line Echo Canceller

APPLICATION CIRCUIT (1)

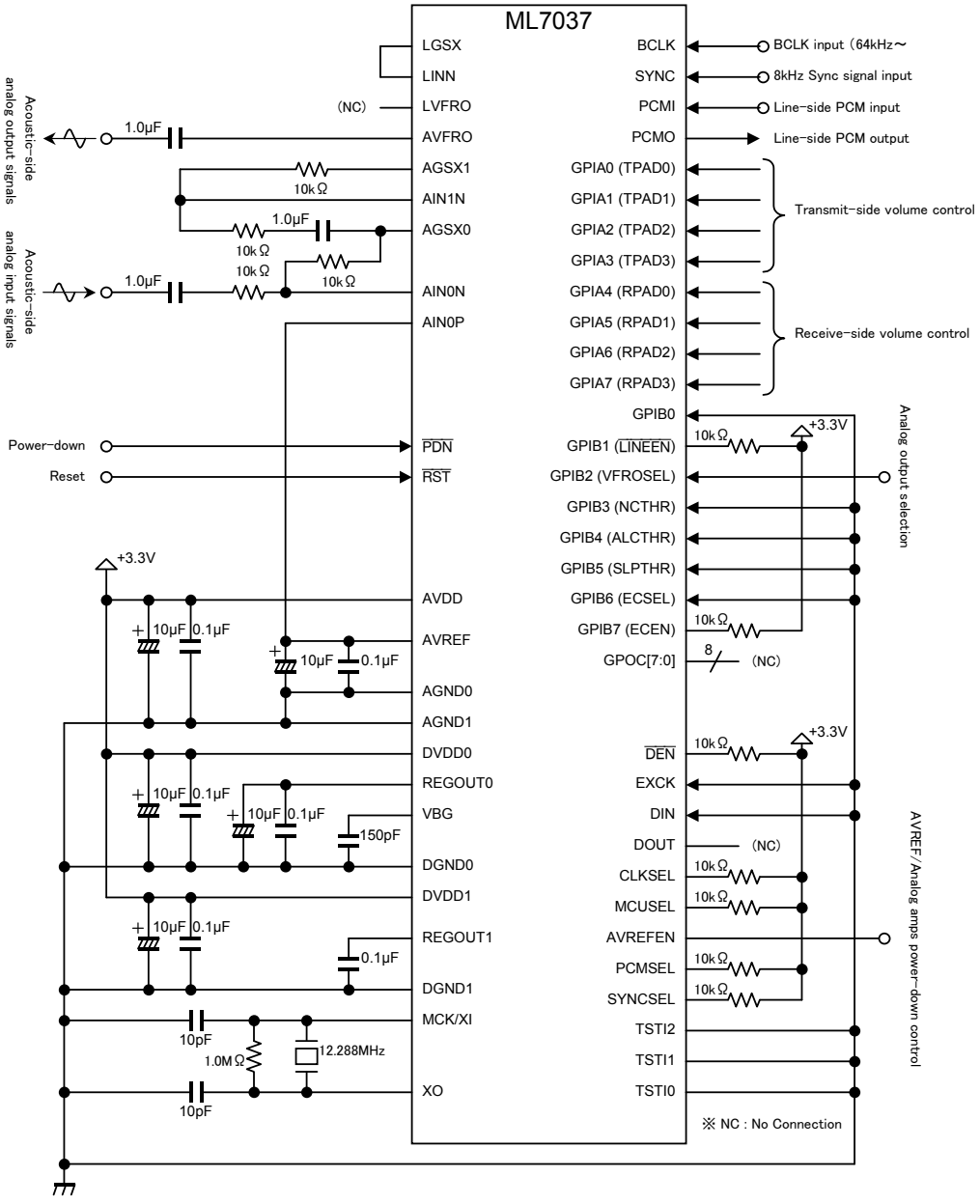


(Conditions)

Speech signal interface on line-side	: Analog
Speech signal input on acoustic side	: Differential
PCM coding format	: 16bit Linear PCM
PCM frame sync timing	: Long frame sync
PCM clock mode	: Internal clock mode (Clock master)
MCU interface	: used

Figure 27

APPLICATION CIRCUIT (2)



(Conditions)

Speech signal interface on line-side	: Digital (PCM)
Speech signal input on acoustic side	: Single
PCM coding format	: μ-law PCM
PCM frame sync timing	: Short frame sync
PCM clock mode	: External clock mode (Clock slave)
MCU interface	: not used

Figure 28

REFERENCE DATA

Echo Canceller Characteristics

- **Rin input level vs. echo attenuation**

(Measuring Conditions) Rin signal : 5 kHz band white noise
E.R.L : 6 dB
Delay time : 5 ms
ATT : OFF SLC : ON
Silence threshold of receive signals : -29dBm0
Noise floor : -68 dBm0 (P-message filter unused)

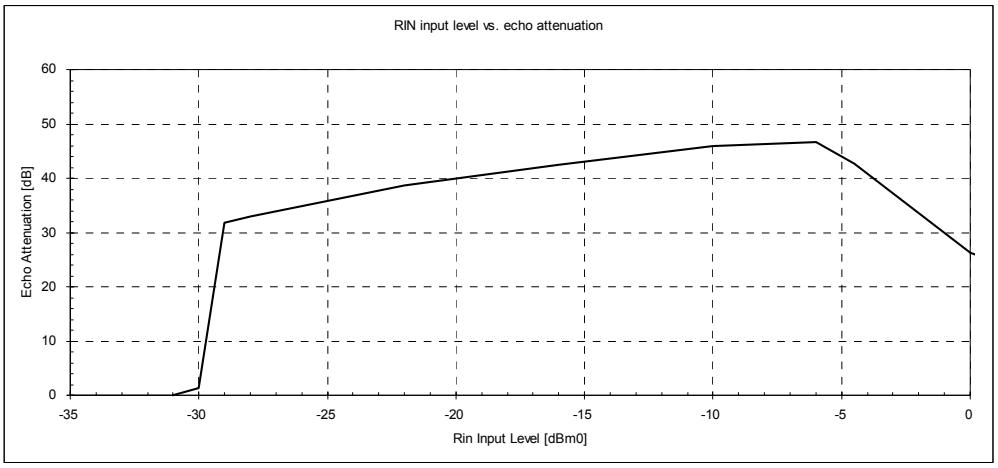


Figure 29

- **E.R.L level vs. echo attenuation (SLC = ON)**

(Measuring Conditions) Rin signal : 5 kHz band white noise
Rin input level : -12.3 dBm0 (with SIOPAD = ±0 dB)
: -18.3 dBm0 (with SIOPAD = ±0 dB)
: -24.3 dBm0 (with SIOPAD = ±0 dB)
: -30.3 dBm0 (with SIOPAD = ±0 dB)
Delay time : 5 ms
ATT : OFF SLC : ON
Noise floor : -68 dBm0 (P-message filter unused)

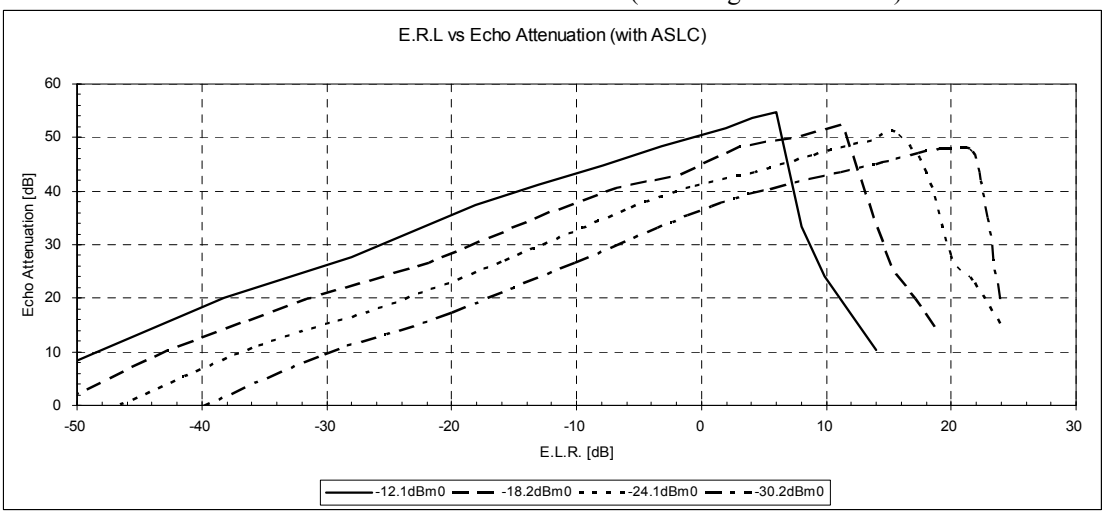


Figure 30

- **E.R.L level vs. echo attenuation (SLC = OFF)**

(Measuring Conditions) Rin signal : 5 kHz band white noise
Rin input level : -12.3 dBm0 (with GLPAD = ±0 dB)
: -12.3 dBm0 (with GLPAD = ±6 dB)
: -12.3 dBm0 (with GLPAD = ±12 dB)
: -12.3 dBm0 (with GLPAD = ±18 dB)
Delay time : 5 ms
ATT : OFF SLC : OFF
Noise floor : -68 dBm0 (P-message filter unused)

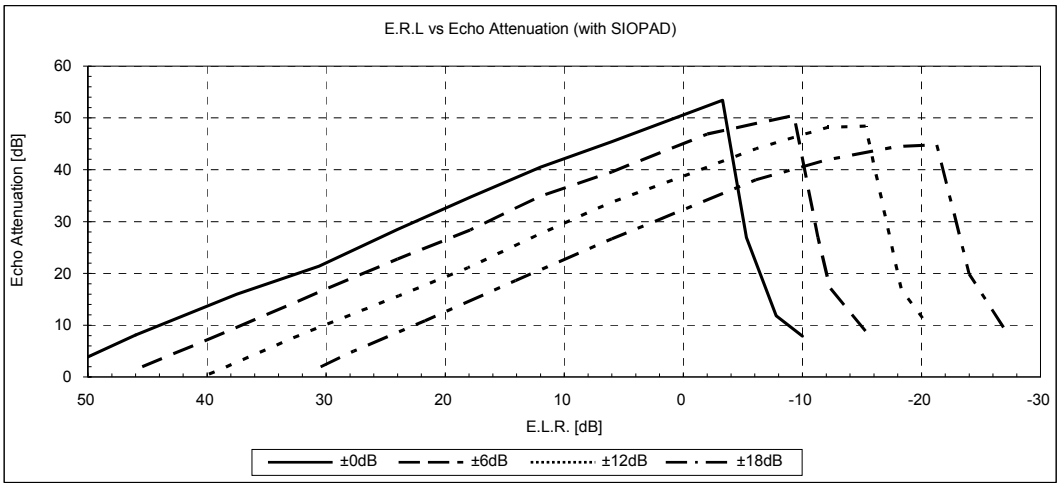


Figure 31

- **Echo delay time vs. echo attenuation (acoustic side)**

(Measuring Conditions) RinA signal : 5 kHz band white noise
RinA input level : -8.3 dBm0
E.R.L. : 6 dB
Delay time : 5 ms
AATT : OFF ASLC : OFF
Noise floor : -68 dBm0 (P-message filter unused)

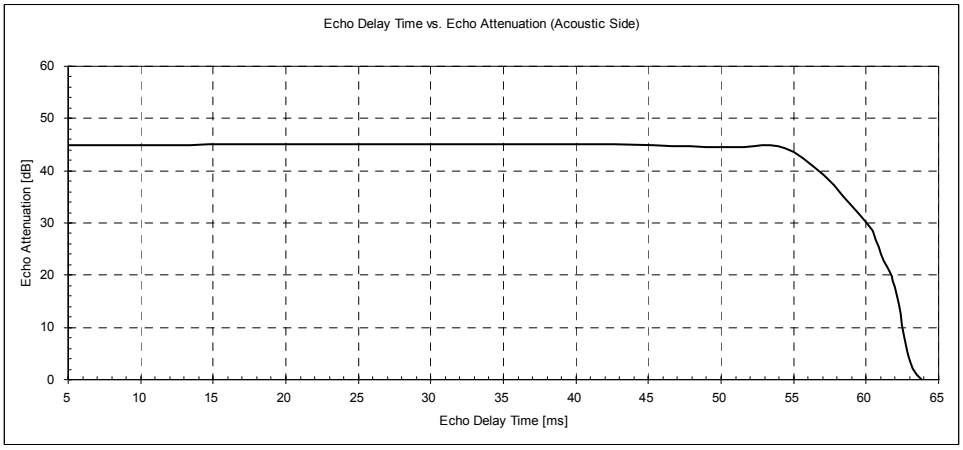


Figure 32

- **Echo delay time vs. echo attenuation (line-side)**

(Measuring Conditions) RinL signal : 5 kHz band white noise
RinL input level : -8.3 dBm0
E.R.L. : 6 dB
LATT : OFF LSLC : OFF
Noise floor : -68 dBm0 (P-message filter unused)

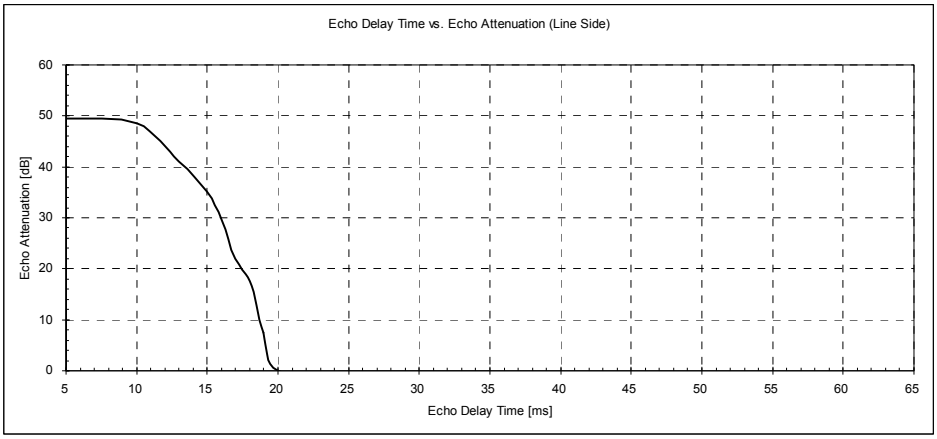


Figure 33

Slope Filter Characteristics

- **Slope filter frequency Characteristics (including CODEC frequency characteristics)**

(Measuring Conditions) Rin signal : 5 kHz band white noise
Rin input : -8.3dBm0
Noise floor : -62 dBm0 (P-message filter unused)

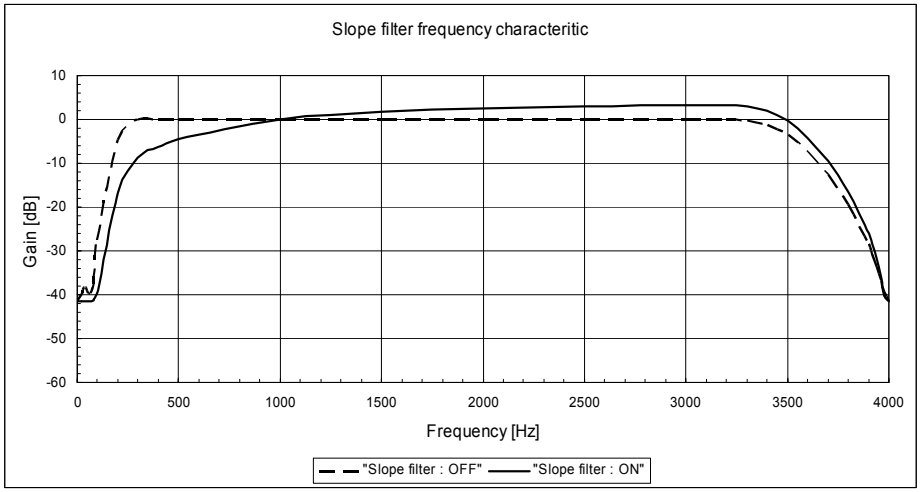


Figure 34

NOTE ON USE

1. Use a stabilized power supply with a low level of noises (especially spike noises and pulse noises of high frequencies) in order to prevent this device from malfunction or degradation in characteristics.

2. Place bypass-capacitors with a good high frequency characteristics for the power supply near the pins of this device in order to assure its electrical characteristics.

3. Place bypass-capacitors with a good high frequency characteristics for the analog signal ground (AVREF pin) near the pins of this device in order to assure its electrical characteristics.

4. Place bypass-capacitors with a good high frequency characteristics for the regulator's reference voltage output (VBG pin) and for the regulator outputs (REGOUT0,1 pins) near the pins of this device in order to assure its electrical characteristics.

5. Connect the AGND0, AGND1, DGND0 and DGND 2 to the system ground at a shortest distance and in a low impedance state.

6. Turn on and off the analog power supply and digital power supply simultaneously, or turn on digital power supply prior to analog power supply and turn off analog power supply prior to digital power supply.

7. After turning on the power, be sure to reset the device with the PDN pin while the master clocks are being supplied.

8. Set a system level diagram so that a value of the Echo Return Loss (E.R.L. = [Power of echo-originating signals at RoutA/RoutL] – [Power of echo signals at SinA/SinL]) is negative and the ASLC function is recommended to be enabled. When the E.R.L. cannot be negative all the time, the GLPAD function is recommended to be enabled with the ASLC function disabled. Refer to a reference data for the E.R.L level vs. echo attenuation of an echo canceller.

9. The input level should be –10 to –20 dBm0. Refer to a reference data for Rin input level vs. echo attenuation.

10. Application-level volume control on use is recommended to be made outside of the echo path such as by the RALC, the RPAD and the TPAD (not between the RoutA and the SinA in the single echo canceller mode; or not between the RoutA and the SinA nor not between the RoutL and the SinL).

    in Dual Echo Canceler mode : to be controlled with the TPAD, the RPAD, and/or the RALC.

    in Signal Echo Canceler mode : to be controlled with the TPAD, the RPAD, the RALC, and/or with the analog input (LINN) that is set at less than 1.3 VPP.

11. Turn off an echo canceller in an environment where no echoes exist.

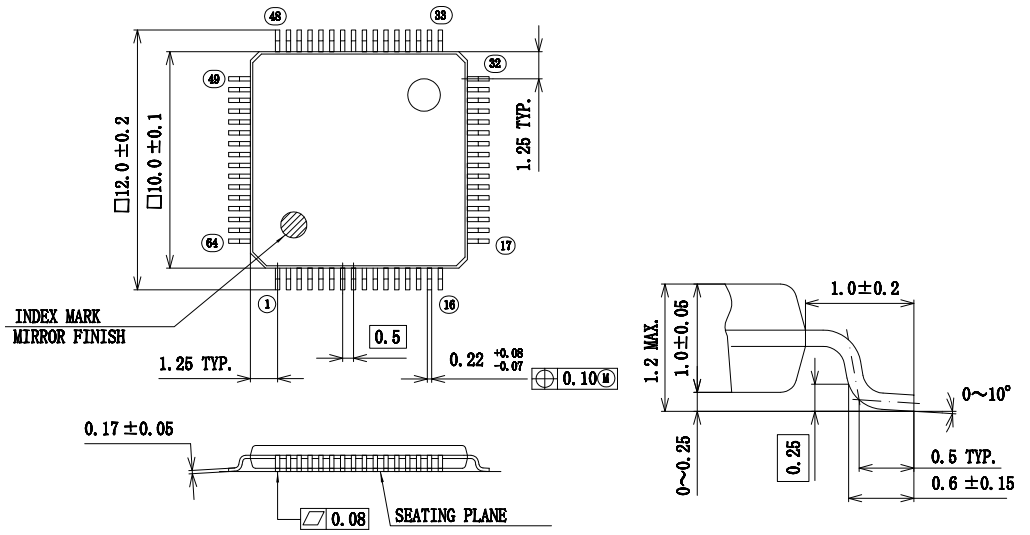
12. When the echo path is changed (such as when resuming telephone communication), reset the device either with the PDN pin, the SPDN bit [CR0-B7], the RST pin or the RST bit [CR0-B6].

13. The Pin Control Mode (the MCUSEL-pin = logic '1') which defines behaviors of this LSI by logic '0' / '1' to concerned input pins has less flexibility in comparison with the External MCU Mode (the MCUSEL-pin = logic '0') which defines behaviors of this LSI through control register setting due to its limitation of the available pin count. Therefore, basically, this LSI is recommended to use in the External MCU Mode.

PACKAGE DIMENSIONS

(Unit : mm)

TQFP64-P-1010-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn / 1 to 3Bi
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.26 TYP.
Rev. No./Last Revised	3/Jun. 24, 2005

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code, and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7037-003-01	Oct. 15, 2007	–	–	Final edition 1
FEDL7037-003-02	Mar. 25, 2008	77	77	Addition of CR20-B3 and CR20-B[2:0] in a table under Difference in Control Registers
		80	80	“used” is corrected to “not used”
FEDL7037-003-03	Aug. 09, 2010	29	29	Cancellable echo delay time 64mS
		82	82	Figure 31 : Rin input level -12.3dBm0 Fix

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