ML7041

Audio CODEC

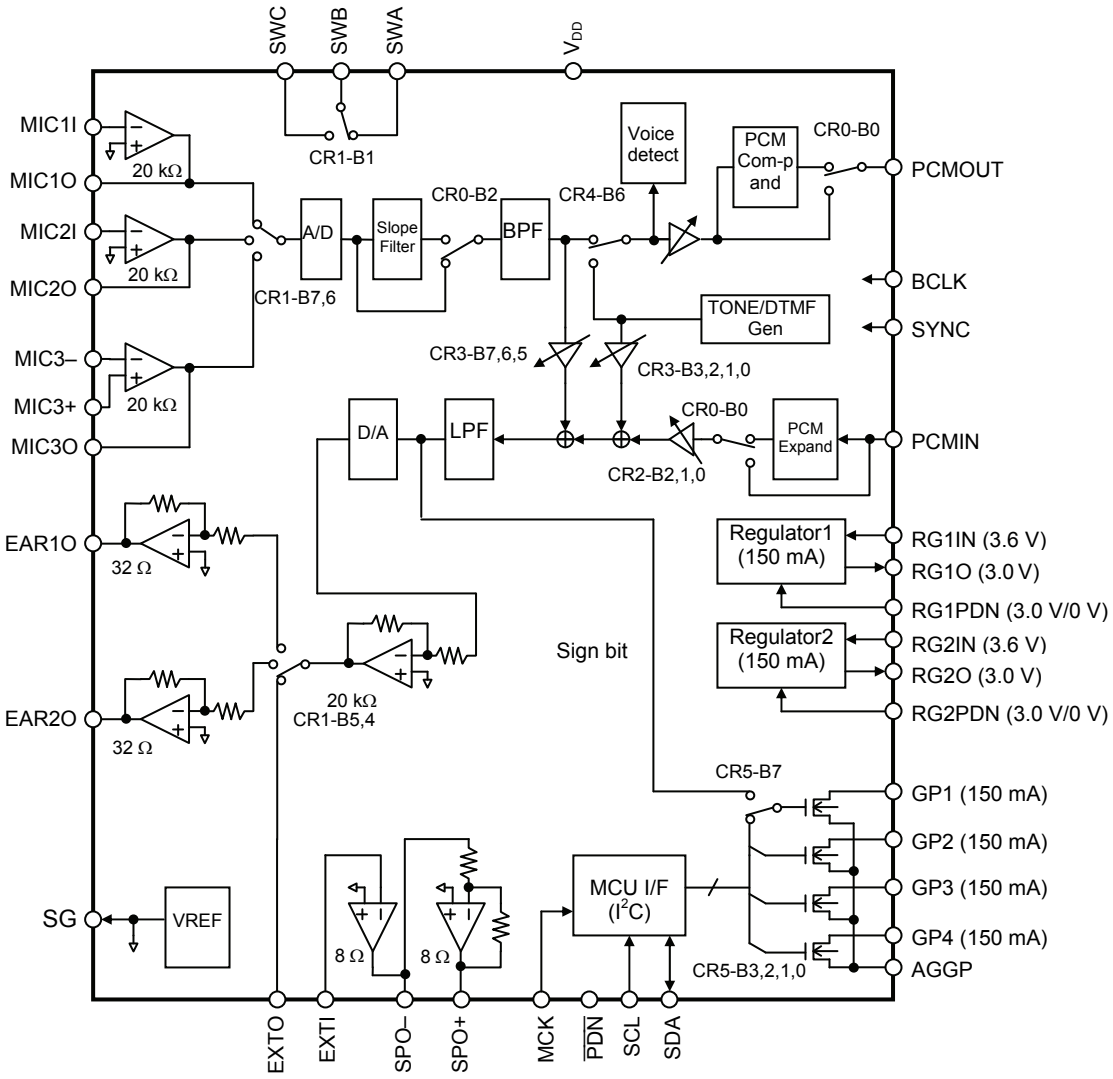
GENERAL DESCRIPTION

The ML7041 is a single-channel full duplex CODEC LSI device which performs mutual transcoding between the analog voice band signals ranging from 300 to 3400 Hz and the 64 kbps PCM serial data.
Provided with such functions as DTMF Tone generation, transmit/receive data gain control, side-tone path, and low-dropout regulator, the ML7041 is best suited for telephone terminals in digital wireless systems.

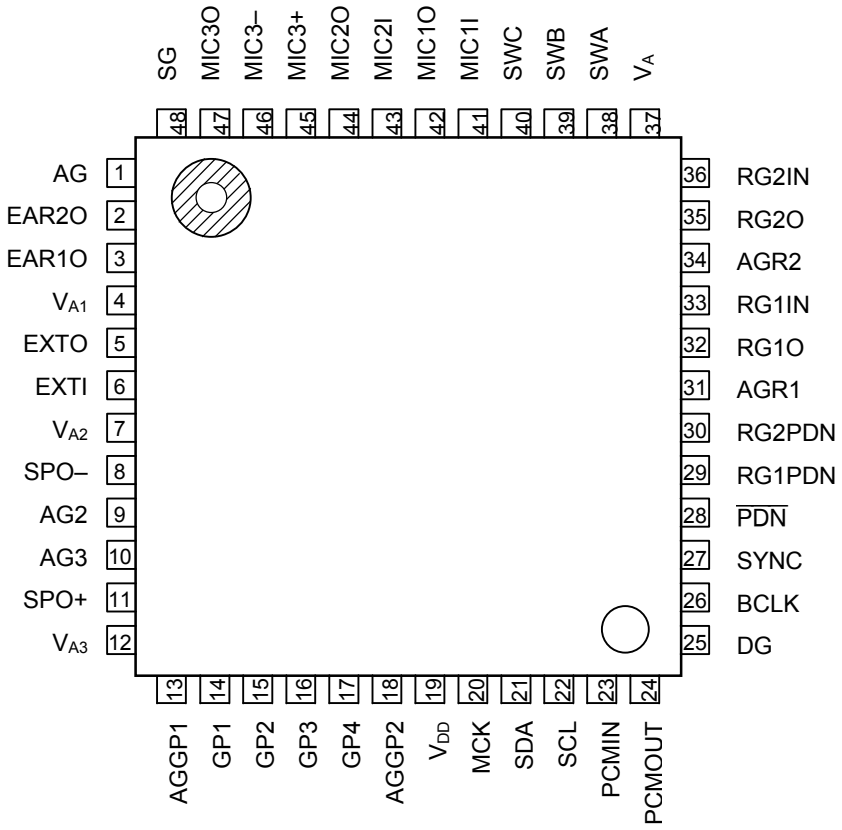
FEATURES

- Single 3 V power supply V_{DD}: 2.4 to 3.3 V
- Coding format: PCM μ-law/PCM A-law/14-bit linear mode selectable
- PCM interface timing: Long frame synchronous timing/short frame synchronous timing selectable
- Transmit/receive full-duplex operation
- Serial PCM transmission data rate: 64 to 2048 kbps
- Low power consumption
  - Operating mode: 15 mW typ. (V_{DD} = 3.0 V)
  - Power-down mode: 3 μW typ. (V_{DD} = 3.0 V)
- Master clock frequency: 2.048 MHz (compatible with PCM shift clock)
- Analog output stage
  - 100 mW (differential type) amplifier output for driving receiver speaker:
    Capable of driving an 8 Ω load.
  - 6.6 mW (single type) amplifier output for driving earphones speaker:
    Capable of driving a 32 Ω load.
- Built-in two low-dropout regulators (150 mA × 2)
- Built-in four general purpose drivers (150 mA × 4)
- Transmit/receive mute, transmit/receive programmable gain control
- Built-in side tone path
- Built-in DTMF tone generator
- Transmit slope filter selectable
- I^2C bus interface (MCU interface)
- Built-in transmit voice signal detector
- Package: 48-pin plastic TQFP (TQFP48-P-0707-0.50-K) (ML7041 TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



48-Pin Plastic TQFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description	State in power-down mode
1	AG	—	Analog ground (0 V)	—
2	EAR2O	O	Receive side voice amplifier output 2	High impedance
3	EAR1O	O	Receive side voice amplifier output 1	High impedance
4	V_{A1}	—	Analog power supply 1 (3.0 V)	—
5	EXTO	O	Receive side voice amplifier output	High impedance
6	EXTI	I	Receive side voice amplifier input	—
7	V_{A2}	—	Analog power supply 2 (3.0 V)	—
8	SPO–	O	Receive side voice amplifier output–	High impedance
9	AG2	—	Analog ground 2 (0 V)	—
10	AG3	—	Analog ground 3 (0 V)	—
11	SPO+	O	Receive side voice amplifier output+	High impedance
12	V_{A3}	—	Analog power supply 3 (3.0 V)	—
13	AGGP1	—	General purpose port ground 1 (0 V)	—
14	GP1	O	General purpose port 1 output (Open drain)	High impedance
15	GP2	O	General purpose port 2 output (Open drain)	High impedance
16	GP3	O	General purpose port 3 output (Open drain)	High impedance
17	GP4	O	General purpose port 4 output (Open drain)	High impedance
18	AGGP2	—	General purpose port ground 2 (0 V)	—
19	V_{DD}	—	Digital power supply (3.0 V)	—
20	MCK	I	Master clock input (2.048 MHz)	—
21	SDA	I/O	I^2C data input/output (Pull-up resister required)	High impedance
22	SCL	I	I^2C shift clock input	—
23	PCMIN	I	PCM receive signal input	—
24	PCMOUT	O	PCM transmit signal output	“H”
25	DG	—	Digital ground (0 V)	—
26	BCLK	I	PCM data shift clock input	—
27	SYNC	I	PCM data shift sync signal input	—
28	$\overline{PDN}$	I	Power down control input	“L”
29	RG1PDN	I	Power down input for regulator 1 (3.0 V/0 V)	“L”
30	RG2PDN	I	Power down input for regulator 2 (3.0 V/0 V)	“L”
31	AGR1	—	Ground for regulator 1 (0 V)	—
32	RG1O	O	Regulator 1 output (3.0 V)	“L” (RG1PDN = “L”)
33	RG1IN	I	Regulator 1 power input (3.6 V)	—
34	AGR2	—	Ground for regulator 2 (0 V)	—
35	RG2O	O	Regulator 2 power output (3.0 V)	“L” (RG2PDN = “L”)
36	RG2IN	I	Regulator 2 input (3.6 V)	—
37	V_A	—	Analog power supply (3.0 V)	—
38	SW A	I/O	Analog switch A	—
39	SW B	I/O	Analog switch B	—
40	SW C	I/O	Analog switch C	—
41	MIC1I	I	Transmit side amplifier 1 inverting input	—
42	MIC1O	O	Transmit side amplifier 1 output	High impedance
43	MIC2I	I	Transmit side amplifier 2 inverting input	—
44	MIC2O	O	Transmit side amplifier 2 output	High impedance
45	MIC3+	I	Transmit side amplifier 3 non-inverting input	—
46	MIC3–	I	Transmit side amplifier 3 inverting input	—
47	MIC3O	O	Transmit side amplifier 3 output	High impedance
48	SG	O	Analog signal ground (1.4 V)	“L”

PIN AND FUNCTIONAL DESCRIPTIONS

MIC1I, MIC1O, MIC2I, MIC2O, MIC3–, MIC3+, MIC3–
Transmit analog inputs and outputs for transmit gain adjustment. Gains of input levels of the pins can be adjusted using external resisters.
MIC1I, MIC2I, and MIC3– are connected to the inverting inputs of the internal transmit amplifiers. MIC3+ is connected to the non-inverting input of the internal transmit amplifier 3. MIC1O, MIC2O, and MIC3O are connected to the internal transmit amplifier outputs. Analog input signals are controlled by the control register (CR1-B7, B6). Also, the amplifiers that are not being selected are deactivated and their outputs are put into high impedance state.
Refer to Figure 1 for gain adjustment.

EAR1O, EAR2O, EXTO, EXTI, SPO–, SPO+
Receive analog outputs and inputs for receive gain adjustment. EAR1O, EAR2O, and EXTO are the receive filter outputs. EAR1O and EAR2O can directly drive a 32 Ω load.
SPO+ and SPO– are differential analog signal outputs which can directly drive an 8 Ω load. The receive side signal outputs can be selected by CR1-B5 and CR1-B4. If the amplifiers connected to EAR1O and EAR2O are not being selected, the amplifiers are deactivated and their outputs are put into high impedance state. Gains of output levels of the pins can be adjusted using the external resistors. The power control is accomplished by CR0-B6.
Refer to Figure 1.

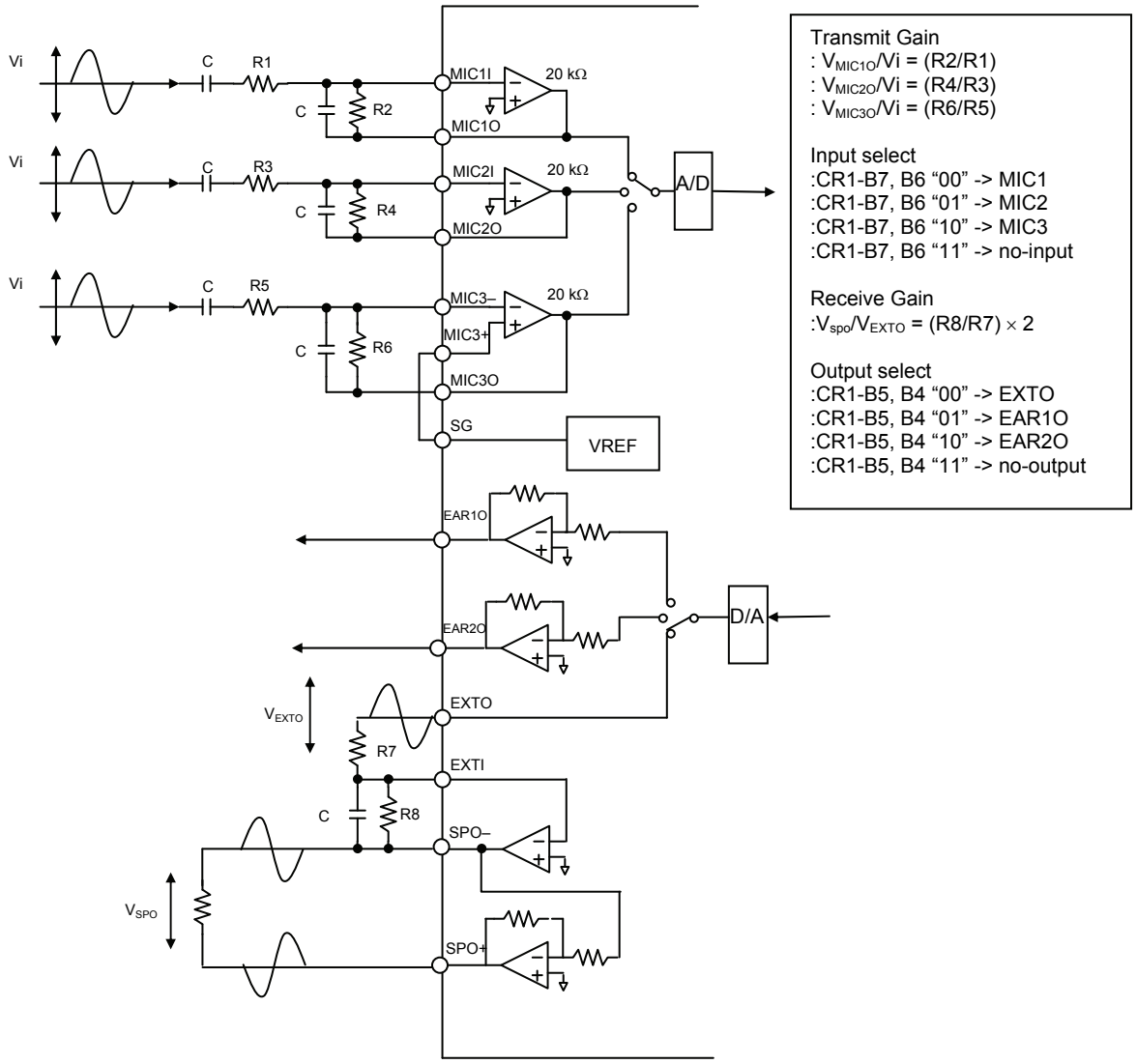


Figure 1 Analog Interface

SG
Analog signal ground.
The output voltage of this pin is approximately 1.4 V. Put the bypass capacitors 0.1 µF ceramic type between this pin and GND to get the specified noise characteristics. During power-down, this output voltage is 0 V.

SWA, SWB, SWC
Used for an internal analog switch. The pin SWB is connected to the pin SWA or the pin SWC. This is controlled by CR1-B1.

RG1PDN, RG1IN, RG1O
Used for Regulator 1. The RG1PDN pin is a power down input. When set to "L", the Regulator 1 changes to the power down state. Since the power down is controlled by a logical OR with CR5-B4 of the control register, set CR5-B4 to logic "0" when using this pin. The RG1IN pin is input to the Regulator 1. The RG1O pin is output from the Regulator 1, whose voltage is 3.0 V. A 1 µF ceramic type bypass capacitor must be connected between the power input pin and GND, and a 10 µF tantalum bypass capacitor must be connected from the output pin to GND.

RG2PDN, RG2IN, RG2O
Used for Regulator 2. The RG2PDN pin is a power down input. When set to "L", the Regulator 2 changes to the power down state. Since the power down is controlled by a logical OR with CR5-B5 of the control register, set CR5-B5 to logic "0" when using this pin. The RG2IN pin is the input to the Regulator 2. The RG2O pin is the output from the Regulator 2, whose voltage is 3.0 V. A 1 µF ceramic type bypass capacitor must be connected between the power input pin and GND, and a 10 µF tantalum bypass capacitor must be connected from the output pin to GND.

Note1: The RG1O and RG2O outputs must not be used as the 3 V supply for the ML7041.
Note2: The RG1IN and RG2IN should be common near the device and supplied from the same power supply.

GP1, GP2, GP3, GP4
General purpose driver output. Each pin is controlled by CR5-B1 through CR5-B4. By selecting CR5-B7, the GP1 pin can be controlled by the receive side sign bit.

V_{DD}, V_A, V_{A1}, V_{A2}, V_{A3}
VDD is the digital power supply. VA, VA1, VA2, and VA3 are the analog power supply pins. Since these pins are separated in the device, connect them as close as possible on the PCB.

DG, AG, AG1, AG2, AG3, AGR1, AGR2, AGGP1, AGGP2
Ground. DG is the digital ground. AG, AG1, AG2, AG3, AGR1, AGR2, AGGP1 and AGGP2 are the analog ground. Since these pins are separated in the device, connect them as close as possible on the PCB.

$\overline{\text{PDN}}$
Power down and reset control input.
When set to digital "L", the device changes to the power down state and the control register is reset. Since the power down mode is controlled by a logical OR with CR0-B5 of the control register, set CR0-B5 to logic "0" when using this pin. The reset pulse width must be 200 ns or more. Be sure to reset the control register after turning on the power.

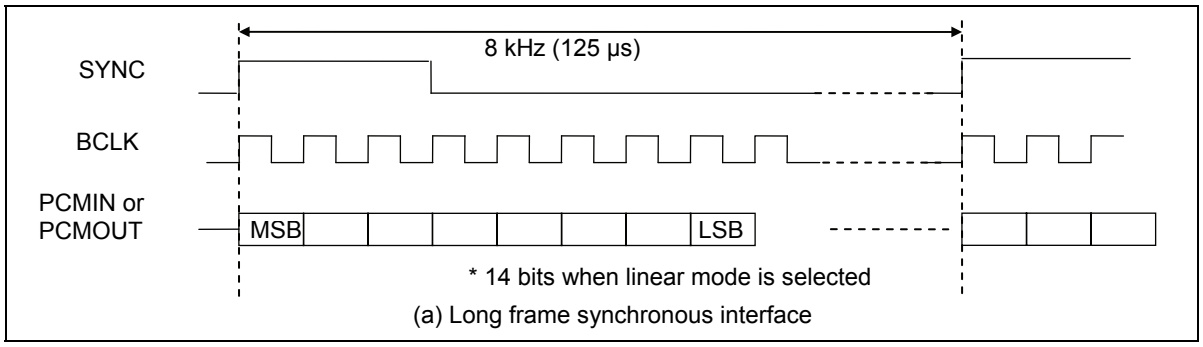
MCK
Master clock input.
The frequency must be 2.048 MHz. MCK can be asynchronous with SYNC and BCLK.
If a frequency of BCLK is 2.048 MHz, the BCLK can be shared with MCK.

BCLK
Shift clock input for the PCM data.
The frequency is set in the range of 64 kHz to 2048 kHz for A/µ-law PCM data and set in the range of 128 kHz to 2048 kHz for linear code selection.

SYNC
8 kHz synchronous signal input for transmit and receive PCM data.
Synchronize this signal with BCLK signal. This signal is used to indicate the MSB of the PCM data stream.

PCMOUT
Transmit PCM data output. The PCM output signal is output from MSB, synchronously with the rising edges of BCLK and SYNC. Refer to Figure 2. This is a logic output pin so that external pull-up is not required. This pin outputs logic "L" except during effective PCM data bits, and outputs logic "H" during power-down.

PCMIN
Receive PCM data input.
The PCM input signal is shifted in on the falling edge of BCLK and is input from MSB.



Refer to Figure 2.

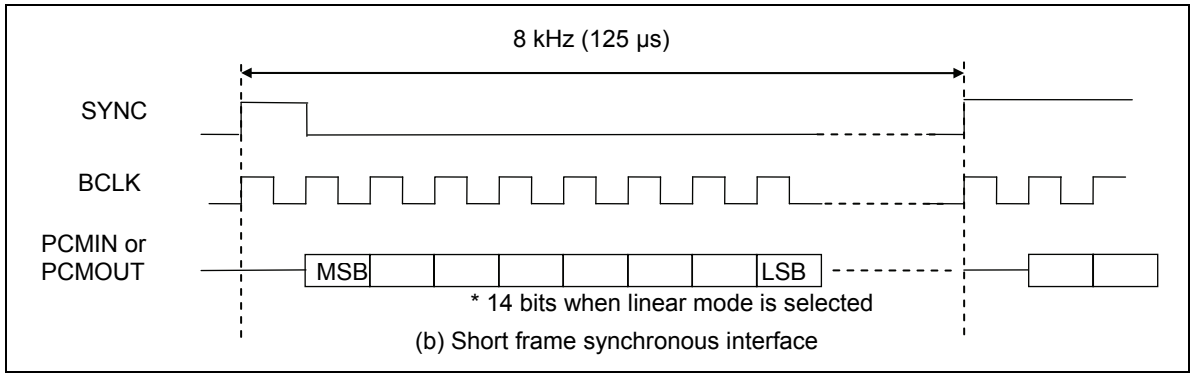


Figure 2 PCM Interface Basic Timing Diagram

SDA, SCL

SDA is the serial data input/output pin and SCL is the serial clock line input pin. A pull-up register of 1 to 10 kΩ is required for the SDA pin. The master clock is required when data is written or read.

Transfer format

The control register can be controlled according to the I^2C bus transfer format.

The control register address is 3 bits long and the register data is 8 bits long. The methods of writing and reading of data are shown below.

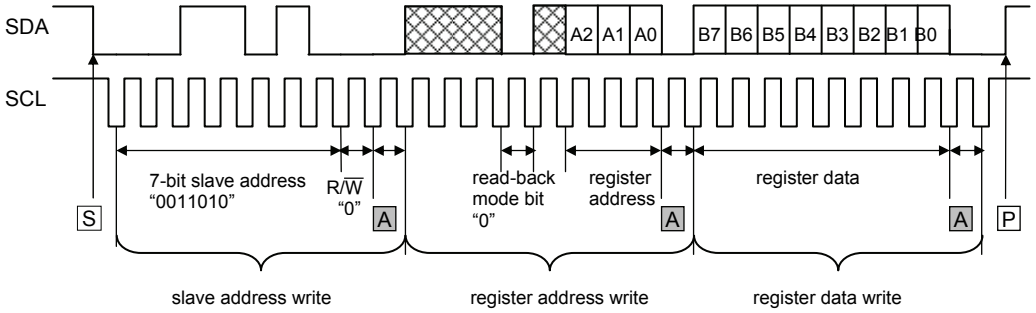


Figure 3 I^2C Interface Write Timing

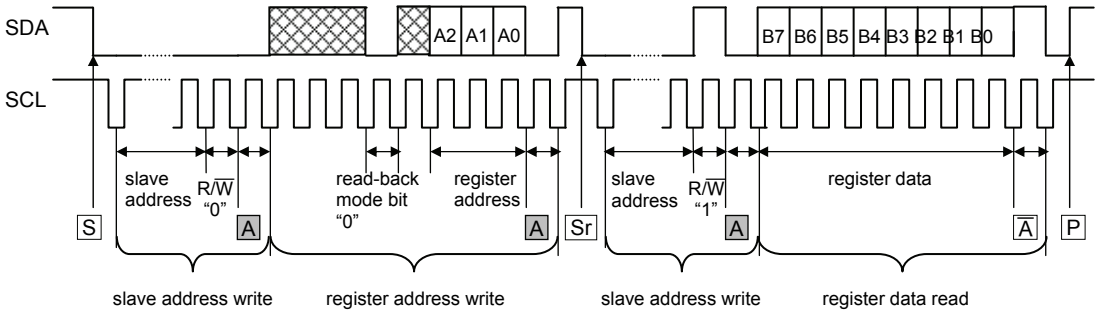


Figure 4 I^2C Interface Read Timing: normal mode

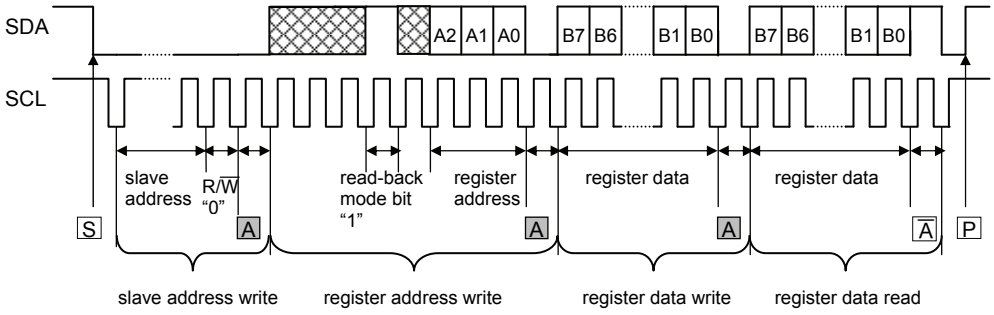


Figure 5 I^2C Interface Read Timing: read-back mode

ML7041 Slave address "0011010"

S START condition	A Acknowledged (ML7041 drive SDA to "0")
P STOP condition	Ā Not Acknowledged
Sr Repeated START condition	⊠ Don't care ("0" or "1")

Table 1 shows the register map.

Table 1 Control Register Map

Name	Address			Control and Detect Data								RW
	A2	A1	A0	B7	B6	B5	B4	B3 B2		B1 B0		
CR0	0	0	0	A/μ SEL	SPOUT PON	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR	R/W
CR1	0	0	1	MIC SEL1	MIC SEL0	SP SEL1	SP SEL0	SHORT FRAME	—	SW C/A	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	SIDE TONE GAIN2	SIDE TONE GAIN1	SIDE TONE GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ OTHERS SEL	TONE SEND	— TONE4		TONE3	TONE2	TONE1	TONE0	R/W
CR5	1	0	1	GP1 SEL CR/TONE	— RG2PDN		RG1PDN	GP4C	GP3C	GP2C	GP1C	R/W
CR6	1	1	0	VOX ON/OFF	ON LVL1	—	—	—	—	—	—	R/W
CR7	1	1	1	VOX OUT	TX NOISE1	TX NOISE0	— —		—	—	—	R

R/W: Read/Write enable R: Read only register

ABSOLUTE MAXIMUM RATINGS

Parameter S	ymbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +4.6	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C
Operating Junction Temperature *	T_{jmax}	—	+150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter S	ymbol	Condition Min.		Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.4	—	3.3	V
Operating Temperature	Ta	—	–40	+25	+85	°C
Operating Junction Temperature (Average) *	T_{jmaxa}	—	—	—	105	°C
Input High Voltage	V_{IH}	all digital input pins	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage	V_{IL}	all digital input pins	0	—	0.20 × V_{DD}	V
Digital Input Rise Time	t_{ir}	all digital input pins	—	—	50	ns
Digital Input Fall Time	t_{if}	all digital input pins	—	—	50	ns
Digital Output Load	C_{DL}	all digital output pins	—	—	100	pF
Bypass Capacitor for SG	C_{SG}	Between SG and AG	0.1	—	—	μF
Master Clock Frequency	F_{MCK}	MCK	–0.01%	2.048	+0.01%	MHz
Bit Clock Frequency	F_{BCK1}	BCLK (A/μ-law) 64		—	2048	kHz
	F_{BCK2}	BCLK (linear)	128	—	2048	kHz
Synchronous Signal Frequency	F_{SYNC}	SYNC	—	8.0	—	kHz
Clock Duty Ratio	D_{CLK}	MCK, BCLK	40	50	60	%
Sync Pulse Setting Time	T_{SB}	SYNC → BCLK	-100	—	100	ns
	T_{BS}	BCLK → SYNC	100	—	—	ns
Synchronous Signal Width	t_{WS}	SYNC	1BCLK	—	100	μs

* The device should be used in such a way that T_{jmax} (average) is less than 105°C.
T_{jmax} is given by the equation:

$T_{jmax} = P \times \theta ja + Ta$

where P = Power dissipation (W)

A 48-pin TQFP package is used.

θja = 195°C (not mounted on a PCB, in still-air-ambient)

θja = 156°C (mounted on a typical PCB, in still-air-ambient)

For more details, refer to PACKAGE INFORMATION DATA BOOK.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition Min.		Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode No signal (V_{DD} = 3.0 V)	0 5.0		11.0	mA
	I_{DD2}	Operating mode No signal (V_{DD} = 3.0 V) SPO+, SPO– or EAR1, 2 is active	0	16.0	32.0	mA
	I_{DD3}	Power down mode (V_{DD} = 3.0 V, Ta = 25°C)	0 1.0		10	μA
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	μA
	I_{IL}	V_I = 0 V	—	—	1.5	μA
Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	0.5 × V_{DD}	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = –1.2 mA	0	0.2	0.4	V
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition Min.		Typ.	Max.	Unit
Input Resistance	R_{INX}	MIC1I, MIC2I, MIC3–, MIC3+	10	—	—	MΩ
Output Load Resistance	R_{LGX1}	MIC1O, MIC2O, MIC3O, EXTO	20	—	—	kΩ
	R_{LGX2}	EAR1O, EAR2O	32	—	—	Ω
	R_{LGX3}	SPO+, SPO– differential output	8	—	—	Ω
Output Load Capacitance	C_{LGX}	Analog output	—	—	50	pF
Output Amplitude *	V_{O1}	MIC1O, MIC2O, MIC3O, EXTO, RL = 20 kΩ	— —		1.3	V_{PP}
		EAR1O, EAR2O, RL = 32 Ω				
	V_{O2}	SPO+, SPO–, (Differential output) V_{DD} = 3.0 V, RL = 8 Ω	— —		2.6	V_{PP}
	V_{O3}	SPO– (Single output) V_{DD} = 3.0 V, RL = 20 kΩ , THD = 1%	2.0 2.6		—	V_{PP}
Total Harmonic Distortion	THD	EAR1O, EAR2O, SPO+, SPO– V_{DD} = 3.0 V (at V_{O1}, V_{O2})	—	—	5.0	%
Offset Voltage	V_{OFGX1}	MIC1O, MIC2O, MIC3O	–40	—	40	mV
	V_{OFGX2}	EAR1O, EAR2O, SPO+, SPO–, EXTO	–100	— 100		mV
SG Output Voltage	V_{SG}	SG	—	1.4	—	V
SG Output Impedance	R_{SG}	SG	—	40	80	kΩ
Internal switch ON Impedance	R_{SW}	All internal analog switches (1.4 V DC bias)	—	—	300	Ω

* –7.7 dBm (600 Ω) = 0 dBm0, +3.17 dBm0 = 1.3 V_{PP}

AC Characteristics

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition			Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)	Others				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0 —		25	—	—	dB
	L_{OSS} T2	300 to 3000			–0.15	—	0.20	dB
	L_{OSS} T3	1020			Reference			dB
	L_{OSS} T4	3300			–0.15	—	0.80	dB
	L_{OSS} T5	3400			0	—	0.80	dB
	L_{OSS} R6	3968.75			13 —		—	dB
Receive Frequency Response *2	L_{OSS} R1	0 to 3000	0 —		–0.15	—	0.20	dB
	L_{OSS} R2	1020			Reference			dB
	L_{OSS} R3	3300			–0.15	—	0.80	dB
	L_{OSS} R4	3400			0	—	0.80	dB
	L_{OSS} R5	3968.75			13 —		—	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3	*1	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		–30		35	—	—	dB
	SD T4		–40		28	—	—	dB
	SD T5		–45		23 —		—	dB
Receive Signal to Distortion Ratio *2	SD R1	1020	3	*1	35	—	—	dB
	SD R2		0		35	—	—	dB
	SD R3		–30		35	—	—	dB
	SD R4		–40		28	—	—	dB
	SD R5		–45		23 —		—	dB
Transmit Gain Tracking	GT T1	1020	3	—	–0.5	—	0.5	dB
	GT T2		–10		Reference			dB
	GT T3		–40		–0.5	—	0.5	dB
	GT T4		–50		–1.0	—	1.0	dB
	GT T5		–55		–1.2	— 1.2		dB
Receive Gain Tracking *2	GT R1	1020	3	—	–0.5	—	0.5	dB
	GT R2		–10		Reference			dB
	GT R3		–40		–0.5	—	0.5	dB
	GT R4		–50		–1.0	—	1.0	dB
	GT R5		–55		–1.2	— 1.2		dB

*1 Use the P-message weighted filter.
*2 EXTO output

AC Characteristics (Continued)

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition			Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)	Others				
Idle Channel Noise	N_{IDLT} —		MIC1I, MIC2I, MIC3 ± = SG	*1	—	—	–68	dBmOp
	N_{IDLR} —		—	*1,*2,*4	—	—	–72	
Absolute Signal Amplitude	A_{VT}	1020 0		MIC1O, MIC2O, MIC3O	0.285	0.320 *3	0.359	Vrms
	A_{VR}			EXTO	0.285	0.320 *3	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT} 30	Noise frequency: 0 to 50 kHz	Noise level: 50 mVpp	—		—	—	dB
	P_{SRRR}				30 —		—	dB
Digital Input/Output Timing PCM Interface	t_{SDX} 0	—	1 LSTTL + 100 pF	See Figure 6		—	200	ns
	t_{XD1} 0					—	200	ns
	t_{XD2} 0					—	200	ns
	t_{XD3}				0 —		200	ns
PCMIN Setup Time	t_{DS} 100	—	—	See Figure 6		—	—	ns
PCMIN Hold Time	t_{DH}				100 —		—	ns
I^2C Interface timing	f_{SCL} 0	—	CL = 50 pF	See Figure 7		—	100	kHz
	t_{BUF} 4.7					—	—	µs
	$t_{HD:STA}$ 4.0					—	—	µs
	t_{LOW} 4.7					—	—	µs
	t_{HIGH} 4.0					—	—	µs
	$t_{SU:STA}$ 4.7					—	—	µs
	$t_{HD:DAT}$ 0					—	—	µs
	$t_{SU:DAT}$ 250					—	—	ns
	$t_{SU:STO}$				4.0 —		—	µs

*1 Use the P-message weighted filter.
*2 PCMIN input code "11010101" (A-law)
"11111111" (µ-law)
*3 0.320 Vrms = 0 dBm0 = –7.7 dBm
*4 EXTO output

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition Min.			Typ.	Max.	Unit
Frequency Difference	D_{FT}	DTMF Tones, Other Tones		–1.5	—	+1.5	%
Original (reference) Tones Signal Level *5	V_{TL}	Transmit tones (gain setting of 0 dB)	DTMF (Low) and Other Tones	–18	–16	–14	dBm0
	V_{TH}		DTMF (High)	–16	–14	–12	dBm0
	V_{RL}	Receive tones (gain setting of –6 dB)	MF (Low)	–4	–2	0	dBm0
	V_{RH}		DTMF (High) and Other Tones	–2	0	+2	dBm0
Relative Level of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		+1	+2	+3	dB

*5 Not including programmable gain set values

AC Characteristics (Programmable Gain Stages)

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition Min.		Typ.	Max.	Unit
Gain Accuracy	D_G	All gain stages, to programmed value	–1	0	+1	dB

AC Characteristics (Voice Detect Function)

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition Min.		Typ.	Max.	Unit
Voice Detection Time	T_{VON}	Silence → Voice (Voice/silence differential: 10 dB)	—	5	—	ms
	T_{VOF}		140	160	180	ms
Voice Detection Accuracy	D_{VX}	For detection level set values by CR6-B6	–2.5	0	2.5	dB

AC Characteristics (General Purpose Drivers)

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

Parameter S	ymbol	Condition Min.		Typ.	Max.	Unit
Output Voltage	V_O	I_{OUT} = 150 mA, GP1 - GP4	—	—	0.7	V
Output Load Resistance	R_O		20 —		—	Ω

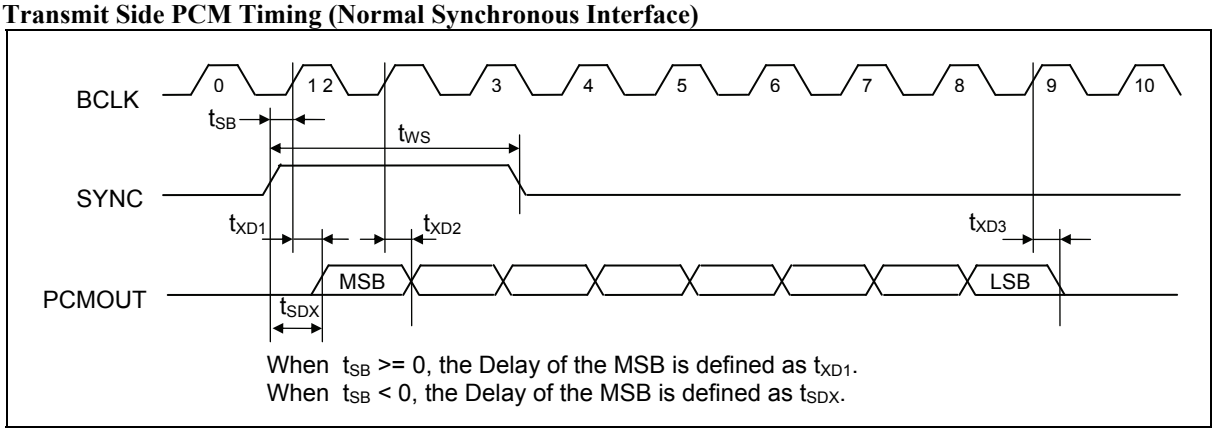
AC Characteristics (Regulator 1 and 2)

(V_{DD} = 2.4 to 3.3 V, Ta = –40 to +85°C)

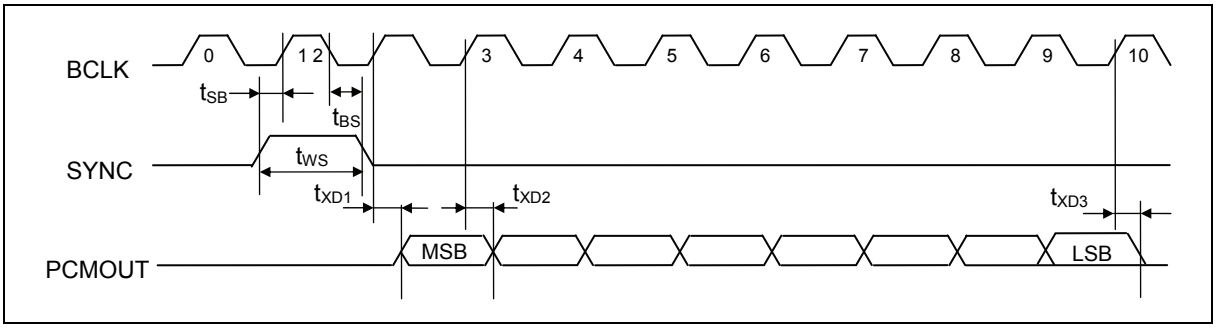
Parameter S	ymbol	Condition Min.		Typ.	Max.	Unit
Input Voltage	V_{i1}	I_{OUT} = 50 mA	3.3	3.6	4.1	V
	V_{i2}	I_{OUT} = 150 mA	3.5	3.6	4.1	V
Output Voltage	V_O	RGIN = 3.6 V, I_{OUT} = 0 mA, Ta = 25°C	2.93	3.00	3.07	V
Load Current	I_O	3.5 V < RGIN < 4.1 V	—	—	150	mA
Dropout Voltage	V_{DROP}	I_{OUT} = 150 mA , RGIN = 3.6 V	—	—	200	mV
Output Voltage Line Regulation	dV_O/dV_I	I_{OUT} = 50 mA 3.3 V < RGIN < 4.1 V, Ta = 25°C	—	0.1	1.25	%/V
Standby Current	I_{stanby}	RG1PDN = 0, RG2PDN = 0		0.1	10	µA

TIMING DIAGRAM

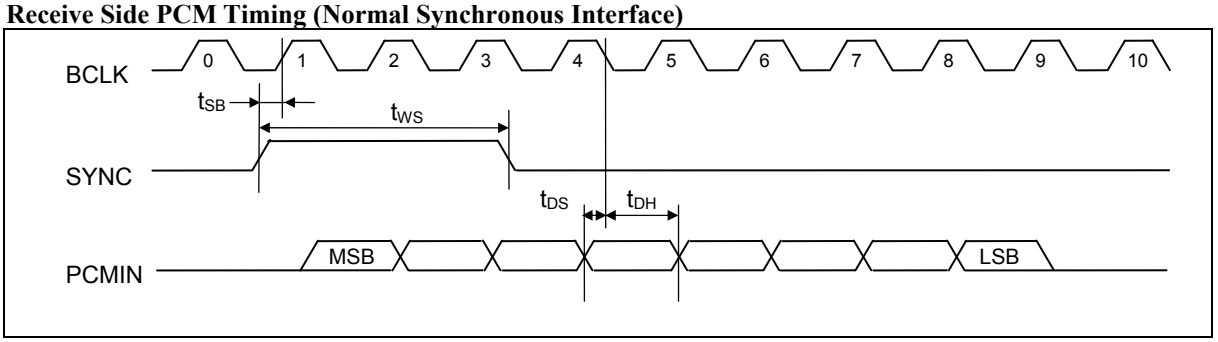
Transmit Side PCM Timing (Normal Synchronous Interface)



Transmit Side PCM Timing (Short Frame Synchronous Interface)



Receive Side PCM Timing (Normal Synchronous Interface)



Receive Side PCM Timing (Short Frame Synchronous Interface)

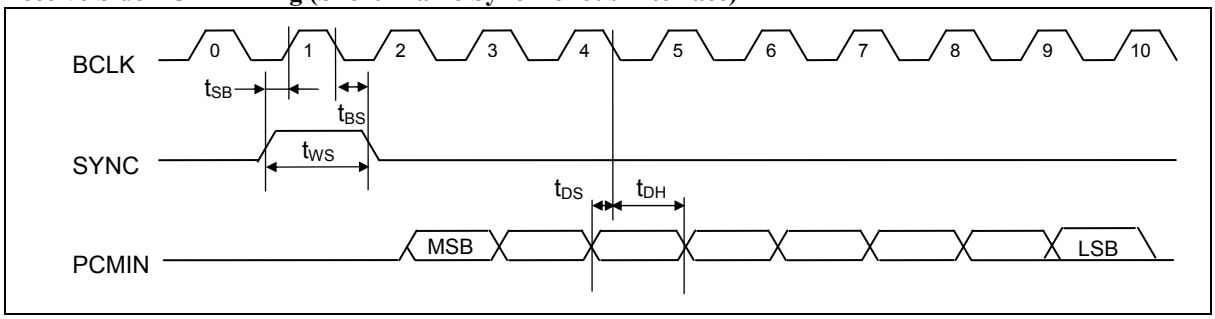


Figure 6 PCM Interface Timing

I²C Interface

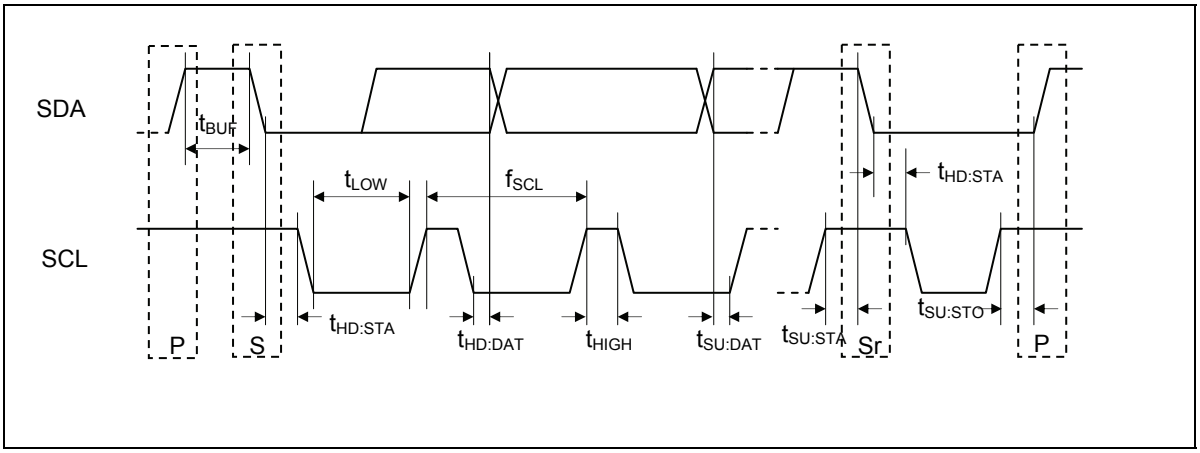


Figure 7 I²C Interface Timing

FUNCTIONAL DESCRIPTION

Control Registers

CR0 (Basic operating mode 1)

Note: The initial value means a value set when the device is reset by the $\overline{PDN}$ pin.

	B7 B6		B5	B4 B3	B2 B1			B0
CR0	A/μ SEL	SPOUT PON	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR
Initial value	0	0	0	0	0	0	0	0

B7 ..... PCM interface companding law select 0: μ-law 1: A-law
B6 ..... Power-on control for output amplifies (SPO+, SPO–) 0: Power down 1: Power on
B5 ..... Power down (entire circuitry) 0: Power on 1: Power down
ORed with the inverted PDN signal. When using this data, set PDN to "L".
The control registers are not reset by this signal.
B4 ..... Power down (transmit only) 0: Power on 1: Power down
B3 ..... Power down (receive only) 0: Power on 1: Power down
B2 ..... Slope filter enable 0: Slope filter disable 1: Slope filter enable
B1 ..... Slope filter frequency response select 0: CASE1 1: CASE2
Either CASE1 or CASE2 can be selected in Figure 8.
B0 ..... PCM interface linear code select
0: PCM companding law selected by CR0-B7
1: 14-bit linear code (2's complement)

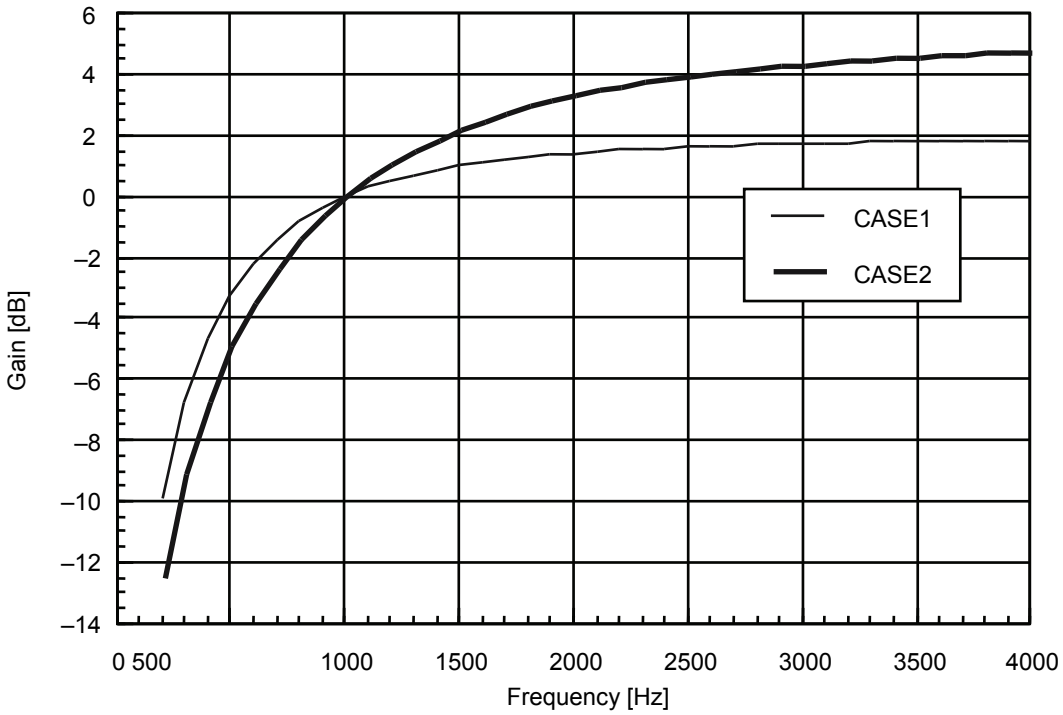


Figure 8 Slope Filter Frequency Characteristics

CR1 (Basic operating mode 2)

	B7 B6		B5	B4 B3	B2 B1			B0
CR1	MIC SEL1	MIC SEL0	SP SEL1	SP SEL0	SHORT FRAME	—	SW C/A	RX PAD
Initial Value	0	0	0	0	0	0	0	0

B7, B6….. Selection of an input amplifier to encoder
(B7, B6) = (0, 0): MIC1
= (0, 1): MIC2
= (1, 0): MIC3
= (1, 1): No input
Amplifiers which are not selected are powered down and their outputs go in the high impedance state.
B5, B4….. Selection of an output amplifier
(B5, B4) = (0, 0): EXTO
= (0, 1): EAR1O
= (1, 0): EAR2O
= (1, 1): No output
Amplifiers which are not selected are powered down and their outputs go in the high impedance state.
B3 ……. Short frame synchronous interface select
0: Long frame synchronous interface,
1: Short frame synchronous interface
B2 ……. Not used. When writing data, write “0”.
B1 ……. Analog switch control 0: The SWB pin is internally connected to the SWA pin.
1: The SWB pin is internally connected to the SWC pin.
The unconnected pins go in a high impedance state.
B0 ……. Receive side PAD 0: No pad
1: A pad of 12 dB loss is inserted in the receive side voice path.

CR2 (PCM CODEC operating mode setting and transmit/receive gain adjustment)

	B7 B6		B5	B4 B3		B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7 ..... Transmit side PCM signal ON/OFF 0: ON 1: OFF
B6, B5, B4 ..... Transmit side signal gain adjustment (refer to Table 2)
B3 ..... Receive side PCM signal ON/OFF 0: ON 1: OFF
B2, B1, B0 ..... Receive side signal gain adjustment (refer to Table 2)

Table 2 Transmit/Receive Gain Settings

B6	B5	B4 T	ransmit Gain B2		B1	B0	Receive Gain
0	0	0 –6	dB 0		0	0	–12 dB
0	0	1 –	4 dB 0		0	1 –	9 dB
0	1	0 –	2 dB 0		1	0 –	6 dB
0	1	1 0	dB 0		1	1	–3 dB
1	0	0 +	2 dB 1		0	0	0 dB
1	0	1 +	4 dB 1		0	1 +	3 dB
1	1	0 +	6 dB 1		1	0 +	6 dB
1	1	1 +	8 dB 1		1	1 +	9 dB

The above gain settings table shows the transmit/receive voice signal gain settings and the transmit side gain settings for DTMF tones and other tones. The DTMF and other tone transmit signals are enabled by CR4-B6, and the gain setting is referenced to the levels shown below.

DTMF tones (low group): ..... –16 dBm0
DTMF tones (high group) and other tones: ... –14 dBm0

For example, if the transmit gain set value is set to +8 dB (B6, B5, B4) = (1,1,1), then the following tones are output at the PCMOUT pin.

DTMF tones (low group): ..... –8 dBm0
DTMF tones (high group) and other tones: ... –6 dBm0

Gains of the side tone (path to receive side from transmit side) and the receive side tone can be set by register CR3.

CR3 (Side tone and other tone generator gain setting)

	B7	B6	B5	B4 B3	B2 B1 B0			
CR3	SIDE TONE GAIN2	SIDE TONE GAIN1	SIDE TONE GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5 .....Side tone path gain setting (refer to Table 3)
B4 .....Tone generator ON/OFF 0: OFF 1: ON
B3, B2, B1, B0....Tone generator gain adjustment for receive side (refer to Table 4)

Table 3 Side Tone Gain Settings

B7	B6	B5	Side Tone Path Gain
0 0		0	OFF
0 0		1	–15 dB
0 1		0	–13 dB
0 1		1	–11 dB
1 0		0	–9 dB
1 0		1	–7 dB
1 1		0	–5 dB
1 1		1	–3 dB

Table 4 Receive Side Tone Generator Gain Settings

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0 0		0 0		OFF	1 0	0 0			–20 dB
0 0		0 1		–34 dB	1 0	0 1			–18 dB
0 0		1 0		–32 dB	1 0	1 0			–16 dB
0 0		1 1		–30 dB	1 0	1 1			–14 dB
0 1		0 0		–28 dB	1 1	0 0			–12 dB
0 1		0 1		–26 dB	1 1	0 1			–10 dB
0 1		1 0		–24 dB	1 1	1 0			–8 dB
0 1		1 1		–22 dB	1 1	1 1			–6 dB

The receive side tone generator gain settings shown in Table 4 are referenced to the following levels as a reference.

DTMF tones (low group): .....+4 dBm0
DTMF tones (high group) and others tones: . +6 dBm0

For example, if the tone g enerator gain set value i s set to –6 dB (B3, B2, B1, B0) = (1, 1, 1, 1), then tones at the following levels are output at EXTO.

DTMF tone (low group): .....–2 dBm0
DTMF tone (high group) and other tones:..... 0 dBm0

CR4 (Tone generator operating mode and frequency select)

	B7	B6 B5 B4 B3 B2				B1 B0	
CR4	DTMF/ Others SEL	TONE SEND	— TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7 .....DTMF or other tones select 0: Others 1: DTMF
B6 .....Tone transmit enable (Transmit side) 0:Voice signal transmit 1: Tone transmit
B5 .....Not used. When writing data, write “0”.
B4, B3, B2, B1, B0 ..Tone frequency setting (refer to Tables 5-1 and 5-2)

(a) B7 = 1 (DTMF tone)

Table 5-1 Tone Generator Frequency Settings

B4	B3	B2		B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
*	0	0		0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0		0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0		1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0		1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz + 1633 Hz
*	0	1		0	0	770 Hz + 1209 Hz	*	1	0	0	0	941 Hz + 1209 Hz
*	0	1		0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1		1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1		1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

*Und efined

(b) B7 = 0 (Other tones)

Table 5-2 Tone Generator Frequency Settings

B4	B3	B2	B1	B0		Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0		2730 Hz/2500 Hz 8 Hz wamb.	1	0	0	0	0	1200 Hz
0	0	0	0	1		2000 Hz/2667 Hz 8 Hz wamb.	1	0	0	0	1	1300 Hz
0	0	0	1	0		1000 Hz/1333 Hz 8 Hz wamb.	1	0	0	1	0	
0	0	0	1	1		—	1	0	0	1	1	1477 Hz
0	0	1	0	0		—	1	0	1	0	0	1633 Hz
0	0	1	0	1		—	1	0	1	0	1	2000 Hz
0	0	1	1	0		—	1	0	1	1	0	2100 Hz
0	0	1	1	1		—	1	0	1	1	1	
0	1	0	0	0		—	1	1	0	0	0	2400 Hz
0	1	0	0	1		400 Hz	1	1	0	0	1	
0	1	0	1	0		440 Hz	1	1	0	1	0	2500 Hz
0	1	0	1	1		480 Hz	1	1	0	1	1	
0	1	1	0	0		—	1	1	1	0	0	
0	1	1	0	1		667 Hz	1	1	1	0	1	2700 Hz
0	1	1	1	0		800 Hz	1	1	1	1	0	
0	1	1	1	1		1000 Hz	1	1	1	1	1	3000 Hz

CR5 (Regulator control, General purpose driver control)

	B7 B6	B5 B4 B3 B2					B1 B0	
CR5	GP1 SEL CR/TONE	—	RG2PDN	RG1PDN	GP4C	GP3C	GP2C	GP1C
Initial Value	0	0	0	0	0	0	0	0

B7 .....Selection of how to control General purpose driver 1.
0: Control register CR5-B0 1: GP1 is controlled by a sign bit of the receiver.
B6 .....Not used
B5 .....Power down control for Regulator 2
0: Power down 1: Power on
When using this data, set the RG2PDN pin at a “L” level.
B4 .....Power down control for Regulator 1
0: Power down 1: Power on
When using this data, set the RG1PDN pin at a “L” level.
B3, B2, B1, B0....General purpose driver control
0: Off (high impedance) 1: On (“L” output)

CR6 (VOX function control)

	B7 B6		B5 B4 B3			B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	— — —			—	—	—
Initial Value	0	0	*	0	0	0	0	0

B7 .....Voice/silence detect function ON/ OFF 0: OFF 1: ON
If B7 is set to a logic “1”, B3 should be set to a logic “1”.
B6 .....Voice detector level setting
0: –26 dBm0 1: –38 dBm0
B5 .....Reserved bit. When writing data, write “0”.
B4, B3, B2, B1, B0 .....Not used. When writing data, write “0”.

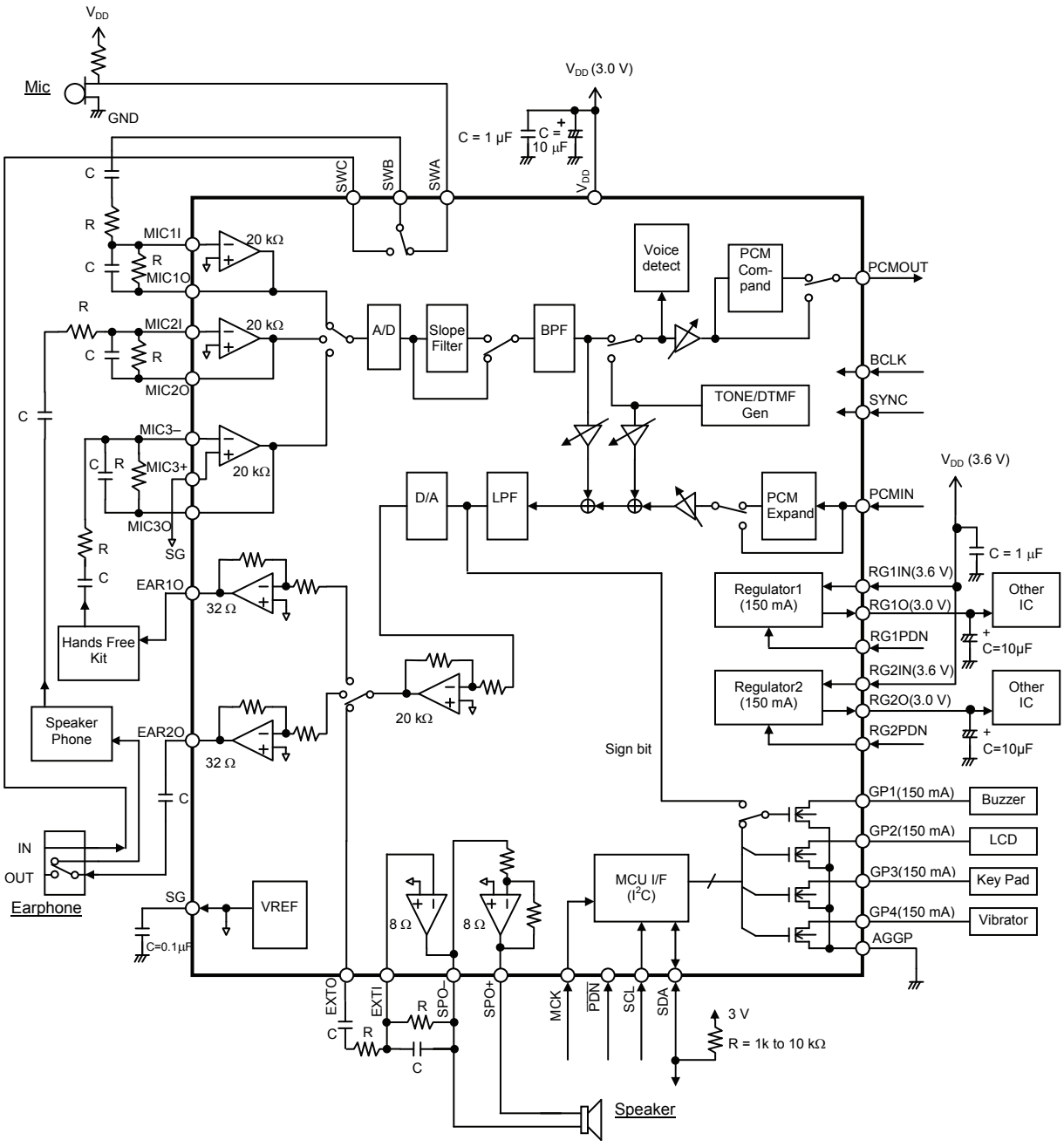
CR7 (Detect register, read only)

	B7 B6	B5 B4 B3 B2 B1						B0
CR7	VOX OUT	TX Noise Level1	TX Noise Level0	—	—	—	—	—
Initial Value	0	0	0	*	*	*	*	*

*Used for testing the device and undefined

B7 ..... Transmit side voice/silence detection 0: silence 1: voice detect
B6, B5..... Transmit side silence detect level (indicator)
(0,0): Below –50 dBm0 (0,1): –40 to –50 dBm0
(1,0): –30 to –40 dBm0 (1,1): Above –30 dBm0
Note: These outputs are enabled only when the VOX (CR6-B7) = “1”.
B4, B3, B2, B1, B0 .... Not used

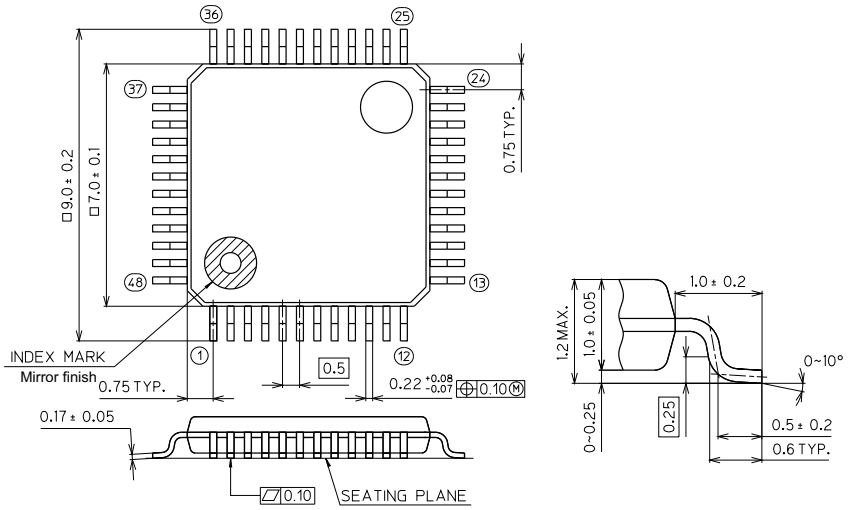
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit: mm)

TQFP48-P-0707-0.50-K



LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.13 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Notes for Mounting the Surface Mount Type Package

The su rface mount type packa ges ar e very susce ptible to hea t in reflow m ounting a nd humidity absorbed in storage.
Therefore, before you pe rform refl ow mounting, co ntact RO HM's re sponsible sales p erson for the product name, package n ame, pin number, pa ckage co de and desire d mou nting con ditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7041-01 Nov.	2000	—	—	1st Edition
FEDL7041-02	Jun. 16, 2004	8	8	More clarification of PCMOUT output state
FEDL7041-03	Nov. 2, 2005	11	11	Addition of t_{SB}
		17 17		Addition of t_{SB} Addition of description about t_{XD1} and t_{SDX}
FEDL7041-04	Mar. 2, 2006	24	24	Addition of description about CR6-B3
FEDL7041-05	Dec. 3, 2007	14	14	Addition of t_{DS}, t_{DH}
		17 17		Corrected Figure 6 PCM Interface Timing Receive Side PCM Timing
		23 23		Addition of "—" to blanks in table 5-2 Tone Generator

NOTES

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