ML7204-003

VoIP CODEC

GENERAL DESCRIPTION

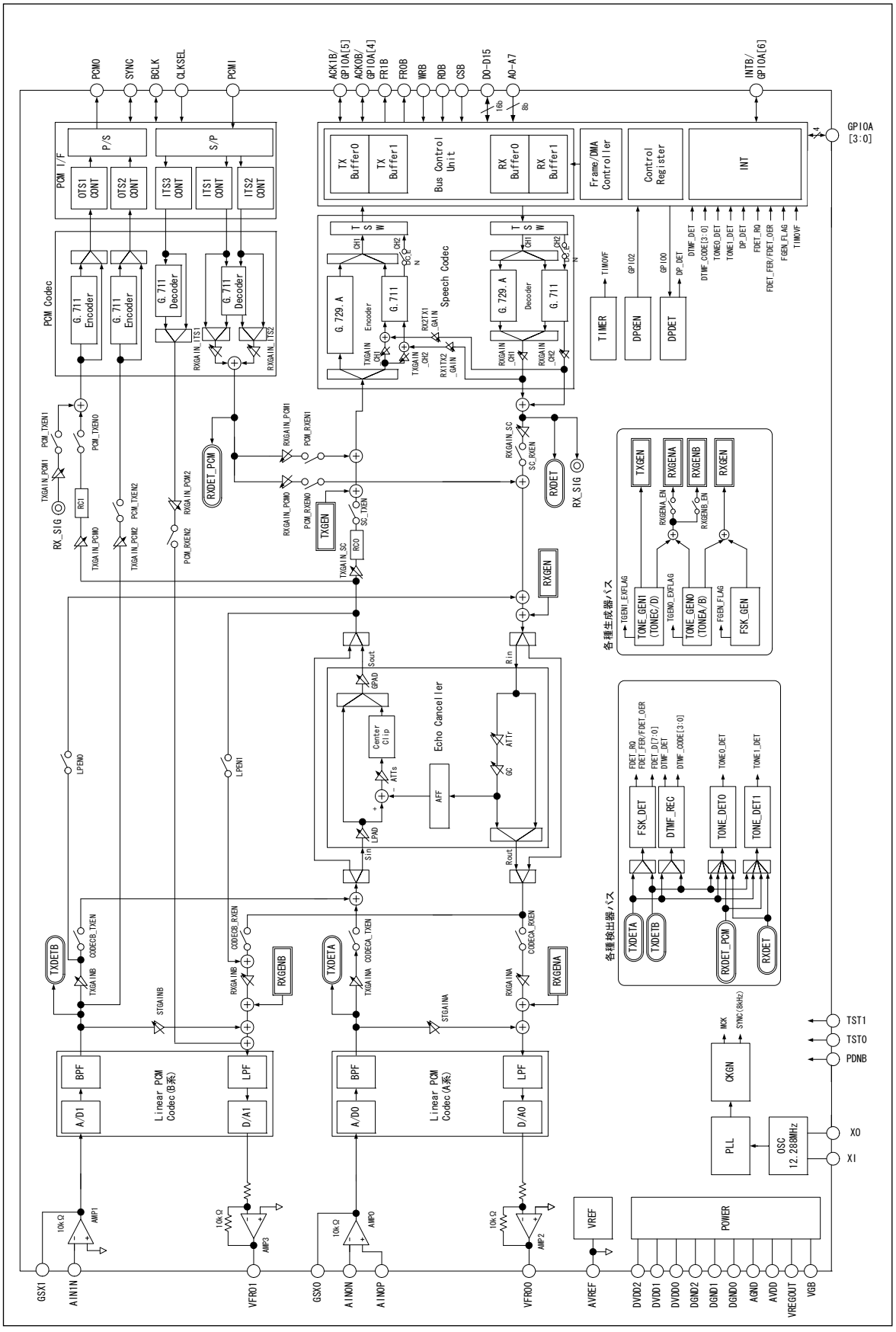
The ML7204-003 is a speech CODEC for VoIP. As a speech CODEC, this LSI allows selection of G.729.A/G711 and supports the PLC (Packet Loss Concealment) function.
With an echo canceler that handles 32 ms-delay and FSK detection/generation, DTMF detection/generation, and tone detection/generation functions, the ML7204-003 is the most suitable LSI for adding the VoIP function to TAs and routers.

FEATURES

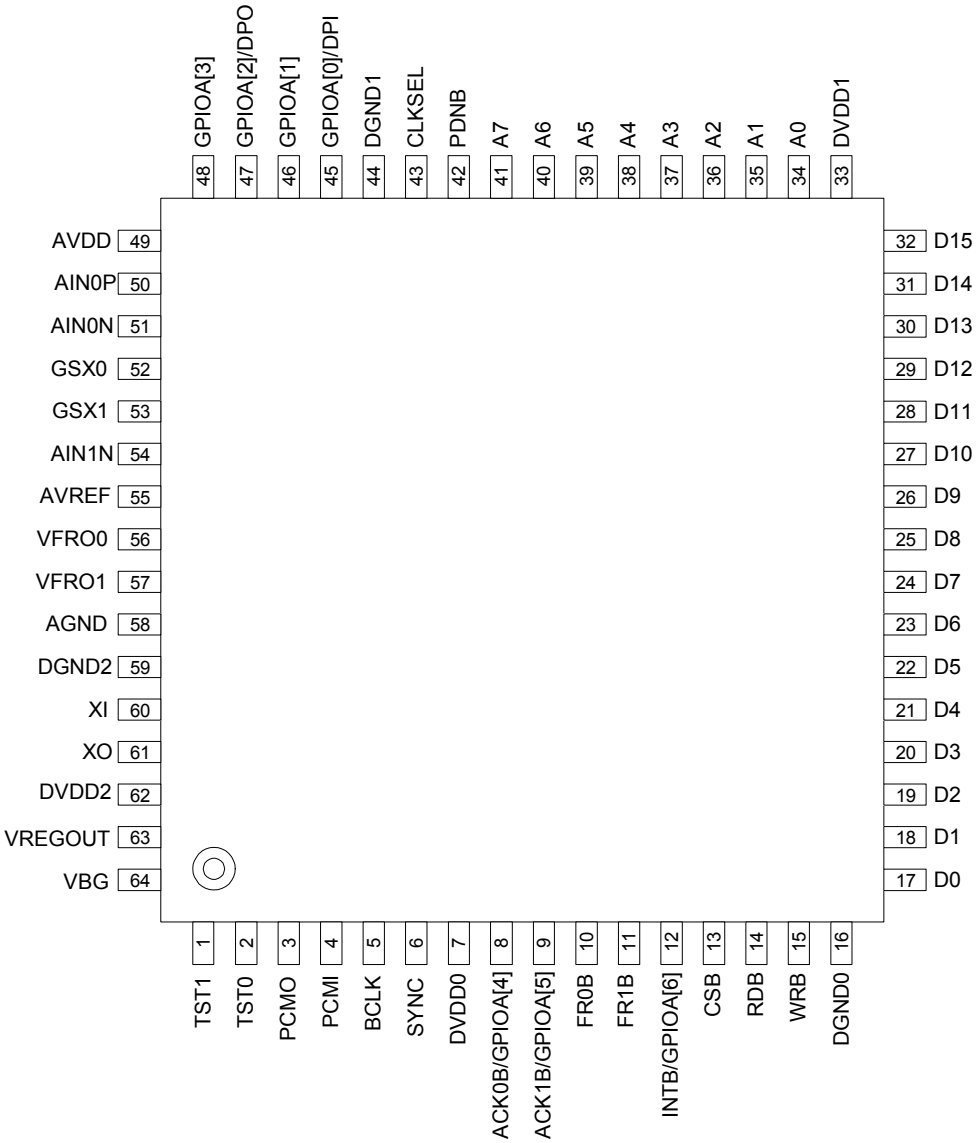
- Power supply voltage
  Digital power supply voltage (DVDD0, 1, 2): 3.0 to 3.6 V
  Analog power supply voltage (AVDD): 3.0 to 3.6 V
- Speech CODEC:
  G.729.A (8 kbps)/G.711 (64 kbps) μ-law and A-law (supports individual setting for transmission and reception)
  Supports ITU-T G.711 Appendix 1 compliant PLC (Packet Loss Concealment) function
  Supports the 2-channel processing function (for 3-way communication)
- Built-in FIFO buffer (640 bytes) for transmission/reception data transfer
  Allows selection of Frame/DMA (slave) interface
- Provided with echo canceler for handling 32 ms delay and Range Controllers
- DTMF detection
- DTMF generation (the tone generation function enables generation of DTMF signals)
- Tone detection: 2 types (1650 Hz and 2100 Hz: Detection frequency can be changed)
- Tone generation: 2 types
- FSK detection
- FSK generation
- Built-in 16-bit timer: 1 channel
- Dial pulse detection function (secondary function of general-purpose I/O ports)
- Dial pulse transmission function (secondary function of general-purpose I/O ports)
- General-purpose I/O ports : Equipped with 7 ports (with some of them having secondary function allocation)
- Two types of built-in linear PCM CODEC (CODEC_A and CODEC_B)
- Analog interface
  CODEC_A side: Incorporates one type each of input amplifier and output amplifier (10 kΩ driving)
  CODEC_B side: Incorporates one type each of input amplifier and output amplifier (10 kΩ driving)
- PCM interface coding format:
  Allows selection of 16-bit linear/G.711 (64 kbps) μ-law or A-law
- PCM serial transmission rate: 64 kHz to 2.048 MHz (fixed to 2.048 MHz for output)
- PCM time slot assignment function (allows up to 2 slots for input and 1 slot for output individually)
  When set to μ-law/A-law: Supports up to 32 slots (BCLK: 2.048 MHz)
  When set to 16-bit linear: Supports up to 16 slots (BCLK: 2.048 MHz)

- Master clock frequency:
  12.288 MHz (crystal; external input)
- Supports hardware and software power down
- Package:
  64-pin plastic QFP (QFP64-P-1414-0.80-BK) (ML7204-003GA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

PIN DESCRIPTIONS

Pin		Symbol	I/O	When PDNB = "0"	Description
	QFP64				
	1	TST1	I	"0"	Test control input 1: Normally, input "0".
	2	TST0	I	"0"	Test control input 0: Normally, input "0".
	3	PCMO	O	"Hi-z"	PCM data output [Open drain output pin]
	4	PCMI	I	I	PCM data input
	5	BCLK	I/O	I	CLKSEL = "0" PCM shift clock input
				"L"	CLKSEL = "1" PCM shift clock output
	6	SYNC	I/O	I	CLKSEL = "0" PCM synchronous signal 8 kHz input
				"L"	CLKSEL = "1" PCM synchronous signal 8 kHz output
	7	DVDD0	—	—	Digital power supply
	8	ACK0B/GPIOA[4]	I/O	I	Transmit buffer DMA access acknowledge signal input (primary function) General-purpose I/O port A[4] (secondary function) [5 V tolerant pin]
	9	ACK1B/GPIOA[5]	I/O	I	Receive buffer DMA access acknowledge signal input (primary function) General-purpose I/O port A [5] (secondary function) [5 V tolerant pin]
	10	FR0B (DMARQ0B)	O	"H"	FR0B:(FD_SEL = "0") Transmit buffer frame signal output DMARQ0B: (FD_SEL = "1") Transmit buffer DMA access request signal output
	11	FR1B (DMARQ1B)	O	"H"	FR1B: (FD_SEL = "0") Receive buffer frame signal output DMARQ1B: (FD_SEL = "1") Receive buffer DMA access request signal output
	12	INTB/GPIOA[6]	I/O	"H"	Interrupt request output (primary function) General-purpose I/O port A [6] (secondary function) [5 V tolerant pin]
	13	CSB	I	I	Chip select control input
	14	RDB	I	I	Read control input
	15	WRB	I	I	Write control input
	16	DGND0	—	—	Digital ground (0.0 V)
	17	D0	I/O	I	Data input-output
	18	D1	I/O	I	Data input-output
	19	D2	I/O	I	Data input-output
	20	D3	I/O	I	Data input-output
	21	D4	I/O	I	Data input-output
	22	D5	I/O	I	Data input-output
	23	D6	I/O	I	Data input-output
	24	D7	I/O	I	Data input-output

Pin		Symbol	I/O	When PDNB = “0”	Description
	QFP64				
	25	D8	I/O	I	Data input-output. Fix the input to “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	26	D9	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	27	D10	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	28	D11	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	29	D12	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	30	D13	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	31	D14	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	32	D15	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = ”1”).
	33	DVDD1	—	—	Digital power supply
	34	A0	I	I	Address input
	35	A1	I	I	Address input
	36	A2	I	I	Address input
	37	A3	I	I	Address input
	38	A4	I	I	Address input
	39	A5	I	I	Address input
	40	A6	I	I	Address input
	41	A7	I	I	Address input
	42	PDNB	I	“0”	Power-down input “0”: Power-down reset ”1”: Normal operation
	43	CLKSEL	I	I	SYNC/BCLK input-output control input “0”: SYNC/BCLK are configured to be input “1”: SYNC/BCLK are configured to be output
	44	DGND1	—	—	Digital ground (0.0 V)
	45	GPIOA[0]/DPI	I/O	I	General-purpose I/O port A[0] [5 V tolerant pin] Secondary function: Input pin for dial pulse detection
	46	GPIOA[1]	I/O	I	General-purpose I/O port A[1] [5 V tolerant pin]
	47	GPIOA[2]/DPO	I/O	I	General-purpose I/O port A[2] [5 V tolerant pin] Secondary function: Output pin for dial pulse transmission
	48	GPIOA[3]	I/O	I	General-purpose I/O port A[3] [5 V tolerant pin]
	49	AVDD	—	—	Analog power supply
	50	AIN0P	I	I	AMP0 non-inverting input
	51	AIN0N	I	I	AMP0 inverted input

Pin		Symbol	I/O	When PDNB = "0"	Description
	QFP64				
	52	GSX0	O	"Hi-z"	AMP0 output (10 kΩ driving)
	53	GSX1	O	"Hi-z"	AMP1 output (10 kΩ driving)
	54	AIN1N	I	I	AMP1 inverted input
	55	AVREF	O	"L"	Analog signal ground (1.4 V)
	56	VFRO0	O	"Hi-z"	AMP2 output (10 kΩ driving)
	57	VFRO1	O	"Hi-z"	AMP3 output (10 kΩ driving)
	58	AGND	—	—	Analog ground (0.0 V)
	59	DGND2	—	—	Digital ground (0.0 V)
	60	XI	I	I	12.288 MHz crystal interface, 12.288 MHz clock input
	61	XO	O	"H"	12.288 MHz crystal interface
	62	DVDD2	—	—	Digital power supply
	63	VREGOUT	—	—	Internal regulator voltage output pin (approx. 2.5 V)
	64	VBG	—	—	Internal regulator reference voltage output pin

* Explanation of symbols used in the PDNB = "0" column

The symbols denote the following pin conditions when PDNB = "0":

"I" : Input a High or Low level signal to the pin.
"0" : Input a Low level signal to the pin
"H" : A High level signal is output from the pin.
"L" : A Low level signal is output from the pin.
"Hi-Z" : The pin goes into a Hi-Z state.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Analog power supply voltage	AVDD	—		–0.3 to +4.6	V
Digital power supply voltage	DVDD	—		–0.3 to +4.6	V
Analog input voltage	VAIN	Analog pin		–0.3 to AVDD+0.3	V
Digital input voltage	VDIN1	Normal digital pin		–0.3 to DVDD+0.3	V
	VDIN2	5 V tolerant pin	DVDD = 3.0 to 3.6 V	–0.3 to +6.0	V
			DVDD < 3.0 V	–0.3 to DVDD+0.3	V
Output current	IO	—		–20 to +20	mA
Power dissipation	PD	Ta = 60 °C, per package		350	mW
Storage temperature	Tstg	—		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog power supply voltage	AVDD	—	3.0	3.3	3.6	V
Digital power supply voltage	DVDD	—	3.0	3.3	3.6	V
Operating temperature range	Ta	—	–20	—	+60	°C
Digital high-level input voltage	VIH1	Normal digital pin	0.75 × DVDD	—	DVDD+ 0.3	V
	VIH2	5 V tolerant pin	0.75 × DVDD	—	5.5	V
Digital low-level input voltage	VIL	Digital pin	–0.3	—	0.19 × DVDD	V
Digital input rise time	tIR	Digital pin	—	2	20	ns
Digital input fall time	tIF	Digital pin	—	2	20	ns
Digital output load capacitance	CDL	Digital pin	—	—	50	pF
Digital output load resistance	RDL	Pull-up resistance, PCMO	500	—	—	Ω
AVREF bypass capacitor	Cvref	Between AVREF-AGND	2.2+0.1	—	4.7+0.1	μF
VREGOUT bypass capacitor	Cvout	Between VREGOUT-DGND	—	10+0.1	—	μF
VBG bypass capacitor	CVBG	Between VBG-DGND	—	150	—	pF
Master clock frequency	Fmck	MCK	–0.01%	12.288	+0.01%	MHz
PCM shift clock frequency	Fbclk	BCLK (at input)	64 (±0.1%)	—	2048 (±0.1%)	kHz
PCM synchronous signal frequency	Fsync	SYNC (at input)	–0.1%	8.0	+0.1%	kHz
Clock duty ratio	DRCLK	MCK, BCLK (at input)	40	50	60	%
PCM synchronous timing	tBS	BCLK to SYNC (at input)	100	—	—	ns
	tSB	SYNC to BCLK (at input)	100	—	—	ns
PCM synchronous signal width	tWS	SYNC (at input)	1BCLK	—	100	μs

(Note) On power-on/shut-down sequence
For the analog power supply voltage (AVDD) and the digital power supply voltage (DVDD) to be supplied to this LSI, it is recommended that power be applied to them simultaneously. However, if simultaneous power-up is difficult due to the power supply circuit configuration, power them up in the order of DVDD → AVDD.
The power supplies should be shut down in the reverse order of power-on sequence.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	ISS	Standby state (PDNB = ”0”, DVDD = AVDD=3.3 V, Ta = 25°C)	—	200	500	μA
	IDD1	Operating status 1 Speech CODEC activated/PCM I/F not used SC_EN = ”1”, AFEA_EN = ”0”, AFEB_EN = ”1”, XI, XO: 12.288 MHz crystal connected	—	45	55	mA
	IDD2	Operating status 2 Speech CODEC activated/PCM I/F used SC_EN = ”1”,PCMI1_EN = ”1”, PCMO1_EN = ”1”, AFEA_EN=”0”, AFEB_EN=”0” XI, XO: 12.288 MHz crystal connected	—	50	65	mA
Digital input pin Input leakage current	IIH	Vin = DVDD	—	0.01	10	μA
	IIL	Vin = DGND	–10	–0.01	—	μA
Digital I/O pin Output leakage current	IOZH	Vout = DVDD	—	0.01	10	μA
	IOZL	Vout = DGND	–10	—	—	μA
High-level output voltage	VOH	Digital output pins, I/O pin IOH = 4.0 mA IOH = 0.5 mA (XO pin) IOH = 1 2.0 mA (CLKOUT pin)	0.78 × DVDD	—	—	V
Low-level output voltage	VOL1	Digital output pins, I/O pin IOL = –4.0 mA IOL = –0.5 mA (XO pin) IO = –12.0 mA (CLKOUT pin)	—	—	0.4	V
	VOL2	Open drain output pins IOL = –12.0 mA	—	—	0.4	V
Input capacitance (*1)	CIN1	Input pins	—	6	—	pF
	CIN2	I/O pins	—	10	—	pF

*1 Design guaranteed value

Analog Interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1 ,2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input resistance (*1)	RIN	AIN0N, AIN0P, AIN1N	10	—	—	MΩ
Output load resistance	RL	GSX0, GSX1, VFRO0, VFRO1	10	—	—	kΩ
Output load capacitance	CL	Analog output pins	—	—	50	pF
Offset voltage	VOF	VFRO0, VFRO1	–40	—	+40	mV
Output voltage level (*2)	VO	GSX0, GSX1, VFRO0, VFRO1 RL = 10kΩ, AMP input 1.3 Vpp	1.158	1.3	1.458	Vpp

*1 Design guaranteed value

*2 –7.7 dBm (600Ω) = 0 dBm0, +3.17 dBm0 = 1.3 Vpp

AC Characteristics in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)				
Transmit frequency characteristics	LT1	0 to 60	0	25	—	—	dB
	LT2	300 to 3000		–0.15	—	0.20	dB
	LT3	1020		Reference			—
	LT4	3300		–0.15	—	0.80	dB
	LT5	3400		0	—	0.80	dB
	LT6	3968.75		13	—	—	dB
Receive frequency characteristics	LR2	0 to 3000	0	–0.15	—	0.20	dB
	LR3	1020		Reference			—
	LR4	3300		–0.15	—	0.80	dB
	LR5	3400		0	—	0.80	dB
	LR6	3968.75		13	—	—	dB
Transmit signal-to-noise ratio (*1)	SDT1	1020	3	35	—	—	dBp
	SDT2		0	35	—	—	dBp
	SDT3		–30	35	—	—	dBp
	SDT4		–40	28	—	—	dBp
	SDT5		–45	23	—	—	dBp
Receive signal-to-noise ratio (*1)	SDR1	1020	3	35	—	—	dBp
	SDR2		0	35	—	—	dBp
	SDR3		–30	35	—	—	dBp
	SDR4		–40	28	—	—	dBp
	SDR5		–45	23	—	—	dBp
Transmit inter-level loss errors	GTT1	1020	3	–0.2	—	0.2	dB
	GTT2		–10	Reference			—
	GTT3		–40	–0.2	—	0.2	dB
	GTT4		–50	–0.6	—	0.6	dB
	GTT5		–55	–1.2	—	1.2	dB
Receive inter-level loss errors	GTR1	1020	3	–0.2	—	0.2	dB
	GTR2		–10	Reference			—
	GTR3		–40	–0.2	—	0.2	dB
	GTR4		–50	–0.6	—	0.6	dB
	GTR5		–55	–1.2	—	1.2	dB
Idle channel noise (*1)	NIDLT	—	Analog input = AVREF	—	—	–70	dBm0p
	NIDLR	—	PCMI = ”1”	—	—	–70	dBm0p
Transmit absolute level (*2)	AVT	1020	0	0.285	0.320	0.359	Vrms
Receive absolute level (*2)	AVR	1020	0	0.285	0.320	0.359	Vrms

*1 P-message weighted filter used

*2 0.320 Vrms = 0 dBm0 = –7.7 dBm (600Ω)

AC Characteristics (Gain Setting) in Speech CODEC = G.711 (μ-law) mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/receive gain setting accuracy	GAC	For all gain set values	–1.0	—	1.0	dB

AC Characteristics (Tone Output) in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency deviation	fDFT	For all frequency set values	–1.5	—	1.5	%
Output level	oLEV	For all gain set values	–2.0	—	2.0	dB

AC characteristics (DTMF Detector and Other Detectors) in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

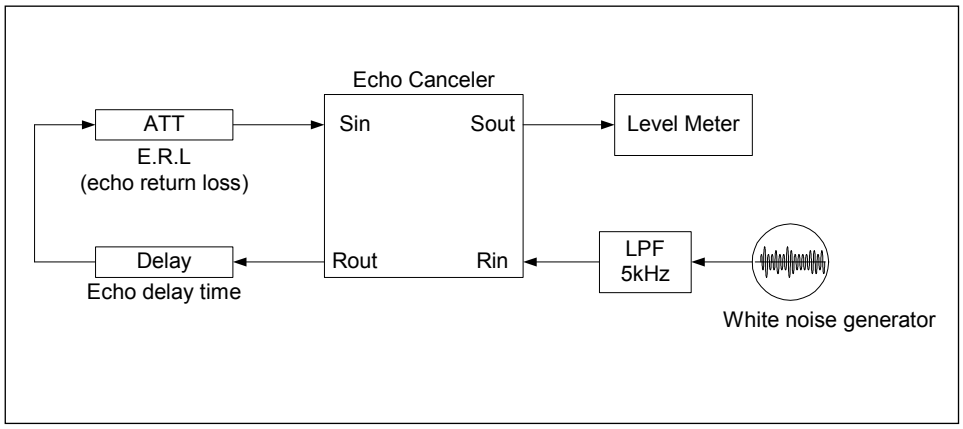
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection level accuracy	dLAC	For all detection level set values	–2.5	—	2.5	dB

AC characteristics (Echo Canceler)

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo attenuation	eRES	—	—	35	—	dB
Erasable echo delay time	tECT	—	—	—	32	ms

Measuring method



Timings of PDNB, XO, and AVREF

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-down signal pulse width	tPDNB	PDNB pin	250	—	—	μs
AVDD supply delay time	tAVDDON	—	0	—	—	ns
Oscillation activation time	txtal	—	—	—	20	ms
AVREF rise time	tAVREF	AVREF = 1.4 (90%) C5 = 4.7 μF, C6 = 0.1 μF (See Figure 9)	—	—	600	ms
		AVREF = 1.4 (90%) C5 = 2.2 μF, C6 = 0.1 μF (See Figure 9)	—	—	300	ms

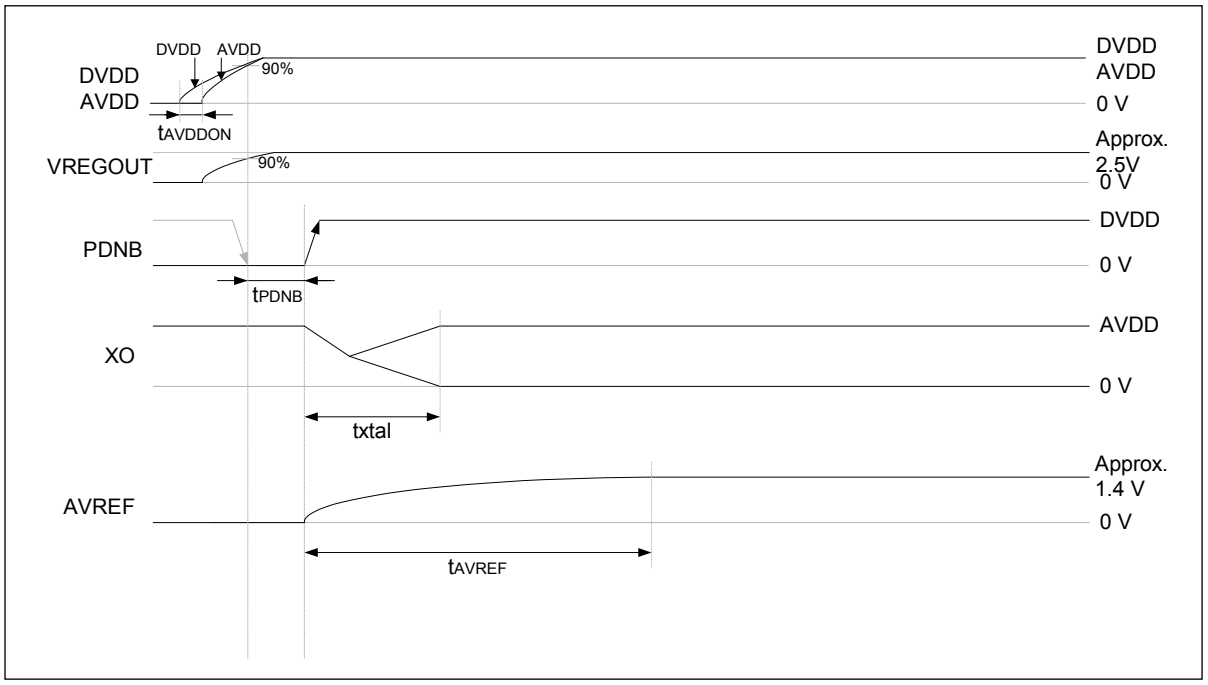


Figure 1 Timings of PDNB, XO, and AVREF

(Note)
The capacitance of the AVREF capacitor (C5) affects the AVREF rise time and analog characteristics. If weight is given to the analog characteristics, specify 4.7 μF, and if it is given to the AVREF rise time, specify 2.2 μF. The electrical characteristics for the analog characteristics that are described above are guaranteed in both capacitances.

PCM interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit clock frequency	fBCLK	CDL = 20 pF (during output)	–0.1%	2.048	+0.1%	MHz
Bit clock duty ratio	dBCLK	CDL = 20 pF (during output)	45	50	55	%
Synchronous signal frequency	fSYNC	CDL = 20 pF (during output)	–0.1%	8	+0.1%	kHz
Synchronous signal duty ratio	dSYNC 1	CDL = 20 pF (during output) BCLK = 2.048 MHz At output	45	50	55	%
Transmit/receive synchronous timing	tBS	BCLK to SYNC (during output)	100	—	—	ns
	tSB	SYNC to BCLK (during output)	100	—	—	ns
Input setup time	tDS	PCMI pin	50	—	—	ns
Input hold time	tDH		50	—	—	ns
Digital output delay time	tSDX	PCMO pin Pull-up resistance RDL = 500Ω CDL = 50 pF	—	—	100	ns
	tXD1		—	—	100	ns
Digital output hold time	tXD2		—	—	100	ns
	tXD3		—	—	100	ns

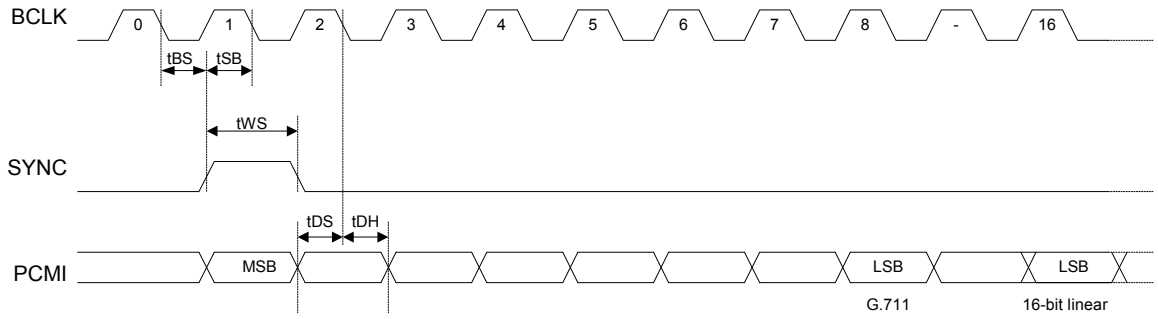


Figure 2 PCM Interface Input Timing (Long Frame)

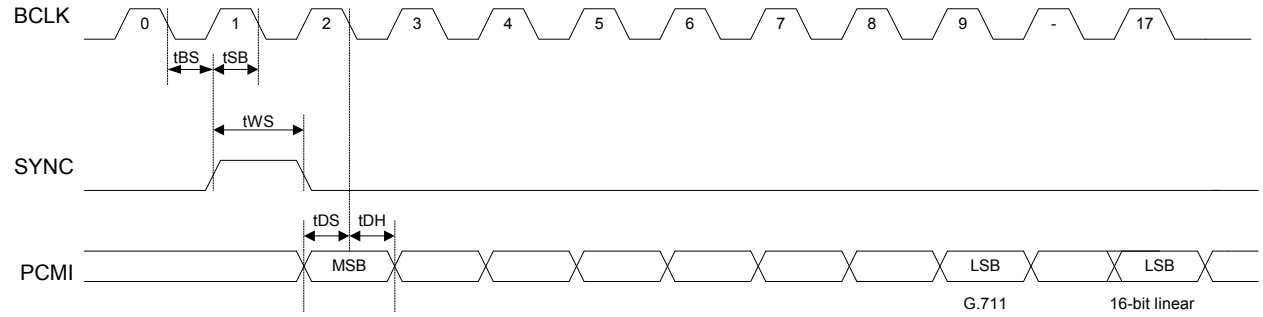


Figure 3 PCM Interface Input Timing (Short Frame)

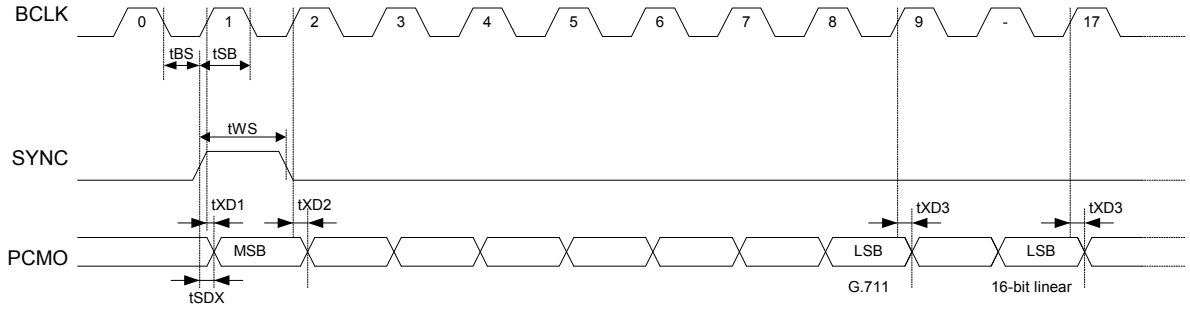


Figure 4 PCM Interface Output Timing (Long Frame)

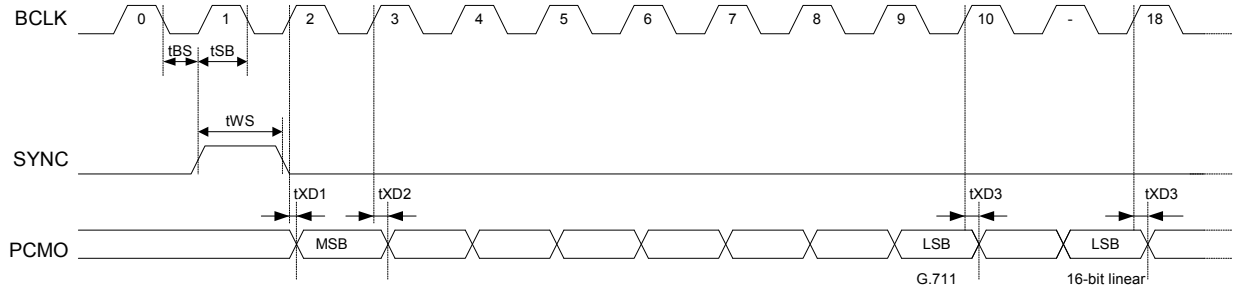


Figure 5 PCM Interface Output Timing (Short Frame)

Control Register Interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta= –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address setup time (at Read)	tRAS	CL = 50 pF	10	—	—	ns
Address hold time (at Read))	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (at Read)	tRCS		10	—	—	ns
CSB hold time (at Read)	tRCH		0	—	—	ns
CSB setup time (at Write)	tWCS		10	—	—	ns
CSB hold time (at Write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
Read data output delay time	tRDD		—	—	20	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		25	—	—	ns
CSB disable time	tCD		10	—	—	ns

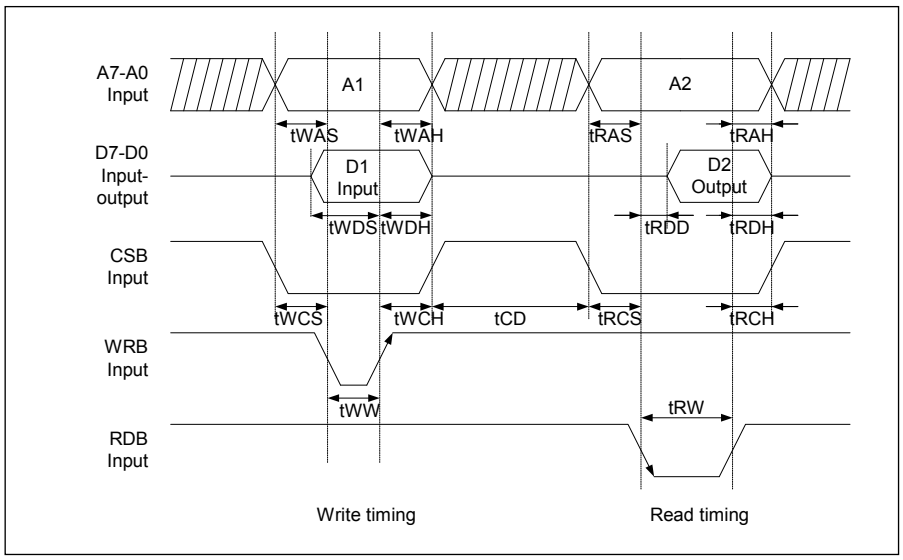


Figure 6 Control Register Interface

Transmit/Receive Buffer Interface (Frame Mode)

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FR1B setup time	tF1S	CL = 50 pF	3	—	—	ns
FR1B output delay time	tF1D		—	—	20	ns
Address setup time (at Read)	tRAS		10	—	—	ns
Address hold time (at Read))	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (at Read)	tRCS		10	—	—	ns
CSB hold time (at Read)	tRCH		0	—	—	ns
CSB setup time (at Write)	tWCS		10	—	—	ns
CSB hold time (at Write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
FR0B setup time	tF0S		3	—	—	ns
FR0B output delay time	tF0D		—	—	20	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
CSB disable time	tCD		10	—	—	ns

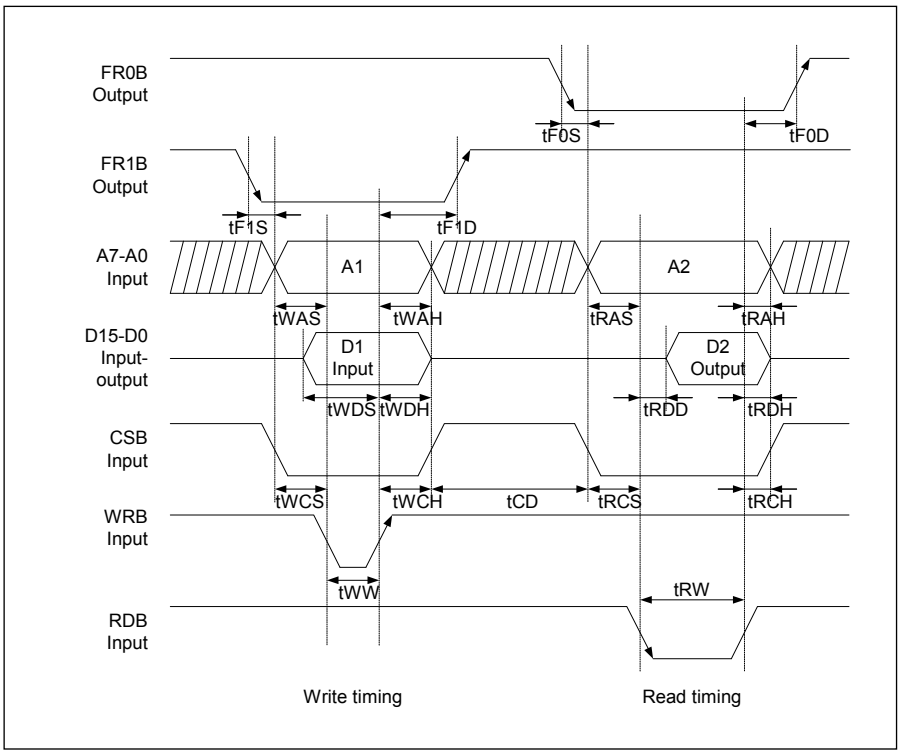


Figure 7 Transmit/Receive Buffer Interface (Frame Mode)

Transmit/Receive Buffer Interface (DMA Mode)

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DMARQ1B setup time	tDR1S	CL = 50 pF	3	—	—	ns
DMARQ1B output delay time	tDR1RD		—	—	30	ns
	tDR1FD		—	—	30	ns
Address setup time (at Read)	tRAS		10	—	—	ns
Address hold time (at Read))	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
ACK0B setup time	tAK0S		10	—	—	ns
ACK0B hold time	tAK0H		0	—	—	ns
ACK1B setup time	tAK1S		10	—	—	ns
ACK1B hold time	tAK1H		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
DMARQ0B setup time	tDR0S		3	—	—	ns
DMARQ0B output delay time	tDR0RD		—	—	30	ns
	tDR0FD		—	—	30	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
ACKB disable time	tAD		10	—	—	ns

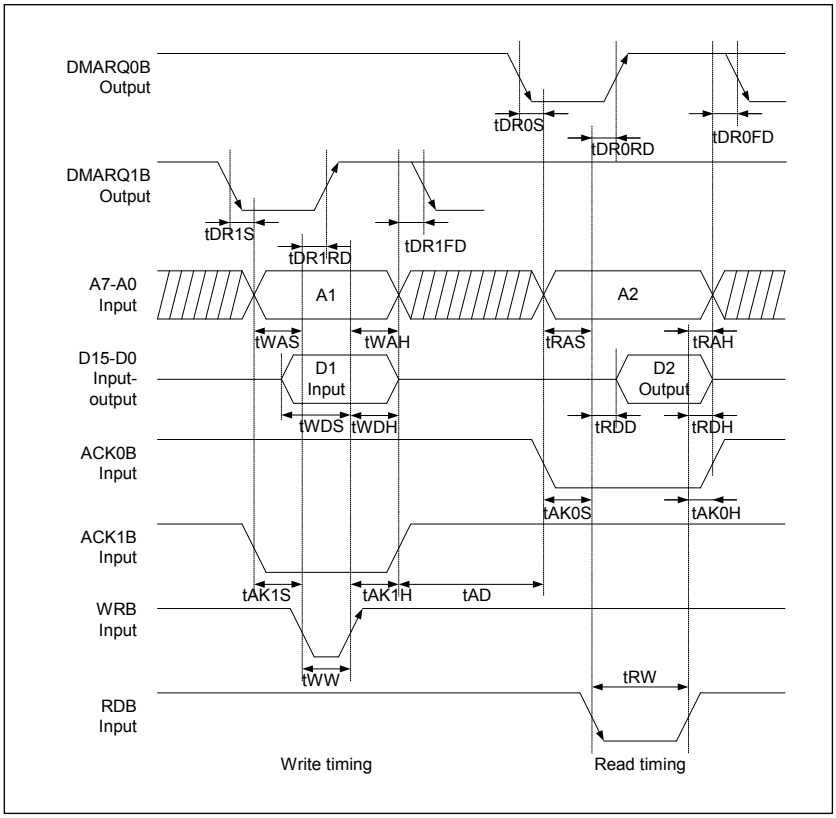


Figure 8 Transmit/Receive Buffer Interface (DMA Mode)

PIN FUNCTIONAL DESCRIPTION

AIN0N, AIN0P, GSX0, AIN1N, and GSX1

These are transmit analog input and transmit gain adjustment pins. AIN0N and AIN1N are connected to inverted input pins of internal transmission amplifiers AMP0 and AMP1, and AIN0P is connected to a noninverting input pin of AMP0. GSX0 and GSX1 are connected to output pins of AMP0 and AMP1. See Figure 9 for the gain adjustment.

At power down (PDNB = "0" or SPDN = "1"), outputs of GSX0 and GSX1 are in a high impedance state. When the application does not use AMP0, short-circuit GSX0 and AIN0N and connect AIN0P with AVREF. When not using AMP1, short-circuit GSX1 and AIN1N.

VFRO0 and VFRO1

These are receive analog output pins. VFRO0 and VFRO1 are connected to output pins of amplifiers AMP2 and AMP3. Output signals, VFRO0 and VFRO1, can be selected using the VFRO0 selection register (VFRO0_SEL) and VFRO1 selection register (VFRO1_SEL): When output is selected ("1"), the receive signal is output and when output is not selected ("0"), AVREF (about 1.4 V) is output. In power down mode, these output pins are set to a high impedance state. It is recommended to use output signals through a DC coupling capacitor.

(Note)

If output selection is changed while the conversation is in progress, a micronoise is generated. Therefore, it is recommended to select output before starting a call and then start a call.

Before canceling reset or resetting, it is recommended to select output of VFRO0 and VFRO1 to the AVREF output side.

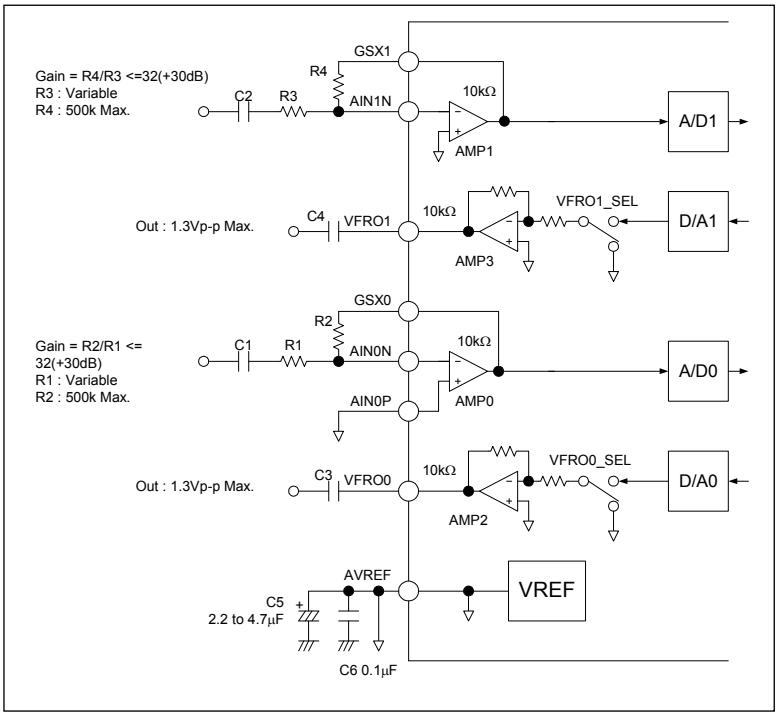
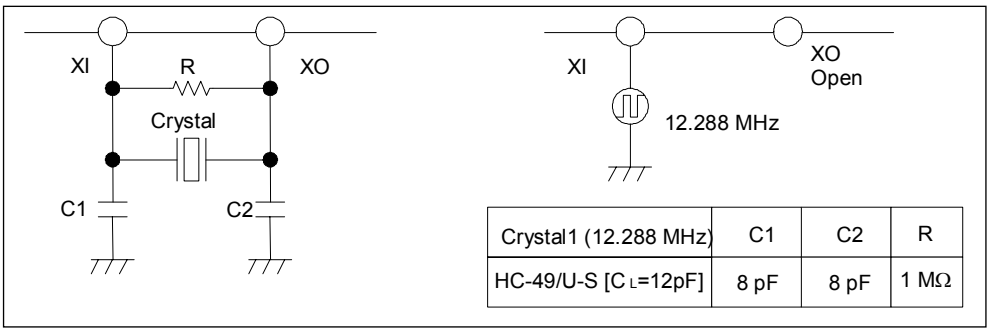


Figure 9 Analog Interface

AVREF
This is an output pin of an analog signal ground potential. With the output potential of about 1.4 V, insert bypass capacitors of 2.2 to 4.7 μF (aluminum electrolysis type) and 0.1 μF (ceramic type) in parallel. AVREF outputs 0.0 V at power down. AVREF starts being powered up after power-down reset, the system restarts from (PDNB = "1" and SPDN = "0").

XI and XO
These are the master clock input pin and the crystal connection pins for the master clock.
Oscillation stops at power down by PDNB or software power down by SPDN. Oscillation starts after power-down is reset and the clock is supplied to the LSI internal section after oscillation stabilization delay time has elapsed (about 21.3 ms). Figure 10 shows a master clock input and a crystal connection example.



Crystal1 (12.288 MHz)	C1	C2	R
HC-49/U-S [C_L=12pF]	8 pF	8 pF	1 MΩ

Figure 10 Example of an Oscillation Circuit and Clock Input

(Note)
For an oscillation circuit, connect a 12,288 MHz crystal and a 1 MΩ feedback resistor (R) between XI and XO. Since the values of capacitors C1 and C2 that are connected between XI and GND and between XO and GND are affected by the production load capacitance of a crystal and the wiring capacitance of the board, contact the manufacturer of the crystal to ask for matching evaluation to detemine the capacitor values.

PDNB
This is a power-down control input pin. A power-down state can be set by setting this pin to "0". This pin also functions as an LSI reset pin. To prevent an LSI operation error, use PDNB for the initial power-down reset after power is applied. To put the LSI into a power-down state, fix PDNB to "0" for 250 μs or more.
LSI power-down reset can be performed by setting the software power down reset control register SPDN to "0" → "1" → "0".
After 200ms from power-down release, the initial mode display register (READY) is set to "1" and various function setting modes (initial modes) are entered.
See Figure 1 for the timings of PDNB, AVREF, XO, and the initial mode.

(Note)
Turn on the power in a power-down state by PDNB.
When using the LSI by inputting a master clock to the XI pin, first maintain the power-down state (PDNB = 0) until power is applied to the digital power supply (DVDD0, 1, and 2) and the analog power supply (AVDD) (90% or more) and the master clock is input to the XI pin, then release the power-down state (PDNB = 0 → 1) . In this case also, fix PDNB to "0" for 250 μs or more.

DVDD0, DVDD1, DVDD2, and AVDD
These are power supply pins. DVDD0, DVDD1, and DVDD2 are connected to the power supply of a digital circuit and AVDD is connected to a power supply of an analog circuit. Connect these pins near the LSI and insert bypass capacitors of 10 μF (electrolysis type) and 0.1 μF (ceramic type) between DGND and AGND in parallel.

DGND0, DGND1, DGND2, and AGND
These are ground pins. DGND0, DGND1, and DGND2 are connected to grounds of digital circuits and AGND is connected to a ground of an analog circuit. Connect these pins near the LSI.

VREGOUT
This is an output pin of an internal regulator voltage (about 2.5 V).
Connect a capacitor of about 0.1 μF (ceramic type) in parallel to about 10 μF (ceramic or tantalum type) between this pin and a ground pin.

VBG
This is a reference output pin for an internal regulator.
Connect a laminated ceramic capacitor of about 150 pF between this pin and a ground pin.

TST0 and TST1
These are input pins for testing. At normal use, input "0".

INTB/GPIOA[6]

Primary function: INTB

This in an interrupt request output pin.

When the interrupt cause is changed, this pin outputs a "L" level for about 1.0 μs. When the interrupt factor is not changed, "H" is output. The interrupt factor can be checked by reading CR16-CR22. Table 1 lists the interrupt causes.

The interrupt causes can be masked individually in the internal memory (interrupt cause mask control).

Table 1 Interrupt Causes

CR	BIT	Register name	Rising edge	Falling edge	Remarks
CR16	B2	FSK receive overrun error notification register (FDET_OER)	○	×	
	B1	FSK receive framing error notification register (FDET_FER)	○	×	
	B0	FSK receive data read request notification register (FDET_RQ)	○	×	
CR17	B0	FSK output data setting completion flag (FGEN_FLAG)	×	○	
CR18	B0	Timer overflow display register (TMOVF)	○	×	
CR19	B7	DSP status register (DSP_ERR)	○	×	
	B4	TONE1 detector detection status register (TONE1_DET)	○	○	
	B3	TONE0 detector detection status register (TONE0_DET)	○	○	
	B2	TGEN1 execution flag display register (TGEN1_EXFLAG)	○	○	
	B1	TGEN0 execution flag display register (TGEN0_EXFLAG)	○	○	
CR20	B6	Dial pulse detector detection status register (DP_DET)	○	○	
	B4	DTMF detector detection status register (DTMF_DET)	○	○	
	B3-B0	DTMF code display register (DTMF_CODE[3:0])	○	○	
CR21	B3	CH2 transmit error status register (TXERR_CH2)	○	○	
	B2	CH1 transmit error status register (TXERR_CH1)	○	○	
	B1	CH2 transmit request notification register (FR0_CH2)	○	×	
	B0	CH1 transmit request notification register (FR0_CH1)	○	×	
CR22	B3	CH2 receive error status register (RXERR_CH2)	○	○	
	B2	CH1 receive error status register (RXERR_CH1)	○	○	
	B1	Receive invalid write error notification register (RXBW_ERR)	○	○	
	B0	Receive request notification register (FR1)	○	×	

○: With INTB interrupt generation function ×: Without INTB interrupt generation function

Secondary function: GPIOA[6]

When the primary function/secondary function selection register (GPFA[6]) of GPIOA[6] is set to "1", this pin functions as a general-purpose I/O port GPIOA[6].

A0-A7
These are address input pins for accessing a frame/DMA/control register. Each address is as follows.

Transmit buffer (TX Buffer)
A7-A0 = 80h
Receive buffer (RX Buffer)
A7-A0 = 81h
Control register (CR)
See Tables 5 to 9 for the addresses.

D0-D15
These are data I/O pins for accessing a frame/DMA/control register. Since these pins are I/O pins, connect pull-up resistors. When an 8-bit bus access is selected in the MCU interface data width selection register (BW_SEL), pins D0-D7 are enabled. When using the pins with 8-bit bus access (BW_SEL = "1"), fix the input of high-order D8-D15 to either "0" or "1" since they are constantly in an input state.

CSB
This is a chip select input pin for accessing a frame/control register.

RDB
This is a read enable input pin for accessing a frame/DMA/control register.

WRB
This is a write enable input pin for accessing a frame/DMA/control register.

FR0B (DMARQ0B)

- FR0B (FRAME/DMA selection register FD_SEL = "0" in frame mode)
  This is a transmit frame output pin that outputs data when the transmit buffer for frame access becomes full. When the transmit buffer becomes full, the pin outputs "L" and retains "L" until the specified number of words are read from the MCU.

- DMARQ0B (FRAME/DMA selection register FD_SEL = "1" in DMA mode)
  This is a DMA request output pin that outputs data when the transmit buffer for DMA access becomes full. When the transmit buffer becomes full, the pin outputs "L" and the value is reset to "H" automatically when an acknowledgment signal (ACK0B = "0") and the fall of a read enable signal (RDB = "1" → "0") are received from the MCU side. This operation is repeated until the specified number of words are read from the MCU.

FR1B (DMARQ1B)

- FR1B (FRAME/DMA selection register FD_SEL = "0" in frame mode)
  This receive frame output pin outputs data when the receive buffer for frame access becomes empty. When the receive buffer becomes empty, the pin outputs "L" and retains "L" until the specified number of words are written from the MCU.

- DMARQ1B (FRAME/DMA selection register FD_SEL = "1" in DMA mode)
  This a DMA request output pin that outputs data when the receive buffer for DMA access becomes empty. When the receive buffer becomes empty, the pin outputs "L" and the value is reset to "H" automatically when an acknowledgment signal (ACK1B = "0") and the fall of a write enable signal (WRB = "1" → "0") are received from the MCU side. This opeation is repeated until the specified number of words are written from the MCU side.

ACK0B/GPIOA[4]

Primary function: ACK0B
This is a DMA acknowledgment input pin for DMARQ0B for transmit buffer DMA access; it is enabled in DMA mode (FD_SEL = "1").
When using the pin in frame mode (FD_SEL = "0"), fix this pin to "1".
Secondary function: GPIOA[4]
When the primary function/secondary function selection register (GPFA[4]) of GPIOA[4] is set to "1", the pin functions as a general-purpose I/O port GPIOA[4].

ACK1B/GPIOA[5]

Primary function: ACK0B
This is a DMA acknowledgment input pin for DMARQ1B for receive buffer DMA access; it is enabled in DMA mode (FD_SEL = "1").
When using this pin in frame mode (FD_SEL = "0"), fix this pin to "1".
Secondary function: GPIOA[5]
When the primary function/secondary function selection register (GPFA[5]) of GPIOA[5] is set to "1", the pin functions as a general-purpose I/O port GPIOA[5].

GPIOA[0], GPIOA[1], GPIOA[2], and GPIOA[3]

These are general-purpose I/O ports A[3:0].
However, the following secondary functions are assigned to GPIOA[0] and GPIOA[2].
Secondary function of GPIOA[0]: Input pin (DPI) of a dial pulse detecter (DPDET)
Secondary function of GPIOA[2]: Output pin (DPO) of a dial pulse transmitter (DPGEN)

CLKSEL
This is an input-output control input pin of SYNC and BCLK. The pin controls input when it is set to "0" and output when it is set to "1".
(Note)
This LSI operates at either SYNC/BCLK that is generated inside the LSI or the clock generated based on SYNC/BCLK to be input from the outside the LSI. For this reason, if the CLKSEL pin is set to "0", it is necessary to constantly input SYNC/BCLK from the time the power supply is truned on regardless of whether PCM-IF is used or not.

SYNC
This is a 8 kHz synchronous signal I/O pin of PCM signals. When CLKSEL is "0", constantly input an 8 kHz clock synchronized with BCLK. When CLKSEL is "1", this pin outputs an 8 kHz clock synchronized with BCLK. When the SYNC frame control register (SYNC_SEL) is "0", long frame synchronization is specified and when the register is "1", short frame synchronization is specified.

BCLK
This is a shift clock I/O pin of a PCM signal.
When CLKSEL is "0", clock input synchronized with SYNC is necessary. When G.711 is selected, input a clock of 64 kHz to 2.048 MHz and when 16-bit linear is selected, input a clock of 128 kHz to 2.048 MHz. When CLKSEL is "1", this pin outputs a clock of 2.048 MHz synchronized with SYNC.

(Remarks) Table 2 shows the input-output control of SYNC and BCLK and the frequencies.

Table 2 SYNC and BCLK Input-Output Control

CLKSEL	SYNC	BCLK	Remarks
"0"	Input (8 kHz)	Input (64 kHz to 2048 kHz)	Always input a clock after start of power supply. When G.711 is selected, input a clock of 64 kHz to 2.048 MHz. When 16-bit linear is selected, input a clock of 128 kHz to 2.048 MHz.
"1"	Output (8 kHz)	Output (2.048 MHz)	At power down, "L" is output.

PCMO
This is a PCM signal output pin. A PCM signal is output synchronized with the rise of BCLK or SYNC.
For the output from PCMO, data is output to only the applicable time slot section according to the selected coding format and the setting of the time slot position and other sections are set to a high-impedance state. If a PCM interface is not used, PCMO is set to a high impedance state.

(Note)
Be sure to connect a pull-up resistor externally to the PCMO pin, because the pin is an open drain output pin.
Do not use a pull-up voltage greater than the digital power supply voltage (DVDD).

PCMI
This is a PCM signal input pin. The signal is shifted at falling of BCLK and is input from MSB.
If a PCM interface is not used, fix the input to "0" or "1".

FUNCTIONAL DESCRIPTION

Transmit and receive buffers

Table 3 lists the controllable parameters of the transmit and receive buffers.
This LSI allows the setting of the Speech CODEC coding format and the buffering time for transmit and receive buffers individually.
[Example] Transmit side (Tx): G.729.A/10 ms, Receive side (Rx): G.711/20 ms

Table 3 Controllable Parameters of Transmit and Receive Buffers

Contents		Modifiable parameter	Initial value	Remarks
Speech CODEC Coding format	Tx side	G.729.A G.711 (μ-law, A-law)	G.729.A	The buffering size of the transmit buffer is changed automatically according to the Speech CODEC coding format of the transmit side.
	Rx side	G.729.A G.711 (μ-law, A-law)	G.729.A	The buffering size of the receive buffer is changed automatically according to the Speech CODEC coding format of the receive side.
Buffering time	Tx side	10 ms 20 ms	10 ms	The number of words of the transmit buffer is changed automatically according to the setting of buffering time on the transmit side.
	Rx side	10 ms 20 ms	10 ms	The number of words of the receive buffer is changed automatically according to the setting of buffering time on the receive side.
Access mode		Frame DMA	Frame	
FIFO data width		16 bits 8 bits	16 bits	The number of words is changed automatically according to the data width.

Transmit and receive buffer size

Each of the transmit and receive buffers comprises double buffers in FIFO (First In First Out) format, and buffering is performed for data of 10 ms or 20 ms for one buffer.
When the transmit buffer is full or the receive buffer is empty, a requesting frame signal (FR0B or FR1B) or a DMA request signal (DMARQ0B or DMARQ1B) is issued to the MCU. The number of FIFO words is changed automatically according to the selected Speech CODEC and FIFO data width. Table 4 shows the buffer size and the number of words determined by each of Speech CODEC and data width.

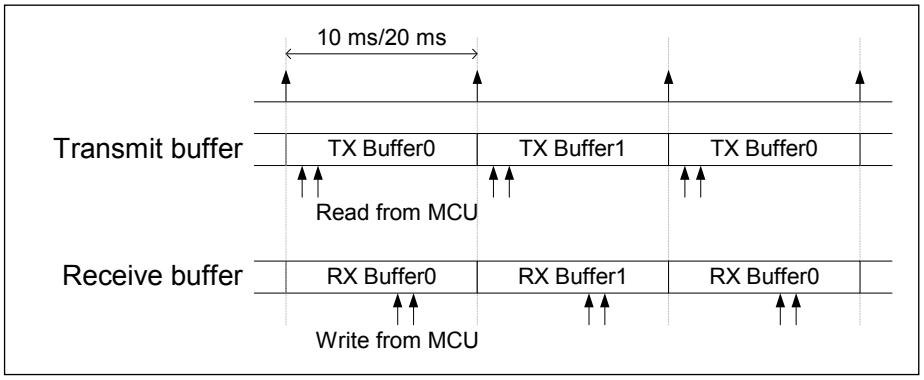
Table 4 Buffer Sizes and the Numbers of Words of Transmit and Receive Buffers

Speech CODEC	10 ms mode			20 ms mode		
	Buffer size	16 bits	8 bits	Buffer size	16 bits	8 bits
G.729.A (8 kbps)	10 bytes	5 words	10 words	20 bytes	10 words	20 words
G.711 (64 kbps)	80 bytes	40 words	80 words	160 bytes	80 words	160 words

Structure of transmit/receive buffers

Figure 11 shows the transmit/receive access timing. Both the transmit and receive buffers are in a double-buffer structure; however, either of them can be accessed as one buffer when accessed from the MCU side.

(1) Single-channel operation (SC_EN = 1, DC_EN = 0)



(2) 2-channel operation (SC_EN=1, DC_EN=1)

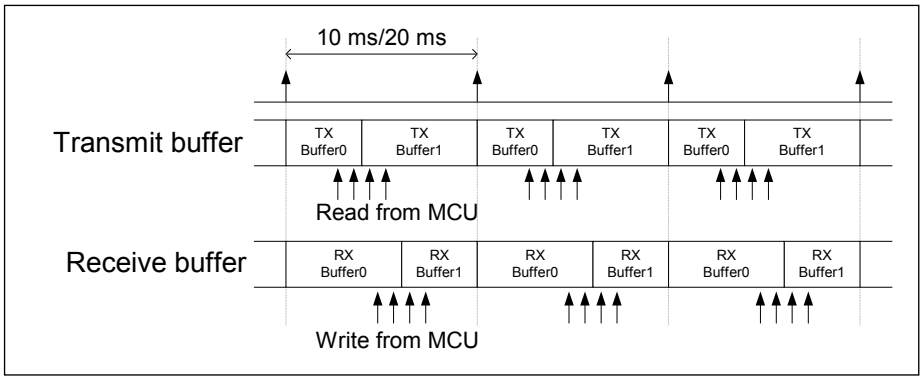


Figure 11 Transmit/Receive Buffer Access Timing

Data width selection (16-bit mode, 8-bit mode)

16-bit mode or 8-bit mode can be selected in the MCU interface data width selection register (BW_SEL) as the transmit/receive buffer access data width.

In 16-bit mode, data is accessed through a 16-bit data width of D15-D0 and in 8-bit mode, transmit and receive data is input-output in D7-D0. In 8-bit access mode, D15-D8 always go into an input state.

Data storage format
Figures 12 and 13 show the storage formats at transmit/receive processing in each parameter.

A. G.729.A

G.729.A(8 kbps)
· 1 frame 80 bits/10 ms
· 2 frames 160 bits/20 ms

G.729.A code and word structure

Symbol name
bit No

Number of words	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	L0	L1 6	L1 5	L1 4	L1 3	L1 2	L1 1	L1 0	L2 4	L2 3	L2 2	L2 1	L2 0	L3 4	L3 3	L3 2
2	L3 1	L3 0	P1 7	P1 6	P1 5	P1 4	P1 3	P1 2	P1 1	P1 0	P0	C1 12	C1 11	C1 10	C1 9	C1 8
3	C1 7	C1 6	C1 5	C1 4	C1 3	C1 2	C1 1	C1 0	S1 3	S1 2	S1 1	S1 0	GA1 2	GA1 1	GA1 0	GB1 3
4	GB1 2	GB1 1	GB1 0	P2 4	P2 3	P2 2	P2 1	P2 0	C2 12	C2 11	C2 10	C2 9	C2 8	C2 7	C2 6	C2 5
5	C2 4	C2 3	C2 2	C2 1	C2 0	S2 3	S2 2	S2 1	S2 0	GA2 2	GA2 1	GA2 0	GB2 3	GB2 2	GB2 1	GB2 0

Word structure

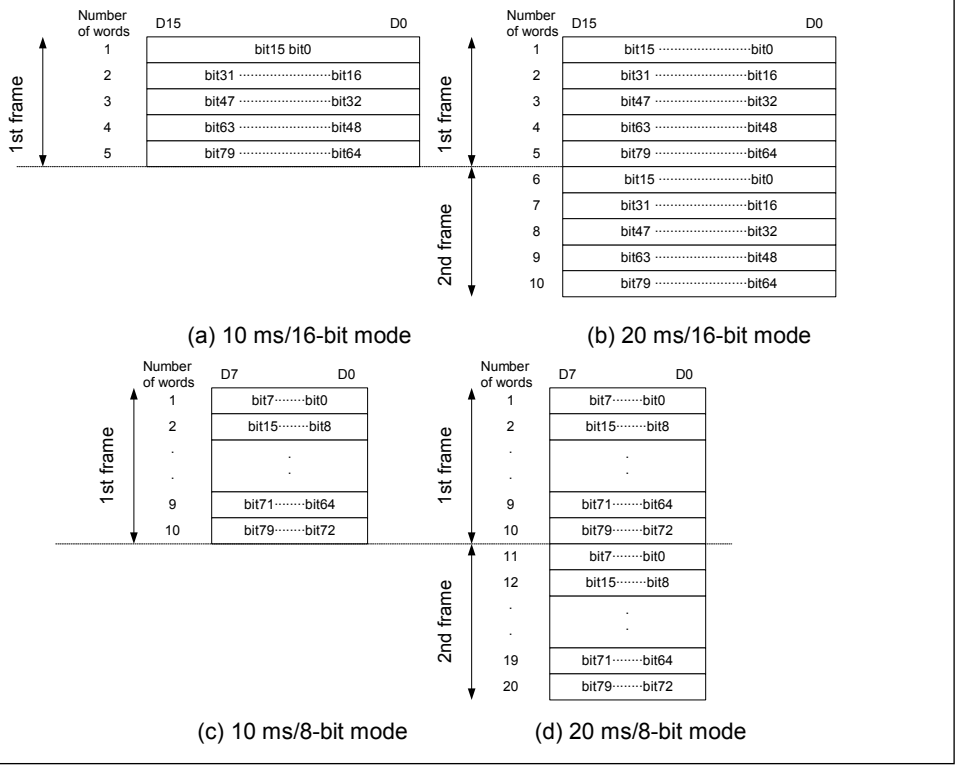


Figure 12 G.729.A Data Format

B. G.711 (64 kbps)

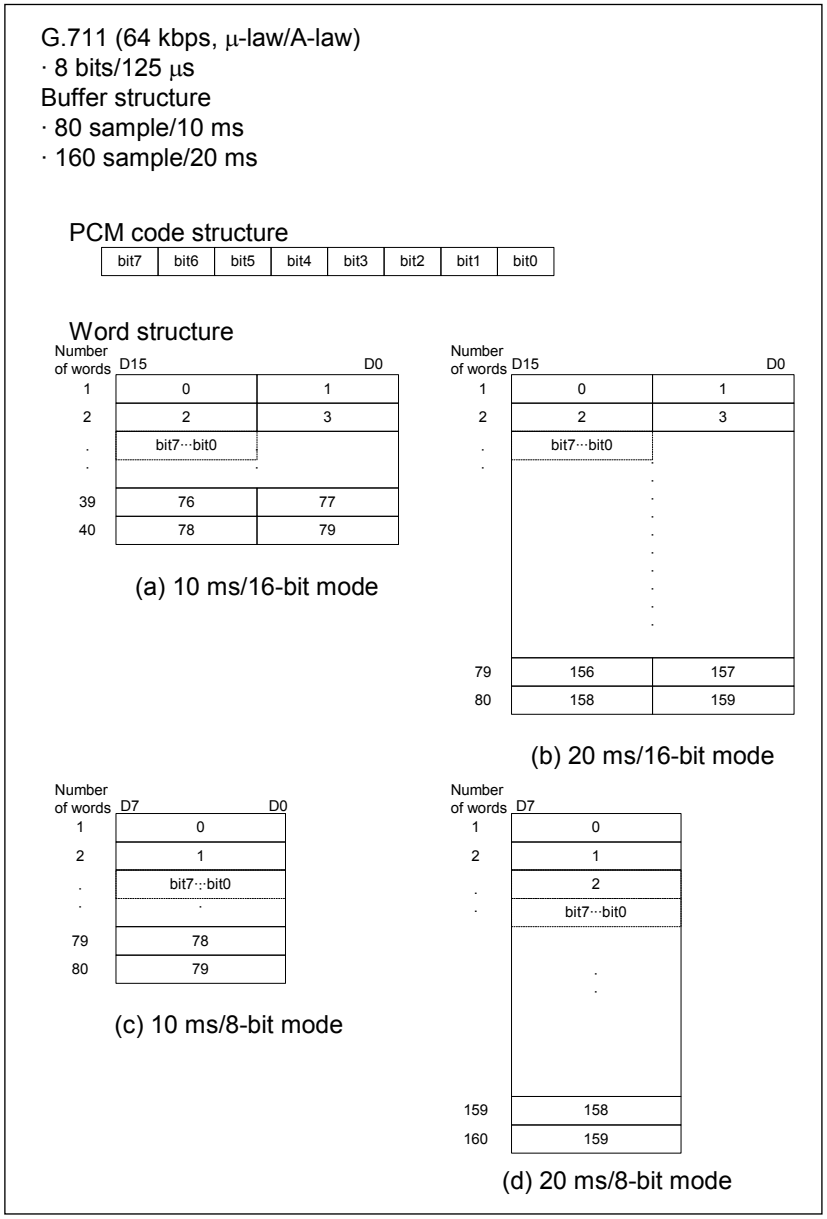


Figure 13 G.711 Data Format

Transmit buffer control methods at single-channel operation
Figures 14 to 17 show the transmit buffer control methods at single-channel operation.

A. G.729.A (10 ms /frame mode)

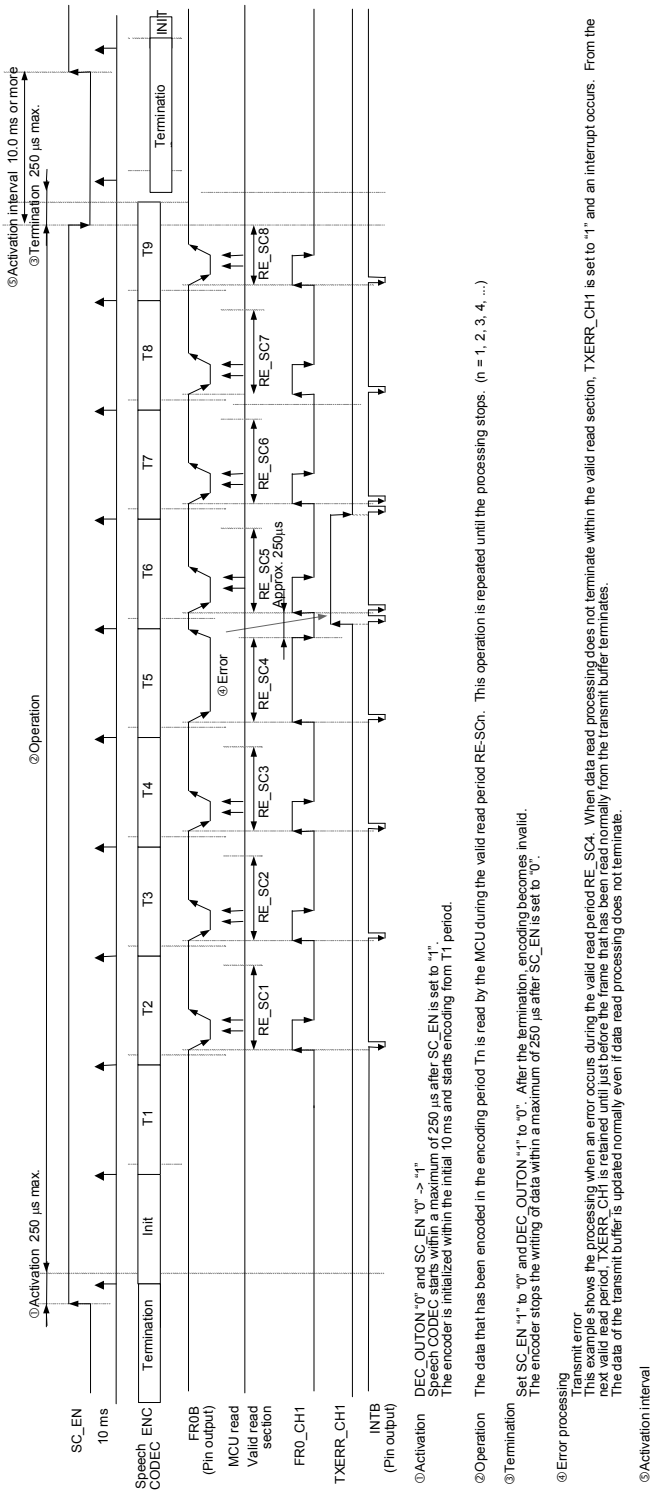


Figure 14 G.729.A Transmit Buffer Control Method at Single-Channel Operation (10 ms/frame mode)

B. G.729.A (20 ms/frame mode)

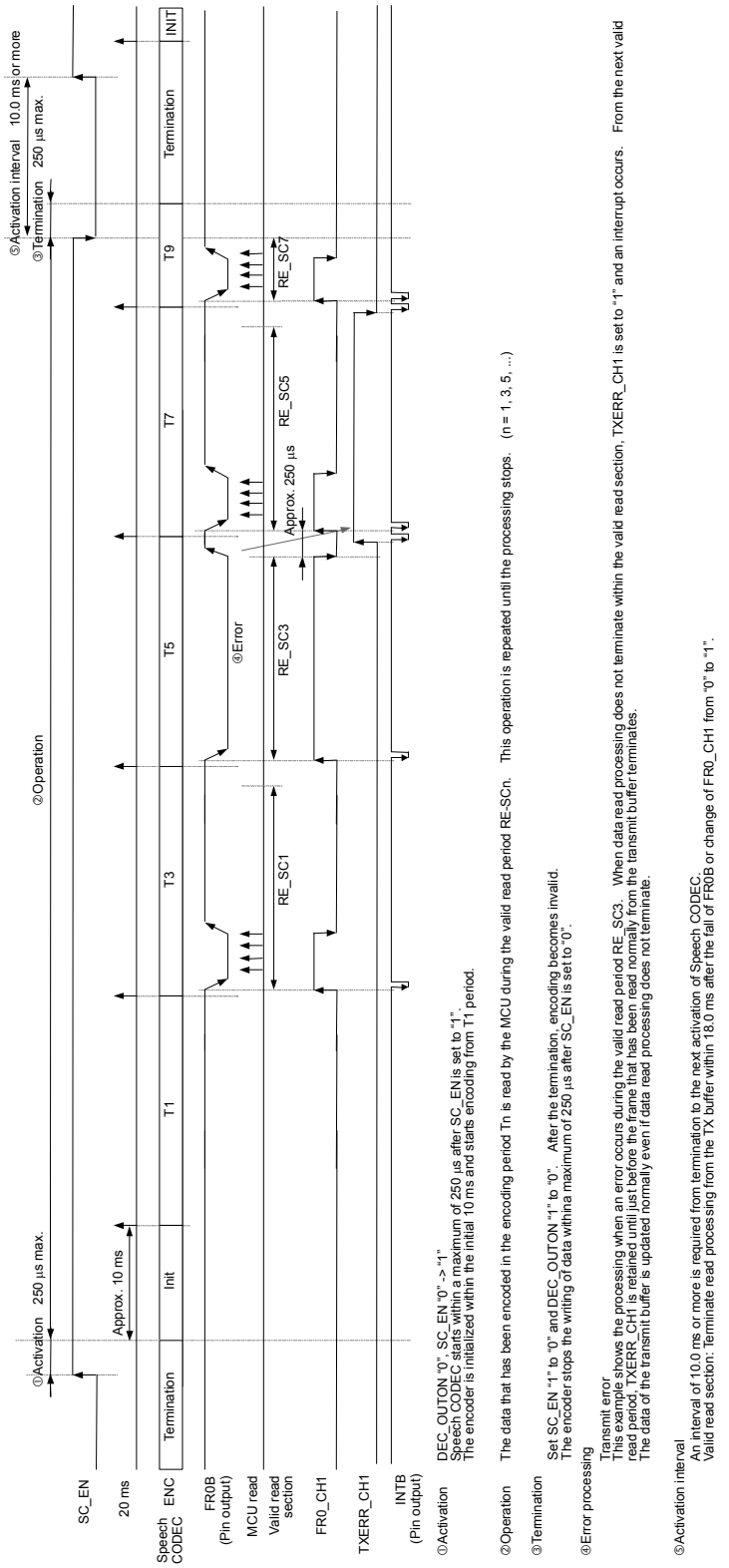


Figure 15 G.729.A Transmit Buffer Control Method at Single-Channel Operation (20 ms/frame mode)

C. G.711 (μ-law and A-law) (10 ms/frame mode)

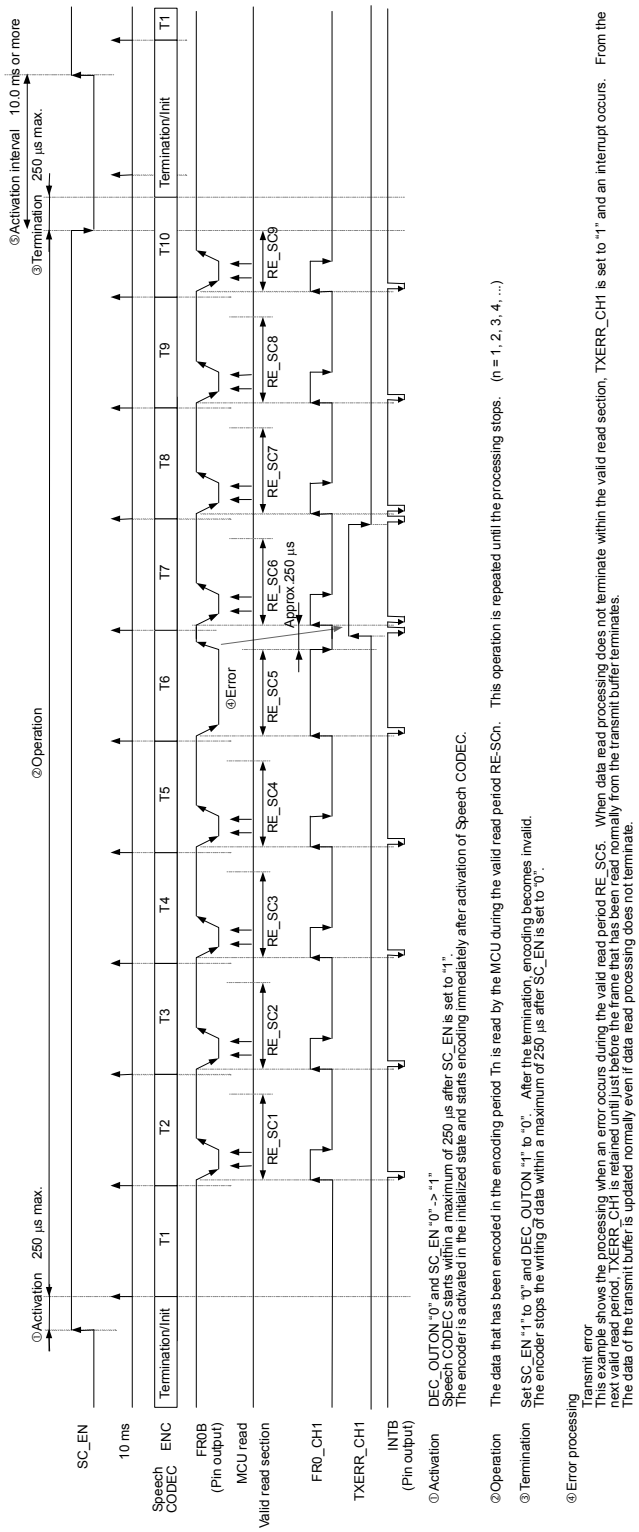


Figure 16 G.711 (μ-law and A-law) Transmit Buffer Control Method at Single-Channel Operation (10 ms/frame mode)

D. G.711 (μ-law and A-law) (20 ms/frame mode)

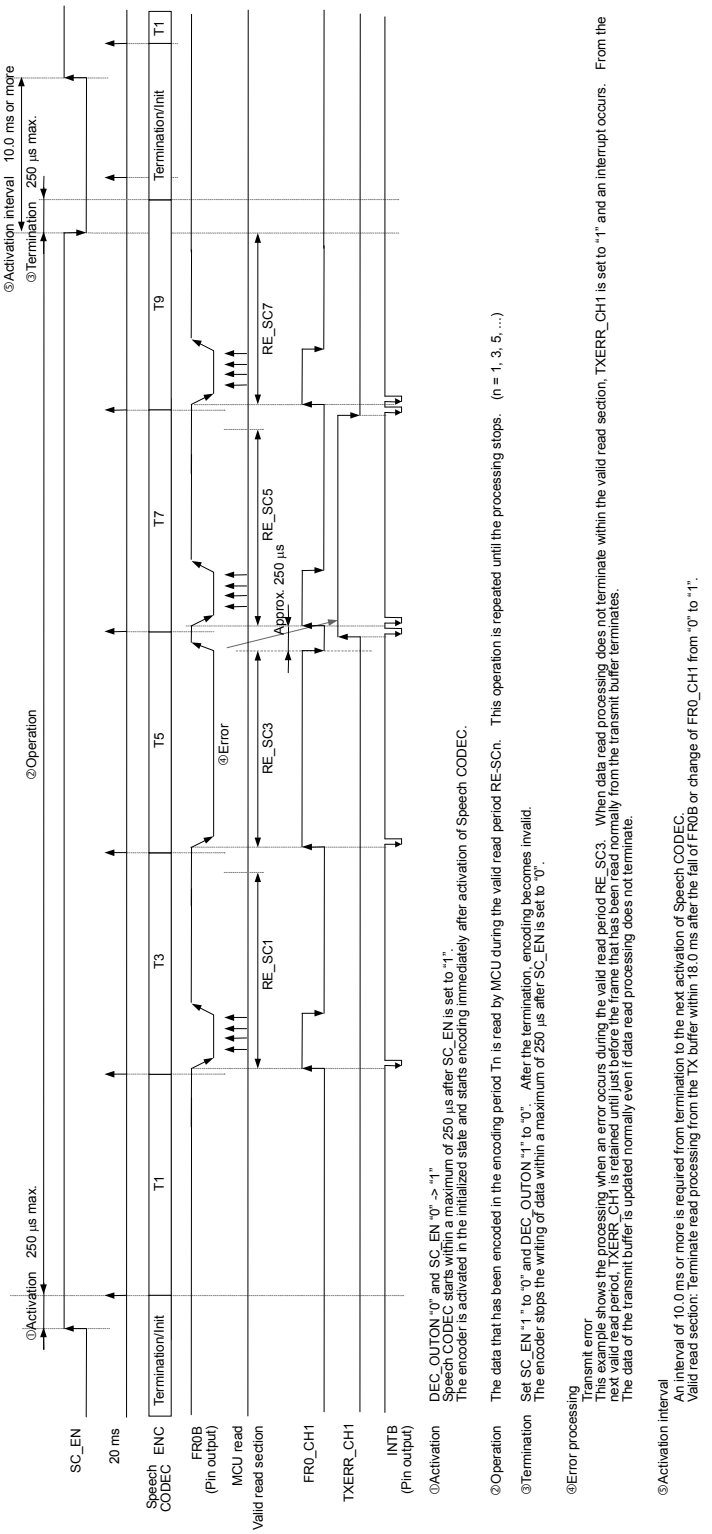


Figure 17 G.711 (μ-law and A-law) Transmit Buffer Control Method at Single-Channel Operation (20 ms/frame mode)

Receive buffer control method at single-channel operation

Figures 18 to 21 show the receive buffer control methods at single-channel operation.

A. G.729.A (10 ms/frame mode)

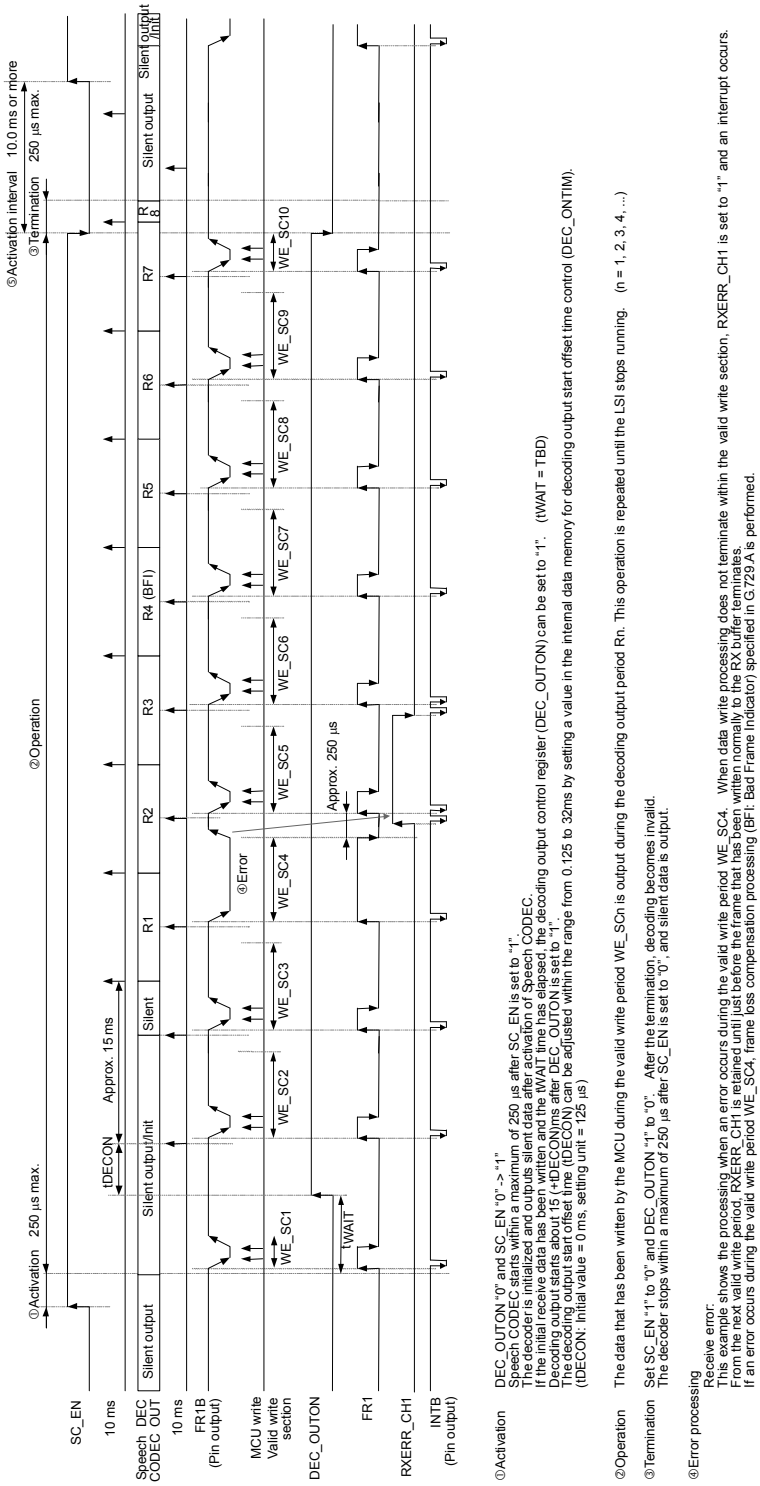


Figure 18 G.729.A Receive Buffer Control Method at Single-Channel Operation (10 ms/frame mode)

B. G.729.A (20m/frame mode)

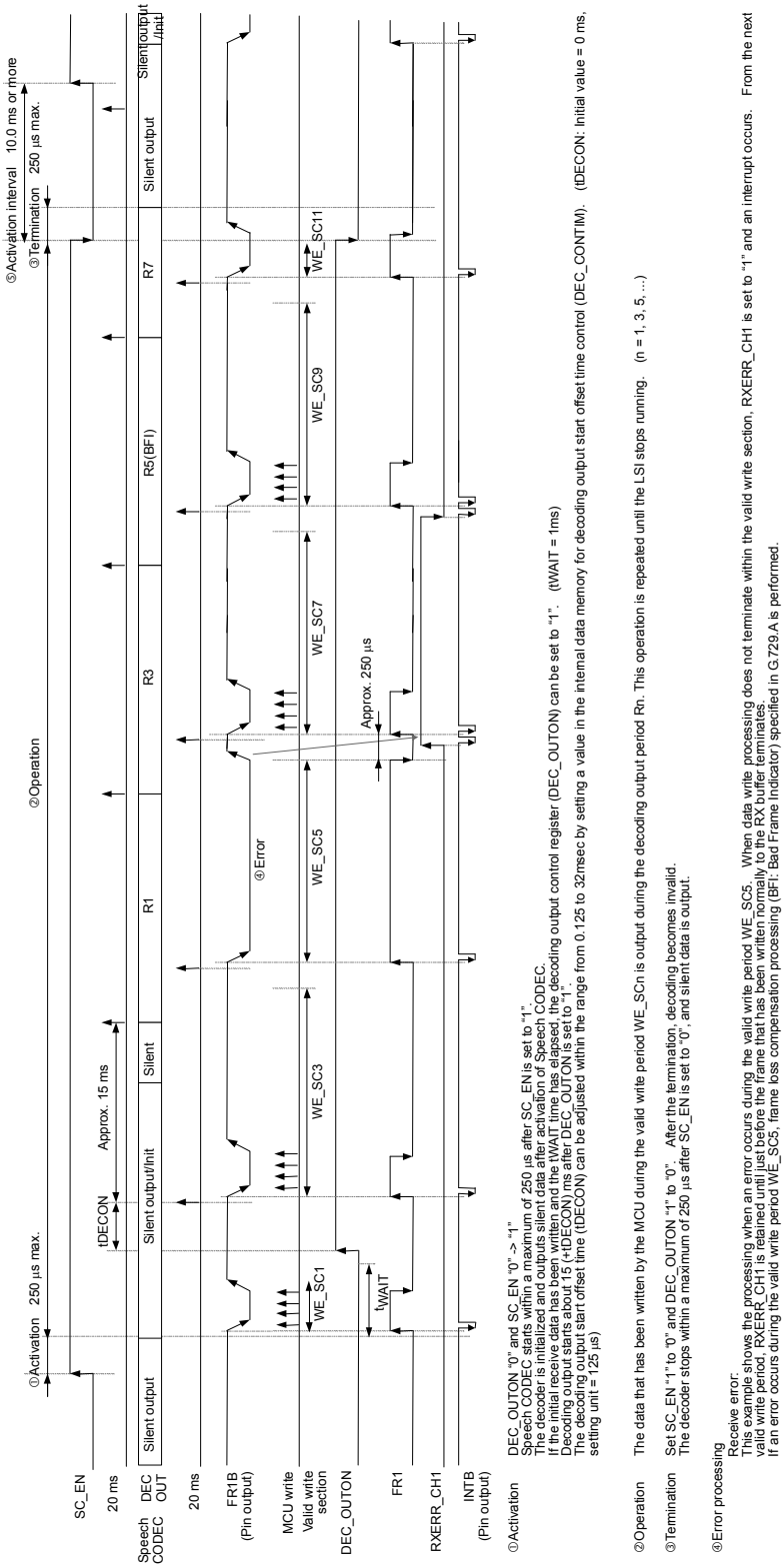


Figure 19 G.729.A Receive Buffer Control Method at Single-Channel Operation (20 ms/frame mode)

C. G.711 (μ-law, A-law) (10 ms/frame mode)

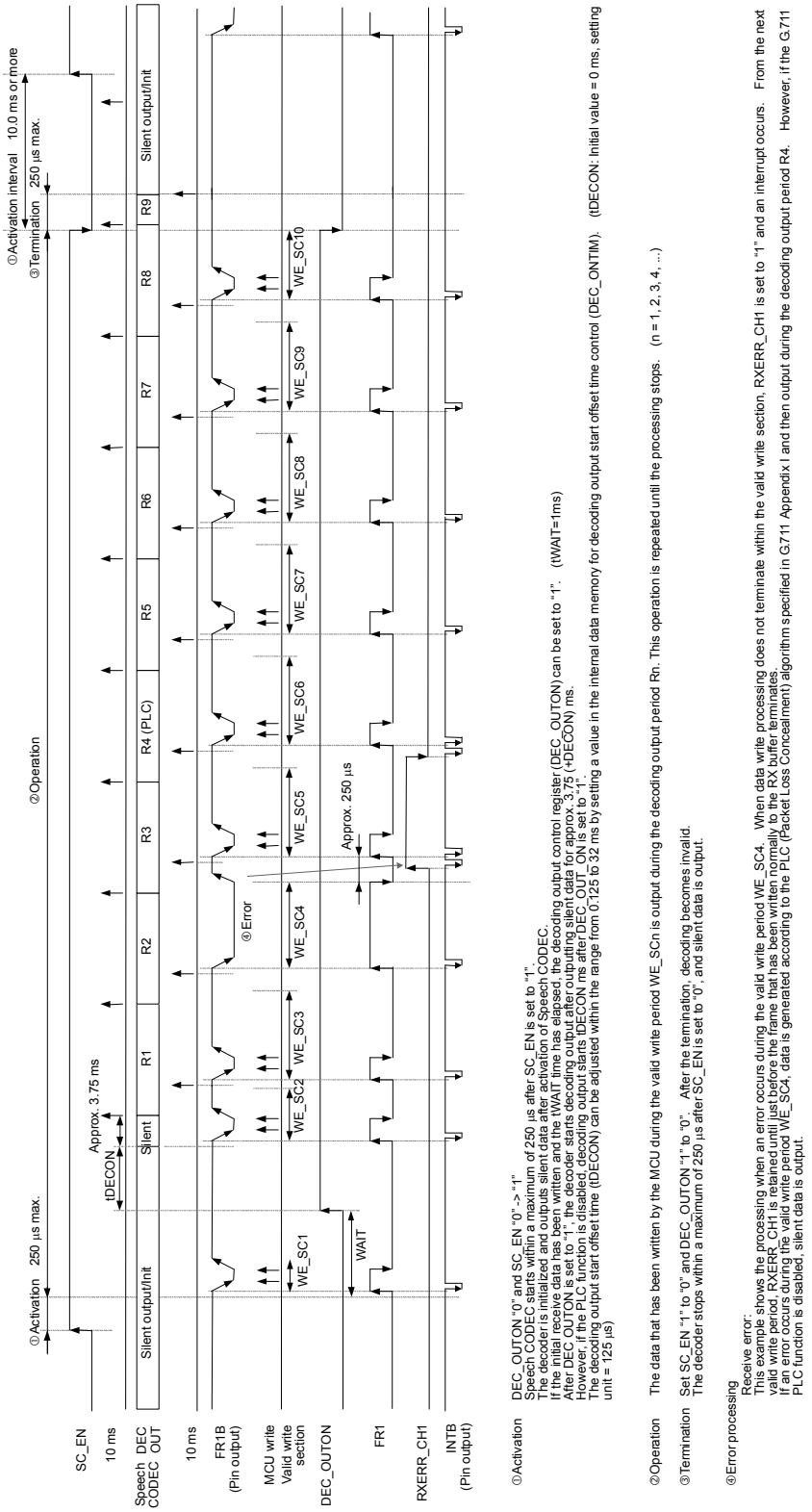


Figure 20 G.711 (μ-law and A-law) Receive Buffer Control Method at Single-Channel Operation (10 ms/frame mode)

D. G.711(μ-law, A-law) (20 ms/frame mode)

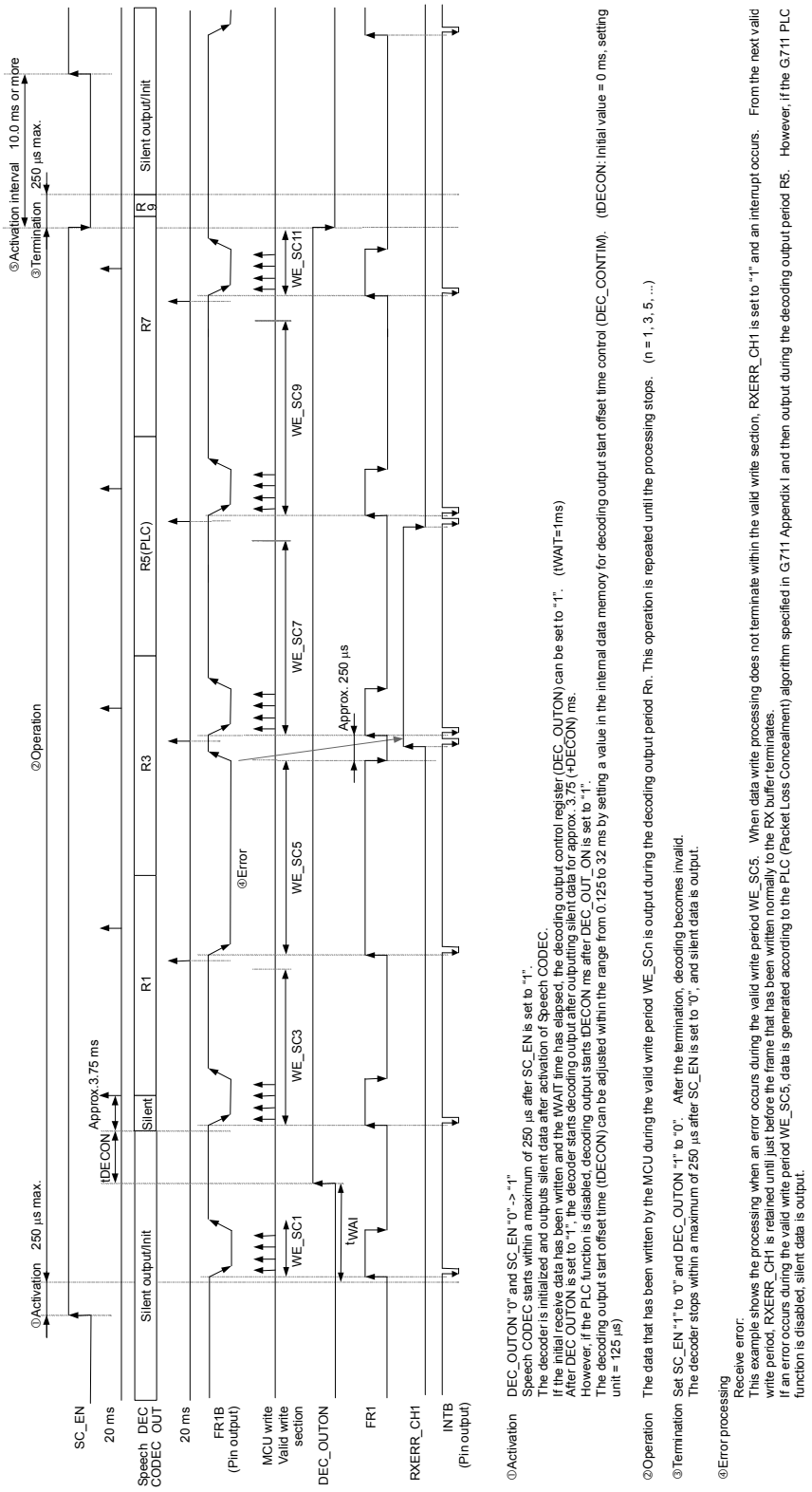


Figure 21 G.711 (μ-law and A-law) Receive Buffer Control Method at Single-Channel Operation (20 ms/frame mode)

Speech CODEC coding format switching control

This LSI allows the switching of Speech CODEC coding format on the transmit and receive sides independently during single-channel operation (SC_EN = 1 and DC_EN = 0). However, only the following patterns are supported for the Speech CODEC coding format switching and any other switching patterns are inhibited.

A) Speech CODEC coding format switching control on the transmit side

A-1) G.729.A → G.711(μ-law/A-law) [Buffering time: Fixed to 10 ms]
A-2) G.729.A → G.711(μ-law/A-law) [Buffering time: Fixed to 20 ms]
A-3) G.711(μ-law/A-law) → G.729.A [Buffering time: Fixed to 10 ms]
A-4) G.711(μ-law/A-law) → G.729.A [Buffering time: Fixed to 20 ms]

B) Speech CODEC coding format switching control on the receive side

B-1) G.729.A → G.711(μ-law/A-law) [Buffering time: Fixed to 10 ms]
B-2) G.729.A → G.711(μ -law/A-law) [Buffering time: Fixed to 20 ms]
B-3) G.711(μ-law/A-law) → G.729.A [Buffering time: Fixed to 10 ms]
B-4) G.711(μ-law/A-law) → G.729.A [Buffering time: Fixed to 20 ms]

Figures 22 to 29 show the detail control methods for the switching control indicated above.

(Note)
1. Changing a buffering time (10 ms/20 ms) during activation of Speech CODEC (SC_EN = 1) is inhibited.
2. Switching from G.711 (A-law) to G.711 (μ-law) or from G.711 (μ-law) to G.711 (A-law) is inhibited.
3. Wait 100 ms or more before switching the Speech CODEC coding format again after the format is switched.

A. Speech CODEC coding format switching control on the transmit side

A-1. G.729.A → G.711 (μ-law and A-law) switching control (10 ms frame mode)

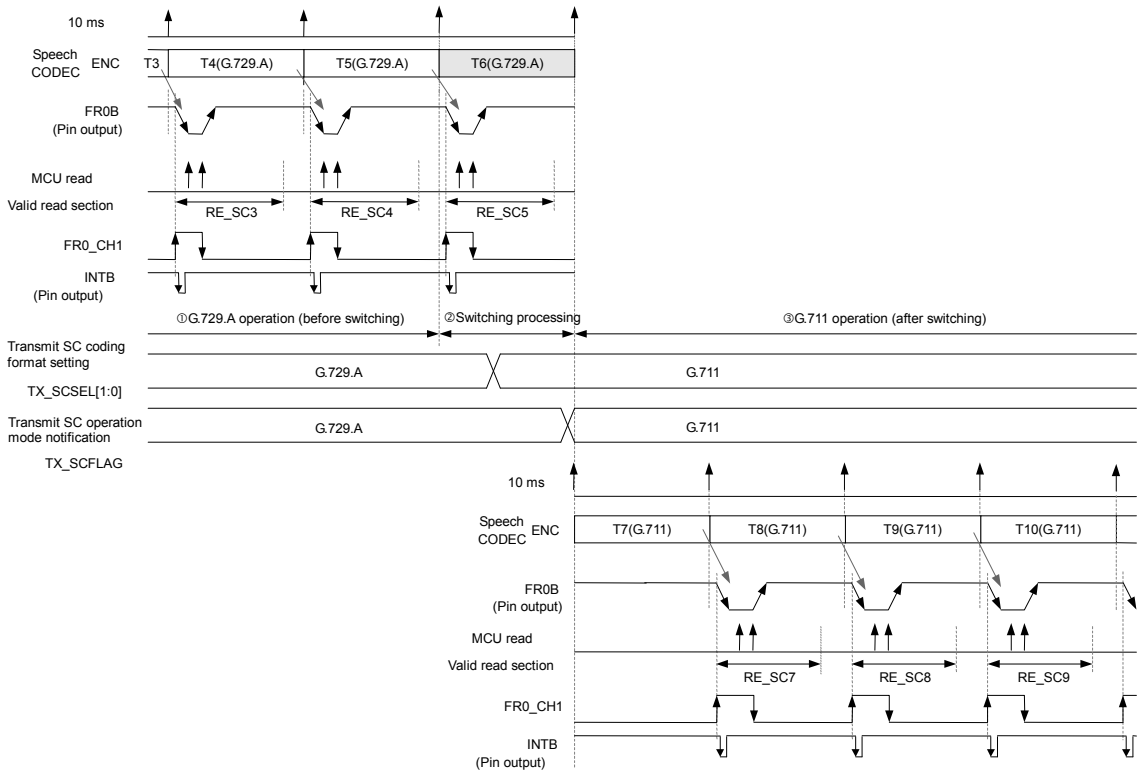


Figure 22 Speech CODEC Format Switching Control Method on the Transmit Side G.729.A→G.711 <10 ms frame mode>

① G.729.A operation (before switching)

Operates according to the contents described in ② Operation and ④ Error processing in Figure 14 G.729.A transmit buffer control method at single-channel operation (10 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G729.A to G.711 within the valid MCU read period according to the setting in the Speech CODEC selection register on the transmit side (TX_SCSEL[1:0]). When the switching of the Speech CODEC coding format is detected, the LSI internal section discards the data currently being encoded (T6 encoding data in the example shown above) and starts encoding in the G.711 coding format from the next frame.

A read request is issued normally by FR0B also for the frame where coding format has been switched; however, a transmit error (TXERR_CH1 = "1") does not occur even if data read processing does not terminate within the valid read period. If a transmit error occurred before this frame, this transmit error is cleared to "0" at termination of this frame.

(Note)

If the coding format is switched outside of the valid MCU read period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check whether the transmit request is for the data encoded in the G.729.A or encoded in the G.711 by referencing the transmit Speech CODEC operation mode notification flag (TX_SCFLAG) when requesting transmission due to the fall of FR0B.

③ G.711 operation (after switching)

Operates according to the contents that are described in ② Operation and ④ Error processing in Figure 16 G.711 (μ-law and A-law) transmit buffer control method (10 ms/frame mode) at single-channel operation.

A-2. G.729.A → G.711 (μ-law and A-law) switching control (20 ms frame mode)

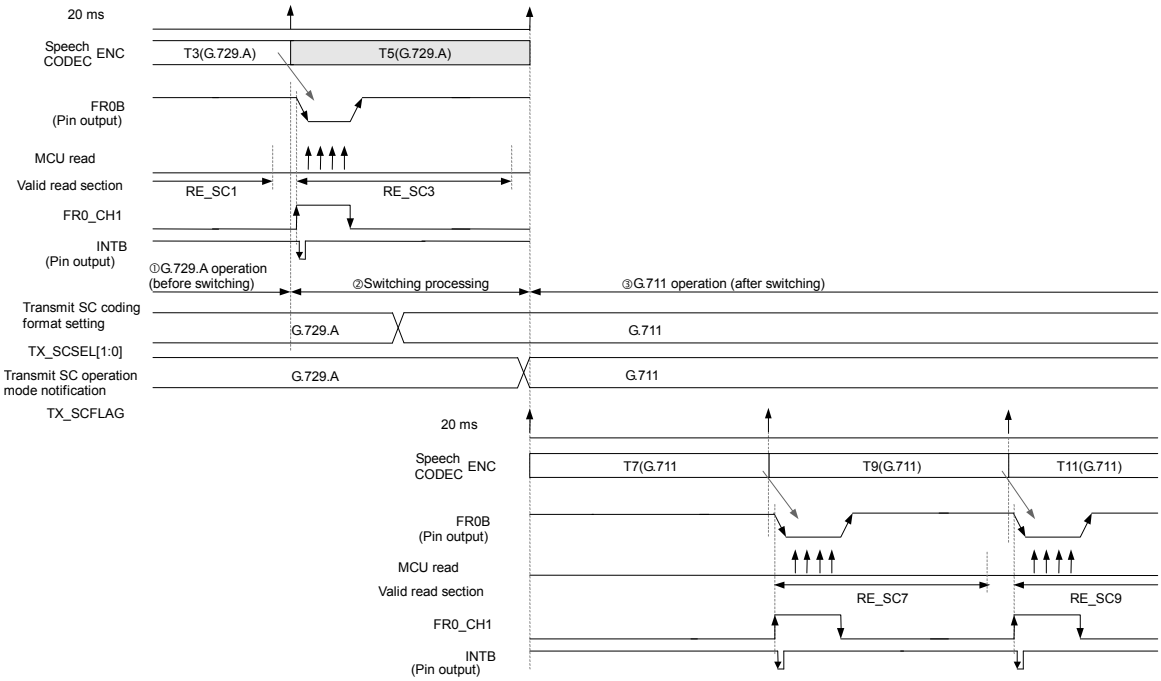


Figure 23 Speech CODEC Coding Format Switching Method on the Transmit Side G.729.A→G.711 <20 ms frame mode>

① G.729.A operation (before switching)

Operates according to the contents described in ②Operation and ④Error processing in Figure 15. G.729.A transmit buffer control method at single-channel operation (20 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G729.A to G.711 within the valid MCU read period according to the setting in the Speech CODEC selection register on the transmit side (TX_SCSEL[1:0]). When the switching of the Speech CODEC coding format is detected, the LSI internal section discards the data currently being encoded (T5 encoding data in the example shown above) and starts encoding in the G.711 coding format from the next frame.

A read request is issued normally by FR0B also for the frame where coding format has been switched; however, a transmit error (TXERR_CH1 = "1") does not occur even if data read processing does not terminate within the valid read period. If a transmit error occurred before this frame, that transmit error is cleared to "0" at termination of this frame.

(Note)

If the coding format is switched outside of the valid MCU read period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check whether the transmit request is for the data encoded in the G.729.A or encoded in the G.711 by referencing the transmit Speech CODEC operation mode notification flag (TX_SCFLAG) when requesting transmission due to the fall of FR0B.

③ G.711 operation (after switching)

Operates according to the contents that are described in ②Operation and ④Error processing in Figure 17 G.711 (μ-law and A-law) transmit buffer control method at single-channel operation (20 ms/frame mode).

A-3. G.711 (μ-law, A-law) → G.729.A switching control (10 ms frame mode)

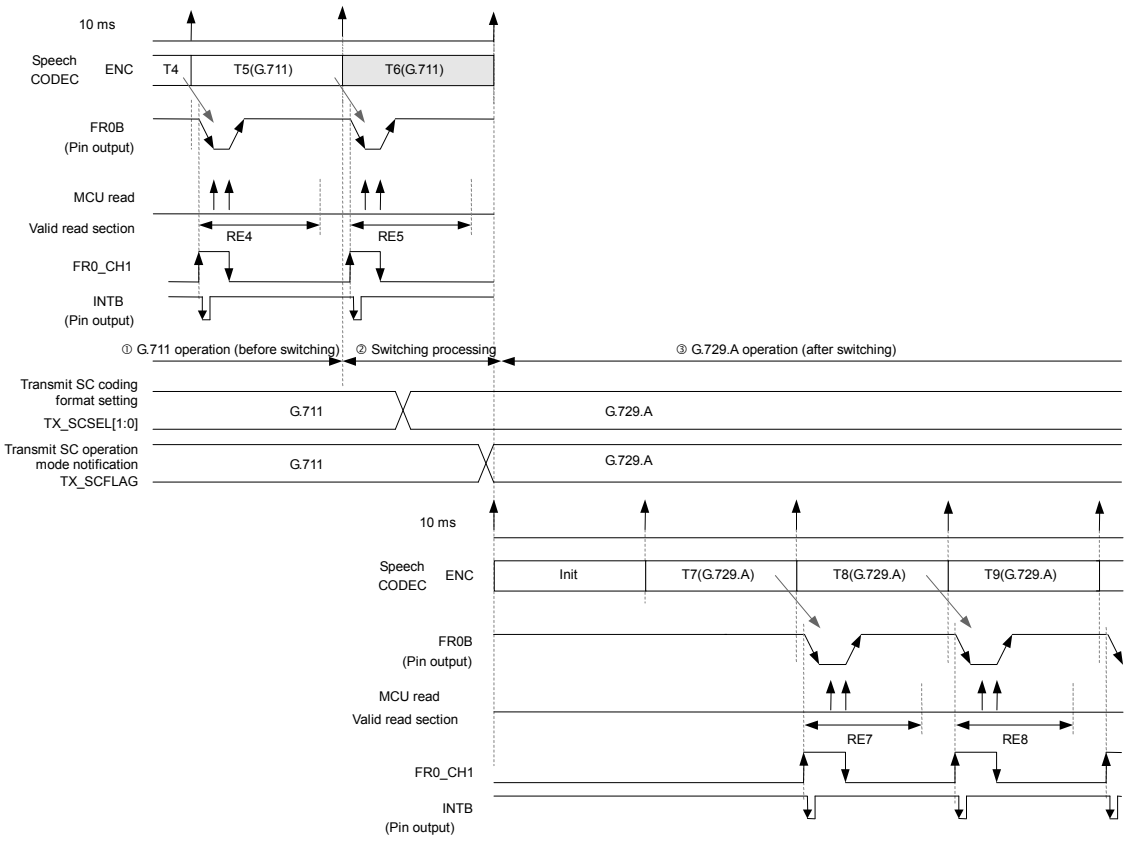


Figure 24 Speech CODEC Coding Format Switching Control Method on the Transmit Side G.711→G.729.A <10 ms frame mode>

① G.711 operation (before switching)

Operates according to the contents described in ② Operation and ④ Error processing in Figure 16 G.711 (μ-law and A-law) transmit buffer control method at single-channel operation (10 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G711 to G.729.A within the valid MCU read period according to the setting in the Speech CODEC selection register on the transmit side (TX_SCSEL[1:0]). When the switching of the Speech CODEC coding format is detected, the LSI internal section discards the data currently being encoded (T6 encoding data in the example shown above) and starts encoding in the G.729.A coding format from the next frame.

A read request is issued normally by FR0B also for the frame where coding format has been switched; however, a transmit error (TXERR_CH1 = "1") does not occur even if data read processing does not terminate within the valid read period. If a transmit error occurred before this frame, that transmit error is cleared to "0" at termination of this frame.

(Note)

If the coding format is switched outside of the valid MCU read period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check if the transmit request is for the data encoded in the G.729.A or encoded in the G.711 coding format by referencing the transmit Speech CODEC operation mode notification flag (TX_SCFLAG) when requesting transmission due to the fall of FR0B.

③ G.729.A operation (after switching)

Operates according to the contents that are described in ②Operation and ④Error processing in Figure 14 G.729.A transmit buffer control method at single-channel operation (10 ms frame mode).

A-4. G.711 (μ-law and A-law) → G.729.A switching control (20 ms frame mode)

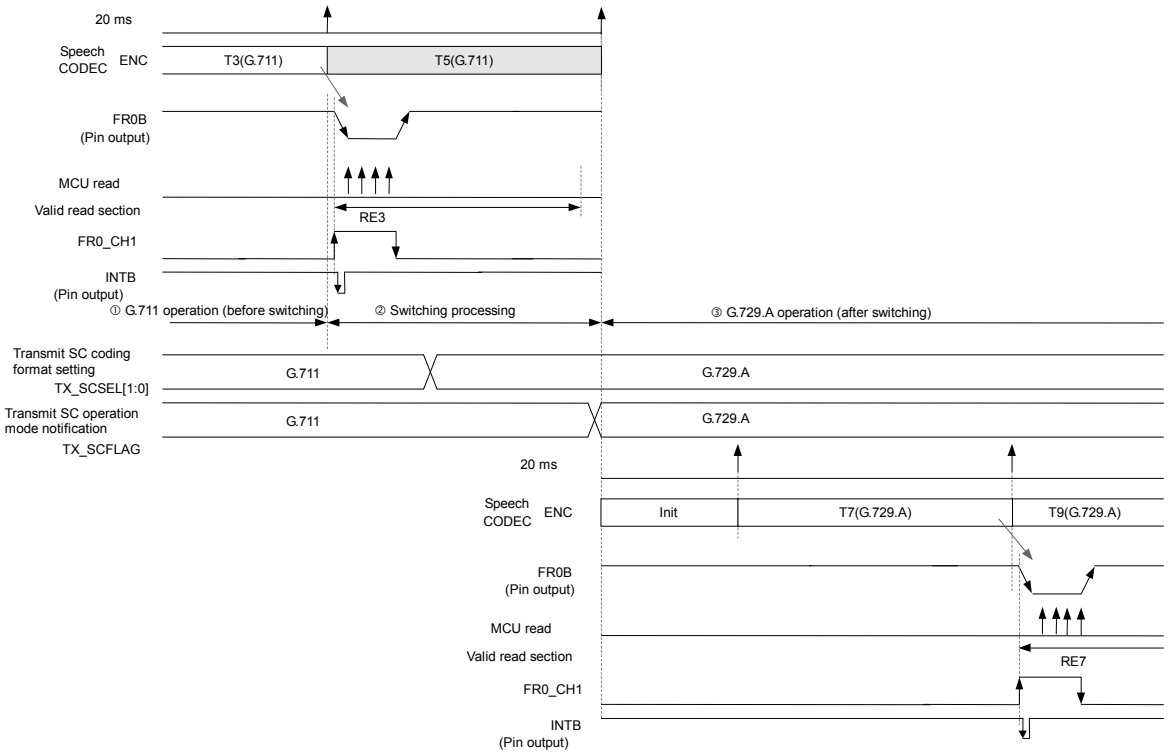


Figure 25 Speech CODEC Coding Format Switching Control Method on the Transmit Side G.711→G.729.A <20 ms frame mode>

① G.711 operation (before switching)

Operates according to the contents described in ②Operation and ④Error processing in Figure 17 G.711 (μ-law and A-law) transmit buffer control method at single-channel operation (20 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G711 to G.729.A within the valid MCU read period according to the setting in the Speech CODEC selection register on the transmit side (TX_SCSEL[1:0]). When detecting the switching of the Speech CODEC coding format, the LSI internal section discards the data currently being encoded (T5 encoding data in the example shown above) and starts encoding in the G.729.A coding format from the next frame.

A read request is issued normally by FR0B also for the frame where coding format has been switched; however, a transmit error (TXERR_CH1 = "1") does not occur even if data read processing does not terminate within the valid read period. If a transmit error occurred before this frame, that transmit error is cleared to "0" at termination of this frame.

(Note)

If the coding format is switched outside of the valid MCU read period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check whether the transmit request is for the data encoded in the G.729.A or encoded in the G.711 by referencing the transmit Speech CODEC operation mode notification flag (TX_SCFLAG) when requesting transmission due to the fall of FR0B.

③ G.729.A operation (after switching)

Operates according to the contents that are described in ②Operation and ④Error processing in Figure 15 G.729.A transmit buffer control method at single-channel operation (20 ms frame mode).

B. Speech CODEC coding format switching control on the receive side

B-1. G.729.A → G.711(μ-law and A-law) switching control (10 ms frame mode)

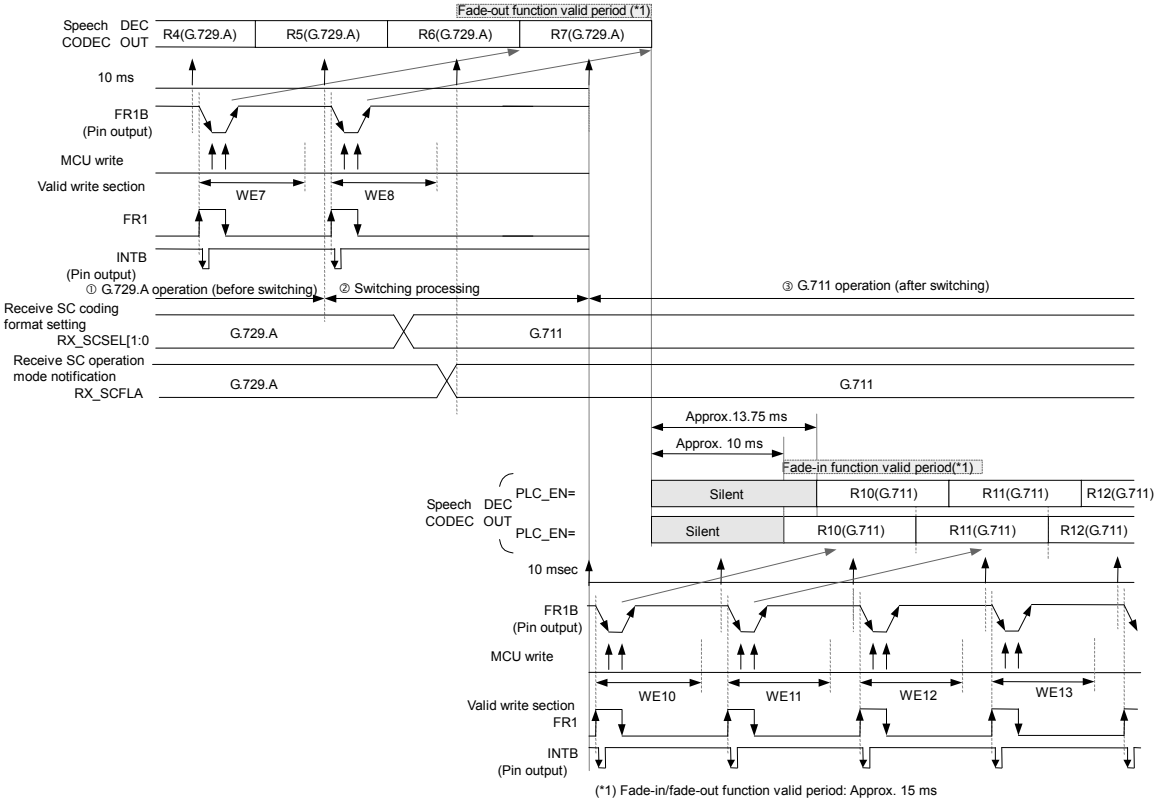


Figure 26 Speech CODEC Coding Format Switching Control Method on the Receive Side G.729.A→G.711 <10 ms frame mode>

① G.729.A operation (before switching)

Operates according to the contents described in ② Operation and ④ Error processing in Figure 18 G.729.A receive buffer method at single-channel operation (10 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G729.A to G.711 within the valid MCU write period according to the setting in the Speech CODEC selection register on the receive side (RX_SCSEL[1:0]). When receive data is written from the MCU in the frame from which the switching of the Speech CODEC coding format has been detected, the LSI internal section performs decoding processing in the next frame. When receive data is not written from the MCU, the frame loss compensation processing (BFI) that is specified in G.729.A is performed in the next frame; however, a receive error (RXERR_CH1 = "1") does not occur.

If a receive error occurred before this frame, that receive error is cleared to "0" at termination of this frame.

To avoid sudden transition from a voice state to a silent state, the function that gradually attenuates decoding output (fade-out function) operates.

(Note)

If the coding format is switched outside of the valid MCU write period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check whether the receive request is for the receive data encoded in the G.729.A or encoded in the G.711 by referencing the receive Speech CODEC operation mode notification flag (RX_SCFLAG) when requesting reception due to the fall of FR1B.

③ G.711 operation (after switching)

Operates according to the operation that is effective on and after the third receive request that is described in ② Operation and ④ Error processing in Figure 20 G.711 (μ-law and A-law) receive buffer control method at single-channel operation (10 ms/ frame mode).

To avoid a sudden transition from a silent state to a voice state, the function that gradually amplifies the initial decoding output (fade-in function) operates.

B-2. G.729.A → G.711 (μ-law and A-law) switching control (20 ms frame mode)

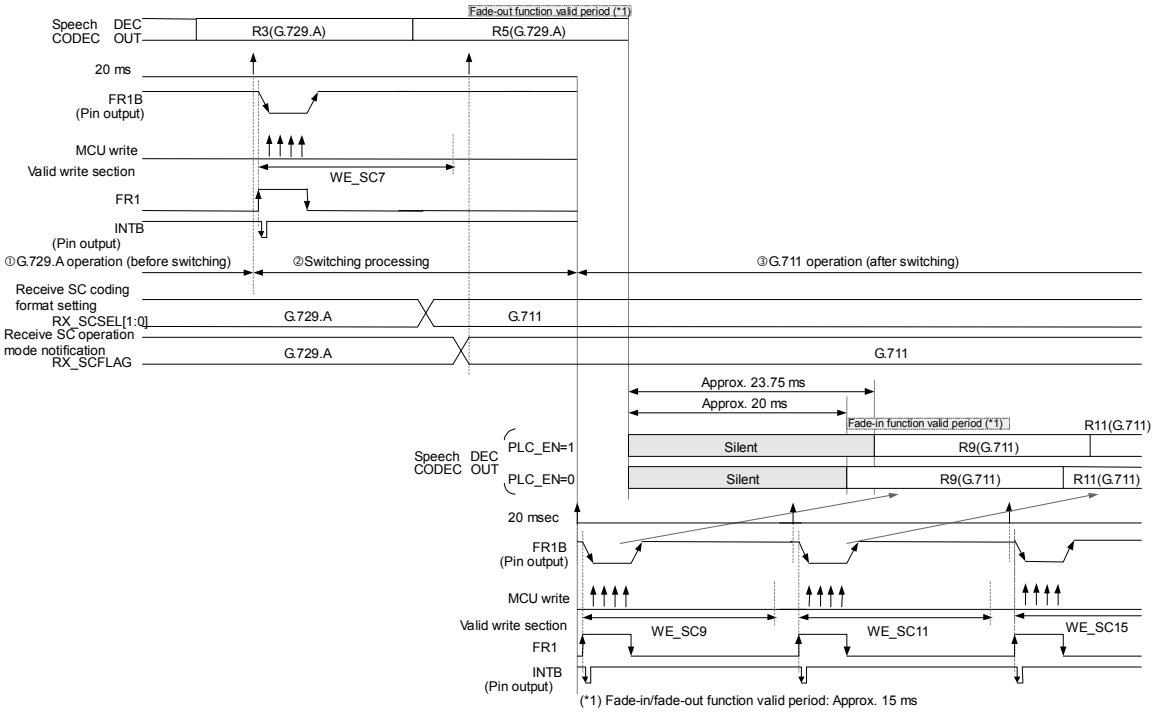


Figure 27 Speech CODEC Coding Format Switching Control Method on the Receive Side G.729.A→G.711 <20 ms frame mode>

① G.729.A operation (before switching)

Operates according to the contents described in ② Operation and ④ Error processing in Figure 19 G.729A receive buffer method at single-channel operation (20 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G729.A to G.711 within the valid MCU write period according to the setting in the Speech CODEC selection register on the receive side (RX_SCSEL[1:0]). When receive data is written from the MCU in the frame from which the switching of the Speech CODEC coding format has been detected, the LSI internal section performs decoding processing for the data of 10 ms in the next frame. When receive data is not written from the MCU, the frame loss compensation processing (BFI) that is specified in G.729.A is performed in the next frame; however, a receive error (RXERR_CH = "1") does not occur.

If a receive error occurred before this frame, that receive error is cleared to "0" at termination of this frame.

To avoid sudden transition from a voice state to a silent state, the function that gradually attenuates decoding output (fade-out function) operates.

(Note)

If the coding format is switched outside of the valid MCU write period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check whether the receive request is for the receive data encoded in the G.729.A or encoded in the G.711 by referencing the receive Speech CODEC operation mode notification flag (RX_SCFLAG) when requesting reception due to the fall of FR1B.

③ G.711 operation (after switching)

Operates according to the operation that is effective on and after the third receive request that is described in ② Operation and ④ Error processing in Figure 21 G.711 (μ-law and A-law) receive buffer control method at single-channel operation (20 ms/ frame mode).

To avoid a sudden transition from a silent state to a voice state, the function that gradually amplifies the initial decoded output that was initially written from the MCU (fade-in function) operates.

B-3. G.711 (μ-law and A-law) → G.729.A switching control (10 ms frame mode)

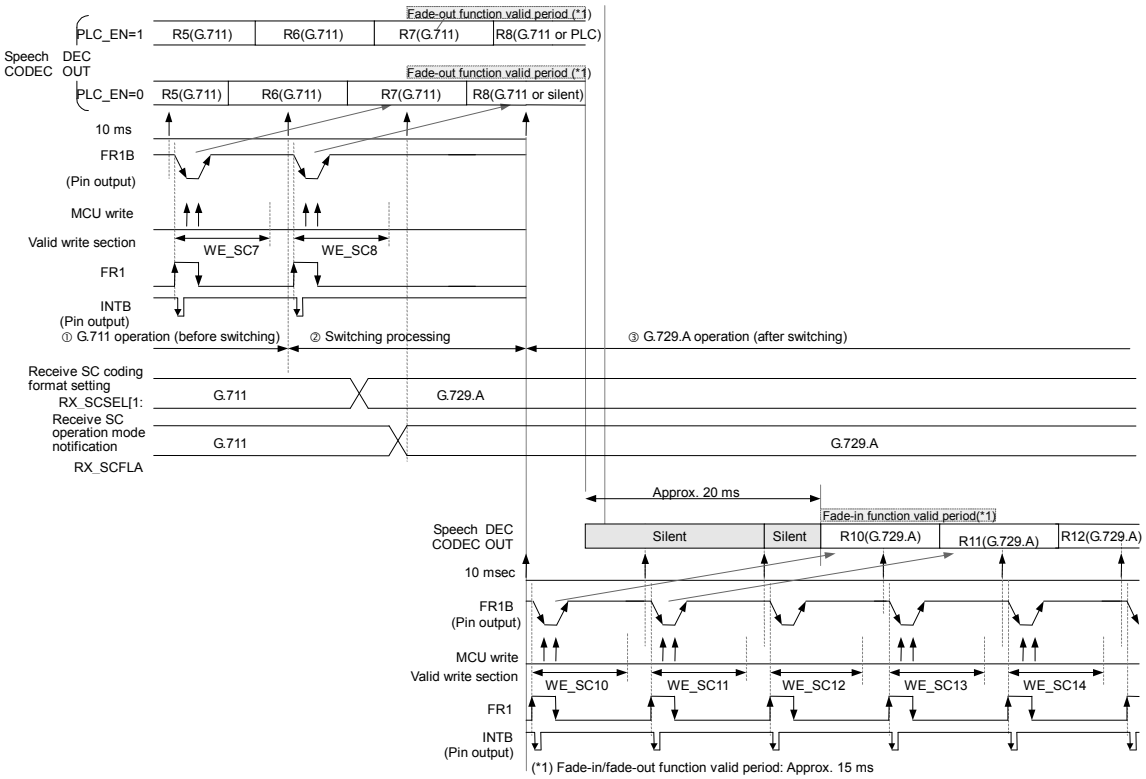


Figure 28 Speech CODEC Coding Format Switching Control Method on the Receive Side G.711→G.729.A<10 ms frame mode>

① G.711 operation (before switching)

Operates according to the contents described in ②Operation and ④Error processing in Figure 20 G.711 (μ-law and A-law) receive buffer control method at single-channel operation (10 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G.711 to G.729A within the valid MCU write period according to the setting in the Speech CODEC selection register on the receive side (RX_SCSEL[1:0]). When receive data is written from the MCU in the frame from which the switching of the Speech CODEC coding format has been detected, the LSI internal section performs decoding processing in the next frame. When receive data is not written from the MCU, data is generated according to the PLC algorithm and then output (silent output when the PLC function is disabled) in the next frame; however, a receive error (RXERR_CH = "1") does not occur.

If a receive error occurred before this frame, that receive error is cleared to "0" at termination of this frame. To avoid a sudden transition from a voice state to a silent state, the function that gradually attenuates the decoding output (fade-out function) operates.

(Note)

If the coding format is switched outside of the valid MCU write period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check whether the receive request is for the receive data encoded in the G.729.A or encoded in the G.711 by referencing the receive Speech CODEC operation mode notification flag (RX_SCFLAG) when requesting reception due to the fall of FR1B.

③ G.729.A operation (after switching)

Operates according to the operation that is effective on and after the second receive request that is described in ②Operation and ④Error processing in Figure 18 G.729.A receive buffer control method at single-channel operation (10 ms/ frame mode).

To avoid a sudden transition from a silent state to a voice state, the function that gradually amplifies the decoding output of the receive data that was initially written from MCU (fade-in function) operates.

B-4. G.711 (μ-law, A-law) → G.729.A switching control (20 ms frame mode)

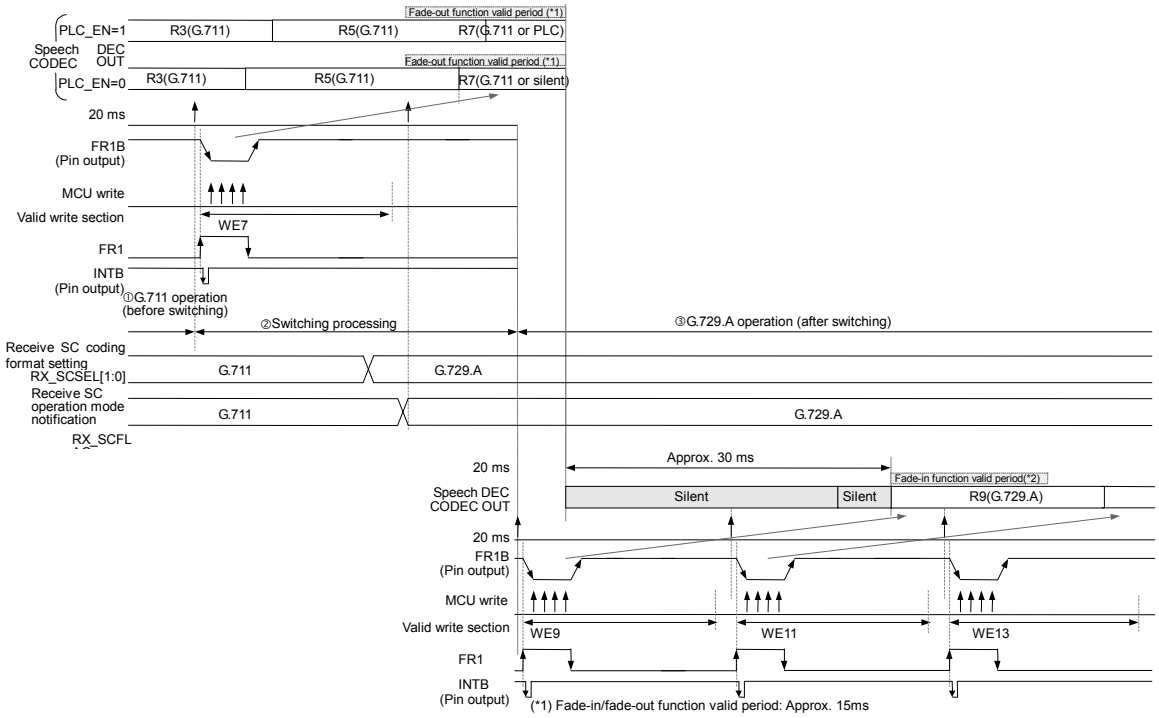


Figure 29 Speech CODEC Coding Format Switching Control Method on the Receive Side G.711→G.729.A <20 ms frame mode>

① G.711 operation (before switching)

Operates according to the contents described in ② Operation and ④ Error processing in Figure 21 G.711 (μ-law and A-law) receive buffer control method at single-channel operation (20 ms/frame mode).

② Switching processing

Switch the Speech CODEC coding format from G.711 to G.729.A within the valid MCU write period according to the setting in the Speech CODEC selection register on the receive side (RX_SCSEL[1:0]). When receive data is written from the the MCU in the frame from which the switching of the Speech CODEC coding format has benn detected, the LSI internal section performs decoding processing for the data of 10 ms in the next frame. When receive data is not written from the MCU, data is generated according to the PLC algorithm and then output (silent output when the PLC function is disabled) in the next frame; however, a receive error (RXERR_CH1 = "1") does not occur.

If a receive error occurred before this frame, that receive error is cleared to "0" at termination of this frame. To avoid a sudden transition from a voice state to a silent state, the function that gradually attenuates the decoding output (fade-out function) operates.

(Note)

If the coding format is switched outside of the valid MCU write period, the G.729.A → G.711 switching processing may be delayed by one frame. Therefore, check whether the receive request is for the receive data encoded in the G.729.A or encoded in the G.711 by referencing the receive Speech CODEC operation mode notification flag (RX_SCFLAG) when requesting reception due to the fall of FR1B.

③ G.729.A operation (after switching)

Operates according to the operation that is effective on and after the second receive request that is described in ②Operation and ④Error processing in Figure 19 G.729.A receive buffer control method at single channel operation (20 ms/ frame mode).

To avoid a sudden transition from a silent state to a voice state, the function that gradually amplifies the decoding output of the receive data that was initially written from MCU (fade-in function) operates.

Transmit/receive buffer control at 2-channel operation

When G.711 (μ-law/A-law) is selected as the Speech CODEC coding format for both transmission and reception operations, the mode for the following operations can be switched through the settings in SC_ EN (Speech CODEC control register) and DC_EN (2-channel operation control register).

Transmission and reception of voice data of a single channel (SC_EN = 1, DC_EN = 0)
Transmission and reception of 2-channel voice data (SC_EN = 1, DC_EN = 1)

The G.711 PLC function can be enabled or disabled by setting the option in the G.711 PLC function enable control register (G711_PLCEN). However, G711_PLCEN must be set to "0" (disabled) before activating 2-channel operation.

Figure 30 shows the transition of Speech CODEC operation modes when G.711 (μ-law/A-law) is selected as the Speech CODEC coding format for both transmission and reception operations.

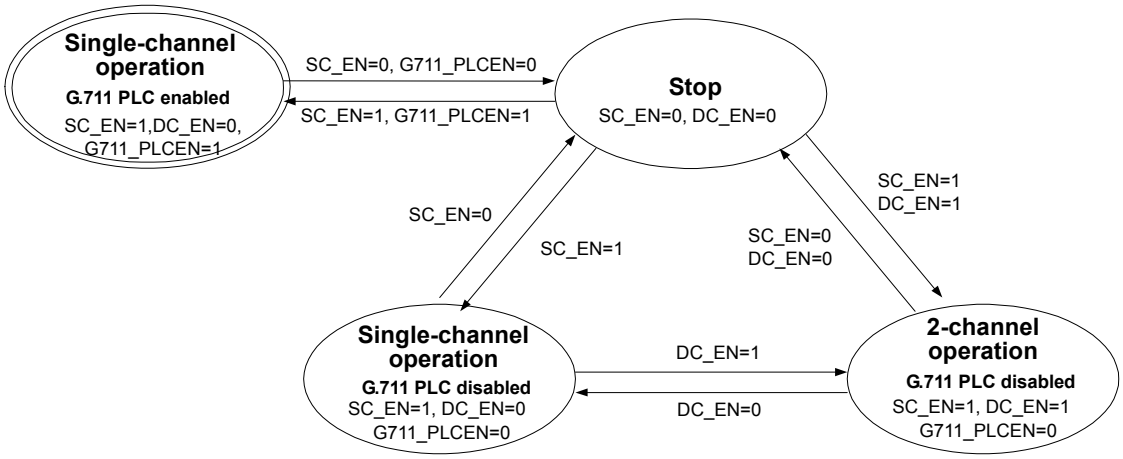


Figure 30 Transition of Speech CODEC Operation Modes (G.711 μ-law/A-law)

See Figures 16, 17, 20, and 21 for details of the transmit/receive buffer control method in single-channel operation.

See below for the details of the transmit/receive control method in 2-channel operation in Speech CODEC.

When 2-channel voice data transmission/reception is specified, Speech CODEC performs the following operation. The receive side decodes the received data of CH1 and CH2 that has been written from MCU and adds the data to the Speech CODEC output. The transmit side encodes the following two types of voice data and requests the reading of the data to the MCU for CH1 and CH2 individually.

Encoder input signal (CH1)
= (Transmit data AIN_x input to Speech CODEC) + (CH2 receive data Rx_CH2)
Encoder input signal (CH2)
= (Transmit data AIN_x input to Speech CODEC)+ (CH1 receive data Rx_CH1)

This function enables 3-way communication between the NW side (2 parties) and the terminal side (1 party). Figure 31 shows the transmit/receive data flow in Speech CODEC under the three-way communication that is performed between the terminal (A), which is connected to the analog interface of this LSI, and the terminal (B) and another terminal (C) on the NW side.
Figures 32 to 35 show the transmit/receive buffer control methods at 2-channel processing.

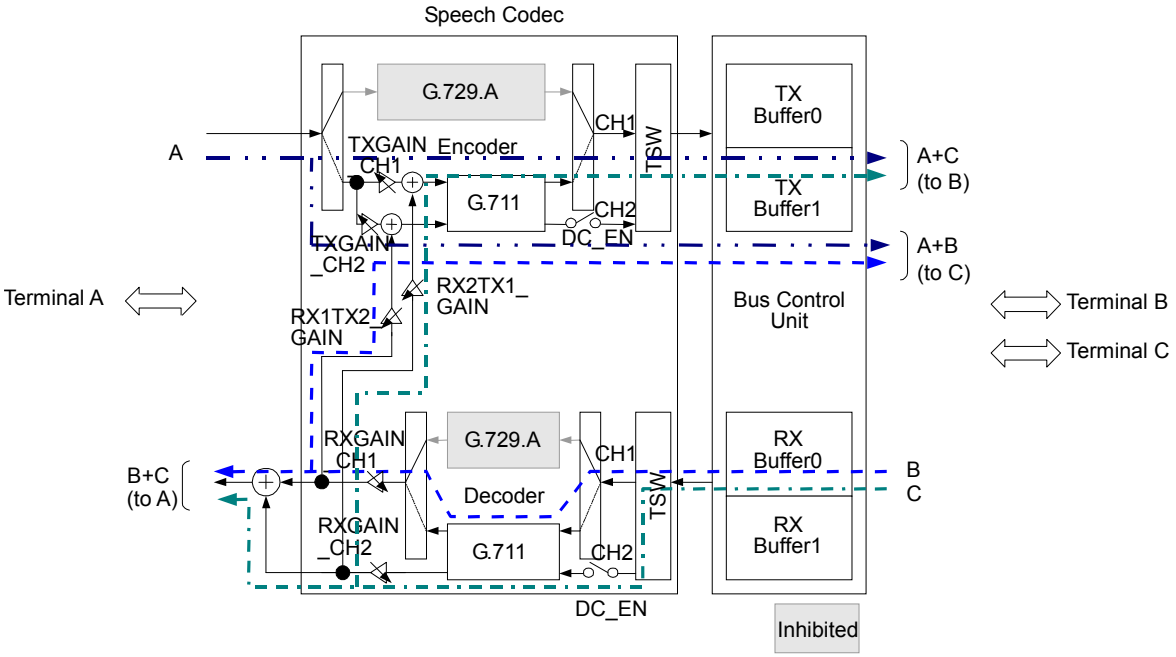


Figure 31 Transmit/Receive Data Flow at 2-Channel Operation

(Note)
When G.729.A is selected as the Speech CODEC coding format, the setting of DC_EN = 1 is inhibited.
When the G.711 PLC function is enabled, the setting of DC_EN = 1 is inhibited.

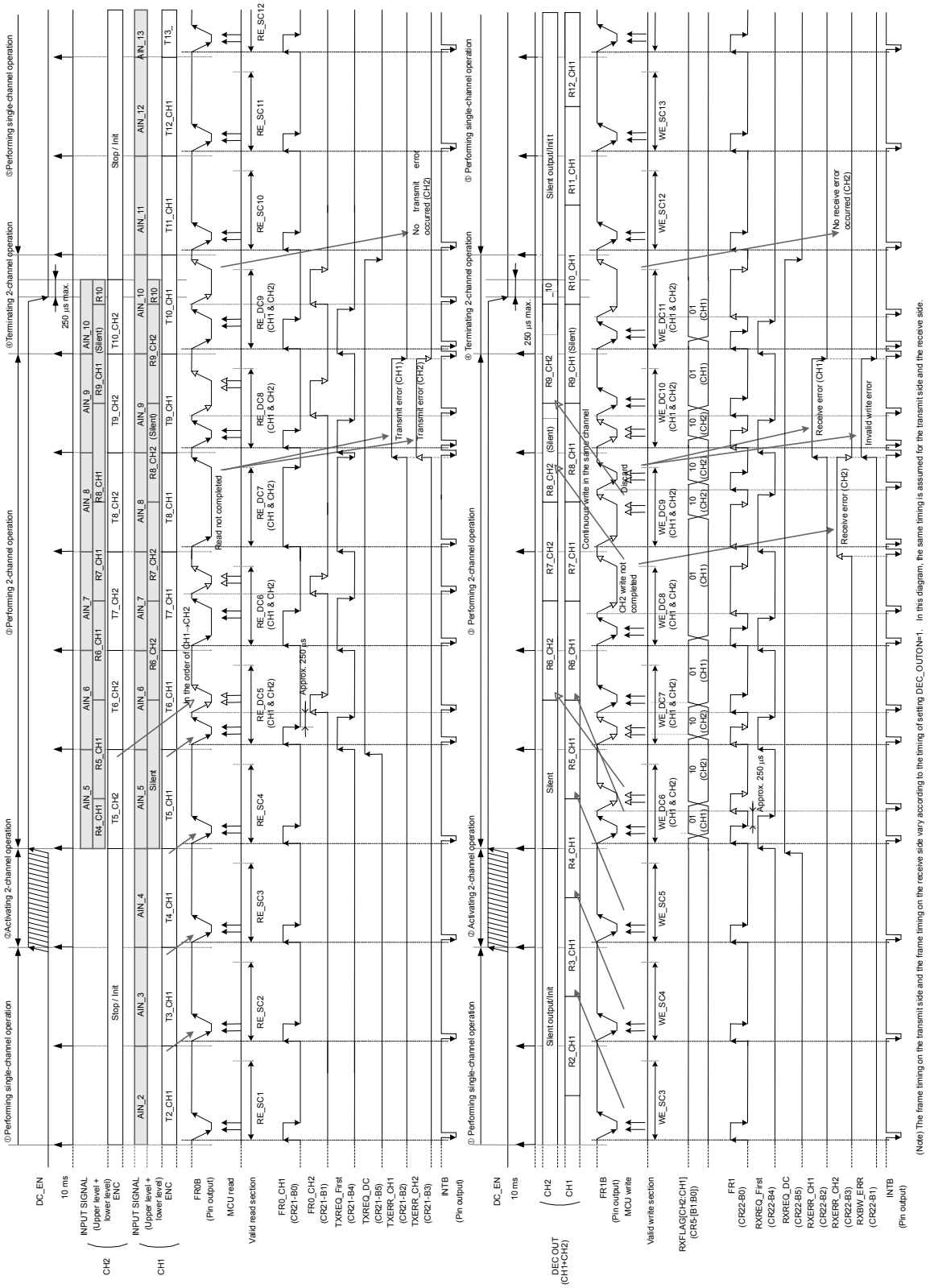


Figure 32 Transmit/Receive Buffer Control Method (10 ms frame, G.711) at 2-channel operation) <When changed from single-channel operation to 2-channel operation>

Description of operation (Figure 32)

① Performing single-channel operation

• Transmit

Operates according to the contents described in ② Operation and ④ Error processing in Figure 16.

• Receive

Operates according to the contents described in ② Operation and ④ Error processing in Figure 20. The G.711PLC function enable control register (G711_PLCEN) must be set to "0" at activation of Speech CODEC.

② Activating 2-channel operation

To change the mode from a single-channel operation mode to a 2-channel operation mode, set DC_EN = 1 (& SC_EN = 1).

Encoder: Starts encoding signals from CH1 and CH2 after processing of up to one frame following the setting of DC_EN = 1.

Decoder: Starts two receive data write requests in one frame after processing of up to one frame following the setting of DC_EN = 1.

(Note)

When G.729.A is selected as the Speech CODEC coding format, the setting of SC_EN = DC_EN = 1 is inhibited.

When the G.711 PLC function is enabled, the setting of SC_EN = DC_EN = 1 is inhibited.

③ Performing 2-channel operation

• Transmit

· 2-channel transmit request notification register (TXREQ_DC)

The 2-channel transmit request notification register (TXREQ_DC) is set to "1" while two transmit data read requests are issued in one frame.

· Channel data read sequence

Two transmit data read requests are issued in one frame in the order of CH1→CH2.

However, when read operation from the MCU side does not terminate for the CH1 transmit data read request, a read request for CH2 transmit data is not issued.

· Read sequence

After encoding processing for CH1 and CH2 of one frame terminates, an interrupt is generated by setting FR0_CH1 = 1 and a CH1 transmit data read request is issued. Read CH1 transmit data (80 bytes) according to the read request.

When CH1 transmit data read processing terminates, an interrupt is generated by setting FR0_CH2 = 1 and a CH2 transmit data read request is issued.

Read CH2 transmit data (80 bytes) according to the read request.

In this operation state, the following signals are input to the encoder from CH1 and CH2.

Encoder input signal (CH1) = (Transmit data AIN_x input to Speech CODEC) + (CH2 receive data Rx_CH2)

Encoder input signal (CH2) = (Transmit data AIN_x input to Speech CODEC) + (CH1 receive data Rx_CH1)

· Valid read period RE_DCn (CH1 & CH2)

Terminate transmit data read processing from CH1 and CH2 within 9.0 ms after a CH1 transmit data read request (FR0_CH1 = 1) is issued.

· Transmit error processing
If read processing from the MCU side does not terminate within the valid read period, an interrupt is generated by setting the transmit error flag of the relevant channel (CH1:TXERR_CH1, CH2:TXERR_CH2) to "1". The transmit error is retained from the next valid read period until just before termination of the frame for which transmit data read processing has been performed normally for the channel. Even if data read processing does not terminate, the data in the transmit buffer is updated normally.

• Receive
2-channel receive request notification register (RXREQ_DC)
In this operation state, the MCU side is notified that two receive data write requests will be issued in one frame by setting the 2-channel receive request notification register (RXREQ_DC) to "1".

· Data write channel sequence
Since data can be written to the channels in any sequence, write receive data in either sequence of CH1 → CH2 or CH2→CH1 in one frame.

(Note)
Do not write receive data of the same channel in one frame in such a manner as CH1 → CH1 and CH2 → CH2. If receive data of the same channel is written in one frame, the receive data that is written by the first receive request is decoded; however, the receive data that is written in the second receive request is discarded and an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1".

· Write procedure
This section describes the operation performed when receive data is written in the sequence of CH1 → CH2.
Write CH1 receive data (80 bytes) according to the first receive data write request (FR1 = 1&RXREQ_First = 1).
Before starting write operation of CH1 receive data, notify the LSI that CH1 receive data will be written by setting the receive data write channel notification register ((RXFLAG_[CH2:CH1]) to [0:1].
After termination of CH1 receive data write processing, the second receive data write request (FR1 = 1 & RXREQ_First = 0) is issued.
Write CH2 receive data (80 bytes) according to the second write request. In this case also, notify the LSI that CH2 receive data will be written by setting the receive data write channel notification register ((RXFLAG_[CH2:CH1]) to [1:0], before starting CH2 receive data write processing. When a receive data write request is issued, an interrupt is generated by setting FR1 to "1" regardless of the first or second request.

(Note)
The setting of RXFLAG_[CH2:CH1] = [1:1] or [0:0] is inhibited at notification of a receive data channel.
If RXFLAG_[CH2:CH1] = [1:1] or [0:0] is set, the receive data is discarded and an interrupt is generated by setting the receive side invalid write error flag (RXBW_ERR) to "1".

· Valid write period WE_DCn (CH1 & CH2)
The valid write period is 9 ms.

· Receive error processing
Terminate write processing of CH1 receive data and CH2 receive data within the valid write period.
If write processing from the MCU does not terminate within the valid write period, an interrupt is generated by setting the receive error flag of the relevant channel (CH1:RXERR_CH1 or CH2:RXERR_CH2) to "1".
The receive error is retained from the next valid write period until immediately before the termination of the frame for which receive data of the channel has been written normally. When write processing of the receive data of the channel is not performed, silent data is output.

When receive data of the same channel is written in one frame or the receive data channel notification is invalid, an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1". RXBW_ERR is retained from the next valid write period until immediately before the termination of the frame for which invalid receive data has no longer been written.

④ Terminating 2-channel operation

When returning a 2-channel operation mode to a single-channel operation mode, it is possible to notify which channel's transmit/receive data is continuously encoded or decoded by setting an option in ACTCH_FLAG.

To continue encoding/decoding of transmit/receive data of channel 1, set ACTCH_FLAG to "0" and then set SC_EN = 1 and DC_EN = 0. Encoding/decoding of channel 2 transmit/receive data stops within a maximum of 250 μs; however, encoding/decoding of channel 1 transmit/receive data continues.

To continue encoding/decoding of channel 2 transmit/receive data, set ACTCH_FLAG to "1" and then set SC_EN = 1 and DC_EN = 0. Encoding/decoding of channel 1 transmit/receive data stops within a maximum of 250 μs; however, encoding/decoding of channel 2 transmit/receive data continues. Figure 32 shows an example where exchange of channel 1 transmit/receive data is continued.

(Note)

1. In the frame where SC_EN = 1 and DC_EN = 0 are set, CH1/CH2 transmit data read requests and receive data write requests are issued normally. However, even if transmit data or receive data of the channel that was terminated is not read or written, an error does not occur.
2. After RXREQ_DC is cleared to "0", write processing to RXFLAG_[CH2:CH1] is not necessary.
3. To set DC_EN = 1 again after setting DC_EN = 0, a wait period of approx. 10 ms or more is required after TXREQ_DC = 0 and RXREQ_DC = 0 are set.

⑤ Performing single-channel operation

• Transmit

Operates according to the contents described in ② Operation and ④ Error processing in Figure 16.

Note that FR0_CH1 is set to "1" when a transmit data read request is issued in this operation state or the CH1 transmit error flag (TXERR_CH1) is set to "1" at the occurrence of an error also in this operation state, even if continuation of encoding/decoding of channel 2 transmit/receive data is set in ④ Terminating 2-channel operation.

• Receive

Operates according to the contents described in ② Operation and ④ Error processing in Figure 20. The G.711 PLC function enable control register (G711_PLCEN) is set to "0".

Note that the CH1 receive error flag (RXERR_CH1) is set to "1" at the occurrence of an error in this operation state even if continuation of encoding/decoding of the channel 2 transmit/receive data is set in ④ Terminating 2-channel operation.

Figure 33 Transmit/Receive Buffer Control Method at 2-Channel Operation (20 ms frame, G.711) <When changed from single-channel operation to 2-channel operation>

Description of operation (Figure 33)

① Performing single-channel operation

• Transmit

Operates according to the contents described in ②Operation and ④Error processing in Figure 17.

• Receive

Operates according to the contents described in ②Operation and ④Error processing in Figure 21. The G.711PLC function enable control register (G711_PLCEN) must be set to "0" at activation of Speech CODEC.

② Activating 2-channel operation

To change the mode from a single-channel operation mode to a 2-channel operation mode, set DC_EN = 1 (& SC_EN = 1).

Encoder: Starts encoding signals from CH1 and CH2 after processing of up to one frame following the setting of DC_EN = 1.

Decoder: Starts two receive data write requests in one frame after processing of up to one frame following the setting of DC_EN = 1.

(Note)

When G.729.A is selected as the Speech CODEC coding format, the setting of SC_EN = DC_EN = 1 is inhibited.

When the G.711 PLC function is enabled, the setting of SC_EN = DC_EN = 1 is inhibited.

③ Performing 2-channel operation

• Transmit

· 2-channel transmit request notification register (TXREQ_DC)

The 2-channel transmit request notification register (TXREQ_DC) is set to "1" while two transmit data read requests are issued in one frame.

· Channel data read sequence

Two transmit data read requests are issued in one frame in the order of CH1 → CH2.

However, when read operation from the MCU side does not terminate for the CH1 transmit data read request, a read request for CH2 transmit data is not issued.

· Read sequence

After encoding processing for CH1 and CH2 of one frame terminates, an interrupt is generated by setting FR0_CH1 and a CH1 transmit data read request is issued. Read CH1 transmit data (160 bytes) according to the read request.

When CH1 transmit data read processing terminates, an interrupt is generated by setting FR0_CH2 = 1 and a CH2 transmit data read request is issued.

Read CH2 transmit data (160 bytes) according to the read request.

In this operation state, the following signals are input to the encoder from CH1 and CH2.

Encoder input signal (CH1) = (Transmit data AIN_x input to Speech CODEC) + (CH2 receive data Rx_CH2)

Encoder input signal (CH2) = (Transmit data AIN_x input to Speech CODEC) + (CH1 receive data Rx_CH1)

· Valid read period RE_DCn(CH1 & CH2)

Terminate transmit data read processing from CH1 and CH2 within 18.0 ms after a CH1 transmit data read request (FR0_CH1 = 1) is issued.

· Transmit error processing
If read processing from the MCU side does not terminate within the valid read period, an interrupt is generated by setting the transmit error flag of the relevant channel (CH1: TXERR_CH1, CH2: TXERR_CH2) to "1". The transmit error is retained from the next valid read period until just before termination of the frame for which transmit data read processing has been performed normally for the channel. Even if data read processing does not terminate, the data in the transmit buffer is updated normally.

• Receive
· 2-channel receive request notification register (RXREQ_DC)
In this operation state, the MCU side is notified that two receive data write requests will be issued in one frame by setting the 2-channel receive request notification register (RXREQ_DC) to "1".

· Data write channel sequence
Since data can be written to the channels in any sequence, write receive data in either sequence of CH1 → CH2 or CH2 → CH1 in one frame.

(Note)
Do not write receive data of the same channel in one frame in such a manner as CH1 → CH1 and CH2 → CH2. If receive data of the same channel is written in one frame, the receive data that is written by the first receive request is decoded; however, the receive data that is written in the second receive request is discarded and an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1".

· Write procedure
This section describes the operation performed when receive data is written in the sequence of CH1 → CH2.
Write CH1 receive data (160 bytes) according to the first receive data write request (FR1 = 1 & RXREQ_First = 1).
Before starting write operation of CH1 receive data, notify the LSI that CH1 receive data will be written by setting the receive data write channel notification register ((RXFLAG_[CH2:CH1]) to [0:1].
After termination of CH1 receive data write processing, the second receive data write request (FR1 = 1 & RXREQ_First = 0) is issued.
Write CH2 receive data (160 bytes) according to the second write request. In this case also, notify the LSI that CH2 receive data will be written by setting the receive data write channel notification register ((RXFLAG_[CH2:CH1]) to [1:0], before starting CH2 receive data write processing. When a receive data write request is issued, an interrupt is generated by setting FR1 to "1" regardless of the first or second request.

(Note)
The setting of RXFLAG_[CH2:CH1] = [1:1] or [0:0] is inhibited at notification of a receive data channel.
If RXFLAG_[CH2:CH1] = [1:1] or [0:0] is set, the receive data is discarded and an interrupt is generated by setting the receive side invalid write error flag (RXBW_ERR) to "1".

· Valid write period WE_DCn (CH1 & CH2)
The valid write period is 18.0 ms.

· Receive error processing
Terminate write processing of CH1 receive data and CH2 receive data within the valid write period.
If write processing from the MCU does not terminate within the valid write period, an interrupt is generated by setting the receive error flag of the relevant channel (CH1: RXERR_CH1 or CH2: RXERR_CH2) to "1".
The receive error is retained from the next valid write period until immediately before the termination of the frame for which receive data of the channel has been written normally. When write processing of the receive data of the channel is not performed, silent data is output.

When receive data of the same channel is written in one frame or the receive data channel notification is invalid, an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1". RXBW_ERR is retained from the next valid write period until immediately before the termination of the frame for which invalid receive data has no longer been written.

④ Terminating 2-channel operation

When returning a 2-channel operation mode to a single-channel operation mode, it is possible to notify which channel's transmit/receive data is continuously encoded or decoded by setting an option in ACTCH_FLAG.
To continue encoding/decoding of transmit/receive data of channel 1, set ACTCH_FLAG to "0" and then set SC_EN = 1 and DC_EN = 0. Encoding/decoding of channel 2 transmit/receive data stops within a maximum of 250 μs; however, encoding/decoding of channel 1 transmit/receive data continues.
To continue encoding/decoding of channel 2 transmit/receive data, set ACTCH_FLAG to "1" and then set SC_EN = 1 and DC_EN = 0. Encoding/decoding of channel 1 transmit/receive data stops within a maximum of 250 μs; however, encoding/decoding of channel 2 transmit/receive data continues. Figure 33 shows an example where exchange of channel 1 transmit/receive data is continued.

(Note)
1. In the frame where SC_EN = 1 and DC_EN = 0 are set, CH1/CH2 transmit data read requests and receive data write requests are issued normally. However, even if transmit data or receive data of the channel that was terminated is not read or written, an error does not occur.
2. After RXREQ_DC is cleared to "0", write processing to RXFLAG_[CH2:CH1] is not necessary.
3. To set DC_EN = 1 again after setting DC_EN = 0, a wait period of about 10 ms or more is required after TXREQ_DC = 0 and RXREQ_DC = 0 are set.

⑤ Performing single-channel operation

• Transmit

Operates according to the contents described in ② Operation and ④ Error processing in Figure 17.
Note that FR0_CH1 is set to "1" when a transmit data read request is issued in this operation state or the CH1 transmit error flag (TXERR_CH1) is set to "1" at the occurrence of an error also in this operation state, even if continuation of encoding/decoding of channel 2 transmit/receive data is set in ④ Terminating 2-channel operation.

• Receive

Operates according to the contents described in ② Operation and ④ Error processing in Figure 21. The G.711 PLC function enable control register (G711_PLCEN) is set to "0".

Note that the CH1 receive error flag (RXERR_CH1) is set to "1" at the occurrence of an error in this operation state even if continuation of encoding/decoding of the channel 2 transmit/receive data is set in ④ Terminating 2-channel operation.

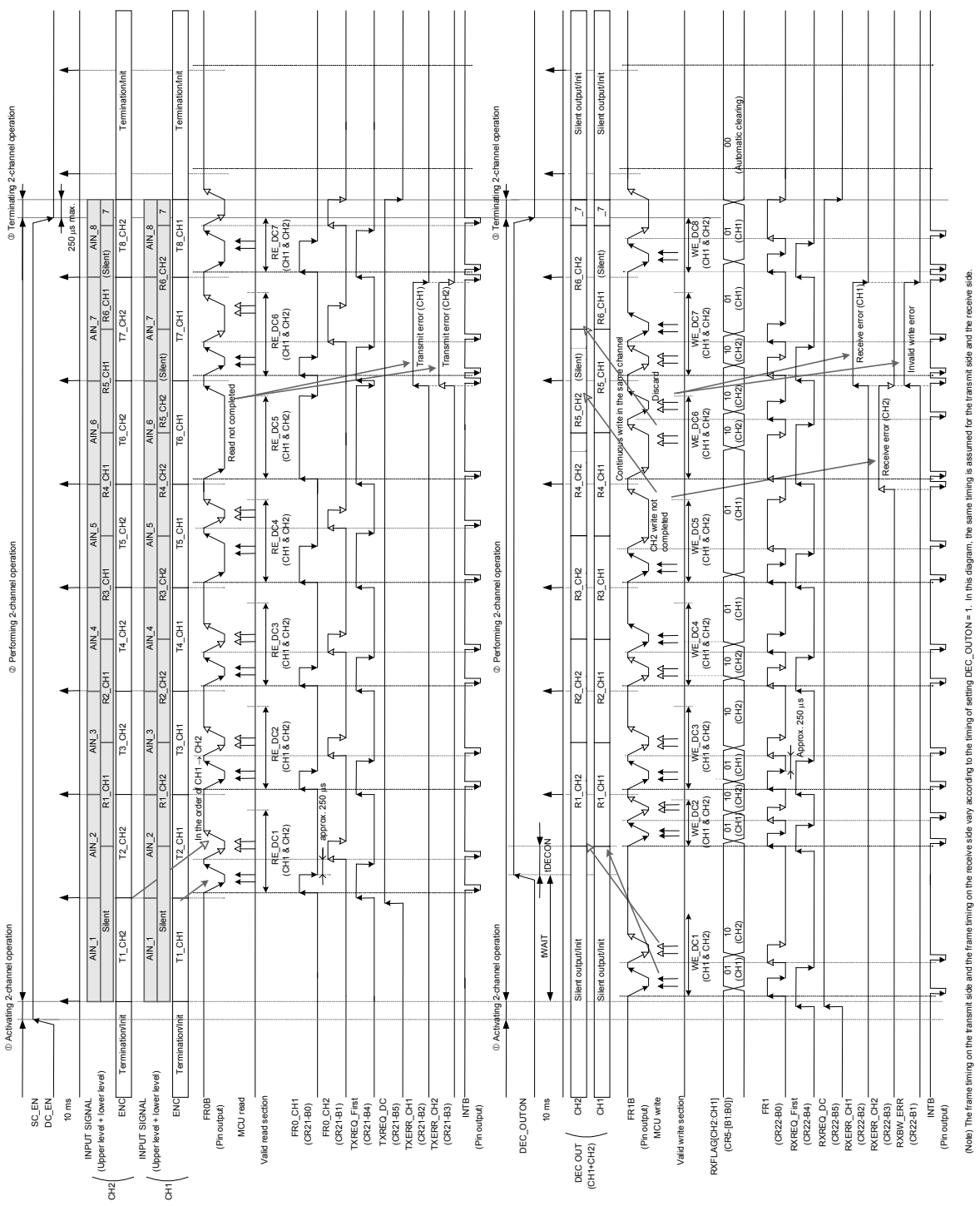


Figure 34 Transmit/Receive Buffer Control Method at 2-Channel Operation (10 ms frame, G.711) <When performing 2-channel operation from the beginning>

Description of operation (Figure 34)

① Activating 2-channel operation
To activate 2-channel operation from the Speech CODEC termination state, set SC_EN and DC_EN to "1" concurrently.
Encoder: Starts encoding of CH1 and CH2 signals within a maximum of 250 μs after SC_EN = DC_EN = 1 is set.
Decoder: Issues a receive data write request within a maximum of 250 μs after SC_EN = DC_EN = 1 is set.

(Note)
When G.729.A is selected as the Speech CODEC coding format, the setting of SC_EN = DC_EN = 1 is inhibited.
When the G.711 PLC function is enabled, the setting of SC_EN = DC_EN = 1 is inhibited.

②Performing 2-channel operation
• Transmit
· 2-channel transmit request notification register (TXREQ_DC)
The 2-channel transmit request notification register (TXREQ_DC) is set to "1" while two transmit data read requests are issued in one frame.

· Channel data read sequence
Two transmit data read requests are issued in one frame in the order of CH1 → CH2.
However, when read operation from the MCU side does not terminate for the CH1 transmit data read request, a read request for CH2 transmit data is not issued.

· Read sequence
After encoding processing for CH1 and CH2 of one frame terminates, an interrupt is generated by setting FR0_CH1 = 1 and a CH1 transmit data read request is issued. Read CH1 transmit data (80 bytes) according to the read request.
When CH1 transmit data read processing terminates, an interrupt is generated by setting FR0_CH2 = 1 and a CH2 transmit data read request is issued.
Read CH2 transmit data (80 bytes) according to the read request.
In this operation state, the following signals are input to the encoder from CH1 and CH2.
Encoder input signal (CH1) = (Transmit data AIN_x input to Speech CODEC) + (CH2 receive data Rx_CH2)
Encoder input signal (CH2) = (Transmit data AIN_x input to Speech CODEC) + (CH1 receive data Rx_CH1)

· Valid read period RE_DCn(CH1 & CH2)
Terminate transmit data read processing from CH1 and CH2 within 9.0 ms after a CH1 transmit data read request (FR0_CH1 = 1) is issued.

· Transmit error processing
If read processing from the MCU side does not terminate within the valid read period, an interrupt is generated by setting the transmit error flag of the relevant channel (CH1: TXERR_CH1, CH2: TXERR_CH2) to "1". The transmit error is retained from the next valid read period until just before termination of the frame for which transmit data read processing has been performed normally for the channel. Even if data read processing does not terminate, the data in the transmit buffer is updated normally.

• Receive

· 2-channel receive request notification register (RXREQ_DC)
In this operation state, the MCU side is notified that two receive data write requests will be issued in one frame by setting the 2-channel receive request notification register (RXREQ_DC) to "1".

· Data write channel sequence
Since data can be written to the channels in any sequence, write receive data in either sequence of CH1 → CH2 or CH2 → CH1 in one frame.

(Note)
Do not write receive data of the same channel in one frame in such a manner as CH1 → CH1 and CH2 → CH2. If receive data of the same channel is written in one frame, the receive data that is written by the first receive request is decoded; however, the receive data that is written in the second receive request is discarded and an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1".

· Write procedure
This section describes the operation performed when receive data is written in the sequence of CH1 → CH2.
Write CH1 receive data (80 bytes) according to the first receive data write request (FR1 = 1&RXREQ_First = 1).
Before starting write operation of CH1 receive data, notify the LSI that CH1 receive data will be written by setting the receive data write channel notification register (RXFLAG_[CH2:CH1]) to [0:1].
After termination of CH1 receive data write processing, the second receive data write request (FR1 = 1 & RXREQ_First = 0) is issued.
Write CH2 receive data (80 bytes) according to the second write request. In this case also, notify the LSI that CH2 receive data will be written by setting the receive data write channel notification register (RXFLAG_[CH2:CH1]) to [1:0], before starting CH2 receive data write processing. When a receive data write request is issued, an interrupt is generated by setting FR1 to "1" regardless of the first or second request.

(Note)
The setting of RXFLAG_[CH2:CH1] = [1:1] or [0:0] is inhibited at notification of a receive data channel.
If RXFLAG_[CH2:CH1] = [1:1] or [0:0] is set, the receive data is discarded and an interrupt is generated by setting the receive side invalid write error flag (RXBW_ERR) to "1".

· Valid write period WE_DCn (CH1 & CH2)
WE_DC1 (CH1 & CH2)
There is no time restriction on the initial valid write period after activation of Speech CODEC (CH1 & CH2).
DEC_OUTON can be set to "1" after a lapse of the tWAIT time following completion of receive data write processing for CH1 and CH2. Decoding output starts tDECON after DEC_OUTON is set to "1". (*)
(tWAIT=1ms, tDECON = 0 ms[initial value] ... Can be set within the range from 0.125 to 32 ms in the internal data memory.)
WE_DC2 (CH1 & CH2)
The second valid write period is 4 ms.
WE_DCn (CH1 & CH2) n = 3, 4, 5, ...
The third valid write period is 9 ms.

(Note) (*)
It is prohibited to change the mode to a single-channel operation mode (SC_EN = 1, DC_EN = 0) before the decoding output starting offset time elapses after DEC_OUTON is set to "1".

· Receive error processing
Terminate write processing of CH1 receive data and CH2 receive data within the valid write period.
If write processing from the MCU does not terminate within the valid write period, an interrupt is generated by setting the receive error flag of the relevant channel (CH1: RXERR_CH1 or CH2: RXERR_CH2) to "1".
The receive error is retained from the next valid write period until immediately before the termination of the frame for which receive data of the channel has been written normally. When write processing of the receive data of the channel is not performed, silent data is output.

When receive data of the same channel is written in one frame or the receive data channel notification is invalid, an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1". RXBW_ERR is retained from the next valid write period until immediately before the termination of the frame for which invalid receive data has no longer been written.

③ Terminating 2-channel operation
To return from a 2-channel mode to a termination mode, set SC_EN = 0 and DC_EN = 0. The encoder of Speech CODEC (CH1 & CH2) stops data write processing within a maximum of 250 μs after SC_EN = 0 and DC_EN = 0 are set.
(Note)
1. After SC_EN = 0 and DC_EN = 0 are set, RXFLAG_[CH2:CH1] are cleared to 00b automatically within a maximum of 250 μs.
2. A wait period of 10 ms or more is required after SC_EN = 0 is set until SC_EN = 1 is set again.

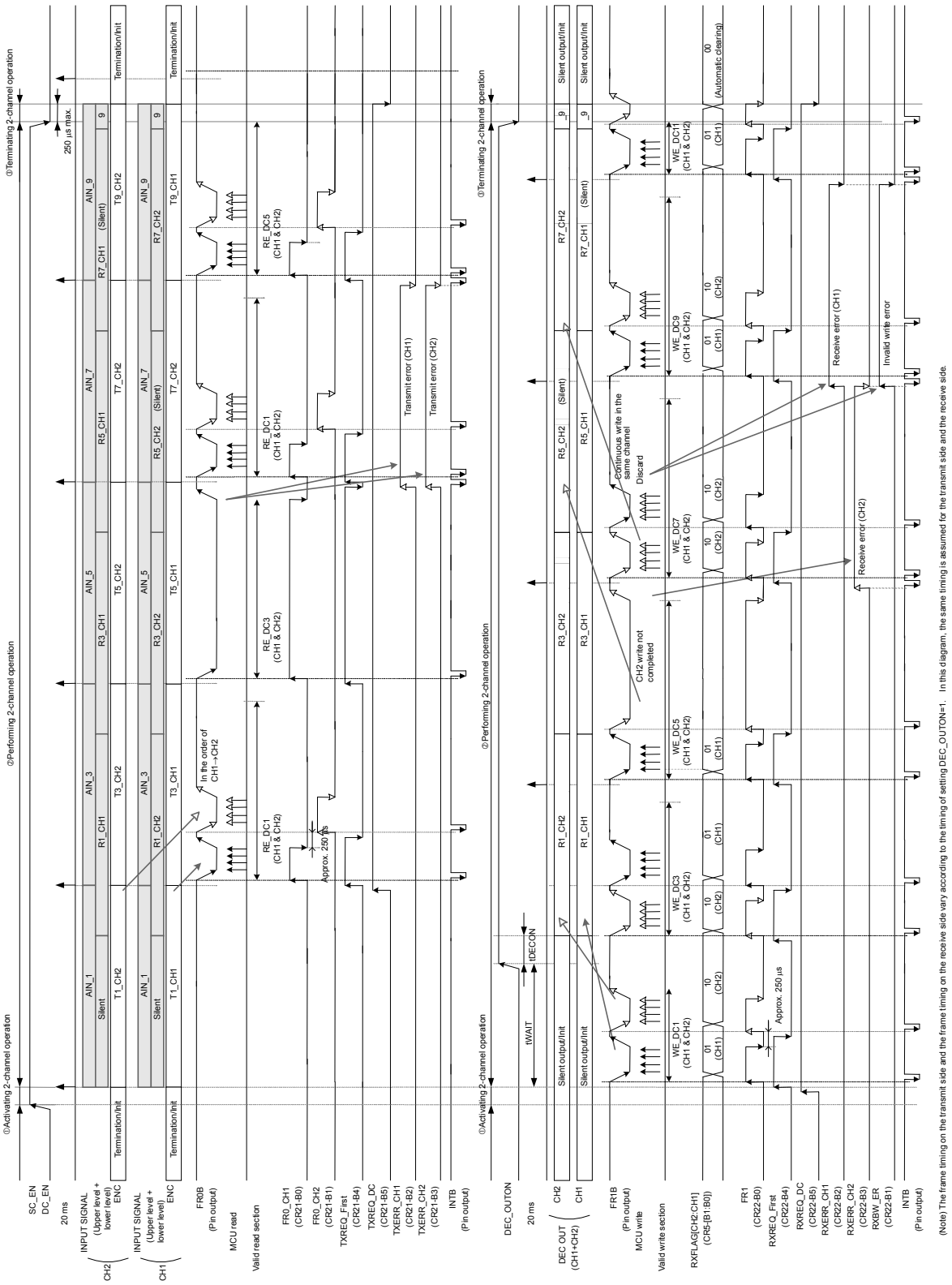


Figure 35 Transmit/Receive Buffer Control Method at 2-Channel Operation (20 ms frame, G.711) <When performing 2-channel operation from the beginning>

Description of operation (Figure 35)

① Activating 2-channel operation
To activate 2-channel operation from the Speech CODEC termination state, set SC_EN and DC_EN to "1" concurrently.
Encoder: Starts encoding of CH1 and CH2 signals within a maximum of 250 μs after SC_EN = DC_EN = 1 is set.
Decoder: Issues a receive data write request within a maximum of 250 μs after SC_EN = DC_EN = 1 is set.

(Note)
When G.729.A is selected as the Speech CODEC coding format, the setting of SC_EN = DC_EN = 1 is inhibited.
When the G.711 PLC function is enabled, the setting of SC_EN = DC_EN = 1 is inhibited.

② Performing 2-channel operation
• Transmit
· 2-channel transmit request notification register (TXREQ_DC)
The 2-channel transmit request notification register (TXREQ_DC) is set to "1" while two transmit data read requests are issued in one frame.

· Channel data read sequence
Two transmit data read requests are issued in one frame in the order of CH1 → CH2.
However, when read operation from the MCU side does not terminate for the CH1 transmit data read request, a read request for CH2 transmit data is not issued.

· Read sequence
After encoding processing for CH1 and CH2 of one frame terminates, an interrupt is generated by setting FR0_CH1 = 1 and a CH1 transmit data read request is issued. Read CH1 transmit data (160 bytes) according to the read request.
When CH1 transmit data read processing terminates, an interrupt is generated by setting FR0_CH2 = 1 and a CH2 transmit data read request is issued.
Read CH2 transmit data (160 bytes) according to the read request.
In this operation state, the following signals are input to the encoder from CH1 and CH2.
Encoder input signal (CH1) = (Transmit data AIN_x input to Speech CODEC) + (CH2 receive data Rx_CH2)
Encoder input signal (CH2) = (Transmit data AIN_x input to Speech CODEC) + (CH1 receive data Rx_CH1)

· Valid read period RE_DCn(CH1 & CH2)
Terminate transmit data read processing from CH1 and CH2 within 18.0 ms after a CH1 transmit data read request (FR0_CH1 = 1) is issued.

· Transmit error processing
If read processing from the MCU side does not terminate within the valid read period, an interrupt is generated by setting the transmit error flag of the relevant channel (CH1: TXERR_CH1, CH2: TXERR_CH2) to "1". The transmit error is retained from the next valid read period until just before termination of the frame processing for which transmit data read processing has been performed normally for the channel. Even if data read processing does not terminate, the data in the transmit buffer is updated normally.

• Receive

· 2-channel receive request notification register (RXREQ_DC)
In this operation state, the MCU side is notified that two receive data write requests will be issued in one frame by setting the 2-channel receive request notification register (RXREQ_DC) to "1".

· Data write channel sequence
Since data can be written to the channels in any sequence, write receive data in either sequence of CH1 → CH2 or CH2 → CH1 in one frame.

(Note)
Do not write receive data of the same channel in one frame in such a manner as CH1 → CH1 and CH2 → CH2. When receive data of the same channel is written in one frame, the receive data that is written by the first receive request is decoded; however, the receive data that is written in the second receive request is discarded and an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1".

· Write procedure
This section describes the operation performed when receive data is written in the sequence of CH1 → CH2.
Write CH1 receive data (160 bytes) according to the first receive data write request (FR1 = 1 & RXREQ_First = 1).
Before starting write operation of CH1 receive data, notify the LSI that CH1 receive data will be written by setting the receive data write channel notification register ((RXFLAG_[CH2: CH1]) to [0:1].
After termination of CH1 receive data write processing, the second receive data write request (FR1 = 1 & RXREQ_First = 0) is issued.
Write CH2 receive data (160 bytes) according to the second write request. In this case also, notify the LSI that CH2 receive data will be written by setting the receive data write channel notification register ((RXFLAG_[CH2:CH1]) to [1:0]., before starting CH2 receive data write processing. When a receive data write request is issued, an interrupt is generated by setting FR1 to "1" regardless of the first or second request.

(Note)
The setting of RXFLAG_[CH2:CH1] = [1:1] or [0:0] is inhibited at notification of a receive data channel.
If RXFLAG_[CH2:CH1] = [1:1] or [0:0] is set, the receive data is discarded and an interrupt is generated by setting the receive side invalid write error flag (RXBW_ERR) to "1".

· Valid write period WE_DCn (CH1 & CH2)
WE_DC1 (CH1 & CH2)
There is no time restriction on the initial valid write period after activation of Speech CODEC (CH1 & CH2).
DEC_OUTON can be set to "1" after a lapse of the tWAIT time following completion of receive data write processing for CH1 and CH2. Decoding output starts tDECON after DEC_OUTON is set to "1". (*)
(tWAIT = 1ms, tDECON = 0 ms[initial value] ... Can be set within the range from 0.125 to 32 ms in the internal data memory.)
WE_DC2 (CH1 & CH2)
The second valid write period is 13 ms.
WE_DCn (CH1 & CH2) n = 3, 4, 5, ...
The third valid write period is 18 ms.

(Note) (*)
It is inhibited to change the mode to a single-channel operation mode (SCN=1, DC_EN=0) before the decoding output starting offset time elapses after DEC_OUTON is set to "1".

· Receive error processing
Terminate write processing of CH1 receive data and CH2 receive data within the valid write period.
If write processing from the MCU does not terminate within the valid write period, an interrupt is generated by setting the receive error flag of the relevant channel (CH1: RXERR_CH1 or CH2: RXERR_CH2) to "1".
The receive error is retained from the next valid write period until immediately before the termination of the frame for which receive data of the channel has been written normally. When write processing of the receive data of the channel is not performed, silent data is output.

When receive data of the same channel is written in one frame or the receive data channel notification is invalid, an interrupt is generated by setting a receive side invalid write error flag (RXBW_ERR) to "1". RXBW_ERR is retained from the next valid write period until immediately before the termination of the frame for which invalid receive data has no longer been written.

③ Terminating 2-channel operation
To return from a 2-channel operation mode to a termination mode, set SC_EN = 0 and DC_EN = 0. The encoder of Speech CODEC (CH1 & CH2) stops data write processing within a maximum of 250 μs after SC_EN = 0 and DC_EN = 0 are set.
(Note)
1. After SC_EN = 0 and DC_EN = 0 are set, RXFLAG_[CH2:CH1] are cleared to 00b automatically within a maximum of 250 μs.
2. A wait period of 10 ms or more is required after SC_EN = 0 is set until SC_EN = 1 is set again.

Control Register Control Method

Figure 36 shows the control register control method.
This LSI incorporates control registers CR0-CR47 and GPCR0-GPCR8 for performing control. The LSI also performs control by changing the DSP internal data memory that is built into the LSI using the following control registers allocated in those control registers.

Internal data memory 1-word write control register (XDMWR)
Internal data memory 2-word write control register (XDMWR_2)
Internal data memory address and data setting registers (CR6-CR9)

See the INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD that are described later for the access method of the DSP internal data memory.
See Tables 5 to 9 for control register addresses.
The control registers are controlled with an 8-bit width of D7 to D0 regardless of the data width of 16 bits or 8 bits that is selected in the MCU interface data width selection register (BW_SEL). When a data bus is used in 16-bit access mode, input-output of D15-D8 depends on the write or read control of the control register. At write processing, "1" or "0" is set in D15-D8 and at read processing, "1" is read.

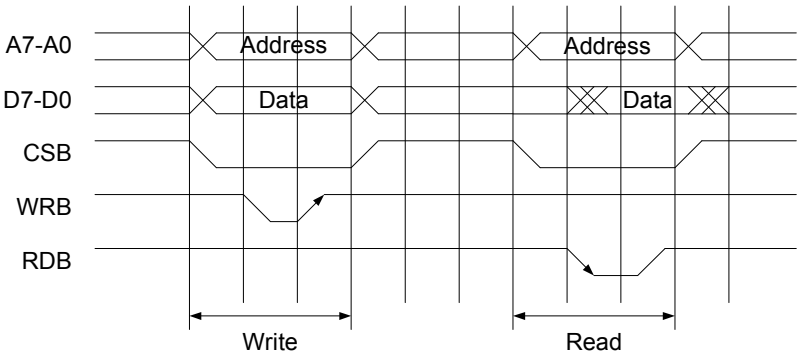


Figure 36 Control Register Control Method

Transmit/Receive Buffer Access Method

A. Frame mode (FRAME/DMA selection register FD_SEL = "0")

Figure 37 shows the transmit buffer (TX Buffer) control timing and access method in frame mode.

When the transmit buffer storing compressed voice data on the transmit side (voice data compression side) becomes full, a read request is issued to the MCU side by changing FR0B from "H" to "L". Read data from the data transmit buffer in the following timing. The transmit buffer read address is "80h". FR0B maintains "L" until the entire data in the transmit buffer is read.

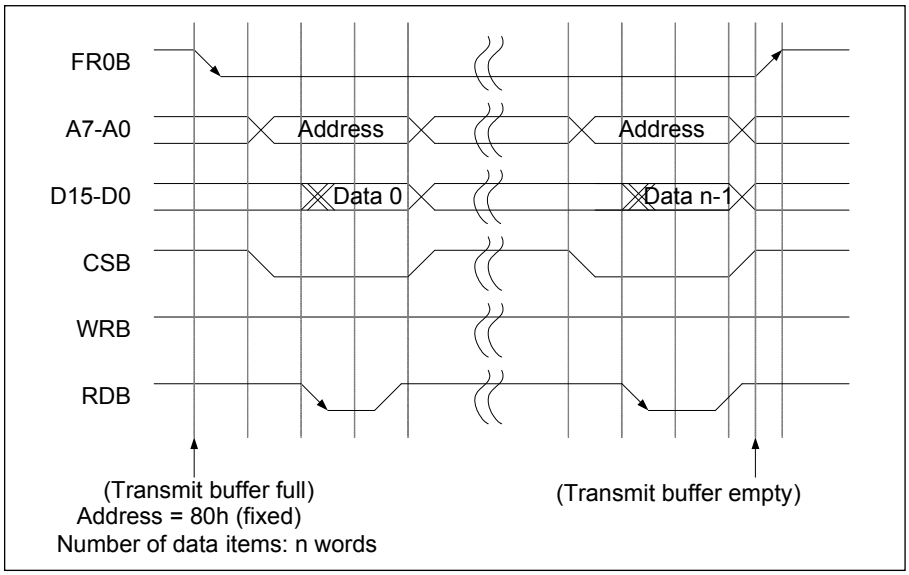


Figure 37 Transmit Buffer Control Timing

Figure 38 shows the receive buffer (RX Buffer) control timing in frame mode. When the receive buffer storing compressed voice data on the receive side (voice expansion side) becomes empty, a write request is issued to the MCU side by setting FR1B from "H" to "L". Write data in the receive buffer in the following timing. The receive buffer write address is "81h". FR1B maintains "L" until the receive buffer becomes full.

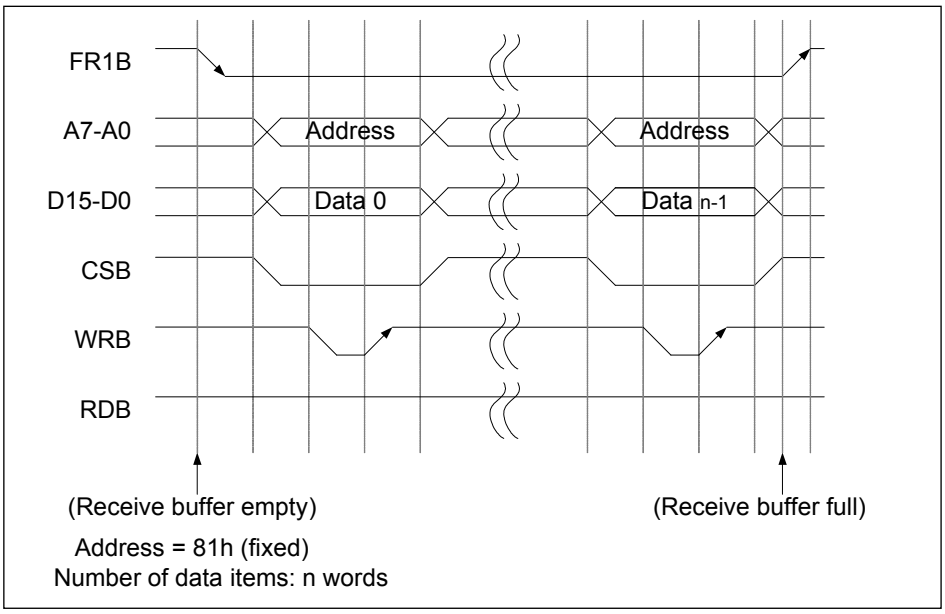


Figure 38 Receive Buffer Control Timing

B. DMA mode (FRAME/DMA selection register FD_SEL = "1")
Figure 39 shows the transmit buffer control timing in DMA mode. When the transmit buffer for storing compressed voice data on the transmit side (voice data compression side) becomes full, DMARQ0B goes to "L" from "H", thereby issuing a DMA request to the MCU side. After the DMA request is issued, when DMAACK0B becomes "0" from "1", acknowledgement is input. Then, when the fall of the read enable signal (RDB = "1" → "0") is accepted, DMARQ0B is automatically cleared ("L" → "H"). Read the data from the transmit buffer in the following timing concurrently with acknowledgment input. DMARQ0B continues issuing a DMA request until the entire data in the transmit buffer is read.

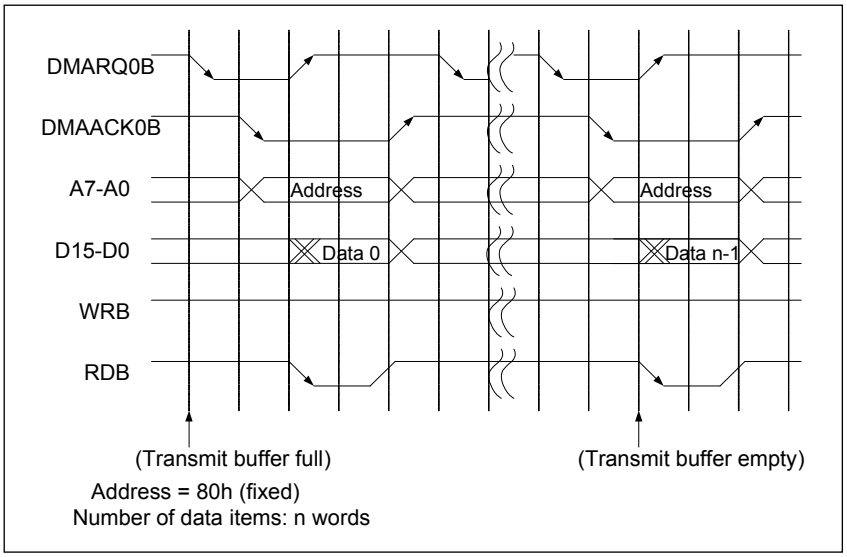


Figure 39 Transmit Buffer Control Timing in DMA Mode

Figure 40 shows the receive buffer control timing in DMA mode. When the receive buffer that stores compressed voice data on the receive side (voice data expansion side) becomes empty, DMARQ1B goes to "L" from "H", thereby issuing a DMA request to the MCU side. When DMAACK1B is set from "1" to "0" after the DMA request is issued, acknowledgment is input. Then, when the fall of the write enable signal (WRB="1" → "0") is accepted, DMARQ1B is automatically cleared ("L" → "H"). Write data to the receive buffer in the following timing concurrently with acknowledgement input. DMARQ1B continues issuing a DMA request until the receive buffer becomes full.

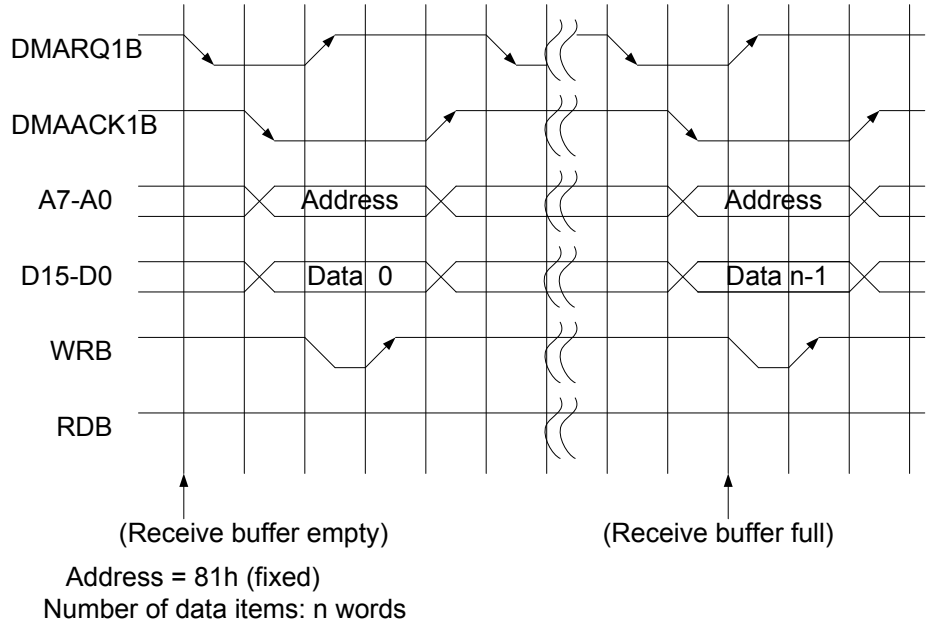
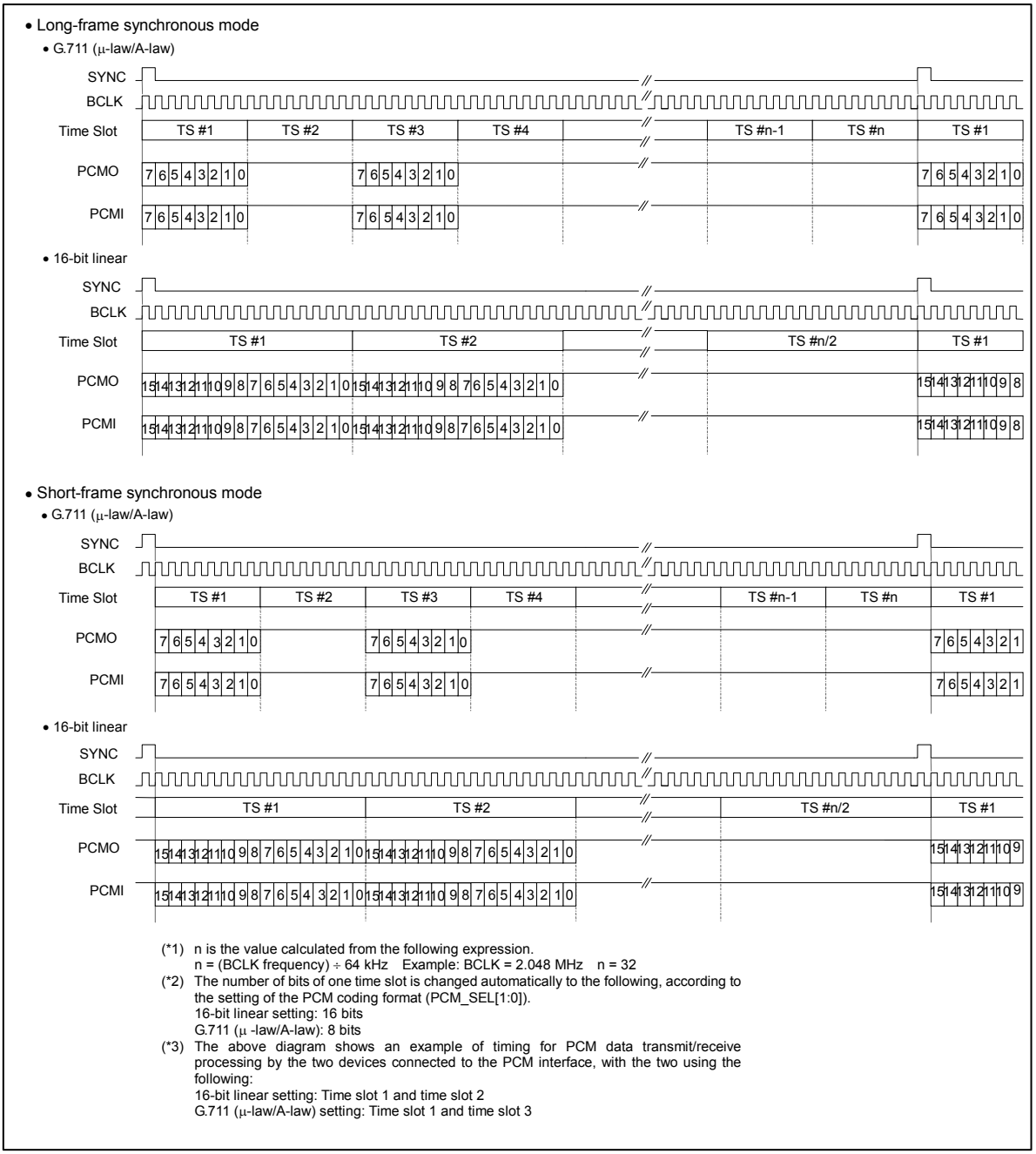


Figure 40 Receive Buffer Control Timing in DMA Mode

PCM Interface

A. Example of PCM interface bit configuration
Figure 41 shows an example of PCM interface bit configuration.



(*1) n is the value calculated from the following expression.
n = (BCLK frequency) ÷ 64 kHz Example: BCLK = 2.048 MHz n = 32
(*2) The number of bits of one time slot is changed automatically to the following, according to the setting of the PCM coding format (PCM_SEL[1:0]).
16-bit linear setting: 16 bits
G.711 (μ -law/A-law): 8 bits
(*3) The above diagram shows an example of timing for PCM data transmit/receive processing by the two devices connected to the PCM interface, with the two using the following:
16-bit linear setting: Time slot 1 and time slot 2
G.711 (μ-law/A-law) setting: Time slot 1 and time slot 3

Figure 41 Example of PCM Interface Bit Configuration

B. Time slot assignment function

The PCM interface of this LSI is compatible with the serial transmission rate from 64 kHz to 2.048 MHz. Therefore, by connecting multiple LSIs on the PCM interface, it is possible to logically achieve PCM data multiplexing of up to 32 slots at G.711(μ-law/A-law) setting and up to 16 slots at 16-bit linear setting.
This LSI can be set up to 3 input time slots independently by using the following registers:
PCM input time slot selection register 1 (PCM_ITS1[4:0])
PCM input time slot selection register 2 (PCM_ITS2[4:0])
PCM input time slot selection register 3 (PCM_ITS3[4:0])
Also, 2 output time slots can be set independently by using the following registers:
PCM output time slot selection register 1(PCM_OTS1[4:0])
PCM output time slot selection register 2(PCM_OTS2[4:0])
Note that the following rules are applied for the setting of time slots.

(Note)
The number of bits of one time slot changes automatically according to the setting of the PCM coding format (PCM_SELL [1:0])as follows.
16-bit linear setting: 16 bits
G.711 (μ-law/A-law) setting: 8 bits
Therefore, the maximum number of time slots that can be set will be as follows:
16-bit linear setting: n/2
G.711 (μ-law/A-law) setting: n
[n = (BCLK frequency) ÷ 64 kHz]
Setting a time slot number greater than the largest time slot number indicated above is inhibited.

C. Application example
By connecting multiple LSIs on the PCM interface, two-way communication or three-way communication is enabled.

C-1. Two-way communication
Figure 42 shows an application example of two-way communication by transmitting/receiving PCM data between two ML7204 devices connected on the PCM interface.

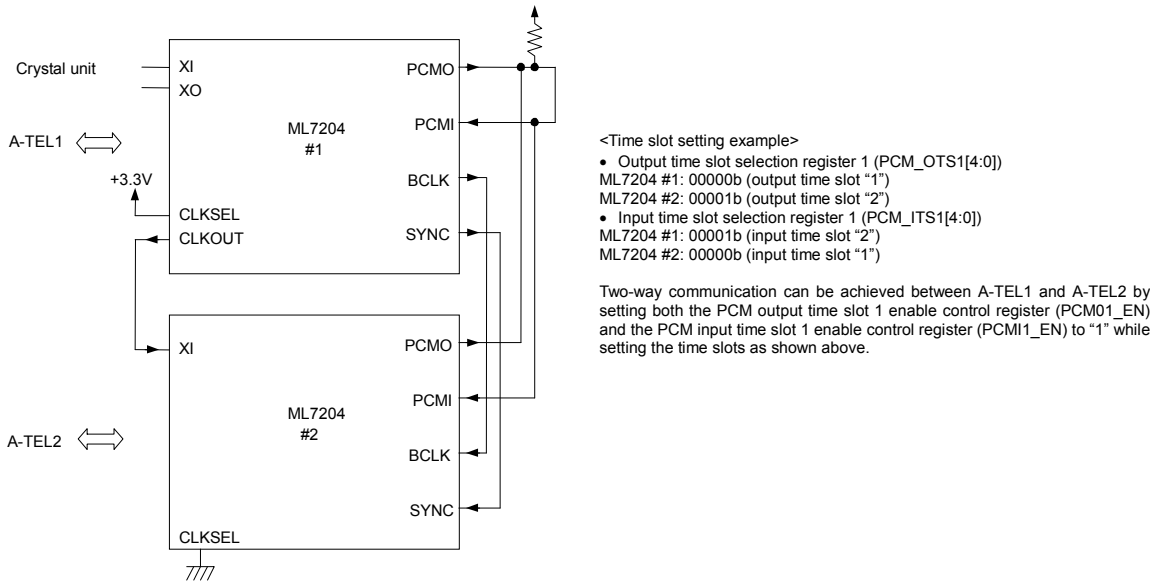


Figure 42 Example of Connection for Two-Way Communication via PCM I/F

C-2. Three-way communication

Figure 43 shows an application example of three-way communication performed by transmitting/receiving PCM data between three ML7204 devices connected on the PCM interface.

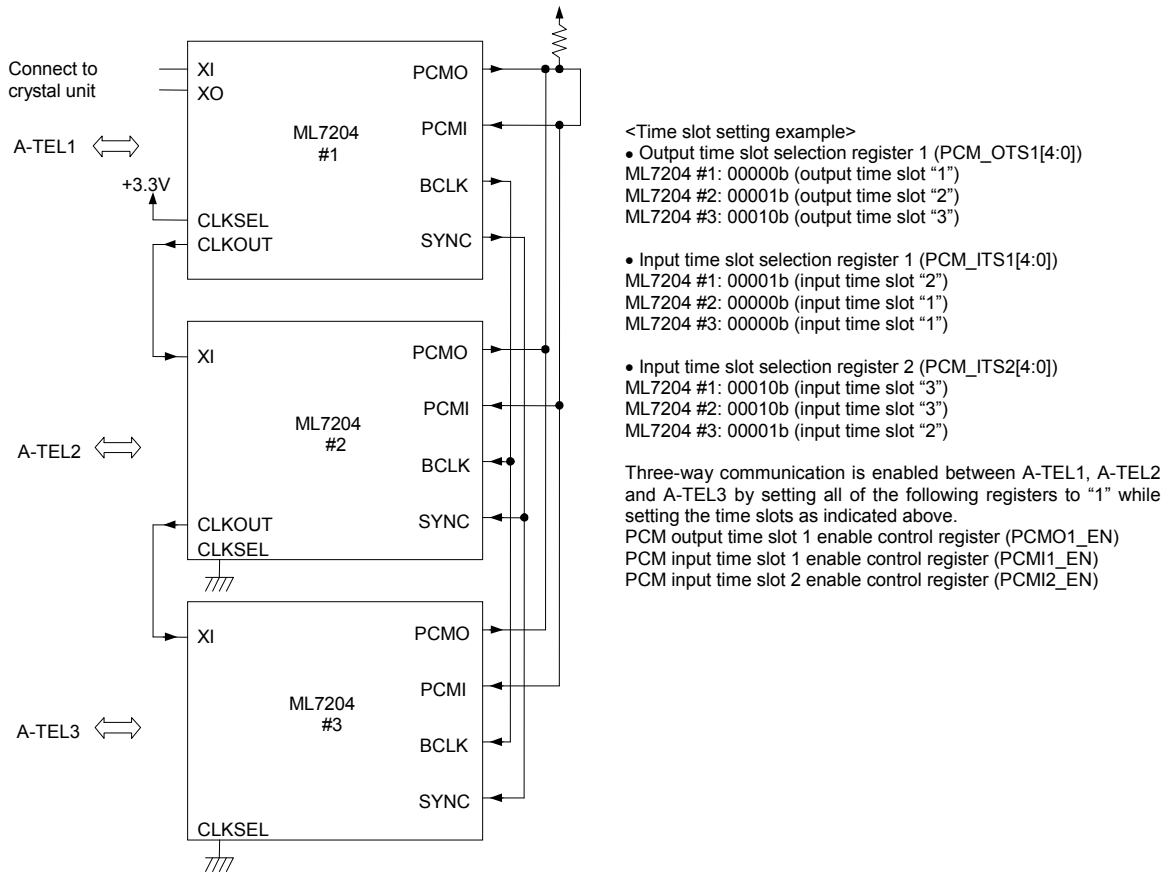


Figure 43 Example of Connection for Three-Way Communication via PCM I/F

(Note)

The maximum digital pin output load capacitance (recommended value) is 50pF. When the load connected to the PCMO pin exceeds the recommended value, insertion of a buffer external to the LSI is recommended.

Control Registers

Tables 5 shows the maps of control registers. CR6-CR9 are used for DSP internal data memory access. The changeable operation mode is indicated below each register name.

Table 5 Control Register Map (1 of 4)

Reg Name	Address A7-A0	Contents B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR0	00h	SPDN	AFEB _EN	AFEA _EN	#	#	#	SYNC _SEL	OPE _STAT	R/W
		/E	I/	I/	—	—	—	I/	I/	
CR1	01h	XDMWR	XDMRD	#	#	XDMWR _2	#	#	#	R/W
		I/E	I/E	—	—	I/E	—	—	—	
CR2	02h	TGEN0 _RXAB	TGEN0 _RX	TGEN0 _CNT5	TGEN0 _CNT4	TGEN0 _CNT3	TGEN0 _CNT2	TGEN0 _CNT1	TGEN0 _CNT0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR3	03h	TGEN1 _RXAB	TGEN1 _TX	TGEN1 _CNT5	TGEN1 _CNT4	TGEN1 _CNT3	TGEN1 _CNT2	TGEN1 _CNT1	TGEN1 _CNT0	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR4	04h	#	#	#	#	#	#	#	#	/
		—	—	—	—	—	—	—	—	
CR5	05h	READY	#	#	#	#	#	RXFLAG _CH2	RXFLAG _CH1	R/W
		—	—	—	—	—	—	I/E	I/E	
CR6	06h	Internal data memory access (high-order address/high-order data)								/W
		A15/D15	A14/D14	A13/D13	A12/D12	A11/D11	A10/D10	A9/D9	A8/D8	
		I/E								
CR7	07h	Internal data memory access (low-order access/low-order data)								/W
		A7/D7	A6/D6	A5/D5	A4/D4	A3/D3	A2/D2	A1/D1	A0/D0	
		I/E								
CR8	08h	Internal data memory access (high-order data)								R/W
		D15	D14	D13	D12	D11	D10	D9	D8	
		I/E								
CR9	09h	Internal data memory access (low-order data)								R/W
		D7	D6	D5	D4	D3	D2	D1	D0	
		I/E								
CR10	0Ah	#	#	#	#	#	VFRO1 _SEL	VFRO0 _SEL	#	R/W
		—	—	—	—	—	I/E	I/E	—	
CR11	0Bh	PCM _SEL1	PCM _SEL0	#	PCMI3 _EN	PCMO2 _EN	PCMI2 _EN	PCMI1 _EN	PCMO1 _EN	R/W
		I/	I/	—	/E	/E	/E	/E	/E	

Table 5 Control Register Map (2 of 4)

Reg Name	Address	Contents								R/W
	A7-A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR12	0Ch	$	$	$	$	$	$	$	$	/
CR13	0Dh	FD_ SEL	BW_ SEL	TXSC _SEL1	TXSC _SEL0	TXBUF _TIM	RXSC _SEL1	RXSC _SEL0	RXBUF _TIM	R/W
		I/	I/	I/E	I/E	I/	I/E	I/E	I/	
CR14	0Eh	#	#	#	#	#	#	#	MGEN_ FRFLAG	/
		—	—	—	—	—	—	—	—	
CR15	0Fh	$	$	$	$	$	$	$	$	/
CR16	10h	#	#	#	#	#	FDET _OER	FDET _FER	FDET _RQ	R/W
		—	—	—	—	—	/E	/E	/E	
CR17	11h	#	#	#	#	#	#	#	FGEN _FLAG	R/W
		—	—	—	—	—	—	—	I/E	
CR18	12h	#	#	#	#	#	#	#	TMOVF	R/W
		—	—	—	—	—	—	—	/E	
CR19	13h	DSP _ERR	#	#	TONE1_ DET	TONE0_ DET	TGEN1_ EXFLAG	TGEN0_ EXFLAG	#	R/
		—	—	—	—	—	—	—	—	
CR20	14h	INT	DP_DET	#	DTMF _DET	DTMF_ CODE3	DTMF_ CODE2	DTMF_ CODE1	DTMF_ CODE0	R/
		—	—	—	—	—	—	—	—	
CR21	15h	TX_SC FLAG	TX_BT FLAG	TXREQ _DC	TXREQ _First	TXERR _CH2	TXERR _CH1	FR0_ CH2	FR0_ CH1	R/
		—	—	—	—	—	—	—	—	
CR22	16h	RX_SC FLAG	RX_BT FLAG	RXREQ_ DC	RXREQ_ First	RXERR _CH2	RXERR _CH1	RXBW _ERR	FR1	R/
		—	—	—	—	—	—	—	—	
CR23	17h	SC_EN	DC_EN	DEC_ OUTON	ACTCH _FLAG	G711_ PLCEN	#	#	#	R/W
		I/E	I/E	/E	/E	I/E	—	—	—	
CR24	18h	#	#	#	#	#	#	PCM_ TXEN2	PCM_ RXEN2	R/W
		—	—	—	—	—	—	I/E	I/E	

Table 5 Control Register Map (3 of 4)

Reg Name	Address	Contents								R/W
	A7-A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR25	19h	FDET_D7	FDET_D6	FDET_D5	FDET_D4	FDET_D3	FDET_D2	FDET_D1	FDET_D0	R/
		-								
CR26	1Ah	DPDET_DATA7	DPDET_DATA6	DPDET_DATA5	DPDET_DATA4	DPDET_DATA3	DPDET_DATA2	DPDET_DATA1	DPDET_DATA0	R/
		—								
CR27	1Bh	FGEN_D7	FGEN_D6	FGEN_D5	FGEN_D4	FGEN_D3	FGEN_D2	FGEN_D1	FGEN_D0	R/W
		I/E								
CR28	1Ch	FDET_EN	FGEN_EN	TIM_EN	TDET1_EN	TDET0_EN	DTMF_EN	EC_EN	#	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
CR29	1Dh	#	DPGEN_EN	DPGEN_POL	DPGEN_PPS	DPGEN_DATA3	DPGEN_DATA2	DPGEN_DATA1	DPGEN_DATA0	R/W
		—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
CR30	1Eh	#	FDET_SEL	#	DTMF_SEL	TDET1_SEL1	TDET1_SEL0	TDET0_SEL1	TDET0_SEL0	R/W
		—	I/E	—	I/E	I/E	I/E	I/E	I/E	
CR31	1Fh	LPEN1	LPEN0	CODECB_TXEN	CODECB_RXEN	CODECA_TXEN	CODECA_RXEN	SC_TXEN	SC_RXEN	R/W
		I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
CR32	20h	#	#	RXGENA_EN	RXGENB_EN	PCM_TXEN1	PCM_TXEN0	PCM_RXEN1	PCM_RXEN0	R/W
		—	—	I/E	I/E	I/E	I/E	I/E	I/E	
CR33	21h	#	#	#	PCM_ITS1[4]	PCM_ITS1[3]	PCM_ITS1[2]	PCM_ITS1[1]	PCM_ITS1[0]	R/W
		—	—	—	I/E	I/E	I/E	I/E	I/E	
CR34	22h	#	#	#	PCM_ITS2[4]	PCM_ITS2[3]	PCM_ITS2[2]	PCM_ITS2[1]	PCM_ITS2[0]	R/W
		—	—	—	I/E	I/E	I/E	I/E	I/E	
CR35	23h	#	#	#	PCM_OTS1[4]	PCM_OTS1[3]	PCM_OTS1[2]	PCM_OTS1[1]	PCM_OTS1[0]	R/W
		—	—	—	I/E	I/E	I/E	I/E	I/E	
CR36	24h	#	#	#	PCM_ITS3[4]	PCM_ITS3[3]	PCM_ITS3[2]	PCM_ITS3[1]	PCM_ITS3[0]	R/W
		—	—	—	I/E	I/E	I/E	I/E	I/E	
CR37	25h	$	$	$	$	$	$	$	$	/
CR38	26h	#	#	#	PCM_OTS2[4]	PCM_OTS2[3]	PCM_OTS2[2]	PCM_OTS2[1]	PCM_OTS2[0]	R/W
		—	—	—	I/E	I/E	I/E	I/E	I/E	
CR39 to CR42	27h to 2Ah	$	$	$	$	$	$	$	$	/
CR43	2Bh	#	#	#	#	#	#	DPDET_POL	DPDET_EN	R/W
		—	—	—	—	—	—	I/	I/E	
CR44 to CR47	2Ch to 2Fh	$	$	$	$	$	$	$	$	/
—	30h to 3Fh	$	$	$	$	$	$	$	$	/

Table 5 Control Register Map (4 of 4)

Reg Name	Address	Contents								R/W
	A7-A0	B7	B6	B5	B4	B3	B2	B1	B0	
GP CR0	40h	#	GPMA [6]	GPMA [5]	GPMA [4]	GPMA [3]	GPMA [2]	GPMA [1]	GPMA [0]	R/W
		—	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GP CR1	41h	#	GPDA [6]	GPDA [5]	GPDA [4]	GPDA [3]	GPDA [2]	GPDA [1]	GPDA [0]	R/W
			I/E	I/E	I/E	I/E	I/E	I/E	I/E	
GP CR2	42h	#	GPFA [6]	GPFA [5]	GPFA [4]	#	GPFA [2]	#	GPFA [0]	R/W
		—	I/E	I/E	I/E	—	I/E	—	I/E	
GP CR3	43h	#	#	#	#	#	#	#	#	R/W
		—	—	—	—	—	—	—	—	
GP CR4	44h	#	#	#	#	#	#	#	#	R/W
		—	—	—	—	—	—	—	—	
GP CR5	45h	#	#	#	#	#	#	#	#	R/W
		—	—	—	—	—	—	—	—	
GP CR6	46h	#	#	#	#	#	#	#	#	R/W
		—	—	—	—	—	—	—	—	
GP CR7	47h	#	#	#	#	#	#	#	#	R/W
		—	—	—	—	—	—	—	—	
GP CR8	48h	#	#	#	#	#	#	#	#	R/W
		—	—	—	—	—	—	—	—	
—	49h to 7Fh	$	$	$	$	$	$	$	$	/
—	82h to FFh	$	$	$	$	$	$	$	$	/

Notation:
Register name
: Reserved bit. Do not change the initial value (“0”).
$: Access inhibit bit. Do not make R/W access to this bit.
Changeability mode
I/E : Can be changed during initial mode or operating mode
I/ : Can be changed during initial mode only
/E : Can be changed during operating mode only

R/W
R/W : Read and write processing are enabled
/W : Write only
R/ : Read only
/ : Access inhibit

(Note)
When any of the following control registers is set during operation, maintain the state for 250 μs or more since read processing is performed synchronized with the SYNC signal (8 kHz).
CR1-CR3, CR5, CR11, CR13, CR16-CR18, CR23, CR24, CR27-CR36, CR38, and CR43

See the INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD for the method of setting the following control registers.
CR6, CR7, CR8, and CR9

(1) CR0

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR0	SPDN	AFEB _EN	AFEA _EN	#	#	#	SYNC _SEL	OPE _STAT	R/W
Change enable mode	/E	I/	I/	—	—	—	I/	I/	
Initial value	0	0	0	0	0	0	0	0	

B7: Software power-down reset control register

0: Normal operating mode

1: Power-down reset

This LSI can be put into a power-down reset state by setting this bit to "1" for 200 ns or more.

At power-down reset, the contents of the control register and internal data memory are cleared automatically. Power-down reset can be released by setting "0" after setting "1".

B6: Analog front end power-down control register on the CODEC_B side

0: Normal operating state

1: Power-down state (excluding AVREF)

Power-down can be applied to the analog front end on the CODEC_B side by setting this bit to "1".

It is recommended to set this bit to "1" when the analog front end on the CODEC_B side is not used.

When setting this bit to "1", set output of VFRO1 to the AVREF side ("0") using the VFRO1 selection register (VFRO1_SEL).

B5: Analog front end power-down control register on the CODEC_A side

0: Normal operating state

1: Power-down state (excluding AVREF)

Power-down can be applied to the analog front end on the CODEC_A side by setting this bit to "1".

It is recommended to set this bit to "1" when the analog front end on the CODEC_A side is not used.

When setting this bit to "1", set output of VFRO0 to the AVREF side ("0") using the VFRO0 selection register (VFRO0_SEL).

B4-B2: Reserved bit. Change of the initial value is inhibited.

B1: SYNC frame control register

0: Long frame synchronous signal

1: Short frame synchronous signal

B0: Operation start control register

0: Operation hold

1: Operation start

After release of power-down reset, the LSI enters an initial mode. In initial mode, control register settings and internal data memory contents can be changed. Start changing the control registers or the contents of the internal memory after reading the initial mode display register (READY) continuously and detecting "1".

When this bit is set to "1" after completion of changing the control register settings or internal data memory write processing, the READY register is set to "0", returning the mode to a normal operation mode.

To change the control register settings or the contents of the internal data memory again after setting this bit to "1", change the mode to the normal operating mode. Figure 44 shows the flowchart in initial mode.

See the internal data memory change method described later for the method of changing the internal data memory.

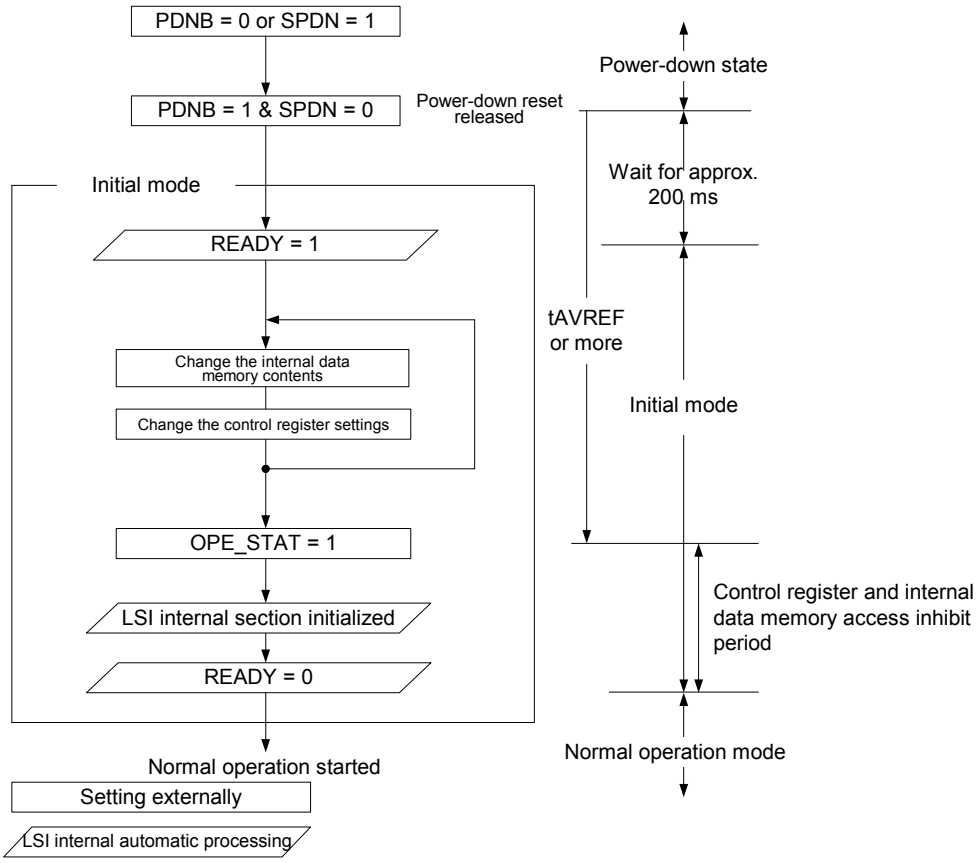


Figure 44 Flowchart in Initial Mode

(Note)
A wait period of the AVERF rise time (tAVREF) or more is required from release of power-down reset by PDNB or software power-down reset by SPDN to the setting of OPE_STAT to "1". See Figure 1 for the AVERF rise time (tAVREF).

(2) CR1

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR1	XDMWR	XDMRD	#	#	XDMWR_2	#	#	#	R/W
Change enable mode	I/E	I/E	—	—	I/E	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Internal data memory one-word write control register

0: Stops write processing

1: Writes one word

Use this register for writing one word to the address areas that are distributed in the internal data memory. Write the data that is set in CR8 and CR9 (D15 to D0) to the addresses that are set in CR6 and CR7 (A15 to A0). At termination of write processing, this bit is automatically cleared to "0". When setting data continuously, check that this bit is set to "0" before setting.

See the INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later for the details of the control method.

B6: Internal data memory read control register

0: Stops read processing

1: Reads data

Use this register for reading the internal memory data by setting the internal memory address into CR6 and CR7 (A15 to A0). The data is stored into CR8 and CR9 (D15 to D0). At termination of read processing, this bit is automatically cleared to "0". When reading data continuously, check this bit is set to "0" before reading data.

See the INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later for the details of the control method.

B5-B4: Reserved bits Change of the initial values is inhibited

B3: Internal data memory two-word write control register

0: Stops write processing

1: Writes two words

Use this register to write multiple words in continuous address areas of the internal data memory.

See the INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later for the details of the control method.

B2-B0: Reserved bits Change of the initial values is inhibited

(Note)

One-word write control, two-word write control and read control cannot be performed simultaneously for the internal data memory. Namely, Only one bit of CR1 can be set to "1" at a time.

(3) CR2

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR2	TGEN0 _RXAB	TGEN0 _RX	TGEN0 _CNT5	TGEN0 _CNT4	TGEN0 _CNT3	TGEN0 _CNT2	TGEN0 _CNT1	TGEN0 _CNT0	R/W
Change enable mode	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7: TGEN0 Output control register on the RXAB side

0: Stops output

1: Outputs tone to the RXGENA/RXGENB side

(Note)

Connection/non-connection control is enabled for output paths to RXGENA and RXGENB using the RXGENA_EN connection path control register (RXGENA_EN) and the RXGENB_EN connection path control register (RXGENB_EN). Non-connection is set as the initial value.

B6: TGEN0 Output control register on the RX side

0: Stops output

1: Outputs tone to the RXGEN side

See the various generator paths in the block diagram that is shown earlier in this document for RXGENA, RXGENB, and RXGEN.

B5: Addition and multiplication control register for TONE A/B

0: Addition (Adds output of TONE A and TONE B)

1: Multiplication (Multiplies output of TONE A and TONE B)

B4: Output control register of TONE A/B

0: Single output

Stops by outputting the signal for the time period created by adding TIM_M0 and TIM_M1.

After stopping, this register is automatically cleared within the LSI.

1: Continuous output

Outputs repeatedly the signal that is controlled by the time created by adding TIM_M0 and TIM_M1.

Set 00h to this register when stopping signal output.

(Note)

Do not set any value other than 00h since only 00h is permitted as the value that is written to this register from continuous output.

At single output, make the next setting after checking that this register is set to 00h.

When outputting signals again after termination of continuous output, wait for a period of "FADE OUT time + 250 μs" or more before starting output.

B3-B2: Output control registers of TONE A

00: Tone is not output.

01: Stops output to the M0 section and outputs tone to the M1 section.

10: Outputs tone to the M0 section and stops output to the M1 section.

11: Outputs tone to the M0 and M1 sections.

B1-B0: Output control registers of TONE B

00: Tone is not output.

01: Stops output to the M0 section and outputs tone to the M1 section.

10: Outputs tone to the M0 section and stops output to the M1 section.

11: Outputs tone to the M0 and M1 sections.

(Note)
When output control of TONE A and TONE B is set exclusively and the addition result is output, TONE A and TONE B can be output alternately. However, as each signal phase is independent, the waveform after addition is non-continuous.

(4) CR3

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR3	TGEN1 _RXAB	TGEN1 _TX	TGEN1 _CNT5	TGEN1 _CNT4	TGEN1 _CNT3	TGEN1 _CNT2	TGEN1 _CNT1	TGEN1 _CNT0	R/W
Change enable mode	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7: TGEN1 Output control register on the RXAB side

0: Stops output

1: Outputs tone to the RXGENA/RXGENB side

(Note)

Connection/non-connection control is enabled for output paths to RXGENA and RXGENB using the RXGENA_EN connection path control register (RXGENA_EN) and the RXGENB_EN connection path control register (RXGENB_EN). Non-connection is set as the initial value.

B6: TGEN1 Output control register on the TX side

0: Stops output

1: Outputs tone to the TXGEN side

See the various generator paths in the block diagram that is shown earlier in this document for RXGENA, RXGENB, and TXGEN.

B5: Addition and multiplication control register for TONE C/D

0: Addition (Adds output of TONE C and TONE D)

1: Multiplication (Multiplies output of TONE C and TONE D)

B4: Output control register of TONE C/D

0: Single output

Stops by outputting the signal for the time period created by adding TIM_M0 and TIM_M1.

After stopping, this register is automatically cleared within the LSI.

1: Continuous output

Outputs repeatedly the signal that is controlled by the time created by adding TIM_M0 and TIM_M1.

Set 00h to this register when stopping signal output.

(Note)

Do not set any value other than 00h since only 00h is permitted as the value that is written to this register from continuous output.

At single output, make the next setting after checking that this register is set to 00h.

When outputting signals again after termination of continuous output, wait for a period of "FADE OUT time + 250 μs" or more before starting output.

B3-B2: Output control registers of TONE C

00: Tone is not output.

01: Stops output to the M0 section and outputs tone to the M1 section.

10: Outputs tone to the M0 section and stops output to the M1 section.

11: Outputs tone to the M0 and M1 sections.

B1-B0: Output control registers of TONE D

00: Tone is not output.

01: Stops output to the M0 section and outputs tone to the M1 section.

10: Outputs tone to the M0 section and stops output to the M1 section.

11: Outputs tone to the M0 and M1 sections.

(Note)
When output control of TONE C and TONE D is set exclusively and the addition result is output, TONE C and TONE D can be output alternately. However, as each signal phase is independent, the waveform after addition is non-continuous.

Figure 45 shows the block diagram of the tone generation sections (TONE_GEN0 and TONE_GEN1).
Since the same tone generation method is applied by TONE_GEN0 and TONE_GEN1, TONE_GEN0 is used as the examples for the tone output control method in Figure 46 and tone output control parameters in Figures 47 and 48.

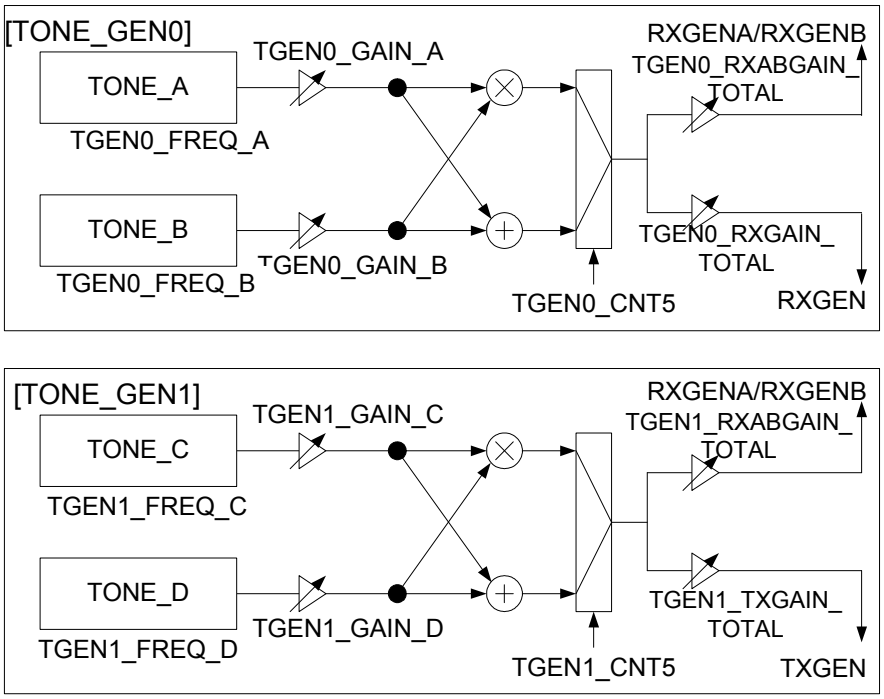
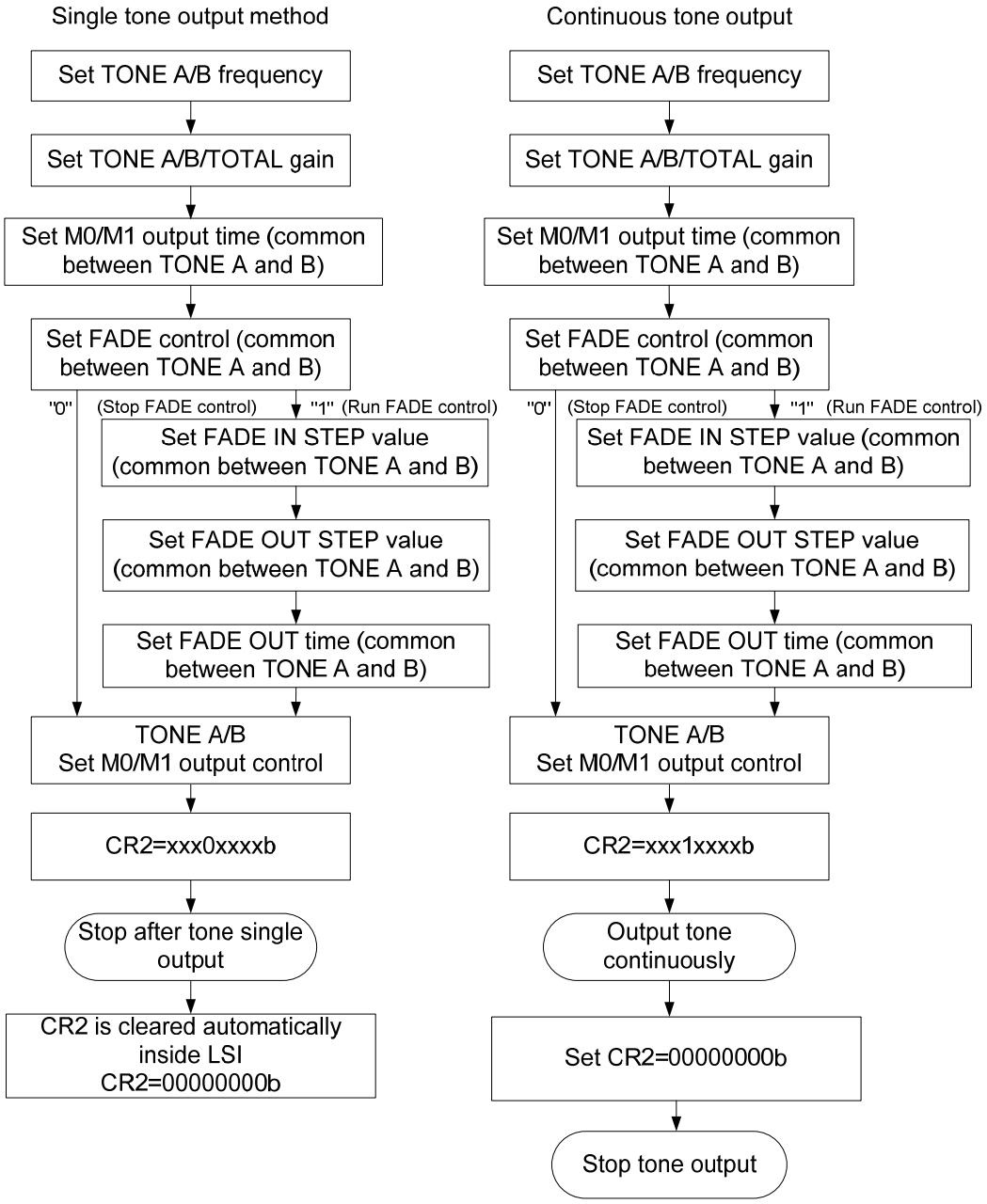


Figure 45 Block Diagram of Tone Generation Sections



Note: When setting output again after stopping output, wait for a period of " FADE OUT time + 250µs" or more before starting output.

Figure 46 Tone Output Control Method (TONE_GEN0)

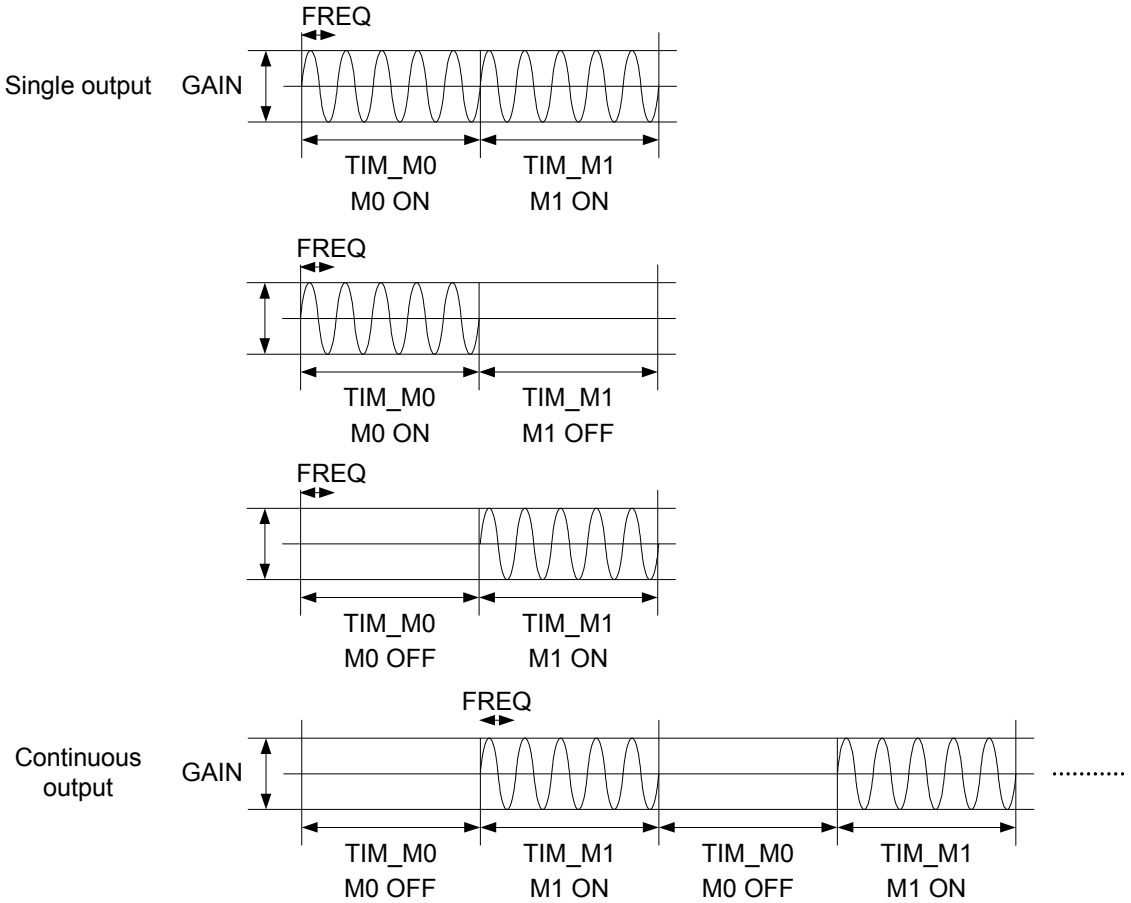


Figure 47 Tone Output Control Parameters (TONE_GEN0/TGEN0_FADE_CONT OFF)

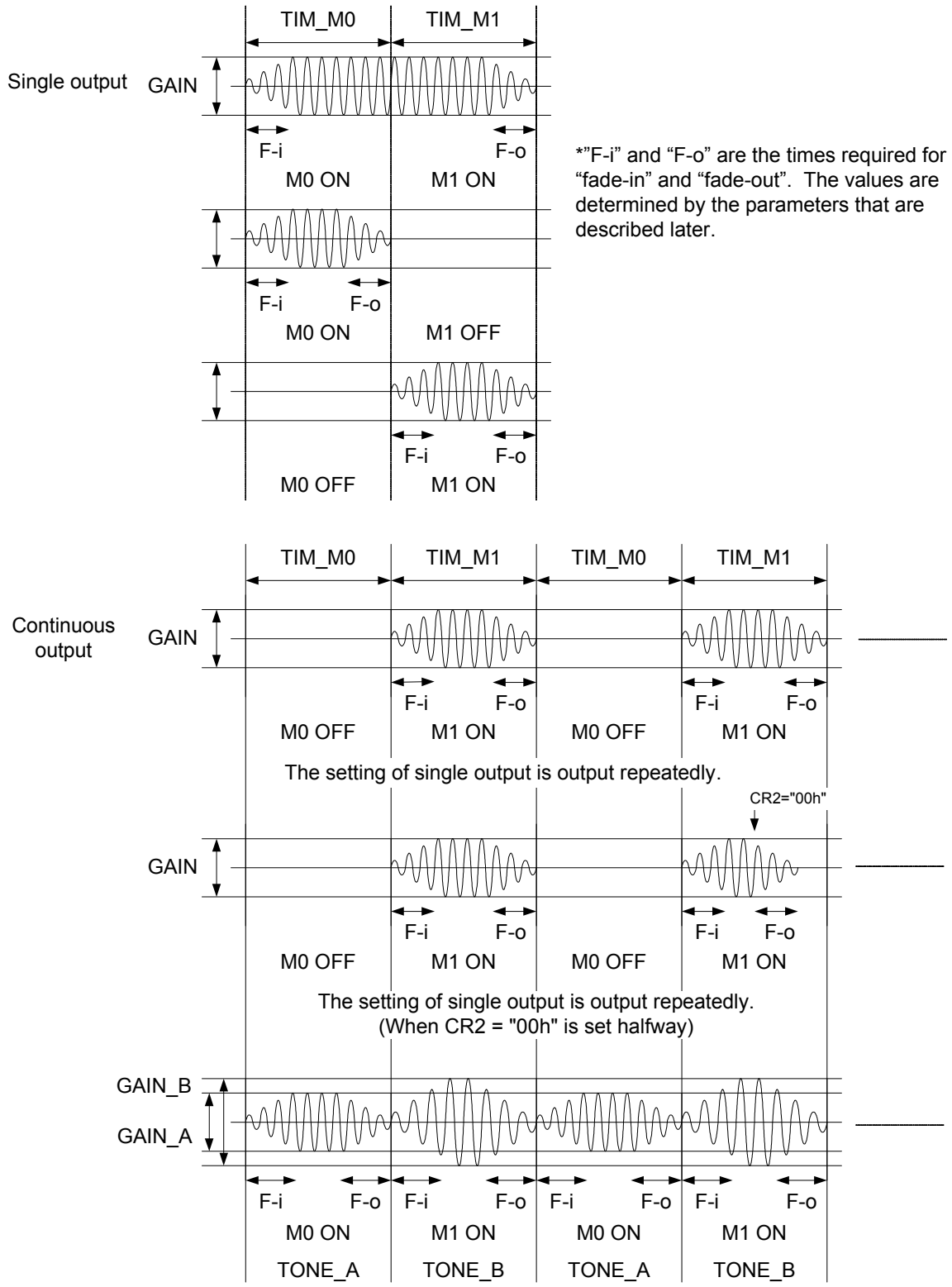


Figure 48 Tone Output Control Parameters (TONE_GEN0/TGEN0_FADE_CONT ON)

(5) CR4

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR4	#	#	#	#	#	#	#	#	/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7-B0: Reserved bits Change of the initial values is inhibited.

(6) CR5

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR5	READY	#	#	#	#	#	RXFLAG _CH2	RXFLAG _CH1	R/W
Change enable mode	—	—	—	—	—	—	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7: Initial mode display register

0: Mode other than initial mode

1: Initial mode

After release of power-down reset, this LSI enters an initial mode. In initial mode, this bit is set to "1".

B6-B1: Reserved bits Change of the initial values is inhibited.

B1-B0: Receive data write channel notification register

A receive request is issued twice in one frame during 2-channel receive request processing (RXREQ_DC=1).

Write receive data of channel 1 or channel 2 for each receive request.

Since data can be written in any sequence, notify this LSI of the channel of the receive data by setting RXFLAG_[CH2:CH1] to the following before writing receive data.

RXFLAG_[CH2:CH1] = [1:0] : Channel 2 receive data write notification

RXFLAG_[CH2:CH1] = [0:1] : Channel 1 receive data write notification

See Figures 32 to 35 for the detailed control methods.

(7) CR6

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR6	A15/D15	A14/D14	A13/D13	A12/D12	A11/D11	A10/D10	A9/D9	A8/D8	/W
Change enable mode	I/E								
Initial value	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	

B7-B0: Internal data memory high-order address/high-order data setting register

This is an internal data memory high-order address/high-order data setting register.

See the section of INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD for the write method.

(Note)*

Although the initial value of CR6 is 00h, it is set to 72h automatically before the initial mode starts.

(8) CR7

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR7	A7/D7	A6/D6	A5/D5	A4/D4	A3/D3	A2/D2	A1/D1	A0/D0	/W
Change enable mode	I/E								
Initial value	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	

B7-B0: Internal data memory low-order address/low-order data setting register

This is an internal data memory low-order address/low-order data setting register.
See the section of INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD for the write method.

(Note)*
Although the initial value of CR7 is 00h, it is set to 04h automatically before the initial mode starts.
At the start of initial mode, the LSI type (ML7204) can be checked by reading the values of CR6 and CR7.

(9) CR8

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR8	D15	D14	D13	D12	D11	D10	D9	D8	R/W
Change enable mode	I/E								
Initial value	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	

B7-B0: Internal data memory high-order data setting register

This is an internal data memory high-order data setting register.
See the section of INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD for the write and read method.

(Note)*
Although the initial value of CR8 is 00h, it is set to 01h automatically before the initial mode starts.

(10) CR9

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR9	D7	D6	D5	D4	D3	D2	D1	D0	R/W
Change enable mode	I/E								
Initial value	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	0 (*)	

B7-B0: Internal data memory low-order data setting register

This is an internal data memory low-order data setting register.
See the section of INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD for the write and read method.

(Note)*
Although the initial value of CR9 is 00h, it is set to 03h automatically before the initial mode starts. At the start of initial mode, the code type (-003) can be checked by reading the value of CR9.

(11) CR10

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR10	#	#	#	#	#	VFRO1 _SEL	VFRO0 _SEL	#	R/W
Change enable mode	—	—	—	—	—	I/E	I/E	—	
Initial value	0	0	0	0	0	0	0	0	

B7-B3: Reserved bits Change of the initial values is inhibited.

B2: VFRO1 selection register
0: AVREF (outputs about 1.4 V)
1: Voice output on the receive side

B1: VFRO0 selection register
0: AVREF (outputs about 1.4 V)
1: Voice output on the receive side

B0: Reserved bits Change of the initial values is inhibited.

(12) CR11

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR11	PCM _SEL1	PCM _SEL0	#	PCMI3 _EN	PCMO2 _EN	PCMI2 _EN	PCMI1 _EN	PCMO1 _EN	R/W
Change enable mode	I/	I/	—	/E	/E	/E	/E	/E	
Initial value	0	0	0	0	0	0	0	0	

B7 and B6: PCM I/F coding format selection control register

These are PCM I/F coding format selection bits.

(0 , 0): 16-bit linear (two's complement format)

(0 , 1): G.711(μ-law)

(1 , 0): Inhibited

(1 , 1): G.711(A-law)

(Note) When G.711 (A-law) is selected by setting the PCM I/F coding format selection control register (PCM_SEL[1:0]) to (1,1), decrease your target gain setting of a very next gain control following G.711 decoder such as RXGAIN_ITS1 by 18.6dB, and increase your target gain setting of the following gain control such as RXGAIN_PCM0 by 18.6dB.
Examples in a case where the PCM input time slot 1 enable control register (PCMI1_EN)="1" and the VFRO0-pin is assigned as an LSI output pin for PCMI-pin input signals are shown in a table below.
When a tone detector (TONE_DET0 and/or TONE_DET1) located between the concerned two gain controls is enabled, adjust the detection level accordingly.

Gain Control	Your Target (example)	Recommendation	Remarks
RXGAIN_ITS1	0008h (0dB)	000Fh (-18.6dB)	
RXGAIN_PCM0	0039h (-7.03dB)	01E6h (+11.60dB)	
	001Ah (-13.8dB)	00DEh (+4.78dB)	
	000Bh (-21.3dB)	005Eh (-2.69dB)	

B5: Reserved bits Change of the initial values is inhibited.

B4: PCM input time slot selection 3 enable control register

0: Stops PCM input time slot selection 3

1: Activates PCM input time slot selection 3

When this bit is set to "1", the PCM data in the time slot position that has been set in the PCM input time slot selection register 3 (PCM_ITS3[4:0]) is fetched and decoding processing is performed with the coding format selected in the PCM I/F coding format selection control register (PCM_SEL[1:0]). PCM data fetching starts from the frame following the frame where this bit has been detected having been set to "1". Figure 50 shows the PCM input timing.

(Note) When G.711 (A-law) is selected by setting the PCM I/F coding format selection control register (PCM_SEL[1:0]) to (1,1), it's recommended to set this PCM input time slot 3 enable control register (PCMI3_EN) to "0" (Stops PCM input time slot selection 3).

B3: PCM output time slot selection 2 enable control register

0: Stops PCM output time slot selection 2

1: Activates PCM output time slot selection 2

When this bit is set to "1", the PCM data that was encoded with the coding format selected by the PCM I/F coding format selection control register (PCM_SEL[1:0]) is output to the time slot position that has been set in the PCM output time slot selection register 2 (PCM_OTS2[4:0]). PCM data encoding starts from the frame following the frame where this bit has been detected having been set to "1". Figure 51 shows the PCM output timing.

B2: PCM input time slot selection 2 enable control register

0: Stops PCM input time slot selection 2

1: Activates PCM input time slot selection 2

When this bit is set to "1", the PCM data in the time slot position that has been set in the PCM input time slot selection register 2 (PCM_ITS2[4:0]) is fetched and decoding processing is performed with the coding format selected in the PCM I/F coding format selection control register (PCM_SEL[1:0]). PCM data fetching starts from the frame following the frame where this bit has been detected having been set to "1". Figure 50 shows the PCM input timing.

B1: PCM input time slot selection 1 enable control register

0: Stops PCM input time slot selection 1

1: Activates PCM input time slot selection 1

When this bit is set to "1", the PCM data in the time slot position that has been set in the PCM input time slot selection register 1 (PCM_ITS1[4:0]) is fetched and decoding processing is performed with the coding format selected in the PCM I/F coding format selection control register (PCM_SEL[1:0]). PCM data fetching starts from the frame following the frame where this bit has been detected having been set to "1". Figure 50 shows the PCM input timing.

When both of B2 and B1 are set to "1", each decoding result is added and output on the speech path.

B0: PCM output time slot selection 1 enable control register

0: Stops PCM output time slot selection 1

1: Activates PCM output time slot selection 1

When this bit is set to "1", the PCM data that was encoded with the coding format selected by the PCM I/F coding format selection control register (PCM_SEL[1:0]) is output to the time slot position that has been set in the PCM output time slot selection register 1 (PCM_OTS1[4:0]). PCM data encoding starts from the frame following the frame where this bit has been detected having been set to "1". Figure 51 shows the PCM output timing.

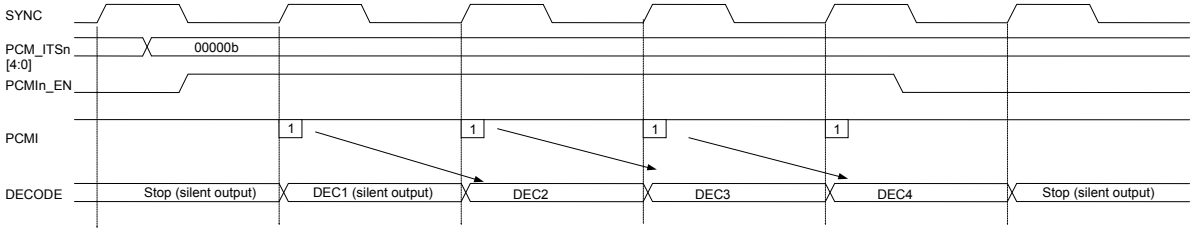
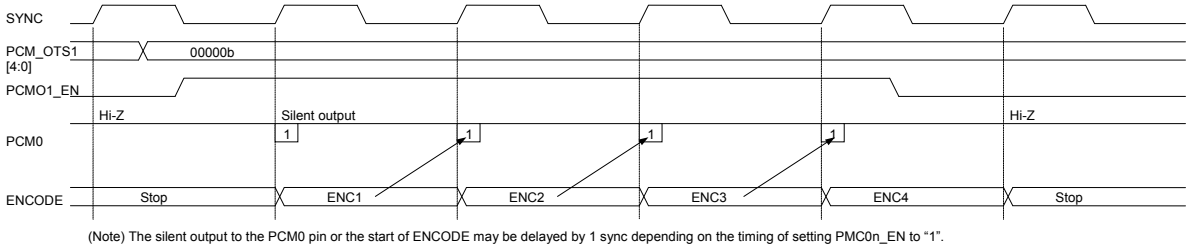


Figure 50 PCM Input Timing



(Note) The silent output to the PCM0 pin or the start of ENCODE may be delayed by 1 sync depending on the timing of setting PMC0n_EN to "1".

Figure 51 PCM Output Timing

(Note)
The frame following the frame where PCMO1_EN or PCMO2_EN has been detected having been set to "1" outputs the following silent data according to the coding format selected in PCM_SEL[1:0].

16-bit linear (two's complement format)	: 0000h
G.711(μ-law)	: FFh
G.711(A-law)	: D5h

(13) CR12

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR12	$	$	$	$	$	$	$	$	/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7-B0: Reserved bits Access is inhibited.

(14) CR13

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR13	FD_ SEL	BW_ SEL	TXSC _SEL1	TXSC _SEL0	TXBUF _TIM	RXSC _SEL1	RXSC _SEL0	RXBUF _TIM	R/W
Change enable mode	I/	I/	I/E	I/E	I/	I/E	I/E	I/	
Initial value	0	0	0	0	0	0	0	0	

B7: FRAME/DMA selection register
0: FRAME access
1: DMA slave interface access
Select a transmit buffer or a receive buffer access method. Frame access is set as the initial value.

B6: MCU interface data width selection register
0: 16-bit data width interface
1: 8-bit data width interface
Select a data path width to a transmit buffer or a receive buffer. The initial value is 16 bits.
When selecting a 8-bit data width, fix D15 to D18 to “1” or “0”.

B5-B4: Speech CODEC selection register on the transmit side
(0 , 0): G.729.A
(0 , 1): G.711 (μ-law)
(1 , 0): Inhibited
(1 , 1): G.711 (A-law)

B3: Transmit buffering time selection register
0: 10 ms
1: 20 ms
Select a buffering time of a transmit buffer. The initial value is 10 ms.

B2-B1: Speech CODEC selection register on the receive side
(0 , 0): G.729.A
(0 , 1): G.711 (μ-law)
(1 , 0): Inhibited
(1 , 1): G.711 (A-law)

(Note) When G.711 (A-law) is selected by setting the PCM I/F coding format selection control register (PCM_SEL[1:0]) to (1,1), decrease your target gain setting of a very next gain control following G.711 decoder such as RXGAIN_ITS1 by 18.6dB, and increase your target gain setting of the following gain control such as RXGAIN_PCM0 by 18.6dB.
Examples in a case where the PCM input time slot 1 enable control register (PCMI1_EN)=”1” and the VFRO0-pin is assigned as an LSI output pin for PCMI-pin input signals are shown in a table below.
When a tone detector (TONE_DET0 and/or TONE_DET1) located between the concerned two gain controls is enabled, adjust the detection level accordingly.

Gain Control	Your Target (example)	Recommendation	Remarks
RXGAIN_ITS1	0008h (0dB)	000Fh (-18.6dB)	
RXGAIN_PCM0	0039h (-7.03dB)	01E6h (+11.60dB)	
	001Ah (-13.8dB)	00DEh (+4.78dB)	
	000Bh (-21.3dB)	005Eh (-2.69dB)	

B0: Receive buffering time selection register
0: 10 ms
1: 20 ms
Select a buffering time of a receive buffer. The initial value is 10 ms.

(15) CR14

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR14	#	#	#	#	#	#	#	#	/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7-B0: Reserved bits Change of the initial values is inhibited.

(16) CR15

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR15	$	$	$	$	$	$	$	$	/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7-B0: Reserved bits Access is inhibited.

(17) CR16

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR16	#	#	#	#	#	FDET _OER	FDET _FER	FDET _RQ	R/W
Change enable mode	—	—	—	—	—	/E	/E	/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B3: Reserved bits Change of the initial values is inhibited.

B2: FSK receive overrun error notification register

0: No overrun error occurred

1: Overrun error occurred

When an overrun error occurred during FSK data receive processing, this bit is also set to "1"at the next read request (FDET_RQ=1). When FDET_RQ is cleared, make sure this bit is also cleared by writing "0" to this bit.

B1: FSK receive framing error notification register

0: No framing error occurred

1: Framing error occurred

When SP (Stop Bit "1") is not detected normally at reception of FSK data, this bit is also set to "1" when the reading of the relevant data is requested(FDET_RQ=1). When FDET_RQ is cleared, make sure that this bit is also cleared by writing "0" to this bit.

B0: FSK receive data read request notification register

0: No read request issued

1: Read request issued

When receiving FSK data (10 bits), the LSI stores the data bits (8 bits) excluding ST (Start Bit "0") and SP (Stop Bit "1") in FDET_D[7:0] and sets this bit to "1". After completion of receive data read processing, clear this bit by writing "0" to this bit.

For details of the control method relating to FSK_DET, see the section of the FSK receiver (FSK_DET) of the internal data memory access and control method that are described later.

When the setting of the bits B2-B0 is changed ("0" → "1"), an INTB interrupt occurs.

(18) CR17

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR17	#	#	#	#	#	#	#	FGEN _FLAG	R/W
Change enable mode	—	—	—	—	—	—	—	/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B1: Reserved bits Change of the initial values is inhibited.

B0: FSK output data setting completion flag

Set this bit to "1" after writing data to the FSK output data setting register (FGEN_D[7:0]). This bit is cleared to "0" automatically at completion of the fetching of data to the internal buffer of the FSK signal generation section and an interrupt occurs. Do not write any data to this register while this bit is "1".
For details, see the section of the FSK generator of the internal data memory access and control method that are described later.

When the setting of the B0 bit is changed ("1" → "0"), an INTB interrupt occurs.

(19) CR18

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR18	#	#	#	#	#	#	#	TMOVF	R/W
Change enable mode	—	—	—	—	—	—	—	/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B1: Reserved bits Change of the initial values is inhibited.

B0: Timer overflow display register

0: No timer overflow occurred.
1: Timer overflow occurred.

When the timer counter value and the data setting value match and consequently a timer overflow occurs, the timer overflow display register (TMOVF) is set to "1" and an INTB interrupt occurs.
The timer overflow interrupt is cleared to "0" when the timer is stopped as a result of writing "0" to TMOVF from the MCU side or writing "0" to the timer control register (TIM_EN).

When the setting of the B0 bit is changed ("0" → "1"), an INTB interrupt occurs.

(20) CR19

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR19	DSP _ERR	#	#	TONE1_ DET	TONE0_ DET	TGEN1_ EXFLAG	TGEN0_ EXFLAG	#	R/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: DSP status register

0: Normal operating status

1: Abnormal operating status

This LSI is equipped with a built-in watchdog timer. When a DSP program loses control due to a disturbance surrounding this LSI or power supply abnormality, the DSP status register (DSP_ERR) is set to "1" and an interrupt occurs. When this bit is set to "1", set power-down reset by using PDNB or the software power-down reset control register (SPDN). This bit is cleared by setting power-down reset.

(Note)

The DSP status register (DSP_ERR) does not detect all the abnormal operations. The register cannot detect the abnormal operating status that causes the clearing of the watchdog timer even if DSP loses control.

B6-B5: Reserved bits Change of the initial values is inhibited.

B4: TONE1 detecter detection status register

0: Non-detection

1: Detection

B3: TONE0 detecter detection status register

0: Non-detection

1: Detection

For details of TDET0 and TDET1, see the sections of tone detecter 0 and tone detecter 1 of the internal data memory access and the control method that are described later.

B2: TGEN1 execution status flag display register

0: Inactive

1: Active

B1: TGEN0 execution status flag display register

0: Inactive

1: Active

For details of TGEN0_EXFLAG/TGEN1_EXFLAG, see the sections of tone generater 0/tone generator 1 of the internal data memory access and the control method that are described later.

B0: Reserved bit Change of the initial value is inhibited.

When the setting of the B7 bit is changed ("0" → "1") or the setting of the bits B4-B1 is changed ("0" → "1" or "1" → "0"), an INTB interrupt occurs.

(21) CR20

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR20	INT	DP_DET	#	DTMF_DET	DTMF_CODE3	DTMF_CODE2	DTMF_CODE1	DTMF_CODE0	R/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Interrupt occurrence status register

This is a direct connection register with inverted INTB logic.
When INTB is “L”, “1” is read. In other cases, “0” is read.

0: Section where INTB is “H”
1: Section where INTB is “L”

(Note)
When DSP_ERR occurs, the INT register and the status of INTB may not match.

B6: Dial pulse detector detection status register

The bit is set to “1” in the section from which a dial pulse signal is detected. The bit is set to “0” in other cases.

0: No dial pulse detected
1: Dial pulse detected.

B5: Reserved bits Change of the initial values is inhibited.

B4: DTMF detector detection status register

This bit is set to “1” in the section from which a DTMF signal is detected. The bit is set to “0” in other cases.

0: Non-detection
1: Detection

B3-B0: DTMF code display register

When the DTMF detector control register (DTMF_EN) is set to “1”, a valid code is stored in this register for the time period in which a DTMF signal is being detected (DTMF detector detection status register DTMF_DET = “1”).
When the DTMF signal is not detected (DTMF_DET = “0”), “0000” is output.
Table 6 lists the codes.

When the setting of B6 or B4-B0 is changed (“0” → “1” or “1” → “0”), an INTB interrupt occurs.

Table 6 DTMF Detection Codes

DTMF_3	DTMF_2	DTMF_1	DTMF_0	Low group [Hz]	High group [Hz]	Dial number
0	0	0	0	697	1209	1
0	0	0	1	770	1209	4
0	0	1	0	852	1209	7
0	0	1	1	941	1209	*
0	1	0	0	697	1336	2
0	1	0	1	770	1336	5
0	1	1	0	852	1336	8
0	1	1	1	941	1336	0
1	0	0	0	697	1477	3
1	0	0	1	770	1477	6
1	0	1	0	852	1477	9
1	0	1	1	941	1477	#
1	1	0	0	697	1633	A
1	1	0	1	770	1633	B
1	1	1	0	852	1633	C
1	1	1	1	941	1633	D

(22) CR21

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR21	TX_SC FLAG	TX_BT FLAG	TXREQ _DC	TXREQ _First	TXERR _CH2	TXERR _CH1	FR0_ CH2	FR0_ CH1	R/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Transmit side Speech CODEC operating mode notification flag

0: G.729.A

1: G.711 (μ-law/A-law)

The operating mode of Speech CODEC on the transmit side can be checked by referencing this bit at switching of the Speech CODEC coding format on the transmit side. If this bit is "0" when a transmit request is issued due to the fall of FR0B, it indicates that the transmit data has been encoded in the G.729.A coding format. If this bit is set to "1" when transmission is requested due to the fall of FR0B, it indicates that the transmit data has been encoded in the G.711 coding format (μ-law/A-law).

See Figures 22 to 25 for Speech CODEC coding format switching control on the transmit side.

B6: Transmit side buffering time operating mode notification flag

0: 10 ms

1: 20 ms

By referencing this bit, the operating mode of the transmit side buffering time can be checked. If this bit is set to "0" when transmission is requested due to the fall of FR0B, encoded data of 10 ms is buffered. If this bit is set to "1" when transmission is requested, encoded data of 20 ms is buffered in the transmit buffer.

B5: 2-channel transmit request notification register

0: Not in cases where 2-channel transmission is being requested

1: 2-channel transmission is being requested

Transmission is requested twice within one frame while 2-channel transmission is being requested (TXREQ_DC = 1).

Read transmit data of channel 1 in response to CH1 transmit request (FR0_CH1 = 1) and read transmit data of channel 2 in response to CH2 transmit request (FR0_CH2).

B4: Transmit frame start notification register

Transmission is requested twice within one frame while 2-channel transmission is being requested (TXREQ_DC = 1). This bit enables the checking of the start timing of each transmit frame.

While 2-channel transmit is being requested (TXREQ_DC = 1), this bit is set to "1" immediately before CH1 transmit request (FR0_CH1 = 1) and the bit is cleared to "0" immediately before CH2 transmit request (FR0_CH2 = 1).

See the transmit/receive buffer control method at 2-channel processing in Figures 32 to 35.

B3: CH2 transmit error status register

0: No CH2 transmit error occurred

1: CH2 transmit error occurred

This bit is set to "1" when the CH2 transmit data read processing is not completed within the valid read period and in other cases, the bit is set to "0".

B2: CH1 transmit error status register

0: No CH1 transmit error occurred

1: CH1 transmit error occurred

When read processing of CH1 transmit data is not completed within the valid read period, this bit is set to "1" and in other cases, the bit is set to "0".

B1: CH2 transmit request notification register
0: No CH2 transmit request generated
1: CH2 transmit request generated
When the transmit buffer storing the CH2 transmit data becomes full, this bit is set to "1" and the bit is set to "0" at completion of reading of the data from the transmit buffer or the processing time exceeded the specified time.

B0: CH1 transmit request notification register
0: No CH1 transmit request generated
1: CH1 transmit request generated
When the transmit buffer storing CH1 transmit data becomes full, this bit is set to "1" and the bit is set to "0" at completion of reading of the data from the transmit buffer or the processing time exceeded the specified time.

In frame mode (FD_SEL = 0), the signal obtained by NORing bit B1 with bit B0 is output to the FR0B pin. (*)

(Note)*
In DMA mode (FD_SEL = 1), the bit B1, bit B0, and FR0B (DMARQ0B) pin statuses do not match.

When the setting of the bits B3-B2 ("0" → "1" or "1" → "0") or bits B1-B0 ("0" → "1") changes, an INTB interrupt occurs.

(23) CR22

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR22	RX_SC FLAG	RX_BT FLAG	RXREQ _DC	RXREQ _First	RXERR _CH2	RXERR _CH1	RXBW _ERR	FR1	R/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Receive side Speech CODEC operating mode notification flag

0: G.729.A

1: G.711 (μ-law/A-law)

The operating mode of Speech CODEC on the receive side can be checked by referencing this bit at switching of the Speech CODEC coding format on the receive side. If this bit is set to "0" when a receive request is issued due to the fall of FR1B, it indicates that receive data in the G.729.A coding format is being requested. If this bit is set to "1" when a receive request is issued due to the fall of FR1B, it indicates that receive data in the G.711 coding format (μ-law/A-law) is being requested.
See Figures 26 to 29 for Speech CODEC coding format switching control on the receive side.

B6: Receive side buffering time operating mode notification flag

0: 10 ms

1: 20 ms

The buffering time operating mode on the receive side can be checked by referencing this bit. If this bit is set to "0" when a receive request is issued due the fall of FR1B, it indicates that the receive buffer is requesting the writing of data of 10 ms. If this bit is set to "1" when a receive request is issued due the fall of FR1B, it indicates that the receive buffer is requesting the writing of data of 20 ms.

B5: 2-channel receive request notification register

0: Not in cases where 2-channel reception is being requested

1: 2-channel reception is being requested

While 2-channel reception is being requested (RXREQ_DC = 1), a receive request is issued twice within one frame.
Write receive data of channel 1 or channel 2 for each receive request (FR1 = 1).

B4: Receive frame start notification register

While 2-channel reception is being requested (RXREQ_DC = 1), a receive request is issued twice within one frame. Use this bit to check if the request is the first receive request.
If this bit is set to "1" when a receive request is generated (FR1 = 1), the request is the first request and if the bit is set to "0", the request is the second receive request. See also the transmit/receive buffer control method at 2-channel processing in Figures 32 to 35.

B3: CH2 receive error status register

0: No CH2 receive error occurred

1: CH2 receive error occurred

This bit is set to "1" when CH2 receive data write processing is not completed within the valid write period and set to "0" in other cases.

B2: CH1 receive error status register

0: No CH1 receive error occurred

1: CH1 receive error occurred

This bit is set to "1" when CH1 receive data write processing is not completed within the valid write period and set to "0" in other cases.

B1: Invalid receive data write error notification register

0: No invalid receive data write generated

1: Invalid receive data write generated

This bit is set to "1" if receive data channel notification is issued from the MCU side without observing the following prohibition while 2-chanel reception is being requested (RXREQ_DC = 1). In other cases, the bit is set to "0".

◆ Prohibition 1: Do not write receive data of the same channel in the same frame consecutively.
If receive data of the same channel of the same frame is written consecutively, RXBW_ERR is set to "1". In this case, the data that is written in response to the first receive request (FR1 = 1 & RXREQ_First = 1) is decoded, but the data that is written in response to the second receive request (FR1 = 1 & RXREQ_First = 0) is discarded.

◆ Prohibition 2: Do not set RXFLAG_[CH2:CH1] = [1:1] or [0:0].
If RXFLAG_[CH2:CH1] is set to [1:1] or [0:0], the receive data is discarded and RXBW_ERR is set to "1".

B0: Receive request notification register

0: No receive request issued

1: Receive request issued

This bit is set to "1" when the receive buffer that stores receive data becomes empty. When the receive buffer becomes full or the processing exceeds the specified time, the bit is set to "0".
In frame mode (FD_SEL = 0), the signal generated by inverting the logic of bit B0 is output to the FR1B pin. (*)

(Note)*
In DMA mode (FD_SEL = 1), bit B0 and the FR1B (DMARQ1B) pin statuses do not match.

When the status of bits B3-B1 is changed ("0" → "1" or "1" → "0") or that of bit B0 changed("0" → "1") , an INTB interrupt occurs.

Table 7 lists the transmit/receive buffer control registers.
Note that the register that is referenced or set on the MCU side varies depending on the operating mode (1-channel operation/2-channel operation) of Speech CODEC.

Table 7 Transmit/Receive Buffer Control Registers

	CR	Bit	Register name (abbreviation)	Single-channel operation	2-channel operation
				SC_EN=1,DC_EN=0	SC_EN=1,DC_EN=1
Transmit control	CR21	B0	CH1 transmit request notification register (FR0_CH1)	○	○
		B1	CH2 transmit request notification register (FR0_CH2)	×	○
		B2	CH1 transmit error status register (TXERR_CH1)	○	○
		B3	CH2 transmit error status register (TXERR_CH2)	×	○
		B4	Transmit frame start notification register (TXREQ_First)	×	○
		B5	2-channel transmit request notification register (TXREQ_DC)	×	○
		B6	Transmit side buffering time operating mode notification flag (TX_BTFLAG)	○	○
		B7	Transmit side Speech CODEC operating mode notification flag (TX_SCFLAG)	○	○
Receive control	CR22	B0	Receive request notification register (FR1)	○	○
		B1	Invalid receive data write error notification register (RXBW_ERR)	×	○
		B2	CH1 receive error status register (RXERR_CH1)	○	○
		B3	CH2 receive error status register (RXERR_CH2)	×	○
		B4	Receive frame start notification register (RXREQ_First)	×	○
		B5	2-channel receive request notification register (RXREQ_DC)	×	○
		B6	Receive side buffering time operating mode notification flag (RX_BTFLAG)	○	○
		B7	Receive side Speech CODEC operating mode notification flag (RX_SCFLAG)	○	○
	CR5	B1-B0	Receive data write channel notification register RXFLAG_[CH2:CH1]	×	○

(Remarks) ○: Used, ×: Unused

(24) CR23

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR23	SC_EN	DC_EN	DEC_ OUTON	ACTCH _FLAG	G711_ PLCEN	#	#	#	R/W
Change enable mode	I/E	I/E	/E	/E	I/E	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Speech CODEC control register

0: Stops Speech CODEC

The encoder stops and storing data into the transmit buffer is stopped. The decoder stops and outputs silent data constantly.

1: Activates Speech CODEC

Setting this bit to "1" starts the Speech CODEC operation. Speech CODEC is initialized and starts operation.

(Note)
When stopping Speech CODEC
When stopping Speech CODEC, be sure to make the following settings in advance:
- Writing 00FFh to CR21 rising edge interrupt mask control (CR21_INTR_MSKCNT)
- Writing 00FFh to CR22 rising edge interrupt mask control (CR22_INTR_MSKCNT)

B6: Speech CODEC 2-channel processing control register

0: Stops Speech CODEC 2-channel processing.

1: Activates Speech CODEC 2-channel processing.

B5: Decoded data output control register

This bit controls the first decoded data output timing after activation of Speech CODEC.
After activation of Speech CODEC, this bit can be set to "1" if the initial receive data has been written and the tWAIT time has elapsed. When this bit is set to "1", the following decoded data is output in the selected Speech CODEC coding format.

- When G.711 (μ-law/A-law) is selected:
  When the PLC function is enabled, silent data is output for about 3.75 ms and decoded data is output after this bit is set to "1".
  When the PLC function is disabled, decoded data is output after this bit is set to "1".
- When G.729.A is selected:
  Decoded data is output about 15 ms after this bit is set to "1".

The decoded data output delay time can be increased in steps of 0.125 ms by setting the time in the internal data memory (DEC_ONTIM) for controlling decoded data output starting offset time.
(Allowable DEC_ONTM setting range: 0.125 ms to 32 ms)
Clear this bit to "0" when stopping Speech CODEC by setting SC_EN to "0".
See the diagrams of receive buffer control timing in Figures 18 to 21 for details of the control method.

(Note) The tWAIT delay time of 1 ms or more is required after activation of Speech CODEC.

(Note)
It is also possible to set DEC_OUTON to "1" at the same time as setting SC_EN to "1". If soing so, however, set the offset time to a value between 0008h (1 ms) and 0100h (32 ms) in the internal data memory for controlling decoded output starting offset time (DEC_ONTIM) in advance.
Output of decoded data will start when the writing of the first receive data after the activation of Speech CODEC is completed and when the above offset time elapses.

B4: Operation channel notification register

0: Continues encoding and decoding for CH1

1: Continues encoding and decoding for CH2

When changing the mode from 2-channel operation (SC_EN = 1, DC_EN = 1) to single-channel operation (SC_EN = 1, DC_EN = 0), notify the channel (CH1 or CH2) for which encoding and decoding is continued using this bit. When stopping Speech CODEC (SC_EN = 0) in single-channel operation mode (SC_EN = 1, DC_EN = 0), clear this bit to "0" from the MCU side.

Even if encoding and decoding for CH2 are continued, LSI performs the processing as single-channel operation and displays statuses of CH1 as statuses of receive requests, transmit requests, and so on.

B3: G.711 PLC function enable control register

The G.711 PLC function can be enabled by setting this bit to "1".

0: Disable

1: Enable

(Note) When setting G711_PLCEN to "1", make sure that SC_EN is "0".

B2-B1: Reserved bits Change of the initial value is inhibited.

B0: Reserved bit Change of the initial value is inhibited.

(25) CR24

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR24	#	#	#	#	#	#	PCM_ TXEN2	PCM_ RXEN2	R/W
Change enable mode	—	—	—	—	—	—	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B2: Reserved bits Change of the initial value is inhibited.

B1: PCM_TXEN2 connection path control

0: Does not connect the path

1: Connects the path

B0: PCM_RXEN2 connection path control

0: Does not connect the path

1: Connects the path

(26) CR25

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR25	FDET _D7	FDET _D6	FDET _D5	FDET _D4	FDET _D3	FDET _D2	FDET _D1	FDET _D0	R/
Change enable mode	—								
Initial value	0	0	0	0	0	0	0	0	

B7-B0: FSK received data storage register

For details, see the section of the FSK Receiver (FSK_DET) in INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later.

(27) CR26

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR26	DPDET_ DATA7	DPDET_ DATA6	DPDET_ DATA5	DPDET_ DATA4	DPDET_ DATA3	DPDET_ DATA2	DPDET_ DATA1	DPDET_ DATA0	R/
Change enable mode	—								
Initial value	0	0	0	0	0	0	0	0	

B7-B0: Detected dial pulse count display register

Displays the dial pulse count that was detected.

For details, see the section of the Dial Pulse Detector (DPDET) in INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later.

(Note)

Read the “detected dial pulse count display register (DPDET_DATA [7:0]) when the setting of the dial pulse detection status register (DP_DET) is changed from “1” to “0”.

(28) CR27

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR27	FGEN _D7	FGEN _D6	FGEN _D5	FGEN _D4	FGEN _D3	FGEN _D2	FGEN _D1	FGEN _D0	R/W
Change enable mode	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7-B0: FSK output data setting register

For details, see the section of the FSK Generator (FSK_GEN) in INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later.

(29) CR28

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR28	FDET _EN	FGEN _EN	TIM_EN	TDET1 _EN	TDET0 _EN	DTMF _EN	EC_EN	#	R/W
Change enable mode	I/E	I/E	I/E	I/E	I/E	I/E	I/E	—	
Initial value	0	0	0	0	0	0	0	0	

B7: FSK_DET control register

0: Stops FSK_DET

1: Activates FSK_DET

When this bit is set to "1", the FSK receiver (FSK_DET) starts operation. For details, see the section of the FSK Receiver (FSK_DET) in INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later.

B6: FSK_GEN control register

0: Stops FSK_GEN

1: Activates FSK_GEN

When this bit is set to "1", the FSK generator (FSK_GEN) starts operation. For details, see the section of the FSK Generator in INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD described later.

B5: Timer control register

When this bit is set to "1", the timer starts counting.

When "0" is set, the timer stops counting and the counter value is cleared.

0: Stops counting

1: Starts counting

B4: TONE1 detector control register

0: Stops TONE_DET1

1: Activates TONE_DET1

When this bit is set to "1", the TONE1 detector starts operation. The TONE1 detector detection status register (TONE1_DET) is set to "1" while the tone of 2100 Hz* is detected.

(Remarks)

* The detection frequency can be changed. When changing the frequency, contact ROHM's responsible sales person.

B3: TONE0 detection control register

0: Stops TONE_DET0

1: Activates TONE_DET0

When this bit is set to "1", the TONE0 detector starts operation. The TONE0 detector detection status register (TONE0_DET) is set to "1" while the tone of 1650Hz* is detected.

(Remarks)

* The detection frequency can be changed. When changing the frequency, contact ROHM's responsible sales person.

B2: DTMF detection control register

0: Stops the DTMF detection function

1: Activates the DTMF detection function

When this bit is set to "1", the DTMF detector starts operation. The DTMF detector detection register (DTMF_DET) is set to "1" while DTMF signals are detected.

B1: Echo canceler control register
0: Stops the echo canceler function (The echo canceler is bypassed.)
1: Activates the echo canceler function
(Remarks) The echo canceler internal coefficient is cleared to start the operation.

B0: Reserved bit Change of the initial value is inhibited.

(30) CR29

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR29	#	DPGEN _EN	DPGEN _POL	DPGEN _PPS	DPGEN _DATA3	DPGEN _DATA2	DPGEN _DATA1	DPGEN _DATA0	R/W
Change enable mode	—	I/E	I/	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bit Change of the initial value is inhibited.

B6: Dial pulse transmitting control register
0: Stops dial pulse output
1: Activates dial pulse output

B5: Dial pulse output polarity control register
0: Positive logic (Low: Break zone, High: Make zone)
1: Negative logic (Low: Make zone, High: Break zone)

B4: Dial pulse speed control register
0: 10 pps
1: 20 pps

B3-B0: Dial pulse count setting register
Set a dial pulse count to be transmitted.
Upper limit: 10 (Data: Ah)
Lower limit: 1 (Data: 1h)

(Note) Be sure to set the following before activating DPGEN (DPGEN_EN = 1).
- Be sure to set the dial pulse output polarity control register (DPGEN_POL).
  By this setting, the output level (initial value) of the dial pulse output pin is set as follows.
  When DPGEN_POL = 0 (positive logic) : GPO0[2]/DPO = “0”
  When DPGEN_POL = 1 (negative logic) : GPO0[2]/DPO = “1”
- After setting the above, set the secondary function (dial pulse output pin) by setting the primary function/secondary function selection register (GPFA[2]) of GPIOA[2] to “1”.

(31) CR30

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR30	#	FDET _SEL	#	DTMF _SEL	TDET1_ SEL1	TDET1_ SEL0	TDET0_ SEL1	TDET0_ SEL0	R/W
Change enable mode	—	I/E	—	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

Select signals to be input to the various detectors in this LSI. For TXDETA, TXDETB, RXDET, and RXDET_PCM, see various detector paths that are shown in the block diagram provided earlier in this document.

B7: Reserved bits Change of the initial value is inhibited.

B6: FSK detection path selection register
0: TXDETA
1: TXDETB

B5: Reserved bits Change of the initial value is inhibited.

B4: DTMF detection path selection register
0: TXDETA
1: TXDETB

B3-B2: TONE_DET1 detection path selection register
00: TXDETA
01: TXDETB
10: RXDET
11: RXDET_PCM

B1-B0: TONE_DET0 detection path selection register
00: TXDETA
01: TXDETB
10: RXDET
11: RXDET_PCM

(32) CR31

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR31	LPEN1	LPEN0	CODEC B_TXEN	CODEC B_RXEN	CODEC A_TXEN	CODEC A_RXEN	SC_ TXEN	SC_ RXEN	R/W
Change enable mode	I/E	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

Set connection/non-connection of various communication paths that are shown in the block diagram provided earlier in this document.

B7: LPEN1 connection path control
0: Non-connection
1: Connection

B6: LPEN0 connection path control
0: Non-connection
1: Connection

B5: CODECB_TXEN connection path control
0: Non-connection
1: Connection

B4: CODECB_RXEN connection path control
0: Non-connection
1: Connection

B3: CODECA_TXEN connection path control
0: Non-connection
1: Connection

B2: CODECA_RXEN connection path control
0: Non-connection
1: Connection

B1: SC_TXEN connection path control
0: Non-connection
1: Connection

B0: SC_RXEN connection path control
0: Non-connection
1: Connection

(33) CR32

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR32	#	#	RXGEN A_EN	RXGEN B_EN	PCM_ TXEN1	PCM_ TXEN0	PCM_ RXEN1	PCM_ RXEN0	R/W
Change enable mode	—	—	I/E	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

Set connection/non-connection of various communication paths that are shown in the block diagram provided earlier in this document.

B7-B6: Reserved bits Changing of the initial values is inhibited.

B5: RXGENA_EN connection path control
0: Non-connection
1: Connection

B4: RXGENB_EN connection path control
0: Non-connection
1: Connection

B3: PCM_TXEN1 connection path control
0: Non-connection
1: Connection

B2: PCM_TXEN0 connection path control
0: Non-connection
1: Connection

B1: PCM_RXEN1 connection path control
0: Non-connection
1: Connection

B0: PCM_RXEN0 connection path control
0: Non-connection
1: Connection

(34) CR33

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR33	#	#	#	PCM_ ITS1[4]	PCM_ ITS1[3]	PCM_ ITS1[2]	PCM_ ITS1[1]	PCM_ ITS1[0]	R/W
Change enable mode	—	—	—	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B5: Reserved bits Changing of the initial values is inhibited.

B4-B0: PCM input time slot selection register 1

Set the time slot number for fetching PCM data according to the selection table 8.

To receive PCM data in the selected time slot position, set the PCM input time slot 1 enable control register (PCMI1_EN) to "1".

Table 8 PCM Input Time Slot Selection Table 1

B4	B3	B2	B1	B0	Time Slot	B4	B3	B2	B1	B0	Time Slot
0	0	0	0	0	Slot1	1	0	0	0	0	Slot17
0	0	0	0	1	Slot2	1	0	0	0	1	Slot18
0	0	0	1	0	Slot3	1	0	0	1	0	Slot19
0	0	0	1	1	Slot4	1	0	0	1	1	Slot20
0	0	1	0	0	Slot5	1	0	1	0	0	Slot21
0	0	1	0	1	Slot6	1	0	1	0	1	Slot22
0	0	1	1	0	Slot7	1	0	1	1	0	Slot23
0	0	1	1	1	Slot8	1	0	1	1	1	Slot24
0	1	0	0	0	Slot9	1	1	0	0	0	Slot25
0	1	0	0	1	Slot10	1	1	0	0	1	Slot26
0	1	0	1	0	Slot11	1	1	0	1	0	Slot27
0	1	0	1	1	Slot12	1	1	0	1	1	Slot28
0	1	1	0	0	Slot13	1	1	1	0	0	Slot29
0	1	1	0	1	Slot14	1	1	1	0	1	Slot30
0	1	1	1	0	Slot15	1	1	1	1	0	Slot31
0	1	1	1	1	Slot16	1	1	1	1	1	Slot32

(Note)

Make sure that the PCM input time slot selection 1 enable control register (PCMI1_EN) is kept "0" when the register is set.

(Note)

The number of bits of one time slot changes automatically according to the setting of the PCM coding format (PCM_SEL[1:0]):

16-bit linear setting : 16 bits

G.711 (μ-law/A-law) setting : 8 bits

Therefore, the maximum time slot number that can be set is as follows.

16-bit linear setting : n/2

G.711 (μ-law/A-law) setting : n

[n = (BCLK frequency) ÷ 64 kHz]

Any number exceeding the maximum time slot number cannot be set.

(35) CR34

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR34	#	#	#	PCM_ ITS2[4]	PCM_ ITS2[3]	PCM_ ITS2[2]	PCM_ ITS2[1]	PCM_ ITS2[0]	R/W
Change enable mode	—	—	—	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B5: Reserved bits Changing of the initial values is inhibited.

B4-B0: PCM input time slot selection register 2

Set the time slot number for fetching PCM data according to the selection table 9.

To receive PCM data in the selected time slot position, set the PCM input time slot 2 enable control register (PCMI2_EN) to "1".

Table 9 PCM Input Time Slot Selection Table 2

B4	B3	B2	B1	B0	Time Slot	B4	B3	B2	B1	B0	Time Slot
0	0	0	0	0	Slot1	1	0	0	0	0	Slot17
0	0	0	0	1	Slot2	1	0	0	0	1	Slot18
0	0	0	1	0	Slot3	1	0	0	1	0	Slot19
0	0	0	1	1	Slot4	1	0	0	1	1	Slot20
0	0	1	0	0	Slot5	1	0	1	0	0	Slot21
0	0	1	0	1	Slot6	1	0	1	0	1	Slot22
0	0	1	1	0	Slot7	1	0	1	1	0	Slot23
0	0	1	1	1	Slot8	1	0	1	1	1	Slot24
0	1	0	0	0	Slot9	1	1	0	0	0	Slot25
0	1	0	0	1	Slot10	1	1	0	0	1	Slot26
0	1	0	1	0	Slot11	1	1	0	1	0	Slot27
0	1	0	1	1	Slot12	1	1	0	1	1	Slot28
0	1	1	0	0	Slot13	1	1	1	0	0	Slot29
0	1	1	0	1	Slot14	1	1	1	0	1	Slot30
0	1	1	1	0	Slot15	1	1	1	1	0	Slot31
0	1	1	1	1	Slot16	1	1	1	1	1	Slot32

(Note)

Make sure that the PCM input time slot selection 2 enable control register (PCMI2_EN) is kept "0" when the register is set.

(Note)

The number of bits of one time slot changes automatically according to the setting of the PCM coding format (PCM_SEL[1:0]):

16-bit linear setting : 16 bits

G.711 (μ-law/A-law) setting : 8 bits

Therefore, the maximum time slot number that can be set is as follows.

16-bit linear setting : n/2

G.711 (μ-law/A-law) setting : n

[n = (BCLK frequency) ÷ 64 kHz]

Any number exceeding the maximum time slot number cannot be set.

(36) CR35

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR35	#	#	#	PCM_ OTS1[4]	PCM_ OTS1[3]	PCM_ OTS1[2]	PCM_ OTS1[1]	PCM_ OTS1[0]	R/W
Change enable mode	—	—	—	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B5: Reserved bits Changing of the initial values is inhibited.

B4-B0: PCM output time slot selection register 1

Set the time slot number for outputting PCM data according to the selection table 10.

To output PCM data in the selected time slot position, set the PCM output time slot 1 enable control register (PCMO1_EN) to "1".

Table 10 PCM Output Time Slot Selection Table 1

B4	B3	B2	B1	B0	Time Slot	B4	B3	B2	B1	B0	Time Slot
0	0	0	0	0	Slot1	1	0	0	0	0	Slot17
0	0	0	0	1	Slot2	1	0	0	0	1	Slot18
0	0	0	1	0	Slot3	1	0	0	1	0	Slot19
0	0	0	1	1	Slot4	1	0	0	1	1	Slot20
0	0	1	0	0	Slot5	1	0	1	0	0	Slot21
0	0	1	0	1	Slot6	1	0	1	0	1	Slot22
0	0	1	1	0	Slot7	1	0	1	1	0	Slot23
0	0	1	1	1	Slot8	1	0	1	1	1	Slot24
0	1	0	0	0	Slot9	1	1	0	0	0	Slot25
0	1	0	0	1	Slot10	1	1	0	0	1	Slot26
0	1	0	1	0	Slot11	1	1	0	1	0	Slot27
0	1	0	1	1	Slot12	1	1	0	1	1	Slot28
0	1	1	0	0	Slot13	1	1	1	0	0	Slot29
0	1	1	0	1	Slot14	1	1	1	0	1	Slot30
0	1	1	1	0	Slot15	1	1	1	1	0	Slot31
0	1	1	1	1	Slot16	1	1	1	1	1	Slot32

(Note)

Make sure that the PCM output time slot selection 1 enable control register (PCMO1_EN) is kept "0" when the register is set.

(Note)

The number of bits of one time slot changes automatically according to the setting of the PCM coding format (PCM_SEL[1:0]):

16-bit linear setting : 16 bits

G.711 (μ-law/A-law) setting : 8 bits

Therefore, the maximum time slot number that can be set is as follows.

16-bit linear setting : n/2

G.711 (μ-law/A-law) setting : n

[n = (BCLK frequency) ÷ 64 kHz]

Any number exceeding the maximum time slot number cannot be set.

(37) CR36

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR36	#	#	#	PCM_ ITS3[4]	PCM_ ITS3[3]	PCM_ ITS3[2]	PCM_ ITS3[1]	PCM_ ITS3[0]	R/W
Change enable mode	—	—	—	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B5: Reserved bits Changing of the initial values is inhibited.

B4-B0: PCM input time slot selection register 3

Set the time slot number for fetching PCM data according to the selection table 11.

To receive PCM data in the selected time slot position, set the PCM input time slot 3 enable control register (PCMI3_EN) to "1".

Table 11 PCM Input Time Slot Selection Table 3

B4	B3	B2	B1	B0	Time Slot	B4	B3	B2	B1	B0	Time Slot
0	0	0	0	0	Slot1	1	0	0	0	0	Slot17
0	0	0	0	1	Slot2	1	0	0	0	1	Slot18
0	0	0	1	0	Slot3	1	0	0	1	0	Slot19
0	0	0	1	1	Slot4	1	0	0	1	1	Slot20
0	0	1	0	0	Slot5	1	0	1	0	0	Slot21
0	0	1	0	1	Slot6	1	0	1	0	1	Slot22
0	0	1	1	0	Slot7	1	0	1	1	0	Slot23
0	0	1	1	1	Slot8	1	0	1	1	1	Slot24
0	1	0	0	0	Slot9	1	1	0	0	0	Slot25
0	1	0	0	1	Slot10	1	1	0	0	1	Slot26
0	1	0	1	0	Slot11	1	1	0	1	0	Slot27
0	1	0	1	1	Slot12	1	1	0	1	1	Slot28
0	1	1	0	0	Slot13	1	1	1	0	0	Slot29
0	1	1	0	1	Slot14	1	1	1	0	1	Slot30
0	1	1	1	0	Slot15	1	1	1	1	0	Slot31
0	1	1	1	1	Slot16	1	1	1	1	1	Slot32

(Note)

Make sure that the PCM input time slot selection 3 enable control register (PCMI3_EN) is kept "0" when the register is set.

(Note)

The number of bits of one time slot changes automatically according to the setting of the PCM coding format (PCM_SEL[1:0]):

16-bit linear setting : 16 bits

G.711 (μ-law/A-law) setting : 8 bits

Therefore, the maximum time slot number that can be set is as follows.

16-bit linear setting : n/2

G.711 (μ-law/A-law) setting : n

[n = (BCLK frequency) ÷ 64 kHz]

Any number exceeding the maximum time slot number cannot be set.

(38) CR37

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR37	$	$	$	$	$	$	$	$	/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7-B0: Reserved bits Access is inhibited.

(39) CR38

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR38	#	#	#	PCM_ OTS2[4]	PCM_ OTS2[3]	PCM_ OTS2[2]	PCM_ OTS2[1]	PCM_ OTS2[0]	R/W
Change enable mode	—	—	—	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B5: Reserved bits Changing of the initial values is inhibited.

B4-B0: PCM output time slot selection register 2

Set the time slot number for outputting PCM data according to the selection table 12.

To output PCM data in the selected time slot position, set the PCM output time slot 2 enable control register (PCMO2_EN) to "1".

Table 12 PCM Output Time Slot Selection Table 2

B4	B3	B2	B1	B0	Time Slot	B4	B3	B2	B1	B0	Time Slot
0	0	0	0	0	Slot1	1	0	0	0	0	Slot17
0	0	0	0	1	Slot2	1	0	0	0	1	Slot18
0	0	0	1	0	Slot3	1	0	0	1	0	Slot19
0	0	0	1	1	Slot4	1	0	0	1	1	Slot20
0	0	1	0	0	Slot5	1	0	1	0	0	Slot21
0	0	1	0	1	Slot6	1	0	1	0	1	Slot22
0	0	1	1	0	Slot7	1	0	1	1	0	Slot23
0	0	1	1	1	Slot8	1	0	1	1	1	Slot24
0	1	0	0	0	Slot9	1	1	0	0	0	Slot25
0	1	0	0	1	Slot10	1	1	0	0	1	Slot26
0	1	0	1	0	Slot11	1	1	0	1	0	Slot27
0	1	0	1	1	Slot12	1	1	0	1	1	Slot28
0	1	1	0	0	Slot13	1	1	1	0	0	Slot29
0	1	1	0	1	Slot14	1	1	1	0	1	Slot30
0	1	1	1	0	Slot15	1	1	1	1	0	Slot31
0	1	1	1	1	Slot16	1	1	1	1	1	Slot32

(Note)

Make sure that the PCM output time slot selection 2 enable control register (PCMO2_EN) is kept "0" when the register is set.

(Note)

The number of bits of one time slot changes automatically according to the setting of the PCM coding format (PCM_SEL[1:0]):

16-bit linear setting : 16 bits

G.711 (μ-law/A-law) setting : 8 bits

Therefore, the maximum time slot number that can be set is as follows.

16-bit linear setting : n/2

G.711 (μ-law/A-law) setting : n

[n = (BCLK frequency) ÷ 64 kHz]

Any number exceeding the maximum time slot number cannot be set.

(40) CR39 to CR42

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR39 to CR42	$	$	$	$	$	$	$	$	/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7-B0: Reserved bits Access is inhibited.

(41) CR43

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR43	#	#	#	#	#	#	DPDET_POL	DPDET_EN	R/W
Change enable mode	—	—	—	—	—	—	I/	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7-B2: Reserved bits Changing of the initial values is inhibited.

B1: Dial pulse detection polarity control register
Controls the polarity that is input from the DPI pin.
0: Polarity not inverted
1: Polarity inverted

B0: Dial pulse detector control register
0: Stops a dial pulse detector
1: Activates a dial pulse detector

(42) CR44 to CR47

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR44 to CR47	$	$	$	$	$	$	$	$	/
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7-B0: Reserved bits Access is inhibited.

(43) GPCR0

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR0	#	GPMA [6]	GPMA [5]	GPMA [4]	GPMA [3]	GPMA [2]	GPMA [1]	GPMA [0]	R/W
Change enable mode	—	I/E	I/E	I/E	I/E	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

Using this register (GPMA[6:0]), the direction (input or output) of general-purpose I/O port A [6:0] (GPIOA[6:0]) can be set in bit units.

B7: Reserved bits Changing of the initial values is inhibited.

B6: Input-output setting register of GPIOA[6]
0: Input
1: Output
When GPFA[6] is set to the secondary function (INTB), the pin is always set to the output state.

B5: Input-output setting register of GPIOA[5]
0: Input
1: Output
When GPFA[5] is set to the secondary function (ACK1B), the pin is always set to the input state.

B4: Input-output setting register of GPIOA[4]
0: Input
1: Output
When GPFA[4] is set to the secondary function (ACK0B), the pin is always set to the input state.

B3: Input-output setting register of GPIOA[3]
0: Input
1: Output

B2: Input-output setting register of GPIOA[2]
0: Input
1: Output
When GPFA[2] is set to the secondary function (DPO), the pin is always set to the output state.

B1: Input-output setting register of GPIOA[1]
0: Input
1: Output

B0: Input-output setting register of GPIOA[0]
0: Input
1: Output
When GPFA[0] is set to the secondary function (DPI), the pin is always set to the input state.

(44) GPCR1

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR1	#	GPDA [6]	GPDA [5]	GPDA [4]	GPDA [3]	GPDA [2]	GPDA [1]	GPDA [0]	R/W
Change enable mode		I/E	I/E	I/E	I/E	I/E	I/E	I/E	
Initial value	0	*	*	*	*	*	*	*	

* Depends on the pin status.

This register (GPDA[6:0]) is used to store input-output data of general-purpose I/O port A[6:0]. (GPIOA[6:0]).
When this register is set to a general-purpose output port and a value is written to an appropriate bit, the written value is output from the corresponding pin. In this case, when read processing is performed for the bit, the value in the bit is read.
When this register is set to a general-purpose input port, the status of an appropriate pin can be read by reading the corresponding bit. Even if write processing is performed for the bit, the pin status remains unchanged although the register value is updated.
When the port is set to the secondary function in the primary function/secondary function selection register, the register value is updated when data is written to an appropriate bit, but, the pin status remains unchanged. When input is set in GPMA[6:0], the pin status is read. When output is set, the bit value is read.

B7: Reserved bits Changing of the initial values is inhibited.

B6: Data register of GPIOA[6]

GPFA[6]	GPMA[6]	At read processing	At write processing
0: GPIOA[6]	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[6]	Written value is output from the appropriate pin
1: INTB	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[6]	Pin status remains unchanged

B5: Data register of GPIOA[5]

GPFA[5]	GPMA[5]	At read processing	At write processing
0: GPIOA[5]	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[5]	Written value is output from the appropriate pin
1: ACK1B	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[5]	Pin status remains unchanged

B4: Data register of GPIOA[4]

GPFA[4]	GPMA[4]	At read processing	At write processing
0: GPIOA[4]	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[4]	Written value is output from the appropriate pin
1: ACK0B	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[4]	Pin status remains unchanged

B3: Data register of GPIOA[3]

GPMA[3]	At read processing	At write processing
0: Input	Pin status	Pin status remains unchanged
1: Output	Value of GPDA[3]	Written value is output from the appropriate pin

B2: Data register of GPIOA[2]

GPFA[2]	GPMA[2]	At read processing	At write processing
0: GPIOA[2]	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[2]	Written value is output from the appropriate pin
1: DPO	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[2]	Pin status remains unchanged

B1: Data register of GPIOA[1]

GPMA[1]	At read processing	At write processing
0: Input	Pin status	Pin status remains unchanged
1: Output	Value of GPDA[1]	Written value is output from the appropriate pin

B0: Data register of GPIOA[0]

GPFA[0]	GPMA[0]	At read processing	At write processing
0: GPIOA[0]	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[0]	Written value is output from the appropriate pin
1: DPI	0: Input	Pin status	Pin status remains unchanged
	1: Output	Value of GPDA[0]	Pin status remains unchanged

(45) GPCR2

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR2	#	GPFA [6]	GPFA [5]	GPFA [4]	#	GPFA [2]	#	GPFA [0]	R/W
Change enable mode	—	I/E	I/E	I/E	—	I/E	—	I/E	
Initial value	0	1	1	1	0	0	0	0	

Use this register (GPFA[6-4,2]) to select the primary function/secondary function of general-purpose I/O port A [6-4,2,0] (GPIOA[6-4,2,0]).

B7: Reserved bits Changing of the initial values is inhibited.

B6: Primary/secondary selection register of GPIOA[6]
0: General-purpose I/O port A[6]
1: INTB (Initial value)

B5: Primary/secondary selection register of GPIOA[5]
0: General-purpose I/O port A[5]
1: ACK1B (Initial value)

B4: Primary/secondary selection register of GPIOA[4]
0: General-purpose I/O port A[4]
1: ACK0B (Initial value)

B3: Reserved bit Changing of the initial value is inhibited.

B2: Primary/secondary selection register of GPIOA[2]
0: General-purpose I/O port A[2] (Initial value)
1: DPO (Dial pulse output pin)

B1: Reserved bits Changing of the initial values is inhibited.

B0: Primary/secondary selection register of GPIOA[0]
0: General-purpose I/O port A[0] (Initial value)
1: DPI (Dial pulse input pin)

Table 13 lists primary functions/secondary functions of general-purpose I/O port A (GPIOA[6:0])

Table 13 GPIOA[6:0] Primary Functions/Secondary Functions

Pin	Primary function	Secondary function
GPIOA[6]	General-purpose I/O port A[6]	INTB
GPIOA[5]	General-purpose I/O port A[5]	ACK1B
GPIOA[4]	General-purpose I/O port A[4]	ACK0B
GPIOA[3]	General-purpose I/O port A[3]	—
GPIOA[2]	General-purpose I/O port A[2]	DPO (dial pulse output pin)
GPIOA[1]	General-purpose I/O port A[1]	—
GPIOA[0]	General-purpose I/O port A[0]	DPI (dial pulse input pin)

(46) GPCR3

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR3	#	#	#	#	#	#	#	#	R/W
Changeable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bits Changing of the initial values is inhibited.
B6: Reserved bits Changing of the initial values is inhibited.
B5: Reserved bits Changing of the initial values is inhibited.
B4: Reserved bits Changing of the initial values is inhibited.
B3: Reserved bits Changing of the initial values is inhibited.
B2: Reserved bits Changing of the initial values is inhibited.
B1: Reserved bits Changing of the initial values is inhibited.
B0: Reserved bits Changing of the initial values is inhibited.
(Note) Access to this register is inhibited.

(47) GPCR4

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR4	#	#	#	#	#	#	#	#	R/W
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bits Changing of the initial values is inhibited.
B6: Reserved bits Changing of the initial values is inhibited.
B5: Reserved bits Changing of the initial values is inhibited.
B4: Reserved bits Changing of the initial values is inhibited.
B3: Reserved bits Changing of the initial values is inhibited.
B2: Reserved bits Changing of the initial values is inhibited.
B1: Reserved bits Changing of the initial values is inhibited.
B0: Reserved bits Changing of the initial values is inhibited.
(Note) Access to this register is inhibited.

(48) GPCR5

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR5	#	#	#	#	#	#	#	#	R/W
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bits Changing of the initial values is inhibited.
B6: Reserved bits Changing of the initial values is inhibited.
B5: Reserved bits Changing of the initial values is inhibited.
B4: Reserved bits Changing of the initial values is inhibited.
B3: Reserved bits Changing of the initial values is inhibited.
B2: Reserved bits Changing of the initial values is inhibited.
B1: Reserved bits Changing of the initial values is inhibited.
B0: Reserved bits Changing of the initial values is inhibited.
(Note) Access to this register is inhibited.

(49) GPCR6

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR6	#	#	#	#	#	#	#	#	R/W
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bits Changing of the initial values is inhibited.
B6: Reserved bits Changing of the initial values is inhibited.
B5: Reserved bits Changing of the initial values is inhibited.
B4: Reserved bits Changing of the initial values is inhibited.
B3: Reserved bits Changing of the initial values is inhibited.
B2: Reserved bits Changing of the initial values is inhibited.
B1: Reserved bits Changing of the initial values is inhibited.
B0: Reserved bits Changing of the initial values is inhibited.
(Note) Access to this register is inhibited.

(50) GPCR7

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR7	#	#	#	#	#	#	#	#	R/W
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bits Changing of the initial values is inhibited.
B6: Reserved bits Changing of the initial values is inhibited.
B5: Reserved bits Changing of the initial values is inhibited.
B4: Reserved bits Changing of the initial values is inhibited.
B3: Reserved bits Changing of the initial values is inhibited.
B2: Reserved bits Changing of the initial values is inhibited.
B1: Reserved bits Changing of the initial values is inhibited.
B0: Reserved bits Changing of the initial values is inhibited.
(Note) Access to this register is inhibited.

(51) CRCR8

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
GPCR8	#	#	#	#	#	#	#	#	R/W
Change enable mode	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bits Changing of the initial values is inhibited.
B6: Reserved bits Changing of the initial values is inhibited.
B5: Reserved bits Changing of the initial values is inhibited.
B4: Reserved bits Changing of the initial values is inhibited.
B3: Reserved bits Changing of the initial values is inhibited.
B2: Reserved bits Changing of the initial values is inhibited.
B1: Reserved bits Changing of the initial values is inhibited.
B0: Reserved bits Changing of the initial values is inhibited.
(Note) Access to this register is inhibited.

INTERNAL DATA MEMORY ACCESS AND CONTROL METHOD

The 8-bit registers (CR6 to CR9) that are mapped in the control registers are assigned to the following:
16-bit address of the internal data memory (A15 to A0)
16-bit data for write/read processing (D15 to D0)
The LSI is set to an initial mode about 200 ms after resetting by power-down reset with PDNB or by software power-down reset with SPDN, and the initial mode display register (READY) is set to "1". In initial mode, control register and internal data memory can be changed. This section describes how to write and read internal data memory.

Write Method (Single-Word)

Single-word internal data write processing is completed by setting the internal data memory single-word write control register (XDMWR) to "1" after an internal data memory address and data to be written are set in CR6-CR9. After termination of write operation, XDMWR is automatically cleared to "0". Figure 52 shows the method of writing single-word to internal data memory.
To rewrite data to multiple memory spaces with distributed address arears, repeat the write operation described above.
By setting the operation start control register (OPE_STAT) to "1" after completion of the entire write operation, normal operation can be started.

Write operation to the internal data memory is allowed in normal operation mode also. In this case also, use the method described above.

(Note)
When the internal data memory is changed during in normal operation mode, retain the changed data for 250 μs or more since read operation is performed synchronized with a SYNC signal (8 kHz).

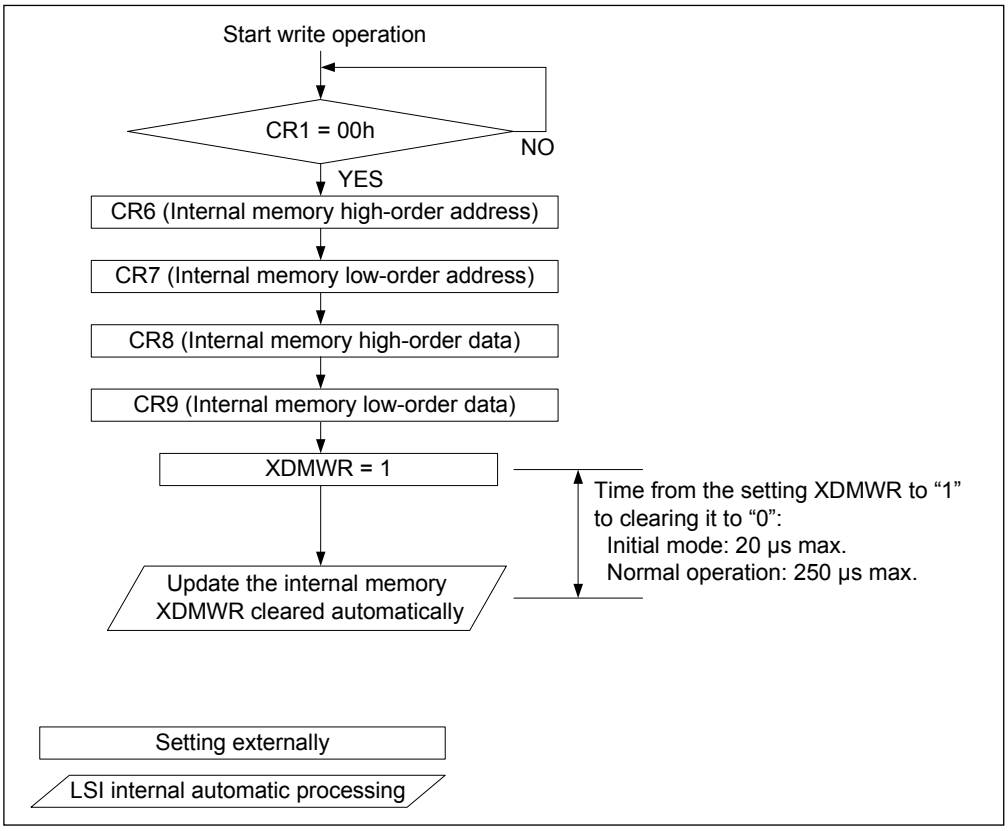


Figure 52 Internal Data Memory Write Method (Single-Word)

Write Method (Multiple Words)

When data is written to consecutive address spaces in the internal data memory, multiple-word (2N words) continuous write operation is allowed.

1) Setting a starting address
   Use the write method (single-word) in Figure 52 for setting a starting address.
   Set address 00E9h in CR6-CR7. This address is for setting the starting address for writing multiple words.
   Also set in CR8-CR9 the starting address (START_ADDRESS) of the internal data memory to which multiple words are to be written.
   By setting the internal data memory single-word write control register (XDMWR) to "1", the START_ADDRESS is written in address 00E9h in the internal data memory. After termination of write operation, XDMWR is automatically cleared to "0".

2) Writing data
   After termination of START_ADDRESS write operation, data can be written consecutively in 2-word units without setting the addresses individually using the following procedure.
   Set in CR6-CR7 first word of the data to be written and 2nd word in CR8-CR9 and set the internal data memory 2-word write control register (XDMWR_2) to "1". By doing this, the first word is written in START_ADDRESS+0 and the second word is written in START_ADDRESS+1. After termination of write operation, XMWR_2 is automatically cleared to "0".

   Subsequently, repeat 2-word data write operation using the data write procedure that is described in 2) until completion of write operation for 2N words. (The write destination addresses are updated automatically.)
   Figure 53 shows the internal data memory write method (multiple words).

   Write operation to the internal data memory is allowed in normal operation mode also. In this case also, use the method described above.

   (Note)
   When the internal data memory is changed during normal operation mode, retain the changed data for 250 μs or more since read operation is performed synchronized with a SYNC signal (8 kHz).

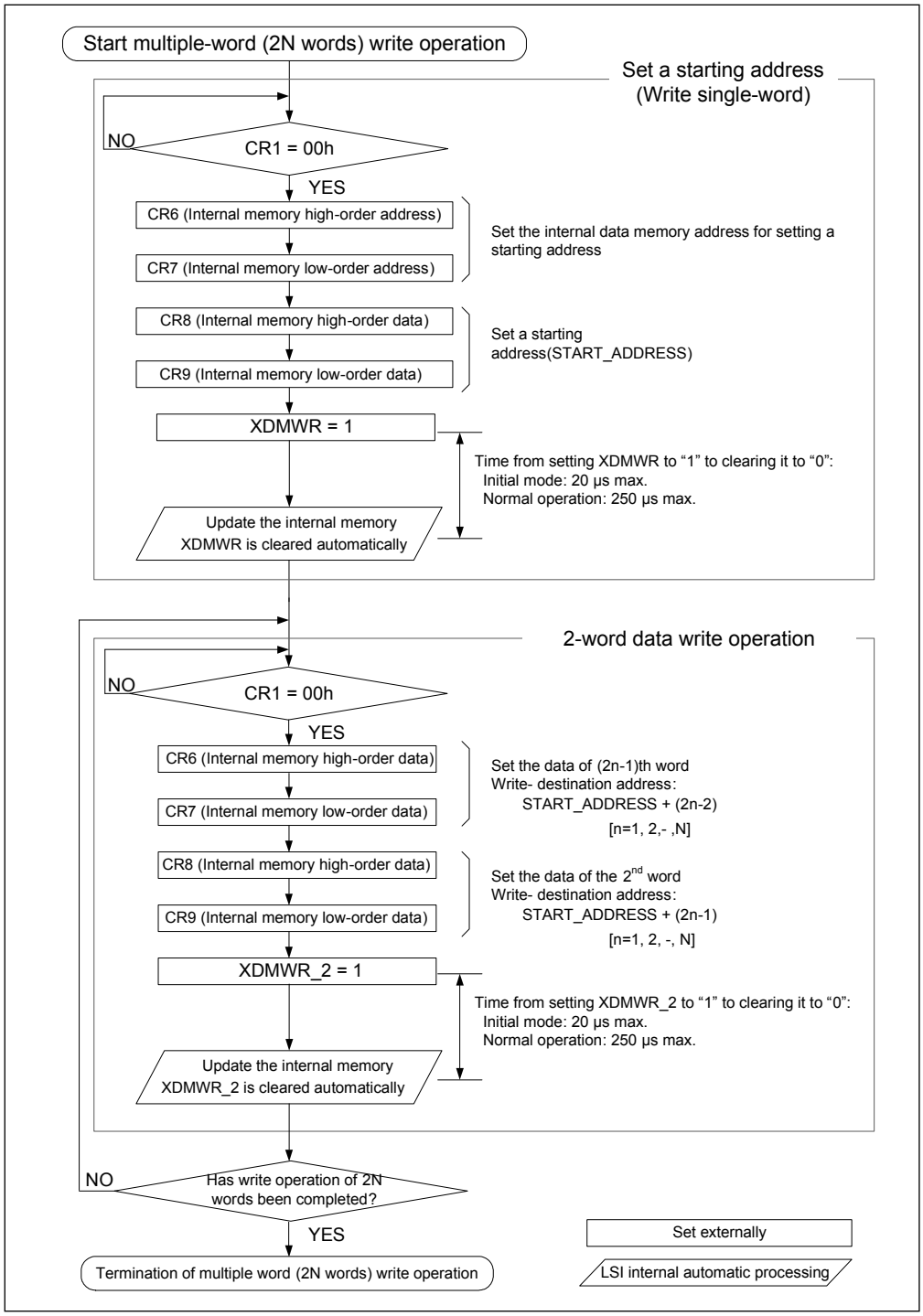


Figure 53 Internal Data Memory Write Method (Multiple Words)

Read Method

By setting an internal data memory address in CR6 and CR7 and setting the internal memory read control register (XDMRD) to "1", single-word data in the internal data memory is stored in CR8 and CR9. After termination of read operation, XDMRD is cleared to "0" automatically. Figure 54 shows the internal data memory read method.
Internal data memory read operation is allowed only for the internal data memory that is shown in Table 14 and read only data memory in the related registers.
Read operation for the internal data memory is allowed in normal operation mode also. In this case also, use the method described above.
(Note)
When internal data memory is read in normal operation mode, maintain the address that was set for 250 μsec or more since read operation is performed synchronized with a SYNC signal (8 kHz).

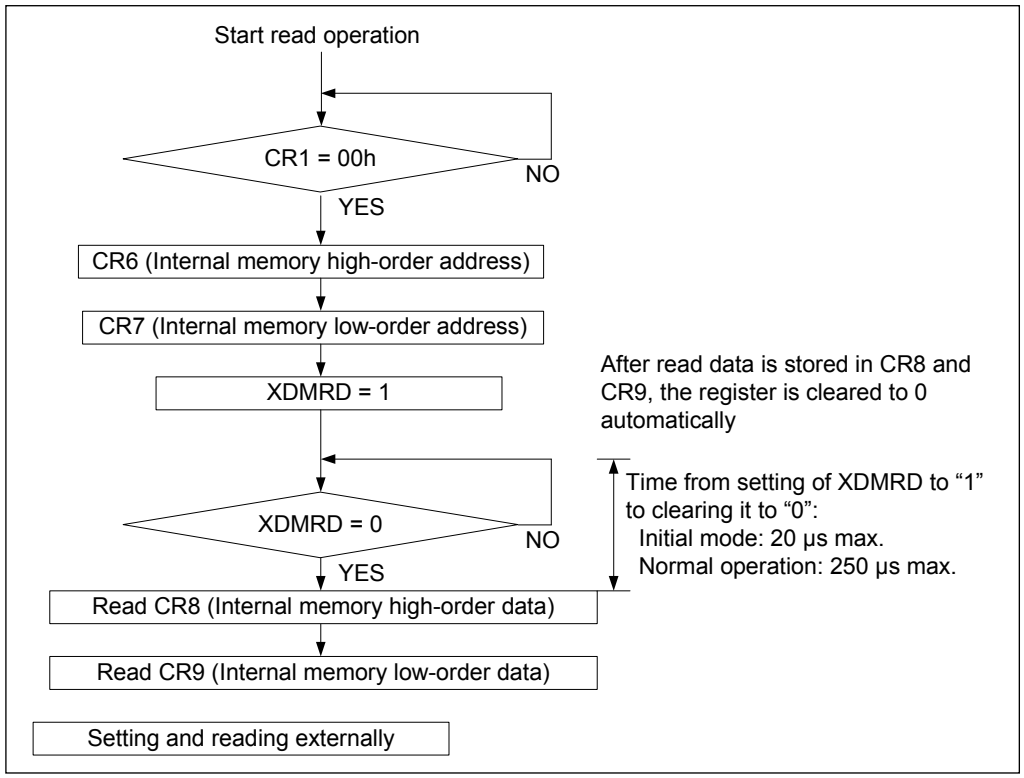


Figure 54 Internal Data Memory Read Method

Table 14 Internal Data Memory/Related Control Registers (1 of 7)

Function name	Internal data memory/related control register name	Address	Initial value		Change/read enable mode		
			Data	Data value	Initial mode	Inactive	Active
Gain control	Transmit path related						
	Speech CODEC transmit gain (TXGAIN_SC)	05E7h	0080h	0 dB	○	○	○
	CODECA transmit gain (TXGAINA)	05E3h	0080h	0 dB	○	○	○
	CODECB transmit gain (TXGAINB)	05E4h	0080h	0 dB	○	○	○
	Receive path related						
	Speech CODEC receive gain (RXGAIN_SC)	05E8h	0080h	0 dB	○	○	○
	CODECA receive gain (RXGAINA)	05E5h	0080h	0 dB	○	○	○
	CODECB receive gain (RXGAINB)	05E6h	0080h	0 dB	○	○	○
	Side tone related						
	CODECA side tone gain (STGAINA)	05DFh	0000h	MUTE	○	○	○
	CODECB side tone gain (STGAINB)	05E0h	0000h	MUTE	○	○	○
	PCM related						
	PCM transmit gain0 (TXGAIN_PCM0)	05EAh	0080h	0 dB	○	○	○
	PCM transmit gain1 (TXGAIN_PCM1)	05E9h	0080h	0 dB	○	○	○
	PCM transmit gain2 (TXGAIN_PCM2)	05F1h	0080h	0 dB	○	○	○
	PCM receive gain0 (RXGAIN_PCM0)	05EBh	0080h	0 dB	○	○	○
	PCM receive gain1 (RXGAIN_PCM1)	05ECh	0080h	0 dB	○	○	○
	PCM receive gain2 (RXGAIN_PCM2)	05F2h	0080h	0 dB	○	○	○
	PCM input time slot selection 1 receive gain (RXGAIN_ITS1)	05EDh	0080h	0 dB	○	○	○
	PCM input time slot selection 2 receive gain (RXGAIN_ITS2)	05EEh	0080h	0 dB	○	○	○
	Three-way communication related						
	CH1 receive gain (RXGAIN_CH1)	0132h	0080h	0 dB	○	○	○
	CH2 receive gain (RXGAIN_CH2)	0131h	0080h	0 dB	○	○	○
	CH1 transmit gain (TXGAIN_CH1)	0134h	0080h	0 dB	○	○	○
	CH2 transmit gain (TXGAIN_CH2)	0133h	0080h	0 dB	○	○	○
	CH2 receive→CH1 transmit loop back gain (RX2TX1_GAIN)	0136h	0080h	0 dB	○	○	○
	CH1 receive→CH2 transmit loop back gain (RX1TX2_GAIN)	0135h	0080h	0 dB	○	○	○
	Fade control related						
	Gain fade control 0 (GAIN_FADE_CONT0)	05F3h	0000h	Stop	○	○	×
	Gain fade control 1 (GAIN_FADE_CONT1)	0137h	0040h	Stop	○	○	×
	Gain fade control 2 (GAIN_FADE_CONT2)	05F4h	0000h	Stop	○	○	×
	Gain fade-in step value control (GAIN_FADE_IN_ST)	05F5h	4C10h	+1.5 dB	○	○(*1)	×
	Gain fade-out step value control (GAIN_FADE_OUT_ST)	05F6h	35D9h	−1.5 dB	○	○(*1)	×

(*1) Applies when the gain fade control is inactive.

Table 14 Internal Data Memory/Related Control Registers (2 of 7)

Function name	Internal data memory/related control register name	Address	Initial value		Change/read enable mode		
			Data	Data value	Initial mode	Inactive	Active
Tone generation 0 TONE _GEN0	TGEN0 transmit control register	CR2	00h	Stop transmission	○	○	○
	TONE A frequency control (TGEN0_FREQ_A)	02E2h	0CCDh	400Hz	○	○	×
	TONE B frequency control (TGEN0_FREQ_B)	02E4h	007Bh	15Hz	○	○	×
	TONE A gain control (TGEN0_GAIN_A)	02E6h	0080h	−13.3 dBm0	○	○	○
	TONE B gain control (TGEN0_GAIN_B)	02E7h	0080h	−13.3 dBm0	○	○	○
	TGEN0 output time control 0 (TGEN0_TIM_M0)	02E8h	0FA0h	500 ms	○	○	×
	TGEN0 output time control 1 (TGEN0_TIM_M1)	02EBh	0FA0h	500 ms	○	○	×
	TGEN0 RXAB side tone total gain control (TGEN0_RXABGAIN_TOTAL)	02EFh	0080h	0 dB	○	○	○
	TGEN0 RX side tone total gain control (TGEN0_RXGAIN_TOTAL)	02F0h	0080h	0 dB	○	○	○
	TGEN0 fade control (TGEN0_FADE_CONT)	02DAh	0000h	Stop	○	○	×
	TGEN0 fade-in step value control (TGEN0_FADE_IN_ST)	02DBh	47CFh	+1 dB	○	○	×
	TGEN0 fade-out step value control (TGEN0_FADE_OUT_ST)	02DCh	390Ah	−1 dB	○	○	×
	TGEN0 fade-out time control (TGEN0_FADE_OUT_TIM)	02DDh	002Bh	43 Sync	○	○	×
	TGEN0 total gain fade control (TGEN0_GAIN_TOTAL_FADE_CONT)	02ECh	0000h	Stop	○	○	×
	TGEN0 total gain fade-in step value control (TGEN0_GAIN_TOTAL_FADE_IN_ST)	02EDh	4C10h	+1.5 dB	○	○	×
	TGEN0 total gain fade-out step value control (TGEN0_GAIN_TOTAL_FADE_OUT_ST)	02EEh	35D9h	−1.5 dB	○	○	×
	TGEN0 execution flag display register (TGEN0_EXFLAG)	CR19 -B1	0b	Stop	○	○	○
Tone generation 1 TONE _GEN1	TGEN1 transmit control register	CR3	00h	Stop transmission	○	○	○
	TONE C frequency control (TGEN1_FREQ_C)	02F9h	0CCDh	400Hz	○	○	×
	TONE D frequency control (TGEN1_FREQ_D)	02FBh	007Bh	15Hz	○	○	×
	TONE C gain control (TGEN1_GAIN_C)	02FDh	0080h	−13.3 dBm0	○	○	○
	TONE D gain control (TGEN1_GAIN_D)	02FEh	0080h	−13.3 dBm0	○	○	○
	TGEN1 output time control 0 (TGEN1_TIM_M0)	02FFh	0FA0h	500 ms	○	○	×
	TGEN1 output time control 1 (TGEN1_TIM_M1)	0302h	0FA0h	500 ms	○	○	×
	TGEN1 RXAB side tone total gain control (TGEN1_RXABGAIN_TOTAL)	0306h	0080h	0 dB	○	○	○
	TGEN1 TX side tone total gain control (TGEN1_TXGAIN_TOTAL)	0307h	0080h	0 dB	○	○	○

Table 14 Internal Data Memory/Related Control Registers (3 of 7)

Function name	Internal data memory/related control register name	Address	Initial value		Change/read enable mode		
			Data	Data value	Initial mode	Inactive	Active
Tone generation 1 TONE _GEN1	TGEN1 fade control (TGEN1_FADE_CONT)	02F1h	0000h	Stop	○	○	×
	TGEN1 fade-in step value control (TGEN1_FADE_IN_ST)	02F2h	47CFh	+1 dB	○	○	×
	TGEN1 fade-out step value control (TGEN1_FADE_OUT_ST)	02F3h	390Ah	−1 dB	○	○	×
	TGEN1 fade-out time control (TGEN1_FADE_OUT_TIM)	02F4h	002Bh	43 Sync	○	○	×
	TGEN1 total gain fade control (TGEN1_GAIN_TOTAL_FADE_CONT)	0303h	0000h	Stop	○	○	×
	TGEN1 total gain fade-in step value control (TGEN1_GAIN_TOTAL_FADE_IN_ST)	0304h	4C10h	+1.5 dB	○	○	×
	TGEN1 total gain fade-out step value control (TGEN1_GAIN_TOTAL_FADE_OUT_ST)	0305h	35D9h	−1.5 dB	○	○	×
	TGEN1 execution flag display register (TGEN1_EXFLAG)	CR19 -B2	0b	Stop	○	○	○
FSK generator FSK _GEN	FSK_GEN control register (FGEN_EN)	CR28 -B6	0b	Stop	○	○	○
	FSK output data setting completion flag display register (FGEN_FLAG)	CR17 -B0	0b	Write enable	○	○	○
	FSK output data setting register (FGEN_D[7:0])	CR27	00h	00h	○	○	○
	FSK gain control (FGEN_GAIN)	0230h	0080h	−13.3 dBm0	○	○	×
FSK receiver FSK _DET	FSK_DET control register (FDET_EN)	CR28 -B7	0b	Stop	○	○	○
	FSK receive data read request notification register (FDET_RQ)	CR16 -B0	0b	No request	○	○	○
	FSK receive framing error notification register (FDET_FER)	CR16 -B1	0b	No error	○	○	○
	FSK receive overrun error notification register (FDET_OER)	CR16 -B2	0b	No error	○	○	○
	FSK receive data storage register (FDET_D[7:0])	CR25	00h	00h	○	○	○
	FSK detection level control (FDET_TH)	02B5h	1000h	−39.3 dBm0	○	○	×
	FSK receive mark guard time control (FSK_MK_GT)	02CAh	00F0h	30 ms	○	○	×

Table 14 Internal Data Memory/Related Control Registers (4 of 7)

Function name	Internal data memory/related control register name	Address	Initial value		Change/read enable mode		
			Data	Data value	Initial mode	Inactive	Active
TONE0 detector TONE_DET0	TONE0 detector control register (TDET0_EN)	CR28-B3	0b	Stop	○	○	○
	TONE0 detector detection status register (TONE0_DET)	CR19-B3	0b	Non-detection	○	○	○
	TDET0 main signal detection level control (TDET0_S_TH)	134Ch	1EBBh	−5.3 dBm0	○	○	×
	TDET0 noise detection level control (TDET0_N_TH)	1361h	1EBBh	−5.3 dBm0	○	○	×
	TDET0 detection ON guard timer control (TDET0_ON_TM)	1362h	0028h	5 ms	○	○	×
	TDET0 detection OFF guard timer control (TDET0_OFF_TM)	1363h	0028h	5 ms	○	○	×
	TDET0 detection frequency (TDET0_FREQ)	- - - - h	—	1650Hz	○	○	×
TONE1 detector TONE_DET1	TONE1 detector control register (TDET1_EN)	CR28-B4	0b	Stop	○	○	○
	TONE1 detector detection status register (TONE1_DET)	CR19-B4	0b	Non-detection	○	○	○
	TDET1 main signal detection level control (TDET1_S_TH)	1378h	1EBBh	−5.3 dBm0	○	○	×
	TDET1 noise detection level control (TDET1_N_TH)	138Dh	1EBBh	−5.3 dBm0	○	○	×
	TDET1 detection ON guard timer control (TDET1_ON_TM)	138Eh	0028h	5 ms	○	○	×
	TDET1 detection OFF guard timer control (TDET1_OFF_TM)	138Fh	0028h	5 ms	○	○	×
	TDET1 detection frequency (TDET1_FREQ)	- - - - h	—	2100Hz	○	○	×
DTMF detector DTMF_REC	DTMF detector control register (DTMF_EN)	CR28-B2	0b	Stop	○	○	○
	DTMF code display register (DTMF_CODE[3:0])	CR20-B[3:0]	0000b	0000b	○	○	○
	DTMF detector detection status register (DTMF_DET)	CR20-B4	0b	Non-detection	○	○	○
	DTMF detection level control (DTMF_TH)	018Dh	1000h	−37.0 dBm0	○	○	×
	DTMF detection ON guard timer (DTMF_ON_TM)	01F2h	00A0h	20 ms	○	○	×
	DTMF detection OFF guard timer (DTMF_OFF_TM)	01F4h	00A0h	20 ms	○	○	×
	DTMF noise detection function control (DTMF_NDET_CONT)	01F5h	0002h	Noise detection enabled	○	○	×
Echo canceler	Echo canceler control register (EC_EN)	CR28-B1	0b	Stop	○	○	○
	Echo canceler control (EC_CR)	002Ch	0012h	HD ATT OFF	○	○	○
	GLPAD control (GLPAD_CR)	002Dh	000Fh	+6/−6 dB	○	○	×

Table 14 Internal Data Memory/Related Control Registers (5 of 7)

Function name	Internal data memory/related control register name	Address	Initial value		Change/read enable mode		
			Data	Data value	Initial mode	Inactive	Active
RC0	RC0 control (RC0_CR)	00E6h	0000h	Stop	○	○	○
	RC0 threshold 1 for loss (RC0_TH1)	11C6h	0090h	–40dBm0	○	○	×
	RC0 threshold 2 for loss (RC0_TH2)	11C7h	0051h	–45dBm0	○	○	×
	RC0 threshold 3 for loss (RC0_TH3)	11C8h	002Dh	–50dBm0	○	○	×
	RC0 threshold 4 for loss (RC0_TH4)	11C9h	000Eh	–60dBm0	○	○	×
	RC0 loss value in the case of threshold 1 or 2 for loss (RC0_LOSS1)	11CBh	005Ah	3dB	○	○	×
	RC0 loss value in the case of threshold 2 or 3 for loss (RC0_LOSS2)	11CCh	0040h	6dB	○	○	×
	RC0 loss value in the case of threshold 3 or 4 for loss (RC0_LOSS3)	11CDh	0020h	12dB	○	○	×
	RC0 loss value in the case of threshold 4 or less for loss (RC0_LOSS4)	11CEh	0020h	12dB	○	○	×
	RC0 plus step value (RC0_PL)	11CFh	47CFh	1dB/SYNC	○	○	×
	RC0 minus step value(RC0_MI)	11D0h	3F44h	–0.1dB/SYNC	○	○	×
	RC0 input signal level detecting sensitivity 1 (RC0_POW_C1)	11C4h	3E00h	—	○	○	×
	RC0 input signal level detecting sensitivity 2 (RC0_POW_C2)	11C5h	0200h	—	○	○	×
RC1	RC1 control (RC1_CR)	00E7h	0000h	Stop	○	○	○
	RC1 threshold 1 for loss (RC1_TH1)	11D3h	0090h	–40dBm0	○	○	×
	RC1 threshold 2 for loss (RC1_TH2)	11D4h	0051h	–45dBm0	○	○	×
	RC1 threshold 3 for loss (RC1_TH3)	11D5h	002Dh	–50dBm0	○	○	×
	RC1 threshold 4 for loss (RC1_TH4)	11D6h	000Eh	–60dBm0	○	○	×
	RC1 loss value in the case of threshold 1 or 2 for loss (RC1_LOSS1)	11D8h	005Ah	3dB	○	○	×
	RC1 loss value in the case of threshold 2 or 3 for loss (RC1_LOSS2)	11D9h	0040h	6dB	○	○	×
	RC1 loss value in the case of threshold 3 or 4 for loss (RC1_LOSS3)	11DAh	0020h	12dB	○	○	×
	RC1 loss value in the case of threshold 4 or less for loss (RC1_LOSS4)	11DBh	0020h	12dB	○	○	×
	RC1 plus step value (RC1_PL)	11DCh	47CFh	1dB/SYNC	○	○	×
	RC1 minus step value(RC1_MI)	11DDh	3F44h	–0.1dB/SYNC	○	○	×
	RC1 input signal level detecting sensitivity 1 (RC1_POW_C1)	11D1h	3E00h	—	○	○	×
	RC input signal level detecting sensitivity 2 (RC1_POW_C2)	11D2h	0200h	—	○	○	×

Table 14 Internal Data Memory/Related Control Registers (6 of 7)

Function name	Internal data memory/related control register name	Address	Initial value		Change/read enable mode		
			Data	Data value	Initial mode	Inactive	Active
Dial pulse detector DPDET	Dial pulse detector control register (DPDET_EN)	C43-B0	0b	Stop	○	○	○
	Dial pulse detector detection status register (DP_DET)	CR20-B6	0b	Non-detection	○	○	○
	Dial pulse detection polarity control register (DPDET_POL)	CR43-B1	0b	Positive logic	○	×	×
	Detection dial pulse count display register (DPDET_DATA[7:0])	CR26	00h	Non-detection	○	○	○
	Dial pulse detection ON guard timer control (DPDET_ON_TIM)	13F7h	0028h	5 ms	○	○	×
	Dial pulse detection OFF guard timer control (DPDET_OFF_TIM)	13F8h	0028h	5 ms	○	○	×
	Detection termination timer control (DPDET_DETOFF_TIM)	0743h	03E8h	125 ms	○	○	×
Dial pulse transmitter DPGEN	Dial pulse transmit control register (DPGEN_EN)	CR29-B6	0b	Stop	○	○	○
	Dial pulse count setting register (DPGEN_DATA[3:0])	CR29-B[3:0]	0000b	Stop	○	○	×
	Dial pulse speed control register (DPGEN_PPS)	CR29-B4	0b	10pps	○	○	×
	Dial pulse output polarity control register (DPGEN_POL)	CR29-B5	0b	Positive logic	○	×	×
	Dial pulse make rate control (DPGEN_DUTY)	016Bh	0108h	33 ms	○	○	×
	Dial pulse output termination control (DPGEN_OFF_TIM)	016Dh	03E8h	125 ms	○	○	×
TIMER	Timer control register (TIM_EN)	CR28-B5	0b	Stop	○	○	○
	Timer overflow display register (TMOVF)	CR18-B0	0b	Stop/active	○	○	○
	Timer counter value display (TIM_COUNT) (Read Only data memory)	13BEh	0000h	Count value	○	○	○
	Timer data setting (TIM_DATA)	13BFh	FFFFh	FFFFh max.	○	○	×
Outband control	Outband control (OUTBAND_CONTROL)	021Dh	0000h	Stop	○	×	×
Outband G.729.Adata	Outband G.729.A data (OUTBAND_G729_DAT)	089Fh 08A0h 08A1h 08A2h 08A3h	7852h 80A0h 00FAh C200h 07D6h	—	○	×	×

Table 14 Internal Data Memory/Related Control Registers (7 of 7)

Function name	Internal data memory/related control register name	Address	Initial value		Change/read enable mode		
			Data	Data value	Initial mode	Inactive	Active
Interrupt mask control	Rise mask control						
	CR16 rising edge interrupt mask control (CR16_INTP_MSKCNT)	002Fh	00F8h	Mask setting OFF	○	×	×
	CR18 rising edge interrupt mask control (CR18_INTP_MSKCNT)	0031h	00FEh	Mask setting OFF	○	×	×
	CR19 rising edge interrupt mask control (CR19_INTP_MSKCNT)	0032h	0060h	Mask setting OFF	○	×	×
	CR20 rising edge interrupt mask control (CR20_INTP_MSKCNT)	0034h	0020h	Mask setting OFF	○	×	×
	CR21 rising edge interrupt mask control (CR21_INTP_MSKCNT)	0036h	00F0h	Mask setting OFF	○	×	×
	CR22 rising edge interrupt mask control (CR22_INTP_MSKCNT)	0038h	00F0h	Mask setting OFF	○	×	×
	Fall mask control						
	CR17 falling edge interrupt mask control (CR17_INTN_MSKCNT)	0030h	00FEh	Mask setting OFF	○	×	×
	CR19 falling edge interrupt mask control (CR19_INTN_MSKCNT)	0033h	0060h	Mask setting OFF	○	×	×
	CR20 falling edge interrupt mask control (CR20_INTN_MSKCNT)	0035h	0020h	Mask setting OFF	○	×	×
	CR21 falling edge interrupt mask control (CR21_INTN_MSKCNT)	0037h	00F3h	Mask setting OFF	○	×	×
	CR22 falling edge interrupt mask control (CR22_INTN_MSKCNT)	0039h	00F1h	Mask setting OFF	○	×	×
Speech CODEC decoding control	Decoding output start offset time control (DEC_ONTIM)	0108h	0000h (*1)	0 ms	○	○	×
Internal RAM write	Multiple-word write starting address setting (START_ADDRESS)	00E9h	0000h	0000h	○	○	○

(Remarks)
Initial mode:
Indicates the state in which the initial values of the control register and internal data memory can be changed after power-down reset is released.
Inactive: Indicates the state in which the function indicated by the function name is inactive.
Active: Indicates the state in which the function indicated by the function name is active.
: Related control register

*1: Though 0000h (0 ms) is set as the initial value, be sure to set an offset time of 0001h (0.125 ms) to 0100h (32 ms).

Gain Control

A. Transmit path related gain

A-1: Internal data memory for adjustment of Speech CODEC transmit gain (TXGAIN_SC)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the amount of gain.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

A-2: Internal data memory for adjustment of CODECA transmit gain (TXGAINA)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the amount of gain.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

A-3: Internal data memory for adjustment of CODECB transmit gain (TXGAINB)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the amount of gain.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

B. Receive path related gain

B-1: Internal data memory for adjustment of Speech CODEC receive gain (RXGAIN_SC)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

B-2: Internal data memory for adjustment of CODECA receive gain (RXGAINA)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

B-3: Internal data memory for adjustment of CODECB receive gain (RXGAINB)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

C. Side tone gain

C-1: Internal data memory for adjustment of CODECA side tone gain (STGAINA)
Initial value: 0000h (MUTE)
Use the following calculation expression when changing the side tone gain amount.
Calculation expression: 1000h×GAIN
<Example> Set the gain amount to −20 dB (×0.1)
1000h×0.1 = 019Ah
Upper limit: 0 dB (Data: 1000h)
Lower limit: Approx. −72 dB (Data: 0001h)
: MUTE (Data: 0000h)

C-2: Internal data memory adjustment for CODECB side tone gain (STGAINB)
Initial value: 0000h (MUTE)
Use the following calculation expression when changing the side tone gain amount.
Calculation expression: 1000h×GAIN
<Example> Set the gain amount to −20 dB (×0.1).
1000h×0.1 = 019Ah
Upper limit: 0 dB (Data: 1000h)
Lower limit: Approx. −72 dB (Data: 0001h)
: MUTE (Data: 0000h)

D. PCM related gain

D-1: Internal data memory for adjustment of PCM transmit gain 0 (TXGAIN_PCM0)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. −42 dB (Data: 0001h)
: MUTE (Data: 0000h)

D-2: Internal data memory for adjustment of PCM transmit gain 1 (TXGAIN_PCM1)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. −42 dB (Data: 0001h)
: MUTE (Data: 0000h)

D-3: Internal data memory for adjustment of PCM transmit gain 2 (TXGAIN_PCM2)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

D-4: Internal data memory for adjustment of PCM receive gain 0 (RXGAIN_PCM0)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

D-5: Internal data memory for adjustment of PCM receive gain 1 (RXGAIN_PCM1)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

D-6: Internal data memory for adjustment of PCM receive gain 2 (RXGAIN_PCM2)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

D-7: Internal data memory for adjustment of PCM input time slot selection 1 receive gain (RXGAIN_ITS1)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: Approx. +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: Approx. –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

D-8: Internal data memory for adjustment of PCM input time slot selection 2 receive gain (RXGAIN_ITS2)
Initial value: 0080h (0.0 dB)
Use the following expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h

Upper limit:	Approx. +40 dB	(Data: 3200h)
	: 0 dB	(Data: 0080h)
Lower limit:	Approx. –42 dB	(Data: 0001h)
	: MUTE	(Data: 0000h)

E. Gain related to three-way communication

E-1: Internal data memory for adjustment of CH1 receive gain (RXGAIN_CH1)
A receive gain at single channel operation (SC_EN = 1, DC_EN = 0) in Speech CODEC and a channel 1 receive gain at 2-channel operation (SC_EN-1, DC_EN = 1) can be set.
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h

Upper limit:	About +40 dB	(Data: 3200h)
	: 0 dB	(Data: 0080h)
Lower limit:	About –42 dB	(Data: 0001h)
	: MUTE	(Data: 0000h)

E-2: Internal data memory for adjustment of CH2 receive gain (RXGAIN_CH2)
A channel 2 receive gain at 2-channel operation (SC_EN-1, DC_EN = 1) in Speech CODEC can be set.
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h

Upper limit:	About +40 dB	(Data: 3200h)
	: 0 dB	(Data: 0080h)
Lower limit:	About –42 dB	(Data: 0001h)
	: MUTE	(Data: 0000h)

E-3: Internal data memory for adjustment of CH1 transmit gain (TXGAIN_CH1)
A transmit gain at single channel operation (SC_EN = 1, DC_EN = 0) in Speech CODEC and a channel 1 transmit gain at 2-channel operation (SC_EN-1, DC_EN = 1) can be set.
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h

Upper limit:	About +40 dB	(Data: 3200h)
	: 0 dB	(Data: 0080h)
Lower limit:	About –42 dB	(Data: 0001h)
	: MUTE	(Data: 0000h)

E-4: Internal data memory for adjustment of CH2 transmit gain (TXGAIN_CH2)
A transmit gain of channel 2 at 2-channel operation (SC_EN = 1, DC_EN = 1) in Speech CODEC can be set.
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: About +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: About –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

E-5: Internal data memory for adjustment of CH2 receive→CH1 transmit loop back gain (RX2TX1_GAIN)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: About +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: About –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

E-6: Internal data memory for adjustment of CH1 receive→CH2 transmit loop back gain (RX1TX2_GAIN)
Initial value: 0080h (0.0 dB)
Use the following calculation expression when changing the gain amount.
Calculation expression: 0080h×GAIN
<Example> Set the gain amount to +6 dB (×2).
0080h×2 = 0100h
Upper limit: About +40 dB (Data: 3200h)
: 0 dB (Data: 0080h)
Lower limit: About –42 dB (Data: 0001h)
: MUTE (Data: 0000h)

F. Gain fade control internal data memory (GAIN_FADE_CONT0/GAIN_FADE_CONT1)
This LSI is equipped with the function for attenuating or amplifying (gain fade-in/fade-out function) signals to the required gain when a gain amount is changed, except for STGAINA and STGAINB.

F-1: Gain fade control internal data memory 0 (GAIN_FADE_CONT0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	RXGAIN_ ITS2_FC	RXGAIN_ ITS1_FC	RXGAIN_ PCM1_FC	RXGAIN_ PCM0_FC	TXGAIN_ PCM1_FC	TXGAIN_ PCM0_FC
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	OUT BAND_FC	—	RXGAINB _FC	RXGAINA _FC	RXGAIN _SC_FC	TXGAINB _FC	TXGAINA _FC	TXGAIN _SC_FC
Initial value	0	0	0	0	0	0	0	0

B15-B14: Reserved bits Changing of the initial values is inhibited.

B13: RXGAIN_ITS2_FADECONT control
1: ON (Performs fade-in/fade-out processing when RXGAIN_ITS2 is modified)
0: OFF

B12: RXGAIN_ITS1_FADECONT control
1: ON (Performs fade-in/fade-out processing when RXGAIN_ITS1 is modified)
0: OFF

B11: RXGAIN_PCM1_FADECONT control
1: ON (Performs fade-in/fade-out processing when RXGAIN_PCM1 is modified)
0: OFF

B10: RXGAIN_PCM0_FADECONT control
1: ON (Performs fade-in/fade-out processing when RXGAIN_PCM0 is modified)
0: OFF

B9: TXGAIN_PCM1_FADECONT control
1: ON (Performs fade-in/fade-out processing when TXGAIN_PCM1 is modified)
0: OFF

B8: TXGAIN_PCM0_FADECONT control
1: ON (Performs fade-in/fade-out processing when TXGAIN_PCM0 is modified)
0: OFF

B7: OUTBAND_FADE_CONT control
1: ON (Performs fade-in/fade-out processing at transition to MUTE processing or returning to MUTE processing)
0: OFF

B6: Reserved bit Changing of the initial value is inhibited.

B5: RXGAINB _FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RXGAINB)
0: OFF

B4: RXGAINA _FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RXGAINA)
0: OFF
B3: RXGAIN_SC_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RXGAIN_SC)
0: OFF

B2: TXGAINB _FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of TXGAINB)
0: OFF

B1: TXGAINA _FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of TXGAINA)
0: OFF

B0: TXGAIN_SC_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of TXGAIN_SC)
0: OFF

F-2: Gain fade control internal data memory 1 (GAIN_FADE_CONT1)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	RX1TX2_ GAIN_FC	RX2TX1_ GAIN_FC	RXGAIN_ CH2_FC	RXGAIN_ CH1_FC	TXGAIN_ CH2_FC	TXGAIN_ CH1_FC
Initial value	0	1	0	0	0	0	0	0

B15-B6: Reserved bits Changing of the initial values is inhibited.

B5: RX1TX2_GAIN_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RX1TX2_GAIN)
0: OFF

B4: RX2TX1_GAIN_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RX2TX1_GAIN)
0: OFF

B3: RXGAIN_CH2_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RXGAIN_CH2)
0: OFF

B2: RXGAIN_CH1_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RXGAIN_CH1)
0: OFF

B1: TXGAIN_CH2_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of TXGAIN_CH2)
0: OFF

B0: TXGAIN_CH1_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of TXGAIN_CH1)
0: OFF

F-3: Gain fade control internal data memory 2 (GAIN_FADE_CONT2)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	—	TXGAIN_ PCM2_FC	RXGAIN_ PCM2_FC
Initial value	0	1	0	0	0	0	0	0

B15-B2: Reserved bits Changing of the initial values is inhibited.

B1: TXGAIN_PCM2_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of TXGAIN_PCM2)
0: OFF

B0: RXGAIN_PCM2_FADECONT control
1: ON (Performs fade-in/fade-out processing at modification of RXGAIN_PCM2)
0: OFF

G. Gain fade-in step value control internal data memory (GAIN_FADE_IN_ST)
Initial value: 4C10h (+1.5 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Example> Set the step value to +3 dB.
$10^{(3/20)} \times 16384 = 23143d = 5A67h$
Maximum step value: +6.0 dB (Data: 7FB2h)
Minimum step value: +0.1 dB (Data: 40BEh)

H. Gain fade-out step value control internal data memory (GAIN_FADE_OUT_ST)
Initial value: 35D9h (–1.5 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Value> Set the step value to –3 dB.
$10^{(-3/20)} \times 16384 = 11599d = 2D4Fh$
Maximum step value: –6.0 dB (Data: 2013h)
Minimum step value: –0.1 dB (Data: 3F44h)

(Supplementary information) Step values of fade-in and fade-out can be set separately; however, the parameters that are set are commonly used by all the gain controllers for which fade-in/fade-out processing is enabled.

Tone Generator 0 (TONE_GEN0)

Various parameters of tone generator 0 can be set.

A. Tone frequency control internal data memory
TONE A frequency control (TGEN0_FREQ_A)
Initial value: 0CCDh (400 Hz)
TONE B frequency control (TGEN0_FREQ_B)
Initial value: 007Bh (15 Hz)

For the initial values, tone of 400 Hz is output as TONE A and tone of 15 Hz as TONE B. Use the following calculation expression when changing the frequency.
Calculation expression: f × 8.192 (f: Desired frequency)
<Example> Frequency = 2100 Hz
2100 × 8.192 ≅ 4333h
Upper limit: 3 kHz (Data: 6000h)
Lower limit: 15 Hz (Data: 007Bh)

B. Tone gain control internal data memory
TONE A gain control (TGEN0_GAIN_A)
Initial value: 0080h
TONE B gain control (TGEN0_GAIN_B)
Initial value: 0080h

The initial value of the output level is -13.3 dBm0. Use the following calculation expression when changing the output level.
Calculation expression: 0080h × GAIN
<Example> Reduce the gain amount by 6 dB (×0.5).
0080h × 0.5 = 0040h
Upper limit: +12 dB (Data: 01FEh)
Lower limit: −12 dB (Data: 0020h)

(Note)
The result of multiplication or addition of each tone must not exceed the maximum amplitude 3.17 dBm0.

C. Tone output time control internal data memory (TGEN0_TIM_M0/TGEN0_TIM_M1)

TGEN0 output time control 0 (TGEN0_TIM_M0)
Initial value: 0FA0h (500 ms)

TGEN0 output time control 1 (TGEN0_TIM_M1)
Initial value: 0FA0h (500 ms)

Use the following calculation expression when changing the value.
Calculation expression: T/0.125 (T: Time in ms)
<Example> Time = 200 ms is set.
200/0.125 = 1600d = 0640h
Upper limit: 4095.875 ms (Data: 7FFFh)
Lower limit: 0.125 ms (Data: 0001h)

(Note)
The setting of 0000h (0 ms) is inhibited.

D. Tone total gain control internal data memory (TGEN0_RXABGAIN_TOTAL/TGEN0_RXGAIN_TOTAL)

TGEN0 RXAB side tone total gain control (TGEN0_RXABGAIN_TOTAL)
Initial value: 0080h
TGEN0 RX side tone total gain control (TGEN0_RXGAIN_TOTAL)
Initial value: 0080h

The initial value is 0 dB. Use the following calculation expression when changing the output level.
Calculation expression: 0080h × GAIN
<Example> Reduce the output level by 6 dB.
0080h × 0.5 = 0040h
Upper limit: +40 dB (Data: 3200h)
Lower limit: –40 dB (Data: 0001h)
: MUTE (Data: 0000h)

(Note)
The amplitude must not exceed the maximum amplitude 3.17 dBm0.

E. TGEN0 fade control internal data memory (TGEN0_FADE_CONT)

Initial value: 0000h (Stop)

The fade-in/fade-out function of TGEN0 gain control can be activated by setting "0001h" in this data memory.

0000h: Stops the fade-in/fade-out function.
0001h: Activates the fade-in/fade-out function

(Note)
When using this control function, set a correct fade-out time.

F. TGEN0 fade-in step value control internal data memory (TGEN0_FADE_IN_ST)

Initial value: 47CFh (+1.0 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Example> Set the step value to +3 dB.
$10^{(3/20)} \times 16384 = 23143d = 5A67h$
Maximum step value: +6.0 dB (Data: 7FB2h)
Minimum step value: +0.1 dB (Data: 40BEh)

G. TGEN0 fade-out step value control internal data memory (TGEN0_FADE_OUT_ST)

Initial value: 390Ah (–1.0 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Example> Set the step value to –3 dB.
$10^{(-3/20)} \times 16384 = 11599d = 2D4Fh$
Maximum step value: –6.0 dB (Data: 2013h)
Minimum step value: –0.1 dB (Data: 3F44h)

H. TGEN0 fade-out time control internal data memory (TGEN0_FADE_OUT_TIM)

Initial value: 002Bh (43 Sync)
Use the following calculation expression when changing the fade-out time.
Calculation expression: 43 dB/"fade-out step value" dB
<Example> The step value is 2 dB.
43/2 = 22d = 16h
Upper limit: 430 Sync (Data: 01AEh)
Lower limit: 8 Sync (Data: 0008h)

(Note)
Do not set 0000h since the value is inhibited.
The condition, fade-out time<TIM_M0,TIM_M1, must be observed.

(Supplementary information) Step values can be set individually; however, the parameters that are set are commonly used for TONE_A and TONE_B. In addition, the operation control and stop time parameters are commonly used for TONE_A and TONE_B.

I. TGEN0 total gain fade control internal data memory (TGEN0_GAIN_TOTAL_FADE_CONT)

Initial value: 0000h (Stop)

The fade-in/fade-out function of the RXAB side/RX side total gain control can be activated by setting "0001h" in this data memory.

0000h: Stops the fade-in/fade-out function.
0001h: Activates the fade-in/fade-out function.

J. TGEN0 total gain fade-in step value control internal data memory (TGEN0_GAIN_TOTAL_FADE_IN_ST)

Initial value: 4C10h (+1.5 dB)

Use the following calculation expression when changing step amount X.

Calculation expression: $10^{(X/20)} \times 16384$

<Example> Set the step value to +3 dB.

$10^{(3/20)} \times 16384 = 23143d = 5A67h$

Maximum step value: +6.0 dB (Data: 7FB2h)

Minimum step value: +0.1 dB (Data: 40BEh)

K. TGEN0 total gain fade-output step value control internal data memory (TGEN0_GAIN_TOTAL_FADE_OUT_ST)

Initial value: 35D9h (−1.5 dB)

Use the following calculation expression when changing step amount X.

Calculation expression: $10^{(X/20)} \times 16384$

<Example> Set the step value to –3 dB.

$10^{(-3/20)} \times 16384 = 11599d = 2D4Fh$

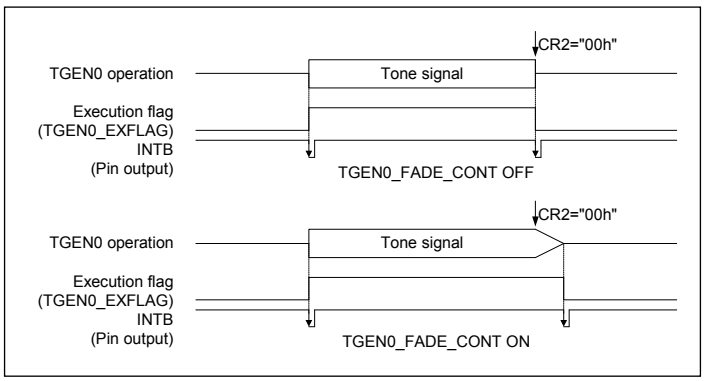
Maximum step value: −6.0 dB (Data: 2013h)

Minimum step value: −0.1 dB (Data: 3F44h)

(Supplementary information) Step values can be set individually. However, the parameters that are set are commonly used for TGEN0_RXABGAIN_TOTAL and TGEN0_RXGAIN_TOTAL.
The operation control is also commonly used for TGEN0_RXABGAIN_TOTAL and TGEN0_RXGAIN_TOTAL.

L. TGEN0 execution flag display register (TGEN0_EXFLAG)

TGEN0_EXFLAG is set to "1" while the tone generator is active. (Initial value "0": Inactive)



Tone Generator 1 (TONE_GEN1)

Various parameters of tone generator 1 can be set.

A. Tone frequency control internal data memory
TONE C frequency control (TGEN1_FREQ_C)
Initial value: 0CCDh (400 Hz)
TONE D frequency control (TGEN1_FREQ_D)
Initial value: 007Bh (15 Hz)

As the initial values, a tone of 400 Hz is output for TONE C and a tone of 15 Hz is output for TONE D. Use the following calculation expression when changing the frequency.
Calculation expression: f × 8.192 (f: Frequency to be set)
<Example> Frequency = 2100 Hz
2100 × 8.192 ≅ 4333h
Upper limit: 3kHz (Data: 6000h)
Lower limit: 15Hz (Data: 007Bh)

B. Tone gain control internal data memory
TONE C gain control (TGEN1_GAIN_C)
Initial value: 0080h
TONE D gain control (TGEN1_GAIN_D)
Initial value: 0080h

The initial value of the output level is −13.3 dBm0. Use the following calculation expression when changing the output level.
Calculation expression: 0080h × GAIN
<Example> Reduce the gain amount by 6 dB (× 0.5).
0080h × 0.5 = 0040h
Upper limit: +12 dB (Data: 01FEh)
Lower limit: −12 dB (Data: 0020h)
(Note)
The result of multiplication or addition of each tone must not exceed the maximum amplitude 3.17 dBm0.

C. Tone output time control internal data memory (TGEN1_TIM_M0/TGEN1_TIM_M1)

TGEN1 output time control 0 (TGEN1_TIM_M0)
Initial value: 0FA0h (500 ms)
TGEN1 output time control 1 (TGEN1_TIM_M1)
Initial value: 0FA0h (500 ms)

Use the following calculation expression when changing the value.
Calculation expression : T/0.125 (T: Time in ms)
<Example> Time = 200 ms is set.
200/0.125 = 1600d = 0640h
Upper limit: 4095.875 ms (Data: 7FFFh)
Lower limit: 0.125 ms (Data: 0001h)

(Note)
Do not set 0000h (0 ms) as the time since the value is inhibited.

D. Tone total gain control internal data memory (TGEN1_RXABGAIN_TOTAL/TGEN1_TXGAIN_TOTAL)

TGEN1 RXAB side tone total gain control (TGEN1_RXABGAIN_TOTAL)
Initial value: 0080h
TGEN TX side tone total gain control (TGEN1_TXGAIN_TOTAL)
Initial value: 0080h

The initial value is 0 dB. Use the following calculation expression when changing the output level.
Calculation expression: 0080h × GAIN
<Example> Reduce the output level by 6 dB.
0080h × 0.5 = 0040h

Upper limit	: +40 dB	(Data: 3200h)
Lower limit	: –40 dB	(Data: 0001h)
	: MUTE	(Data: 0000h)

(Note)
The amplitude must not exceed the maximum amplitude 3.17 dBm0.

E. TGEN1 fade control internal data memory (TGEN1_FADE_CONT)
Initial value: 0000h (Stop)
By setting "0001h" in this data memory, the fade-in/fade-output function of TGEN1 gain control can be activated.

0000h: Stops the fade-in/fade-out function.
0001h: Activates the fade-in/fade-out function.

(Note)
When using this control function, set a correct fade-out time.

F. TGEN1 fade-in step value control internal data memory (TGEN1_FADE_IN_ST)
Initial value: 47CFh (+1.0 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Example> Set the step value to +3 dB.
$10^{(3/20)} \times 16384 = 23143d = 5A67h$
Maximum step value: +6.0 dB (Data: 7FB2h)
Minimum step value: +0.1 dB (Data: 40BEh)

G. TGEN1 fade-out step value control internal data memory (TGEN1_FADE_OUT_ST)
Initial value: 390Ah (–1.0 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Example> Set the step value to –3 dB.
$10^{(-3/20)} \times 16384 = 11599d = 2D4Fh$
Maximum step value: –6.0 dB (Data: 2013h)
Minimum step value: –0.1 dB (Data: 3F44h)

H. TGEN1 fade-out time control internal data memory (TGEN1_FADE_OUT_TIM)
Initial value: 002Bh (43 Sync)
Use the following calculation expression when changing the fade-out time.
Calculation expression: 43 dB/"fade-out step value" dB
<Example> The step value is 2 dB.
43/2 = 22d = 16h
Upper limit: 430 Sync (Data: 01AEh)
Lower limit: 8 Sync (Data: 0008h)

(Note)
Do not set 0000h since the value is inhibited.
The condition, fade-out time<TIM_M0, TIM_M1, must be observed.

(Supplementary information) Step values can be set individually. However, the parameters that are set are commonly used for TONE_C and TONE_D. The operation control and stop time parameters are also commonly used for TONE_C and TONE_D.

I. TGEN1 total gain fade control internal data memory (TGEN1_GAIN_TOTAL_FADE_CONT)
Initial value: 0000h (Stop)
By setting "0001h" in this data memory, the fade-in/fade-out of RXAB side/TX side total gain control can be activated.

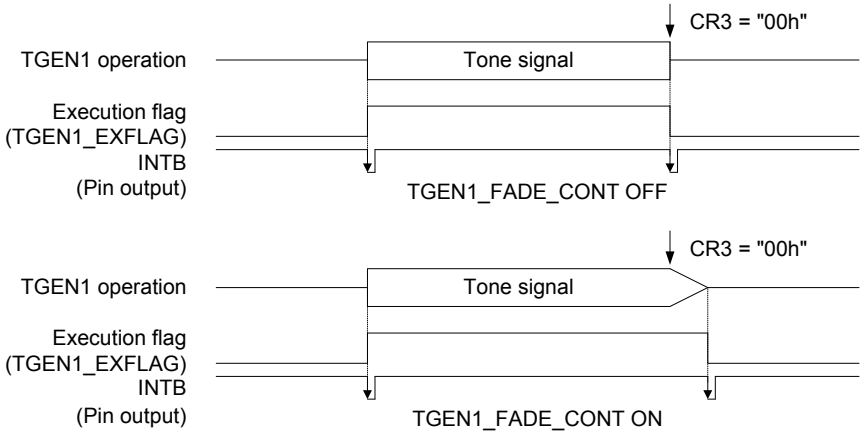
0000h: Stops the fade-in/fade-out function.
0001h: Activates the fade-in/fade-out function.

J. TGEN1 total gain fade-in step value control internal data memory (TGEN1_GAIN_TOTAL_FADE_IN_ST)
Initial value: 4C10h (+1.5 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Example> Set the step value to +3 dB.
$10^{(3/20)} \times 16384 = 23143d = 5A67h$
Maximum step value: +6.0 dB (Data: 7FB2h)
Minimum step value: +0.1 dB (Data: 40BEh)

K. TGEN1 total gain fade-out step value control internal data memory
(TGEN1_GAIN_TOTAL_FADE_OUT_ST)
Initial value: 35D9h (–1.5 dB)
Use the following calculation expression when changing step amount X.
Calculation expression: $10^{(X/20)} \times 16384$
<Example> Set the step value to –3 dB.
$10^{(-3/20)} \times 16384 = 11599d = 2D4Fh$
Maximum step value: -6.0 dB (Data: 2013h)
Minimum step value: -0.1 dB (Data: 3F44h)

(Supplementary information) Step values can be set individually. However, the parameters that are set are commonly used for TGEN1_RXABGAIN_TOTAL and TGEN1_TXGAIN_TOTAL. The operation control parameter is also commonly used for TGEN1_RXABGAIN_TOTAL and TGEN1_TXGAIN_TOTAL.

L. TGEN1 execution flag display register (TGEN1_EXFLAG)
TGEN1_EXFLAG is set to "1" while the tone generator is active. (Initial value "0": Inactive)



FSK Generator (FSK_GEN)

The FSK generator (FSK_GEN) modulates the frequency of the data that was set in the control register and outputs the result to VFRO0 and VFRO1. Table 15 shows the specification and Figure 55 shows the block diagram of the FSK generator.
The FSK generator comprises a FSK signal generation section that can perform buffering of up to three words, a data setting register, and a gain adjustment section. When FGEN_EN is set o "1", the FSK generator starts operation and transmits a mark bit ("1") continuously. When transmitting data, set the first transmit data in FGEN_D[7:0] and set FGEN_FLAG to "1". When FGEN_FLGA is set to "1", the transmit data of FGEN_D[7:0] is transferred to the internal buffer if there is free internal buffer space, and FGEN_FLAG is cleared to "0". ST (Start Bit "0") and SP (Stop Bit "1") are added to the data that was transferred to the internal buffer and is output in the transmit sequence shown in Figure 56. When setting the next transmit data, make sure that FGEN_FLAG is set to "0". A mark bit ("1") is sent continuously while there is no data waiting to be transmitted in the internal buffer of the FGEN signal generation section.
The internal buffer of the FSK signal generation section is structured in three levels and data of up to four words can be buffered including the FSK output data setting register FGEN_D[7:0]. To terminate transmission, set FGEN_EN to "0" while FGEN_FLAG is set to "0". After transmission of the data that has been set in FGEN_D[7:0] by the time that FGEN_EN is set to "0", the FSK generator stops. When FGEN_EN is set to "0" during consecutive transmission of a mark bit ("1") and no data is waiting to be transmitted, the FSK generator stops after output a mark bit ("1") for a period of up to one bit. Figure 57 shows the transmission start and stop timing and Figure 58 shows an example of control. The FSK generator output level can be changed using the internal data memory (FGEN_GAIN).

Table 15 FSK Generator Specification

Modulation method	Frequency modulation method
Synchronization mode	Start-stop synchronization mode
Transfer rate	1200bps
Output frequency	1300 Hz (Data "1" mark)
	2100 Hz (Data "0" space)
Data setting register	8-bit (FGEN_D[7:0])
Output level	−13.3 dBm0 (Initial value; gain adjustable)

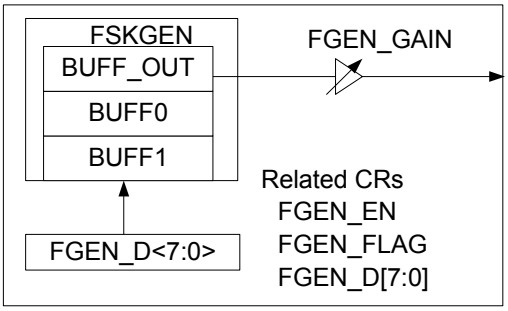


Figure 55 FSK Generator Block

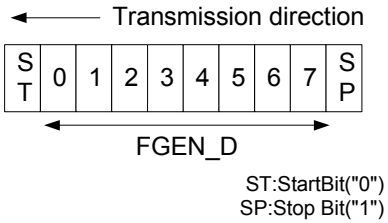


Figure 56 Data Transmission Sequence

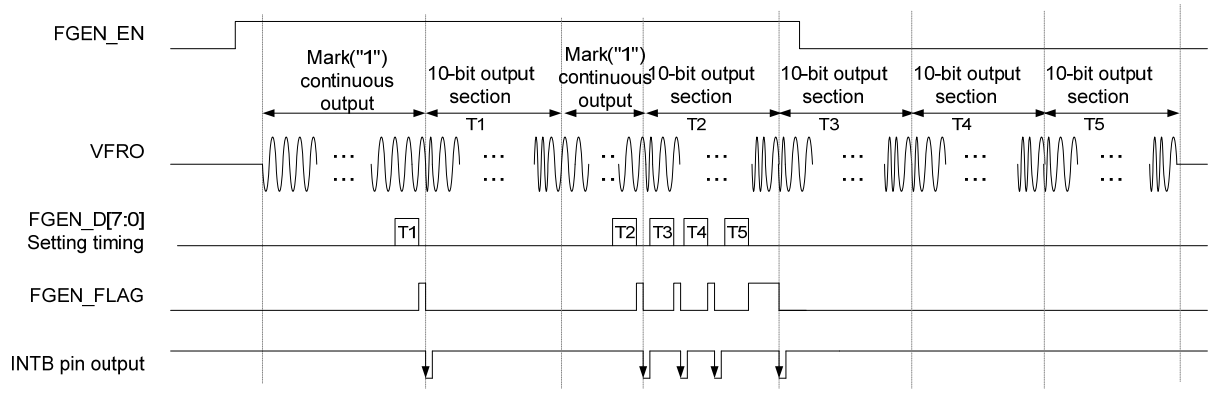


Figure 57 FSK Data Transmission Start and Stop Timing (50-bit Transmission)

(Remarks)
It is recommended to operate the FSK generator with detection circuits made inactive in order to avoid the occurrence of interrupts due to some other factors.

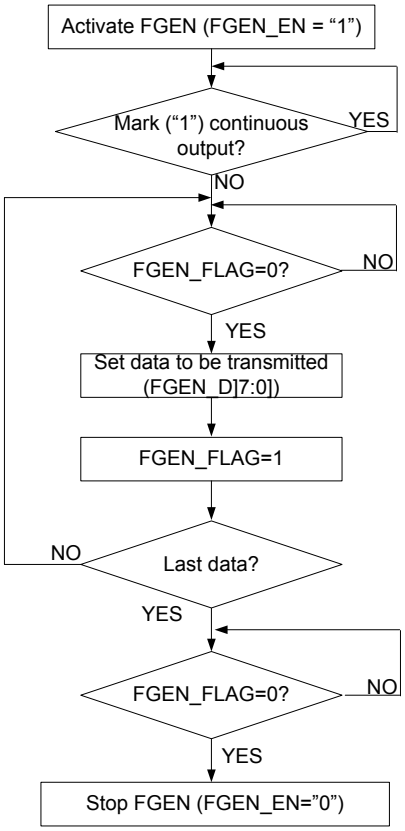


Figure 58 FSK Output Control Method

A. FSK_GEN control register (FGEN_EN)
0: Stops FSK_GEN (Initial value)
1: Activates FSK_GEN

B. FSK output data setting completion flag display register (FGEN_FLAG)
After writing data in the FSK output data setting register (FGEN_D[7:0]), set this bit to "1". When the data is stored in the internal buffer of the FSK signal generation section, this bit is automatically cleared to "0" and an interrupt is generated. Do not write data to this register while this bit is "1".

C. FSK output data setting register (FGEN_D[7:0])
Initial value: 00h

D. FSK gain control internal data memory (FGEN_GAIN)
Initial value: 0080h
The initial value of the output level is –13.3 dBm0. Use the following calculation expression when changing the output level.
Calculation expression: 0080h × GAIN
<Example> Reduce the output level by 6 dB.
0080h × 0.5 = 0040h
Upper limit: +40 dB (Data: 3200h)
Lower limit: –40 dB (Data: 0001h)

(Note) The amplitude must not exceed the maximum amplitude 3.17 dBm0.

FSK Receiver (FSK_DET)

Table 16 shows the specification of the FSK receiver and Figure 59 shows the operation outline.

Activation and receive operation

The FSK receiver is enabled when the FSK_DET control register (FDET_EN) is set to "1".
When receiving FSK data (10 bits), the FSK receiver stores the data bit (8 bits) excluding ST (Start Bit "0") and SP (Stop Bit "1") in the FSK receive data storage register FDET_D[7:0] and sets the FSK receive data read request notification register (FDET_RQ) to "1". When FDET_RQ is set to "1", read the receive data from FDET_D[7:0] and clear the read request by writing "0" to FDET_RQ.

Buffering function

The FSK receiver is equipped with an internal buffer that can buffer receive data of up to three words, or four words if FDET_D[7:0] is included. When new FSK data is received while FDET_RQ = 1, the receive data is transferred to the internal buffer.

Overrun error

When FSK data of 1 word is received while the internal buffer already contains receive data of three words, the contents are updated by shifting 1 word of receive data in the internal buffer and the initial receive data is deleted. The occurrence of an overrun error is notified to the MCU side at the next read request (FDET_RQ = 1) by setting the FSK receive overrun error notification register (FDET_OER) to "1".

Framing error

When SP (Stop Bit "1") is not detected correctly, the FSK receiver notifies an error when issuing the receive data read request (FDET_RQ = 1), by setting the FSK receive framing error notification register (FDET_FER) to "1". Note that FDET_FER is not set to "1" when receive data from which SP (Stop Bit "1") was not detected is overwritten due to the occurrence of overrun while that data is stored in the internal buffer.

Clearing an error

Be sure to clear two error statuses (FDET_FER = 1 and FDET_OER = 1) by writing FDET_FER = 0 and FDET_OER = 0 when clearing (writing FDET_RQ = 0) the FSK receive data read request notification register.

Stopping

The FSK receiver can be stopped by setting the FSK_DET control register (FDET_EN) to "0".
An interval of 500usec or more is required before reactivating the FSK receiver after stopping it.
When the FSK receiver is stopped while FSK receive data read is being requested (FDET_RQ = 1), FDET_RQ, FDET_FER, and FDET_OER are all cleared to "0". When the FSK receiver is stopped, FDET_D[7:0] is cleared to 00h.

Table 16 FSK Receiver Specification

Modulation method	Frequency modulation method
Synchronization mode	Start-stop synchronization mode
Transfer rate	1200bps
Detection frequency	1300Hz (Data "1" mark)
	2100Hz (Data "0" space)
Receive data storage register	8-bit (FDET_D[7:0])
Detection level	–39.3 dBm0 (Initial value, adjustable)

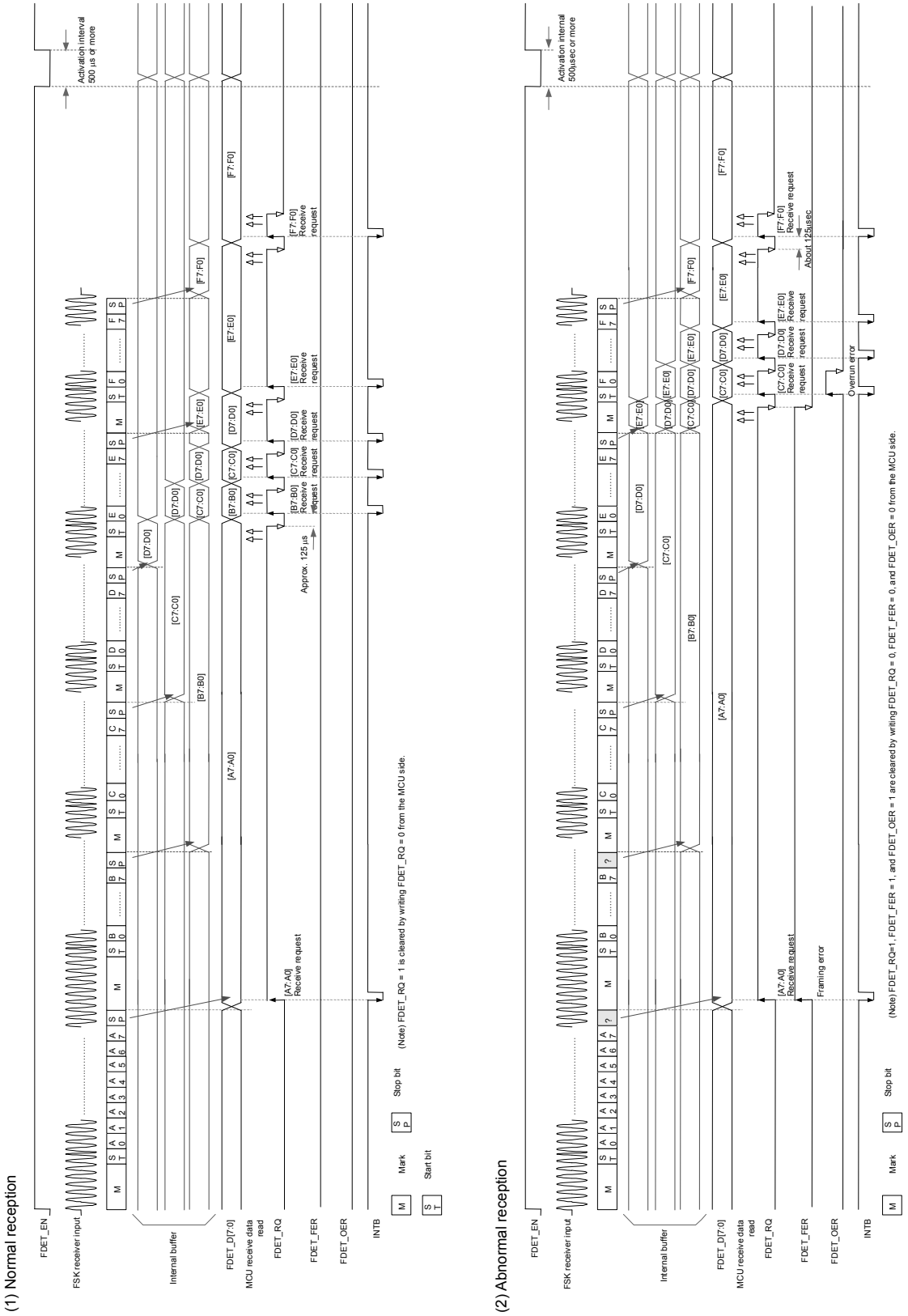


Figure 59 FSK Receive Timing

A. FSK_DET control register (FDET_EN)
0: Stops FSK_DET (Initial value)
1: Activates FSK_DET

B. FSK receive data read request notification register (FDET_RQ)
0: No read request issued (Initial value)
1: Read request issued

C. FSK receive framing error notification register (FDET_FER)
0: No framing error occured (Initial value)
1: Framing error occured

D. FSK receive overrun error notification error (FDET_OER)
0: No overrun error occured (Initial value)
1: Overrun error occured

E. FSK receive data storage register (FDET_D[7:0])
Initial value: 00h

F. FSK receiver detection level control internal data memory (FDET_TH)
Initial value: 1000h
The initial value of the detection level is –39.3 dBm0. Use the following calculation expression when changing the detection level.
Calculation expression: $4096 \times (1/10^{(X/20)})$
<Example> Increase the detection level by 6 dB.
$4096 \times (1/10^{(6/20)}) = 2053d = 0805h$
Upper limit: +12 dB (Data: 0405h)
Lower limit: −12dB (Data: 3FB2h)

G. FSK receive mark guard time control internal data memory (FDET_MK_GT)
Initial value: 00F0h (30 ms)
After the FSK receiver makes a transition from an FSK signal non-detection state to a detection state, that is, after activation of the FSK receiver for example, receive data fetching starts after a mark bit is detected in succession for a specified period (mark guard time).
Use the following calculation expression when changing the mark guard time.
Calculation expression: (Mark guard time)/0.125 ms
<Example> Set the mark guard to 60 ms.
60/0.125 = 01E0h
Upper limit: 4095.875 ms (Data: 7FFFh)
Lower limit: 0 ms (Data: 0000h)

TONE0 Detector (TONE_DET0)

The TONE0 detector comprises a main signal detection section that detects the signal of an appropriate frequency, a noise detection section that detects signals other than an appropriate frequency, an ON guard timer, and an OFF guard timer. The detector detects single-tone signals of 1650 Hz that are input from AIN.
The TONE0 detector is activated when the control register TDET0_EN is set to "1". When a tone is detected (main signal detection and noise non-detection state), the control register TONE0_DET is set to "1" and when a tone is not detected or TDET0_EN is set to "0", TONE0_DET is set to "0".
A detection time can be adjusted by the ON guard timer and OFF guard timer. In addition, main signal detection and noise detection level adjustment are possible. Both guard timers are initially set to 5 ms. The initial value of the detection levels is –5.3 dBm0 for both main signal detection level and noise detection level. Figure 60 shows the tone detection timing.

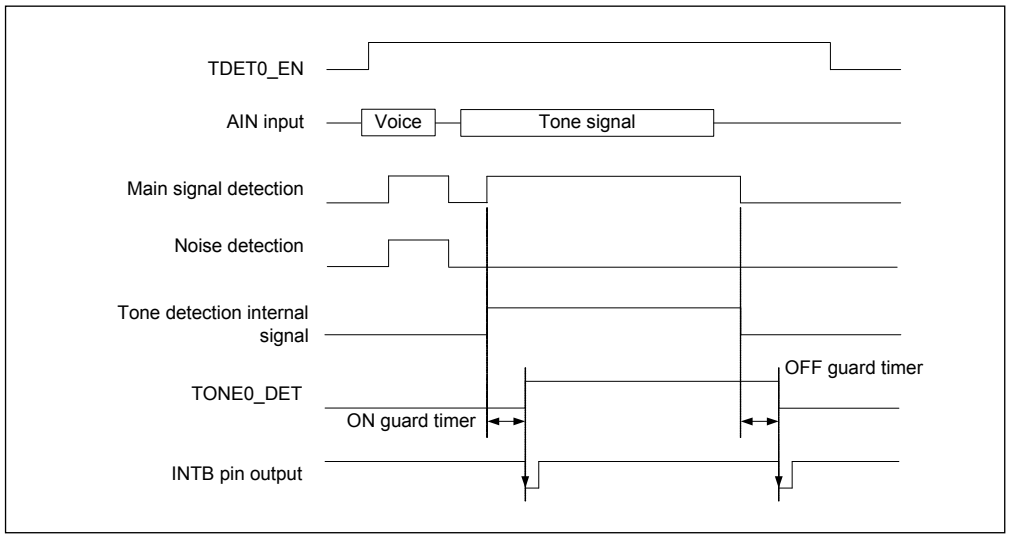


Figure 60 Tone Detection Timing

A. : TONE0 detection control register (TDET0_EN)
0: Stops TONE_DET0 (Initial value)
1: Activates TONE_DET0

B. : TONE0 detector detection status register (TONE0_DET)
0: Non-detection (Initial value)
1: Detection

C. TDET0 main signal detection level control internal data memory (TDET0_S_TH)
Initial value: 1EBBh (–5.3 dBm0)
Use the following calculation expression when setting detection level X.
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Detection level –5.3 dBm0
$10^{((-5.3-3.17)/20)} \times 2/PI \times 32768 = 7867d = 1EBBh$
Upper limit: 3.17 dBm0 (Data: 517Dh)
: –5.3 dBm0 (Data: 1EBBh)
Lower limit: –35 dBm0 (Data: 0102h)

* PI = 3.14……

D. TDET0 noise detection level control internal data memory (TDET0_N_TH)
Initial value: 1EBBh (–5.3 dBm0)
Use the following calculation expression when setting detection level X.
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Detection level -5.3 dBm0
$10^{((-5.3-3.17)/20)} \times 2/PI \times 32768 = 7867d = 1EBBh$
Upper limit: 3.17 dBm0 (Data: 517Dh)
: –5.3 dBm0 (Data: 1EBBh)
Lower limit: –30 dBm0 (Data: 01CAh)

When stopping the noise detection function, write 7FFFh in the internal data memory (TDET0_N_TH) described above.

E. TDET0 detection ON guard timer internal data memory (TDET0_ON_TM)
Initial value: 0028h (5 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: “Guard timer value” ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h
Upper limit: 4095.875 ms (Data: 7FFFh)
: 5 ms (Data: 0028h)
Lower limit: 0.125 ms (Data: 0001h)

F. TDET0 detection OFF guard timer internal data memory (TDET0_OFF_TM)
Initial value: 0028h (5 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: “Guard timer value” ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h
Upper limit: 4095.875 ms (Data: 7FFFh)
: 5 ms (Data: 0028h)
Lower limit: 0.125 ms (Data: 0001h)

G. TDET0 detection frequency control internal data memory (TDET0_FREQ)
Initial value: –
A detection frequency can be changed. When changing the frequency, contact ROHM's responsible sales person.

TONE1 Detector (TONE_DET1)

The TONE1 detector comprises a main signal detection section that detects the signal of an appropriate frequency, a noise detection section that detects signals other than an appropriate frequency, an ON guard timer, and an OFF guard timer. The detector detects single-tone signals of 2100Hz that are input from AIN.
The TONE1 detector is activated when the control register TDET1_EN is set to "1". When a tone is detected (main signal detection and noise non-detection state), the control register TONE1_DET is set to "1" and when a tone is not detected or TDET1_EN is set to "0", TONE1_DET is set to "0".
A detection time can be adjusted by the ON guard timer and OFF guard timer. In addition, main signal detection and noise detection level adjustment are possible Both guard timers are initially set to 5 ms. The initial value of the detection levels is –5.3 dBm0 for both main signal detection level and noise detection level. Figure 61 shows the tone detection timing.

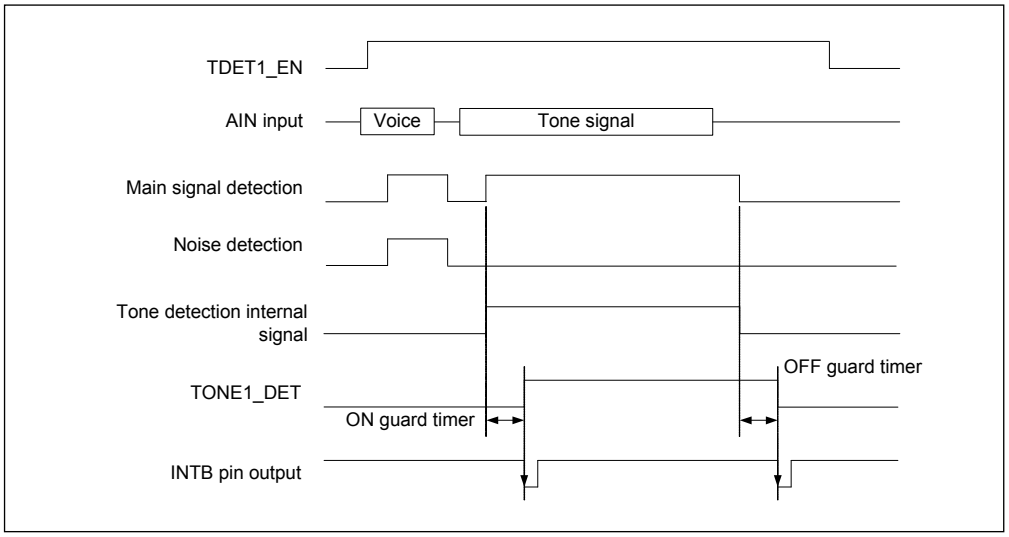


Figure 61 Tone Detection Timing

A. : TONE1 detection control register (TDET1_EN)
0: Stops TONE_DET1 (Initial value)
1: Activates TONE_DET1

B. : TONE1 detector detection status register (TONE1_DET)
0: Non-detection (Initial value)
1: Detection

C. TDET1 main signal detection level control internal data memory (TDET1_S_TH)
Initial value: 1EBBh (–5.3 dBm0)
Use the following calculation expression when setting detection level X.
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Detection level –5.3 dBm0
$10^{((-5.3-3.17)/20)} \times 2/PI \times 32768 = 7867d = 1EBBh$
Upper limit: 3.17 dBm0 (Data: 517Dh)
: –5.3 dBm0 (Data: 1EBBh)
Lower limit: –35 dBm0 (Data: 0102h)

D. TDET1 noise detection level control internal data memory (TDET1_N_TH)
Initial value: 1EBBh (–5.3 dBm0)
Use the following calculation expression when setting the detection level to X.
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Detection level –5.3 dBm0
$10^{((-5.3-3.17)/20)} \times 2/PI \times 32768 = 7867d = 1EBBh$
Upper limit: 3.17 dBm0 (Data: 517Dh)
: –5.3 dBm0 (Data: 1EBBh)
Lower limit: –30 dBm0 (Data: 01CAh)

When stopping the noise detection function, write 7FFFh in the internal data memory (TDET1_N_TH) described above.

E. TDET1 detection ON guard timer internal data memory (TDET1_ON_TM)
Initial value: 0028h (5 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: “Guard timer value” ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h
Upper limit: 4095.875 ms (Data: 7FFFh)
: 5 ms (Data: 0028h)
Lower limit: 0.125 ms (Data: 0001h)

F. TDET1 detection OFF guard timer internal data memory (TDET1_OFF_TM)
Initial value: 0028h (5 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: “Guard timer value” ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h
Upper limit: 4095.875 ms (Data: 7FFFh)
: 5 ms (Data: 0028h)
Lower limit: 0.125 ms (Data: 0001h)

G. TDET1 detection frequency control internal data memory (TDET1_FREQ)
Initial value: –
A detection frequency can be changed. When changing the frequency, contact ROHM's responsible sales person.

DTMF Detector (DTMF_REC)

The DTMF detector detects DTMF signals that are input from AIN.
The DTMF detector comprises a DTMF section that detects DTMF signals, a noise detection section that detects signals other than DTMF signals, an ON guard timer, and an OFF guard timer.
The DTMF detector is activated when the control register DTMF_EN is set to "1". When a valid DTMF signal is detected (detecting a DTMF signal without noise signal), DTMF_DET is set to "1" and the receive code is stored in DTMF_CODE3–0. When a DTMF signal is not detected and DTMF_EN is "0", DTMF_DET is set to"0" and DTMF_CODE3– 0 are set to "0000".
Figure 62 shows DTMF detection timing. The detection time and detection level can be adjusted by the ON guard timer and the OFF guard timer. The initial values of both guard timers are 20 ms. The initial value of the detection level is –37.0 dBm0.

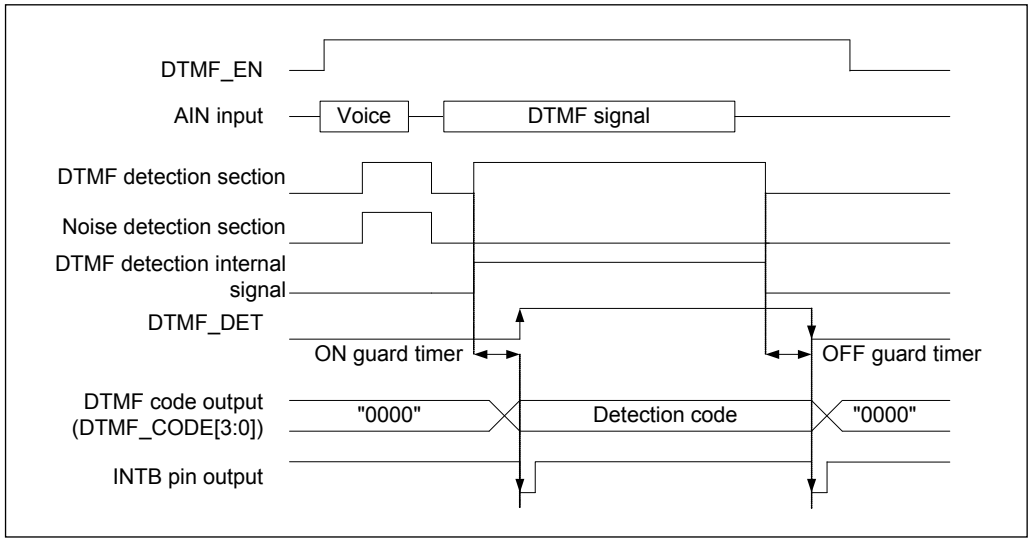


Figure 62 DTMF Detection Timing

A. : DTMF detector control register (DTMF_EN)
0: Stops the DTMF detection function (Initial value)
1: Activates the DTMF detection function

B. : DTMF code display register (DTMF_CODE[3:0])
A valid code is stored in this register for the time period during which DTMF signals are detected (DTMF detector detection status register DTMF_DET = "1") when the DTMF detector control register (DTMF_EN) is set to "1". When DTMF signals are not detected (DTMF_DET = "0"), "0000" is output. (Initial value:0000b)

C. : DTMF detector detection status register (DTMF_DET)
0: Non-detection (Initial value)
1: Detection

D. DTMF detection level control internal data memory (DTMF_TH)
Initial value: 1000h (–37.0 dBm0)
Use the following calculation expression when changing the initial value of the detection level.
Calculation expression: 1000h × 1/GAIN
<Example> Increase the detection level by 6 dB.
1000h × 0.5 = 0800h
Upper limit: +12 dB (Data: 0405h)
Lower limit: –12 dB (Data: 3FB2h)

(Note)
The detection level that is set in the above data memory (DTMF_TH) is used as the common detection level for both the DTMF detection section and the noise detection section.

E. DTMF detection ON guard timer internal data memory (DTMF_ON_TM)
Initial value: 00A0h (20 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: "Guard timer value" ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h
Upper limit: 4095.875 ms (Data: 7FFFh)
: 5 ms (Data: 0028h)
Lower limit: 0.125 ms (Data: 0001h)

F. DTMF detection OFF guard timer internal data memory (DTMF_OFF_TM)
Initial value: 00A0h (20 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: "Guard timer value" ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h
Upper limit: 4095.875 ms (Data: 7FFFh)
: 5 ms (Data: 0028h)
Lower limit: 0.125 ms (Data: 0001h)

G. DTMF noise detection function control internal data memory (DTMF_NDET_CONT)
Initial value: 0002h (noise detection function is enabled)
By writing 000h in this internal data memory, the noise detection function of the DTMF detector is disabled.

(Note)
If DTMF signals are changed to other codes in succession during detection of DTMF signals, the receive codes may change while DTMF_DET is "1", causing an interrupt.

Echo Canceler

Figure 63 shows an echo canceler block diagram.
The echo canceler, which has a delay time of 32 ms, is activated by setting the echo canceler control register (EC_EN) to "1". The operation of the echo canceler is specified mainly in the internal data memories EC_CR and GLPAD_CR.

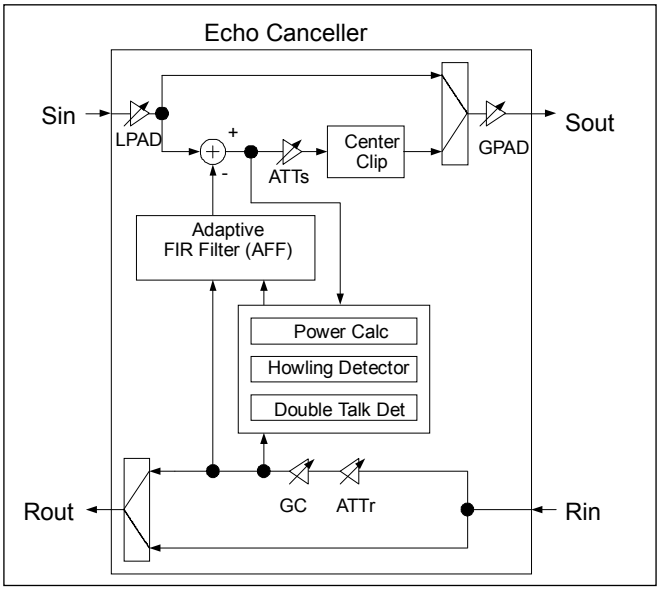


Figure 63 Echo Canceler Block Diagram

A. Echo canceler control register (EC_EN)
0: Stops the echo canceler function: Passes through the echo canceler. (Initial value)
1: Activates the echo canceler function.

B. Echo canceler control internal data memory (EC_CR)
Initial value: 0012h

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	THR	—	HLD	HDB	CLP	—	ATTB	GC
Initial value	0	0	0	1	0	0	1	0

B15-B8: Reserved bits Changing of the initial values is inhibited.

B7: Through mode control
1: Through mode
0: Normal mode (echo cancellation operation)
Rin data and Sin data are output to Rout and Sout in through mode, retaining the echo coefficients. In through mode, the functions of HLD, HDB, CLP, ATTB, and GC are disabled.

B6: Reserved bit Changing of the initial value is inhibited.

B5: Coefficient update control
1: Fixes the coefficient
0: Updates the coefficient
This bit specifies whether the coefficient of the echo canceler adaptive FIR filter (AFF) is updated. This function is enabled when THR is set to a normal mode.

B4: Howling detector control
1: OFF
0: ON
This function detects howling that can occur in hands-free acoustic systems and eliminates howling. This function is enabled when THR is set to a normal mode.

B3: Center clip control
1: ON
0: OFF
When Sout output of the echo canceler is −57 dBm0 or less, this center clip function fixes the Sout output to the positive minimum value forcibly. This function is enabled when THR is set to a normal mode.

B2: Reserved bit Changing of the initial value is inhibited.

B1: Attenuator control
1: ATT OFF
0: ATT ON
Use this function to select ON/OFF of the ATT function that prevents howling through the attenuators (ATTs and ATTr) provided for Rin input and Sout output of the echo canceler. When a signal is input to Rin only, ATT(ATTs) of Sout is inserted. When a signal is input to Sin only or input to both Sin and Rin, ATT(ATTr) of Rin input is inserted. The ATT value is approx. 6 dB for both ATTs and ATTr. This function is enabled when THR is set to a normal mode.

B0: Gain controller control
1: OFF
0: ON
Use this function to select ON/OFF of the gain control function that uses the attenuator (GC) provided for Rin input of the echo canceler. The gain control function is for suppressing overinput at an Rin input level and howling.
When the peak of an input signal to the attenuator (GC) is −10 dBm0 or less, no output of the attenuator is attenuated.
When the peak of an input signal to the attenuator (GC) is in the range of −10 dBm0 to approx. −1.5 dBm0, the output of the attenuator is attenuated to approx.−10 dBm0.
When the peak of an input signal to the attenuator (GC) is −1.5 dBm0 or more, the output of the attenuator is attenuated by approx. 8.5 dBm0. This function is enabled when THR is set to a normal mode.

C. GLPAD control internal data memory (GLPAD_CR)
Initial value: 000Fh
GLPAD control memory in the echo canceler

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	GPAD2	GPAD1	LPAD2	LPAD1
Initial value	0	0	0	0	1	1	1	1

B15-B4: Reserved bits Changing of the initial values is inhibited.

B3 , 2: Output level control
GPAD level control of echo canceler output gain
(0,1): +18 dB
(0,0): +12 dB
(1,1): + 6 dB
(1,0): 0 dB

B1, 0: Input level control
LPAD level control of echo canceler input loss
(0,1): –18 dB
(0,0): –12 dB
(1,1): – 6 dB
(1,0): 0 dB

D. Notes on using the echo canceler

D-1
Make sure that echo signal saturation or waveform distortion will not be caused by an external amplifier in the echo path. Saturation or waveform distortion deteriorates echo attenuation.

D-2
The E.R.L. (Echo Return Loss) level should be more than 0dB. In particular, care must be taken when TXGAINA, TXGAINB, RXGAINA, or RXGAINB is changed. When the E.R.L. level is 0dB or less, it is recommended to use the GLPAD function. If the E.R.L. level is 0 dB or less, echo attenuation performance can be degraded.
E.R.L. refers to an echo attenuation (loss) from echo canceler output (Rout) to echo canceler input (Sin).

D-3
When an echo path changes (upon re-calling), it is recommended to reset the echo canceler through EC_EN, PDNB, or SPDN.

D-4
When using the echo canceler, it is recommended to output signals through RXGEN from various generators to the receive side. If signals are output from RXGENA or RXGENB, echoes may not be eliminated.

RC0 (Range Controller 0)

RC0 (Range Controller 0) is designed to improve the idle channel noise characteristics on the transmitting side by attenuating an output signal by a certain level with respect to the level of an input signal.

Figure 64 shows the input/output characteristics of RC0. Setting RC0_EN of the RC0 control internal memory (RC0_CR) to "1" will operate RC0. The settings for RC0 operation are configured using the internal data memories descrbed below.

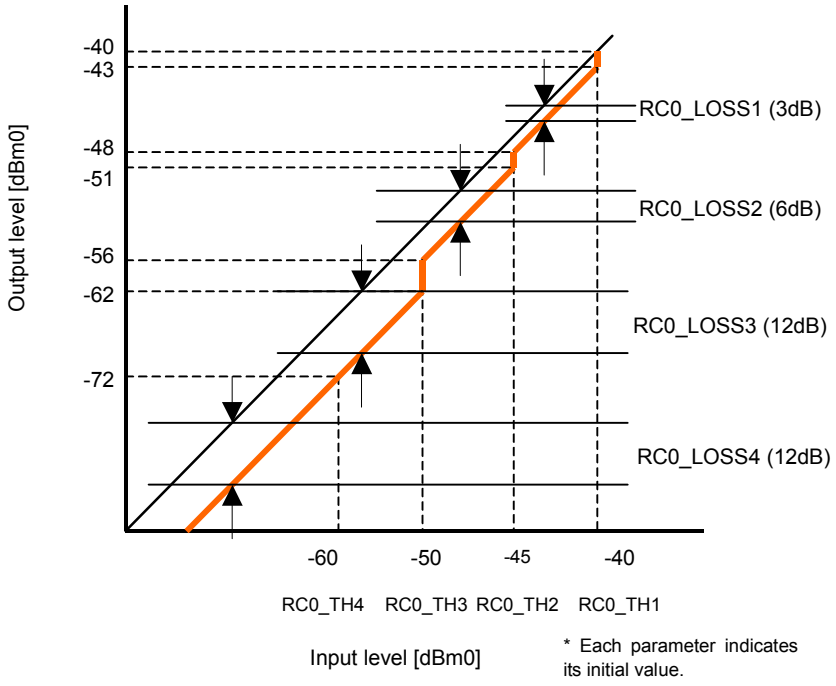


Figure 64 RC0 Input/Output Characteristics

A. Internal data memory for RC0 control (RC0_CR)
Initial value: 0000h
Internal data memory for RC0 control

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	—	—	RC0_EN
Initial value	0	1	0	0	0	0	0	0

B15-B1: Reserved bits Changing of the initial values is inhibited.

B0: RC0 control register (RC0_EN)
1: Disables the RC0 function. … RC0 is passed undetected (Default)
0: Enables the RC0 function.

B-1: RC0 internal data memory for adjustment of threshold 1 for loss (RC0_TH1)
Initial value: 0090h (approx. –40 dBm0)
Use the following calculation expression when changing threshold 1 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 1 for loss to –40 dBm0.
$10^{((-40-3.17)/20)} \times 2/PI \times 32768 \approx 144d = 0090h$
Upper limit: +3.17 dBm0 (Data: 517Ch)
: Approx. –40 dBm0 (Data: 0090h)
Lower limit: –∞ (Data: 0000h)

B-2: RC0 internal data memory for adjustment of threshold 2 for loss (RC0_TH2)
Initial value: 0051h (approx. –45 dBm0)
Use the following calculation expression when changing threshold 2 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 2 for loss to –45 dBm0.
$10^{((-45-3.17)/20)} \times 2/PI \times 32768 \approx 81d = 0051h$
Upper limit: Less than RC0_TH1
: Approx. –45 dBm0 (Data: 0051h)
Lower limit: –∞ (Data: 0000h)

B-3: RC0 internal data memory for adjustment of threshold 3 for loss (RC0_TH3)
Initial value: 002Dh (approx. –50 dBm0)
Use the following calculation expression when changing threshold 3 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 3 for loss to –50 dBm0.
$10^{((-50-3.17)/20)} \times 2/PI \times 32768 \approx 45d = 002Dh$
Upper limit: Less than RC0_TH2
: Approx. –50 dBm0 (Data: 002Dh)
Lower limit: –∞ (Data: 0000h)

B-4: RC0 internal data memory for adjustment of threshold 4 for loss (RC0_TH4)
Initial value: 000Eh (approx. –60 dBm0)
Use the following calculation expression when changing threshold 4 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 4 for loss to –60 dBm0.
$10^{((-60-3.17)/20)} \times 2/PI \times 32768 \approx 14d = 000Eh$
Upper limit: Less than RC0_TH3
: Approx. –60 dBm0 (Data: 000Eh)
Lower limit: –∞ (Data: 0000h)

C-1: RC0 internal data memory for adjusting a loss value in the case of threshold 1 or 2 for loss (RC0_LOSS1)

Initial value: 005Ah (approx. 3 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 3 dB.

$128/10^{(3/20)} \approx 90d = 005Ah$

Upper limit: 0 dB (Data: 0080h)

: Approx. 3 dB (Data: 005Ah)

Lower limit: RC0_LOSS2

C-2: RC0 internal data memory for adjusting a loss value in the case of threshold 2 or 3 for loss (RC0_LOSS2)

Initial value: 0040h (approx. 6 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 6 dB.

$128/10^{(6/20)} \approx 64d = 0040h$

Upper limit: RC0_LOSS1

: Approx. 6 dB (Data: 0040h)

Lower limit: RC0_LOSS3

C-3: RC0 internal data memory for adjusting a loss value in the case of threshold 3 or 4 for loss (RC0_LOSS3)

Initial value: 0020h (approx. 12 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 12 dB.

$128/10^{(12/20)} \approx 32d = 0020h$

Upper limit: RC0_LOSS2

: Approx. 12 dB (Data: 0020h)

Lower limit: RC0_LOSS4

C-4: RC0 internal data memory for adjusting a loss value in the case of threshold 4 or less for loss (RC0_LOSS4)

Initial value: 0020h (approx. 12 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 12 dB.

$128/10^{(12/20)} \approx 32d = 0020h$

Upper limit: RC0_LOSS3

: Approx. 12 dB (Data: 0020h)

Lower limit: MUTE (Data: 0000h)

D-1: RC0 internal data memory for adjusting a plus step value for loss (RC0_PL)

The loss value changes to the target loss value with the step value set in RC0_PL when the input level becomes higher than each threshold level.

Initial value: 47CFh (approx. 1 dB)

Use the following calculation expression when changing the plus step value to X:

Calculation expression: $10^{(X/20)} \times 16384$

<Example> Set the plus step value to 1 dB.

$10^{(1/20)} \times 16384 \approx 18383d = 47CFh$

Upper limit: +6 dB (Data: 7FB2h)

: Approx. 1 dB (Data: 47CFh)

Lower limit: Approx. +0.0005 dB (Data: 4001h)

D-2: RC0 internal data memory for adjusting a minus step value for loss (RC0_MI)

The loss value changes to the target loss value with the step value set in RC0_MI when the input level becomes lower than the threshold level that corresponds.

Initial value: 3F44h (approx. –0.1 dB)

Use the following calculation expression when changing the step value to X:

Calculation expression: $10^{(X/20)} \times 16384$

<Example> Set the step value to –0.1 dB.

$10^{(-0.1/20)} \times 16384 \approx 16196d = 3F44h$

Upper limit: –6 dB (Data: 2013h)

: Approx. –0.1 dB (Data: 3F44h)

Lower limit: Approx. –0.0005 dB (Data: 3FFFh)

E. RC0 internal data memory for adjusting the input signal level detecting sensitivity 1/2 (RC0_POW_C1/RC0_POW_C2)

Initial value: RC0_POW_C1: 3E00h

RC0_POW_C2: 0200h

This is an internal data memory for adjusting the input signal detecting sensitivity in RC0. By adjusting this memory, the detecting sensitivity for a voice signal on the transmitting side that is input at a level near threshold is decreased, so that fluctuations in output signal can be supressed.

Following shows the settings for decreasing the input signal detecting sensitivity.

- To decrease the detecting sensitivity to about one-half the initial value:

  Setting value: RC0_POW_C1: 3F00h

  RC0_POW_C2: 0100h

- To decrease the detecting sensitivity to about one-fourth of the initial value:

  Setting value: RC0_POW_C1: 3F80h

  RC0_POW_C2: 0080h

RC1 (Range Controller 1)

RC1 (Range Controller 1) is designed to improve the idle channel noise characteristics on the transmitting side by attenuating an output signal by a certain level with respect to the level of an input signal.

Figure 65 shows the input/output characteristics of RC1. Setting RC1_EN of the RC1 control internal memory (RC1_CR) to "1" will operate RC1. The settings for RC1 operation are configured using the internal data memories descrbed below.

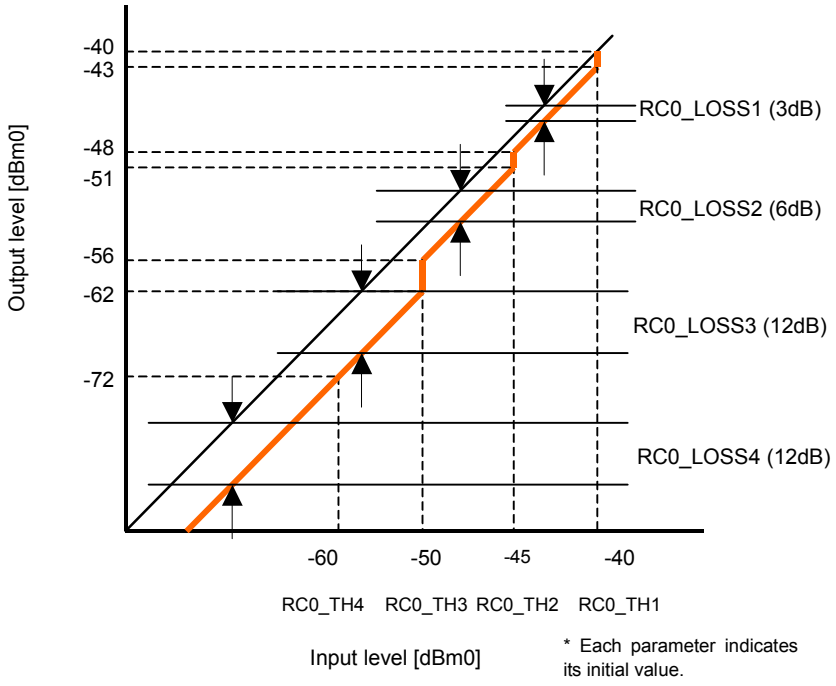


Figure 65 RC1 Input/Output Characteristics

A. Internal data memory for RC1 control (RC1_CR)
Initial value: 0000h
Internal data memory for RC1 control

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	—	—	RC1_EN
Initial value	0	1	0	0	0	0	0	0

B15-B1: Reserved bits Changing of the initial values is inhibited.

B0: RC1 control register (RC1_EN)
1: Disables the RC1 function. … RC1 is passed undetected (Default)
0: Enables the RC1 function.

B-1: RC1 internal data memory for adjustment of threshold 1 for loss (RC1_TH1)
Initial value: 0090h (approx. –40 dBm0)
Use the following calculation expression when changing threshold 1 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 1 for loss to –40 dBm0.
$10^{((-40-3.17)/20)} \times 2/PI \times 32768 \approx 144d = 0090h$
Upper limit: +3.17 dBm0 (Data: 517Ch)
: Approx. –40 dBm0 (Data: 0090h)
Lower limit: –∞ (Data: 0000h)

B-2: RC1 internal data memory for adjustment of threshold 2 for loss (RC1_TH2)
Initial value: 0051h (approx. –45 dBm0)
Use the following calculation expression when changing threshold 2 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 2 for loss to –45 dBm0.
$10^{((-45-3.17)/20)} \times 2/PI \times 32768 \approx 81d = 0051h$
Upper limit: Less than RC1_TH1
: Approx. –45 dBm0 (Data: 0051h)
Lower limit: –∞ (Data: 0000h)

B-3: RC1 internal data memory for adjustment of threshold 3 for loss (RC1_TH3)
Initial value: 002Dh (approx. –50 dBm0)
Use the following calculation expression when changing threshold 3 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 3 for loss to –50 dBm0.
$10^{((-50-3.17)/20)} \times 2/PI \times 32768 \approx 45d = 002Dh$
Upper limit: Less than RC1_TH2
: Approx. –50 dBm0 (Data: 002Dh)
Lower limit: –∞ (Data: 0000h)

B-4: RC1 internal data memory for adjustment of threshold 4 for loss (RC1_TH4)
Initial value: 000Eh (approx. –60 dBm0)
Use the following calculation expression when changing threshold 4 for loss to X:
Calculation expression: $10^{((X-3.17)/20)} \times 2/PI \times 32768$
<Example> Set threshold 4 for loss to –60 dBm0.
$10^{((-60-3.17)/20)} \times 2/PI \times 32768 \approx 14d = 000Eh$
Upper limit: Less than RC1_TH3
: Approx. –60 dBm0 (Data: 000Eh)
Lower limit: –∞ (Data: 0000h)

C-1: RC1 internal data memory for adjusting a loss value in the case of threshold 1 or 2 for loss (RC1_LOSS1)

Initial value: 005Ah (approx. 3 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 3 dB.

$128/10^{(3/20)} \approx 90d = 005Ah$

Upper limit: 0 dB (Data: 0080h)

: Approx. 3 dB (Data: 005Ah)

Lower limit: RC1_LOSS2

C-2: RC1 internal data memory for adjusting a loss value in the case of threshold 2 or 3 for loss (RC1_LOSS2)

Initial value: 0040h (approx. 6 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 6 dB.

$128/10^{(6/20)} \approx 64d = 0040h$

Upper limit: RC1_LOSS1

: Approx. 6 dB (Data: 0040h)

Lower limit: RC1_LOSS3

C-3: RC1 internal data memory for adjusting a loss value in the case of threshold 3 or 4 for loss (RC1_LOSS3)

Initial value: 0020h (approx. 12 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 12 dB.

$128/10^{(12/20)} \approx 32d = 0020h$

Upper limit: RC1_LOSS2

: Approx. 12 dB (Data: 0020h)

Lower limit: RC1_LOSS4

C-4: RC1 internal data memory for adjusting a loss value in the case of threshold 4 or less for loss (RC1_LOSS4)

Initial value: 0020h (approx. 12 dB)

Use the following calculation expression when changing the loss value to X:

Calculation expression: $128/10^{(X/20)}$

<Example> Set the loss value to 12 dB.

$128/10^{(12/20)} \approx 32d = 0020h$

Upper limit: RC1_LOSS3

: Approx. 12 dB (Data: 0020h)

Lower limit: MUTE (Data: 0000h)

D-1: RC1 internal data memory for adjusting a plus step value for loss (RC1_PL)

The loss value changes to the target loss value with the step value set in RC1_PL when the input level becomes higher than the threshold level that corresponds.

Initial value: 47CFh (approx. 1 dB)

Use the following calculation expression when changing the step value to X:

Calculation expression: $10^{(X/20)} \times 16384$

<Example> Set the step value to 1 dB.

$10^{(1/20)} \times 16384 \approx 18383d = 47CFh$

Upper limit: +6 dB (Data: 7FB2h)

: Approx. 1 dB (Data: 47CFh)

Lower limit: Approx. +0.0005 dB (Data: 4001h)

D-2: RC1 internal data memory for adjusting a minus step value for loss (RC1_MI)

The loss value changes to the target loss value with the step value set in RC1_MI when the input level becomes lower than the shreshold level that corresponds.

Initial value: 3F44h (approx. –0.1 dB)

Use the following calculation expression when changing the step value to X:

Calculation expression: $10^{(X/20)} \times 16384$

<Example> Set the step value to –0.1 dB.

$10^{(-0.1/20)} \times 16384 \approx 16196d = 3F44h$

Upper limit: –6 dB (Data: 2013h)

: Approx. –0.1 dB (Data: 3F44h)

Lower limit: Approx. –0.0005 dB (Data: 3FFFh)

E. RC1 internal data memory for adjusting the input signal level detecting sensitivity 1/2 (RC1_POW_C1/RC1_POW_C2)

Initial value: RC1_POW_C1: 3E00h

RC1_POW_C2: 0200h

This is an internal data memory for adjusting the input signal detecting sensitivity in RC1. By adjusting this memory, the detecting sensitivity for a voice signal on the transmitting side that is input at a level near threshold is decreased, so that fluctuations in output signal can be supressed.

Following shows the settings for decreasing the input signal detecting sensitivity.

- To decrease the detecting sensitivity to about one-half the initial value:

  Setting value: RC1_POW_C1: 3F00h

  RC1_POW_C2: 0100h

- To decrease the detecting sensitivity to about one-fourth of the initial value:

  Setting value: RC1_POW_C1: 3F80h

  RC1_POW_C2: 0080h

Dial Pulse Detector (DPDET)

When the general-purpose I/O port GPIOA[0] is configured as its secondary function (DPI: dial pulse input pin), dial pulse signals can be detected.
The dial pulse detector is enabled when the control register (DPDET_EN) of the dial pulse detector is set to "1". When a dial pulse signal is detected, the dial pulse detector status register (DP_DET) is set to "1" and the detected pulse count is stored in the detected dial pulse count display register (DPDET_DATA[7:0]). Read a dial pulse count from DPDET_DATA[7:0] at the timing when DP_DET has changed from "1" to "0". When a dial pulse signal is not detected or DPDET_EN is "0", DP_DET is set to "0".
Figure 66 shows the dial pulse detection timing.
The dial pulse detector samples dial pulse signals that are input from GPIOA[0] at every 8kHz and detects dial pulses according to the values set in the ON guard timer (DPDET_ON_TIM) and OFF guard timer (DPDET_OFF_TIM). A detection termination time can be adjusted by setting a detection termination timer (DPDET_DETOFF_TIM).

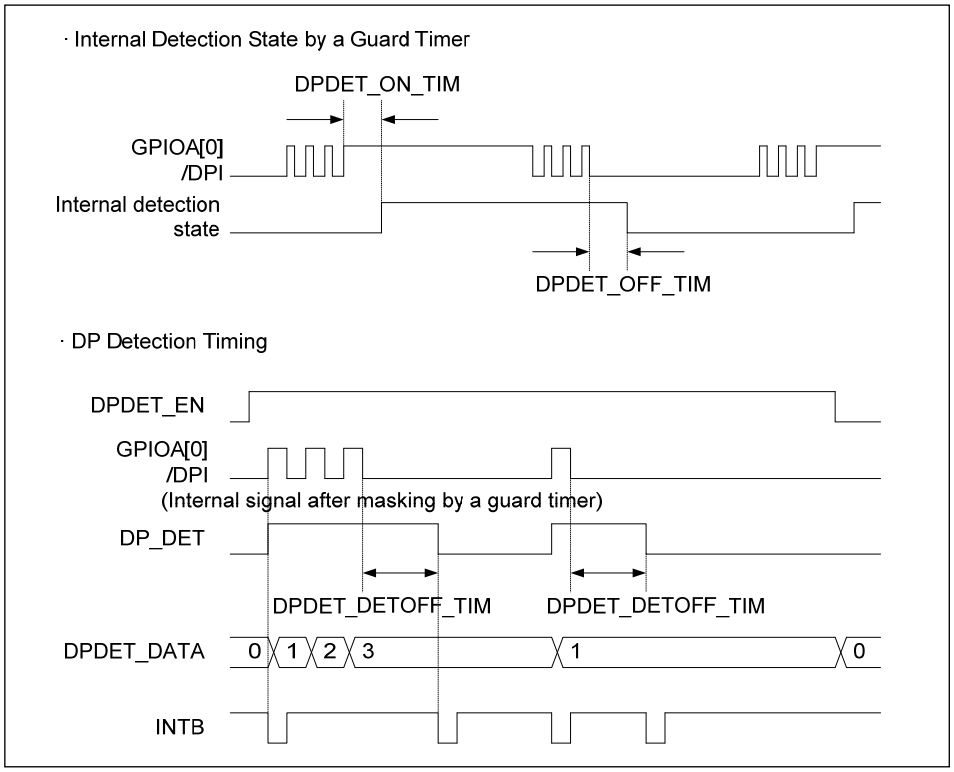


Figure 66 Dial Pulse Detection Timing

A. Dial pulse detector control register (DPDET_EN)
0: Stops the dial pulse detector (Initial value)
1: Activates the dial pulse detector

B. Dial pulse detector detection status register (DP_DET)
0: Dial pulse non-detection (Initial value)
1: Dial pulse detection

An input edge of the DPI pin is detected after DPDET_EN and the register is set to "1".
When no edge is detected within the period that is set in DPDET_DETOFF_TIM, the register is cleared to "0".

C. Dial pulse detection polarity control register (DPDET_POL)
Control the polarity that is input from the DPI pin.
0: No polarity inversion (Initial value)
1: Polarity inversion

D. Detected dial pulse count display register (DPDET_DATA[7:0])
Initial value: 00h (Non-detection state)
Displays the dial pulse count that was detected. This register is updated at edge detection.

E. Dial pulse detection ON guard timer internal data memory (DPDET_ON_TIM)
Initial value: 0028h (5 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: Guard timer value ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(Data: 7FFFh)
	: 5 ms	(Data: 0028h)
Lower limit	: 0.125 ms	(Data: 0001h)

F. Dial pulse detection OFF guard timer internal data memory (DPDET_OFF_TIM)
Initial value: 0028h (5 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: Guard timer value ms/0.125 ms
<Example> 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(Data: 7FFFh)
	: 5 ms	(Data: 0028h)
Lower limit	: 0.125 ms	(Data: 0001h)

G. Detection termination timer control internal data memory (DPDET_DETOFF_TIM)
Initial value: 03E8h (125 ms)
Use the following calculation expression when changing the timer value.
Calculation expression: Guard timer value ms/0.125 ms
<Example> 125 ms
125/0.125 = 1000d = 03E8h

Upper limit	: 4095.875 ms	(Data: 7FFFh)
	: 125 ms	(Data: 03E8h)
Lower limit	: 0.125 ms	(Data: 0001h)

(Note)
When activating DPDET, first set the primary function/secondary function selection register (GPFA[0]) of GPIOA[0] to "1" to select the secondary function (dial pulse input pin), then activate DPDET. When DPDET is activated under the following conditions, an interrupt occurs after the ON guard timer set time. In this case, ignore the first interrupt.

- DPDET_POL = "0", DPI = "1"
- DPDET_POL = "1", DPI = "0"

Dial Pulse Transmitter (DPGEN)

The dial pulse transmitter can output dial pulse signals when the general-purpose I/O port GPIOA[2] is set to the secondary function (DPO: dial pulse output pin).

The dial pulse transmitter is enabled when the dial pulse transmit control register (DPGEN_EN) is set to ”1” and outputs dial pulse signals of the pulse count that is set in dial pulse count setting register (DPGEN_DATA[3:0]). Figure 67 shows the dial pulse output timing.

A dial pulse speed of 10 pps or 20 pps can be selected using the dial pulse speed control register (DPGEN_PPS). A make rate can be adjusted through DPGEN_DUTY by setting a time of a break section. A dial pulse signal output polarity can be changed by the dial pulse output polarity control register (DPGEN_POL).

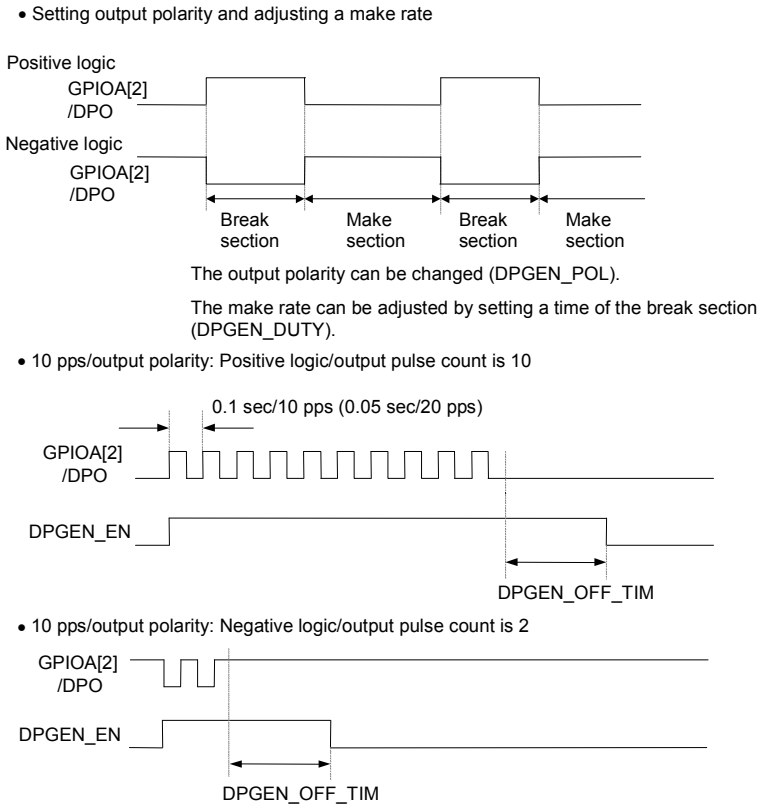


Figure 67 Dial Pulse Output Timing

A. Dial pulse transmit control register (DPGEN_EN)

0: Stops dial pulse output (Initial value)
1: Activates dial pulse output

B. Dial pulse count setting register (DPGEN_DATA[3:0])
Initial value: 0h
Upper limit: 10 (Data: Ah)
Lower limit: 1 (Data: 1h)

C. Dial pulse speed control register (DPGEN_PPS)

0: 10 pps (Initial value)
1: 20 pps

D. Dial pulse output polarity control register (DPGEN_POL)
Control the output polarity from GPIOA[2].

0: Positive logic (Low: Make section, High: Break section), initial value
1: Negative logic (Low: Break section, High: Make section)

E. Dial pulse make rate control internal data memory (DPGEN_DUTY)
Initial value: 0108h (33 ms/10 pps, 16.5 ms/20 pps)
Use the following calculation expression when setting a time of a break section.
When the pulse speed is set to 20 pps, the time will be 1/2 of the specified value.

Calculation expression: "Break section output time" ms/0.125 ms
<Example> 33 ms
33/0.125 = 264d = 0108h

Upper limit:	100 ms	(Data: 0320h)
:	33 ms	(Data: 0108h)
Lower limit:	0.125 ms	(Data: 0001h)

F. Dial pulse output termination control internal data memory (DPGEN_OFF_TIM)
Initial value: 03E8h (125 ms)
Use the following calculation expression when setting output termination control.
Calculation expression: "Output termination time" ms/0.125 ms
<Example> 125 ms
125/0.125 = 1000d = 03E8h

Upper limit:	4095.875 ms	(Data: 7FFFh)
:	125 ms	(Data: 03E8h)
Lower limit:	0 ms	(Data: 0001h)

(Note) Be sure to set the following before activating DPGEN (DPGEN_EN = 1).

- Set the dial pulse output polarity control register (DPGEN_POL).
  The output level (initial value) of the dial pulse output pin is set as follows.
  DPGEN_POL=0 (positive logic): GPOA[2]/DPO = "0"
  DPGEN_POL=1 (negative logic): GPOA[2]/DPO = "1"
- After setting the above, set the primary function/secondary function selection register (GPFA[2]) of GPIOA[2] to "1" to select the secondary function (dial pulse output pin).

Timer (TIMER)

This is a 16-bit incremental timer. When the timer control register (TIM_EN) is set to "1", this timer starts incrementing the timer counter at every 125 μs. When the timer counter value (TIM_COUNT) and the timer data setting value (TIM_DATA) match, causing overflow, the timer counter value is reset to "0000h" and the counter is incremented again. When overflow occurs, the timer overflow display register (TMOVF) is set to "1", causing an INTB interrupt. The timer overflow interrupt can be cleared by writing "0" to TMOVF from the MCU side.

A. Timer control register (TIM_EN)
When this bit is set to "1", the timer starts incrementing the counter.
When "0" is set, the timer stops counting and clears the timer counter value.
0: Stops counting (Initial value)
1: Starts counting

B. Timer overflow display register (TMOVF)
When the timer counter value and the timer data setting value match, causing timer overflow, the timer overflow display register (TMOVF) is set to "1", causing an INTB interrupt.
When "0" is written either to TMOVF on the MCU side or to the timer control register (TIM_EN), the timer stops and the timer overflow interrupt is cleared to "0".

C. Timer counter value display internal data memory (TIM_COUNT)
Initial value: 0000h

D. Timer data setting internal data memory (TIM_DATA)
Initial value: FFFFh

Upper limit	: 8192 ms	(Data: FFFFh)
Lower limit	: 0.250 ms	(Data: 0001h)

Outband Control (OUTBAND_CONTROL)

When the detection flag (DET) of tone detector 0, tone detector 1, or DTMF detector is set to "1", MUTE processing is performed automatically inside the LSI or silent data is written to the transmit buffer.
Processing contents in each Speech CODEC are shown below.

G.711(μ-law) MUTE processing is performed for Speech CODEC input data.
G.711(A-law) MUTE processing is performed for Speech CODEC input data.
G.729.A Fixed silent data is written to the transmit buffer (TX Buffer) and
Fixed silent data of 80 bits can be changed in initial mode.

Initial value: 0000h

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	TDET1_OB_EN	TDET0_OB_EN	DTMFDET_OB_EN
Initial value	0	0	0	0	0	0	0	0

B15-B3: Reserved bits Changing of the initial values is inhibited.
B2: TDET1_OUTBAND_EN control
1: ON (MUTE processing or silent data write processing is performed while TONE1_DET is "1")
0: OFF
B1: TDET0_OUTBAND_EN control
1: ON (MUTE processing or silent data write processing is performed while TONE0_DET is "1")
0: OFF
B0: DTMFDET_OUTBAND_EN control
1: ON (MUTE processing or silent data write processing is performed while DTMF_DET is "1")
0: OFF

- Time of tone leakage to transmit buffer
  Use the following expression as the reference for the transmit buffer tone leakage time in each Speech CODEC.

G.711 0 ms + A + B
G.729.A –10 ms to –20 ms + A + B
Note: –10 ms to –20 ms by prediction and framing process.
A : Detection delay time of each detector (ms)
Detection delay time A of each detector depends on the condition such as the input level frequency.
B : ON guard timer time of each detector (ms)

<Example>
When the detection delay time of the detector is approx. 30 ms and the ON guard timer time is 20 ms, the transmit buffer leakage time will be as follows.

G.711 30 ms(A) +20 ms(B) = Approx. 50 ms
G.729.A –10 ms to –20 ms +30 ms(A) +20 ms(B) = Approx. 30 ms to 40 ms

Outband G.729.A Data (OUTBAND_G729_DAT)
When G.729.A is selected as Speech CODEC at outband control and the detection flag (DET) of each detector is set to "1", the following fixed data is stored in the transmit buffer. The fixed data can be changed in initial mode.

Address:	089Fh	08A0h	08A1h	08A2h	08A3h
Initial value:	7852h	80A0h	00FAh	C200h	07D6h

Interrupt Cause Mask Control
See Table 1 for the list of interrupt causes.
When an interrupt cause is changed, "L" is output to the INTB pin for about 1.0 μs and when an interrupt cause remains unchanged, "H" is output.
When "1" is written to an appropriate bit position of the internal memory, the INTB pin retains the "H" state even if the interrupt cause is changed. (The change is reflected in the register that displays each interrupt factor status.)

(Note)
As the default, an INTB interrupt occurs according to the interrupt cause that is indicated in Table 1 (mask setting OFF). When an INTB interrupt is not required, set "1" in the related bit of the interrupt cause mask control internal data memory during initial mode to set the mask setting to ON.

A. Rising edge interrupt mask control

A-1: CR16 rising edge interrupt mask control (CR16_INTP_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	FDET_OER_PMSK	FDET_FER_PMSK	FDET_RQ_PMSK
Initial value	1	1	1	1	1	0	0	0

B15-B3: Reserved bits Changing of the initial values is inhibited.

B2: FSK receive overrun error rising edge mask setting (FDET_OER_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B1: FSK receive framing error rising edge interrupt mask setting (FDET_FER_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B0: FSK receive data read request rising edge interrupt mask setting (FDET_RQ_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

A-2: CR18 rising edge interrupt mask control (CR18_INTP_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	—	—	TMOVF_ _PMSK
Initial value	1	1	1	1	1	1	1	0

B15-B1: Reserved bits Changing of the initial values is inhibited.

B0: Timer overflow status rising edge interrupt mask setting (TMOVF_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

A-3: CR19 rising edge interrupt mask control (CR19_INTP_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	TONE1_DET_PMSK	TONE0_DET_PMSK	TGEN1_EXFLAG_PMSK	TGEN0_EXFLAG_PMSK	—
Initial value	0	1	1	0	0	0	0	0

B15-B5: Reserved bits Changing of the initial values is inhibited.

B4: TONE1 detector detection status rising edge interrupt mask setting (TONE1_DET_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B3: TONE0 detector detection status rising edge interrupt mask setting (TONE0_DET_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B2: TONE generator 1 execution flag rising edge interrupt mask setting (TGEN1_EXFLAG_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B1: TONE generator 0 execution flag rising edge interrupt mask setting (TGEN0_EXFLAG_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B0: Reserved bit. Changing the initial value is inhibited.

A-4: CR20 rising edge interrupt mask control (CR20_INTP_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	DP_DET _PMSK	—	DTMF _DET _PMSK	DTMF _CODE3 _PMSK	DTMF _CODE2 _PMSK	DTMF _CODE1 _PMSK	DTMF _CODE0 _PMSK
Initial value	0	0	1	0	0	0	0	0

B15-B7: Reserved bits Changing of the initial values is inhibited.

B6: Dial pulse detector detection status rising edge interrupt mask setting (DP_DET_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B5: Reserved bit Changing of the initial value is inhibited.

B4: DTMF detector detection status rising edge interrupt mask setting (DTMF_DET_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B3-B0: DTMF detection code rising edge interrupt mask setting (DTMF_CODE[3:0]_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

A-5: CR21 rising edge interrupt mask control (CR21_INTP_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	TXERR_CH2_PMSK	TXERR_CH1_PMSK	FR0_CH2_PMSK	FR0_CH1_PMSK
Initial value	1	1	1	1	0	0	0	0

B15-B4: Reserved bits Changing of the initial values is inhibited.

B3: CH2 transmit error status rising edge interrupt mask setting (TXERR_CH2_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B2: CH1 transmit error status rising edge interrupt mask setting (TXERR_CH1_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B1: CH2 transmit request rising edge interrupt mask setting (FR0_CH2_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B0: CH1 transmit request rising edge interrupt mask setting (FR0_CH1_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

(Note) When stopping Speech CODEC, be sure to make the following settings in advance:
- Writing 00FFh to CR21 rising edge interrupt mask control (CR21_INTP_MSKCNT)
- Writing 00FFh to CR22 rising edge interrupt mask control (CR22_INTP_MSKCNT)

A-6: CR22 rising edge interrupt mask control (CR22_INTP_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	RXERR_CH2_PMSK	RXERR_CH1_PMSK	RXBW_ERR_PMSK	FR1__PMSK
Initial value	1	1	1	1	0	0	0	0

B15-B4: Reserved bits Changing of the initial values is inhibited.

B3: CH2 receive error status rising edge interrupt mask setting (RXERR_CH2_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B2: CH1 receive error status rising edge interrupt mask setting (RXERR_CH1_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B1: Receive invalid write error status rising edge interrupt mask setting (RXBW_ERR_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

B2-B1: Reserved bits Changing of the initial values is inhibited.

B0: Receive request rising edge interrupt mask setting (FR1_PMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the rising edge)
0: Mask setting OFF

(Note) When stopping Speech CODEC, be sure to make the following settings in advance:
- Writing 00FFh to CR21 rising edge interrupt mask control (CR21_INTP_MSKCNT)
- Writing 00FFh to CR22 rising edge interrupt mask control (CR22_INTP_MSKCNT)

B. Falling edge interrupt mask control

B-1:CR17 falling edge interrupt mask control (CR17_INTN_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	—	—	—	FGEN _FLAG _NMSK
Initial value	1	1	1	1	1	1	1	0

B15-B1: Reserved bits Changing of the initial values is inhibited.

B0: FSK output data setting completion flag falling edge interrupt mask setting (FGEN_FLAG_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B-2: CR19 falling edge interrupt mask control (CR19_INTN_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	TONE1_DET_NMSK	TONE0_DET_NMSK	TGEN1_EXFLAG_NMSK	TGEN0_EXFLAG_NMSK	—
Initial value	0	1	1	0	0	0	0	0

B15-B5: Reserved bits Changing of the initial values is inhibited.

B4: TONE1 detector detection status falling edge interrupt mask setting (TONE1_DET_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B3: TONE0 detector detection status falling edge interrupt mask setting (TONE0_DET_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B2: TONE generator 1 execution flag falling edge interrupt mask setting (TGEN1_EXFLAG_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B1: TONE generator 0 execution flag falling edge interrupt mask setting (TGEN0_EXFLAG_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B0: Reserved bit Changing of the initial value is inhibited.

B-3: CR20 falling edge interrupt mask control (CR20_INTN_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	DP_DET _NMSK	—	DTMF _DET _NMSK	DTMF _CODE3 _NMSK	DTMF _CODE2 _NMSK	DTMF _CODE1 _NMSK	DTMF _CODE0 _NMSK
Initial value	0	0	1	0	0	0	0	0

B15-B7: Reserved bits Changing of the initial values is inhibited.

B6: Dial pulse detector detection status falling edge interrupt mask setting (DP_DET_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B5: Reserved bit Changing of the initial value is inhibited.

B4: DTMF detector detection status falling edge interrupt mask setting (DTMF_DET_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B3-B0: DTMF detection code falling edge interrupt mask setting (DTMF_CODE[3:0]_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B-4: CR21 falling edge interrupt mask control (CR21_INTN_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	TXERR_CH2_NMSK	TXERR_CH1_NMSK	—	—
Initial value	1	1	1	1	0	0	1	1

B15-B4: Reserved bits Changing of the initial values is inhibited.

B3: CH2 transmit error status falling edge interrupt mask setting (TXERR_CH2_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B2: CH1 transmit error status falling edge interrupt mask setting (TXERR_CH1_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B1-B0: Reserved bits Changing of the initial values is inhibited.

B-5: CR22 falling edge interrupt mask control (CR22_INTN_MSKCNT)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	—	—	—	—	RXERR_CH2_NMSK	RXERR_CH1_NMSK	RXBW_ERR_NMSK	—
Initial value	1	1	1	1	0	0	0	1

B15-B4: Reserved bits Changing of the initial values is inhibited.

B3: CH2 receive error status falling edge interrupt mask setting (RXERR_CH2_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B2: CH1 receive error status falling edge interrupt mask setting (RXERR_CH1_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B1: Receive invalid write error status falling edge interrupt mask setting (RXBW_ERR_NMSK)
1: Mask setting ON (Masks the interrupt request signal INTB that occurs at the falling edge)
0: Mask setting OFF

B0: Reserved bit Changing of the initial value is inhibited.

Decoded Output Starting Offset Time Control (DEC_ONTIM)

Initial value: 0000h (0 ms)
Use the following calculation expression when changing the decoded output starting offset time (tDECON).
For tDECON, see the receive buffer control timing of Figures 18 to 21.

Calculation expression: Decoded output starting offset time ms/0.125 ms
<Example> 5 ms
5/0.125 = 0040d = 0028h
Upper limit: 32 ms (Data: 0100h)
Lower limit: 0 ms (Data: 0000h)

(Note)
Regardless of decoded output starting offset time value, in G.711 (PLC function enabled), decoded output starts after the decoded output control register (DEC_OUTON) is set to "1" and silent data of approx. 3.75 ms is output. (Due to the delay of the G.711 PLC algorithm)
Note that the time required up to the actual start of the decoded output is calculated by adding approx. 3.75 ms to the value set for the decoded output starting offset time. In G.711 (PLC function disabled), decoded output starts after the decoded output starting offset time that is set in the data memory.
In G.729.A, note that a time of approx. 15 ms is added to the setting value of the decoded output starting offset time that is set in the internal data memory for the time required up to the actual start of decoded output.

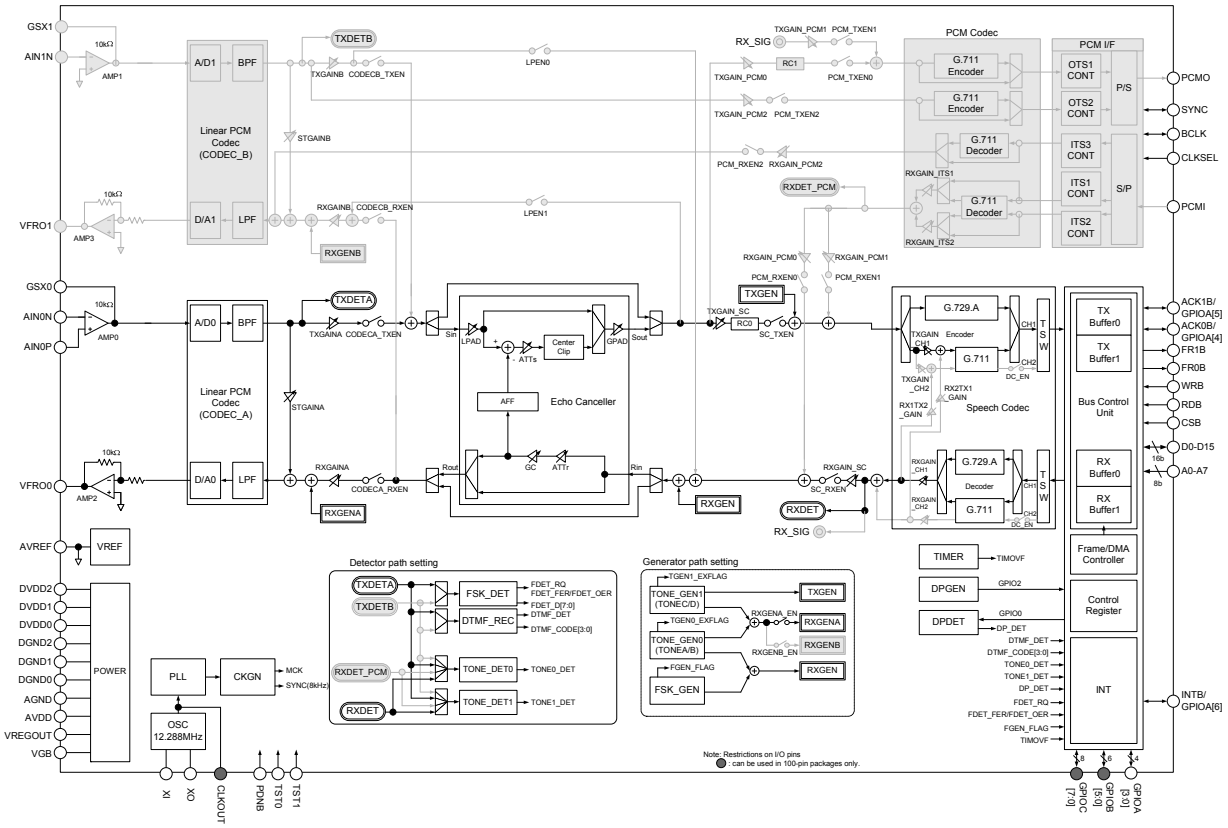
(Note)
Though the initial value of the decoded output starting offset time control (DEC_ONTIM) is defined as 0000h (0 ms), be sure to set the offset time to 0001h (0.125 ms) to 0100h (32 ms).

Multiple Word Write Starting Address Setting Internal Data Memory (START_ADDRESS)

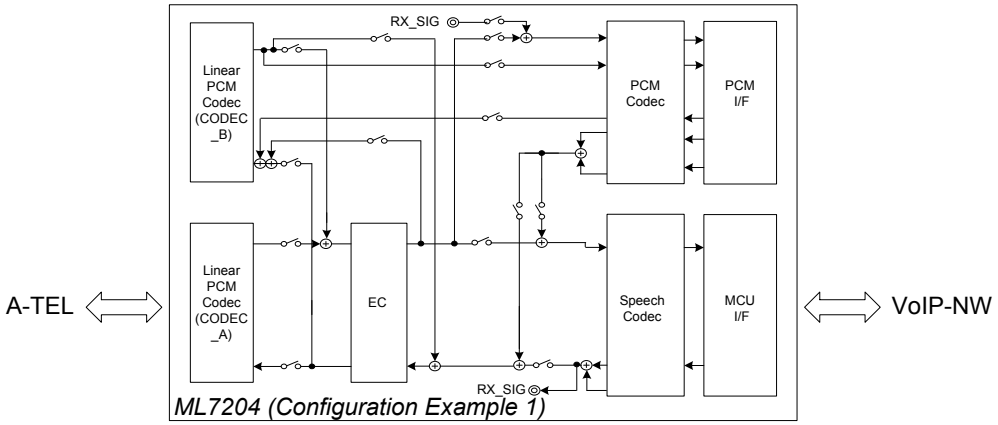
Set an internal data memory starting address when writing to consecutive addresses in the internal data memory according to the procedure that is shown in Figure 53. (Initial value: 0000h)

CONFIGURATION EXAMPLES

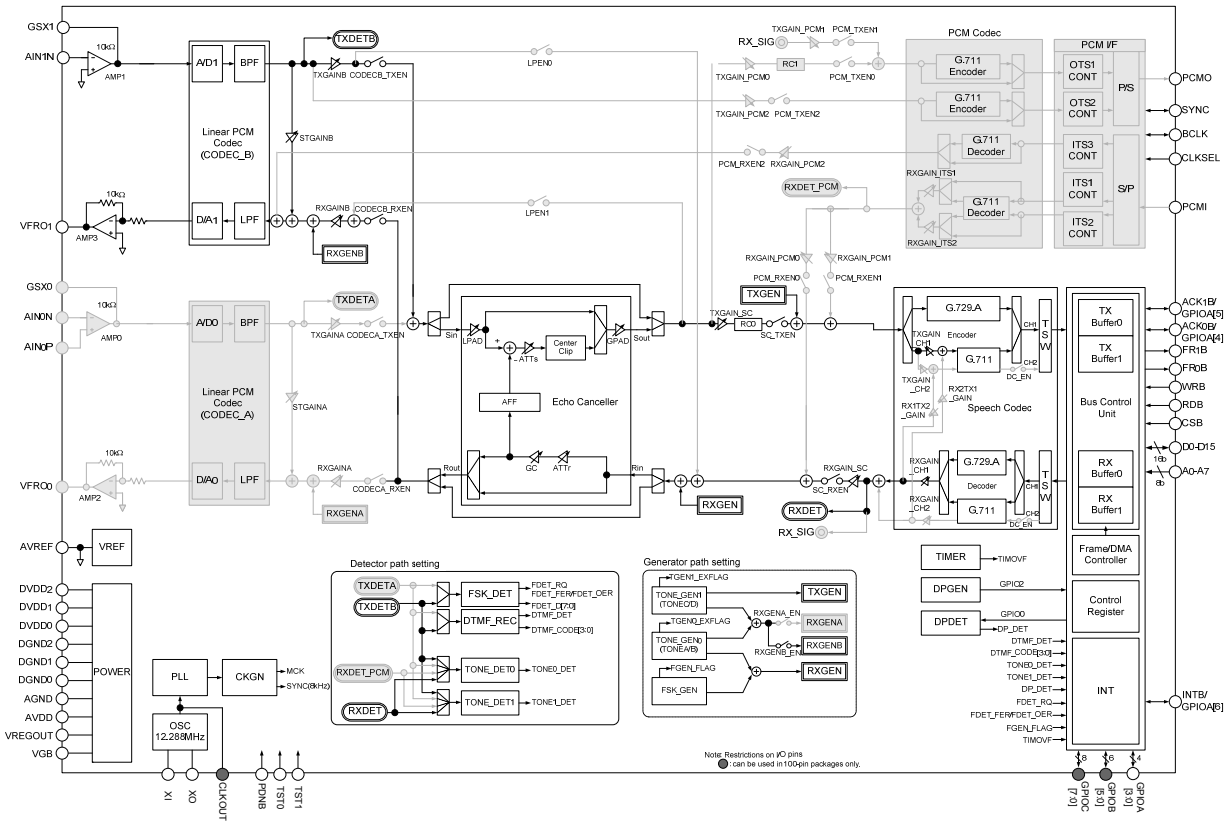
Configuration Example 1 (Basic Call, CODEC_A)



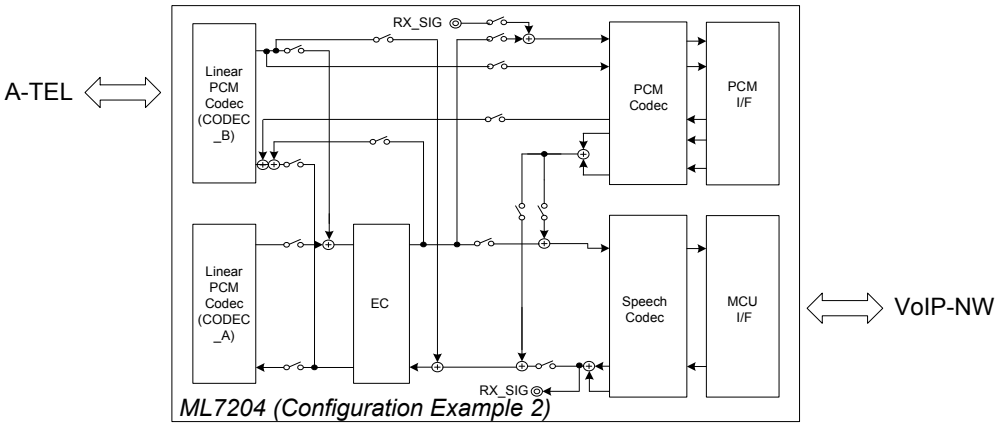
This example shows the configuration for making calls with an analog telephone set (A-TEL) on the NW side by connecting the analog telephone interface on the Linear PCM CODEC_A side.



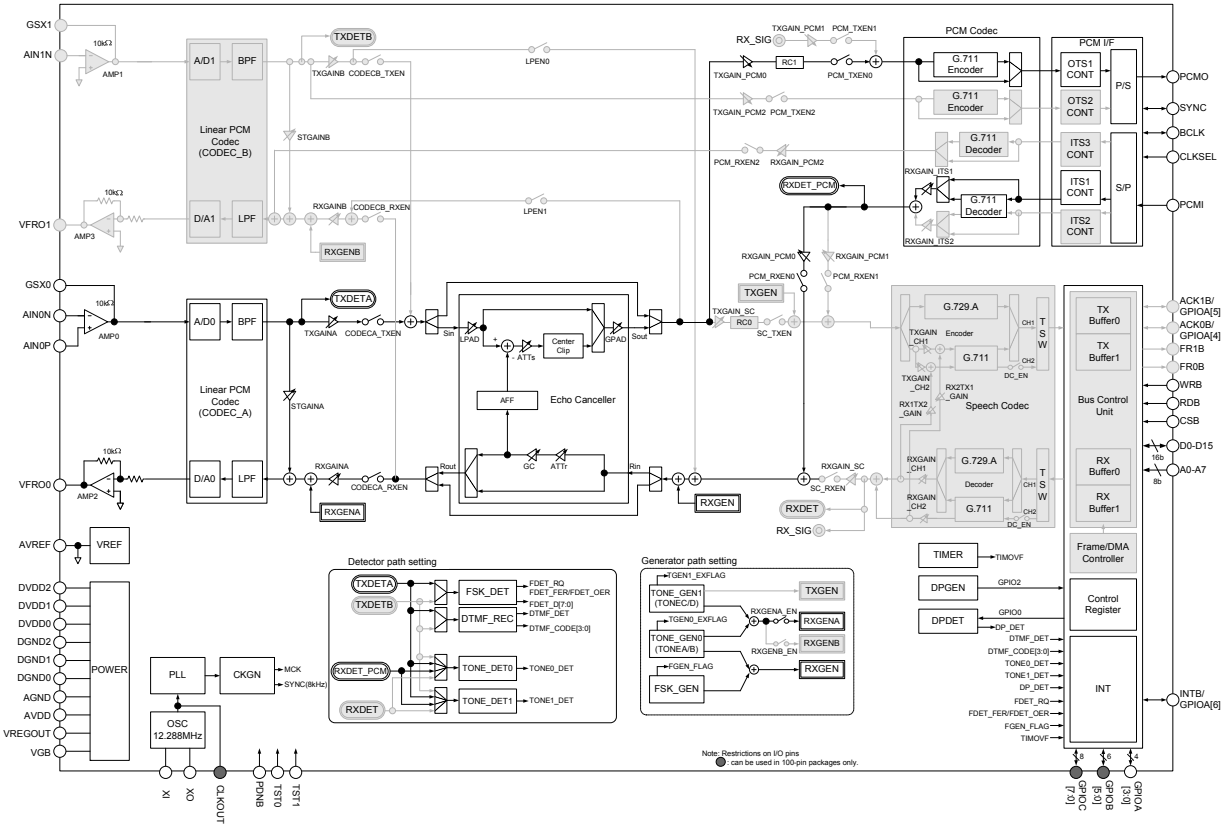
Configuration Example 2 (Basic Call, CODEC_B)



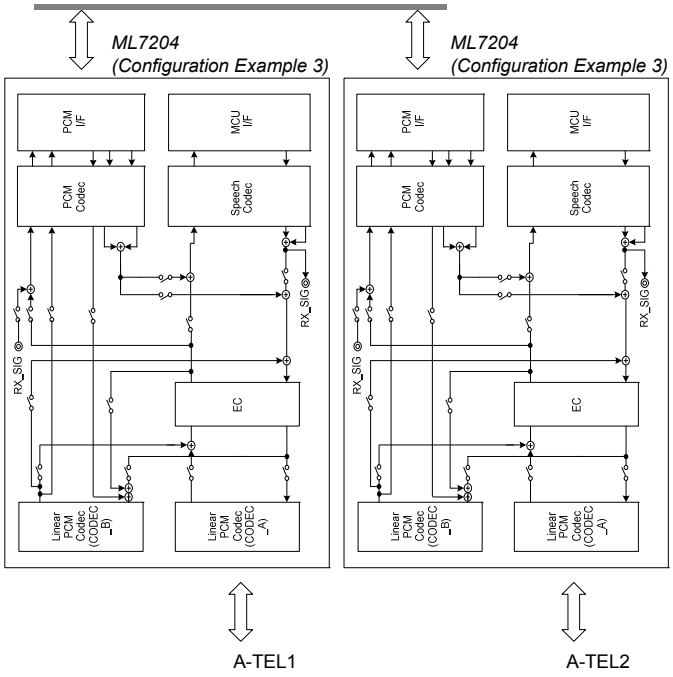
This example shows the configuration for making calls with an analog telephone set (A-TEL) on the NW side by connecting the analog telephone interface on the Linear PCM CODEC_B side.



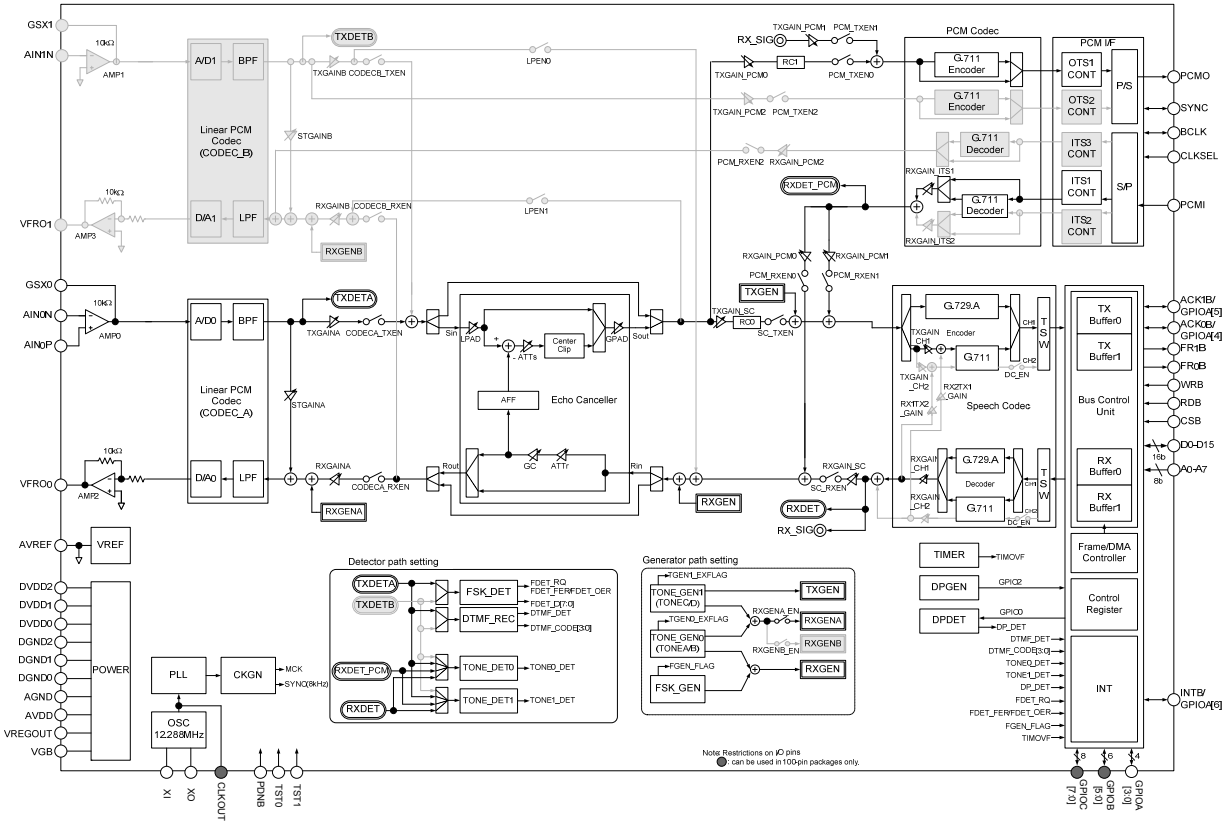
Configuration Example 3 (Calling Using Extension with PCM)



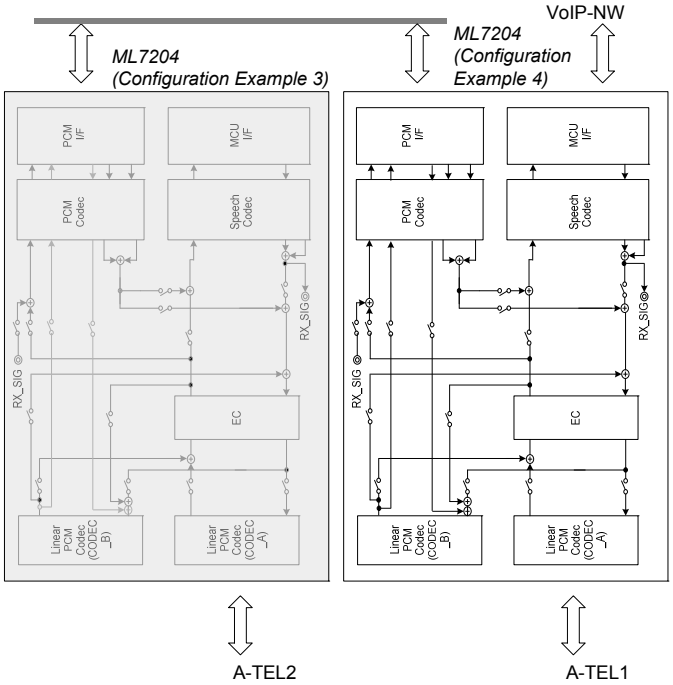
This example shows the configuration for making calls using extension between two analog telephone sets (A-TEL1 and A-TEL2) on the equipment that has two or more analog telephone interface ports.



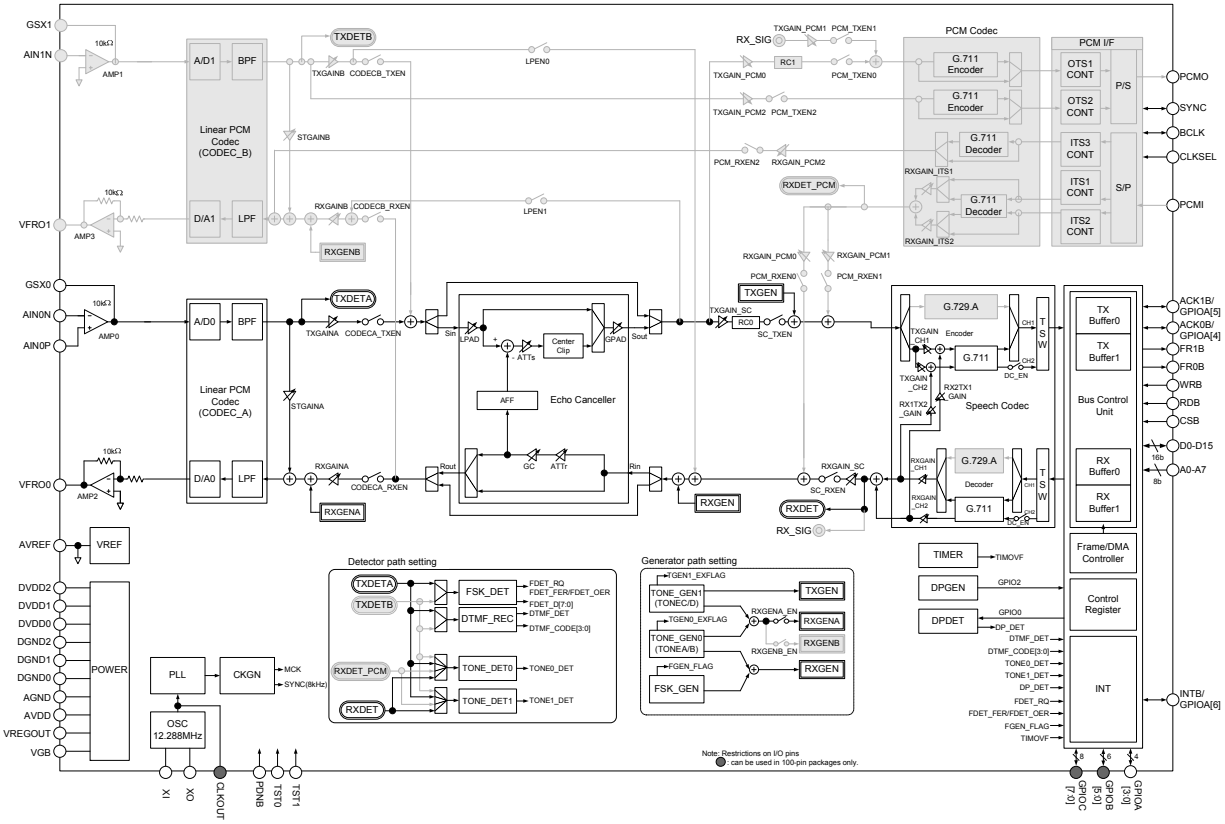
Configuration Example 4 (Three-Way Calling: Terminal Side [Two Parties] – NW Side [One Party])



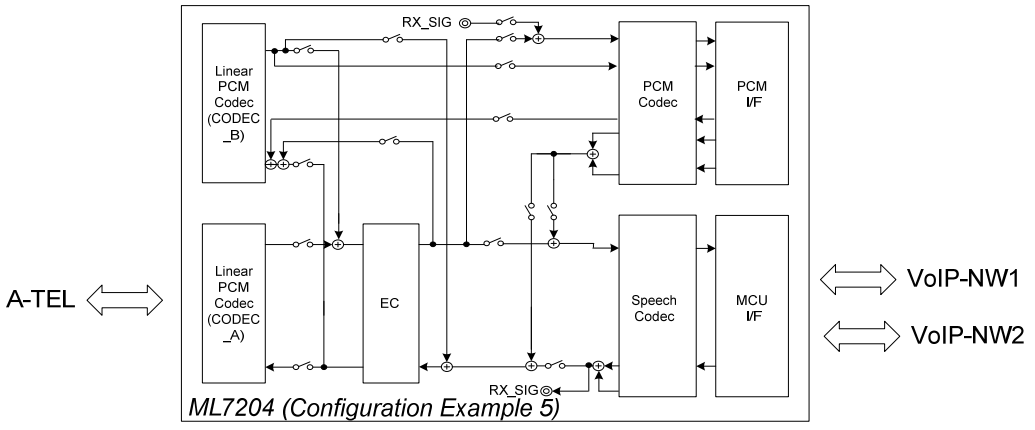
This example shows the configuration for making three-way calling between the terminal side (two parties) and the VoIP NW side (one party).



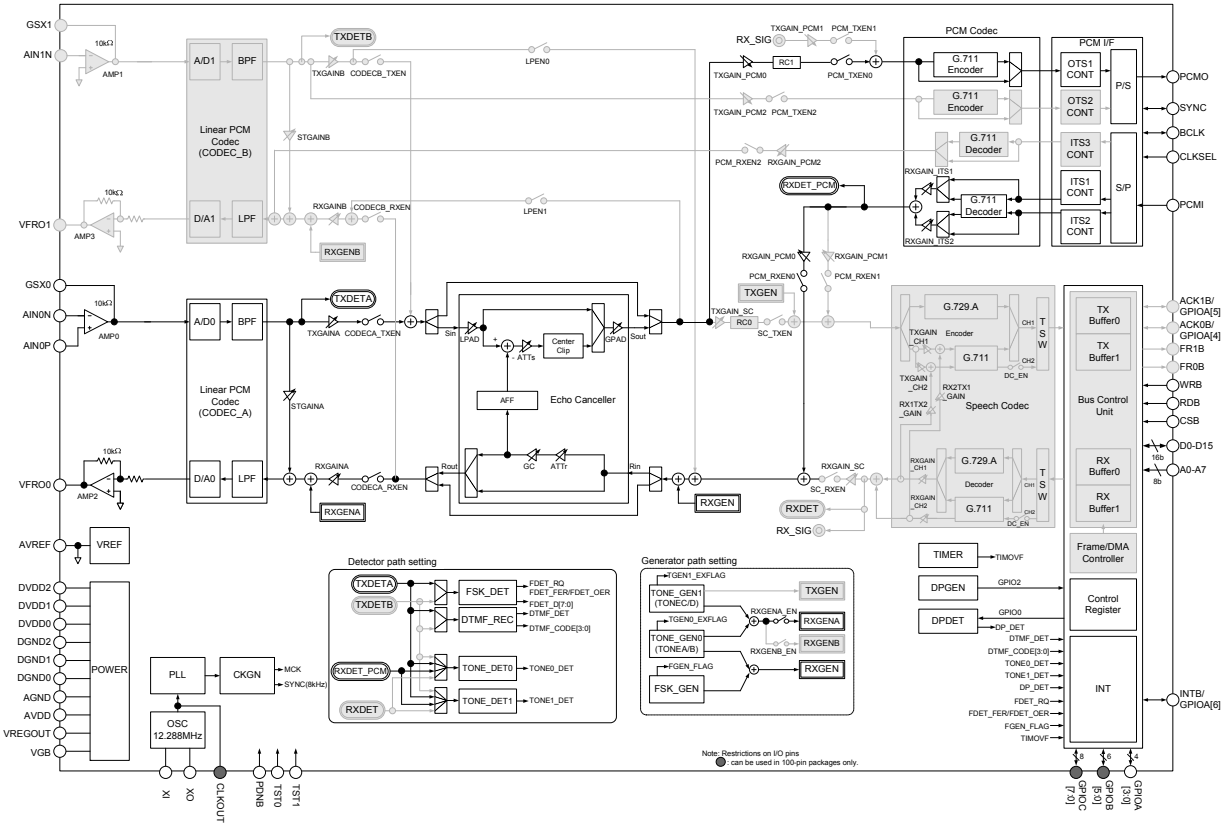
Configuration Example 5 (Three-Way Calling: Terminal Side [One Party] – NW Side [Two Parties])



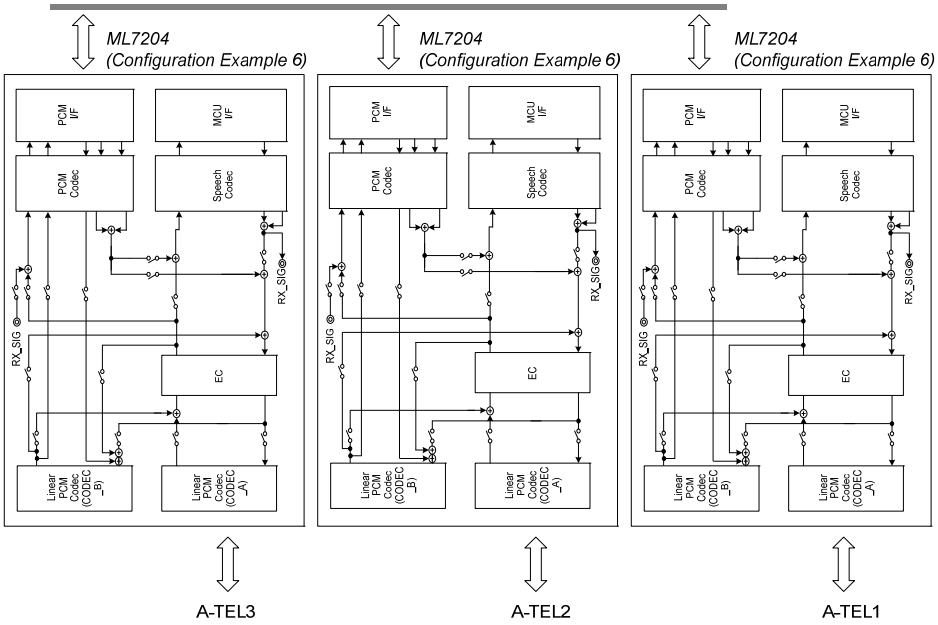
This example shows the configuration for making three-way calling between the terminal side (one party) and VoIP NW side (two parties).



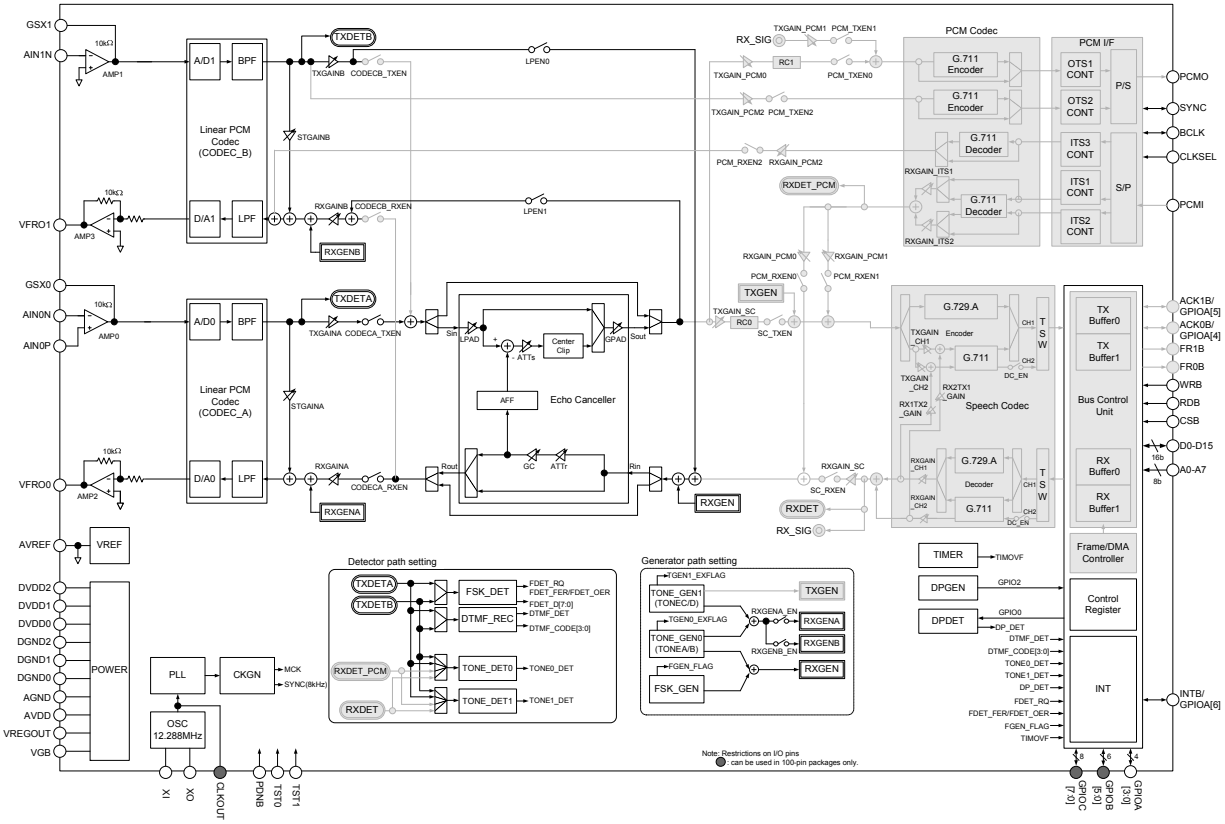
Configuration Example 6 (Three-Way Calling: Terminal Side [Three Parties])



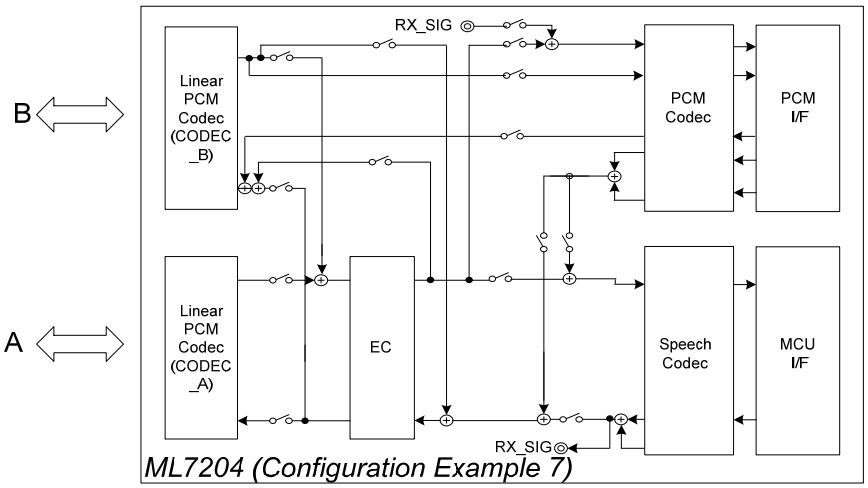
This example shows the configuration for making three-way calling between analog telephones (A-TEL1, A-TEL2, and A-TEL3) on the equipment with multiple analog telephone interface ports.



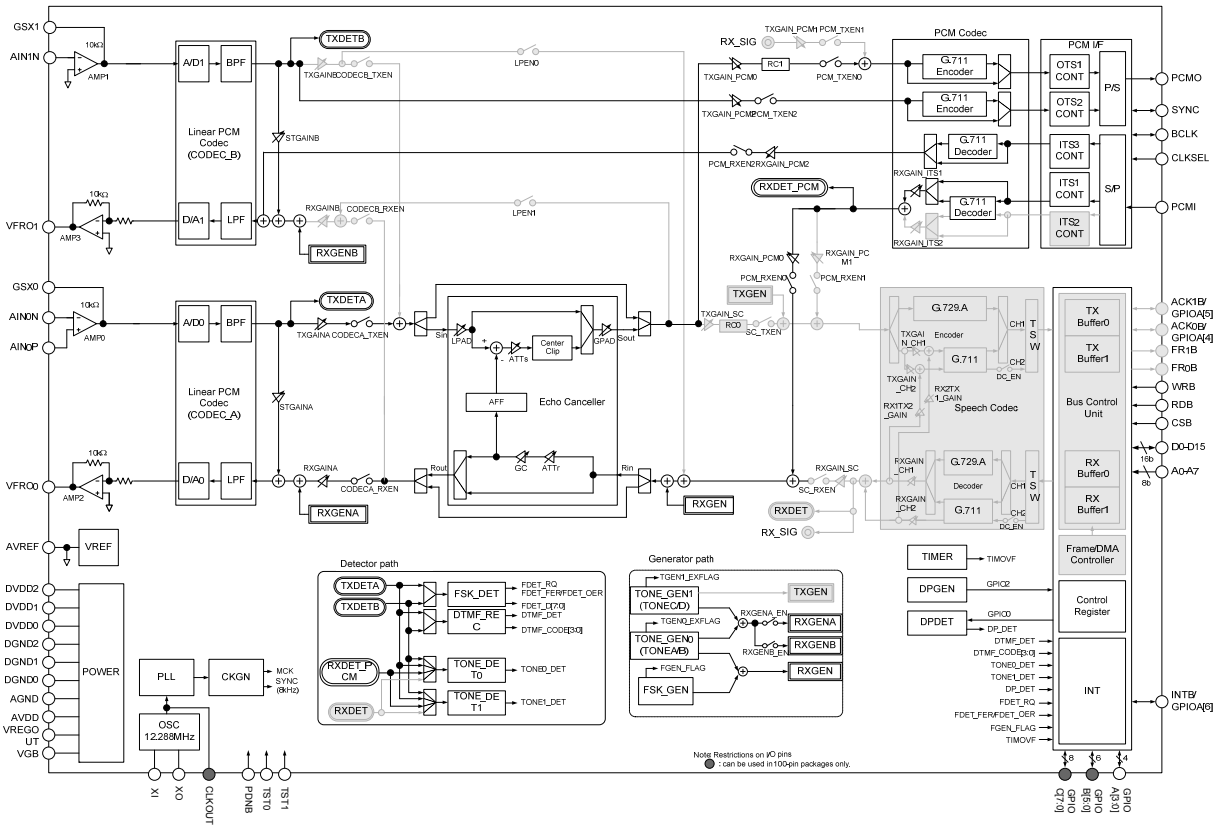
Configuration Example 7 (CODEC-A-CODEC-B Loop Back Mode)



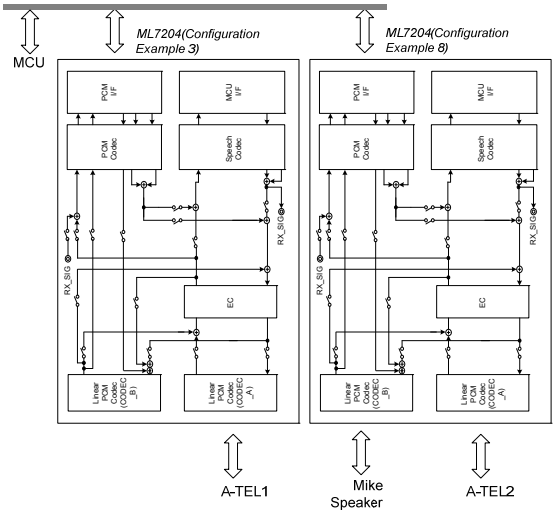
This example shows the configuration where CODEC_A and CODEC_B are connected in loopback mode according to the internal path settings.



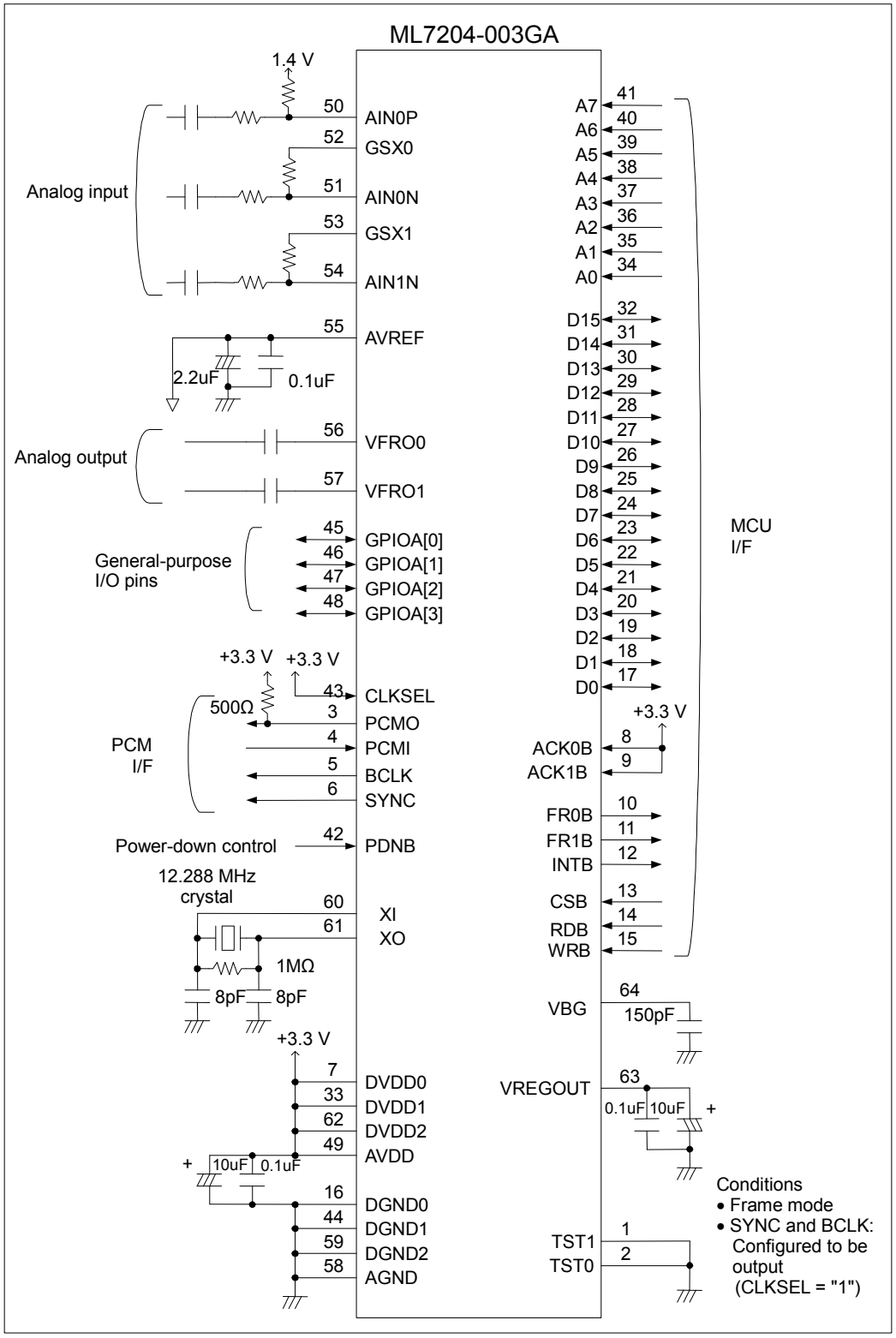
Configuration Example 8 (Calling Using Extension with PCM + Extended Call Functions)



This example shows the configuration for making calls using extension between two analog telephone sets (A-TEL1 and A-TEL2) on the equipment that has two or more analog telephone interface ports. This configuration also supports various functions of extended calling between the Mike/Speaker of A-TEL2 and an MCU.



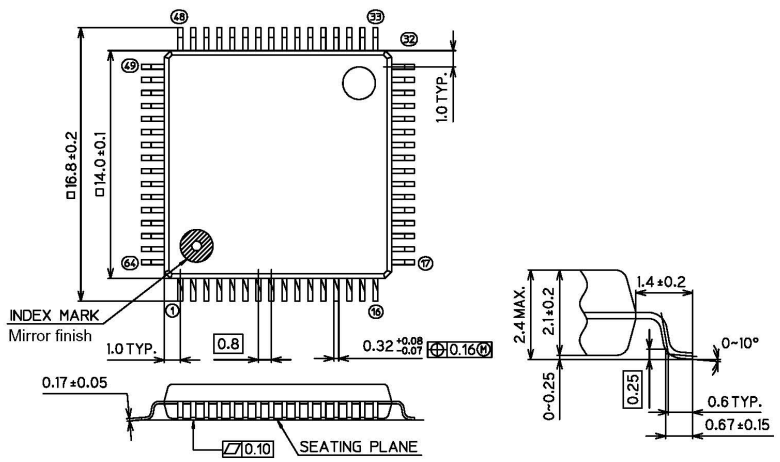
APPLICATION CIRCUITS



PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P-1414-0.80-BK



LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7204-003-01	June 14, 2006	–	–	First Edition
FEDL7204-003-02	Oct 14, 2011	1 - 224	1 - 214	Deletions of 100 pin package type. (ML7204V-003TB)

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