ML7386/7386B

Sub GHz band wireless transmitter IC

■Overview

ML7386/ML7386B are a low power RF transmitter IC for narrowband system. It includes RF part, MOD part and HOST interface part in single-chip. It supports various frequency band from 200 MHz to 972 MHz. It is possible to use as wireless alarm and security systems, low power telemetory and industrial remote control systems.
ML7386 supports only 10mW mode. ML7386B supports both 10mW and 1mW mode.

■Features

- Support 200 MHz to 972 MHz operation. (*1)
- Support narrow band systems with channel spacing of 12.5 or 25 kHz
- High accurate modulation implemented by direct modulation scheme using fractional-N PLL
- Multiple modulation scheme : 2-FSK/MSK
- Data speed : 2400/4800/7200 bps (NRZ coding)
  Extended data rate function can set 1.2kbps to 100kbps (NRZ coding) (*1)
- Supports NRZ code and Manchester code
  In case of using Manchester code, DCLK frequency becomes half to NRZ coding case.
- Programmable frequency deviation: ±0.6kHz to ±100kHz (*1)
- Configurable data polarity
- On chip oscillation cell: 16MHz to 36MHz (*1)
- Support direct input from TCXO: 16MHz to 36MHz (*1)
- Frequency trimming function (Fractional-N PLL architecture enables fine tuning of synthsizer frequency)
- Synchronous serial peripheral interface (SPI)
- Built in voltage regulated Power Amp (PA) and power control function
  ML7386 suppoers 10mW mode only
  ML7386B supports 10mW and 1mW mode.
- Test Pattern generation (PN9, CW, 0/1, all-1, all-0 pattern)
- Power supply voltage : 2.0 V to 3.6V (10mW mode)
  1.8 V to 3.6V (1mW mode)
- Operating temperature -40 to +85 ˚C
- Power consumption (tentative)

Deep Sleep Mode	0.03 uA (Typ.) (Register non-retain)
Sleep Mode	0.3 uA (Typ) (Register retain)
Idle Mode	0.25 mA (Typ) (Oscillator cell OFF)
Stop Mode	1.0 mA (Typ.) (Transmitter OFF)
TX (10mW)	23.8 mA (Typ.) (TCXO mode)
TX (1mW)	6.4 mA (Typ.) (TCXO mode)

- Package
  28 pin WQFN 4.0mm x 4.0mm x 0.8mm
  Pb free, RoHS compliant

*1: These specifications show the setting range base on the ML7386 and ML7386B function.
Performance is guaranteed under the condition specified in “Performance guarantee condition”
If using ML7386 and ML7386B under the condition not specified in “Performance guarantee condition”, evaluation and confirmation should be required under user specific condition.

■Description Convention

1) Numbers description

'0xnn' indicates hexadecimal and '0bnn' indicates binary

Example: 0x11=17 (decimal), 0b11=3 (decimal)

2) Register description

[<register name>: <register address>] register

Example: [RF_MODE: 0x00] register
Register name: RF_MODE
Register address: 0x00

3) Bit name description

<bit name> ([<register name>: <register address> (<bit location>)])

Example: txtest_en([TXD_SEL: 0x02(3)])
Bit name: test_en
Register name: TXD_SEL
Register address: 0x02
Bit location: bit3

■Block Diagram

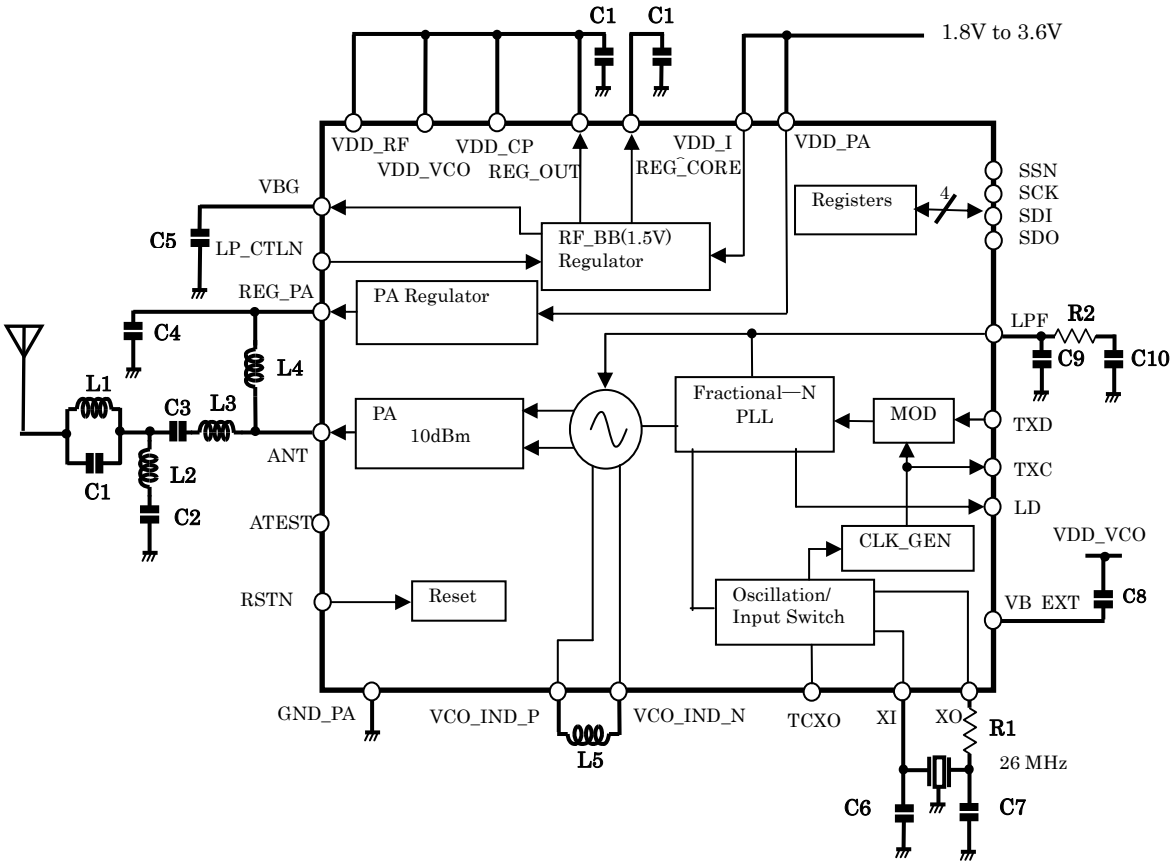


Fig.1 Block diagram

■PIN Assignment

28 pin WQFN

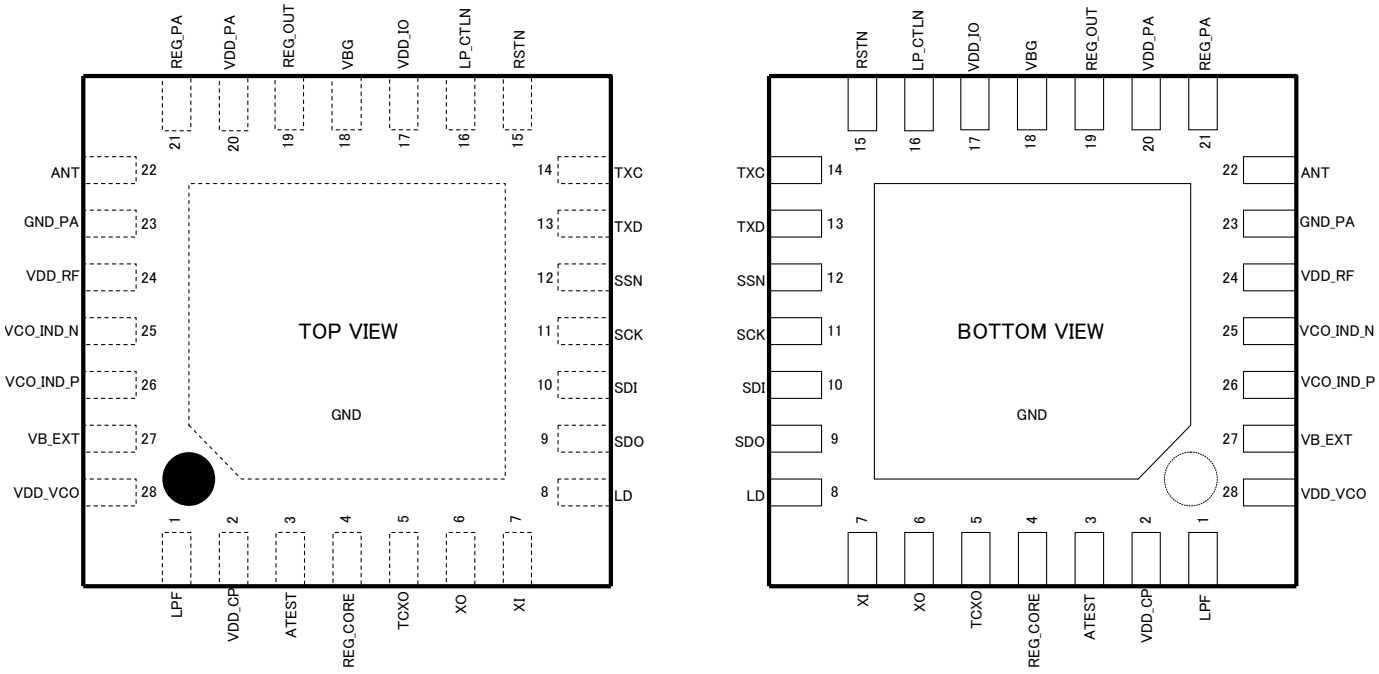


Fig.2 PIN ASSIGNMENT

NOTE: Pattern shown in the centre of the chip is located at bottom side of the chip (GND PAD)

■PIN Definitions

Symbols

I_{RF}	: RF input
O_{RF}	: RF output
I_A	: Analog input
I_{OSc}	: Oscillator input
O_{OSc}	: Oscillator output
I	: Digital input
O	: Digital output
Is	: Schmitt Trigger input

●RF / Analog pins

Pin No	Pin name	I/O	Active Level	at reset	Detail function
1	LPF	I_{RF}	-	-	PLL loop filter pin
3	ATEST	O_{RF}	-	O	Analog test output
22	ANT	O_{RF}		O	RF signal output to antenna
25	VCO_IND_N	-	-	-	Pin for external inductor of VCO
26	VCO_IND_P	-	-	-	Pin for external inductor of VCO
38	VB_EXT	-	-	-	External capacitor pin for local oscillator stability

●SPI interface pins

Pin No	Pin name	I/O	Active Level	at reset	Detail function
9	SDO	O	-	L	SPI data output
10	SDI	I	-	I	SPI data input
11	SCK	Is	P	I	SPI clock input SDI is captured at rising edge SDO is output at falling edge
12	SSN	Is	L	I	SPI enable input

●TX data interface pins

Pin No	Pin name	I/O	Active Level	at reset	Detail function
13	TXD	I	-	I	TX data input
14	TXC	O	P	L	TX clock output TXD is captured at rising edge

●Regulator pinst

Pin No	Pin name	I/O	Active Level	at reset	Detail function
4	REG_CORE	-	-	-	Monitor pin for power supply to digital core (typ.1.5V) Connection for external capacitor with 10uF
18	VBG	-	-	-	Back bias pin. Connection for external capacitor with 0.1 µF.
19	REG_OUT	-	-	-	Regulator output (typ.1.5V) Connection for external capacitor with 6.8 µF
21	REG_PA	-	-	-	Regulator output for PA. (1.5V to 2.0V) Connection for external capacitor with 1 uF.

●Miscellaneous

Pin No	Pin name	I/O	Active Level	at reset	Detail function
5	TCXO	I_A	-	I	External clock (TCXO) input pin. *Fixed to GND level when crystal oscillator is used.
6	XO	Oosc	-	O	26MHoecillator pin2 *Fixed to GND level when external clock generator is used
7	XIN	Iosc	-	I	26MHz oscillator pin1 *Fixed to GND level when external clock generator is used
8	LD *1	O	H	L	PLL Lock detect pin L: PLL unlock status H: PLL lock status
15	RSTN	Is	L	I	Hardware reset L: Rest, stop H: Normal operation
16	LP_CTLN	I	L	I	Sleep mode control pin L: Deep sleep mode H: Exit from deep sleep mode

*1 Activated when write 0x18 to the [RF_MODE: 0x00] register.

●Power Supply

Pin No	Pin name	I/O	Active Level	at reset	Detail function
2	VDD_CP	-	-	-	Power supply pin for PLL charge pump block. (Connection for REG_OUT pin. Typ.1.5V)
17	VDD_IO	-	-	-	Power supply for digital IOs (Input voltage from 1.8 V to 3.3 V)
20	VDD_PA	-	-	-	Power supply pin for PA block. (Input voltage from 1.8V to 3.3V)
23	GND_PA	-	-	-	GND pin for PA block.
24	VDD_RF	-	-	-	Power supply pin for RF blocks. (Connection for REG_OUT pin. Typ.1.5V)
28	VDD_VCO	-	-	-	Power supply pin for VCO block. (Connection for REG_OUT pin. Typ.1.5V)

●Unused pins

Followings are recommendation for unused pins

Pin Name	Recommendation
XO	Fixed to GND (When TCXO is used)
XI	Fixed to GND (When TCXO is used)
TCXO	Fixed to GND (When Crystal OSC is used)
ATEST	Left OPEN

(Note)
If input pins are high-impedence state and leave open, excess current could be drawn. Care must be taken that unused input pins and unused I/O pins should not be left open.

■Electrical Characteristics

●Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Power Supply (I/O) (*1)	V_{DDIO}	Ta=-40 to 85°C GND=0V	-0.3 to +4.6	V
Power Supply (RF) (*2)	V_{DDRF}		-0.3 to +2.0	V
Digital Input Voltage	V_{DIN}		-0.3 to V_{DDIO}+0.3	V
RF Input Voltage	V_{RFIN}		-0.3 to V_{DDRF}+0.3	V
Analog Input Voltage	V_{AIN}		-0.3 to V_{DDIO}+0.3	V
Analog Input Voltage2 (*3)	V_{AIN2}		-0.3 to V_{DDRF}+0.3	V
Digital Output Voltage	V_{DO}		-0.3 to V_{DDIO}+0.3	V
RF Output Voltage	V_{RFO}		-0.3 to V_{DDRF}+0.3	V
Analog Output Voltage	V_{AO}		-0.3 to V_{DDIO}+0.3	V
Analog Output Voltage2 (*4)	V_{AO2}		-0.3 to V_{DDRF}+0.3	V
Digital Input Current	I_{DI}		-10 to +10	mA
RF Input Current	I_{RF}		-2 to +2	mA
Analog Input Current	I_{AI}		-2 to +2	mA
Analog Input Current2 (*3)	I_{AI2}		-2 to +2	mA
Digital Output Current	I_{DO}		-10 to +10	mA
RF Output Current	I_{RFO}		-2 to +2	mA
Analog Output Current	I_{AO}		-2 to +2	mA
Analog Output Current2 (*4)	I_{AO2}		-2 to +2	mA
Power Dicipatin	P_d	Ta=+25°C	500	mW
Storage Temperature	T_{stg}	-	-55 to +125	°C

(*1) VDD_IO, VDD_PA pins
(*2) VDD_RF, VDD_VCO, VDD_CP pins
(*3) XI pins
(*4) XO pin

●Recommended Operating Conditions

Item	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply (I/O)	V_{DDIO}	VDD_IO, VDD_PA pins	1.80	2.70	3.60	V
Power Supply (RF)	V_{DDRF}	VDD_RF, VDD_VCO, VDD_CP pins	1.45	1.50	1.55	V
RF characteristic temperature	T_a	-	-25	+25	+85	℃
Operating Temperature	T_a	-	-40	+25	+85	℃
Rising time Digital Input	T_{IR1}	Digital input pins (*1)	−	−	20	ns
Falling time Digital Input	T_{IF1}	Digital Input pins (*1)	−	−	20	ns
Output loads Digital Ouput	C_{DL}	All Digital Output pins	−	−	50	pF
Master Clock1	F_{MCK1}	XIN, XOUT pins (*2)	-4ppm	26	+4ppm	MHz
Master Clock2	F_{MCK2}	TCXO pin (*2)	-4ppm	26	+4ppm	MHz
TX clock Output	F_{CLKOUT}	TXC pin	-400ppm -200ppm -200ppm	7200 4800 2400	+400ppm +200ppm +200ppm	Vpp
SPI clock frequency	F_{SCLK}	SCLK pin	0.1	2	8	MHz
SPI clock duty ratio	D_{SCLK}	SCLK pin	45	50	55	%
RF frequency	F_{RF1}	ANT pin 12.5kHz channel spacing	426.2500	−	426.8375	Mhz

(*1) Those pines with symbol I or Is at I/Ocolumn in the Pin Definition section
(*2) Minimum and maximum limit are defined in standards. Please refer standards, i.e ARIB STD-T67, RCR STD-30 and so on.

●Power Consumption

(Condition: VDDIO=1.8V to 3.6V, Ta=-40˚C to + 85˚C, Fmck=26MHz)

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Power Consumption (*1)	I_{DDS1}	Deep Sleep state (Registers are not retained)	−	0.03	15.0	µA
	I_{DDS2}	Sleep state (Registres are retained)	−	0.3	30.0	µA
	I_{DD1}	Idle state (*3) (OSC circuit OFF, RF OFF)	−	0.25	1.5	mA
	I_{DD2}	Stop state (OSC circuit ON, RF OFF)	−	0.65	3.0	mA
	I_{DD3}	TX state (10mW) (*4), (*5)	−	23.8	52.0	mA
	I_{DD4}	TX state (1mW) (*4), (*5)	−	6.4	20.0	mA

(*1) Power consumption is sum of current consumption of all power supply pins
(*2) “Typ” value is centre value under condition of VDDIO=2.7V, 25 °C .
(*3) If using SPI access with 8 MHz speed, specified current is added to the each value.
(*4) SPI access speed is 2 MHz and data transmission speed at 4800 bps
(*5) In case of using TCXO. In case of using crystal, adding 0.3mA under the typical condtiion.

●DC Characteristics

(Condition: VDDIO=1.8V to 3.6V, V_{DDR1}=1.45V to 1.55V, Ta=-40˚C to + 85˚C, Fmck=26MHz)

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Voltage Input High	VIH1	(*1), (*2)	V_{DDIO} * 0.77	–	V_{DDIO}	V
	VIH2	XI pin	V_{DDRF} * 0.9	–	V_{DDRF}	V
Voltage Input Low	VIL1	(*1), (*2)	0	–	V_{DDIO} * 0.18	V
	VIL2	XI pin	0	–	V_{DDRF} * 0.10	V
Input Voltage	VI	TCXO pin	0.8	–	V_{DDRF}	Vp-p
Threshold Voltage High level	VT+	(*2)	–	1.2	V_{DDIO} * 0.77	V
Threshold Voltage Low level	VT-	(*2)	V_{DDIO} * 0.18	0.8	–	V
Input Leakage Current	IIH1	VIH = V_{DDIO} (*1), (*2)	-2	–	2	µA
	IIL1	VIL = 0 V (*1), (*2)	-2	–	2	µA
Voltage Ouput level H	VOH	IOH=-4 mA (*3)	V_{DDIO} * 0.78	–	V_{DDIO}	V
Voltage Ouput level L	VOL	IOL= 4 mA (*3)	0	–	0.3	V
Regulator output voltage	REG_CORE	Sleep state	–	1.3	–	V
		Other states	–	1.5	–	V
	REG_OUT	Exclude sleep state	–	1.5	–	V
Input Capacitance	CIN	Input pins (*1),(*2)	–	6	–	pF
	COUT	Output pins (*3)	–	9	–	pF
	CRFI	RF input pins (*4)	–	9	–	pF
	CRFO	RF output pins (*5	–	9	–	pF
	CAI	Analog input pins (*6)	–	9	–	pF

(*1) Pins with symbol I at the I/O column in the Pin Definitions section
(*2) Pins with symbol Is at the I/O column in the Pin Definitions section
(*3) Pins with symbol O ar the I/O column in the Pin Definitions section. XO pin is excluded
(*4) Pins with symbol I_{RF} at the I/O column in the Pin Definitions section
(*5) Pins with symbol O_{RF} at the I/O column in the Pin Definitions section
(*6) Pins with symbol I_A at the I/O column in the Pin Definitions section

●RF Characteristics

[Performance guarantee condition]

Data Rate	:	2400 bps / 4800 bps / 7200 bps
Modulation scheme	:	2-FSK/MSK
Channel spacing	:	12.5 kHz / 25.0 kHz
Frequency	:	426.0250 MHz to 426.8375MHz
Power supply	:	1.8V to 3.6V (unless specifing alternate condition)
Temperatute	:	-25°C to 85 °C (unless specifing alternate condition)
Master clock	:	26 MHz (unless specifing alternate condition)

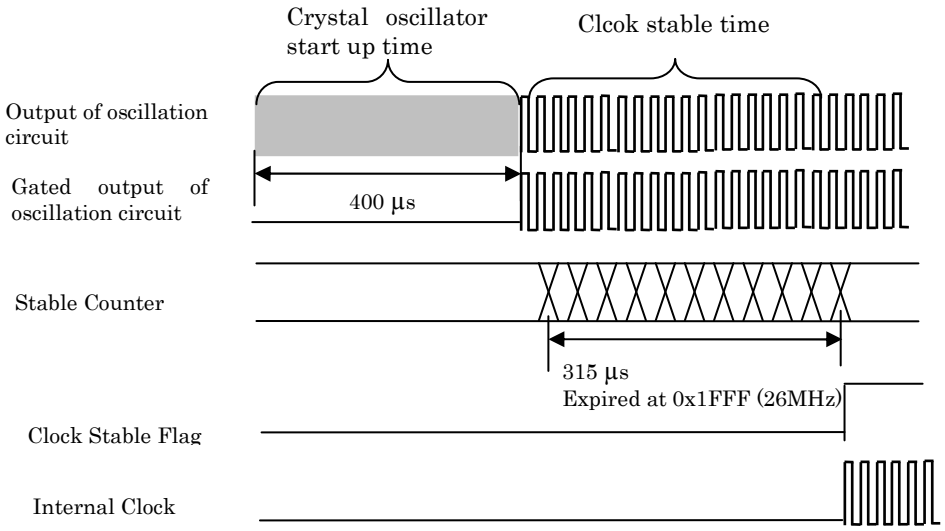
[Start up time]

Item	Condition	Min	Typ	Max	Unit
Regulator start up time	LP_CTLN = H	-	600	1500	µs
Crystal oscillator start up time (*1)	26 MHz	-	715	1115	µs
TX start up time (*2)	PLL amd PA start up time (TCXO mode :IDLE mode) (OSC mode :STOP mode)	-	1460	1600	µs
PLL lock up time (*3)	frequency change in TX state	-	50	100	µs

[TX]

Item	Condition	Min	Typ	Max	Unit
TX Power (10 mW mode) (*4)	[PA_ADJ:0x10]=0xnn	5	–	12	mW
TX Power (1 mW mode) (*4), (*7)	[PA_ADJ: 0x10]=0xnn [PA_BIAS:0x16]=0xnn	0.5	–	1.2	mW
Adjacent Channel Power Ratio [ACPR] (*5)	±12.5kHz offset ± 4.25 kHz bandwidth 4800 bps, Fdev=2.1 kHz		-48	-40	dBc
Occupied bandwidth [OBW]	99%, 4800 bps, Fdev=2.1 kHz	4.0	–	8.5	kHz
Frequency deviation range (*6)		±0.6	–	±4.2	kHz
Modultation index	MSK 4800 bps, Fdev=1.2 kHz	0.49	0.50	0.51	-
Spurious emission radiated CW	10mW output	–	-32	-26	dBm
Adjacent spurious emission	PN9, 10mW output ±112.5kHz offset ± 50 kHz bandwidth 4800 bps, Fdev=2.1 kHz	–	-32	-26	dBm

(*1) The time to output rectangular clock from oscillation circuit into the stable counter from setting STOP mode (0x10) to [RF_MODE:0x00] register. After counting 0x1FFF, the oscillation block output to internal circuits and enable to start TX operation.



(*2) The time to converge in ±10 kHz of PLL frequency from setting ACT mode (0x18) into [RF_MODE:0x00] register. LD pin will rise before PLL is converged.
(*3) When in operating F0 with TX state, the transition time to converge in ±10 kHz in PLL frequency (F1).
(*4) Fine adjustment of PA_ADJ value is required because of variation of external components or PCB. Output power may be varied depending on temperature or power supply variation. It is recommended to adjust [PA_ADJ:0x10] register in order to meet required power.(*5) ACPR performance is result after adjusting channel frequency within +/-0.25ppm accuracy.
(*6) Frequency deviation range and RF channel frequency are showing possible range, it is not guranteed the all performance described in this data sheet.
(*7) 1mW mode is applied to ML7386B only.

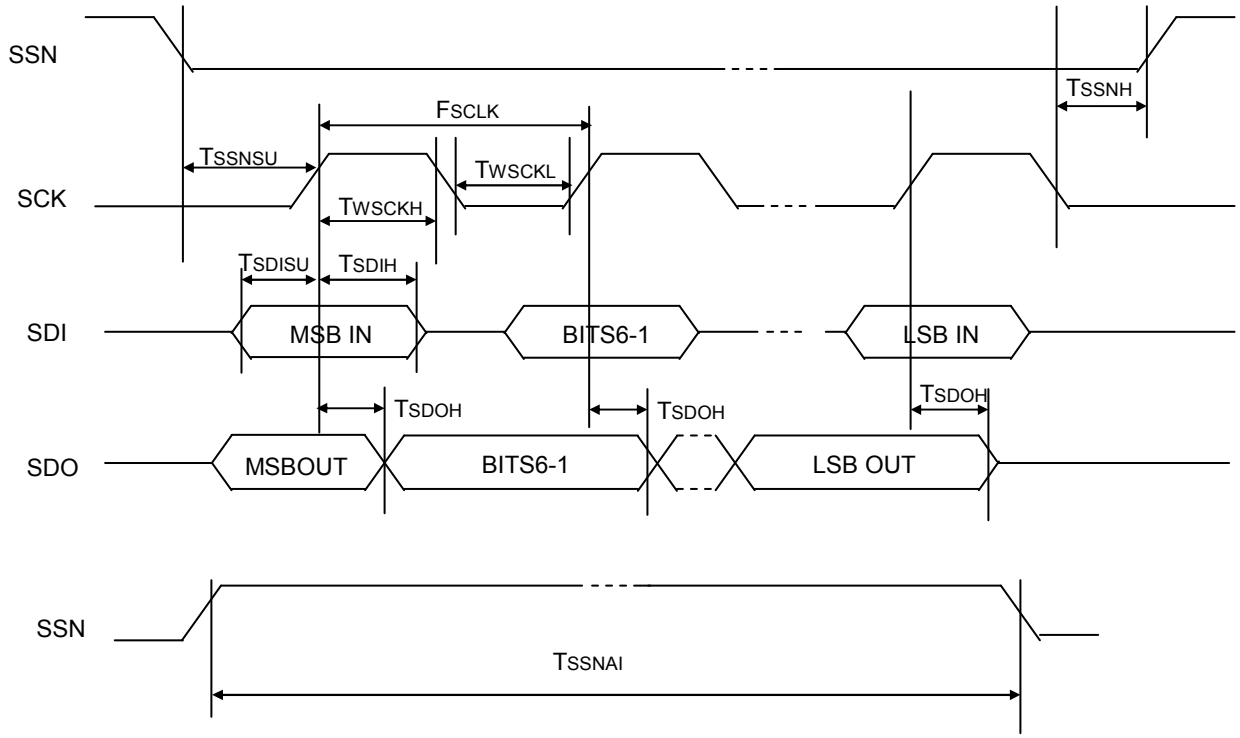
■Timing Characteristics

●SPI interface

(Condition: VDDIO=1.8V to 3.6V, Ta=-40˚C to + 85˚C)

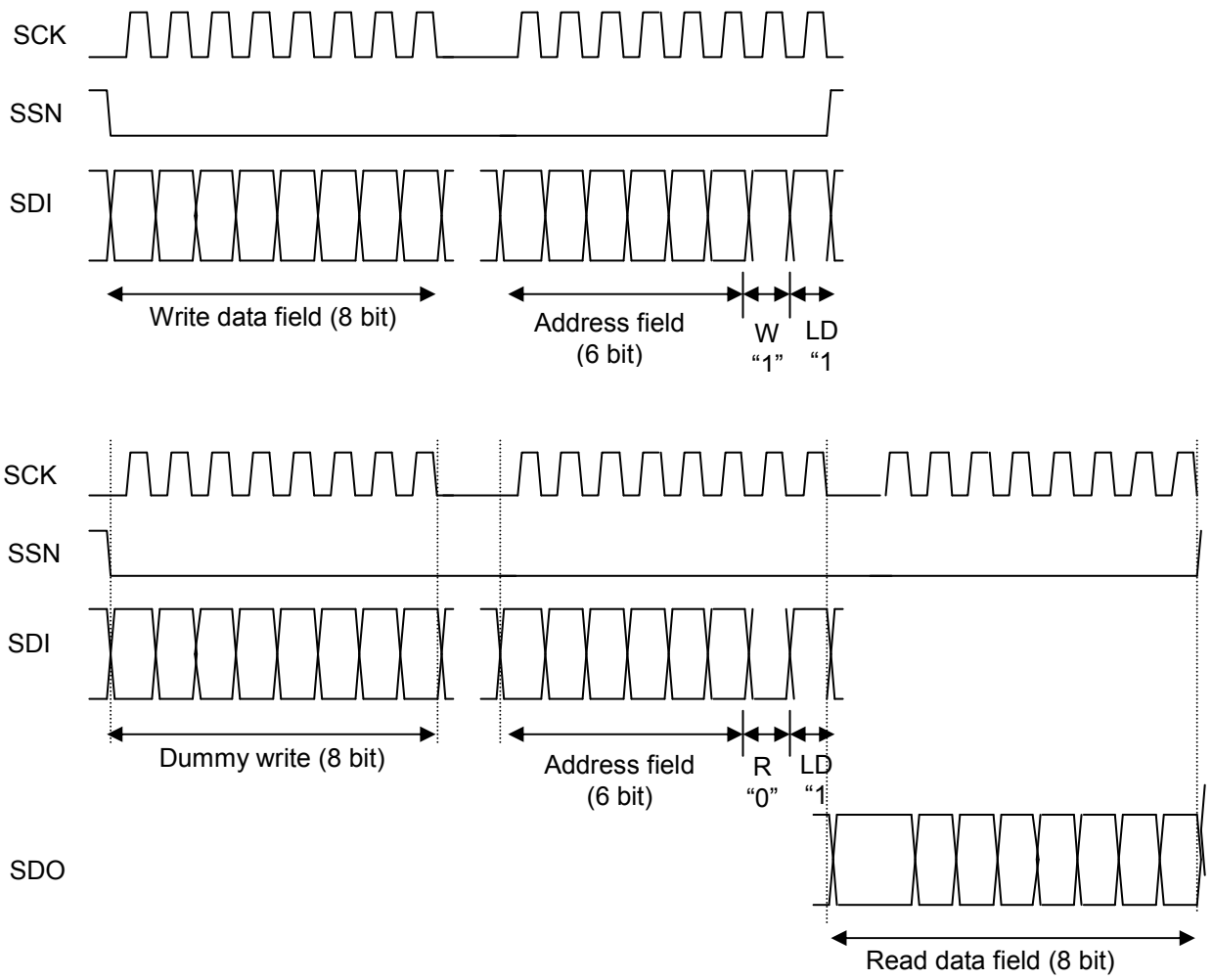
Item	Symbol	Condition	Min	Typ	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL=20pF	0.1	2	8	MHz
SSN input setup time	TSSNSU		125	–	–	ns
SSN input hold time	TSSNH		20	–	–	ns
SCK high pulse width	TWSCKH		56	–	–	ns
SCK low pulse width	TWSCKL		56	–	–	ns
SDI input setup time	TSDISU		5	–	–	ns
SDI input hold time	TSDIH		15	–	–	ns
SSN assert interval	TSSNAI		125	–	–	ns
SDO output delay	TSDOH		SCK high pulse width	–	SCK 1 clock	ns

NOTE: All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%.



SCK has to be “L” when it is not active.

SPI Data format

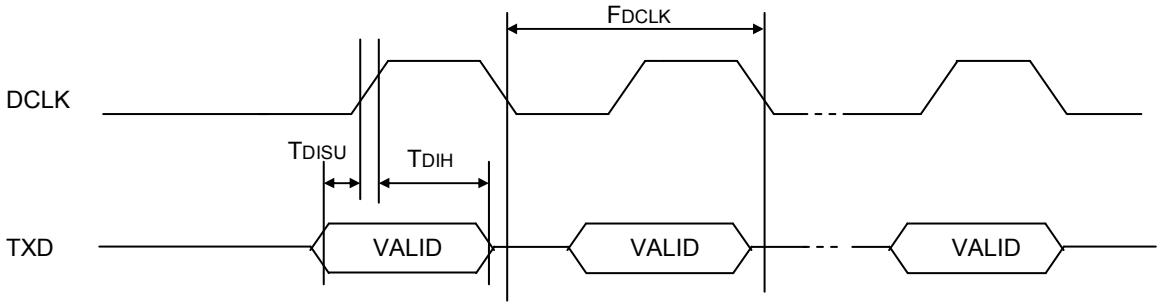


●TX Data interface

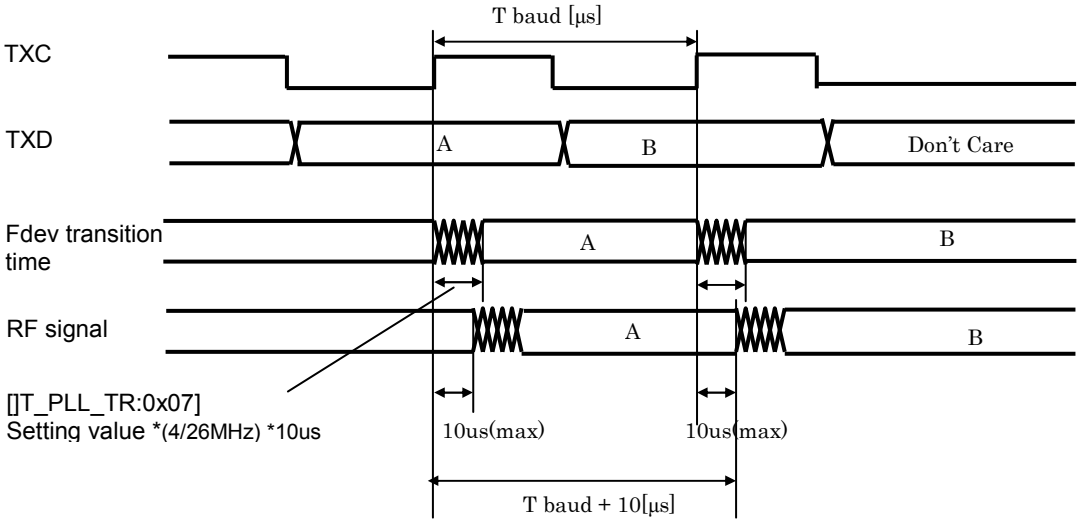
(Condition: VDDIO=1.8V to 3.6V, Ta=-40˚C to + 85˚C)

Item	Symbol	Condition	Min	Typ	Max	Unit
TXD Input setup time	T_{DISU}	Load capacitance CL=50pF	5	–	–	µs
TXD Input hold time	T_{DIH}		5	–	–	µs
TXC clock frequency	F_{DCLK}		-400 ppm -200 ppm -200 ppm	7200 4800 2400	+400 ppm +200 ppm +200 ppm	kHz

NOTE: All timing parameter is defined at voltage level of V_{DDIO} x 20% and V_{DDIO} x 80%.



[Delay timing of demodulated RF signal]



[Note]

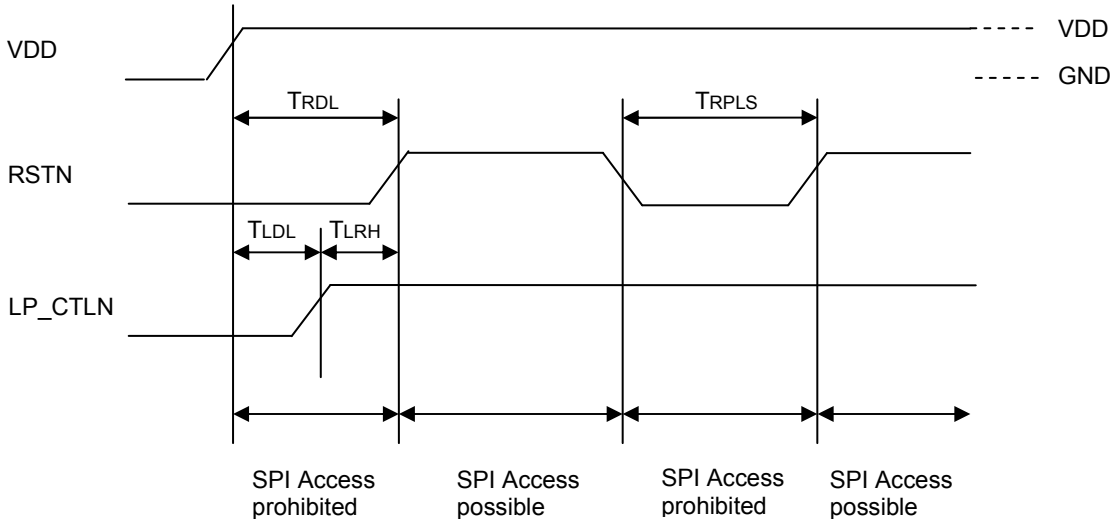
After data input is end at TX data interface, valid RF signal is still transmitting due to demodulation delay. When transit from ACT mode by [RF_MODE: 0x00] register, this delay timing should be considered.

●Power ON

(Condition: VDDIO=1.8V to 3.6V, Ta=-40˚C to + 85˚C)

Item	Symbol	Condition	Min	Typ	Max	Unit
RESETN delay time (Power on)	T_{RDL}	All power supply pins (After power on)	1.6	–	–	ms
RESETN assert time (pulse width)	T_{RPLS}		200	–	–	ns
LP_CNLN delay time (Power on)	T_{LDL}	All power supply pins (After power on)	100	–	–	µs
LP_CTLN rising time	T_{LRH}	VDD="H"	1.5	–	–	ms

NOTE: All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%.

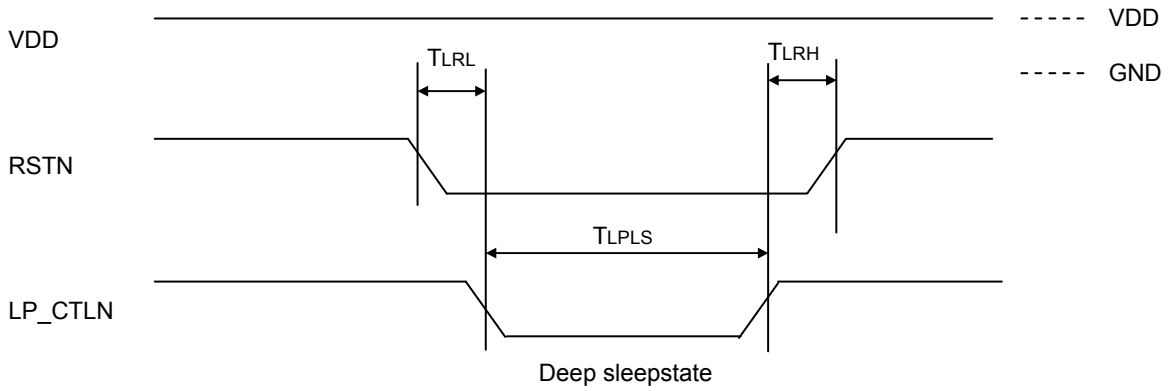


●Low Power Control interface

(Condition: VDDIO=1.8V to 3.6V, Ta=-40˚C to + 85˚C)

Item	Symbol	Condition	Min	Typ	Max	Unit
LP_CTLN falling time	T_{LRL}	VDD="H"	0	−	−	µs
LP_CTLN pulse width	T_{LPLS}	VDD="H"	1200	−	−	µs
LP_CTLN rising time	T_{LRH}	VDD="H"	1.5	−	−	ms

NOTE: All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%.



●State Transition

ML7386/ML7386B has 5 operating modes. Except for Deep Sleep state, state transition is available by [RF_MODE: 0x00] register.

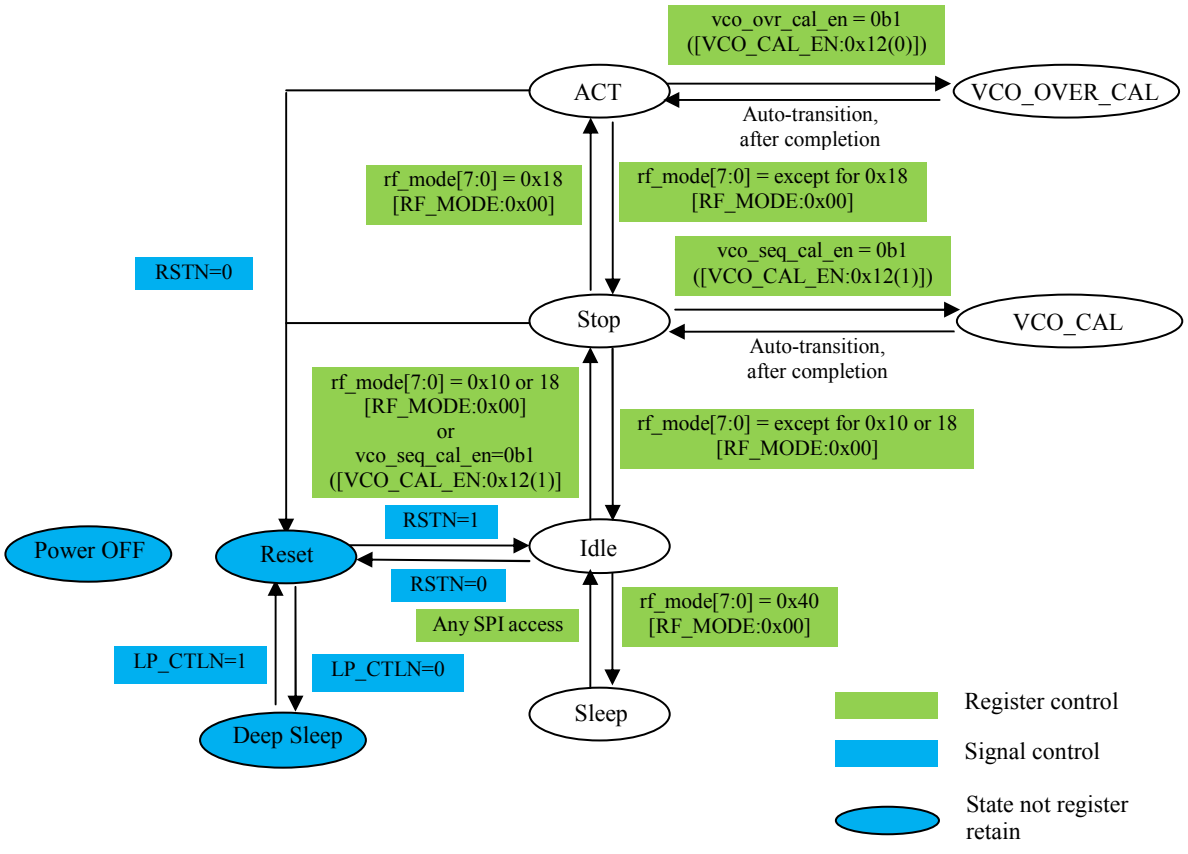
- Deep Sleep state: Shut down the LSI and current consumption is minimum.
- Sleep state: Retain register values and minimized current consumption.
- Idle state: Register access is available and oscillation circuit is off state.
- Stop state: Register access is available and oscillation circuit is on state.
- ACT state: RF circuit is on state.

Block condition in each state is shown as below table.

State	Registers	SPI Access	Oscillation Circuit	RF Circuit	Current (Typ.)
Deep Sleep	Not Retain	Not available	OFF	OFF	0.03μA
Sleep	Retain	Not available (*1)	OFF	OFF	0.3μA
Idle	Retain	Available	OFF	OFF	0.25mA
Stop	Retain	Available	ON	OFF	0.65mA
Act	Retain	Available	ON	ON	23.8mA(10mW) 6.4mA (1mW)

*1: In the Sleep state, only the Idle state transition command is acceptable.

[State Diagram]



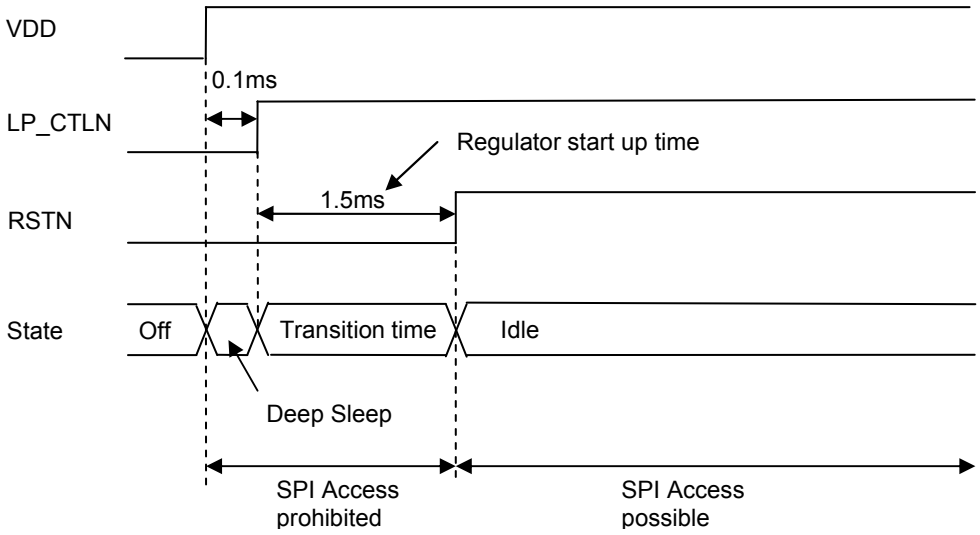
Required wait time at each state transition is shown as below table.

No.	Current state	State to be moved	Possibility	rf_mode[7:0] [RF_MODE:0x00]	Required Wait Time [ms] (*2)
1	Sleep	Idle	O	0x00	1.5
2	Sleep	Stop	O	0x10	2.3
3	Sleep	ACT	X (*1)	-	-
4	Idle	Sleep	O	0x40	0.1
5	Idle	Stop	O	0x10	0.8
6	Idle	ACT	O	0x18	2.715
7	Stop	Sleep	O	0x40	0.1
8	Stop	Idle	O	0x00	0.1
9	Stop	ACT	O	0x18	1.6
10	ACT	Sleep	O	0x40	0.12
11	ACT	Idle	O	0x00	0.1
12	ACT	Stop	O	0x10	0.1

*1: The state transition from Sleep state to ACT state is proghibited. Once Idle transiion is necessary.
In this case, total transition time 1.5ms + 2.715ms = 4.215ms
*2: During the waiting time, [RF_MODE:0x00, [CLK_SEL:0x0E]and [VCO_CAL_EN:0x12] register accesses are prohibited.

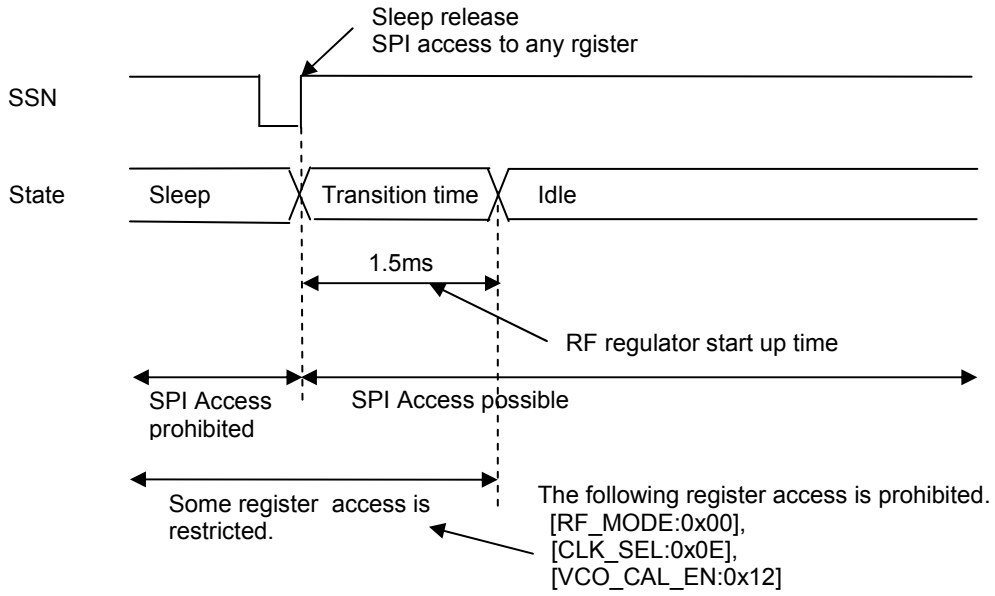
[Off to Idle]

The following shows the operation timing from power off state to Idle state.



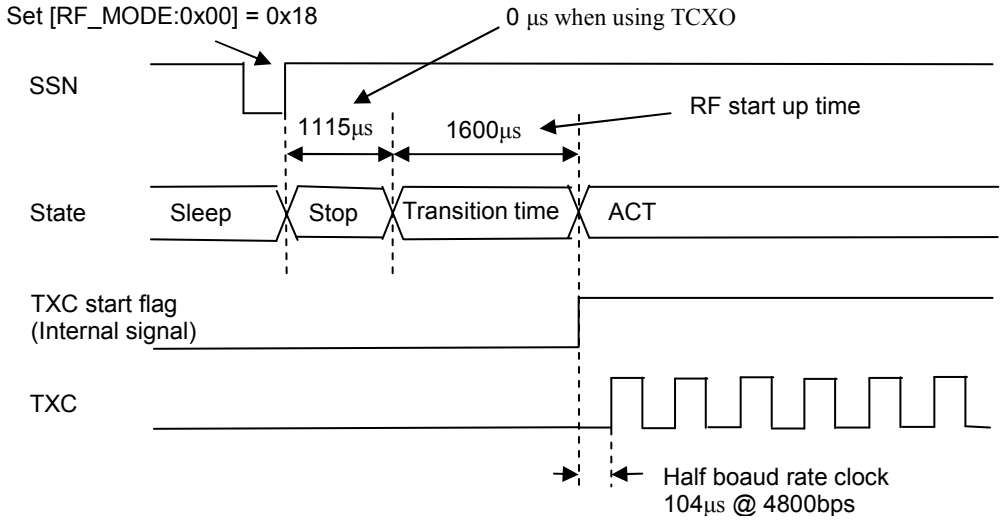
[Sleep to Idle]

The following shows the operation timing from sleep state to Idle state.



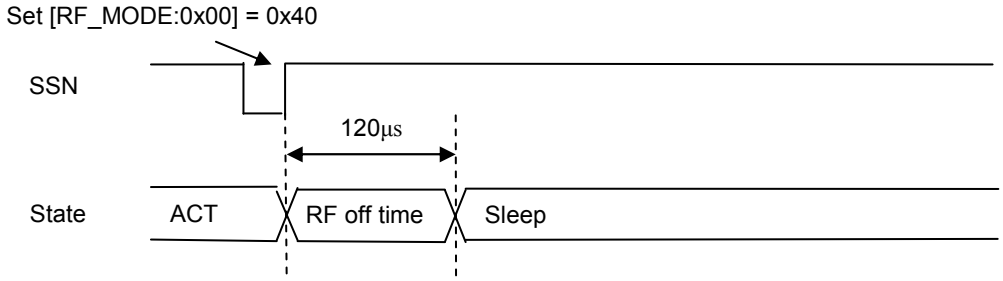
[Idle to ACT]

The following shows the operation timing from Idle state to ACT state.



[ACT to Sleep]

The following shows the operation timing from ACT state to Sleep state.



●VCO calibration

VCO calibration is for correcting the VCO oscillation frequency.
ML7386/ML7386B supports two type of VCO calibration.

- Idle calibration: The caliration done at Idle state.
- Active calibration: The calibration done at ACT state.

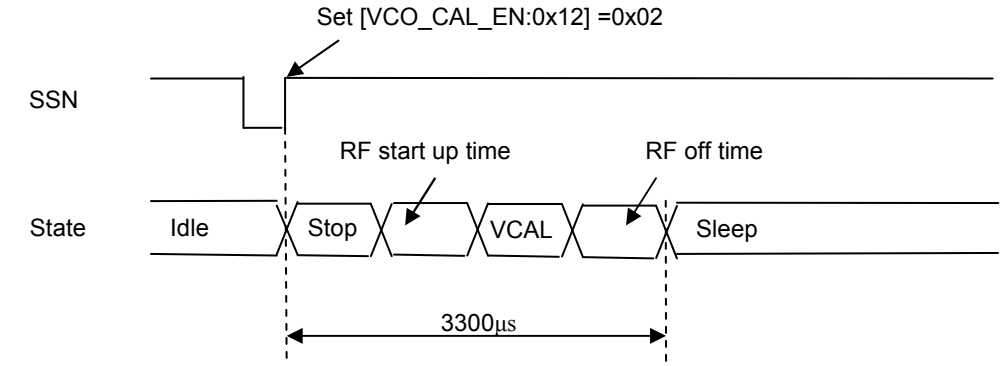
Required wait time at each calibration mode is shown as below table.

No.	CAL mode	State to be executed	State to be moved up on completion	Set value to [VCO_CAL_EN:0x12]	Required Wait Time [ms] (*1)
1	Idle	Idle	Idle	0x02	3.3
2	Active	ACT	ACT	0x01	1.5

*1: During the waiting time, any register access is prohibited.

NOTE: When using TCXO, TCXO should be stabilized before executing command..

The following shows the operation timing of Idle calibration.



■Registers

●Register setting flow

The following shows the register setting flow which uses test pattern transmission as a reference.
For details of setting value to each register, please refer to the "ML7386Family_Register_tool_20130910.xls".

No	Register Address	Setting value	Remark
1	0x01	0x00	Baud rate setting (2400bps)
2	0x02	0x08	Select test pattern ("PN9"=0x08, "CW"=0C, "1010"=0x09)
3	0x03	0x10	Channel frequency setting (426.250MHz)
4	0x04	0xC4	
5	0x05	0x4E	
6	0x06	0x06	
7	0x08	0x1A	Frequency deviation setting (2.1kHz)
8	0x09	0x31	
9	0x0A	0x44	
10	0x0B	0x50	
11	0x0C	0x54	
12	0x0D	0xFF	Frequency deviation transition time setting (2400bps)
13	0x0E	0x00	Select clock source ("Xtal"=0x00, "TCXO"=0x01)
14	0x10	0x02	Transmission power adjustment
15	0x16	0x55	
16	0x17 *1	0x00	Select PA ("1mW"=00, "10mW"=0x01)
17	0x2A *1	0x00	PA bias setting ("1mW"=02, "10mW"=0x07)
18	0x12	0x02	Execute VCO Idle calibration
3.3ms wait			
19	0x00	0x18	Set ACT state
Data transmitted after 2.715ms			
20	0x00	0x00	Stop transmission and move to Idle state.

*1: Tese registers are supported at ML7386B.

●Register map

The space shown as gray highlighted part are not implemented in LSI or reserved bits. The space shown as lined mesh part are required to fill fixed value. The address not exisit in the memory map is not accesible.

plemented as functionable register (Read and Write)
pelemted as reserved bits
pelemted as required to fill fixed value

Address	Symbol	Function	Bit assignment								Default
			7	6	5	4	3	2	1	0	
0x00	RF_MODE	RF state setting									0x00
0x01	BR	Baud Rate setting									0x00
0x02	TXD_SEL	Data configuration									0x00
0x03	PLL_N	PLL N parameter setting									0x10
0x04	PLL_FL	PLL Frequency setting (low byte)									0xC4
0x05	PLL_FM	PLL Frequency setting (middlebyte)									0x4E
0x06	PLL_FH	PLL Frequency setting (high4 bits)									0x06
0x07	PLL_FIT	PLL frequency adjustment									0x00
0x08	F_DEV0	Frequency deviation #0 setting									0x1A
0x09	F_DEV1	Frequency deviation #1 setting									0x32
0x0A	F_DEV2	Frequency deviation #2 setting									0x44
0x0B	F_DEV3	Frequency deviation #3 setting									0x52
0x0C	F_DEV4	Frequency deviation #4 setting									0x54
0x0D	T_PLL_TR	Frequency deviation transition time setting									0x86
0x0E	CLK_SEL	clock configuration									0x00
0x0F	SRST	Software reset setting	w	w	w	w	w	w	w	w	0x00
0x10	PA_ADJ	PA gain adjustment									0x77
0x11	VCO_CAL	VCO calibration value R/W control									0x20
0x12	VCO_CAL_EN	VCO calibration execution									0x00
0x13	PLL_CPI	PLL charge pump current control									0x0F
0x14	BR_FLEX_SET_L	Extended baud rate setting (low byte)									0x28
0x15	BT_FLEX_SET_H	Extended baud rate setting (high byte)									0x15
0x16	PA_BIAS	PA bias control									0x16
0x17	PA_SEL	PA selection									0x01
0x1A	F_DEV_RESO	Frequency deviation resolution setting									0x00
0x2A	PA_REG	PA requlator output setting									0x07

[Note] All register access is available when RSTN="H".
The method to access each register described in "SPI Data format" section.

■RF Adjustment

●Tx Power Adjustment

The ML7386B has two Popwer Amplifiers(PA) for 10mW mode and 1mW mode. Appropriate PA should be selected in the design. This section shows the power sdjusting methodology for each power mode.

In each power mode, optimum matching circuit should be reqired. In the 10mW mode design, if select 1mW mode PA, RF performances are not guranteed. Sama as in 1mW mode design.

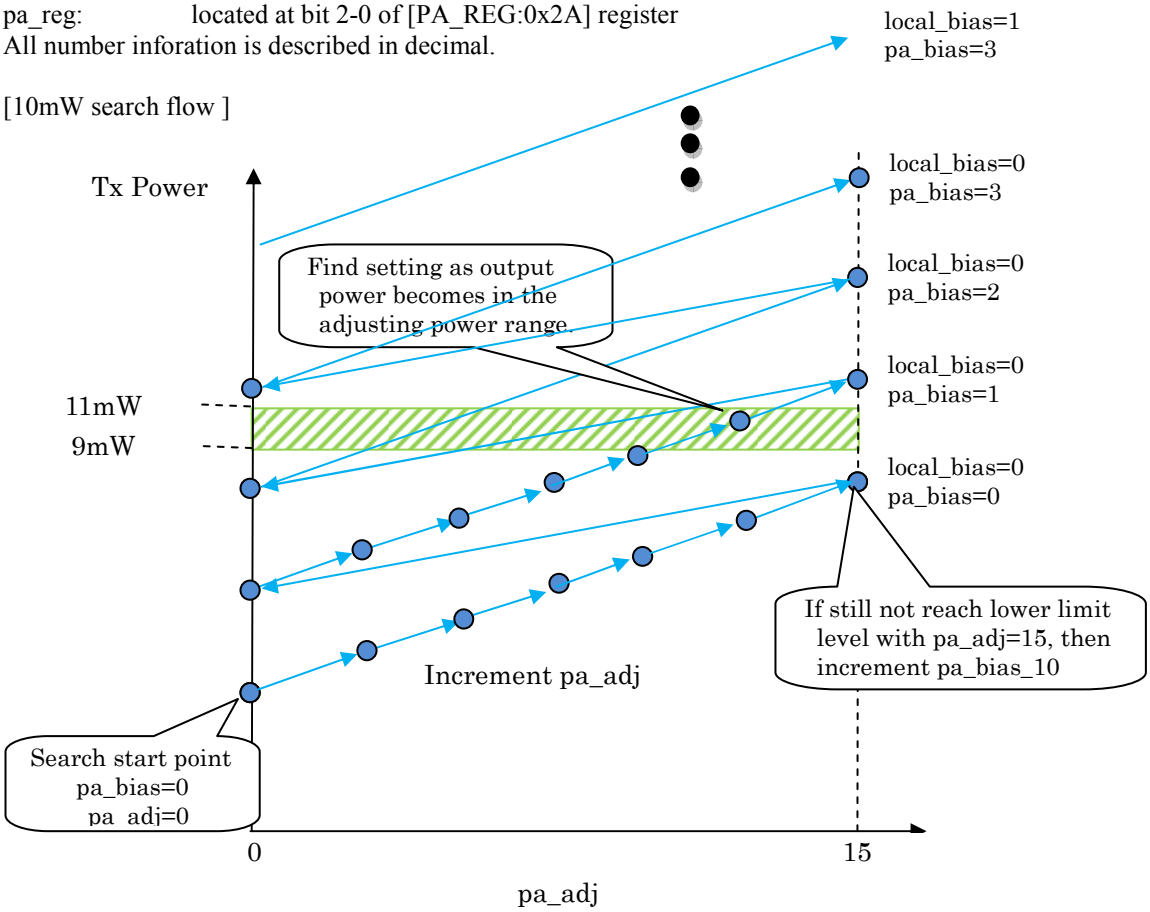
●10mW Tx Power Adjustment

It is possible to adjust the Tx power by [PA_ADJ:0x10] and [PA_BIAS:0x16] registers. The following flow shows the example to adjusting Tx power to 10mW.

Adjusting power range should be set to more than +/- 5% to the desired level.
(In the following flow, the upper limit set to 11mW and the lower limit set to 9mW, ie +/- 10%.)

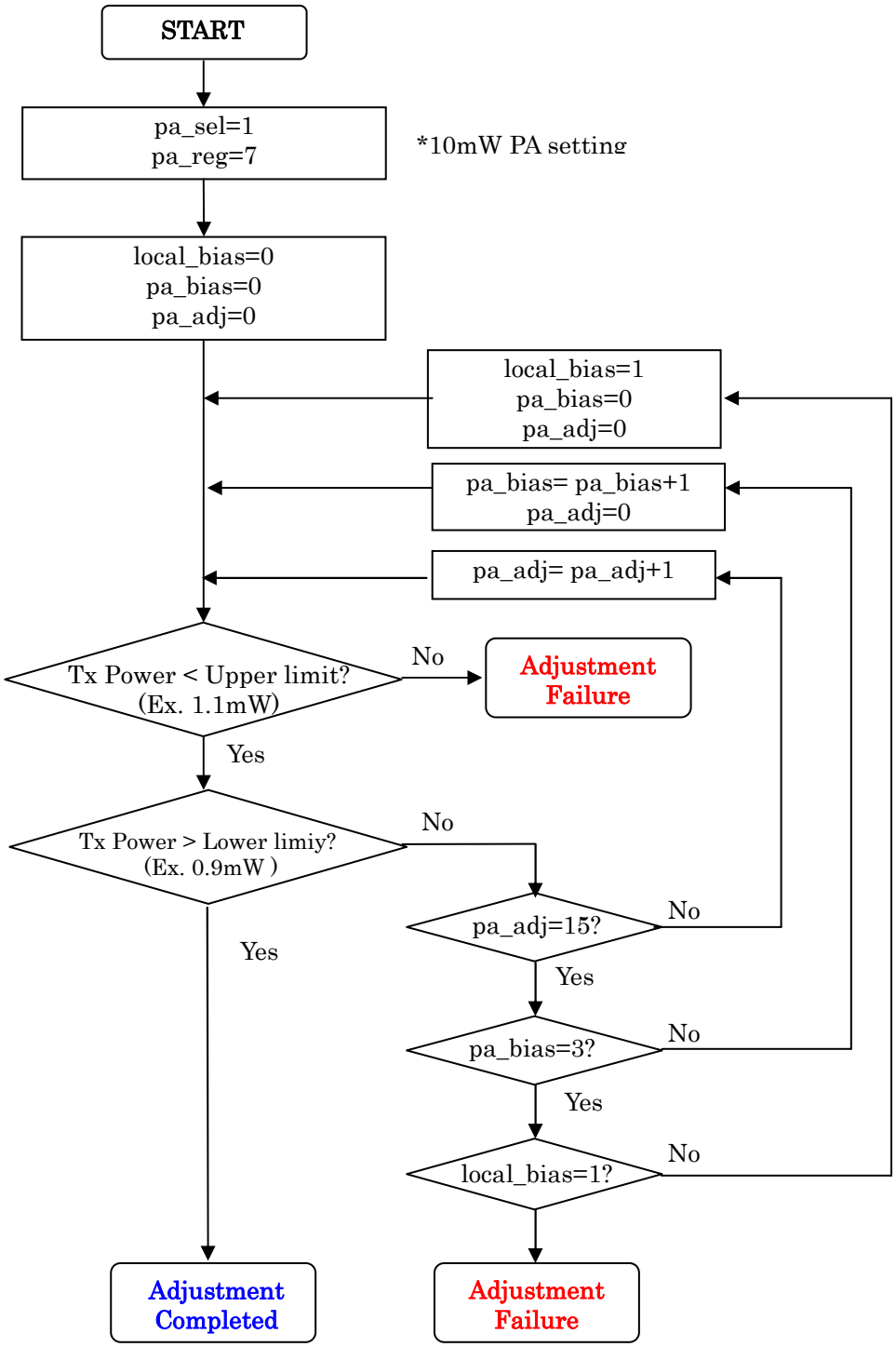
pa_sel: located at bit 0 of [PA_SEL:0x2A] reister
pa_adj : located at bit 7-4 of [PA_ADJ:0x10] register
local_bias: located at the bit 6 of [PA_BIAS:0x16] register
pa_bias: located at bit 5-4 of [PA_BIAS:0x16] register
pa_reg: located at bit 2-0 of [PA_REG:0x2A] register
All number inforation is described in decimal.

[10mW search flow]



[Note] If set local_bias=1, higher power is achivable than local_bias=0. Overrup power zone will exist.

[10mW power adjustment flow]
All number inforation is described in decimal.



●1mW Tx Power Adjustment

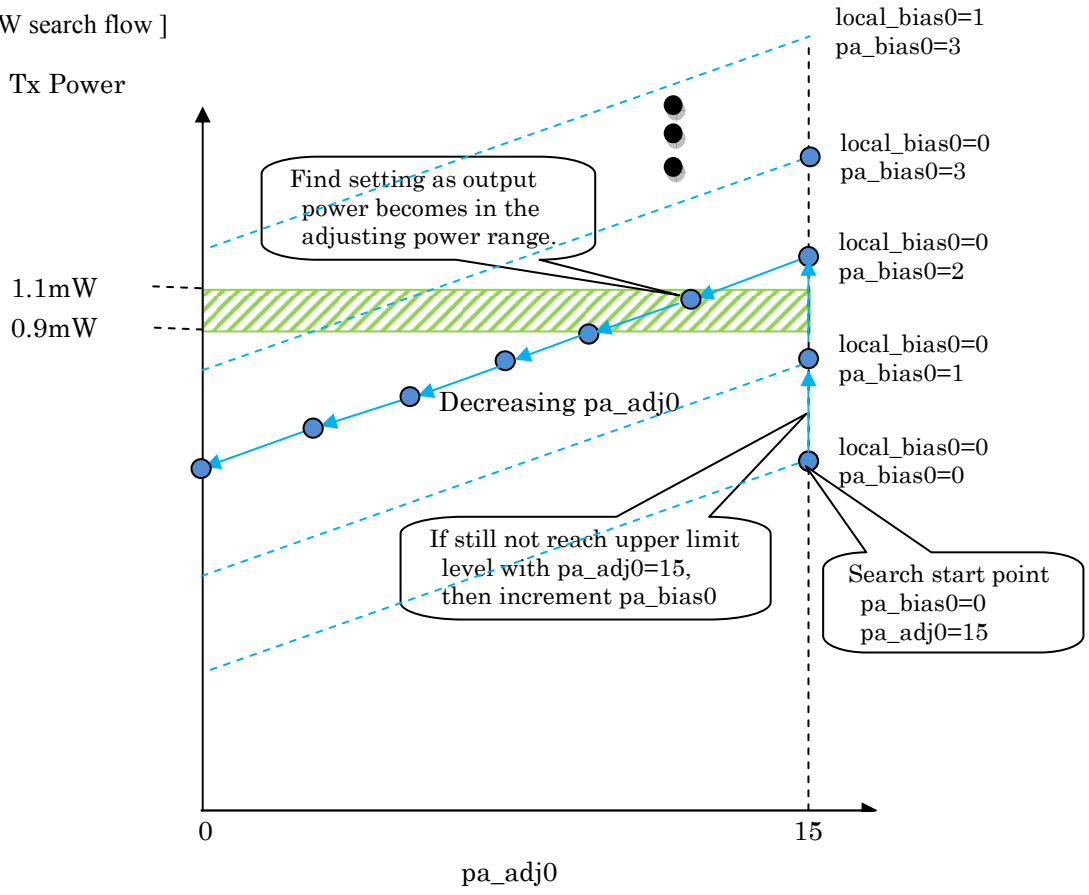
It is possible to adjust the Tx power by [PA_ADJ:0x10] and [PA_BIAS:0x16] registers. The following flow shows the example to adjusting Tx power to 10mW.

Adjusting power range should be set to more than +/- 5% to the desired level.
(In the following flow, the upper limit set to 1.1mW and the lower limit set to 0.9mW, ie +/- 10%.)

pa_sel:	located at bit 0 of [PA_SEL:0x2A] reister
pa_adj0 :	located at bit 3-0 of [PA_ADJ:0x10] register
local_bias0:	located at the bit 2 of [PA_BIAS:0x16] register
pa_bias0:	located at bit 1-0 of [PA_BIAS:0x16] register
pa_reg:	located at bit 2-0 of [PA_REG:0x2A] register

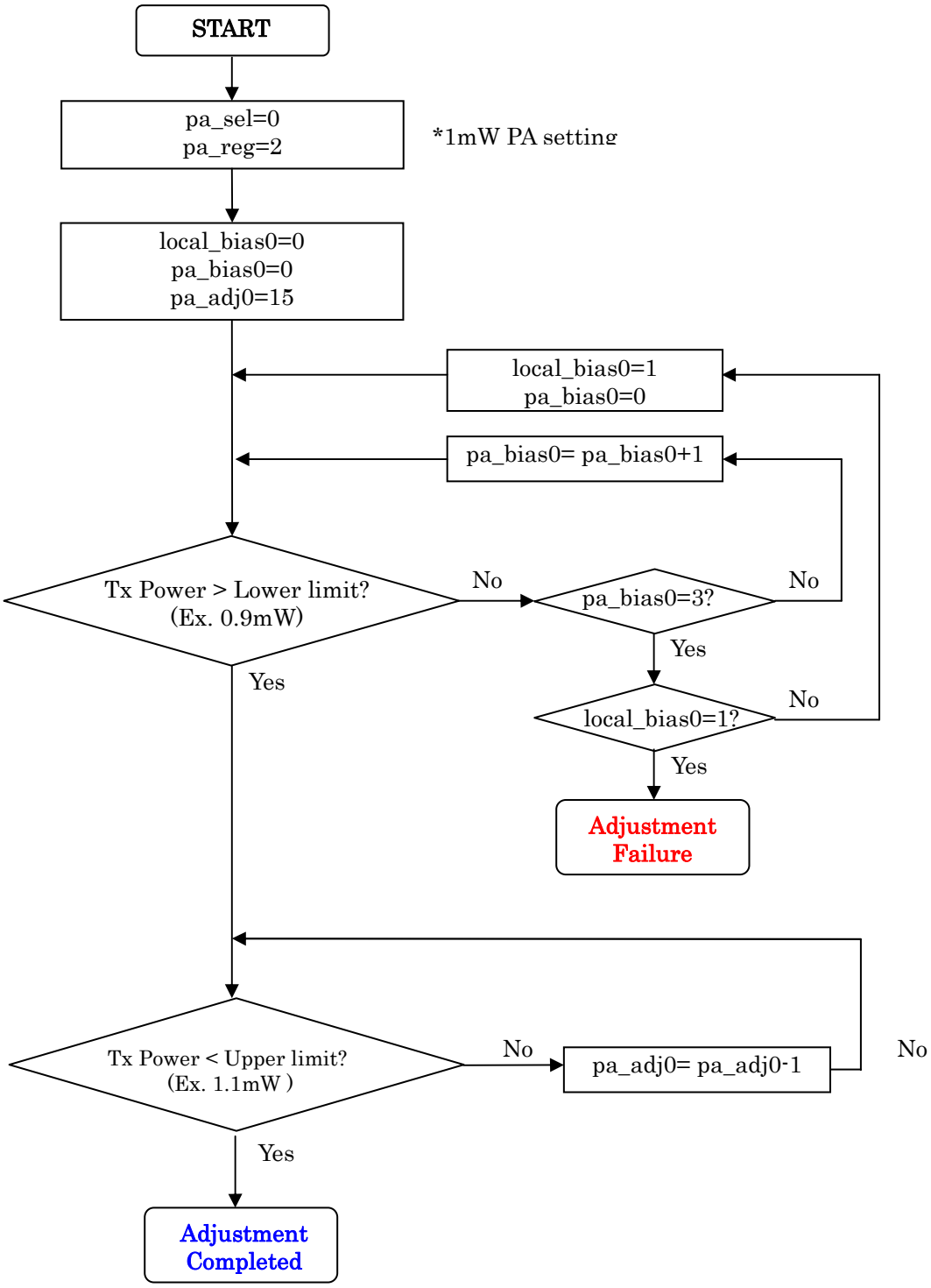
All number inforation is described in decimal.

[1mW search flow]



[Note] If set local_bias0=1, higher power is achivable than local_bias0=0. Overrup power zone will exist.

[1mW power adjustment flow]
All number inforation is described in decimal.



●Programming Channel Frequency

It is possible to configure channel frequency by registers of [PLL_N:0x03], [PLL_FL:0x04], [PLL_FM:0x05] and [PLL_FH:0x06] registers.
The relation between setting frequency and each parameter are shown in the following formula.

$$f = f_{REF} * (N+F/2^{20})$$

f	: PLL oscillation frequency
freal	: Desired frequency
ferr	: freqency error (freal – f)
f_{REF}	: PLL reference frequency (master clock: 26MHz)
N	: N parameter (Integer part)
F	: F parameter (Fractional part

Each frequency register will have following values.

$N = int[f / f_{REF}]$
$F = int[(f / f_{REF} - N) * 2^{20}]$ ••• Internal block uses 20 bits width

Therefore frequency error will be ferr = f real - $\{f_{REF} \times \{(N+F/2^{20})\}$

Ex) If f=426.2500MHz, each parameter will be as follows when f_{REF} = 26MHz
$N = int[426.2500M / 26M] = 16$
$F = int[\{426.2500M /26M - 16 * 2^{20}] = 413380$ (0x64EC4)

Here
[PLL_N:0x03] = 0x10
[PLL_FL:0x04] = 0xC4
[PLL_FM:0x05] = 0x4E
[PLL_NA:0x06] = 0x06

In this case freuqency error will be ferr=426. 2500M - $\{26M * (16+ 413380 /2^{20})\}$ = + 22.9Hz
Setting resolution depends on master clock. If 26MHz, the resolution is 25Hz.

Following shows the setting table for 426MHz channels of Japan band as reference.

[RCR STD-30]

CH No.	Frequency [MHz]	PLL_NA (0x03)	PLL_FL (0x04)	PLL_FM (0x05)	PLL_FH (0x06)	Ferr (Hz)
1	426.2500	10	C4	4E	06	22.9
2	426.2625	10	BD	50	06	1.1
3	426.2750	10	B5	52	06	4.2
4	426.2875	10	AD	54	06	7.2
5	426.3000	10	A5	56	06	10.3
6	426.3125	10	9D	58	06	13.4
7	426.3250	10	95	5A	06	16.4
8	426.3375	10	8D	5C	06	19.5
9	426.3500	10	85	5E	06	22.5
10	426.3625	10	7E	60	06	0.8
11	426.3750	10	76	62	06	3.8
12	426.3875	10	6E	64	06	6.9
13	426.4000	10	66	66	06	9.9
14	426.4125	10	5E	68	06	13.0
15	426.4250	10	56	6A	06	16.0
16	426.4375	10	4E	6C	06	19.1
17	426.4500	10	46	6E	06	22.1
18	426.4625	10	3F	70	06	0.4
19	426.4750	10	37	72	06	3.4
20	426.4875	10	2F	74	06	6.5
21	426.5000	10	27	76	06	9.5
22	426.5125	10	1F	78	06	12.6
23	426.5250	10	17	7A	06	15.6
24	426.5375	10	0F	7C	06	18.7
25	426.5500	10	07	7E	06	21.7
26	426.5625	10	00	80	06	0.0
27	426.5750	10	F8	81	06	3.1
28	426.5875	10	F0	83	06	6.1
29	426.6000	10	E8	85	06	9.2
30	426.6125	10	E0	87	06	12.2
31	426.6250	10	D8	89	06	15.3
32	426.6375	10	D0	8B	06	18.3
33	426.6500	10	C8	8D	06	21.4
34	426.6625	10	C0	8F	06	24.4
35	426.6750	10	B9	91	06	2.7
36	426.6875	10	B1	93	06	5.7

[RCR STD-30] (continue)

CH No.	Frequency [MHz]	PLL_NA (0x03)	PLL_FL (0x04)	PLL_FM (0x05)	PLL_FH (0x06)	Ferr (Hz)
37	426.7000	10	A9	95	06	8.8
38	426.7125	10	A1	97	06	11.8
39	426.7250	10	99	99	06	14.9
40	426.7375	10	91	9B	06	17.9
41	426.7500	10	89	9D	06	21.0
42	426.7625	10	81	9F	06	24.0
43	426.7750	10	7A	A1	06	2.3
44	426.7875	10	72	A3	06	5.3
45	426.8000	10	6A	A5	06	8.4
46	426.8125	10	62	A7	06	11.4
47	426.8250	10	5A	A9	06	14.5
48	426.8375	10	52	AB	06	17.5

[ARIB STD-T67]

CH No.	Frequency [MHz]	PLL_NA (0x03)	PLL_FL (0x04)	PLL_FM (0x05)	PLL_FH (0x06)	Ferr (Hz)
1	426.0250	10	52	2B	06	17.55
2	426.0375	10	4A	2D	06	20.60
3	426.0500	10	42	2F	06	23.65
4	426.0625	10	3B	31	06	1.91
5	426.0750	10	33	33	06	4.96
6	426.0875	10	2B	35	06	8.01
7	426.1000	10	23	37	06	11.06
8	426.1125	10	1B	39	06	14.11
9	426.1250	10	13	3B	06	17.17
10	426.1375	10	0B	3D	06	22.22

The following table shows the relation between master clock and frequency setting range

Master clock [MHz]	PLL frequency setting raneg		Frequency Resolution [Hz]
	Minimum [MHz]	Maximum [MHz]	
18	200	486	17
19	211	513	18
20	222	540	19
21	233	567	20
22	244	594	21
23	255	621	22
24	266	648	23
25	278	675	24
26	289	702	25
27	300	729	26
28	311	756	27
29	322	783	28
30	333	810	29
31	344	837	30
32	355	864	31
33	366	891	31
34	377	918	32
35	389	945	33
36	400	972	34

.

●Programming FSK modulation

ML7386/ML7386B outputs filtered FSK modulation, the shaping figure is defined by fiollowing registers [F_DEV0:0x08] to [F_DEV4:0x0C] and [T_PLL_TR: 0x0D] registers.

Keeping better performance of OBWand suprious emission , each fdev parameter should be set as below table depnds on the wanted frequency deviation. Tansision time parameter should be set depends on the data rate.

If using except for 26MHz master clock, the setting parameters can be calcurated by the "ML7386Family_ Register_tool_20130910.xls". And evaluation and confirmation should be required under user specific condition.

[Frequency deviation setting list]

[Master Clock = 26MHz]

Fdev (KHz)	F_DEV0 (0x08)	F_DEV1 (0x09)	F_DEV2 (0x0A)	F_DEV3 (0x0B)	F_DEV4 (0x0C)
0.6	07	0E	13	16	18
0.7	08	10	16	1A	1C
0.8	0A	13	1A	1E	20
0.9	0B	15	1D	22	24
1.0	0C	17	20	26	28
1.1	0D	1A	23	2A	2C
1.2	0F	1C	27	2D	30
1.3	10	1E	2A	31	34
1.4	11	21	2D	35	38
1.5	12	23	31	39	3C
1.6	14	26	34	3D	40
1.7	15	28	37	41	44
1.8	16	2A	3A	44	48
1.9	17	2D	3E	48	4C
2.0	19	2F	41	4C	50
2.1 (default)	**1A**	**31**	**44**	**50**	**54**
2.2	1B	34	47	54	58
2.3	1C	36	4B	58	5C
2.4	1E	39	4E	5B	60
2.5	1F	3B	51	5F	64
2.6	20	3D	54	63	68
2.7	21	40	58	67	6C
2.8	23	42	5B	6B	70
2.9	24	45	5E	6F	74
3.0	25	47	62	72	78

[Master Clock = 26MHz] (continue)

Fdev (KHz)	F_DEV0 (0x08)	F_DEV1 (0x09)	F_DEV2 (0x0A)	F_DEV3 (0x0B)	F_DEV4 (0x0C)
3.1	26	49	65	76	7D
3.2	28	4C	68	7A	81
3.3	29	4E	6B	7E	85
3.4	2A	50	6F	82	89
3.5	2B	53	72	86	8D
3.6	2D	55	75	89	91
3.7	2E	58	78	8D	95
3.8	2F	5A	7C	91	99
3.9	30	5C	7F	95	9D
4.0	32	5F	82	99	A1
4.1	33	61	85	9D	A5
4.2	34	63	89	A0	A9

[Frequency deviation transition time setting list]

[Master Clock = 26MHz]

Data rate [bps]	[T_PLL_TR: 0x0D] Tim_plltr[7:0]
2400	0xFF
4800	0x87
7200	0x5A

●Fractional Spurious

Fractional N spurious appears depends on the carrier frequency by following equations.

1. fractional[Carrier frequency / master clock] * master clock
2. (1- fractional[Carrier frequency /master clock]) * master clock

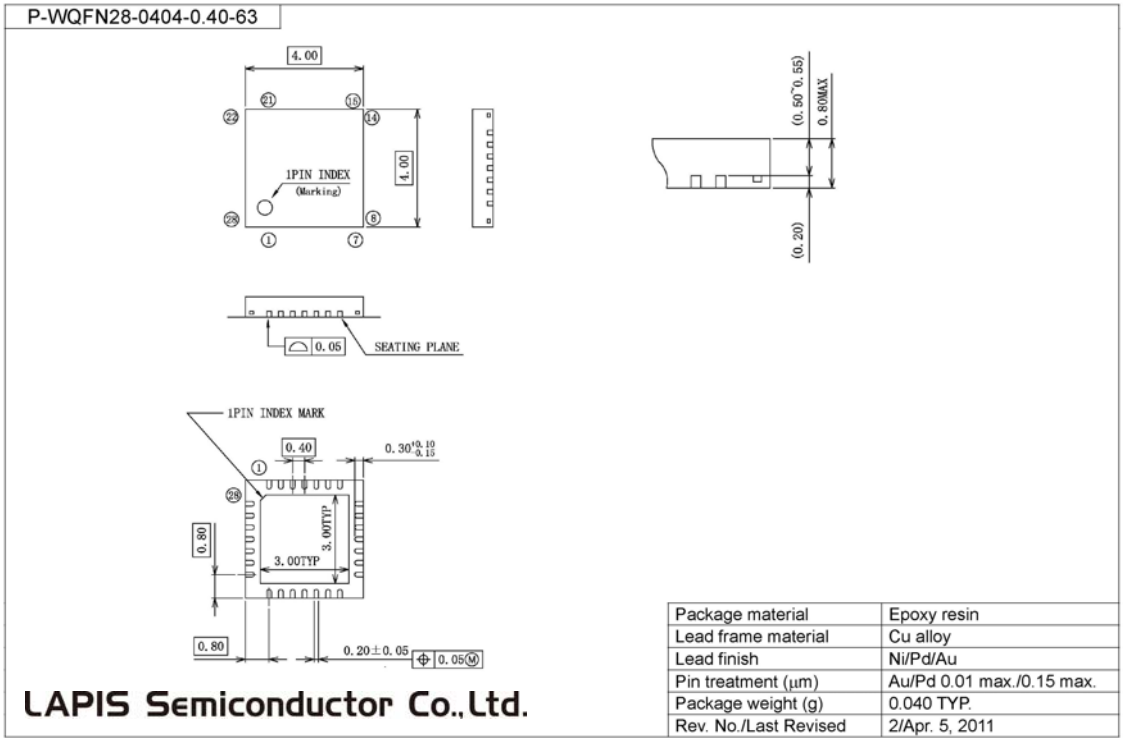
If a fractional spurious appears within +/- 200 kHz to the channel frequency, the fractional spurious emission could not be decreased. It is strongly recommended that the channel frequency should not be used.

So it means the range +/- 200 kHz to (26MHz * n) is not usable. (n=1,2,3.)
ML7386/ML7386B supports the operation frequency range from 200MHz to 972MHz. For this range following frequency is unable operation frequency by the fractional spurious.

[Master Clock = 26MHz]

n	Spurious frequency [MHz]	Spurious lower limit [MHz]	Spurious upper limit [MHz]
n-8	208	207.8	208.2
n=9	234	233.8	234.2
n=10	260	259.8	260.2
n=11	286	285.8	286.2
n=12	312	311.8	312.2
n=13	338	337.8	338.2
n=14	364	363.8	364.2
n=15	390	389.8	390.2
n=16	416	415.8	416.2
n=17	442	441.8	442.2
n=18	468	467.8	468.2
n=19	494	493.8	494.2
n=20	520	519.8	520.2
n=21	546	545.8	546.2
n=22	572	571.8	572.2
n=23	598	597.8	598.2
n=24	624	623.8	624.2
n-25	650	649.8	650.2
n=26	676	675.8	676.2
n=27	702	701.8	702.2
n=28	728	727.8	728.2
n-29	754	753.8	754.2
n=30	780	779.8	780.2
n=31	806	805.8	806.2
n=32	832	831.8	832.2
n=33	858	857.8	858.2
n=34	882	881.8	882.2
n=35	908	907.8	908.2
n=36	934	933.8	934.2
n=37	960	959.8	960.2

■Package diagram



Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 max./0.15 max.
Package weight (g)	0.040 TYP.
Rev. No./Last Revised	2/Apr. 5, 2011

Remarks for surface mount type package

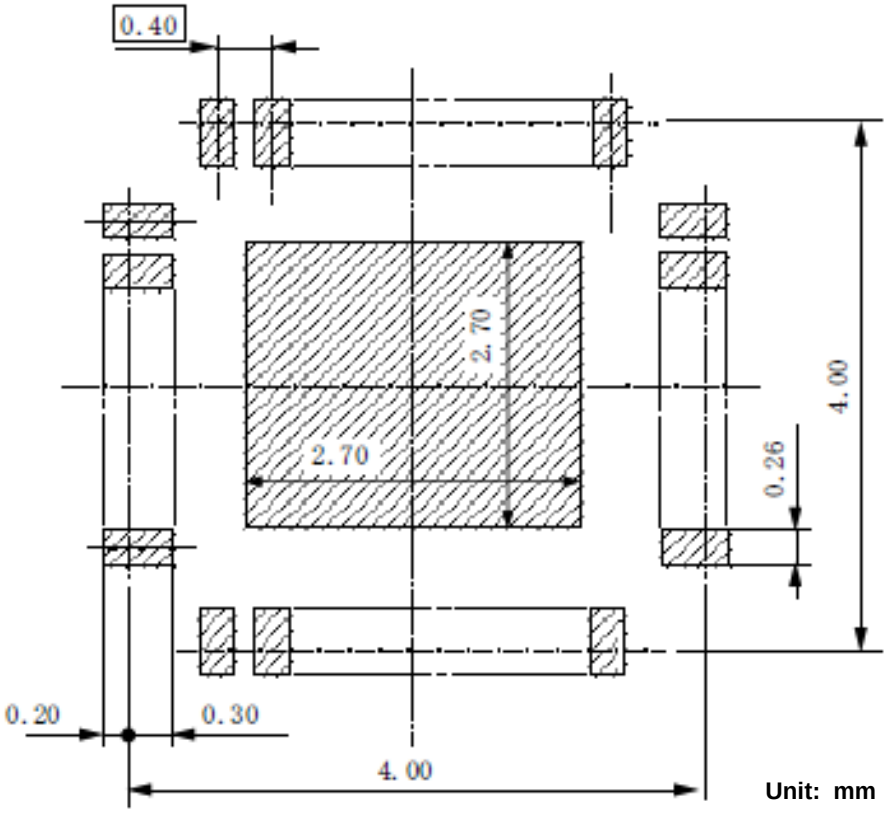
Surface mount type package is very sensitive affected by heating from reflow process, humidity during storaging Therefore, in case of reflow mouting process, please contact sales representative about product name, package name, number of pin, package code and required reflow process condition (reflow method, temperature, number of reflow process), storage condition.

■Reference Footprint Pattern (Recommendation)

P-WQFN28-0404-0.40-63

For reference

Mounting area for package lead soldering to PC boards



Unit: mm

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts, reliability, wiring, and elimination of slder bridges.

The optimum design for the foot pattern varies with the materials of the substrate, the sort and thichness of used soldering paste, and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering PC boards.

LAPIS Semiconductor Co.,Ltd.

■Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7386-01	Dec. 27, 2011	–	–	Initial release (ML7386)
FEDL7386B-01	Dec. 3, 2012	–	–	Initial release (ML7386B including ML7386)
FEDL7386B-02	Jan. 7, 2013	–	15	Added Timing characteristics
FEDL7386B-03	Feb. 18, 2013	–	1	Modified TX Frequency range
FEDL7386B-04	Jun. 11, 2013	–	34	Added PLL_CPI register setting
FEDL7386B-05	Sep. 27, 2013	–	24	Added register setting flow
FEDL7386B-06	Mar. 13, 2014	13	13	Modified TX Frequency range
FEDL7386B-07	Apr. 16, 2014	27	27	Modified a polarity of txdinv

NOTES

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