FEDL7416N-060-01
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ML7416N-060

Sub-GHz (900 MHz Band) Broadband RF Transceiver IC with Built-in MCU

1. General Description

ML7416 is a low power consumption LSI for sub-GHz broadband radio communication, which integrates the MCU block and RF block in a single chip.

The features are shown below. *** For details of the RF block, refer to ML7396B Data Sheet (FJDL7396A_B_E).**

- Industry-standard ARM Cortex-M0+ CPU core * Maximum operating frequency: 40 MHz
- 512 KB flash memory (for program [256 KB x 2 bank configuration is possible]. Can be used as data flash)
- 64 KB RAM (for data. Whether to hold data in low power consumption mode can be selected)
- Start-stop synchronous serial communication interface (UART) * Max. 3 ch
- Synchronous serial communication interface (SPI) * Max. 2 ch (additionally, 1 ch for SPI dedicated to RF control, which does not exist on the external port)
- WDT
- General-purpose IO
- Timer * 32-bit timer x 10 ch. Among them, 4 ch (2 sets) can be used as 64-bit timer by the cascade connection
- RTC
- Flexible timer (FTM) (PWM mode, etc.)
- I2C * Master/slave supported
- RF control transmit/receive data interface (DIO) * As this is dedicated to RF control, it does not have an external port
- Random number generation circuit (RAND)
- Clock correction counter (CLK_Timer)
- SWD (2-wire serial wire debug port)
- X'tal OSC * 32.768 KHz
- PLL * Multiplying/dividing 32 KHz
- ADC * 10 bits, Max. 3 ch (Max. 2 ch when using the temperature sensor function)
- Voltage drop detection (LVD)
- Temperature sensor (TEMP)
- RC OSC * 40 MHz, 32 KHz
- AES * ECB, CBC, CTR, CCM, and GCM supported
- DMA controller * Transfer between SPI and RAM and between AES and RAM, 4 ch
- Flash DMA controller * Write to flash, Verify

ROHM SEMICONDUCTOR

- Supply voltage 1.8 to 3.6 V (when the transmission power is set to 1 mW mode)
  2.3 to 3.6 V (when the transmission power is set to 10 mW mode)
  2.6 to 3.6 V (when the transmission power is set to 20 mW mode)
- Operating temperature -40 to 85 °C

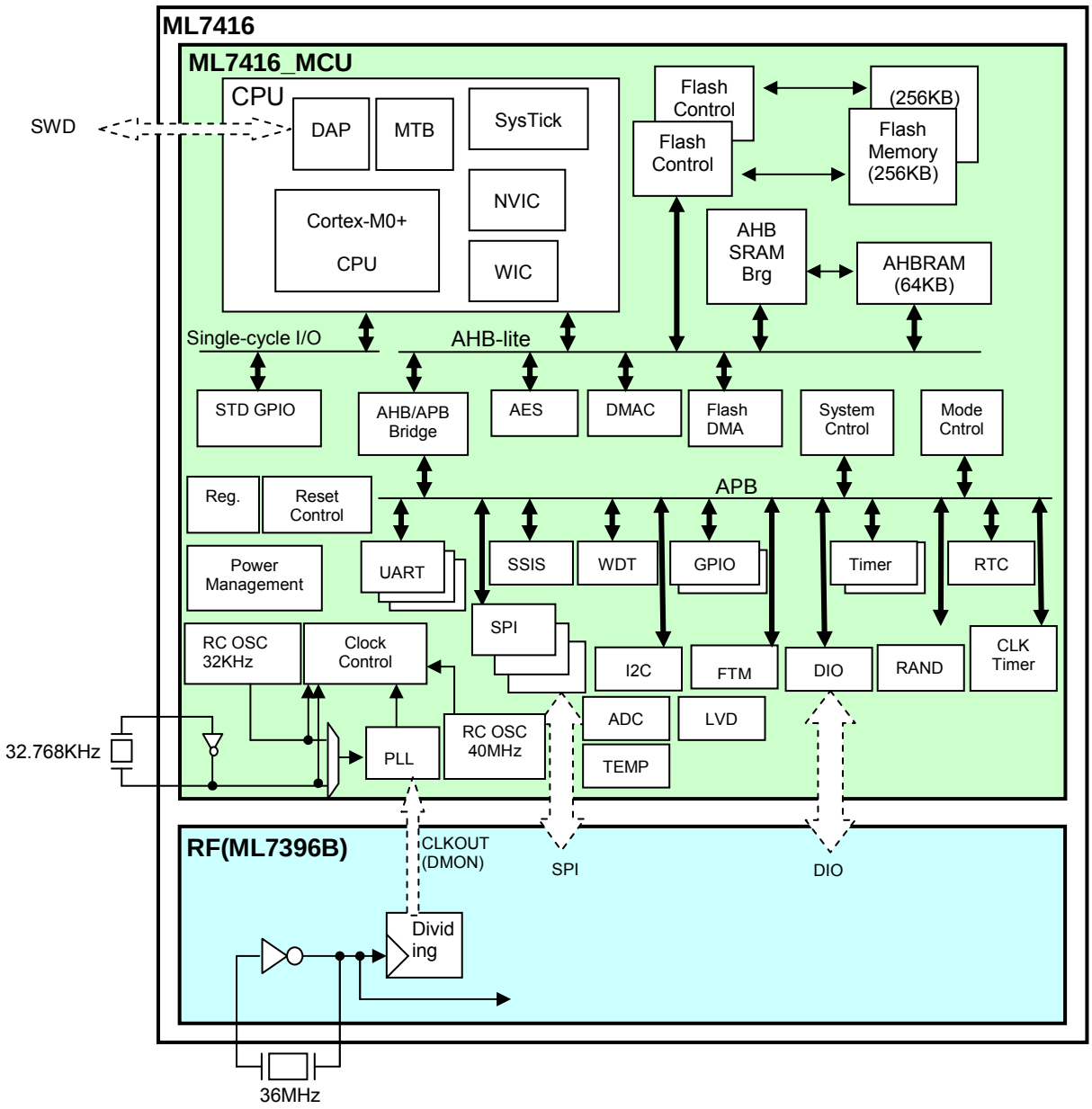
- Current consumption

At deepsleep		2 µA(Typ.)
At idle		11 mA(Typ.)
At reception		24 mA (Typ.)
At transmission	1 mW	22 mA (Typ.)
	10 mW	33 mA(Typ.)
	20 mW	41 mA(Typ.)

- Package

  81-pin BGA (MCP product/P-LFBGA81-1010-1.00-1-MC)
  10 mm x 10 mm (pin pitch: 1 mm)
  Lead-free package conforming to RoHS

2. Block Diagram



3. Pin Layout

*** The pin layout shown below is tentative. Please contact us before board design.**

○81 BGA (10 mm x 10 mm, pin pitch: 1 mm)

1	2	3	4	5	6	7	8	9	
VDDIO_RF	GPIOA0	GPIOA1	GPIOA2	GPIOA4	GPIOA5	GPIOA6	GPIOA7	GND_CPU	A
DCNT	VDD_PA	GPIOA3	MODE0	MODE1	GPIOA12	GPIOA8	GND_CPU	GPIOA9	B
TRX_SW	ANT_SW	VDD_REG	REG_CORE_CPU	TEST_CPU	RESETN	GND_CPU	ADC0	GPIOA10	C
REG_PA	TEST	A_MON	GND_RF	GND_RF	REGPDIN	GND_CPU	ADC1	GPIOA11	D
GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	VDDIO_CPURF	ADC2	CXOUT	E
GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	VPP	VDD_REG_CPU	CXIN	F
PA_OUT	GND_RF	VDD_CP	GND_RF	GND_RF	GND_RF	TCXO	VDDIO_CPU	SWCK	G
LNA_P	GND_RF	VDD_RF	VDD_IF	VDD_VCO	REG_OUT	REG_CORE	VDDIO_CPU	SWD	H
GND_RF	LP1	IND1	IND2	VB_EXT	VBG	XIN	XOUT	VDDIO_CPU	J

TOP View

4. Pin Description

*** The pin names and LSI numbers may be changed in the future.**

Input/output definition

I_{RF}	:RF input pin
O_{RF}	:RF output pin
I_A	:Analog input pin
O_A	:Analog output pin
I_{OS}	:36 MHz resonator circuit input pin
O_{OS}	:36 MHz resonator circuit output pin
I_{OSL}	:32.768 KHz resonator circuit input pin
O_{OSL}	:32.768 KHz resonator circuit output pin
I	:Digital input pin
O	:Digital output pin
Is	:Schmitt trigger input pin
O_D	:Open drain pin

4-1. Power Supply

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
VDDIO_CPU	G8 H8 J9	Power supply	-	- / -	Power supply pin for the digital I/O (Typ. 3.3 V)
VDDIO_RF	A1	Power supply	-	- / -	Power supply pin for RF (Typ. 3.3 V)
VDD_REG	C3	Power supply	-	- / -	Regulator voltage supply pin (RF side/Typ. 3.3 V)
VDD_REG_CPU	F8	Power supply	-	- / -	Regulator voltage supply pin (CPU side/Typ. 3.3 V)
VDD_PA	B2	Power supply	-	- / -	Power supply pin for PA (Typ. 3.3 V)
VDDIO_CPURF	E7	Power supply	-	- / -	Power supply pin for supply from CPU to RF (Typ. 3.3 V)
VDD_RF	H3	Power supply	-	- / -	Power supply pin for LNA/MIX (Typ. 1.5 V)
VDD_IF	H4	Power supply	-	- / -	Power supply pin for IF (Typ. 1.5 V)
VDD_VCO	H5	Power supply	-	- / -	Power supply pin for VCO (Typ. 1.5 V)
VDD_CP	G3	Power supply	-	- / -	Power supply pin for CP (Typ. 1.5 V)
GND_RF	D4 to D5 E1 to E6 F1 to F6 G2,G4 to G6 H2 J1	Ground	-	- / -	Ground pin (for RF)
GND_CPU	A9 B8 C7 D7	Ground	-	- / -	Ground pin (for CPU)

4-2. Regulator Interface

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
REG_OUT	H6	-	-	- / -	Regulator output (Typ. 1.5 V) C connection (10 uF) * Outputs 0 V at sleep state.
REG_PA	D1	-	-	- / -	PA regulator output pin * Outputs 0 V at sleep state.
VBG	J6	-	-	- / -	C connection pin (RF side/0.1 uF)
REGPDIN	D6	I	H	I / -	Regulator power down pin * Fixed to "L" input in normal operation
REG_CORE	H7	-	-	- / -	Monitor pin for power supply for digital core (RF side /Typ. 1.5V)/C connection(10 uF))
REG_CORE_CPU	C4	-	-	- / -	Monitor pin for power supply for digital core (CPU side/Typ. 1.5 V/C connection (0.22 uF))

4-3. RF Interface

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
LNA_P	H1	I_{RF}	-	I	RF antenna input pin
PA_OUT	G1	O_{RF}	-	O	RF antenna output pin
IND1	J3	-	-	- / -	External inductor connection pin
IND2	J4	-	-	- / -	External inductor connection pin
LP1	J2	-	-	- / -	Loop filter connection pin
VB_EXT	J5	-	-	- / -	Internal bias averaging capacitor connection pin
A_MON	D3	O_{RF}	-	Hi-Z	Test pin for analog monitor, IF block, and analog circuit

4-4. ADC Interface

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
ADC0	C8	I_A	-	I / -	ADC input pin 0
ADC1	D8	I_A	-	I / -	ADC input pin 1
ADC2	E8	I_A	-	I / -	ADC input pin 2 * Input from this pin is disabled when using the temperature sensor

4-5. CPU Interface

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
GPIOA0	A2	I / O	-	oZ / -	Primary function: General-purpose pin
		I	-		Secondary function: UART data input pin (RXD)
		I / O	P or N		Tertiary function: SPI clock pin (SCK)
		Is / O_D	P or N		Quartic function: I2C clock pin (SCL)
		I / O	-		Quintic function: Single cycle IO pin
GPIOA1	A3	I / O	-	oZ / -	Primary function: General-purpose pin
		O	-		Secondary function: UART data output pin (TXD)
		I / O	L		Tertiary function: SPI enable pin (SSN)
		Is / O_D	-		Quartic function: I2C data I/O pin (SDA)
		I / O	-		Quintic function: Single cycle IO pin
GPIOA2	A4	I / O	-	oZ / -	Primary function: General-purpose pin
		I	L		Secondary function: UART CTS (Clear To Send) pin
		O	-		Tertiary function: SPI data I/O pin 1 (MISO)
		I / O	-		Quartic function: FTM I/O pin
		I / O	-		Quintic function: Single cycle IO pin
GPIOA3	B3	I / O	-	oZ / -	Primary function: General-purpose pin
		O	L		Secondary function: UART RTS (Ready To Send) pin
		I / O	-		Tertiary function: SPI data I/O pin 2 (MOSI)
		I / O	-		Quartic function: Reserved
		I / O	-		Quintic function: Single cycle IO pin

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
GPIOA4	A5	I / O	-	oZ / -	Primary function: General-purpose pin
		I	-		Secondary function: UART data input pin (RXD)
		I / O	P or N		Tertiary function: SSI slave clock pin (SSICK)
		Is / O_D	P or N		Quartic function: I2C clock pin (SCL)
		I / O	-		Quintic function: Single cycle IO pin
GPIOA5	A6	I / O	-	oZ / -	Primary function: General-purpose pin
		I	L		Secondary function: UART data output pin (TXD)
		I	L		Tertiary function: SSI slave enable pin (SSIN)
		Is / O_D	-		Quartic function: I2C data I/O pin (SDA)
		I / O	-		Quintic function: Single cycle IO pin
GPIOA6	A7	I / O	-	oZ / -	Primary function: General-purpose pin
		I	L		Secondary function: UART CTS (Clear To Send) pin
		O	-		Tertiary function: SSI Slave data output pin (TXD)
		Is / O_D	-		Quartic function: I2C clock pin (SCL)
		I / O	-		Quintic function: Single cycle IO pin
GPIOA7	A8	I / O	-	oZ / -	Primary function: General-purpose pin
		O	L		Secondary function: UART RTS (Ready To Send) pin
		I	-		Tertiary function: SSI Slave data input pin (RXD)
		I / O	-		Quartic function: Reserved
		I / O	-		Quintic function: Single cycle IO pin
GPIOA8	B7	I / O	-	oZ / -	Primary function: General-purpose pin
		I	-		Secondary function: UART data input pin (RXD)
		I / O	P or N		Tertiary function: SPI clock pin (SCK)
		Is / O_D	P or N		Quartic function: I2C clock pin (SCL)
		I / O	-		Quintic function: Single cycle IO pin
GPIOA9	B9	I / O	-	oZ / -	Primary function: General-purpose pin
		O	-		Secondary function: UART data output pin (TXD)
		I / O	L		Tertiary function: SPI enable pin (SSN)
		Is / O_D	-		Quartic function: I2C data I/O pin (SDA)
		I / O	-		Quintic function: Single cycle IO pin

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
GPIOA10	C9	I / O	-	oZ / -	Primary function: General-purpose pin
		I	L		Secondary function: UART CTS (Clear To Send) pin
		O	-		Tertiary function: SPI data I/O pin 1 (MISO)
		I / O	-		Quartic function: FTM I/O pin
		I / O	-		Quintic function: Single cycle IO pin
GPIOA11	D9	I / O	-	oZ / -	Primary function: General-purpose pin
		O	L		Secondary function: UART RTS (Ready To Send) pin
		I / O	-		Tertiary function: SPI data I/O pin 2 (MOSI)
		I / O	-		Quartic function: Reserved
		I / O	-		Quintic function: Single cycle IO pin
GPIOA12	B6	I / O	-	oZ / -	1Bank Mode: General-purpose pin 2Bank Mode: System mode input pin (for software) 0: User application mode 1: ISP mode

4-6. Debugger Interface

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
SWCK	G9	I	-P or N	I / -	SWD clock input pin
SWD	H9	I / O	H or L	I / -	SWD data I/O pin

4-7. Others

Pin name	LSI number	I/O	Active level	Attribute/value at reset	Functional description
RESETN	C6	Is	L	I / -	Hardware reset pin
XIN	J7	Ios	P or N	I	36 MHz crystal oscillator connection pin 1 * Connect this pin to GND when using an external clock.
XOUT	J8	Oos	P or N	O	36 MHz crystal oscillator connection pin 2 * Connect this pin to GND when using an external clock.
TCXO	G7	I_A	-	I	External clock (TCXO) input pin * Connect this pin to GND when using an oscillator.
CXIN	F9	I_{OSL}	P or N	I	32.768 KHz crystal oscillator connection pin 1
CXOUT	E9	O_{OSL}	P or N	O	32.768 KHz crystal oscillator connection pin 2
TRX_SW	C1	O	H or L or OD	O / L	Transmit/receive switch pin
ANT_SW	C2	O	H or L or OD	O / L	Diversity switch pin
TEST	D2	I	H	I / -	Test mode pin * Fixed to "L" input in normal operation
TEST_CPU	C5	I	H	I / -	Test mode pin * Fixed to "L" input in normal operation
MODE0	B4	I	H or L	I / -	Remapping pin 0: The program executes from the address 0 in the internal Flash ROM 1: The program executes from the boot area in the internal Flash ROM
MODE1	B5	I	H or L	I / -	Test mode pin * Fixed to "L" input in normal operation
DCNT	B1	O	H or L or OD	O / L	External PA control pin
VPP	F7	-	H	- / -	High voltage application pin for flash core test * Normally, leave this pin open.

4-8. Handling of Unused Pins

See below for handling of unused pins.

Pin name	Recommended treatment
XOUT	GND (when TCXO is used)
XIN	GND (when TCXO is used)
TCXO	GND (when an oscillator is used)
A_MON	Open
ANT_SW	Open
DCNT	Open
VPP	Open

5. Electrical Characteristics

TBD

*** The electrical characteristics may be changed as a result of evaluation or any other reason.**

5-1.Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage (I/O) (*1)	VDDIO		-0.3 to +4.6	V
Power supply voltage (RF) (*2)	VDDRF		-0.3 to +2.0	V
Digital input voltage	VDIN		-0.3 to VDDIO+0.3	V
RF input voltage	VRFIN		-1.0 to +2.0	V
Analog input voltage	VAIN		-0.3 to VDDIO+0.3	V
Analog input voltage 2 (*3)	VAIN2		-0.3 to VDDRF+0.3	V
TCXO input voltage	VTCXO		-0.3 to +1.75	V
Digital output voltage	VDO	Ta=-40 to 85°C	-0.3 to VDDIO+0.3	V
RF output voltage	VRFO	GND=0V	-0.3 to VDDRF+1.9	V
Analog output voltage	VAO		-0.3 to VDDIO+0.3	V
Analog output voltage 2 (*4)	VAO2		-0.3 to VDDRF+0.3	V
Digital input current	IDI		-10 to +10	mA
RF input current	IRF		-2 to +2	mA
Analog input current	IAI		-2 to +2	mA
Analog input current 2 (*3)	IAI2		-2 to +2	mA
TCXO input current	ITCXO		-2 to +2	mA
Digital output current	IDO		-8 to +8	mA
RF output current	IRFO		-2 to +60	mA
Analog output current	IAO		-2 to +2	mA
Analog output current 2 (*4)	IAO2		-2 to +2	mA
Power dissipation	PD	Ta=+25°C	300	mW
Storage temperature	Tstg	-	-55 to +150	°C

(*1) VDDIO_CPU, VDDIO_RF, VDD_REG, VDD_REG_CPU, VDD_PA, and VDDIO_CPURF pins

(*2) VDD_RF, VDD_IF, VDD_VCO, and VDD_CP pins

(*3) XIN, TCXO, and CXIN pins

(*4) XOUT and CXOUT pins

5-2. Recommended Operating Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage (I/O)	VDDIO	VDD_IO* pin and VDD_REG* pin	1.8	3.3	3.6	V
Power supply voltage (PA)	VDD_PA	VDD_PA pin Transmission power +1 mW mode	1.8	3.3	3.6	V
		VDD_PA pin 10 mW mode	2.3	3.3	3.6	V
		VDD_PA pin 20 mW mode	2.6	3.3	3.6	V
Power supply voltage (RF) (*2)	VDDRF	VDD_RF pin, VDD_IF pin, VDD_VCO pin and VDD_CP pin	1.4	1.5	1.6	V
Operational temperature	Ta	-	-40	+25	+85	°C
Digital input rise time	tIR1	Digital input pins (*1)	-	-	20	ns
Digital input fall time	tIF1	Digital input pins (*1)	-	-	20	ns
Digital output load	CDL	All digital output pins	-	-	20	pF
Master clock 1 36 MHz crystal oscillator frequency	FMCK1	XIN pin, XOUT pin	-20 ppm (*3)	36	+20 ppm (*3)	MHz
Master clock 2 36 MHz TCXO frequency	FMCK2	TCXO pin	-20 ppm (*3)	36	+20 ppm (*3)	MHz
TCXO	VTCXO	DC cut	0.8	-	1.5	Vpp
Slow clock 32.768 kHz crystal oscillator frequency	FSCK1	CXIN pin, CXOUT pin	TBD	32.768	TBD	kHz
RC clock 1 40 MHz RC clock frequency	FRCK1		TBD	40	TBD	MHz
RC clock 2 32 kHz RC clock frequency	FRCK2		TBD	32	TBD	kHz
SPI clock input frequency	FSCLK	SCLK pin			CPUCLK/ 4	MHz
SPI clock input duty ratio	DSCLK	SCLK pin	45	50	55	%
RF channel frequency	FRF	LNA_P and PA_OUT pins	896	-	960	MHz

(*1) Pins described as I or Is in the Input/output column in "Pin Description".

(*2) Use the REG_OUT output of this LSI.

(*3) If set to 10 kbps, the maximum is +10 ppm, and the minimum is -10 ppm.

[Notices]

The electrical characteristics are measured under the recommended operating conditions above, unless otherwise specially noted.

The timings are measured at the 20% and 80% levels of VDDIO, unless otherwise specially noted.

5-3. Common Characteristics

Item	Symbol	Conditions	Min.	Typ. (*2)	Max.	Unit
Supply current (*1)	IDD1	Sleep state (*3)	-	2	TBD	μA
	IDD2	Idle state	-	11	TBD	mA
	IDD3	RF receiving state (*4)	-	24	TBD	mA
	IDD4	RF transmitting state (1 mW) (*4)	-	22	TBD	mA
	IDD5	RF transmitting state (10 mW) (*4)	-	33	TBD	mA
	IDD6	RF transmitting state (20 mW) (*4)	-	41	TBD	mA
High level input voltage	VIH1	Digital input pin	VDDIOx0.75	-	VDDIO	V
	VIH2	XIN pin	VDDRFx0.9	-	VDDRF	V
Low level input voltage	VIL1	Digital input pin	0	-	VDDIOx0.18	V
	VIL2	XIN pin	0	-	VDDRFx0.1	V
Schmitt trigger high level decision threshold value	VT+	Digital pins with schmitt trigger	-	1.2	VDDIOx0.75	V
Schmitt trigger low level decision threshold value	VT-	Digital pins with schmitt trigger	VDDIOx0.18	0.8	-	V
Input leakage current	IIH1	Digital input pin	-1	-	1	μA
	IIH2	XIN pin	-0.3	-	0.3	μA
	IIL1	Digital input pin	-1	-	1	μA
	IIL2	XIN pin	-0.3	-	0.3	μA
Tri-state Output leakage current	IOZH1	Digital I/O pin	-1	-	1	μA
	IOZL1	Digital I/O pin	-1	-	1	μA
High level output voltage	VOH	IOH=-4mA /-2mA (*5)	VDDIOx0.8	-	VDDIO	V
Low level output voltage	VOL	IOL=4mA /2mA (*5)	0	-	0.3	V
Pin capacitance	CIN	Input pin	-	6	-	pF
	COUT	Output pin	-	9	-	pF
	CRFIO	RF I/O pin	-	9	-	pF
	CAI	Analog input pin	-	20	-	pF

(*1) The power supply current is the total current of all power supply pins.

(*2) The "Typ." value is the center value under the condition of VDDIO = 3.3 V and 25 °C.

(*3) The "Typ." and "Max." values are under the condition of 25 °C.

(*4) Values when the data transfer speed is 100 kpbs and the frequency is 920 MHz.

(*5) For DMON pin, IOH is -2 mA/2 mA.

(*6) REG_CORE pin and REG_OUT pin. REG_OUT outputs 0 V at sleep state.

5-4. RF Characteristics

Modulated data rate	:	10 kbps/ 20 kbps/ 40 kbps/ 50 kbps / 100 kbps / 150 kbps/ 200 kbps/ 400 kbps
Modulation method	:	Binary GFSK
Channel spacing	:	200 kHz / 400 kHz / 600 kHz
Frequency range	:	A frequency from 750 MHz to 1 GHz can be set by changing external circuit constants.

The measurement point is at antenna end specified in the recommended circuits.

Characteristics not described here and ones of 400 kbps (optional) will be provided separately as reference data.

5.4.1 [Transmission Characteristics]

Item	Conditions	Min.	Typ.	Max.	Unit
Transmitter power output	When set to 20 mW (13 dBm) mode	9	13	15	dBm
	When set to 10 mW (10 dBm) mode	6	10	12	dBm
	When set to 1 mW (0 dBm) mode	-4	0	2	dBm
Adjustment range of frequency shift [Fdev] (*1)		-	-	2,250	kHz
920 MHz band (920.5 MHz to 928.1 MHz)					
Occupied bandwidth	n: Number of unit channels (n = 1, 2, 3, 4 or 5)	-	-	200 *n	kHz
Power at the edges of radio channel	20 mW mode (920.5 MHz to 922.3 MHz)	-	-	-7	dBm
	10 mW mode	-	-	-10	dBm
	1 mW mode	-	-	-20	dBm
Adjacent channel leakage [ACP]	20 mW mode ± 1 ch, bandwidth 200 kHz	-	-33	-15	dBm
	10 mW mode ± 1 ch, bandwidth 200 kHz	-	-39	-18	dBm
	1 mW mode ± 1 ch, bandwidth 200 kHz	-	-47	-26	dBm
Unnecessary emission level (20 mW mode)	710 MHz or lower, 100 kHz band	-	-65	-36	dBm
	Higher than 710 MHz to 900 MHz, 1 MHz band	-	-70	-55	dBm
	Higher than 900 MHz to 915 MHz, 100 kHz band	-	-72	-55	dBm
	Higher than 915 MHz to 930 MHz, 100 kHz band (Excluding within 200 + 100xnkHz above and below the channel frequency, however, within 100 + 100xnkHz above and below for 920.5 MHz to 922.3 MHz. n is the number of concurrently used channels)	-	-51	-36	dBm
	Higher than 930 MHz to 1000 MHz, 100 kHz band	-	-70	-55	dBm
	Higher than 1000 MHz to 1215 MHz, 1 MHz band	-	-75	-45	dBm
	Higher than 1215 MHz, 1 MHz band (Equal to or higher than the 2nd harmonics)	-	-40	-30	dBm

915 MHz band (902 MHz to 928 MHz)					
6dB bandwidth	Frequency shift = 171 kHz	500	-	-	kHz
Power spectrum density	20 mW mode, frequency shift = 171 kHz, 3 kHz band	-	-	8	dBm
Unnecessary emission level (20 mW mode)	900 MHz or below	-	-65	-56	dBm
	Higher than 960 MHz (2nd harmonics or higher)	-	-50	-41	dBm
868 MHz band (863 MHz to 870 MHz) (*2)					
Unnecessary emission level (10 mW mode)	Higher than 1000 MHz (2nd harmonics or higher)	-	-35	-30	dBm

*1 While the adjustment range is described as above, the possible maximum value depends on the RF channel frequency to be used.

RF channel frequency ± frequency shift should not include a multiple of 36 MHz (864 MHz, 900 MHz, 936 MHz, and so on).

Example) For 902 MHz, 2,000 kHz can be set at a maximum.

*2 863.5 MHz to 866.2 MHz cannot be used. For details, refer to "Setting channel frequency" in ML7396B Data Sheet.

5.4.2 [Reception Characteristics]

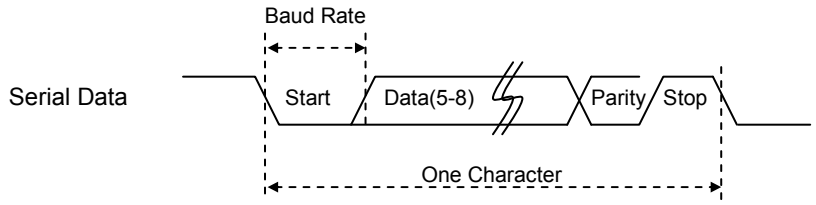
Item	Conditions	Min.	Typ.	Max.	Unit
920 MHz band (920.5 MHz to 928.1 MHz)					
Minimum receiver sensitivity BER < 0.1%	50 kbps mode (*1)	-	-108	-102	dBm
	100 kbps mode (*1)	-	-106	-100	dBm
	200 kbps mode (*1)	-	-102	-97	dBm
Maximum receiver input level	50 kbps mode, 100 kbps mode, 200 kbps mode	0	-	-	dBm
Receiver C/I adjacent interference	50 kbps mode	20	35	-	dB
	100 kbps mode	20	35	-	dB
	200 kbps mode	20	35	-	dB
Receiver C/I second adjacent interference	50 kbps mode	30	45	-	dB
	100 kbps mode	30	45	-	dB
	200 kbps mode	30	45	-	dB
Minimum energy detection level (ED value)		-	-	-100	dBm
Energy detection range	Dynamic range	60	70	-	dB
Energy detection accuracy		-6	-	+6	dB
Collateral emission level ARIB T108 measurement condition 915.9MHz to 916.9MHz 920.5MHz to 929.7MHz	710 MHz or lower, 100 kHz band	-	<-93	-54	dBm
	Higher than 710 MHz to 900 MHz, 1 MHz band	-	<-83	-55	dBm
	Higher than 900 MHz to 915 MHz, 100 kHz band	-	<-93	-55	dBm
	Higher than 915 MHz to 930 MHz, 100 kHz band	-	-63	-54	dBm
	Higher than 930 MHz to 1000 MHz, 100 kHz band	-	<-93	-55	dBm
	Higher than 1000 MHz, 1 MHz band	-	-57	-47	dBm
915 MHz band (902 MHz to 928 MHz)					
Minimum receiver sensitivity BER < 0.1%	100 kbps mode (modulation index = 1) (*1)	-	-106	-99	dBm
	150 kbps mode (modulation index = 0.5) (*1)	-	-102	-96	dBm
	200 kbps mode (modulation index = 1) (*1)	-	-102	-96	dBm
	100 kbps mode (frequency shift: 171 kHz)	-	-100	-87	dBm
	150 kbps mode (frequency shift: 171 kHz)	-	-97.5	-84	dBm
	200 kbps mode (frequency shift: 171 kHz)	-	-96.5	-83	dBm
868 MHz band (863 MHz to 870 MHz) (*2)					
Minimum receiver sensitivity BER < 0.1%	50 kbps mode (*1)	-	-108	-102	dBm
	100 kbps mode (*1)	-	-106	-100	dBm
	200 kbps mode (*1)	-	-102	-97	dBm
Collateral emission level	1000 MHz or below (local frequency)	-	-63	-57	dBm
	Frequency over 1000 MHz	-	-57	-47	dBm

*1 When normal bandwidth mode (NBO_SEL = 0) is set. See the [DATA_SET] register (B0 0x47).

*2 863.5 MHz to 866.2 MHz cannot be used. For details, refer to "Setting channel frequency" in ML7396B Data Sheet.

5-5. UART Interface Characteristics

Item	Symbol	Conditions	Min	Typ	Max	Unit
Baud Rate	F_{BAUD}	Load capacitance CL=20pF	-	115200	-	ns

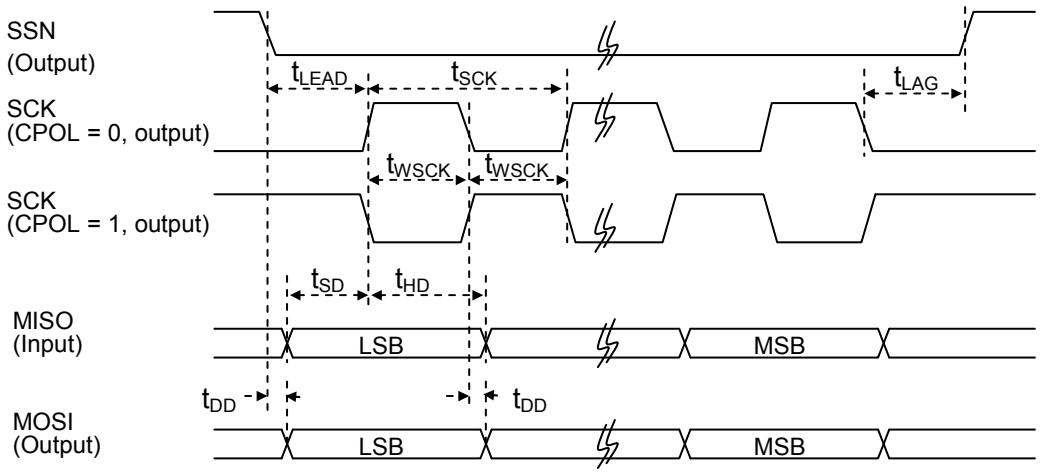


5-6. SPI Interface Characteristics

5-6-1.Master

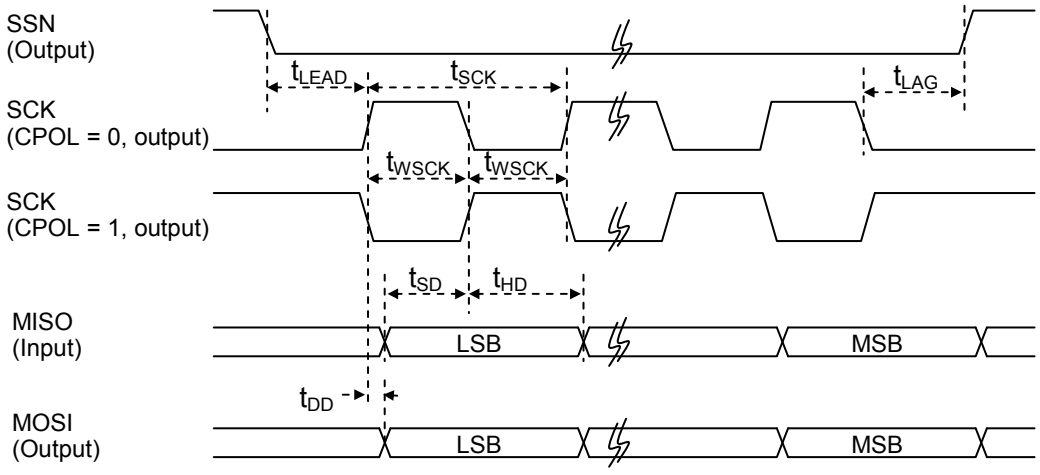
Item	Symbol	Conditions	Min	Typ	Max	Unit
Serial clock cycle time	t_{SCK}	-	100	-	-	ns
Serial clock High/Low time	t_{WSCK}	-	48	-	-	ns
Data delay time (output)	t_{DD}	-	-	-	50	ns
Data setup time (input)	t_{SD}	CL=20pF	-	-	48	ns
Data hold time (input)	t_{HD}	-	0	-	-	ns
SSN-SCK lead time	t_{LEAD}	-	0.5* t_{SCK}	-	1.6* t_{SCK}	ns
SCK-SSN lag time	t_{LAG}	-	0.5* t_{SCK}	-	1.5* t_{SCK}	ns
SSN H minimum guaranteed time	t_{WSSH}	-	1* t_{SCK}	-	511* t_{SCK}	ns
SPI bus input/output rise/fall time	t_R, t_F	-	-	-	25	ns

○ SPI master mode timing (CPHA = 0)



CPHA=0

○ SPI master mode timing (CPHA = 1)



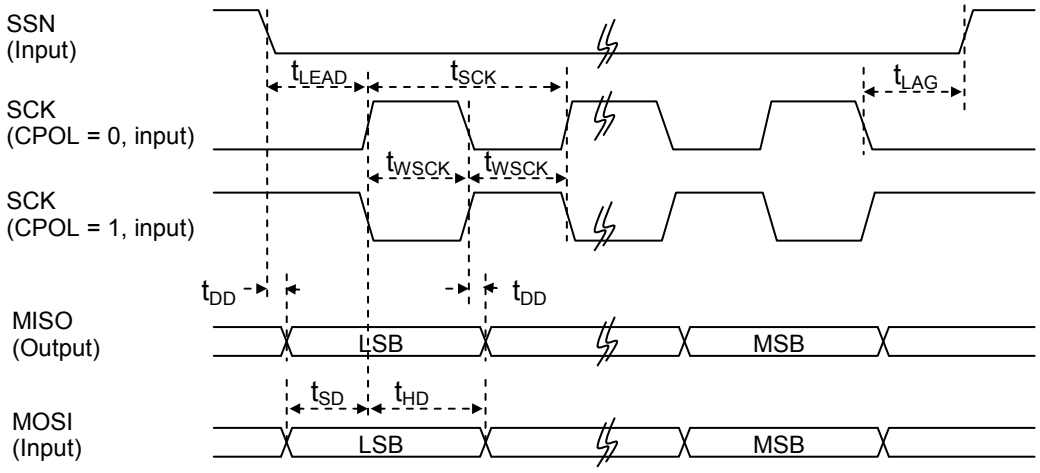
CPHA=1

*Note: For CPHA and CPOL, refer to the register descriptions in "7-8. SPI".

5-6-2.Slave

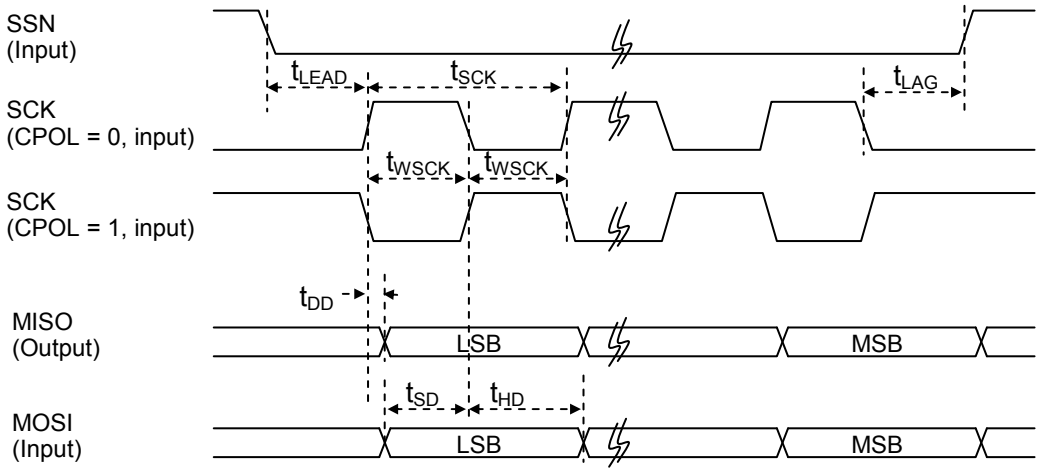
Item	Symbol	Conditions	Min	Typ	Max	Unit
Serial clock cycle time	t_{SCK}	-	100	-	-	ns
Serial clock High/Low time	t_{WSCK}	-	50	-	-	ns
Data delay time (output)	t_{DD}	-	-	-	50	ns
Data setup time (input)	t_{SD}	CL=20pF	-	-	50	ns
Data hold time (input)	t_{HD}	-	10	-	-	ns
SSN-SCK lead time	t_{LEAD}	-	0.5* t_{SCK}	-	-	ns
SCK-SSN lag time	t_{LAG}	-	0.5* t_{SCK}	-	-	ns

○ SPI slave mode timing (CPHA = 0)



CPHA=0

○ SPI slave mode timing (CPHA = 1)



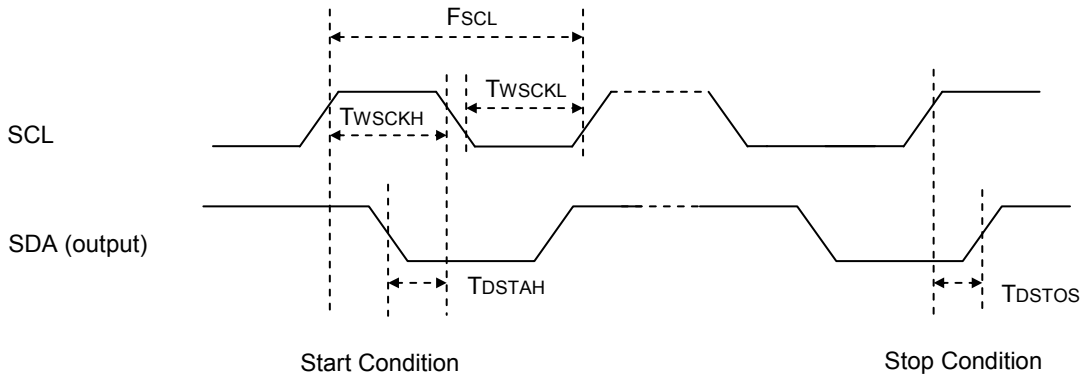
CPHA=1

*Note: For CPHA and CPOL, refer to the register descriptions in "7-8. SPI".

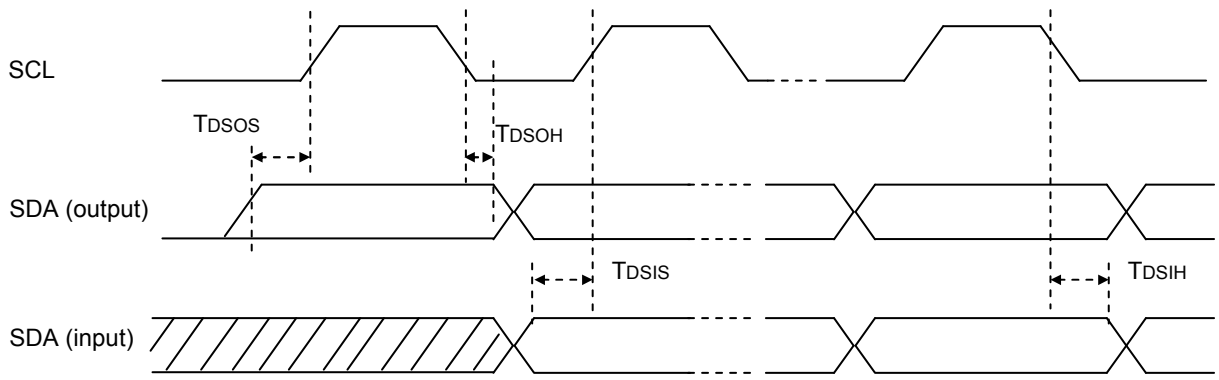
5-7. I2C Interface Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	Fscl	Conditions of load capacitance CL= 20pF	-	-	400	kHz
SCL H pulse width	TWSCKH		600	-	-	ns
SCL L pulse width	TWSCKL		1300	-	-	ns
Start condition hold time	TDSTAH		450	-	-	ns
Stop condition setup time	TDSTOS		575	-	-	ns
SDA output hold time	TDSOH		0	-	-	ns
SCL output delay time	TDSOS		600	-	-	ns
SDA input setup time	TDSIS		100	-	-	ns
SDA input hold time	TDSIH		0	-	-	ns

○ Stop condition (SDA fall at SCL = 1), Start condition (SDA rise at SCL = 1)



○ Transmission/reception



5-8. A/D Conversion Characteristics

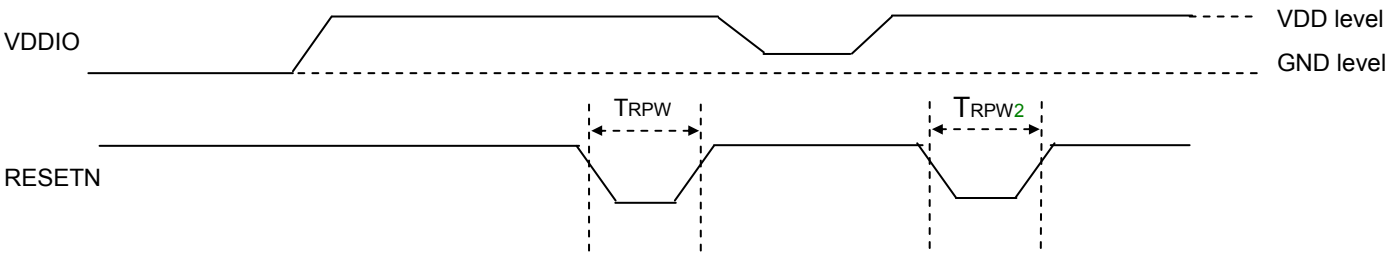
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Number of bits	N_{SAR}	Number of SAR register bits	-	10	-	bits
Resolution	RES	VIN=0 to V_{DDIO}	1.8	-	3.6	mV/LSB
Input voltage range	V_{IN}		0	-	V_{DDIO}	V
Zero-scale error	E_{ZS}	10-bit accuracy	-2.0	-	2.0	LSB
Full-scale error	E_{FS}	10-bit accuracy	-2.0	-	2.0	LSB
Differential non-linearity	DNS	10-bit accuracy	-2.0	-	2.0	LSB
Integral non-linearity	INS	10-bit accuracy	-2.0	-	2.0	LSB
Conversion time	T_L	Clock cycle = 400 ns	10	-	-	us

5-9. Temperature Sensor Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Accuracy	E_{TS}	TBD	-5	-	+5	°C
Temperature gradient	T_C	TBD	-	-3.5	-	mV/°C
Output potential	V_{TS}	25°C	-	760	-	mV
Conversion time	T_L	Clock cycle = 400 ns	10	-	-	us

5-10. Reset Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETN activation time (pulse width) (When starting from VDDIO=0V)	T_{RPW}	-	200	-	-	ns
RESETN pulse time 2 (*1) (When starting from VDDIO≠0V)	T_{RPW2}	VDD>1.8 V	500	-	-	us

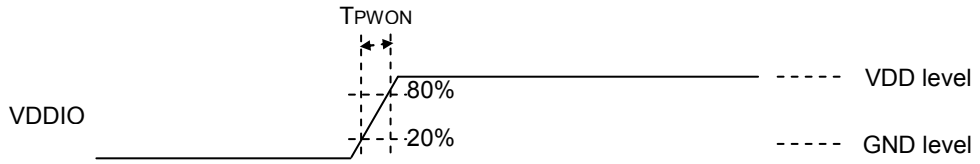


(*1) When starting from VDDIO≠0V, input a pulse to the RESETN signal after VDDIO exceeds 1.8 V.

(*2) This is reset by the power-on reset circuit built in the LSI at power-on.

5-11. Power-On Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power-on time difference	T_{PWON}	At power on (All power supply pins)	-	-	5	ms



6. Functional Description

*** For the RF block, refer to ML7396B Data Sheet.**

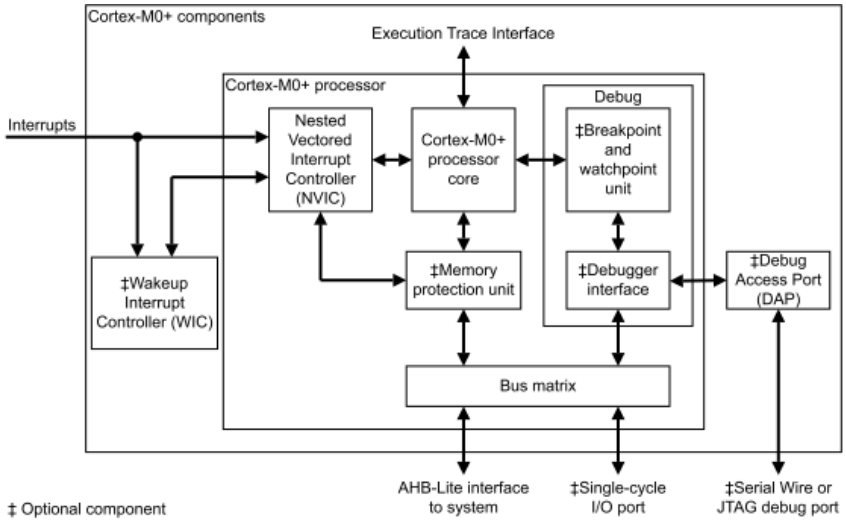
6-1.CPU (Cortex-M0+)

A RISC processor manufactured by ARM.

It is a 32-bit processor for small size and low power consumption applications and has a 2-stage pipeline configuration. It implements the ARMv6-M architecture, and operates with 16-bit Thumb instructions and Thumb-2 instructions.

The configuration is as follows:

- Little-Endian
- Number of break points: 4
- Number of watch points: 2
- SysTick timer, a 24-bit system timer, is included
- NVIC (Nested Vectored Interrupt Controller) is included
- Multiplier: High-speed (1-cycle) hardware multiplier is provided
- SLEEP/DEEPSLEEP supported
- WFI (Wait for Interrupts)/WFE (Wait for Events) supported
- Relocatable vector table
- MTB-M0+ supported



Cortex-M0+ Schematic Diagram

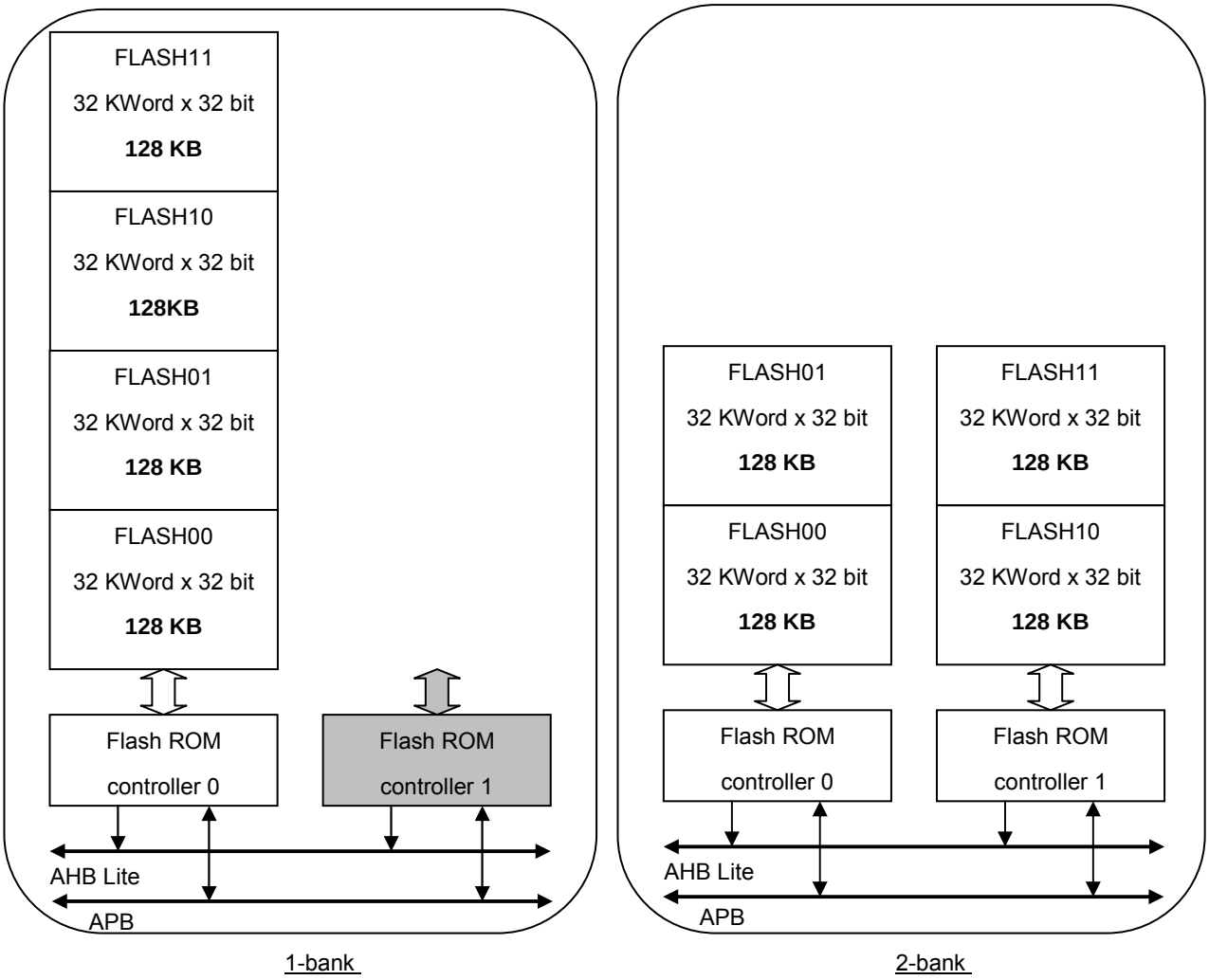
6-2.Flash ROM Controller

Flash ROM controllers are included. The boot from the Flash ROM is possible.

- For the Flash ROM area of 512 KB, the 256 KB x 2 bank configuration or the 512 KB x 1 bank configuration can be selected.
- For each bank, a Flash ROM controller is connected.
- Rewriting from the debugger through the debug port (SWD) is possible.

  In the 2-bank configuration, the program of one bank can be rewritten dynamically while the other CPU is running on another bank.

  In the 1-bank configuration, a rewriting program can be started from the ISP area or SRAM area.
- It is possible to perform the 1-word rewrite, sector erase, block erase, or chip erase.
- The bank can be assigned to the remapping area (4 Kbytes) starting at 0x00000000 by the remapping function.
- The ROM area is divided into the trimming area to store the trimming value of analog macro, boot program area to store the starting program such as ISP, security area to store the security setting, and user area, and the trimming area, boot program area, and security area are protected.



* At power-on, the system always starts in 1 bank mode.

* In 2 bank mode, only the bank 0 side can be rewritten from the debugger.

* Only when both of the two Flash ROM controllers are not executing the processing, the transition to Sleep or DeepSleep is possible.

6-3.Interrupt Controller

The NVIC (Nested Vector Interrupt Controller) is included in Cortex-M0+. The following interrupt sources are provided:

- 30 IRQs

6-4.SRAM IF

The SRAM IF of 64 KB is provided.

6-5.AHB-lite Bus

An AMBA 3 AHB-lite bus is included, to which an AHB slave can be connected.

6-6.APB Bus

An AMBA 2.0 APB bus is included, to which an APB slave can be connected.

6-7.Single-cycle I/O Port

A single-cycle I/O port which can be accessed in one cycle is included.

6-8.Debug Port

The SWD (2-wire serial wire debug port) is included as an interface for communicating with the debugger.

The internal resources can be accessed through this interface.

It also can be used for writing to on-chip memory such as a Flash ROM from the debugger.

6-9.MTB

The MTB (Micro Trace Buffer) which enables the execution trace of Cortex-M0+ is included. This MTB shares the data RAM as the memory for trace.

6-10. Clock

This section describes the following three clocks:

- System clock system
- Debug port clock system
- Peripheral clock system

6.10.1 System Clock System

Clocks supplied to the CPU core and bus.

The maximum frequency is 40 MHz.

There are three derived clocks that are gated depending on the processor operation state.

Clock	Name	Description
CLK	Source Clock	The source clock. This clock can operate at up to 40 MHz with the internal PLL (multiplying/dividing of N/M ratio) or internal RC OSC.
FCLK	Free Running Clock	This clock can be stopped during the DEEPSLEEP state. It is supplied during the SLEEP state. This is used by the Wakeup Interrupt Controller and Power Management Unit in the Cortex-M0+.
SCLK	Processor System Clock	This clock is stopped during the DEEPSLEEP state. It is supplied during the SLEEP state. This clock (or its derived clock) should be connected to any device that needs to operate during the SLEEP state.
HCLK	AHB Clock	This clock is stopped during the DEEPSLEEP or SLEEP state. This clock (or its derived clock) should be connected to any device that does not operate during the SLEEP state.
DCLK	Debug domain clock	This clock is always supplied when the Debugger is connected.

CPU Clock System

6.10.2 Debug Port Clock System

This clock system is supplied to JTAG I/F.

It is supplied from the debugger outside the chip.

The maximum frequency of the debug port clock system is 10 MHz.

6.10.3 Peripheral Clock System

This clock system is supplied to peripherals.

6.10.3.1 UART Reference Clock

This is the reference clock for baud rate generation. To reduce the baud rate error, this clock frequency needs to be adjusted. Example) When the reference clock frequency = 40.57 MHz (32.768 KHz X'tal OSC multiplied by 1238 by PLL), the baud rate error is about 0.1% at 115.2 kbps.

6.10.3.2 SPI Reference Clock

This clock is the source for generating the SPI(Master/Slave) serial clock. The frequency of the clock for serial communication is lower than 1/2 of the frequency of this reference clock.

6.10.3.3 SSIS Sampling Clock

This clock is used for the data transmission/reception in SSIS (SSI Slave, which is available only in the ISP function). It is used in the ISP function. The frequency of the clock for serial communication is lower than 1/10 of the frequency of this reference clock.

6.10.3.4 WDT Clock

This clock drives the watchdog timer.

It can measure the time of about hundreds of μsec to dozens of msec.

32.768 kHz input, 32 KHz CR input or source clock divide can be selected.

6.10.3.5 GPIO Debounce Clock

The debounce circuit that performs sampling at a fixed interval is implemented to eliminate the effect of noise and chattering when using the input signal from GPIO as an external interrupt source. This clock is used by the debounce circuit.

6.10.3.6 Timer Clock

This clock is used by the standard 32-bit timer.

32.768 kHz X'tal input, 32 KHz CR input or source clock divide can be selected.

6.10.3.7 RTC Clock

This clock is used by the real time clock (RTC).

32.768 kHz X'tal input, 32 KHz RC input or source clock divide can be selected.

6.10.3.8 Flexible Timer Clock

This clock is used by the flexible timer (FTM).

32.768 kHz input or 32 KHz RC input can be selected.

6.10.3.9 I2C Reference Clock

The reference clock for generating a serial clock for I2C communication. The I2C clock depends on the serial communication mode (Standard mode, Fast mode) that it supports.

The frequency of I2C reference clock must be higher than that of system clock.

Minimum Frequency of I2C Reference Clock

Mode	Minimum frequency	I2C bus ratio
Standard mode	2.7MHz	100kbps
Fast mode	12MHz	400kbps

6.10.3.10 Flash ROM Controller Clock

This clock is used by the flash ROM controller.

6.10.3.11 DIO Clock

This clock is used by DIO.

6.10.3.12 RAND_GEN Clock

This clock is used by RAND_GEN (pseudo-random number generation circuit).

6.10.3.13 CLK_Timer Reference Clock

This clock counts the low-speed clock with CLK_Timer.

40 MHz RC clock output, RF clock output or PLL clock output can be selected.

6.10.3.14 SysTick Timer Clock

This clock drives the SysTick timer in Cortex-M0+.

It is usually 1 MHz. It is 32 KHz at the CPU low speed (32 KHz) mode.

6.10.3.15 AES Clock

This clock is used by AES.

6.10.3.16 ADC Clock

This clock is used by the ADC controller. It is the ADC sampling frequency (Max = 2.5 MHz) or less.

6.10.3.17 TEMP Clock

This clock is used by the temperature sensor controller. It is the ADC sampling frequency (Max = 2.5 MHz) or less.

6.10.3.18 LVD Clock

This clock is used by the low voltage detection controller.

6.10.3.19 DMAC Clock

This clock is used by the DMA controller.

6.10.3.20 Flash DMA Clock

This clock is used by the flash DMA controller.

6-11. Reset

The relationship between the reset system and the reset target is shown in the table "Reset Causes and Reset Targets" below.

The reset causes include hardware reset, SYSRESETREQ reset of Cortex-M0+, peripheral reset, debugger reset without the debugger connected, WDT reset, voltage detection reset and reset at CPU LOCKUP.

The hardware reset occurs during the initial operation of hardware including reset by an external pin or reset at power-on triggered by power-on detection. When a hardware reset occurs, the reset circuit asserts the reset systems connected to all initializable circuits and initializes those circuits.

The SYSRESETREQ reset of Cortex-M0+ occurs when the SYSRESETREQ bit of Application Interrupt and Reset Control Register (AIRCR) within Cortex-M0+ is set from the CPU or debugger. The CPU, peripherals, bus, and memory IF are initialized, while the program fetches the reset exception vector.

The peripheral reset resets only the target peripheral by setting the bit assigned to each peripheral in the peripheral reset registers.

When the debugger is not connected, the debug circuit is always in reset state to prevent unnecessary switching or malfunctions caused by the debug circuit.

The WDT reset, voltage detection reset and the automatic reset at CPU LOCKUP initialize all initializable circuits except the CPU status register and the debug circuit.

Reset Causes and Reset Targets

Reset system	Reset target					
	Hardware reset Power-on reset	LVD reset	WDT reset/voltage detection reset/automatic reset at CPU LOCKUP	SYSRESETREQ bit set of Cortex-M0+ AIRCR register	Peripheral reset	When the debugger is not connected
CPU_ST register	○	-	-	-	-	-
Control registers with the Sticky attribute, excluding the CPU_ST register	○	○	○	-	-	-
System hardware such as clock control circuit and power management circuit	○	○	○	-	-	-
CPU AHB bus/peripheral	○	○	○	○	-	-
APB bus/peripheral	○	○	○	○	○	-
SingleCycleIO bus/peripheral	○	○	○	○	○	-
Flash ROM	○	○	○	-	-	-
RF	○	○	-	-	○	-
Debug reset	○	-	-	-	-	○

6-12.Power Management

Low power consumption is realized by clock control and power control.

6.12.1 Operation Mode

The power management function of this LSI has the following features:

- The low power consumption states, SLEEP and DEEPSLEEP, are supported.
- The clocks are stopped depending on each low power consumption state.

The following basic power states are defined in this LSI:

Operation mode	Operation state		Current consumption	Return to Active mode	
	Power mode of Cortex-M0+	LSI	Current consumption	Method	Time
Active	RUN	All clocks are supplied. However, the clock delivery to peripherals (including RF) can be set to on/off by the register.	11mA	-	-
SLEEP	Sleep	AHB bus clock (FlashROM/RAM) is stopped. The clock delivery to peripherals (including RF) can be set to on/off by the register.	5mA	Interrupt from a peripheral. Start the debugger	75nsec
DEEPSLEEP	DeepSleep	The main clock is stopped. The clock delivery to sub clock system peripherals (RTC, TIMER, etc.) can be set to on/off by the register. The power supply to FlashROM/SRAM/non-sub clock system peripherals/RF can be set to on/off with the register setting.	2μA	Interrupt from a sub clock system peripheral. Start the debugger	150usec

6.12.2 Power Separation

This LSI can operate at low power consumption by turning off some power supplies in the LSI during DEEPSLEEP state.

The following function blocks can be set to power on/off.

Function block	Target range	Setting register	Remarks
SRAM	Unit of 32 KB (up to 64 KB)	SLEEP setting register (0x40050014) bits 8-9	
FLASH	Whole 512 KB area	SLEEP setting register (0x40050014) bit 10	
RF	Whole RF chip area	SLEEP setting register (0x40050014) bit 11	
Logic	CPU, FlashCnt, STD GPIO, AES, DAMC, FlashDMA, UART, SPI, I2C, RAND, SSIS, FTM, CLK Timer, DIO, ADC, TEMP	SLEEP setting register (0x40050014) bit 12	

6-13.System Control

System Control is a block which controls the whole system (including the control of clocks, reset, remapping, interrupt, and SysTick timer) and displays the ID information specific to each chip and the CPU status information.

6.13.1 Clock Control

- Selects the clock source (CR40M, RF clock, XTAL32K, CR32K, or PLL).
- Stops/resumes the clock of each peripheral.
- Sets the operation (automatically stops the clock) when the CPU goes to the low power consumption state (SLEEP or DEEPSLEEP) for each peripheral.
- Changes the frequency of system clock or clock supplied to each peripheral.

6.13.2 Reset Control

- Able to reset individual peripherals.
- Sets the operation when the CPU goes to the LOCKUP state.
- Indicates that the CPU is initialized by the reset due to LOCKUP or the reset caused by low voltage detection or watchdog timer.

6.13.3 Information Display

Displays the ID information specific to each chip to distinguish individual chips.

6.13.4 Remapping Control

Selects a device to be placed in the remapping area on the address space.

6.13.5 Cortex-M0+ Control

Changes the settings of Nested Vectored Interrupt Controller (NVIC) and SysTick timer mounted in Cortex-M0+.

6.13.6 Boot Program

The boot program stored in the boot program area.

For details, refer to "ML7416 Boot_Programing Function Specifications".

6-14.Peripheral

This LSI implements the following peripherals: UART, SPI, SSIS, WDT, GPIO (APB GPIO), SingleCycleIO (STD GPIO), timer, RTC, flexible timer (FTM), I2C, Flash controller, DIO, RAND_GEN, CLK_Timer, AES, ADC, thermometer (TEMP), low voltage detection (LVD), DMAC, and Flash DMA.

6.14.1 UART

A start-stop synchronous serial communication interface which has functions equivalent to the industry standard 16550. The features are shown below.

- Includes a 16-byte FIFO for each of transmission and reception.
- Full-duplex communication is possible.
- Includes a programmable baud rate generator. Note that the baud rate is the same for transmission and reception.
- The character size of 5- to 8-bit is supported.
- 1 or 2 (1.5 for the 5-bit character size) stop bit can be selected.
- For parity generation/check, supports even/odd/none/stick.
- Supports the auto-flow control function.

6.14.2 SPI

A synchronous serial communication interface (master/slave). The features are shown below.

- Performs the full-duplex data transfer.
- Master or Slave mode can be selected.
- Includes a 16-byte or 16-word (16-bit) FIFO for each of the transmission and reception sides.
- For the transfer size, 8 bits (bytes) or 16 bits (words) can be selected.
- The interrupt caused by the number of received bytes (words) and the number of untransmitted bytes (words) can be set in the range 1 to 16.
- Either LSB first or MSB first can be selected.
- The polarity and phase of the serial clock can be selected.
- Able to control the interval before/after transfer in Master mode.
- Uses the status bit to indicate the completion of transmission/reception and the FIFO status.
- Able to detect a mode fault error to avoid multi-master bus contention.
- Able to detect a write overflow error if any further writing is attempted when the transmit FIFO is in the full state.
- Generates an interrupt when the transmit/receive FIFO is in a specific state or when a cause such as mode fault error occurs.

6.14.3 SSIS(SSI Slave)

A synchronous serial communication interface (for slave only). The features are shown below.

- Supports the Motorola SPI.
- Data length: 4 to 16 bits
- 8-stage FIFO for each of transmit and receive
- It is used in the ISP function.

6.14.4 WDT

Programmable 16-bit watchdog timer. The features are shown below.

- When the counter reaches its timeout, this timer asserts an interrupt at the first timeout, and performs the system reset operation at the second timeout. The mode of asserting only an interrupt without reset operation can be set.
- If the CPU is stopped by the SLEEP mode or debugger, the counter operation of watchdog timer is stopped.
- The source clock of the watchdog timer can be selected using the control register.

6.14.5 GPIO(APB-GPIO)

General-purpose port with interrupt function. The features are shown below.

- 13-bit (GPIOA) general-purpose port.
- Can be used as external interrupt input.* Either level/edge or Low/High can be selected.
- Includes the debounce circuit in the input side, which performs sampling at a fixed interval to eliminate the effect of noise and chattering.
- Can be used as return cause from SLEEP/DEEPSLEEP.

6.14.6 Standard GPIO (Single-cycle I/O)

General-purpose port connected to a single-cycle I/O which can be accessed in one cycle. The features are shown below.

- 4-bit (GPIOA) general-purpose port (assigned to the quintic function).

6.14.7 Timer

32-bit x 10ch general-purpose timer. The features are shown below.

- If the CPU is stopped by the debugger, the counter operation of timer is stopped.
- Can be used as 64-bit timer by the cascade connection (TimerB, TimerC, TimerD, and TimerE only).

6.14.8 RTC

Real time clock with perpetual calendar which can be read/written from a second unit. The features are shown below.

- Operates at 32.768 kHz input from the external or at internal 32 KHz RC.
- It is possible to set, correct, and read the time.
- Can be used as interrupt source.
- The time-designated interrupt can be generated.

6.14.9 Flexible Timer (FTM)

16-bit multifunction timer. The features (operation mode) are shown below.

- Auto-reload timer (ART)
- Compare out (CMO)
- Pulse width modulation (PWM)
- Capture (CAP)

6.14.10 I2C

2-wire (SCL, SDA) serial interface. The features are shown below.

- Supports the standard mode (up to 100 kbps) and the fast mode (up to 400 kbps).
- Supports the 7- or 10-bit addressing.
- Supports the 7- or 10-bit composite format transfer.
- Supports the bulk transfer mode.

6.14.11 Flash ROM Controller

Memory controller that controls the internal Flash ROM.

It operates as AHB slave when reading the Flash ROM.

Erase/write/register access of the Flash ROM operates as an APB slave.

6.14.12 DIO

Data transmission/reception interface dedicated to the RF block (ML7396B) control.

6.14.13 RAND_GEN

Pseudo-random number generation circuit. The features are shown below.

- The RAND length can be selected from RAND9, RAND15, and RAND23.
- Random number generation result can be output with the logical complement of 2.

6.14.14 CLK_Timer

This function uses the high-speed clock to count a certain time period of the low-speed clock and stores the count result in a register.

6.14.15 AES

This function performs the encryption and decryption of transmit/receive data by using Advanced Encryption Standard (AES).

The features are shown below.

- Encryption and decryption of 128-bit data (ECB, CBC, CTR, CCM, GCM, CFB and OFB supported)
- Generation and decryption of attestation tag (CCM128/64/32/16/8)

6.14.16 ADC

This function controls the 10-bit successive approximation type A/D converter.

The features are shown below.

- Programmable scan of up to three channels (CH0 to CH2) (The scan time and scan order can be set.)

  * Two channels when using the temperature sensor (CH2).
- Scan result notification (The scan completion is notified by an interrupt.)
- Averaging of A/D conversion data (The average value of A/D conversion results is displayed.)
- Calculation of CH0 to CH2 input voltage (It is assumed that the reference voltage output from the regulator at CH3 is monitored.)

6.14.17 Thermometer (TEMP)

1-channel temperature sensor to measure the temperature in the chip.

The features are shown below.

- Accuracy: ± 5 °C
- Converts the temperature to voltage and digitizes the converted voltage by using the 10-bit A/D converter.

6.14.18 Low Voltage Detection (LVD)

Low voltage detection function.

The features are shown below.

- The voltage detection level can be set.
- After detection, interrupt notification or reset can be selected.
- Starts the reference voltage (VBG) periodically by using the dedicated low speed timer to compare and determine the voltage detection level.

6.14.19 DMAC

Direct memory access controller. Among peripherals, SPI and AES support DMA transfer.

The features are shown below.

- 4-channel DMA controller.
- Each channel includes a 16-stage FIFO for source transfer and destination transfer.
- Supports the peripheral-to-memory transfer.
- Includes the hardware interface to handshake with SPI and AES.
- Supports up to 2048-byte block transfer.
- Supports the channel priority setting.
- Has one AHB master port.
- Supports increment/decrement of the transfer address and transfer to a single address.
- Supports multiple block transfer using a linked list.

6.14.20 Flash DMA

Controls the data write to the flash area and the data compare of the flash area at high speed, instead of CPU.

The features are shown below.

- Batch writes the data in the RAM area to the flash area.
- Compares the RAM area data and the Flash area data and notifies the result.

6.14.21 Others

Mode control (MODE_CNT): A set of registers for clock dividing setting, power separation control, and adjustment of analog circuits (regulator, RCOSC, RF, etc.).

7. Programming Model

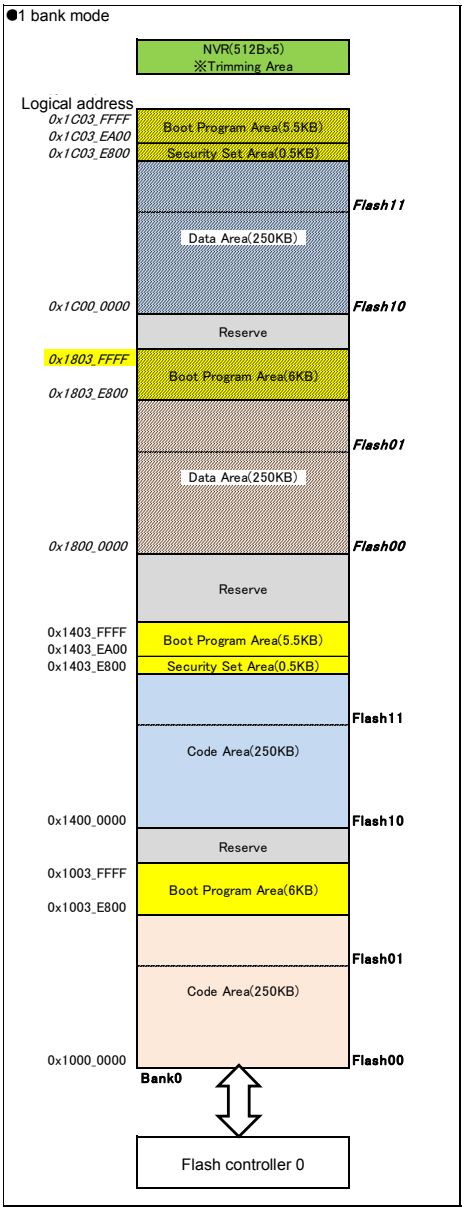
7-1.Address Map

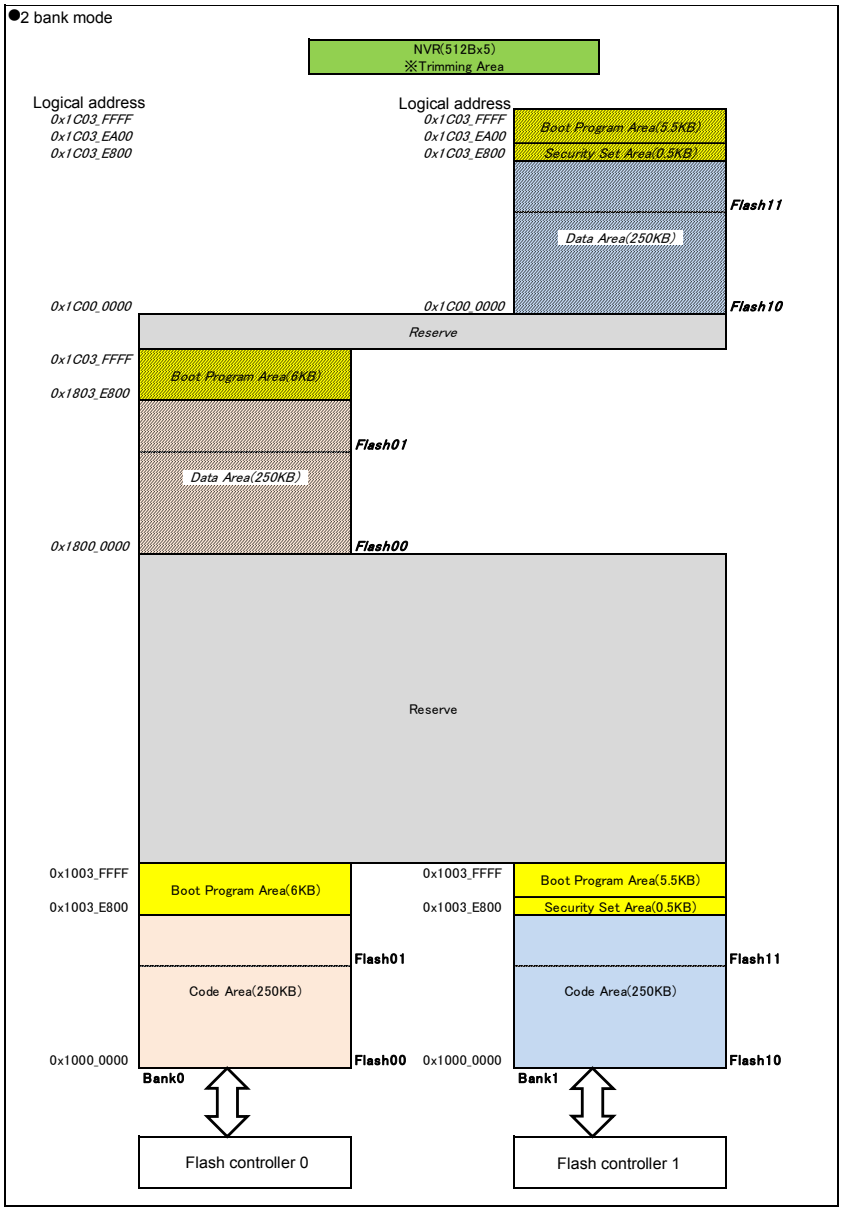
Table 7-1 Address Map and Table 7-2 Address Map (Details of AHB/APB/IO) show address maps.

Table 7-1 Address Map

Address range	Response device		Description
	Normal	REMAP	
0xF000_3000-0xFFFF_FFFF	Reserved		Reserved area.
0xF000_2000-0xF000_2FFF	MTB		Area assigned to the Micro Trace Buffer (SFR). This area is responded by the default slave when the security function of the flash ROM controller is enabled.
0xF000_1000-0xF000_1FFF	Reserved		Reserved area.
0xF000_0000-0xF000_0FFF	ROM Table		Area assigned to the system ROM table. This area is responded by the default slave when the security function of the flash ROM controller is enabled.
0x6000_0000-0xEFFF_FFFF	Reserved		Reserved area.
0x5C00_0404-0x5FFF_FFFF	Reserved		Reserved area.
0x5C00_0000-0x5C00_0403	STD GPIO		Area assigned to the Single-cycle I/O peripheral.
0x5800_0000-0x5BFF_FFFF	Reserved		Reserved area.
0x5000_0000-0x57FF_FFFF	Reserved		Reserved area.
0x4000_0000-0x4FFF_FFFF	AHB/APB		Area assigned to the AHB/APB device. For details, refer to "Table 7-2 Address Map (Details of AHB/APB/IO)".
0x2001_0000-0x3FFF_FFFF	Reserved		Reserved area.
0x2000_0000-0x2000_FFFF	SRAM		SRAM area (64 KB).
0x1C04_0000-0x1FFF_FFFF	Reserved		Reserved area.
0x1C03_EA00-0x1C03_FFFF	Flash ROM		Boot area of FLASH11 (5.5 KB).* Read-only
0x1C03_E800-0x1C03_E9FF	Flash ROM		Security area of FLASH11 (0.5 KB).* Read-only
0x1C02_0000-0x1C03_E7FF	Flash ROM		User area of FLASH11 (122 KB).* Read-only
0x1C00_0000-0x1C01_FFFF	Flash ROM		User area of FLASH10 (128 KB).* Read-only
0x1804_0000-0x1BFF_FFFF	Reserved		Reserved area.
0x1803_E800-0x1803_FFFF	Flash ROM		Boot area of FLASH01 (6 KB).* Read-only
0x1802_0000-0x1803_E7FF	Flash ROM		User area of FLASH01 (122 KB).* Read-only
0x1800_0000-0x1801_FFFF	Flash ROM		User area of FLASH00 (128 KB).* Read-only

Address range	Response device		Description
	Normal	REMAP	
0x1404_0000-0x17FF_FFFF	Reserved		Reserved area.
0x1403_EA00-0x1403_FFFF	Flash ROM		Boot area of FLASH11 (5.5 KB).
0x1403_E800-0x1403_E9FF	Flash ROM		Security area of FLASH11 (0.5 KB).
0x1402_0000-0x1403_E7FF	Flash ROM		User area of FLASH11 (122 KB).
0x1400_0000-0x1401_FFFF	Flash ROM		User area of FLASH10 (128 KB).
0x1004_0000-0x13FF_FFFF	Reserved		Reserved area.
0x1003_E800-0x1003_FFFF	Flash ROM		Boot area of FLASH01 (6 KB).
0x1002_0000-0x1003_E7FF	Flash ROM		User area of FLASH01 (122 KB).
0x1000_0000-0x1001_FFFF	Flash ROM		User area of FLASH00 (128 KB).
0x0008_0000-0x0FFF_FFFF	Reserved		Reserved area.
0x0000_0000-0x0007_FFFF	Flash ROM	SRAM	Remap area. Flash ROM is assigned as a mirror by default. When remapping, Flash ROM and SRAM areas can be assigned by using a value of REMAP pin or control register.


●1 bank mode
NVR(512Bx5)
※Trimming Area
Logical address
0x1C03_FFFF
0x1C03_EA00
0x1C03_E800
Boot Program Area(5.5KB)
Security Set Area(0.5KB)
Flash11
Data Area(250KB)
0x1C00_0000
Flash10
Reserve
0x1803_FFFF
Boot Program Area(6KB)
0x1803_E800
Flash01
Data Area(250KB)
0x1800_0000
Flash00
Reserve
0x1403_FFFF
0x1403_EA00
0x1403_E800
Boot Program Area(5.5KB)
Security Set Area(0.5KB)
Flash11
Code Area(250KB)
0x1400_0000
Flash10
Reserve
0x1003_FFFF
0x1003_E800
Boot Program Area(6KB)
Flash01
Code Area(250KB)
0x1000_0000
Flash00
Bank0
Flash controller 0


●2 bank mode
NVR(512Bx5)
※Trimming Area
Logical address
0x1C03_FFFF
0x1C03_EA00
0x1C03_E800
Boot Program Area(5.5KB)
Security Set Area(0.5KB)
Flash11
Data Area(250KB)
0x1C00_0000
Flash10
Reserve
0x1C03_FFFF
Boot Program Area(6KB)
0x1803_E800
Flash01
Data Area(250KB)
0x1800_0000
Flash00
Reserve
0x1003_FFFF
0x1003_E800
Boot Program Area(6KB)
Flash01
Code Area(250KB)
0x1000_0000
Flash00
Bank0
Flash controller 0
Boot Program Area(5.5KB)
Security Set Area(0.5KB)
Flash11
Code Area(250KB)
0x1000_0000
Flash10
Bank1
Flash controller 1

•The Flash ROM area consists of total 512 KB (128 KB x 4), including FLASH00/FLASH01/FLASH10/FLASH11.

•In 2 bank mode, it consists of FLASH00/FLASH01 (128 KB x 2) and FLASH10/FLASH11 (128 KB x 2).

•At power-on, the system always starts in 1 bank mode.

•The selection between 1 bank mode and 2 bank mode is made by the remapping control register SYSCON_REMAP_CON.

•The Boot Program Area is 11.5 KB in total, consisting of 0x1003_E800 to 0x1003_FFFF (6 KB) and 0x1403_EA00 to 0x1403_FFFF (5.5 KB).

•In the boot program start mode where the power is turned on by setting the mode0 pin to "H", 6 KB from 0x1003_E800 and 5.5 KB from 0x1403_EA00 are mapped to 11.5 KB from 0x0000_0000.

•The Security Set Area is 512 bytes from 0x1403_E800 to 0x1403_E9FF.

•In 2 bank mode, the logical addresses of both the Flash controller 0 and Flash controller 1 start from 0x1000_0000.

•In 2 bank mode, the update program can be written on the other side of the overlapping address from 0x1000_0000 to 0x1003_E800 by specifying the Flash controller in the software.

•For the area from 0x1800_0000 to 0x1C03_0000, 0x1800_0000 to 0x1803_FFFF and 0x1C00_0000 to 0x1C03_FFFF can always be referred by Flash00/Flash01 and Flash10/Flash11 as mirror areas respectively, regardless of the bank mode and bank selection. However, these mirror areas can be used only for data reference, but not for program execution (program code cannot be fetched).

Table 7-2 Address Map (Details of AHB/APB/IO)

Address range	Response device	Description
0x5C000404-0x5FFFFFFF	Reserved	Reserved area.
0x5C000000-0x5C000403	STD GPIO	Single-cycle I/O area.
0x50000000-0x5BFFFFFF	Reserved	Reserved area.
0x4017009C-0x4FFFFFFF	Reserved	Reserved area.
0x40170000-0x4017009B	AES	AES area.
0x40160020-0x4016FFFF	Reserved	Reserved area.
0x40160000-0x4016001F	Flash DMA	Flash DMA area.
0x40150400-0x4015FFFF	Reserved	Reserved area.
0x40150000-0x401503FF	DMAC	DMAC area.
0x40140818-0x4014FFFF	Reserved	Reserved area.
0x40140800-0x40140817	SPI2	SPI2 area.* For ML7396B control (dedicated to master) * Actual address after address conversion
0x40090030-0x401407FF	Reserved	Reserved area.
0x40090000-0x4009002F	LVD	Low voltage detection area.
0x40080040-0x4008FFFF	Reserved	Reserved area.
0x40080000-0x4008003F	Reserved	Reserved area.
0x4007002C-0x4007FFFF	Reserved	Reserved area.
0x40070000-0x4007002B	ADC	ADC area.
0x40060040-0x4006FFFF	Reserved	Reserved area.
0x40060000-0x4006003F	Reserved	Reserved area.
0x40050260-0x4005FFFF	Reserved	Reserved area.
0x40050000-0x4005025F	MODE _CNT	Mode control area.
0x40045014-0x40045FFF	Reserved	Reserved area.
0x40045000-0x40045013	CLK_Timer	CLK_Timer area.
0x4004400C-0x40044FFF	Reserved	Reserved area.
0x40044000-0x4004400B	RAND_GEN	RAND_GEN area.
0x4004303C-0x40043FFF	Reserved	Reserved area.
0x40043000-0x4004303B	DIO	DIO area.* For ML7396B control
0x40042114-0x40042FFF	Reserved	Reserved area.
0x40042000-0x40042113	Ext_Timer	TimerF area.* 6ch

0x40041CB0-0x40041FFF	Reserved	Reserved area.
0x40041C00-0x40041CAF	TimerE	TimerE area.* Making 64-bit can be enabled by TimerD and the cascade connection
0x400418B0-0x40041BFF	Reserved	Reserved area.
0x40041800-0x400418AF	TimerD	TimerD area.* Making 64-bit can be enabled by TimerE and the cascade connection
0x400414B0-0x400417FF	Reserved	Reserved area.
0x40041400-0x400414AF	TimerC	TimerC area.* Making 64-bit can be enabled by TimerB and the cascade connection
0x400410B0-0x400413FF	Reserved	Reserved area.
0x40041000-0x400410AF	TimerB	TimerB area.* Making 64-bit can be enabled by TimerC and the cascade connection
0x40040820-0x40040FFF	Reserved	Reserved area.
0x40040800-0x4004081F	SPI2	SPI2 area.* For ML7396B control (dedicated to master) * Dummy address before address conversion
0x40040420-0x400407FF	Reserved	Reserved area.
0x40040400-0x4004041F	SPI1	SPI1 area.
0x40040020-0x400403FF	Reserved	Reserved area.
0x40040000-0x4004001F	SPI0	SPI0 area.
0x40018210-0x4003FFFF	Reserved	Reserved area.
0x40018000-0x4001820F	Port	Port configuration area.
0x40010100-0x40017FFF	Reserved	Reserved area.
0x40010000-0x400100FF	WDT	WDT area.
0x4000D0F4-0x4000FFFF	Reserved	Reserved area.
0x4000D000-0x4000D0F3	SSIS0	SSI (Slave) area.* It is used in the ISP function
0x4000A278-0x4000CFFF	Reserved	Reserved area.
0x4000A200-0x4000A277	GPIOC	GPIOC area.
0x4000A178-0x4000A1FF	Reserved	Reserved area.
0x4000A100-0x4000A177	GPIOB	GPIOB area.
0x4000A078-0x4000A0FF	Reserved	Reserved area.
0x4000A000-0x4000A077	GPIOA	GPIOA area.* It is used in the ISP function
0x40008100-0x40009FFF	Reserved	Reserved area.
0x40008000-0x400080FF	I2C0	I2C area.
0x40004900-0x40007FFF	Reserved	Reserved area.
0x40004800-0x400048FF	UART2	UART2 area.
0x40004500-0x400047FF	Reserved	Reserved area.

0x40004400-0x400044FF	UART1	UART1 area.
0x40004100-0x400043FF	Reserved	Reserved area.
0x40004000-0x400040FF	UART0	UART0 area.* It is used in the ISP function
0x40003070-0x40003FFF	Reserved	Reserved area.
0x40003000-0x4000306F	RTC	RTC area.
0x40002208-0x40002FFF	Reserved	Reserved area.
0x40002000-0x40002207	Flexible Timer	Flexible timer area.
0x400010B0-0x40001FFF	Reserved	Reserved area.
0x40001000-0x400010AF	TimerA	TimerA area.* It is used in the ISP function
0x40000760-0x40000FFF	Reserved	Reserved area.
0x40000600-0x4000075F	Flash Control1	Flash ROM controller 1 area.
0x40000560-0x400005FF	Reserved	Reserved area.
0x40000400-0x4000055F	Flash Control0	Flash ROM controller 0 area.
0x40000200-0x400003FF	Reserved	Reserved area.
0x40000000-0x400001FF	System Control	System control area.

0x58000000 to 0x5FFFFFFF is responded by the STD GPIO. For the reserved area, writing is ignored and 0 is read at reading.

0x40150000 to 0x57FFFFFF is responded by the AHB peripheral. For the reserved area, responded by AHB error..

0x40000000 to 0x4014FFFF is responded by the APB peripheral. For the reserved area, writing is ignored and 0 is read at reading.

7-2.Remapping Control

A device to be assigned to the remapping area starting at the address 0x00000000 is selected by the external pin or control register. When power-on reset is generated, a memory device to be placed in the remapping area is determined according to the external pin state. After the power-on reset, a memory device to be placed in the remapping area is determined by the remapping control register.

For details of the remapping control register, refer to SYSCON_REMAP_CON (0x40000010).

Example of implementing the remapping control is shown below.

When REMAP_EN of the remapping control register = 0 (initial value)
- When the external pin MODE0 = L, internal Flash ROM is started first.
- When the external pin MODE0 = H, the boot program area in the internal Flash ROM is started first.

When REMAP_EN of the remapping control register = 1 (at software reset after rewriting the remapping control register by software)
- When REMAP[3:0] = 0b0000, internal Flash ROM is started first.
- When REMAP[3:0] = 0bxxx1, internal SRAM is started first.
- When REMAP[3:0] = 0bxx10, reserved
- When REMAP[3:0] = 0bx100, the address (boot program area) set at the remapping base address is started first.
- When REMAP[3:0] = 0b1000, reserved

[About Vector Table Relocation]

Cortex-M0+ makes the vector table relocatable by using the vector table offset register (VTOR). Please note that VTOR is reset by a software reset (AIRCR.SYSRESETREQ).

Also, note that the relocation of the vector table is performed immediately after rewriting VTOR. The access to the SCS area involves the DSB instruction in Cortex-M0+. It is not necessary to insert the DSB instruction. For details, refer to the following:

DAI0321A_programming_guide_memory_barriers_for_m_profile.pdf

4.11 Vector table configuration - Vector Table Offset Register (VTOR)

7-3.Internal Flash ROM Space

Area to which the internal Flash ROM is assigned (512 KB). It is normally used as the program ROM space.

At reading, internal Flash ROM is read via the Flash ROM controller. Rewriting the Flash ROM (erasing and programming) is performed by the rewrite sequence via the Flash ROM control register.

For the assignment of Flash ROM space, refer to the address map.

7-4.Internal SRAM Space

Area where internal SRAM is assigned (64 KB). It is normally used as a data RAM space.

It can be assigned as a remapping area by the remapping control register. It can be used as a program storage area when rewriting the Flash ROM.

7-5.Interrupt Source

Assignment of interrupt sources for this LSI is shown in Table List of Interrupt Sources below.

List of Interrupt Sources

Interrupt number	Interrupt source
NMI	Reserved
IRQ[0]	WDT
IRQ[1]	Reserved
IRQ[2]	GPIOA
IRQ[3]	TimerA
IRQ[4]	GPIOB
IRQ[5]	RTC
IRQ[6]	TimerB
IRQ[7]	TimerC
IRQ[8]	Flexible Timer
IRQ[9]	GPIOC
IRQ[10]	UART0
IRQ[11]	SSIS
IRQ[12]	ADC
IRQ[13]	AES
IRQ[14]	UART1
IRQ[15]	UART2
IRQ[16]	TimerD
IRQ[17]	Flash Control0
IRQ[18]	TimerE
IRQ[19]	Ext_Timer
IRQ[20]	I2C
IRQ[21]	DMAC
IRQ[22]	SPI0
IRQ[23]	SPI1
IRQ[24]	Flash DMA
IRQ[25]	Flash Control1
IRQ[26]	SPI2

IRQ[27]	DIO
IRQ[28]	LVD
IRQ[29]	RF
IRQ[30]	CLK_Timer
IRQ[31]	MODE_CNT

7-6,7-7,…,7-30,7-31.

T.B.D.

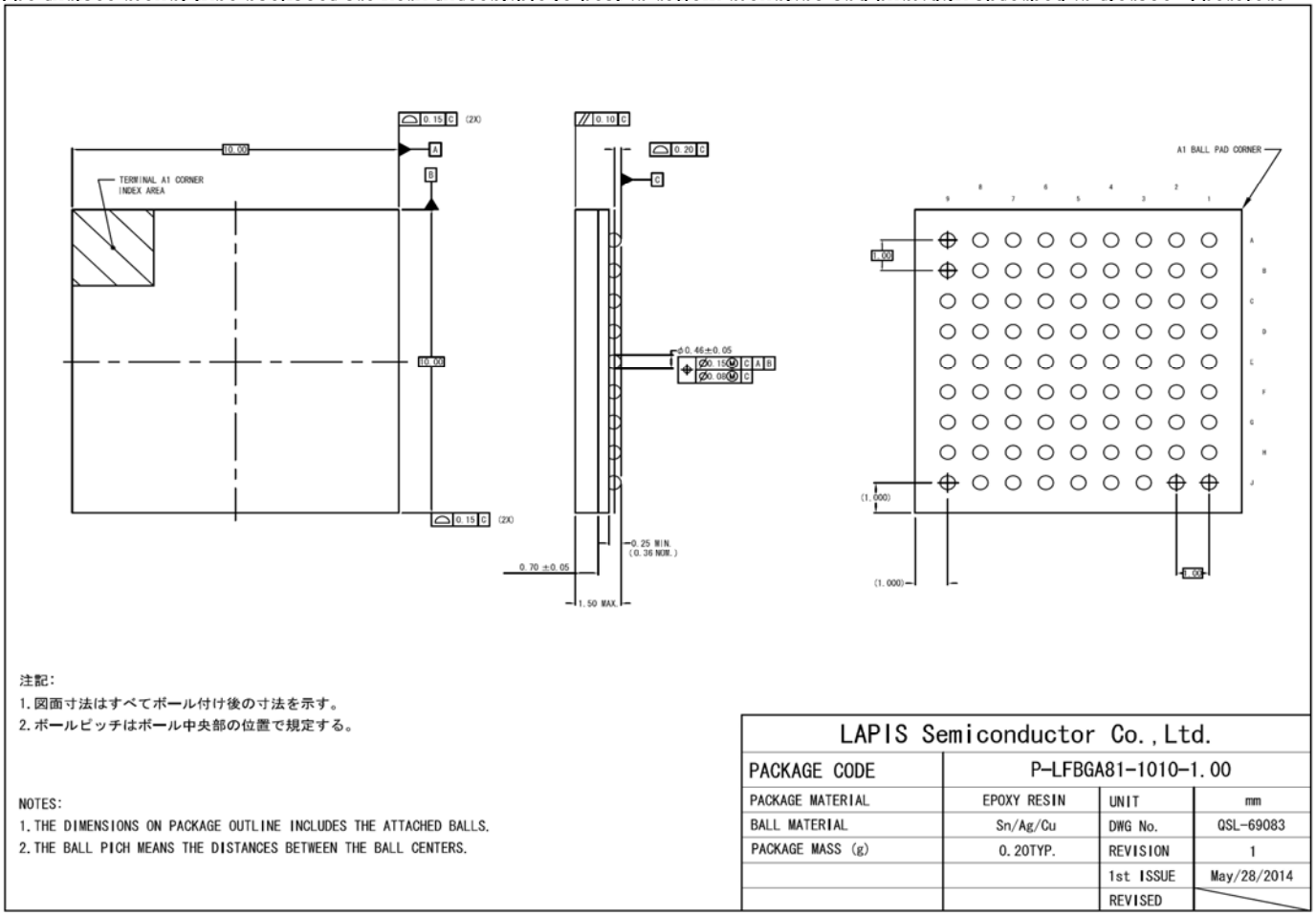
8. Examples of Application Circuit

T.B.D.

9. Package External Dimensions

○81-pin BGA

Remarks for surface mount type package



10. Revision History

Version	Revision description	Before change	After change	Date	Remarks
1	First edition	-	-	Apr 30, 2015	

NOTES

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