FEDL-7631-04
Issue Date December 25, 2025

ML7631

13.56MHz Wireless charging transmitter LSI

■ Overview

The ML7631 is a wireless charging Tx LSI using 13.56MHz carrier frequency, which enables to feed 200mW wirelessly to an Rx device using the ML7630. The ML7631 controls wireless charging and data communication with the ML7630.
ML7631 is equipped with function to detect the illegal situation such as disappearance of the Rx device. This is an ideal solution for small rechargeable devices such as headset, ear-pads and wearables.

■ Features

- Power transmission control
  - Power transmission circuit embedded
  - Abnormaly detection by software control and hardware control(voltage and current monitoring)

- Communication control
  - Command generation function for ML7630 included
  - Communication speed: 212kbps (13.56MHz/64)
  - 1kbyte data flash for storing some data contents

- Host interface(I^2C slave)
  - Normal mode(100kbit/s), Fast mode(400kbit/s) available
  - Each internal controller and external HOST microcontroller can access register function

- General Port(PORT)
  - Input/Output port×11ch

- Reset
  - Reset by RESET_N port
  - Power on reset by magnetic field detection
  - Reset by WDT overflow

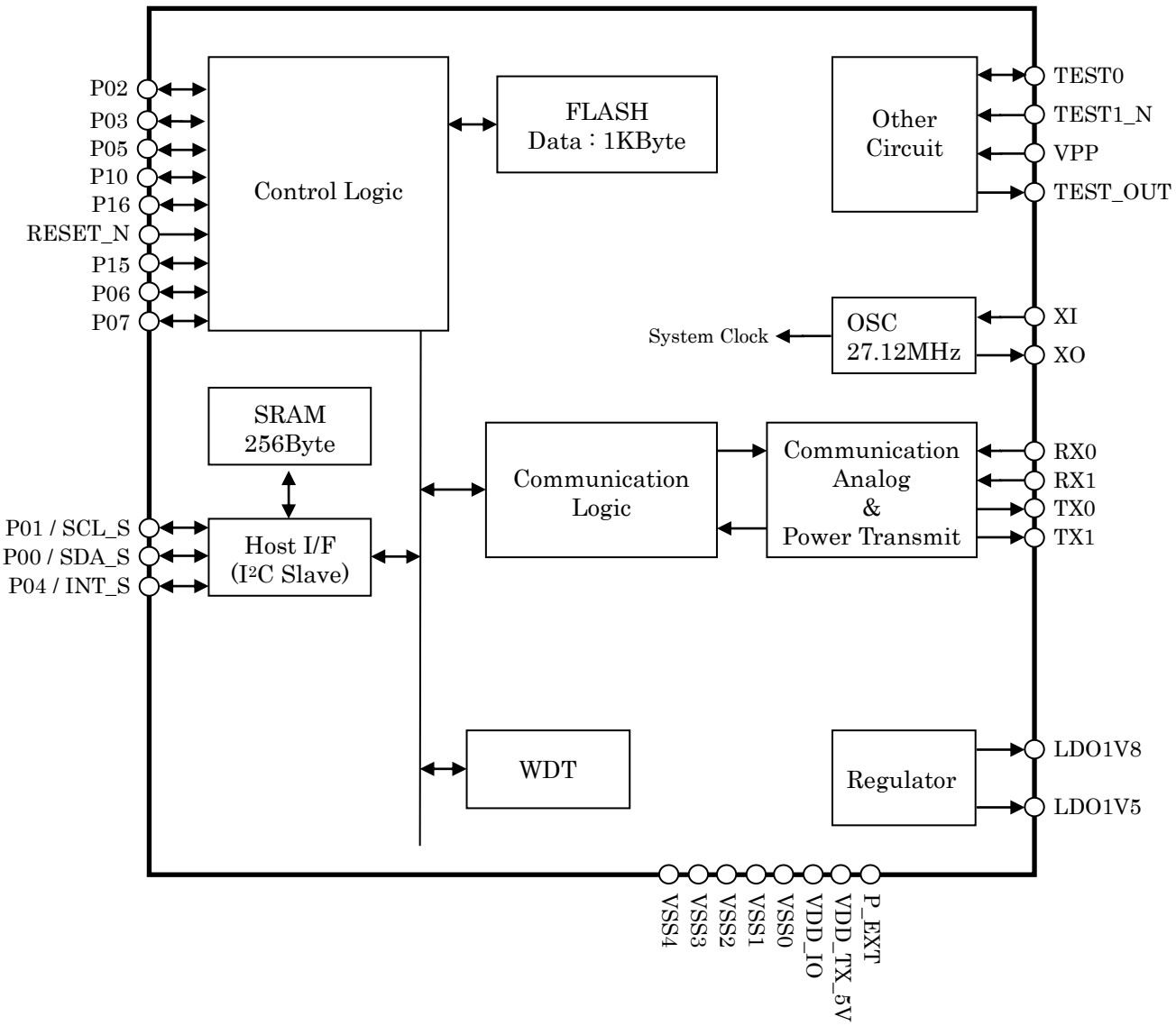
- Clock
  - Low speed clock : Built-in RC oscillation (32.768kHz) for internal timer
  - High speed clock : Crystal osillation(27.12MHz) 6.78MHz is used inside

- Package
  - WQFN 32 pin (P-WQFN32-0505-0.50)

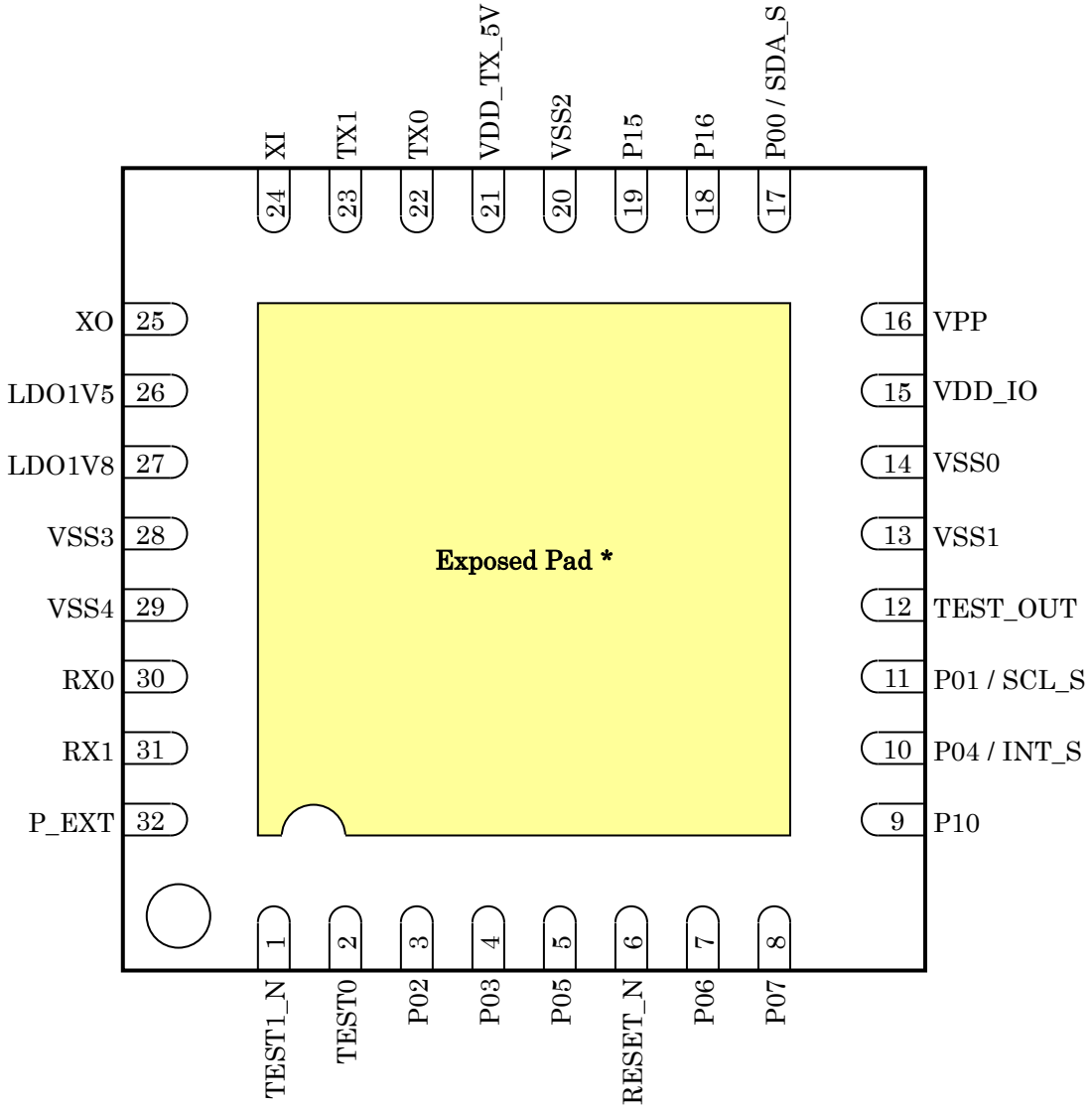
- Product name
  ML7631-103GD
  ML7631-106GD

- Applications
  NFC charging devices, e.g.
  ・smart wathes, fitness trackers and smart wristbands
  ・smart rings
  ・smart glasses
  ・true wireless stereos and hearing aids
  ・stylus pnes, wireless mouses and wireless keyboads
  ・electric toothbrushes
  ・beauty home appliances
  ・personal health care devices
  ・battery packs

■ Functional block structure



■ Pin assignment (Top view)



* Solder the exposed pad onto the PCB

■ Pin description

- Power · GND · reference voltage pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active Level	Description	Process in not use
14	VSS0	−	−	−	Ground	−
13	VSS1					
20	VSS2					
28	VSS3					
29	VSS4					
15	VDD_IO	−	−	−	Logic IO voltage	−
26	LDO1V5	H(A)	O_A	−	Core 1.5V voltage output	−
27	LDO1V8	H(A)	O_A	−	ADC 1.8V voltage output	−
32	P_EXT	−	−	−	External voltage (5V)	−
21	VDD_TX_5V	−	−	−	TX voltage (5V)	−

- Analog signal pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply Power	Active Level	Description	Process in not use
30	RX0	−	I_A	−	−	RF Data receiving	−
31	RX1	−	I_A	−	−	RF Data receiving	−
22	TX0	Z	O_A	VDD_TX_5V	−	RF Data transmitting	−
23	TX1	Z	O_A		−	RF Data transmitting	−

- Clock pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply Power	Active Level	Description	Process in not use
24	XI	I	I	LDO1V5	−	27.12MHz oscillation pin	−
25	XO	O	O	LDO1V5	−	27.12MHz oscillation pin	−

- Reset pin

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply Power	Active Level	Description	Process in not use
6	RESET_N	PU	I	VDD_IO	L	Reset input	Open

- General pins

Since the settings differ depending on the FW Ver., refer to the application note for details.

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply Power	Active Level	Description
17	P00 / SDA_S	Z	I/O	VDD_IO	−	Input/Output port HostIF(I^2C slave) Data
11	P01 / SCL_S	Z	I/O	VDD_IO	−	Input/Output port HostIF(I^2C slave) Clock
3	P02	Z	I/O	VDD_IO	−	Input/Output port
4	P03	Z	I/O	VDD_IO	−	Input/Output port
10	P04 / INT_S	Z	I/O	VDD_IO	−	Input/Output port HostIF INToutput
5	P05	Z	I/O	VDD_IO	−	Input/Output port
7	P06	Z	I_{DA}/O	VDD_IO	−	Input/Output port
8	P07	Z	I_{DA}/O	VDD_IO	−	Input/Output port
9	P10	Z	I/O	VDD_IO	−	Input/Output port
19	P15	Z	I_{DA}/O	VDD_IO	−	Input/Output port
18	P16	Z	I/O	VDD_IO	−	Input/Output port

- Test pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply Power	Active Level	Description	Process in not use
2	TEST0	PD	I/O	VDD_IO	H	For test/For debugger	Open
1	TEST1_N	PU	I	VDD_IO	L	For test/For debugger	Open
16	VPP	−	I_A	−	−	Power supply for Flash test	Open
12	TEST_OUT	L(A)	O	VDD_IO	−	Test output port	Open

(*1) In reset state :

Pin state definition in reset state	L(O)	:	“L” level output
	H(O)	:	“H” level output
	L(A)	:	Analog “L” level output
	H(A)	:	Analog “H” level output
	PU	:	Pull-Up
	PD	:	Pull-Down
	Z	:	Floating state

(*2) I/O : For I/O definition, using under abbreviation

I/O definition	I_A	:	Analog input
	O_A	:	Analog output
	I	:	Digital input
	I/O	:	Bi-directional pin
	I_{DA}/O	:	Bi-directional pin, Input are digital and analog shared
	O	:	Digital output

■ Electrical characteristics

- Absolue maximum ratings

Item	Symbol	Condition	Rating	Unit
Power voltage (Digital IO)	VDD_IO	Ta=25°C	-0.3 to +6.5	V
Regulator input voltage	P_EXT	Ta=25°C	-0.3 to +6.5	V
Tx power voltage	VDD_TX_5V	Ta=25°C	-0.3 to +6.5	V
Core & crystal power voltage	LDO1V5	Ta=25°C	-0.3 to +2.0	V
Analog power voltage	LDO1V8	Ta=25°C	-0.3 to +6.5	V
Input voltage	V_{DIN}	Ta=25°C, Digital port	-0.3 to V_{DD_IO}+0.3	V
		Ta=25°C, TX0/TX1	6.5	V
		Ta=25°C, RX0/RX1	12	V
Input current	Ii	Ta=25°C, Digital port	-10 to +10	mA
Output voltage	V_{DO}	Ta=25°C, Digital port	-0.3 to V_{DD_IO}+0.3	V
Digital output current	I_{DO}	Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	2	W
Storage temperature	T_{stg}		-55 to +150	°C

- Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD_IO		1.8	–	5.5	V
	P_EXT		4.5	5.0	5.5	V
	VDD_TX_5V	Normal	4.5	5.0	5.5	V
Operating temperature	T_{a1}	Normal	-40	+25	+85	°C
	T_{a2}	Power transmission	-10	+25	+50	°C
Crystal oscillator frequency	f_{XTL}		Typ -0.05%	27.12	Typ +0.05%	MHz
Crystal oscillator load capacitance*	C_{DL} C_{GL}	NIHON DEMPA KOGYO Co., Ltd. NX2016SA(CL=6pF)	Typ -1%	8	Typ +1%	pF
	C_{DL} C_{GL}	NIHON DEMPA KOGYO Co., Ltd. NX2016SA(CL=8pF)	Typ -1%	12	Typ +1%	pF
	C_{DL} C_{GL}	KYOCERA Corporation CX1210SB(CL=6pF)	Typ -1%	8	Typ +1%	pF
	C_{DL} C_{GL}	KYOCERA Corporation CX2016SB(CL=8pF)	Typ -1%	12	Typ +1%	pF
	C_{DL} C_{GL}	TXC SMD SEAM SEALING XTAL 2.0 × 1.6(CL=8pF)	Typ -1%	12	Typ +1%	pF
LDO1V5 outside Capacitor	C_{LDO1V5}		Typ -10%	2.2	Typ +10%	µF
P_EXT outside Capacitor	C_{PEXT}		Typ -10%	2.2	Typ +10%	µF
LDO1V8 outside Capacitor	C_{LDO1V8}		Typ -10%	0.47	Typ +10%	µF
VDD_IO outside Capacitor	C_{VDDIO}		Typ -10%	0.1	Typ +10%	µF
VDD_TX_5V outside Capacitor	C_{TX5V}		Typ -10%	2.2	Typ +10%	µF

*) The optimum capacitance value varies depending on the circuit board.
Please consult with the Crystal oscillation circuit manufacturer.

- Flash memory operating conditions

Item	Symbo	Condition	Range	Unit
Operating temperature (Ambience)	T_{OP}	Write/erase	-40 to +85	°C
Operating voltage	P_EXT	Write/erase	2.7 to 5.5	V
Write time	C_{EPD}	–	10,000	times
Erase unit	–	Sector erase	1	KB
Erase time (Maximum)	–	Sector erase	100	ms
Write time	–	–	1 word (2 byte)	–

- Power transmission charactaristics

(VDD_IO=1.8 to 5.5V, VDD_TX_5V=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TX0/TX1 output frequency	F_{TX}	–	–	13.56	–	MHz

- Oscillation characteristic

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Low speed embedded RC oscillator frequency *1	f_{LCR}	–	-5%	32.768	+5%	kHz

*1 : 1024 cycle average

- Reset characteristics

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RESET_N pulse width	P_{RST}	–	200	–	–	µs
RESET_N noise removal Pulse width	P_{NRST}	–	–	–	0.3	µs

- AC characteristics (I^2C bus interface: Standard mode 100 kHz)

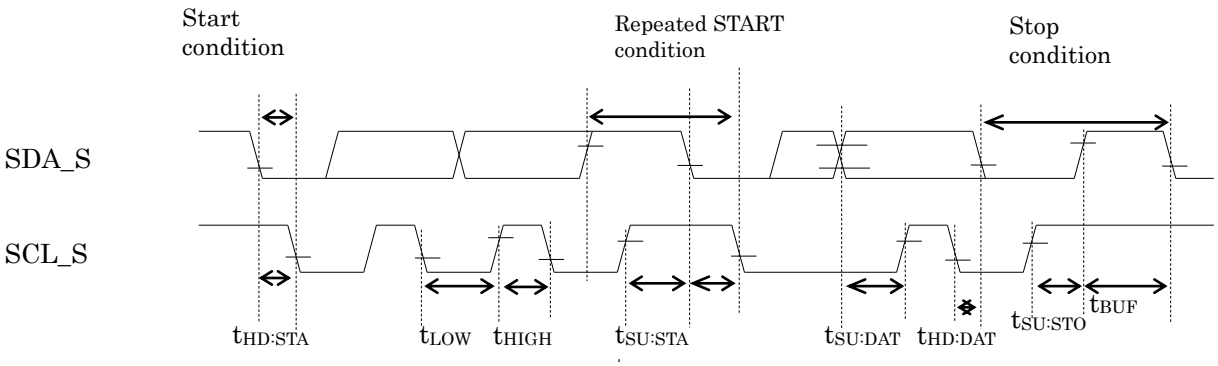
(VDD_IO =1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	100	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL_S "L" level time	t_{LOW}	–	4.7	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus free time	t_{BUF}	–	4.7	–	–	µs

- AC characteristics (I^2C bus interface: Fast mode 400 kHz)

(VDD_IO =1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	400	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL_S "L" level time	t_{LOW}	–	1.3	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus free time	t_{BUF}	–	1.3	–	–	µs



When connecting the I2C slave to the I2C bus common to other devices, insert a multiplexer or level shifter between the I2C bus and ML7631.

- IO characteristics

(Unless otherwise specified, VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Voltage 1 (P00-P07, P10, P15, P16)	VOH1	IOH=-1.0mA	VDD_IO -0.5	–	–	V
	VOL1	IOL=+0.5mA	–	–	0.4	V
Output Voltage 2 (P00-P07, P10, P15, P16) (LED pin)	VOL2	2.7V≤VDD_IO≤5.5V IOL=+5.0mA	–	–	0.6	V
		IOL=+2.0mA	–	–	0.4	V
Output Voltage 3 (SCL_S,SDA_S) (I^2C pin)	VOL3	IOL3= +3mA (I^2Cspec) (VDD_IO ≥2V)	–	–	0.4	V
Output Voltage 4 (SCL_S,SDA_S) (I^2C mode selected)	VOL4	IOL4= +2mA (I^2Cspec) (VDD_IO <2V)	–	–	VDD_IO ×0.2	V
Output Leakage 1 (P00-P07, P10, P15, P16, SCL_S, SDA_S)	IOOH1	VOH=VDD_IO (at high impedance)	–	–	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	–	–	μA
Input Current 1 (RESET_N, TEST1_N)	IIH1	VIH1=VDD_IO	–	–	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input Current 2 (TEST0)	IIH2	VIH2=VDD_IO	20	300	900	μA
	IIL2	VIL2=VSS	-1	–	–	μA
Input Current 3 (P00-P07, P10, P15, P16)	IIH3	VIH3=VDD_IO (In pull down)	1	15	200	μA
	IIL3	VIL3=VSS (In pull up)	-200	-15	-1	μA
	IIH3Z	VIH3=VDD_IO (at high impedance)	–	–	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	–	–	μA
Input Voltage 1 (RESET_N, TEST0, TEST1_N, P00-P07, P10, P15, P16)	VIH1	–	0.7× VDD_IO	–	VDD_IO	V
	VIL1	–	0	–	0.3× VDD_IO	V
Input pin Capacitance (RESET_N, TEST0, TEST1_N, P00-P07, P10, P15, P16)	CIN	f=10kHz Vrms=50mV Ta=25°C	–	10	–	pF

Typ. standard is at Ta=25°C, VDD_IO=3.0V

- Power supply current

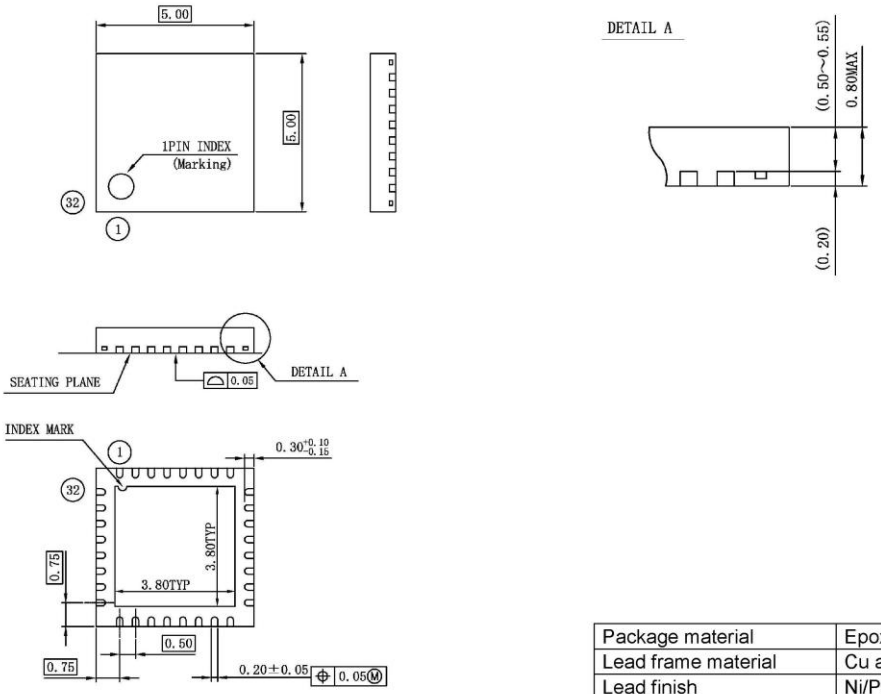
(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	IDD1	HALT*1	–	0.8	1.5	mA
	IDD2	CPU 6.78MHz operation Peripherals stop	–	2.2	3.0	mA
	IDD3	CPU 6.78MHz operation Power transmission mode (100Ω instead of antenna between TX0-TX1) *2	–	85	105	mA

*1) CPU Stops. This status can be released by peripheral interrupt.
*2) This condition and power supply current depend on the antenna.
If load resistance is small, the power supply current increases.
It does not guarantee the current consumption when the system including the power receiving side is installed.

■ Package dimensions

P-WQFN32-0505-0.50-A63



LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 max./0.15 max.
Package weight (g)	0.055 TYP.
Rev. No./Last Revised	2/Feb. 4, 2012

■ Revision history

Document No.	Issue Date	Page		Change contents
		Previous Edition	Current Edition	
PEDL7631-01	Oct. 25, 2016	–	–	Preliminary edition 1
FEDL7631-01	Mar. 23, 2018	–	–	Final edition 1
FEDL7631-02	Jan. 15, 2019	9	9	Add HALT description Revise IO-pin description
	Nov. 18, 2019	1 2 3 4 7	1 2 3 4 7	Delet Unused block
		4 5	4 5	Add Reset pin category Rename Other pins to General pins Added note for application note to general pin
		11	–	Delete Sample Circuit (Described in the application note because it depends on the FW)
		8	8	Change wording of I2C notice
		9	9	Add the conditions for current consumption during power transmission Change notice
		6	6	Change note about external crystal capacity
FEDL7631-03	Jan.11, 2024	-	2	Add product name and appications description
FEDL7631-04	Dec.25, 2025	-	13	Revise the contents of the notice

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