FEDL7660-11
Issue Date：January 30, 2026

ML7660

13.56MHz Wireless charging receiver LSI

■Overview

ML7660 is a 13.56MHz wireless power receiving LSI.
ML7660 can be combined with ML7661 to create a wireless power transfer system with a maximum power output of 1 W.
ML7660 is a 13.56 MHz wireless power transfer LSI.
ML7660 provides a 10-bit ADC for measuring power supply status and wireless power supply control functions in a 2.28 mm x 2.61 mm
(2.44 mm square equivalent) WLCSP chip or 5 mm square 32-pin WQFN package, making it the ideal LSI for wireless power supply in small devices.
In addition, it has a host interface (SPI (peripheral) / I^2C (target)) function and a serial interface (SPI (controller) / I^2C (target)) function,
The serial interface (SPI (controller) / I^2C (controller) / UART) function enables configuration data update and various sensor controls from an external microcontroller.

■Features

- Charging control
  Built-in Charging control circuit
  Voltage/Current supply ON/OFF function to external charging IC
  Voltage/Current supply ON/OFF function to external charging IC
  1W receiving available
  - Abnormality detection function by software control and hardware control
  - Abnormality notification function to the transmission side

- Communication control
  - Communication speed：212kbps, 424kbps
  - Equipped with 2Kbyte Data Flash for storing user data

- Host interface
  - Serial interface with 1-channel peripheral/target function (SPI and I^2C selectable)

- Package
  - WLCSP30pin (S-UFLGA30-2.28x2.61-0.40-W)
  - WQFN32pin (P-WQFN32-0505-0.50-A63)

- Applications
  - NFC Charging devices, e.g.
  - smart watches, fitness Trackers and smart wristbands
  - smart rings
  - smart glasses
  - true wireless stereos and hearing aids
  - stylus pens, wireless mouses and wireless keyboards
  - electric toothbrushes
  - beauty home appliances
  - personal health care devices
  - battery packs
  - rice cooker (for Batteryless)

●Product name

Product name	Packages	Firmware type
ML7660-320GD	WQFN	Charge Control
ML7660-320HB	WLCSP	Charge Control
ML7660-311HB	WLCSP	Charge Control for Reference Design (REF66003)
ML7660-210GD	WQFN	Batteryless
ML7660-NN0GD	WQFN	Blank
ML7660-NN0HB	WLCSP	Blank

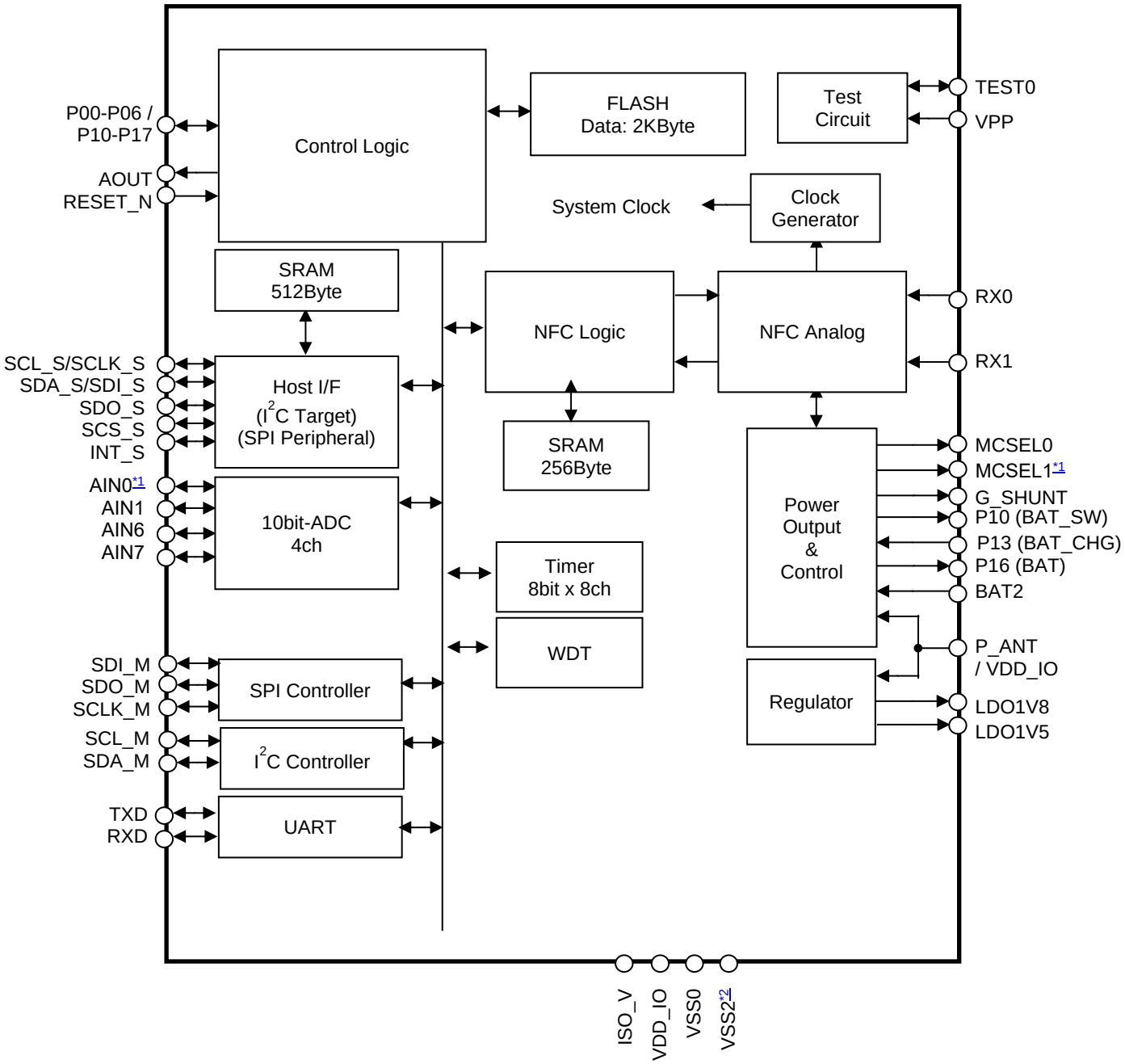
Note:
In the case of Batteryless for Reference Design (REF67011),
We provide the ML7660-NN0 (blank) and the Batteryless SDK sample software.
When ordering samples, please let us know if you need the LSI with the Batteryless SDK sample software written on it.

■Related Documents

In addition to this document, the following documents should also be read together as necessary.

・ML7661 Data Sheet
・ML7660 / ML7661Application Note

■Block Diagram



*1 only WLCSP 30pin
*2 only WQFN 32 pin

■Pin Assignment

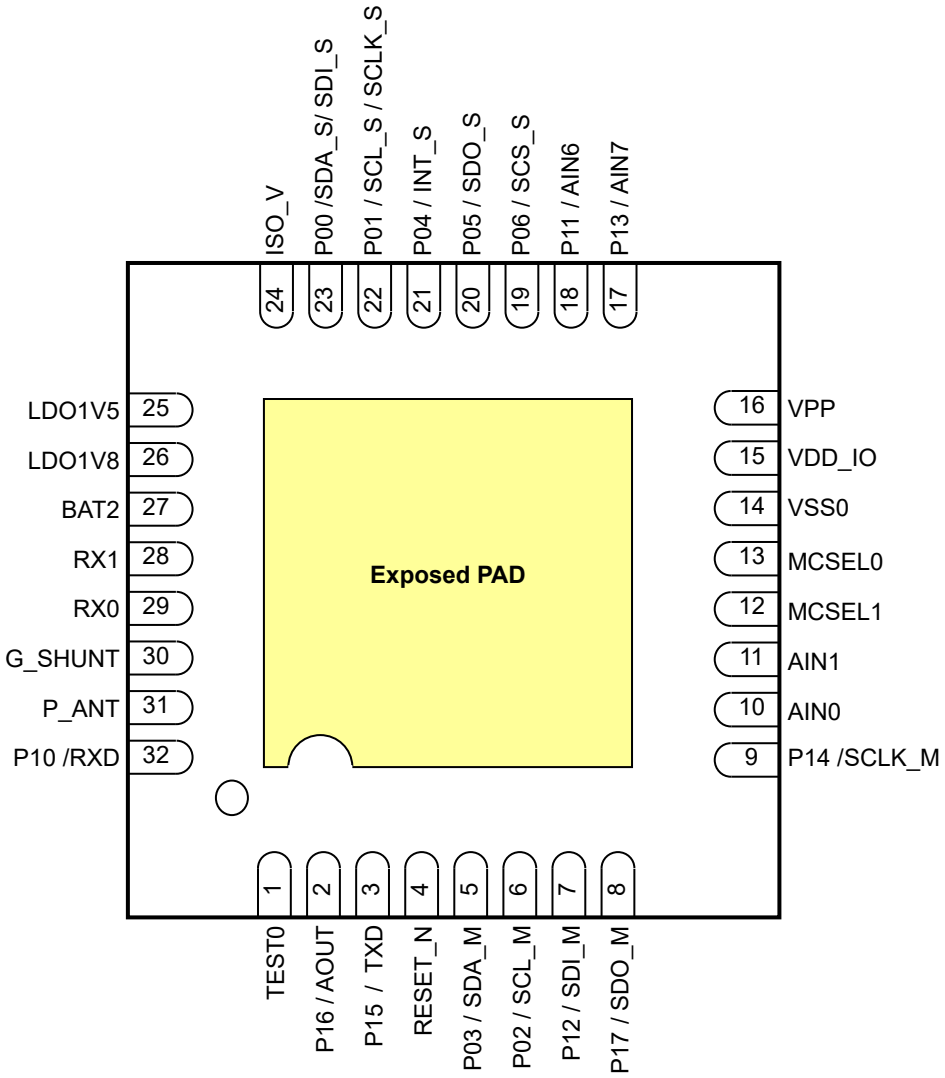
●WLCSP 30pin

BOTTOM VIEW

P13 / AIN7	VDD_IO	MCSEL0	AIN1	P14 / SCLK_M	6
P06 / SCS_S	P11 / AIN6	VPP	P17 / SDO_M	P12 / SDI_M	5
P04 / INT_S	P05 / SDO_S	VSS0	P02 / SCL_M	P03 / SDA_M	4
P00 / SDA_S / SDI_S	P01 / SCL_S / SCLK_S	VSS2	P15 / TXD	P16 / AOUT	3
ISO_V	RESET_N	TEST0	RX1	P10 / RXD	2
LDO1V5	LDO1V8	BAT2	RX0	G_SHUNT	1
E	D	C	B	A	

●WQFN 32pin

TOP VIEW



Note : The center square is the PAD on the back side of the package (exposed PAD).
The exposed PAD should be connected to the GND of the board.

■Pin list

Table 1 Pin list

PIN No. (WLCSP)	PIN No (WQFN)	Pin name (Function name) *3	1st function	2nd function	3rd function
C2	1	TEST0	Debug port	-	-
A3	2	P16/AOUT (BAT_DISCHARGE)	General purpose port	Analog monitor output	-
B3	3	P15/TXD (DEBUG)	General purpose port	UART data output	-
D2	4	RESET_N	Reset pin	-	-
A4	5	P03/SDA_M (INTERFACE)	General purpose port	I2C Controller data I/O	-
B4	6	P02/SCL_M	General purpose port	I2C Controller clock output	-
A5	7	P12/SDI_M (POWER)	General purpose port	SPI Controller data input	-
B5	8	P17/SDO_M (ERROR)	General purpose port	SPI Controller data output	-
A6	9	P14/SCLK_M (CHARGE)	General purpose port	SPI Controller clock output	-
-	10	AIN0	General-purpose port 0 (for AD input)	-	-
B6	11	AIN1	General-purpose port 1 (for current measurement)	-	-
-	12	MCSEL1	Capacitor selection signal (for impedance matching)	-	-
C6	13	MCSEL0	Capacitor selection signal (for impedance matching)	-	-
C4	14	VSS0	GND	-	-
D6	15	VDD_IO	Power supply for logic IO	-	-
C5	16	VPP	Power supply pin for test	-	-
E6	17	P13/AIN7 (BAT_CHG)	General purpose port	General-purpose port 7 for AD input	-
D5	18	P11/AIN6 (RFDET)	General purpose port	General-purpose port 6 for AD input	-
E5	19	P06/SCS_S (SCS_S)	General purpose port	SPI Peripheral chip select input	-
D4	20	P05/SDO_S (SDO_S)	General purpose port	SPI Peripheral data output	-
E4	21	P04/INT_S (INT_S)	General purpose port	Host IF INT output	-
D3	22	P01/SCL_S/SCLK_S (SCL_S / SCLK_S)	General purpose port	I2C Target clock input	SPI Peripheral clock input
E3	23	P00/SDA_S/SDI_S (SDA_S / SDI_S)	General purpose port	I2C Target data I/O	SPI Peripheral data input
E2	24	ISO_V	Power supply for logic IO (for Host IF)	-	-
E1	25	LDO1V5	Internal power supply (1.5V)	-	-
D1	26	LDO1V8	Internal power supply (1.8V)	-	-
C1	27	BAT2	Battery voltage monitor pin	-	-
B2	28	RX1	RF data receiving pin	-	-
B1	29	RX0	RF data receiving pin	-	-
A1	30	G_SHUNT	Shunt transistor control signal	-	-
-	31	P_ANT*4	Rectifier input voltage	-	-
A2	32	P10/RXD (BAT_SW)	General purpose port	UART data input	-
C3	-	VSS2	GND	-	-

*3 Function name assigned by firmware.
*4 If the package is WLCSP, connect to VDD_IO power supply.

■Pin Description

Notation Definition: Pin state in reset

Index	Notation	Description
In reset	L	“L” level output
	H	“H” level output
	PU	Pull-Up
	PD	Pull-Down
	Z	Floating state

Notation Definition: input/output direction

Index	Notation	Description
I/O	I	Input pin
	O	Output pin
	I/O	Bi-directional pin

●Power, GND, and reference voltage pins

PIN No. (WLCSP)	PIN NO. (WQFN)	Pin name	I/O	Pin description
C4	14	VSS0	-	GND
D6	15	VDD_IO	-	Power supply (for Logic IO)
C5	16	VPP	I	Power supply (for Test)
E2	24	ISO_V	-	Power supply (for Host IF)
E1	25	LDO1V5	-	Power supply for internal use (1.5V)
D1	26	LDO1V8	-	Power supply for internal use (1.8V)
C1	27	BAT2	I	Battery voltage monitor pin
-	31	P_ANT	-	Rectifier input voltage
C3	-	VSS2	-	GND

●Analog signal pin

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	I/O	Pin description
B2	28	RX1	I	Pins Connected to LSI internal circuits that demodulate communications.
B1	29	RX0	I	

●General purpose port terminal (VDD_IO system)

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	In reset	I/O	Active Level	Pin description
C2	1	TEST0	Z	I/O	L	Debug port
A3	2	P16 / AOUT	Z	I/O	-	General purpose port Analog monitor output
B3	3	P15 / TXD	Z	I/O	-	General purpose port UART data output
D2	4	RESET_N	PU	I	L	Reset Input Pin L：System reset mode H：Program operation mode
-	10	AIN0	Z	I	-	General-purpose port 0 (for AD input)
B6	11	AIN1	Z	I	-	General-purpose port 1 (for current measurement)
-	12	MCSEL1	PU	O	-	Capacitor selection signal (for impedance matching)
C6	13	MCSEL0	PU	O	-	Capacitor selection signal (for impedance matching)
E6	17	P13 / AIN7	Z	I/O	-	General purpose port General-purpose port 7 (for AD input)
A2	32	P10 / RXD	PU	I/O	-	General purpose port UART data input

●General purpose port terminal (ISO_V system) [*5]

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	In reset	I/O	Pin description
A4	5	P03 / SDA_M	Z	I/O	General purpose port I²C Controller data I/O
B4	6	P02 / SCL_M	Z	I/O	General purpose port I²C Controller Clock output
A5	7	P12 / SDI_M	Z	I/O	General purpose port SPI Controller Data input
B5	8	P17 / SDO_M	Z	I/O	General purpose port SPI Controller Data output
A6	9	P14 / SCLK_M	Z	I/O	General purpose port SPI Controller Clock output
D5	18	P11 / AIN6	Z	I/O	General purpose port General-purpose port 6 (for AD input)
E5	19	P06 / SCS_S	Z	I/O	General purpose port SPI Peripheral Chip Select input
D4	20	P05 / SDO_S	Z	I/O	General purpose port SPI Peripheral Data output
E4	21	P04 / INT_S	Z	I/O	General purpose port Host IF INT output
D3	22	P01 / SCL_S / SCLK_S	Z	I/O	General purpose port I²C Target Clock input SPI Peripheral Clock input
E3	23	P00 / SDA_S / SDI_S	Z	I/O	General purpose port I²C Target Data I/O SPI Peripheral Data input

●General-purpose port pins (P_ANT system)

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	In reset	I/O	Pin description
A1	30	G_SHUNT	L	O	Shunt transistor control signal

■Unused pin processing

Pin name	Pin processing
TEST0	Pull-Up
P00~P6、P10~P17 RESET_N AIN0 AIN1 MCSEL0 MCSEL1 G_SHUNT	Open

[*5] When controlled by an MCU or other device, the voltage should be the same as the interface voltage of the MCU.

■Electrical Characteristics

●Absolute Maximum Ratings

Index		Symbol	Condition	Rated value	Unit
Supply voltage	Power supply for logic IO	VDD_IO	-	-0.3～+6.5	V
	Power supply for logic IO (for Host IF)	ISO_V	-	-0.3～+6.5	V
	Rectifier input voltage	P_ANT	-	-0.3～+6.5	V
	Battery voltage monitor	BAT2	-	-0.3～+6.5	V
	Internal power supply	LDO1V5	-	-0.3～+2.0	V
		LDO1V8	-	-0.3～+6.5	V
Input voltage		VDIN	-	-0.3～VDD_IO+0.3	V
		$VDIN_{DIFF}$	RX0-RX1 (differential)	14	V
Input current		Ii	-	-10～+10	mA
		I_{P_ANT}	-	100	mA
Output voltage		VDO	-	-0.3～VDD_IO+0.3	V
Digital output current		IDO	-	-12～+20	mA
Power dissipation(WQFN)		PD	-	1	W
Power dissipation (CSP)		PD	-	0.5	W
Storage temperature		Tstg	-	-55～+150	°C

●Recommended Operating Conditions

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage range	VDD_IO	-	1.8	-	5.5	V
	ISO_V	-	1.8	-	5.5	V
	P_ANT	During communication	2.0	5.0	5.5	V
	P_ANT	During power transmission	-	-	5.5	V
Operating temperature	Ta	-	-40	+25	+85	°C
Antenna input frequency	F_{ANT}	-	Typ. -0.05%	13.56	Typ. +0.05%	MHz

●Flash Memory Operating Conditions

(VDD_IO=2.7 to 5.5V, P_ANT=2.7 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Range	Unit
Rewrite count	C_{EPD}	Data Flash	10,000	times

●RF Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage level	V_{RX1}	RX0/RX1	2.0	-	5.9	V
Input data amplitude	V_{RX2}	RX0/RX1	50	-	-	mV
Communication speed	F_{RX}	RX0/RX1	-	212	-	kbps
			-	424	-	kbps

●Notification Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
P_ANT limiter	V_{PANT1}	Normal	-	-	5.5	V
	V_{PANT2}	In case of abnormality notice	-	3.0	-	V

●AD Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	AD_{res}	-	-	10	-	bit
Zero-Scale Error	ZSE	-	-6	-	+6	LSB
Full-Scale Error	FSE	-	-6	-	+6	LSB

●AC Characteristics (I^2C Bus Interface)

- Standard Mode 100 kHz

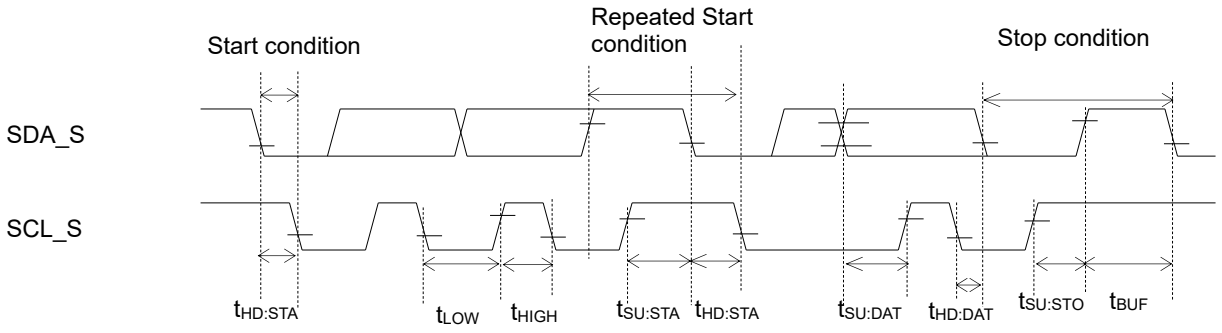
(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S	Clock frequency	f_{SCL}	-	-	-	100	kHz
	Hold time (start/repeated start condition)	$t_{HD:STA}$	-	4.0	-	-	µs
	"L" level time	t_{LOW}	-	4.7	-	-	µs
	"H" level time	t_{HIGH}	-	4.0	-	-	µs
	Setup time (start/repeated start condition)	$t_{SU:STA}$	-	4.7	-	-	µs
SDA_S	Hold time	$t_{HD:DAT}$	-	0	-	-	µs
	Setup time	$t_{SU:DAT}$	-	0.25	-	-	µs
	Setup time (Stop condition)	$t_{SU:STO}$	-	4.0	-	-	µs
Bus free time		t_{BUF}	-	4.7	-	-	µs

- Fast Mode 400 kHz

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S	Clock frequency	f_{SCL}	-	-	-	400	kHz
	Hold time (start/repeated start condition)	$t_{HD:STA}$	-	0.6	-	-	µs
	"L" level time	t_{LOW}	-	1.3	-	-	µs
	"H" level time	t_{HIGH}	-	0.6	-	-	µs
	Setup time (repeated start condition)	$t_{SU:STA}$	-	0.6	-	-	µs
SDA_S	Hold time	$t_{HD:DAT}$	-	0	-	-	µs
	Setup time	$t_{SU:DAT}$	-	0.1	-	-	µs
	Setup time (Stop condition)	$t_{SU:STO}$	-	0.6	-	-	µs
Bus free time		t_{BUF}	-	1.3	-	-	µs

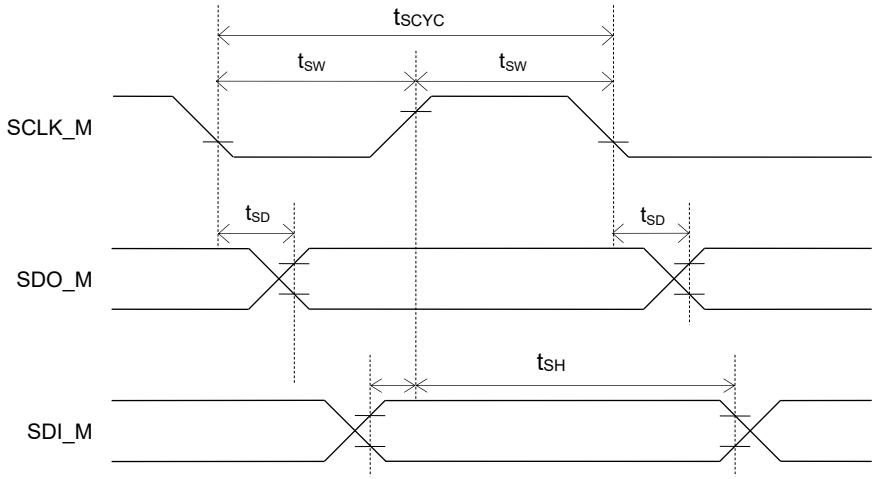


Note : If powering off this LSI, it disables communications of other devices on the I^2C bus
When power is not received from the P_ANT pin and there is a power input to the ISO_V pin of this LSI, the SDA_S/SCL_S pins maintain the Hi-Z state.

●AC Characteristics (Host Interface：SPI Controller)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85℃)

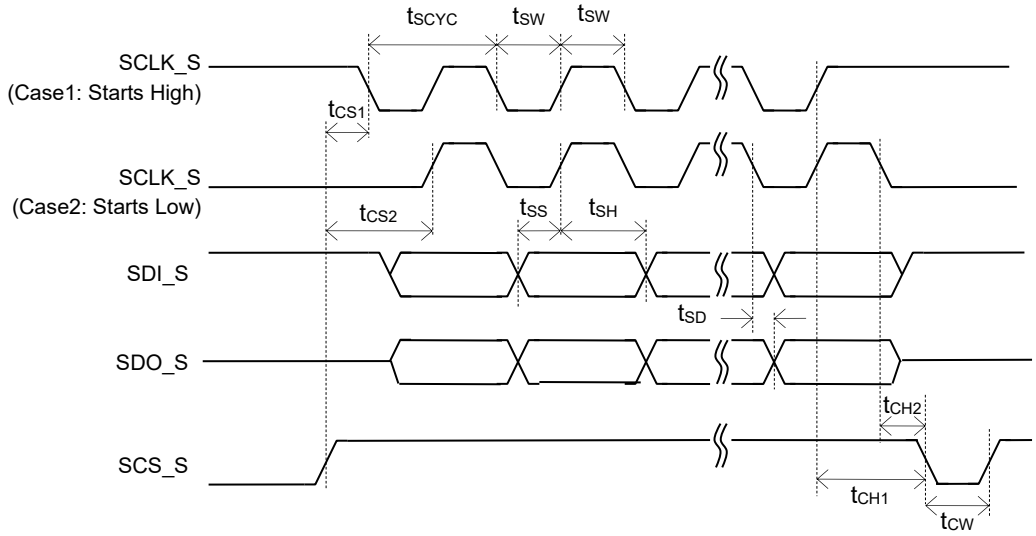
Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_M	Output cycle	t_{SCYC}	-	250	SCLK[*6]	-	ns
	Output pulse width	t_{SW}	-	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	ns
SDO_M	Output delay time	t_{SD}	-	-	-	100	ns
SDI_M	Input setup time	t_{SS}	-	100	-	-	ns
	Input hold time	t_{SH}	-	60	-	-	ns



●AC Characteristics (Host Interface：SPI Peripheral)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_S	Input cycle	t_{SCYC}	-	500	-	-	ns
	Input pulse width	t_{SW}	-	200	-	-	ns
SCS_S[*7]	Setup time	t_{CS1}	-	80	-	-	ns
		t_{CS2}	-	80	-	-	ns
	Hold time	t_{CH1}	-	80	-	-	ns
		t_{CH2}	-	80	-	-	ns
	Input pulse width	t_{CW}	-	80	-	-	ns
SDO_S	Output delay time	t_{SD}	-	-	-	240	ns
SDI_S	Input setup time	t_{SS}	-	80	-	-	ns
	Input hold time	t_{SH}	-	80	-	-	ns

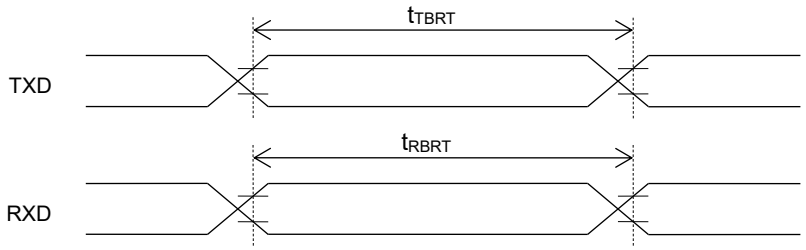


[*6] SCLK is configurable via register. See the ML7660/ML7661 Application Note for details.
[*7] SCS_S polarity (active-high or active-low) is switchable.
See the ML7660/ML7661 Application Note for details.

●AC Characteristics (UART)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

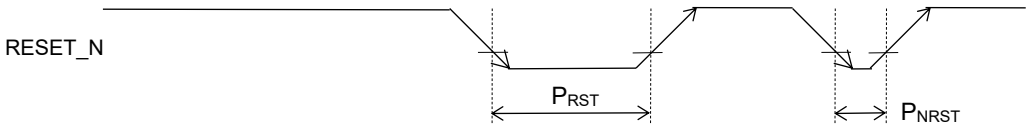
Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Tx Baud Rate	t_{TBRT}	-	-	-	115.2	kbps
Rx Baud Rate	t_{RBRT}	-	-	-	115.2	kbps



●AC Characteristics (Reset)

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Pulse Width	P_{RST}	-	2	-	-	ms
Non-reset Pulse Width	P_{NRST}	-	-	-	0.3	μs



●IO Characteristics

(Unless otherwise specified, VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.[*8]	Max.	Unit
Output voltage 1	VOH1	IOH=-1.0mA	VDD_IO -0.5	-	-	V
	VOL1	IOL=+0.5mA	-	-	0.4	V
Output voltage 2 (LED mode selected)	VOL2	2.7V≦V_{DD}≦5.5V IOL=+5.0mA	-	-	0.6	V
		IOL=+2.0mA	-	-	0.4	V
Output voltage 3 (I^2C mode selected)	VOL3	IOL3= +3mA (I^2C spec.) (VDD_IO ≥2V、ISO_V≥2V)	-	-	0.4	V
Output voltage 4 (I^2C mode selected)	VOL4	IOL4= +2mA (I^2C spec.) (VDD_IO <2V、ISO_V<2V)	-	-	VDD_IO ×0.2	V
Output leakage1	IOOH1	VOH=V_{DD} (at high impedance)	-	-	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	-	-	μA
Input current 1 (RESET_N)	IIH1	VIH1=V_{DD}	-	-	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	-	-	1	μA
	IIL2	VIL2=VSS	-200	-15	-1	μA
Input current 3	IIH3	VIH3=V_{DD} (when pull-down)	1	15	200	μA
	IIL3	VIL3=VSS (when pull-up)	-200	-15	-1	μA
	IIH3Z	VIH3=V_{DD} (at high impedance)	-	-	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	-	-	μA
Input voltage 1	VIH1	-	0.75× VDD_IO	-	VDD_IO	V
	VIL1	-	0	-	0.3× VDD_IO	V
Input pin capacitance	CIN	f=10kHz Vrms=50mV Ta=25°C	-	10	-	pF
Leak current	I_{ISOV}	Voltage supply to the ISO_V pin, no magnetic field input	-	100	-	nA

●Current Consumption

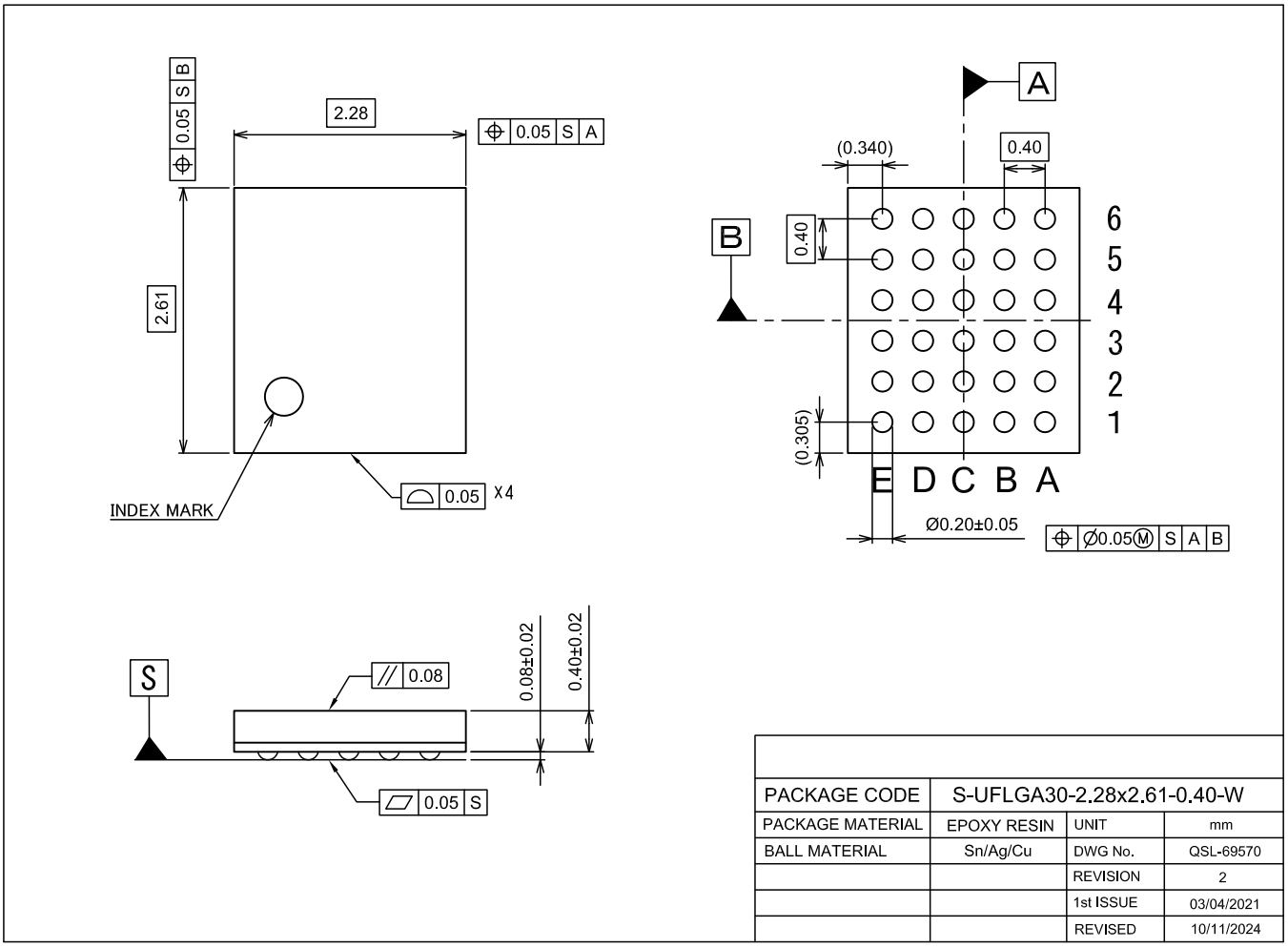
(VDD_IO=1.8 to 5.5V, P_ANT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption[*9]	P_ANT	During communication	0.5	-	-	mA
	P_ANT	During power transmission	-	-	10	mA

[*8] Typical values are listed for Ta=25°C and VDD_IO=3.0V.
[*9] Current consumption depends on the antenna design. The smaller the load resistance, the higher the current consumption. External transistor current is not included.

■Package Dimensions

●WLCSP 30pin

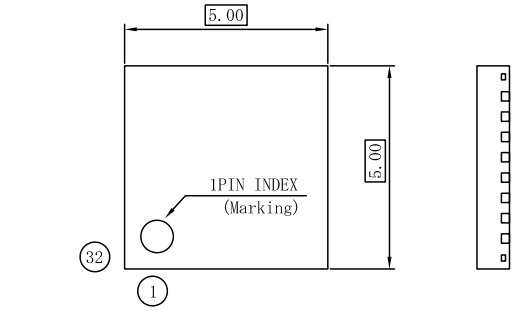


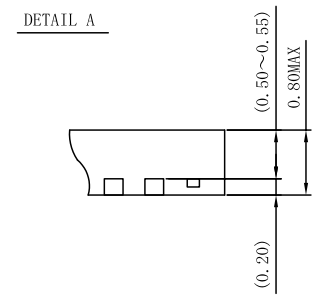
PACKAGE CODE	S-UFLGA30-2.28x2.61-0.40-W		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
BALL MATERIAL	Sn/Ag/Cu	DWG No.	QSL-69570
		REVISION	2
		1st ISSUE	03/04/2021
		REVISED	10/11/2024

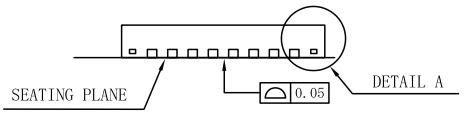
Notes for Mounting the Surface Mount Type Package

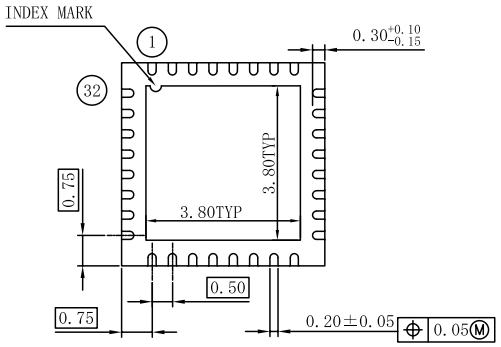
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

●WQFN 32pin









注）
1. 本寸法は、パッケージ反りを含む寸法である。
2. SEATING PLANEとは、パッケージを取り付ける面に対して、パッケージが接触し合う面である。

NOTE
1. THESE DIMENSIONS INCLUDE PACKAGE WARPAGE.
2. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

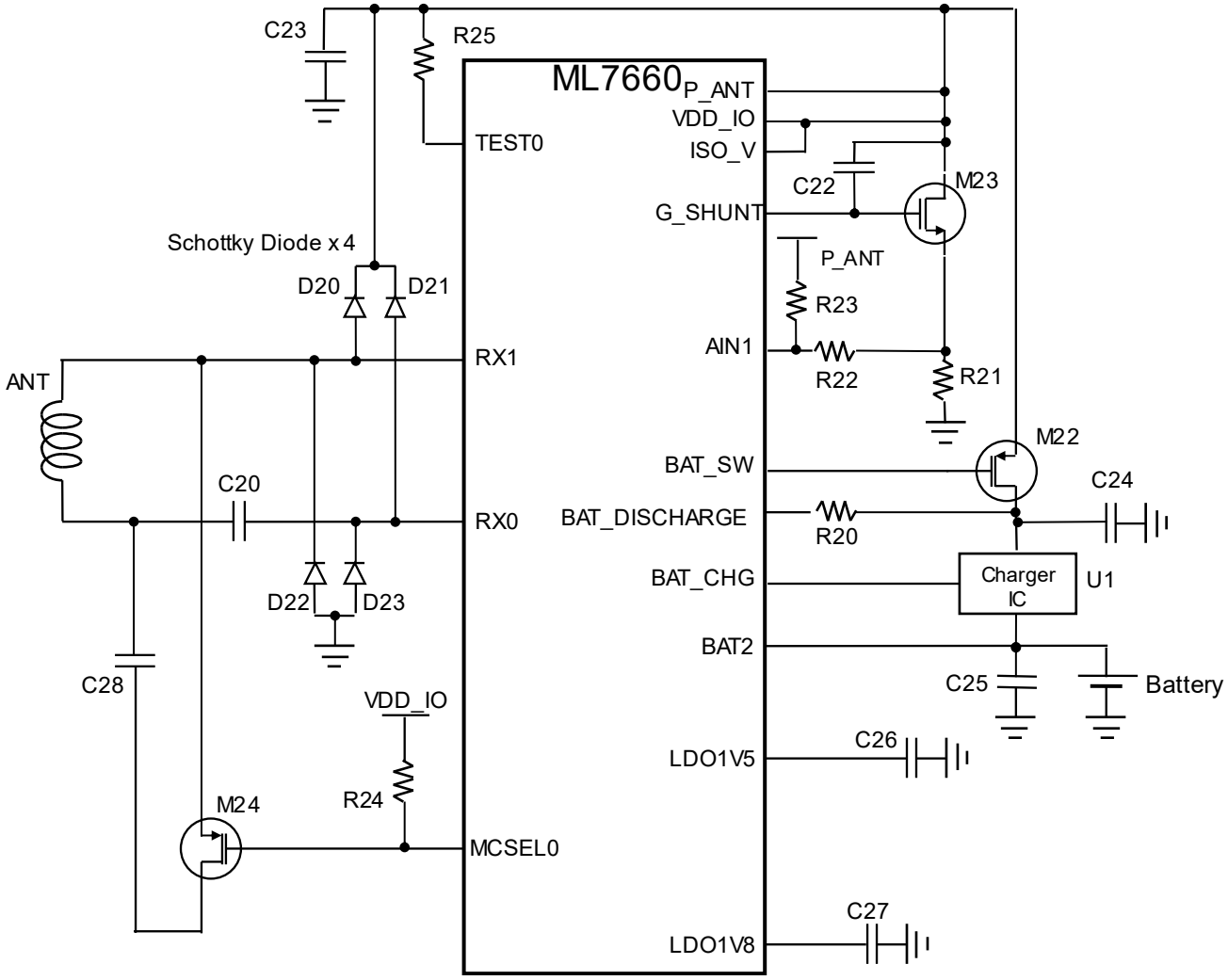
PACKAGE CODE	P-WQFN32-0505-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68630
LEAD FINISH	Ni/Pd/Au	REVISION	4
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/2/2011
PACKAGE MASS (g)	0.055TYP.	REVISED	May/10/2024

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■Application Circuit Example

Please refer to the ML7660 / ML7661 Application Note for details.



■Revision History

Document No.	Issue Date	Page		Change Contents
		Previous Edition	Current Edition	
FEDL7660-01	2021.10.5	-	-	First edition
FEDL7660-02	2022.12.28	P.1-15	P.1-15	Correction of errors.
		P.10	P.10	Correction of Flash operating temperature upper / lower limit, and oscillator frequency range.
		P.18	P.18	Added optional notation to C21, R24, M20
FEDL7660-03	2023.3.10	P.1-15	P.1-13	Removed description of serial interface, and general port.
		P.18	P.16	Removed C12, R2, M3
FEDL7660-04	2023.6.7	P.1-16	P.1-14	Correction of errors.
		P.1-2	P.1	Modified of features.
		P.4-7	P.3-6	Modified of pin names and descriptions.
		P.16	P.14	Added R25.
FEDL7660-05	2023.12.15	P.1	P.1	Added product name and applications.
FEDL7660-06	2024.1.10	P.16	P.16	Modified notes.
FEDL7660-07	2024.1.26	P.1	P.1	Added product name.
FEDL7660-08	-	-	-	Blank
FEDL7660-09	2025.2.14	P.1-15	P.1-15	Full review and company name change Modified: ■Overview Correction of errors. Modified: ■Features Additional product name revision Added: ■Related Documents Added: ●Product name Latest code number added. Modified: ■Block diagram Modified pin names Modified: ■Pin assignment Modified pin names Added: ■Pin list Modified: ■Pin description PIN No. added, General purpose port classification updated. ■Pin Description updated ●General-purpose port pins (ISO_V) ●General-purpose port pins (VDD_IO) Added: ■Electrical characteristics AD characteristics, SPI controller characteristics Modified: ■Package dimension Company name deleted. Modified: Modified “Caution”. Modified: ■Application circuit example modified (M24 added, R24 added, C28 added, RX1/RX0 replaced)

Document No.	Issue Date	Page		Change Contents
		Previous Edition	Current Edition	
FEDL7660-10	2025.8.18	P.2	P.2	Modified: ●Product name 1. Revision of product lineup 2. Add a note for Batteryless for Reference Design (REF67011)
		P.11	P.11	Added: t_{SCYC} MIN. value Added: SCS_S polarity is register-selectable.
FEDL7660-11	2026.1.30	P.12	P.12	Added: AC Characteristics (UART) Added: AC Characteristics (Reset)
		P.14	P.14	Delete: Note for the package with exposed die pad

Notice

Precaution on using ROHM Products

1) When using ROHM Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings[*1], recommended operating conditions, etc.) are within the ranges specified. ROHM disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of ROHM Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of ROHM Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
   *1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. ROHM disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third party with respect to ROHM Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples, etc.). Therefore, ROHM shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) ROHM intends our Products to be used in a way indicated in this document. Please be sure to contact a ROHM sales office if you consider the use of our Products in different way from original use indicated in this document. For use of our Products in medical systems, please be sure to contact a ROHM representative and must obtain written agreement. Do not use our Products in applications which may directly cause injuries to human life, and which require extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc. ROHM disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us without our prior written consent.

6) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

7) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

8) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or ROHM's Products.

9) This document, in part or in whole, may not be reprinted or reproduced without prior consent of ROHM.

(Note) “ROHM” as used in this document means ROHM Co., Ltd.

Other Precaution

1) All information contained in this document is subject to change for the purpose of improvement, etc. without any prior notice. Before purchasing or using ROHM Products, please confirm the latest information with a ROHM sales office.

2) ROHM has used reasonable care to ensure the accuracy of the information contained in this document, however, ROHM shall have no responsibility for any damages, expenses or losses arising from inaccuracy or errors of such information.