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OKI Semiconductor

FEDL86410-01
Issue Date: Jun. 05, 2007

ML86410

MPEG4 Encoding LSI

OVERVIEW

The ML86410 is an LSI that encodes YUV (YCbCr) format digital video signals into MPEG-4-ASP format ones in real time.
The LSI achieves high picture quality by a unique high-speed high-quality motion search method and a unique coding rate control method. For video input, the LSI supports progressive video output from camera modules and interlaced video output from NTSC/PAL digital video decoders.

FEATURES

Image encoding:

– Encoding format
  · MPEG-4 Simple Profile@Level 3
  · MPEG-4 Advanced Simple Profile@Level 5
– Supported image
  · Progressive QVGA, 30 fps
  · Progressive VGA, 30 fps
  · Interlaced NTSC, 29.97 fps
  · Interlaced PAL, 25 fps

– Output frame (with a frame skipping function)
  · QVGA/ VGA : 30/15/1/0.5 fps
  · NTSC : 29.97/14.985/0.999/0.4995 fps
  · PAL : 25/12.5/1/0.5 fps

– Coding type
  · IIII
  · IPPP···

– Encoding mode
  · CBR (Up to 6 Mbps)
  · VBR

– Supports interlaced images (NTSC/PAL)
– Unique high-speed high-quality motion search method
– Unique coding rate control method
– 4MV motion estimation
– Detectes abnormality such as:
  · Camera input abnormality
  · Stream data readout abnormality
  · Set bit rate exceeded
– Can suspend/restart encoding

Video interface:

– QVGA (320 × 240 pixels) / VGA (640 × 480 pixels) : YCbCr (8-bit (YCbCr) (4:2:2)) + sync, 27 MHz
YUV (8-bit (YUV)(4:2:2)) + sync, 27 MHz
– NTSC (720 × 480 pixels)) / PAL (720 × 576 pixels) : ITU-R BT.656, 27 MHz

Note:
Although signals are input in 4:2:2 format, they are converted to 4:2:0 format before encoding processing.

– Can choose the order in which fields are loaded during interlacing (Top first/Bottom first)
– Can choose between the positive polarity and the negative polarity of CLKCAM when loading YUVDATA, VSYNC, or HSYNC
– Clipping can be specified as no clipping or clipping in the range of 16≤Y,U,V≤240
– For the interface, a 3.3 V I/O interface is used.

Host CPU interface:

– General-purpose 8-/16-bit data bus (can be connected directly with Oki's ARM microcontroller series)
– Operable as an I/O device in DMA mode from the host CPU

External SDRAM interface:

– 32-bit data bus, 2 MWords × 32 bits, 81 MHz (equivalent to PC133)
– Automatic initialization sequence
– Column address: 8/9/10 bits selectable

Input clock:

– System clock : 27 MHz
– Video interface : 27 MHz

Power management:

– No power management function is provided

Power supply voltage:

– Core section : 1.35 to 1.65 V
– I/O section : 3.0 to 3.6 V
– PLL section : 1.35 to 1.65 V

Operating frequency:

– Internal : 81 MHz
– Video interface section : 27 MHz

Operating temperature (ambient temperature):

– -20 to +85°C

Package:

– 144-pin plastic LQFP (LQFP144-P-2020-0.50-ZK)

BLOCK DIAGRAM

Figure 1-1 shows the block diagram of the ML86410.

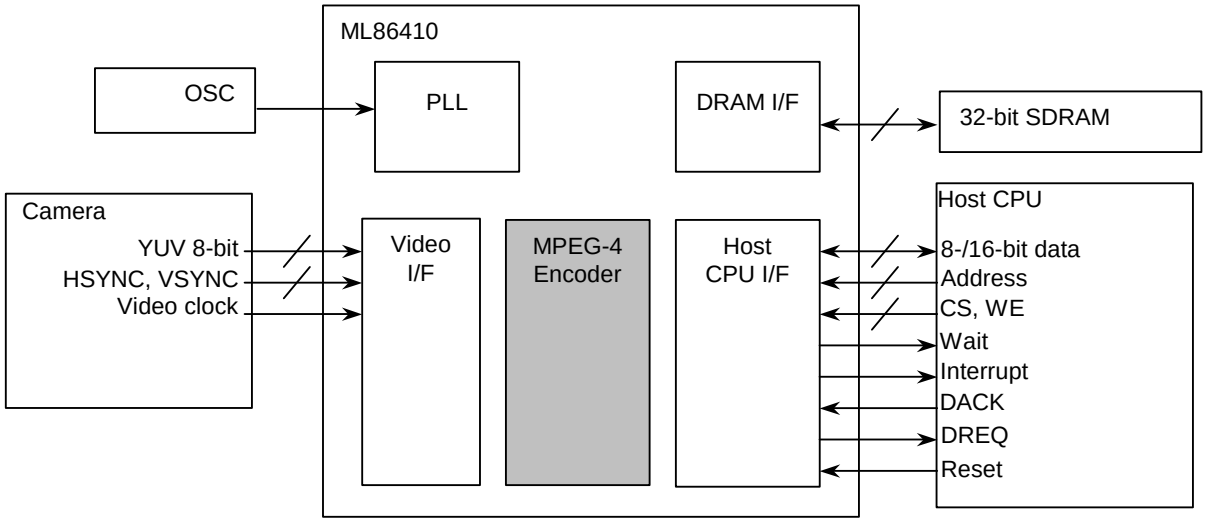


Figure 1 Block Diagram

PIN CONFIGURATION

Figure 1-2 shows the pin configuration of the 144-pin LQFP.

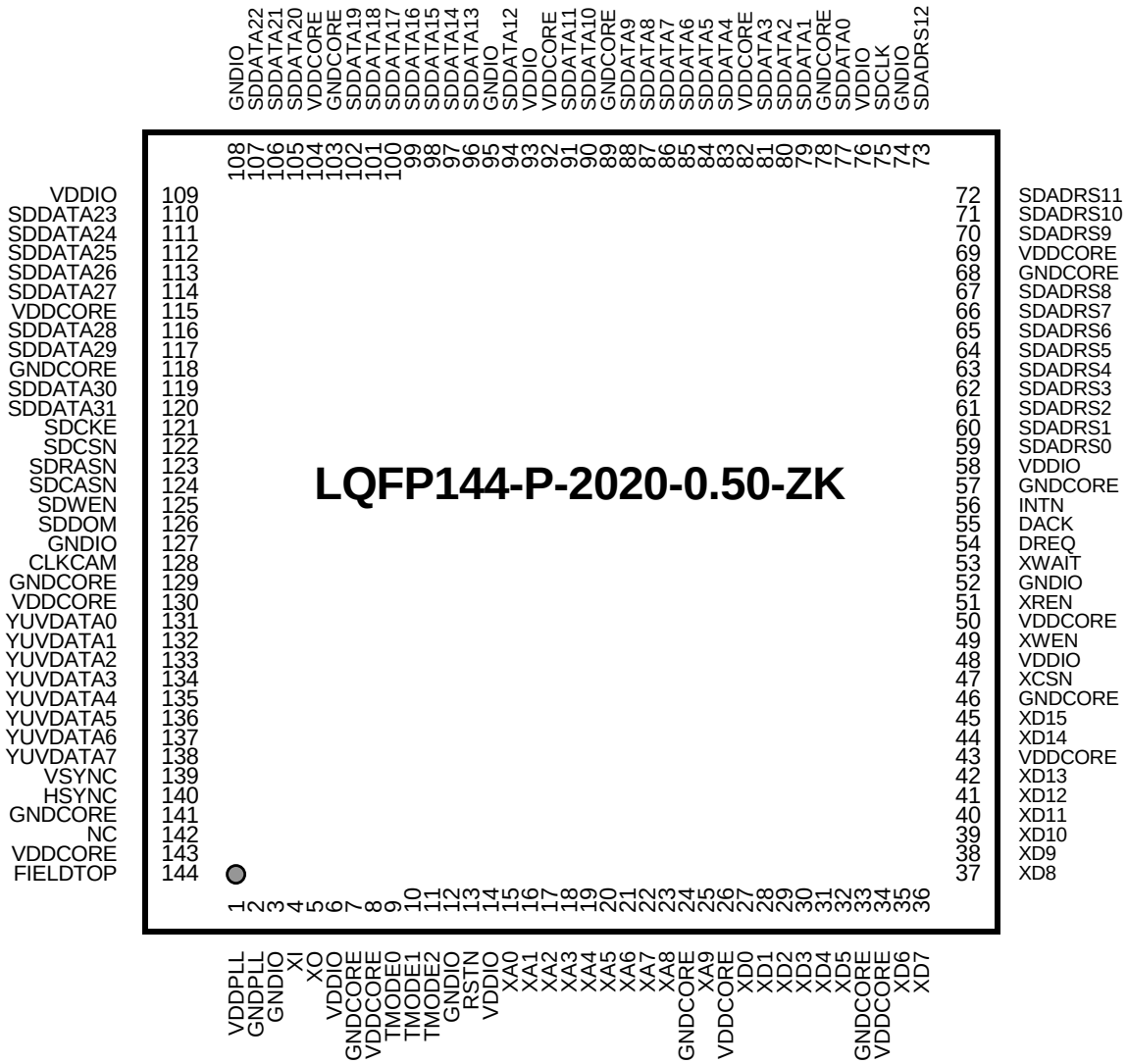


Figure 2 144-Pin LQFP Pin Configuration

LIST OF PINS

Pin No.	Symbol	I/O	Description
1	VDDPLL	VDD	PLL power supply
2	GNDPLL	GND	PLL GND
3	GNDIO	GND	I/O GND
4	XI	—	Input clock (27 MHz)
5	XO	—	Input clock (27 MHz)
6	VDDIO	VDD	I/O power supply
7	GNDCORE	GND	Core GND
8	VDDCORE	VDD	Core power supply
9	TMODE0	I	Test mode 0
10	TMODE1	I	Test mode 1
11	TMODE2	I	Test mode 2
12	GNDIO	GND	I/O GND
13	RSTN	I	Reset
14	VDDIO	VDD	I/O power supply
15	XA0	I	External bus address input signal 0
16	XA1	I	External bus address input signal 1
17	XA2	I	External bus address input signal 2
18	XA3	I	External bus address input signal 3
19	XA4	I	External bus address input signal 4
20	XA5	I	External bus address input signal 5
21	XA6	I	External bus address input signal 6
22	XA7	I	External bus address input signal 7
23	XA8	I	External bus address input signal 8
24	GNDCORE	GND	Core GND
25	XA9	I	External bus address input signal 9
26	VDDCORE	VDD	Core power supply
27	XD0	I/O	External bus input/output data 0
28	XD1	I/O	External bus input/output data 1
29	XD2	I/O	External bus input/output data 2
30	XD3	I/O	External bus input/output data 3
31	XD4	I/O	External bus input/output data 4
32	XD5	I/O	External bus input/output data 5
33	GNDCORE	GND	Core GND
34	VDDCORE	VDD	Core power supply
35	XD6	I/O	External bus input/output data 6
36	XD7	I/O	External bus input/output data 7
37	XD8	I/O	External bus input/output data 8
38	XD9	I/O	External bus input/output data 9
39	XD10	I/O	External bus input/output data 10
40	XD11	I/O	External bus input/output data 11
41	XD12	I/O	External bus input/output data 12
42	XD13	I/O	External bus input/output data 13
43	VDDCORE	VDD	Core power supply
44	XD14	I/O	External bus input/output data 14
45	XD15	I/O	External bus input/output data 15
46	GNDCORE	GND	Core GND
47	XCSN	I	Chip enable signal

Pin No.	Symbol	I/O	Description
48	VDDIO	VDD	I/O power supply
49	XWEN	I	Write enable signal
50	VDDCORE	VDD	Core power supply
51	XREN	I	Read enable signal
52	GNDIO	GND	I/O GND
53	XWAIT	O	Wait signal
54	DREQ	O	DMA request
55	DACK	I	DMA acknowledge
56	INTN	O	Interrupt signal output
57	GNDCORE	GND	Core GND
58	VDDIO	VDD	I/O power supply
59	SDADRS0	O	SDRAM address 0
60	SDADRS1	O	SDRAM address 1
61	SDADRS2	O	SDRAM address 2
62	SDADRS3	O	SDRAM address 3
63	SDADRS4	O	SDRAM address 4
64	SDADRS5	O	SDRAM address 5
65	SDADRS6	O	SDRAM address 6
66	SDADRS7	O	SDRAM address 7
67	SDADRS8	O	SDRAM address 8
68	GNDCORE	GND	Core GND
69	VDDCORE	VDD	Core power supply
70	SDADRS9	O	SDRAM address 9
71	SDADRS10	O	SDRAM address 10
72	SDADRS11	O	SDRAM address 11
73	SDADRS12	O	SDRAM address 12
74	GNDIO	GND	I/O GND
75	SDCLK	O	SDRAM clock
76	VDDIO	VDD	I/O power supply
77	SDDATA0	I/O	SDRAM data 0
78	GNDCORE	GND	Core GND
79	SDDATA1	I/O	SDRAM data 1
80	SDDATA2	I/O	SDRAM data 2
81	SDDATA3	I/O	SDRAM data 3
82	VDDCORE	VDD	Core power supply
83	SDDATA4	I/O	SDRAM data 4
84	SDDATA5	I/O	SDRAM data 5
85	SDDATA6	I/O	SDRAM data 6
86	SDDATA7	I/O	SDRAM data 7
87	SDDATA8	I/O	SDRAM data 8
88	SDDATA9	I/O	SDRAM data 9
89	GNDCORE	GND	Core GND
90	SDDATA10	I/O	SDRAM data 10
91	SDDATA11	I/O	SDRAM data 11
92	VDDCORE	VDD	Core power supply
93	VDDIO	VDD	I/O power supply
94	SDDATA12	I/O	SDRAM data 12
95	GNDIO	GND	I/O GND
96	SDDATA13	I/O	SDRAM data 13
97	SDDATA14	I/O	SDRAM data 14

Pin No.	Symbol	I/O	Description
98	SDDATA15	I/O	SDRAM data 15
99	SDDATA16	I/O	SDRAM data 16
100	SDDATA17	I/O	SDRAM data 17
101	SDDATA18	I/O	SDRAM data 18
102	SDDATA19	I/O	SDRAM data 19
103	GNDCORE	GND	Core GND
104	VDDCORE	VDD	Core power supply
105	SDDATA20	I/O	SDRAM data 20
106	SDDATA21	I/O	SDRAM data 21
107	SDDATA22	I/O	SDRAM data 22
108	GNDIO	GND	I/O GND
109	VDDIO	VDD	I/O power supply
110	SDDATA23	I/O	SDRAM data 23
111	SDDATA24	I/O	SDRAM data 24
112	SDDATA25	I/O	SDRAM data 25
113	SDDATA26	I/O	SDRAM data 26
114	SDDATA27	I/O	SDRAM data 27
115	VDDCORE	VDD	Core power supply
116	SDDATA28	I/O	SDRAM data 28
117	SDDATA29	I/O	SDRAM data 29
118	GNDCORE	GND	Core GND
119	SDDATA30	I/O	SDRAM data 30
120	SDDATA31	I/O	SDRAM data 31
121	SDCKE	O	SDRAM CKE pin control (Clock Enable)
122	SDCSN	O	SDRAM CS pin control (Chip Select)
123	SDRASN	O	SDRAM RAS pin control (Row Address Strobe)
124	SDCASN	O	SDRAM CAS pin control (Column Address Strobe)
125	SDWEN	O	SDRAM WE pin control (Write Enable)
126	SDDQM	O	SDRAM DQM pin control (DQ Mask)
127	GNDIO	GND	I/O GND
128	CLKCAM	I	Pixel clock
129	GNDCORE	GND	Core GND
130	VDDCORE	VDD	Core power supply
131	YUVDATA0	I	YUV data input 0
132	YUVDATA1	I	YUV data input 1
133	YUVDATA2	I	YUV data input 2
134	YUVDATA3	I	YUV data input 3
135	YUVDATA4	I	YUV data input 4
136	YUVDATA5	I	YUV data input 5
137	YUVDATA6	I	YUV data input 6
138	YUVDATA7	I	YUV data input 7
139	VSYNC	I	Vertical sync signal
140	HSYNC	I	Horizontal sync signal
141	GNDCORE	GND	Core GND
142	NC	I	Unused pin
143	VDDCORE	VDD	Core power supply
144	FIELDTOP	I	Field signal

PIN DESCRIPTION

Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
SDRAM interface (52 pins)							
75	SDCLK	out	SDRAM clock	Low	—		6 mA
59	SDADRS0	out	SDRAM address 0	Low	—		4 mA
60	SDADRS1	out	SDRAM address 1	Low	—		4 mA
61	SDADRS2	out	SDRAM address 2	Low	—		4 mA
62	SDADRS3	out	SDRAM address 3	Low	—		4 mA
63	SDADRS4	out	SDRAM address 4	Low	—		4 mA
64	SDADRS5	out	SDRAM address 5	Low	—		4 mA
65	SDADRS6	out	SDRAM address 6	Low	—		4 mA
66	SDADRS7	out	SDRAM address 7	Low	—		4 mA
67	SDADRS8	out	SDRAM address 8	Low	—		4 mA
70	SDADRS9	out	SDRAM address 9	Low	—		4 mA
71	SDADRS10	out	SDRAM address 10	Low	—		4 mA
72	SDADRS11	out	SDRAM address 11	Low	—		4 mA
73	SDADRS12	out	SDRAM address 12	Low	—		4 mA
77	SDDATA0	in/out	SDRAM data 0	Hi-Z	—	Pull-down	4 mA
79	SDDATA1	in/out	SDRAM data 1	Hi-Z	—	Pull-down	4 mA
80	SDDATA2	in/out	SDRAM data 2	Hi-Z	—	Pull-down	4 mA
81	SDDATA3	in/out	SDRAM data 3	Hi-Z	—	Pull-down	4 mA
83	SDDATA4	in/out	SDRAM data 4	Hi-Z	—	Pull-down	4 mA
84	SDDATA5	in/out	SDRAM data 5	Hi-Z	—	Pull-down	4 mA
85	SDDATA6	in/out	SDRAM data 6	Hi-Z	—	Pull-down	4 mA
86	SDDATA7	in/out	SDRAM data 7	Hi-Z	—	Pull-down	4 mA
87	SDDATA8	in/out	SDRAM data 8	Hi-Z	—	Pull-down	4 mA
88	SDDATA9	in/out	SDRAM data 9	Hi-Z	—	Pull-down	4 mA
90	SDDATA10	in/out	SDRAM data 10	Hi-Z	—	Pull-down	4 mA
91	SDDATA11	in/out	SDRAM data 11	Hi-Z	—	Pull-down	4 mA
94	SDDATA12	in/out	SDRAM data 12	Hi-Z	—	Pull-down	4 mA
96	SDDATA13	in/out	SDRAM data 13	Hi-Z	—	Pull-down	4 mA
97	SDDATA14	in/out	SDRAM data 14	Hi-Z	—	Pull-down	4 mA
98	SDDATA15	in/out	SDRAM data 15	Hi-Z	—	Pull-down	4 mA
99	SDDATA16	in/out	SDRAM data 16	Hi-Z	—	Pull-down	4 mA
100	SDDATA17	in/out	SDRAM data 17	Hi-Z	—	Pull-down	4 mA
101	SDDATA18	in/out	SDRAM data 18	Hi-Z	—	Pull-down	4 mA
102	SDDATA19	in/out	SDRAM data 19	Hi-Z	—	Pull-down	4 mA
105	SDDATA20	in/out	SDRAM data 20	Hi-Z	—	Pull-down	4 mA
106	SDDATA21	in/out	SDRAM data 21	Hi-Z	—	Pull-down	4 mA
107	SDDATA22	in/out	SDRAM data 22	Hi-Z	—	Pull-down	4 mA
110	SDDATA23	in/out	SDRAM data 23	Hi-Z	—	Pull-down	4 mA
111	SDDATA24	in/out	SDRAM data 24	Hi-Z	—	Pull-down	4 mA
112	SDDATA25	in/out	SDRAM data 25	Hi-Z	—	Pull-down	4 mA
113	SDDATA26	in/out	SDRAM data 26	Hi-Z	—	Pull-down	4 mA
114	SDDATA27	in/out	SDRAM data 27	Hi-Z	—	Pull-down	4 mA
116	SDDATA28	in/out	SDRAM data 28	Hi-Z	—	Pull-down	4 mA
117	SDDATA29	in/out	SDRAM data 29	Hi-Z	—	Pull-down	4 mA

Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
119	SDDATA30	in/out	SDRAM data 30	Hi-Z	—	Pull-down	4 mA
120	SDDATA31	in/out	SDRAM data 31	Hi-Z	—	Pull-down	4 mA
121	SDCKE	out	SDRAM CKE pin control (Clock Enable)	High	High		4 mA
122	SDCSN	out	SDRAM CS pin control (Chip Select)	High	Low		4 mA
123	SDRASN	out	SDRAM RAS pin control (Row Address Strobe)	High	Low		4 mA
124	SDCASN	out	SDRAM CAS pin control (Column Address Strobe)	High	Low		4 mA
125	SDWEN	out	SDRAM WE pin control (Write Enable)	High	Low		4 mA
126	SDDQM	out	SDRAM DQM pin control (DQ Mask)	High	High		4 mA
Video interface (12 pins)							
131	YUVDATA0	in	YUV data input 0	—	High		—
132	YUVDATA1	in	YUV data input 1	—	High		—
133	YUVDATA2	in	YUV data input 2	—	High		—
134	YUVDATA3	in	YUV data input 3	—	High		—
135	YUVDATA4	in	YUV data input 4	—	High		—
136	YUVDATA5	in	YUV data input 5	—	High		—
137	YUVDATA6	in	YUV data input 6	—	High		—
138	YUVDATA7	in	YUV data input 7	—	High		—
139	VSYNC	in	Vertical sync signal	—	High		—
140	HSYNC	in	Horizontal sync signal	—	High		—
144	FIELDTOP	in	Field signal by interlacing 0 : Bottom Field 1 : Top Field	—	High		—
128	CLKCAM	in	Pixel clock	—	High	Schmitt	—
Host CPU interface (33 pins)							
15	XA0	in	External bus address output signal 0	—	—		—
16	XA1	in	External bus address output signal 1	—	—		—
17	XA2	in	External bus address output signal 2	—	—		—
18	XA3	in	External bus address output signal 3	—	—		—
19	XA4	in	External bus address output signal 4	—	—		—
20	XA5	in	External bus address output signal 5	—	—		—
21	XA6	in	External bus address output signal 6	—	—		—
22	XA7	in	External bus address output signal 7	—	—		—
23	XA8	in	External bus address output signal 8	—	—		—

Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
25	XA9	in	External bus address output signal 9	—	—		—
27	XD0	in/out	External bus input/output data 0	Hi-Z	—		4 mA
28	XD1	in/out	External bus input/output data 1	Hi-Z	—		4 mA
29	XD2	in/out	External bus input/output data 2	Hi-Z	—		4 mA
30	XD3	in/out	External bus input/output data 3	Hi-Z	—		4 mA
31	XD4	in/out	External bus input/output data 4	Hi-Z	—		4 mA
32	XD5	in/out	External bus input/output data 5	Hi-Z	—		4 mA
35	XD6	in/out	External bus input/output data 6	Hi-Z	—		4 mA
36	XD7	in/out	External bus input/output data 7	Hi-Z	—		4 mA
37	XD8	in/out	External bus input/output data 8	Hi-Z	—		4 mA
38	XD9	in/out	External bus input/output data 9	Hi-Z	—		4 mA
39	XD10	in/out	External bus input/output data 10	Hi-Z	—		4 mA
40	XD11	in/out	External bus input/output data 11	Hi-Z	—		4 mA
41	XD12	in/out	External bus input/output data 12	Hi-Z	—		4 mA
42	XD13	in/out	External bus input/output data 13	Hi-Z	—		4 mA
44	XD14	in/out	External bus input/output data 14	Hi-Z	—		4 mA
45	XD15	in/out	External bus input/output data 15	Hi-Z	—		4 mA
47	XCSN	in	Chip enable signal	—	Low		—
49	XWEN	in	Write enable signal	—	Low		—
51	XREN	in	Read enable signal	—	Low		—
53	XWAIT	out	Wait signal	Low	High		4 mA
54	DREQ	out	DMA request 0/1= no request / request	Low	High		4 mA
55	DACK	in	DMA acknowledge 0/1= no clear / clear Connect this pin to GND when performing program transfer using the DMA signal control register.	—	High	Pull-down	—
56	INTN	out	Interrupt signal output	High	Low		2 mA

Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
Clock/Reset (3 pins)							
13	RSTN	in	Reset 0: active	—	Low	Schmitt, pull-up	—
4	XI	—	Input clock (27 MHz)	—	—		—
5	XO	—	Input clock (27 MHz)	—	—		—
Test mode related (3 pins)							
9	TMODE0	in	Test mode signal 0	—	—	Schmitt, pull-down	—
10	TMODE1	in	Test mode signal 1	—	—	Schmitt, pull-down	—
11	TNODE2	in	Test mode signal 2	—	—	Schmitt, pull-down	—
Unused signal (1 pin)							
142	NC	in	Unused pin Connect this pin to GND.	—	—		—
Power supply/GND (40 pins)							
6,14,48, 58,76,93, 109	VDDIO	in	Digital power supply (I/O)	—	—		—
3,12, 52, 74, 95, 108, 127	GNDIO	in	Digital GND (I/O)	—	—		—
8, 26, 34, 43, 50, 69, 82, 92, 104,115, 130, 143	VDDCORE	in	Digital power supply (CORE)	—	—		—
7, 24, 33, 46, 57, 68, 78, 89, 103, 118, 129, 141	GNDCORE	in	Digital GND (CORE)	—	—		—
1	VDDPLL	in	Analog (PLL) power supply	—	—		—
2	GNDPLL	in	Analog (PLL) GND	—	—		—

ABSOLUTE MAXIMUM RATINGS

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage (CORE)	V_{DDCORE}	– (*1)	–0.3 to +2.0	V
Digital power supply voltage (I/O)	V_{DDIO}	– (*1)	–0.3 to +4.6	
PLL power supply voltage	V_{DDPLL}	– (*1)	–0.3 to +2.0	
Input voltage (normal buffer)	V_I	– (*1)	–0.3 to V_{DDIO}+0.3	
Output voltage (normal buffer)	V_O	– (*1)	–0.3 to V_{DDIO}+0.3	
Allowable input current	I_I	– (*1)	–10 to +10	mA
Allowable output current (2 mA buffer)	I_O	– (*1)	–8 to +8	
Allowable output current (4 mA buffer)			–16 to +16	
Allowable output current (6 mA buffer)			–24 to +24	
Power dissipation	P_D	Ta = 85°C	1450	mW
Storage temperature	T_{STG}	—	–50 to +150	°C

*1: The GND pins are at 0 V when Ta = 25°C

RECOMMENDED OPERATING CONDITIONS

Table 2 Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply voltage (CORE)	V_{DDCORE}	$V_{DDIO} \geq V_{DDCORE}$	1.35	1.5	1.65	V
Digital power supply voltage (I/O)	V_{DDIO}		3.0	3.3	3.6	
PLL power supply voltage	V_{DDPLL}		1.35	1.5	1.65	
Operating frequency	f_{OP}		—	—	81	MHz
Ambient temperature	Ta	—	-20	25	85	°C

DC CHARACTERISTICS

Table 3 DC Characteristics

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input "H" voltage (normal pins)	V_{IH1}	Applied to normal pins	2.0	—	V_{DDIO}+0.3	V
Input "L" voltage (normal pins)	V_{IL1}	Applied to normal pins	–0.3	—	0.8	
TTL level Schmitt trigger input threshold voltage	V_{T+}	—	—	—	2.1	
	V_{T-}	—	0.7	—	—	
	ΔV_T	V_{T+} — V_{T-}	0.25	—	—	
Output "H" voltage	V_{OH1}	V_{DDIO} = 3.0 to 3.6 V Applied to normal pins	2.4	—	—	
Output "L" voltage	V_{OL1}	V_{DDIO} = 3.0 to 3.6 V Applied to normal pins	—	—	0.4	
Input leakage current 1	I_{IL1}	V_I = 0V / V_{DDIO} Applied to normal pins	–10	—	10	μA
Input leakage current 2	I_{IL2}	VI = 0 V Applied to pins pulled up with 50 kΩ	–200	—	-10	
Input leakage current 3	I_{IL3}	VI = V_{DDIO} Applied to pins pulled down with 50 kΩ	10	—	200	
Input pin capacitance	C_I	—	—	5	—	pF
Output pin capacitance	C_O	—	—	5	—	
Input/output pin capacitance	C_{IO}	—	—	5	—	
Chip power consumption (operating)	P_{Total}	V_{DDCORE} = 1.5 V, V_{DDIO} = 3.3 V, Ta = 25°C	—	250	—	mW
IO supply current (operating)	I_{DDOIO}		—	30	—	mA
Core and PLL supply current (operating)	$I_{DDOCore}$		—	100	—	mA
IO Supply current (standby)	I_{DDSIO}	V_{DDCORE} = 1.5 V, V_{DDIO} = 3.3 V, Ta = 25°C	—	1	—	uA
Core and PLL Supply current (standby)	I_{DDCore}		—	2	—	mA

AC CHARACTERISTICS

Reset Timing

Table 4 Reset Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset pulse width	t_{RSTW}	—	11	—	—	ms

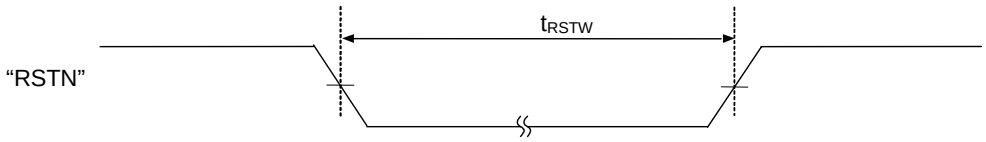


Figure 3 Reset Timing

Clock Timing (XI, XO)

Table 5 Clock Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock (CLK) frequency	f_{CLK}	—	—	27.0	—	MHz
Clock (CLK) cycle	t_{CLK}	—	—	$1/f_{CLK}$	—	s

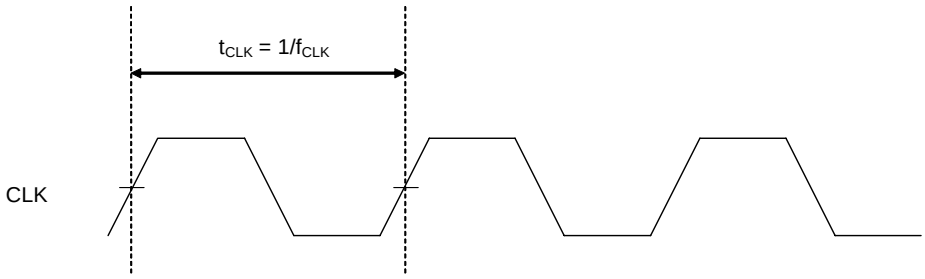


Figure 4 Clock Timing

External SDRAM Timing

Table 6 External SDRAM Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

SDRAM							
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
SDCLK cycle	t_{SDC}	CL = 20 pF	—	t_{CLK} / 3	—	ns	(81 MHz)
CS output delay time	t_{SDCSD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
DQM output delay time	t_{SDDQMD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
RAS output delay time	t_{SDRASD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
CAS output delay time	t_{SDRASD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
WE output delay time	t_{SDWED}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDADRS[12:0] output delay time	t_{SDXAD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDDATA[31:0] output delay time	t_{SDXDOD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDDATA[31:0] output hold time	t_{SDXDOH}		$0.5t_{SDC}$ – 3.0	—	—		
SDDATA[31:0] output enable time	t_{SDXDOE}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDDATA[31:0] output disable time	$t_{SDXDODE}$		$0.5t_{SDC}$ – 3.0	—	—		
SDDATA[31:0] input setup time	t_{SDXDIS}		2	—	—		
SDDATA[31:0] input hold time	t_{SDXDIH}		4.5	—	—		
Minimum delay time, RAS to CAS	t_{SDRCD}	—	n_{SD1} x t_{SDC}	—	—		n_{SD1} = tRCD=2
RAS active time	t_{SDRAS}		n_{SD2} x t_{SDC}	—	—		n_{SD2} = tRAS=5
RAS precharge time	t_{SDRP}		n_{SD3} x t_{SDC}	—	—		n_{SD3}= tRP=2

Note : t_{CLK} =1/ f_{CLK} (f_{CLK}=27MHz)

External SDRAM Read Timing (32-bit bus width SDRAM word access)

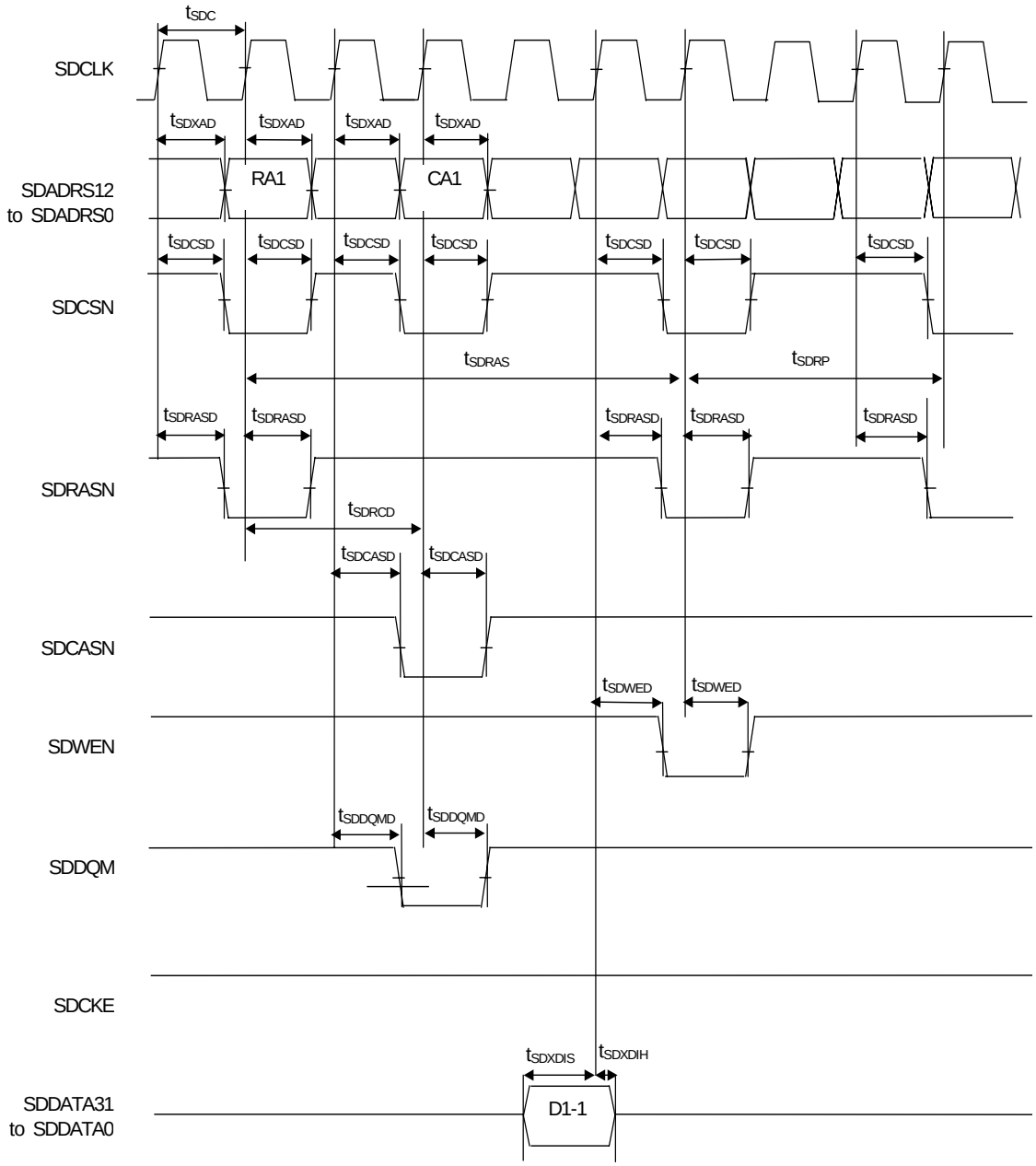


Figure 5 External SDRAM Read Timing

External SDRAM Write Timing (32-bit bus width SDRAM byte/half-word access)

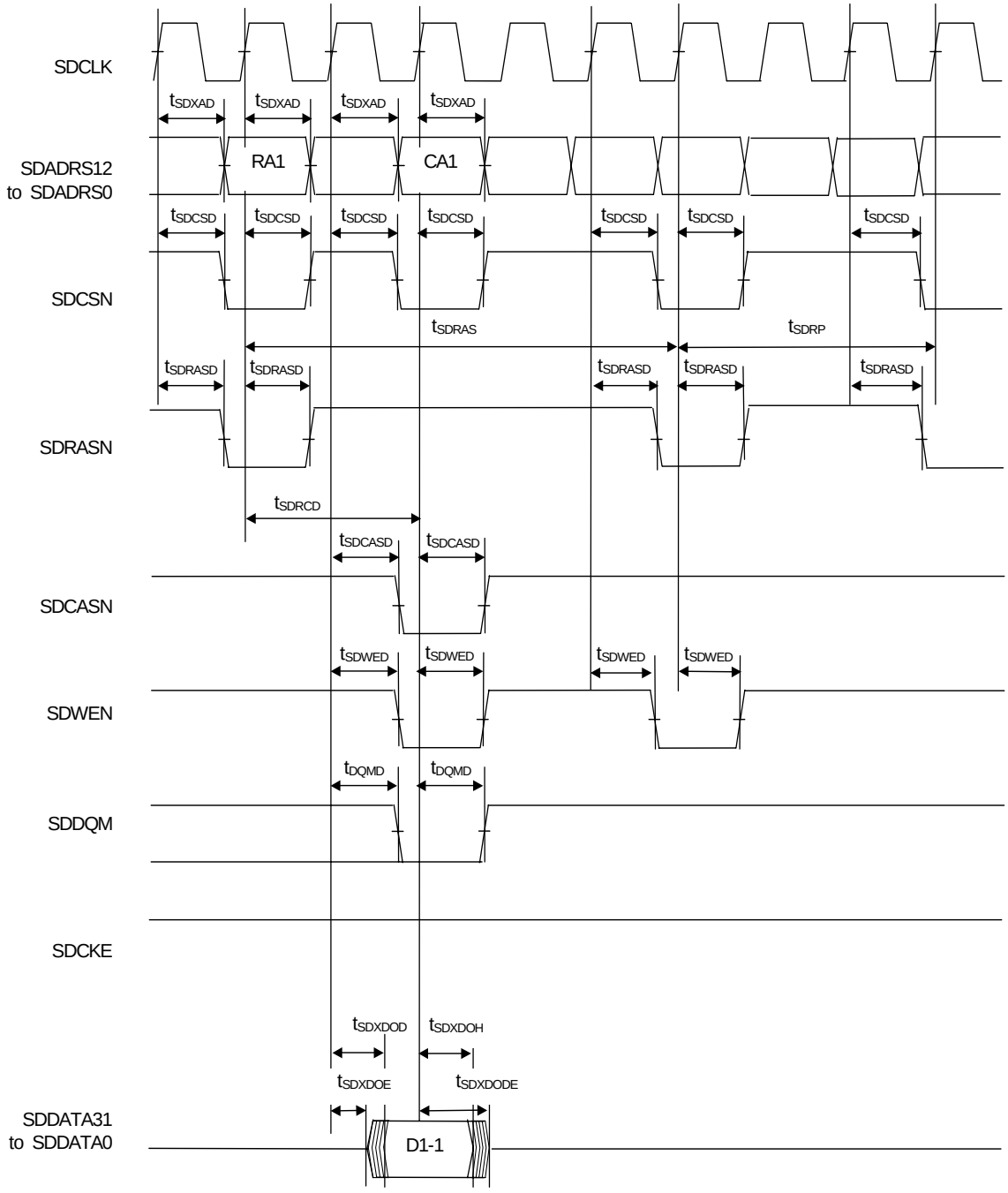


Figure 6 External SDRAM Write Timing

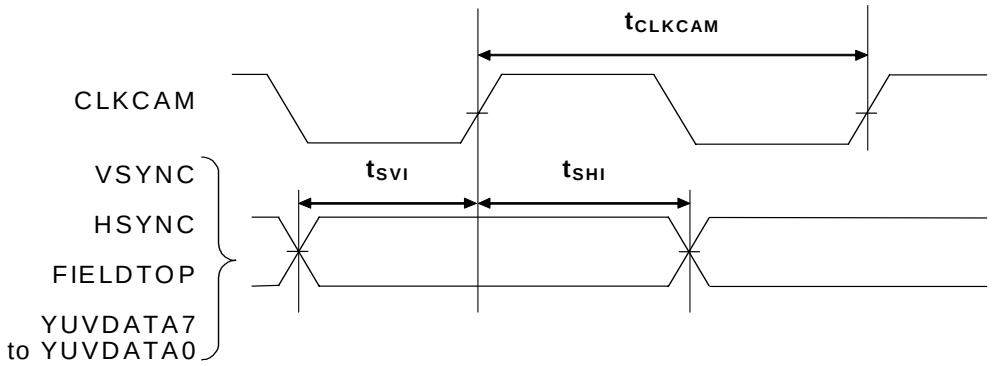
Video Interface Timing

Table 7 Video Interface Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
CLKCAM frequency	f_{CLKCAM}	CL = 20 pF	—	27	—	MHz	
CLKCAM cycle	t_{CLKCAM}		—	$1/f_{CLKCAM}$	—	s	
CLKCAM input setup time	t_{SVI}		10	—	—	ns	
CLKCAM input hold time	t_{HVI}		5	—	—		

Capture clock edge setting: Positive



Capture clock edge setting: Negative

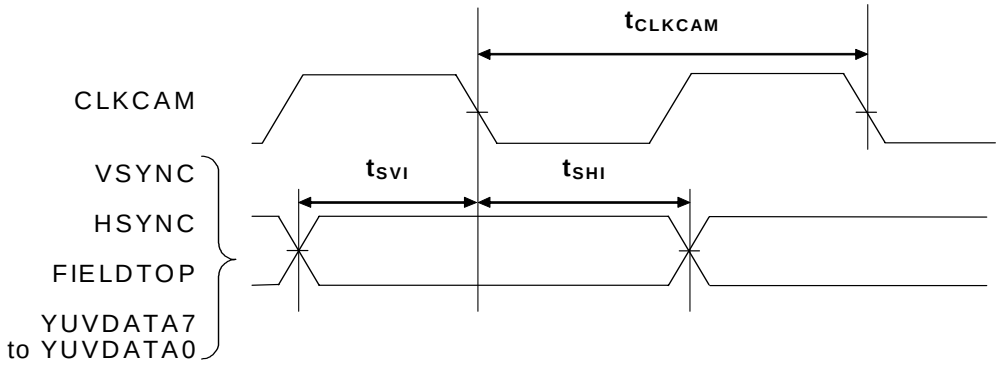


Figure 7 Video Interface Timing

Host CPU Interface Timing

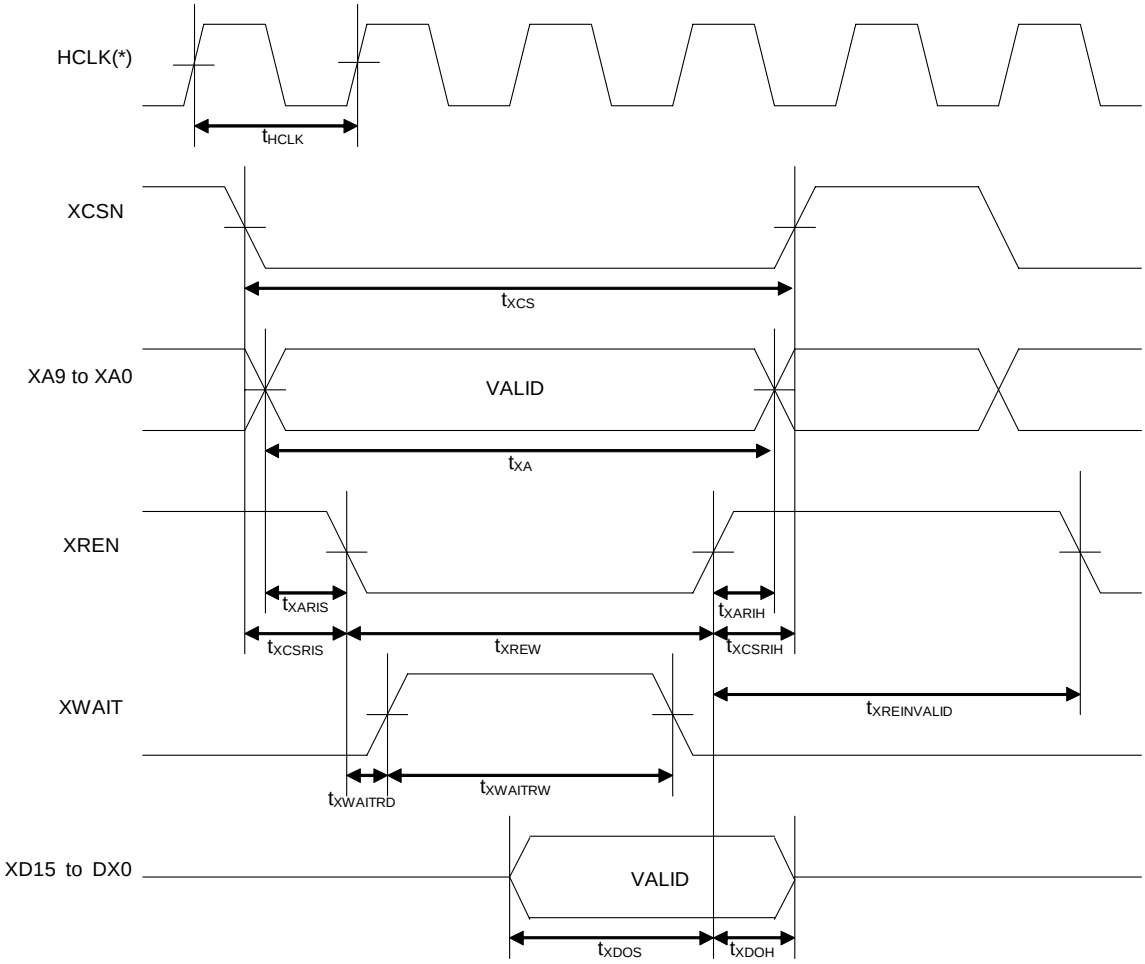
Table 8 Host CPU Interface Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
System clock period	t_{HCLK}	—	—	t_{CLK} / 3	—	ns	The signal internal to the LSI (81 MHz)
XCSN access time	t_{XCS}	CL = 40 pF	$5t_{HCLK}$ + 5.0	—	—	ns	
XA access time	t_{XA}		$5t_{HCLK}$ + 5.0	—	—		
XREN access time	t_{XREW}		$t_{XWAITRD}$ + $t_{XWAITRW}$ + 5.0	—	—		
XREN input setup time 1	t_{XCSRIS}		5.0	—	—		
XREN input setup time 2	t_{XARIS}		5.0	—	—		
XREN input hold time 1	t_{XCSRIH}		5.0	—	—		
XREN input hold time 2	t_{XARIH}		5.0	—	—		
XREN invalid time	$t_{XREINVALID}$		$2t_{HCLK}$ + 5.0	—	—		
XWEN access time	t_{XWEW}		$t_{XWAITWD}$ + $t_{XWAITWW}$ + 5.0	—	—		
XWEN input setup time 1	t_{XCSWIS}		5.0	—	—		
XWEN input setup time 2	t_{XAWIS}		5.0	—	—		
XWEN input hold time 1	t_{XCSWIH}		5.0	—	—		
XWEN input hold time 2	t_{XAWIH}		5.0	—	—		
XWEN invalid time	$t_{XWEINVALID}$		$2t_{HCLK}$ + 5.0	—	—		
XWAIT output delay time (read access)	$t_{XWAITRD}$		0.0	—	10.0		
XWAIT output delay time (write access)	$t_{XWAITWD}$		0.0	—	10.0		
XWAIT output time (read access)	$t_{XWAITRW}$		$4t_{HCLK}$	—	$7t_{HCLK}$		
XWAIT output time (write access)	$t_{XWAITWW}$		$4t_{HCLK}$	—	$7t_{HCLK}$		
XD output setup time	t_{XDOS}		t_{HCLK} – 2.0	—	—		
XD output hold time	t_{XDOH}		1.5	—	10.0		
XD input setup time	t_{XDIS}		5.0	—	—		
XD input hold time	t_{XDIH}		5.0	—	t_{HCLK}		

Note : t_{CLK} =1/ f_{CLK} (f_{CLK}=27MHz)

Read Cycle (Read Access from Host CPU to ML86410)



* The signal internal to the LSI

Figure 8 Host CPU Interface Timing (Read Cycle)

Write Cycle (Write Cycle from Host CPU to ML86410)

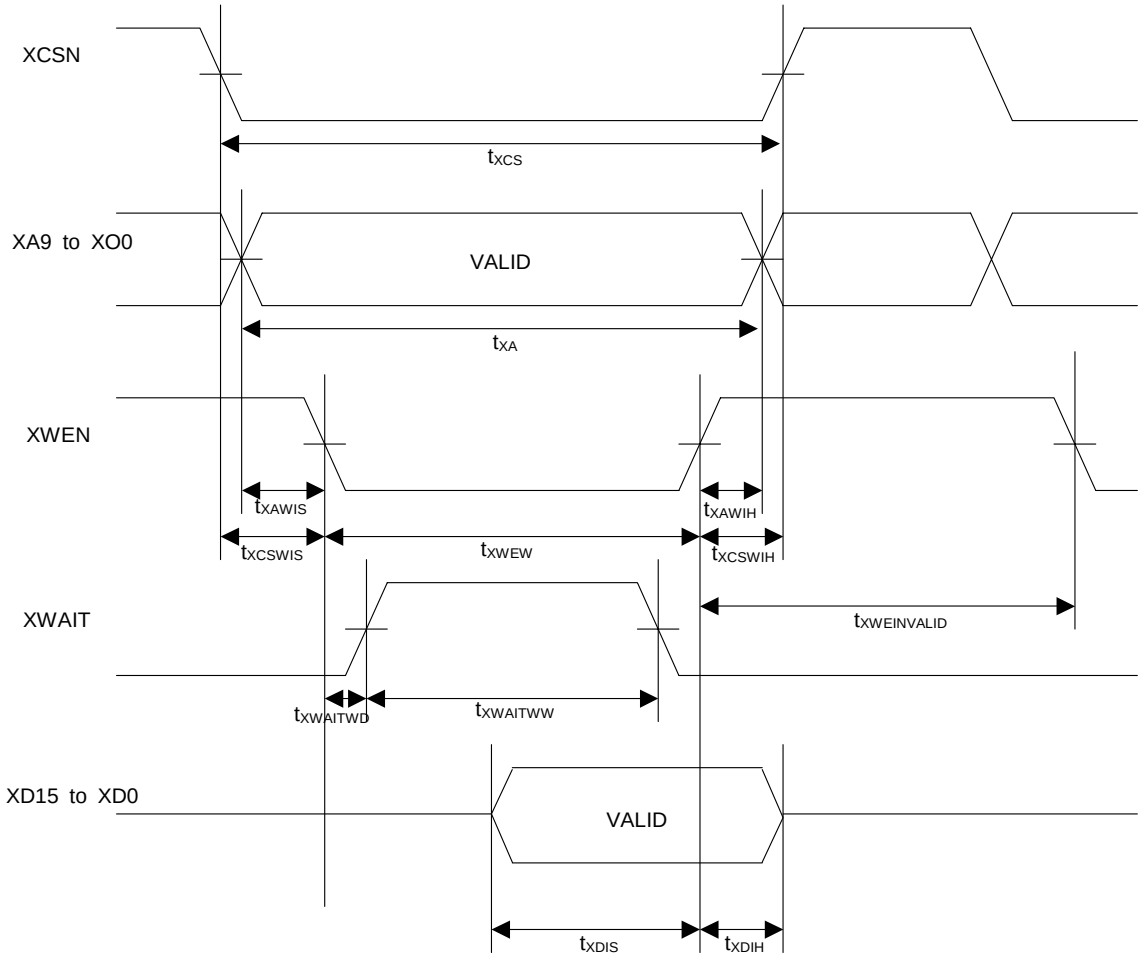


Figure 9 Host CPU Interface Timing (Write Cycle)

DMA Signal Timing

Table 9 DMA Signal Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
System clock period	t_{HCLK}	—	—	t_{CLK} / 3	—	ns	The signal internal to the LSI (81 MHz)
DREQ positive period	$t_{DREQPOS}$	CL=20pF	$4t_{HCLK}$	-	-	ns	
DREQ negative period	$t_{DREQNEG}$	CL=20pF	$3t_{HCLK}$	-	-	ns	
DREQ deassert delay	t_{DREQDD}	CL=20pF	$3t_{HCLK}$	-	$5t_{HCLK}$	ns	This maximum value is a value when DACK is asserted after the DMA read access by this LSI is completed. When DACK is asserted before the access is completed, the DREQ deassert delay increases.
DREQ assert delay	t_{DREQAD}	CL=20pF	$3t_{HCLK}$	-	-	ns	
DACK positive period	$t_{DACKPOS}$	CL=20pF	$3t_{HCLK}$	-	-	ns	
DACK negative period	$t_{DACKNEG}$	CL=20pF	$3t_{HCLK}$	-	-	ns	
DACK deassert delay	t_{DACKDD}	CL=20pF	$0t_{HCLK}$	-	-	ns	
DACK assert delay	t_{DACKAD}	CL=20pF	$0t_{HCLK}$	-	-	ns	

Note : $t_{CLK} = 1/ f_{CLK}$ (f_{CLK}=27MHz)

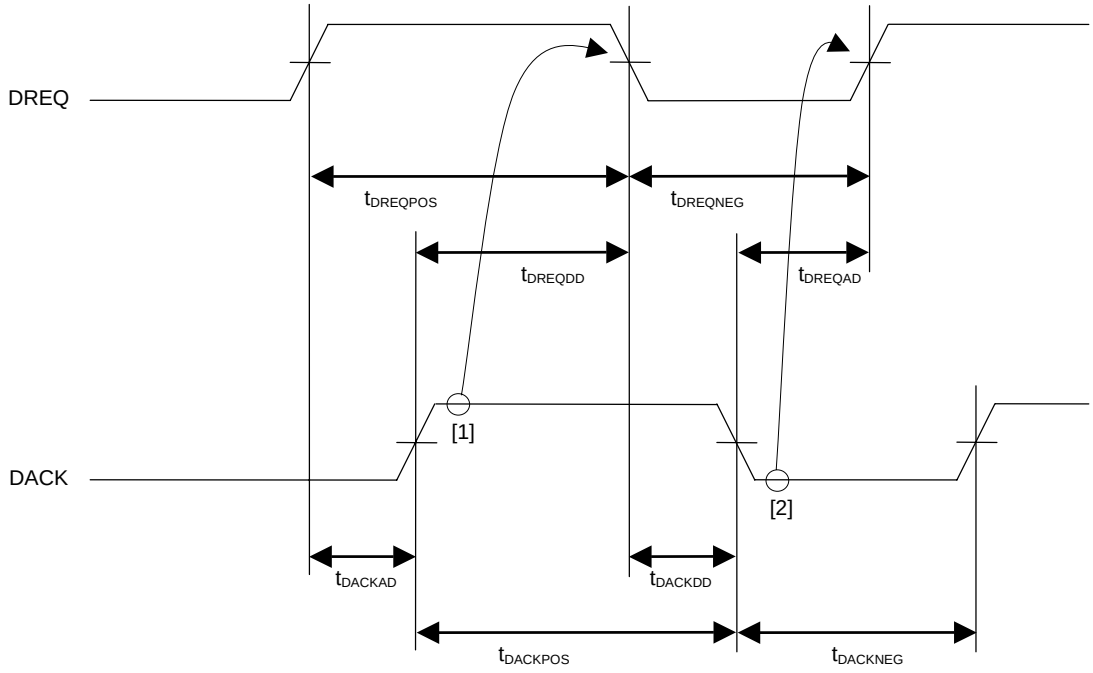


Figure 10 DMA Signal Timing

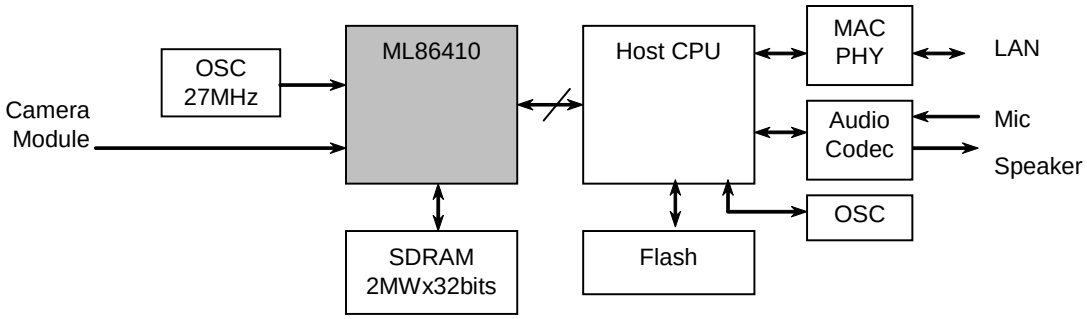
[1]: After the data transfer, the sample does DACK to this LSI. If DACK is high-level, DREQ is deasserted. It is waited to become high-level if it is a low-level.
This LSI operates recognizing the signal level of DACK.

[2]:After the DREQ is deasserted , this LSI waits for DACK to become a low-level.
When the DACK is low-level , the next stream data is transmitted.

Note: In the AC characteristics timing diagrams shown in this section, the intervals are measured at the 1/2 V_{DDIO} on the input and output waveforms.

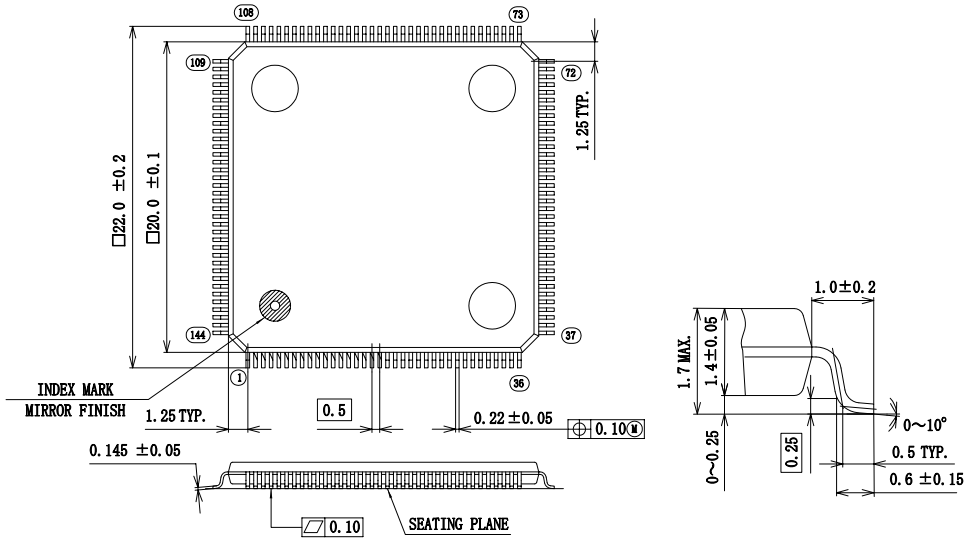
APPLICATION EXAMPLE

Ethernet Camera System



PACKAGE DIMENSIONS

LQFP144-P-2020-0.50-ZK



Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn / 1 to 3Bi
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.29 TYP.
Rev. No./Last Revised	3/Nov. 15, 2004

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL86410-01	OCT.27,2006	–	–	Preliminary edition 1 (This edition is not official.)
PEDL86410-16	Dec.20,2006	–	–	Preliminary edition 16 (Same as Japanese 16th edition)
FEDL86410-01	Jun.05,2007	– 1	– 1	Final edition 1 Changed into "IPPP·····" from "IPPP" of the coding type in 1.1 Features.

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