Preliminary

OKI Semiconductor

This version: Jun. 1999

ML9203-xx

5 × 7 Dot Character × 16-Digit × 2-Line Display Controller/Driver with Character RAM

GENERAL DESCRIPTION

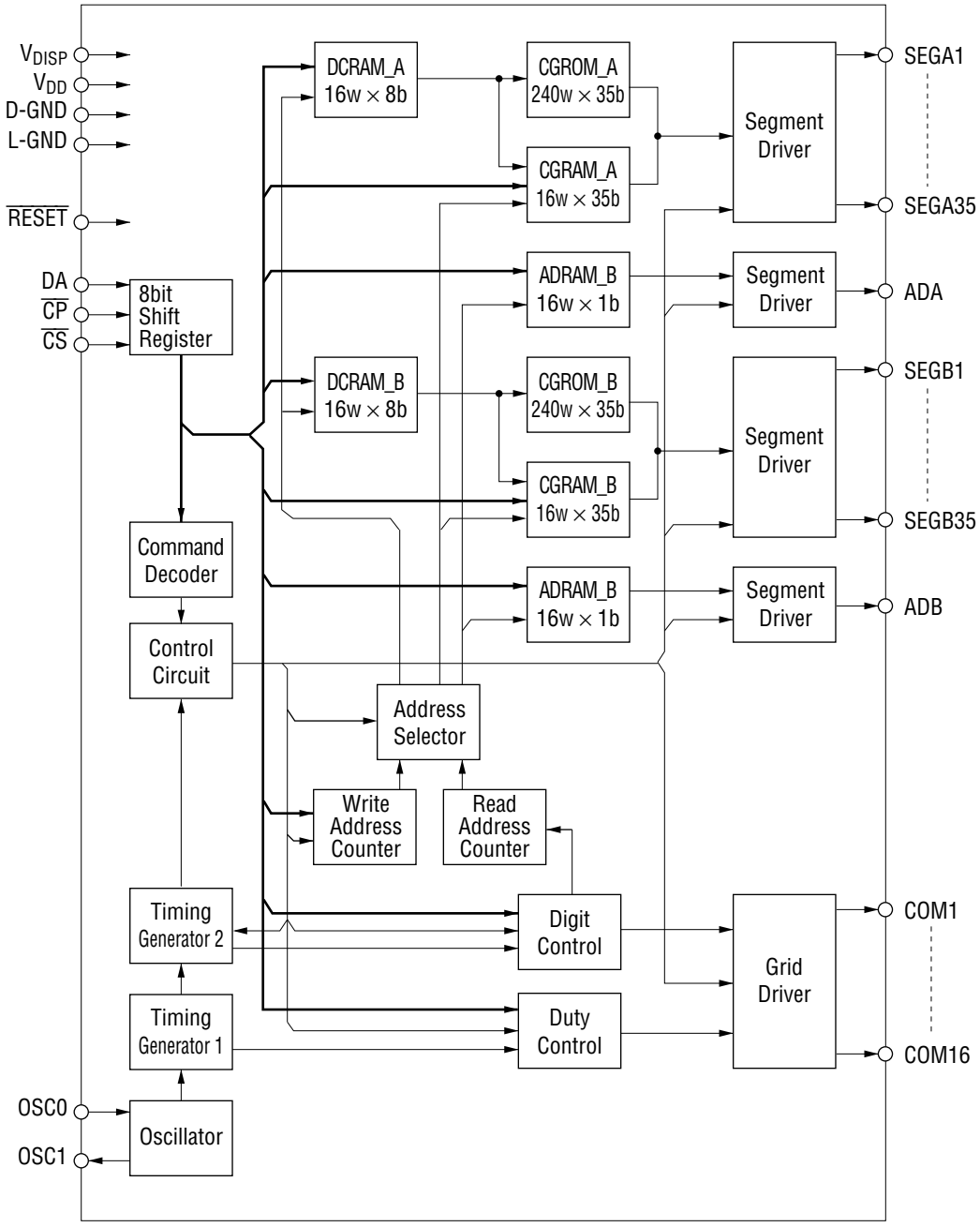
The ML9203-xx is a 5 × 7 dot matrix type vacuum fluorescent display tube controller driver IC which displays characters, numerics and symbols of a maximum of 16 digits × 2 lines.
Dot matrix vacuum fluorescent display tube drive signals are generated by serial data sent from a micro-controller. A display system is easily realized by internal ROM and RAM for character display.
The ML9203-xx has low power consumption since it is made by CMOS process technology.
-01 is available as a general-purpose code.
Custom codes are provided on customer's request.

FEATURES

- Logic power supply (V_{DD}) : 3.3 V±10% or 5.0 V±10%
- VFD tube drive power supply (V_{DISP}) : 20 to 60 V
- VFD driver output current
  (VFD driver output can be connected directly to the VFD tube. No pull-down resistor is required.)
  - Segment driver (SEGA1 to A35, SEGB1 to B35)
    Only one driver output is high : –5 mA (V_{DISP}=60V)
    All the driver outputs are high : –350 mA (V_{DISP}=60V)
  - Segment driver (ADA, ADB) : –20 mA (V_{DISP}=60V)
  - Grid driver (COM1 to 16) : –50 mA (V_{DISP}=60V)
- Content of display
  SEGA1 to SEGA35 and ADA
  - CGROM_A 5×7 dots : 240 types (character data)
  - CGRAM_A 5×7 dots : 16 types (character data)
  - ADRAM_A 16 (display digit) × 1 bit (symbol data; can be used for a cursor.)
  - DCRAM_A 16 (display digit) × 8 bits (register for character data display)

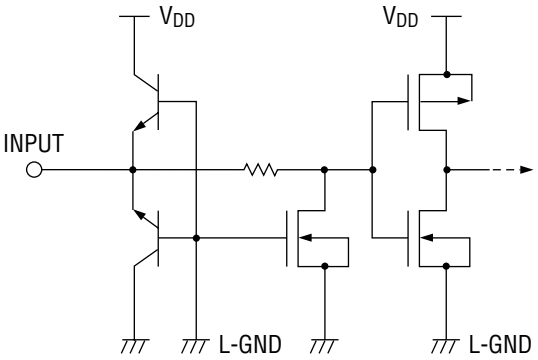
  SEGB1 to SEGB35 and ADB
  - CGROM_B 5×7 dots : 240 types (character data)
  - CGRAM_B 5×7 dots : 16 types (character data)
  - ADRAM_B 16 (display digit) × 1 bit (symbol data; can be used for a cursor.)
  - DCRAM_B 16 (display digit) × 8 bits (register for character data display)
- Display control function
  - Display digit : 1 to 16 digits
  - Display duty (brightness adjustment) : 0 to 1024 stages
  - All lights ON/OFF
- 3 interfaces with microcontroller : DA, $\overline{CS}$, $\overline{CP}$ (4 interfaces when $\overline{RESET}$ is added)
- Built-in oscillation circuit
  Crystal oscillation or ceralock oscillation : 4.0 MHz (Typ)
- Package options:
  100-pin plastic QFP (QFP100-P-1420-0.65-BK) (Product name: ML9203-xxGA)

BLOCK DIAGRAM

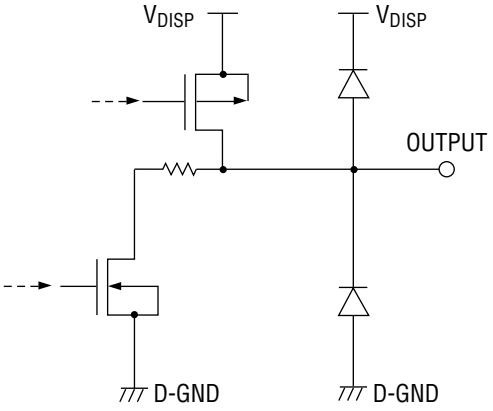


INPUT AND OUTPUT CONFIGURATION

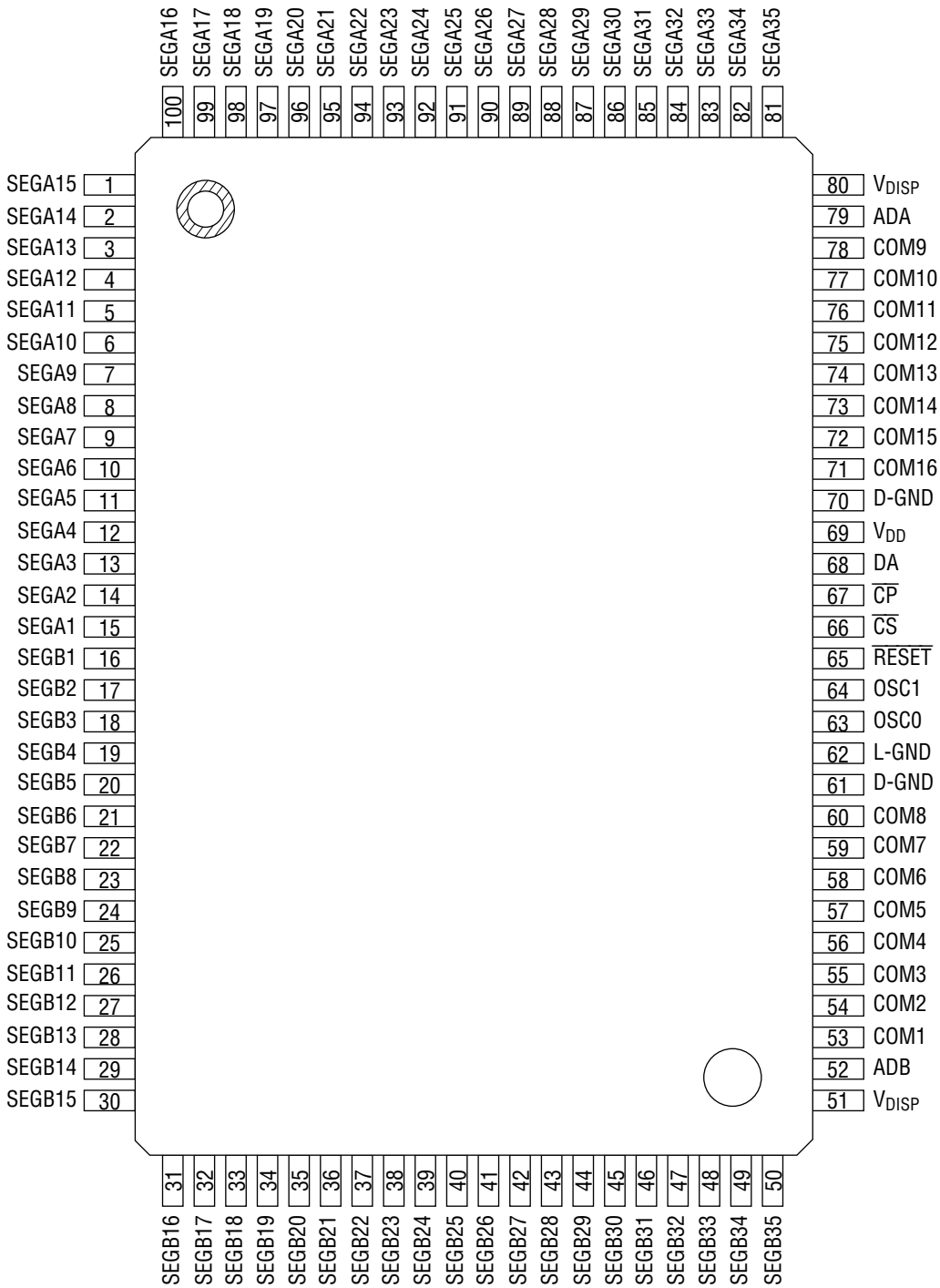
Schematic Diagram of Logic Portion Input Circuit



Schematic Diagram of Driver Output Circuit



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic QFP

PIN DESCRIPTION

Pin	Symbol	Type	Connects to	Description
1 to 15, 81 to 100	SEGA1 to A35	O	VFD tube anode electrode	VFD tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH}>–5 mA
16 to 50	SEGB1 to B35			
53 to 60 71 to 78	COM1 to 16	O	VFD tube grid electrode	VFD tube grid electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH}>–50 mA
52, 79	ADA, ADB	O	VFD tube anode electrode	VFD tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH}>–20 mA
69	V_{DD}	—	Power supply	V_{DD}-L-GND are power supplies for internal logic. V_{DISP}-D-GND are power supplies for driving fluorescent tubes. Apply V_{DISP} after V_{DD} is applied. Use the same power supply for L-GND and D-GND.
62	L-GND			
51, 80	V_{DISP}			
61, 70	D-GND			
68	DA	I	Micro-controller	Serial data input (positive logic). Input from LSB.
67	$\overline{CP}$	I	Micro-controller	Shift clock input. Serial data is shifted on the rising edge of $\overline{CP}$.
66	$\overline{CS}$	I	Micro-controller	Chip select input. Serial data transfer is disabled when $\overline{CS}$ pin is "H" level.
65	$\overline{RESET}$	I	Micro-controller or C, R	Reset input. "Low" initializes all the functions. Initial status is as follows. • Address of each RAM ····· address "00"H • Data of each RAM ····· Content is undefined • Display digit ····· 16 digits • Brightness adjusment ····· 0/1024 • All lights ON or OFF ····· OFF mode For a circuit when R and C are connected externally, see Application Circuit.
63	OSC0	I	Crystal or ceralock resonator	Pins for oscillation. Connect crystal and capacitors or ceralock resonator and capacitors. (Use a built-in feedback resistor.) Set the target oscillation frequency to 4 MHz. For an external circuit, see APPLICATION CIRCUIT.
64	OSC1	O		

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	—	–0.3 to 6.5	V
Supply Voltage (2)	V_{DISP}	—	–0.3 to 70	V
Input Voltage	V_{IN}	—	–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta≥25°C	764	mW
Storage Temperature	T_{STG}	—	–55 to 150	°C
Output Current	I_{O1}	COM1 to COM16	–60 to 0.0	mA
	I_{O2}	ADA, ADB	–30 to 0.0	mA
	I_{O3}	SEGA1 to SEGA35, SEGB1 to SEGB35	–10 to 0.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	When the power supply voltage is 5V (typ.)	4.5	5.0	5.5	V
		When the power supply voltage is 3.3V (typ.)	3.0	3.3	3.6	V
Supply Voltage (2)	V_{DISP}	—	20	—	60	V
Operating Frequency	f_{OSC}	Oscillation	3.5	4.0	4.5	MHz
Frame Frequency	f_{FR}	DIGIT=1 to 16, oscillation	213	244	275	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0V±10%, or V_{DD}=3.3V±10%, V_{DISP}=20 to 60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1	V_{DD}=5.0V±10%		0.7V_{DD}	—	V
			V_{DD}=3.3V±10%		0.8V_{DD}	—	V
Low Level Input Voltage	V_{IL}	*1	V_{DD}=5.0V±10%		—	0.3V_{DD}	V
			V_{DD}=3.3V±10%		—	0.2V_{DD}	V
High Level Input Current	I_{IH}	*1	V_{IH}=V_{DD}		–1.0	1.0	µA
Low Level Input Current	I_{IL}	*1	V_{IL}=0.0V		–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	COM1 to 16	V_{DISP}=60V, I_{OH1}=–50mA		V_{DISP}–1.5	—	V
	V_{OH2}	ADA, ADB	V_{DISP}=60V, I_{OH2}=–20mA		V_{DISP}–1.5	—	V
	V_{OH3}	SEG1 to 35	V_{DISP}=60V, I_{OH3}=–5mA		V_{DISP}–1.5	—	V
Low Level Output Voltage	V_{OL1}	*2	—		—	1.0	V
Current Consumption	I_{DD1}	V_{DD}	V_{DD}=5.0V±10%, f_{OSC}=4.0MHz		—	6	mA
	I_{DD2}		V_{DD}=3.3V±10%, f_{OSC}=4.0MHz		—	4	mA
	I_{DISP1}	V_{DISP}	f_{OSC}=4.0MHz, no load	All output lights ON	—	1	mA
	I_{DISP2}			All output lights OFF	—	T.B.D	mA

*1) $\overline{CS}$, $\overline{CP}$, DA $\overline{RESET}$

*2) SEGA1 to A35, SEGB1 to B35, ADA, COM1 to 16

AC Characteristics

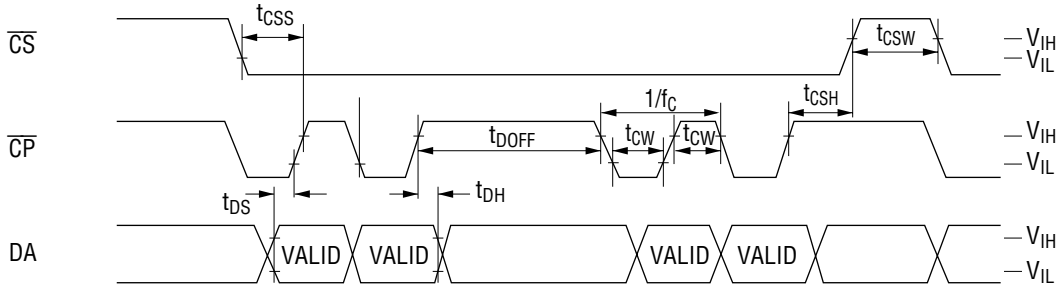
(V_{DD}=5.0V±10%, or V_{DD}=3.3V±10%, V_{DISP}=20 to 60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	1.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		300	—	ns
DA Setup Time	t_{DS}	—		300	—	ns
DA Hold Time	t_{DH}	—		300	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		300	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	Oscillating state		8	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		300	—	ns
Data Processing Time	t_{DOFF}	Oscillating state		4	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input from microcontroller etc. externally		300	—	ns
$\overline{RESET}$ Time	t_{RSON}	—		300	—	ns
DA Wait Time	t_{RSOFF}	—		300	—	ns
All Output Slew Rate	t_R	C_l=100pF	t_R=20% to 80%	—	2.0	µs
	t_F		t_F=80% to 20%	—	2.0	µs
V_{DD} Rise Time	t_{PRZ}	When mounted in the unit		—	100	µs
V_{DD} Off Time	t_{POF}	When mounted in the unit, V_{DD}=0.0V		5.0	—	ms

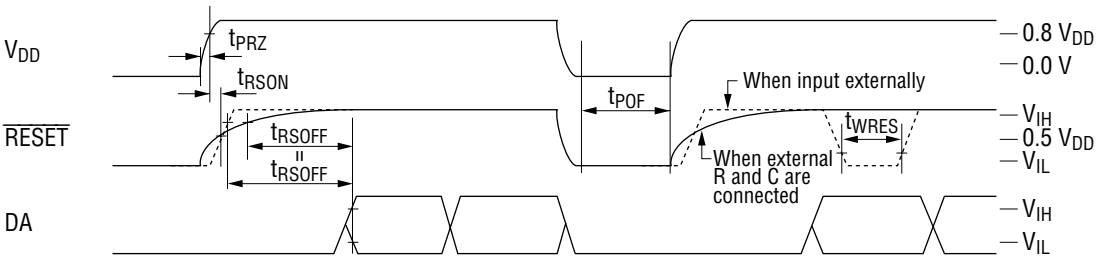
TIMING DIAGRAM

Symbol	V_{DD}=3.3V±10%	V_{DD}=5.0V±10%
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

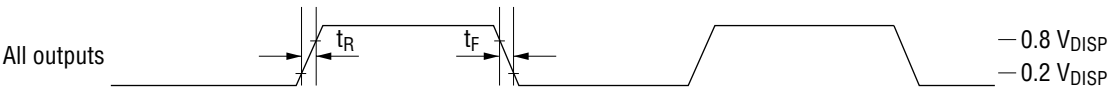
• Data Timing



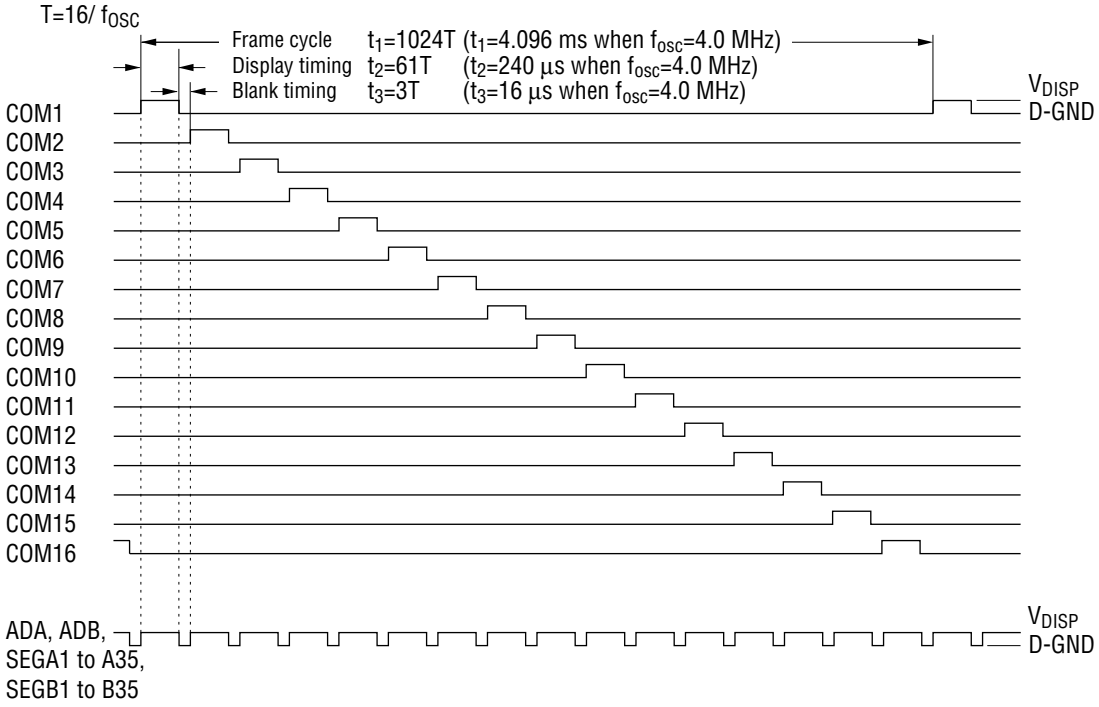
• Reset Timing



• Output Timing



• **Digit Output Timing (for 16-digit display, at a duty of 976/1024)**



FUNCTIONAL DESCRIPTION

Commands List

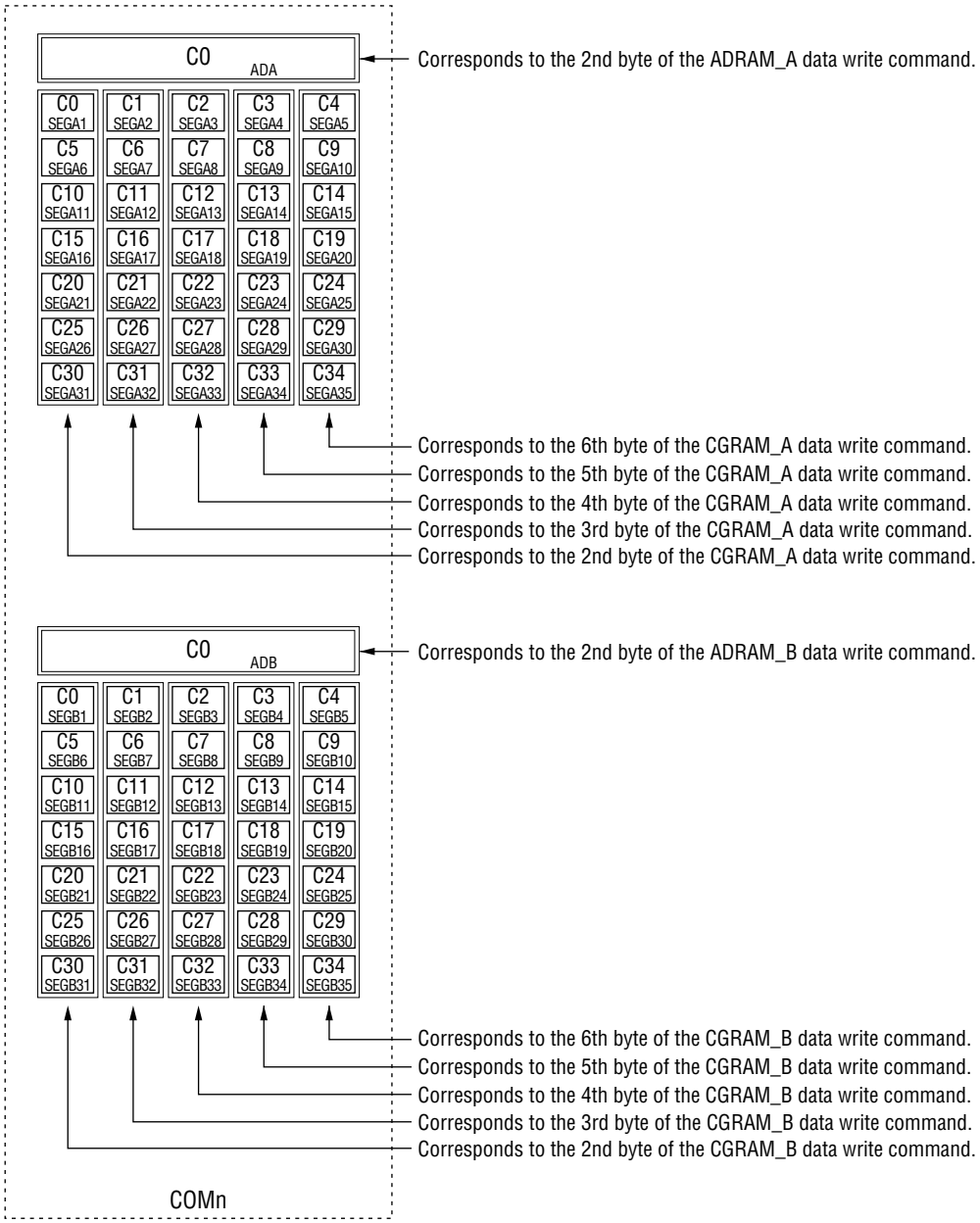
	Command	1st byte LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	2nd byte LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1	DCRAM_A data write	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM_A data write	X0	X1	X2	X3	0	1	0	0	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
3	ADRAM_A data write	X0	X1	X2	X3	1	1	0	0	C0	*	*	*	*	*	*	*	
4	—																	
5	Display duty set	D0	D1	*	*	1	0	1	0	D2	D3	D4	D5	D6	D7	D8	D9	
6	Number of digits set	K0	K1	K2	K3	0	1	1	0									
7	All lights ON/OFF	L	H	*	*	1	1	1	0									
8	—																	
9	DCRAM_B data write	X0	X1	X2	X3	1	0	0	1	C0	C1	C2	C3	C4	C5	C6	C7	
A	CGRAM_B data write	X0	X1	X2	X3	0	1	0	1	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
B	ADRAM_B data write	X0	X1	X2	X3	1	1	0	1	C0	*	*	*	*	*	*	*	
C	—																	
D	—																	
E	—																	
F	—																	
0	Test mode																	

When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Note: The test mode is used for inspection before shipment.
It is not a user function.

* : Don't care
Xn : Address specification for each RAM
Cn : Character code specification for each RAM
Dn : Display duty specification
Kn : Number of digits specification
H : All lights ON instruction
L : All lights OFF instruction

Positional Relationship Between SEGn and ADn (one digit)

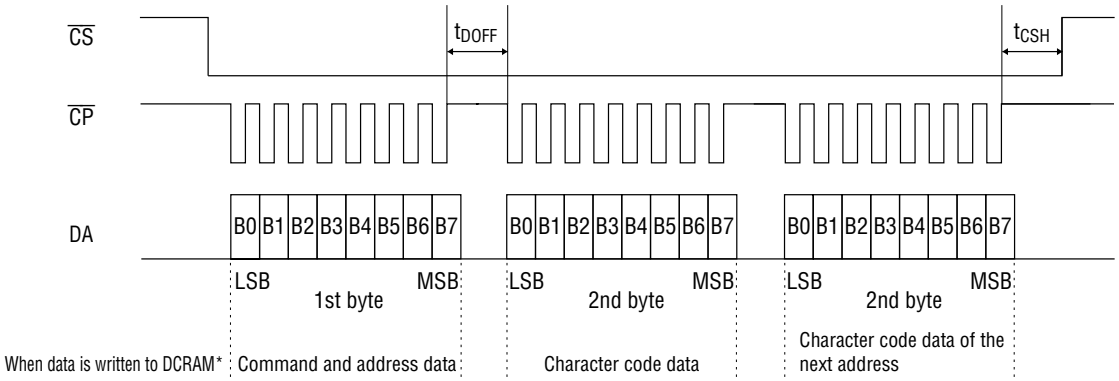


Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{CS}$ pin to "Low" level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the $\overline{CP}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{CS}$ pin to "High" disables data transfer. Data input from the point when the $\overline{CS}$ pin changes from "High" to "Low" is recognized in 8-bit units.



* When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Reset Function

Reset is executed when the $\overline{RESET}$ pin is set to "L", (when turning power on, for example) and initializes all functions.
Initial status is as follows.

- Address of each RAM ..... address "00"H
- Data of each RAM ..... All contents are undefined
- Display digit ..... 16 digits
- Brightness adjustment 0/1024
- All display lights ON or OFF ..... OFF mode
- Segment output ..... All segment outputs go "Low"
- AD output ..... All AD outputs go "Low"

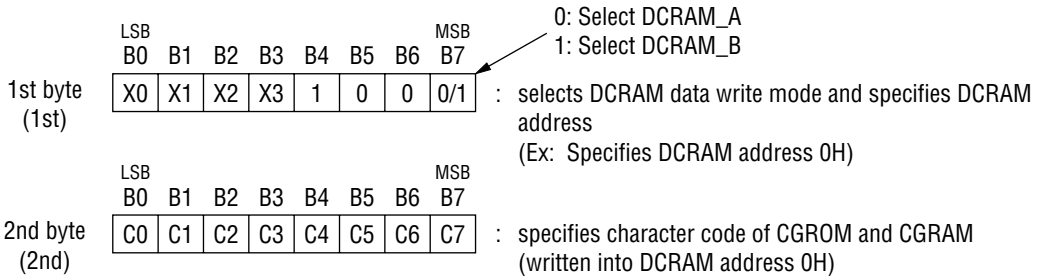
Please set again according to "Setting Flowchart" after reset.

Description of Commands and Functions

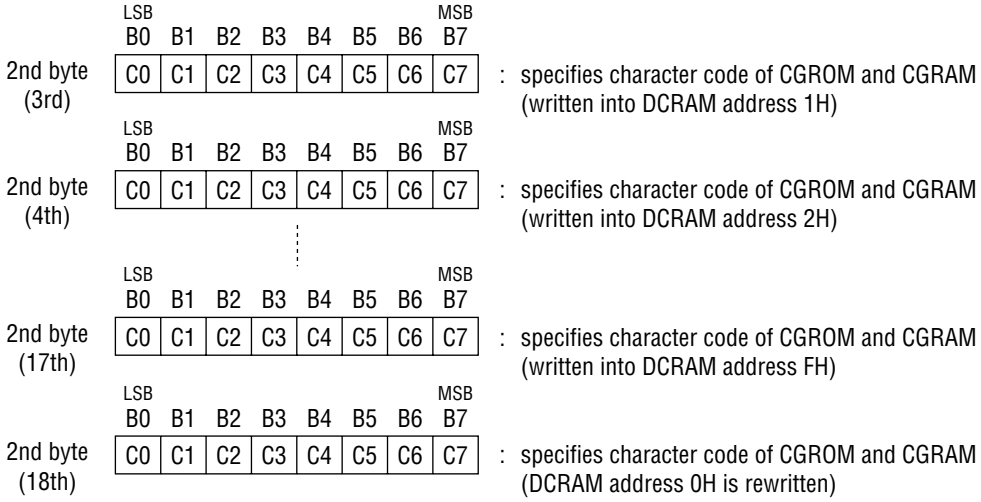
1. DCRAM data write
   (Specifies the address of DCRAM and writes the character code of CGROM and CGRAM.)

DCRAM (Data Control RAM) has a 4-bit address to store character code of CGROM and CGRAM.
The character code specified by DCRAM is converted to a 5×7 dot matrix character pattern via CGROM or CGRAM.
(The DCRAM can store 16 characters.)

[Command format]



To specify the character code of CGROM and CGRAM continuously to the next address, specify only character code as follows.
The addresses of DCRAM are automatically incremented. Specification of an address is unnecessary.



X0 (LSB) to X3 (MSB): DCRAM addresses (4 bits: 16 characters)
C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits: 256 characters)

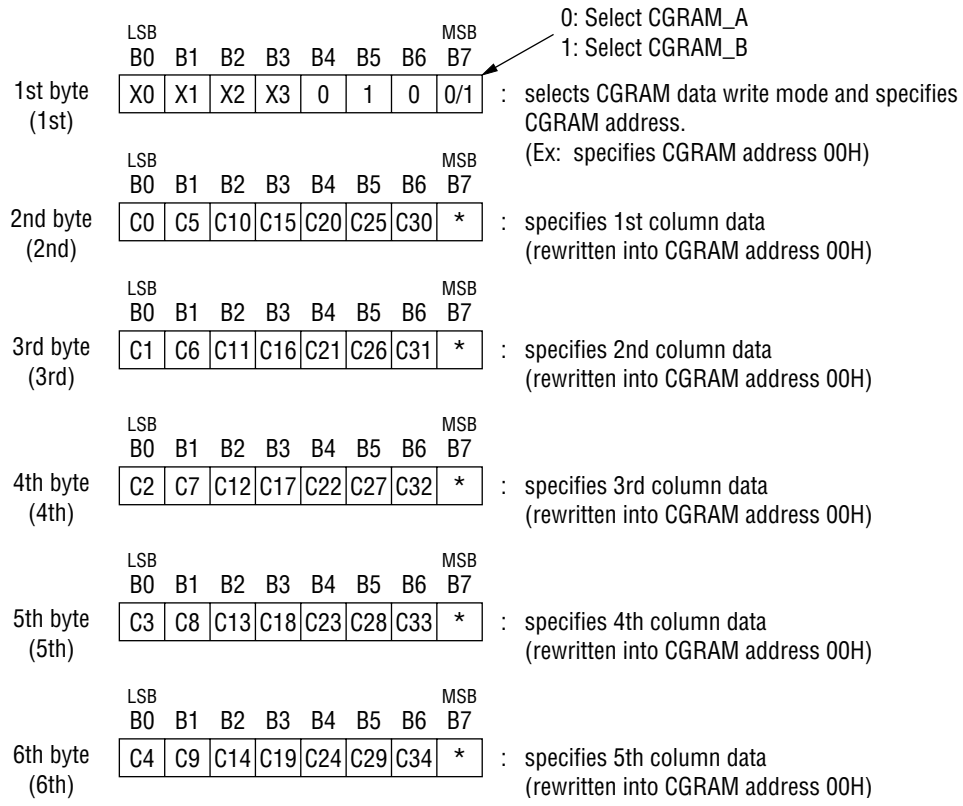
[COM positions and set DCRAM addresses]

HEX	X0	X1	X2	X3	COM position
0	0	0	0	0	COM1
1	1	0	0	0	COM2
2	0	1	0	0	COM3
3	1	1	1	0	COM4
4	0	0	1	0	COM5
5	1	0	1	0	COM6
6	0	1	1	0	COM7
7	1	1	1	0	COM8
8	0	0	0	1	COM9
9	1	0	0	1	COM10
A	0	1	0	1	COM11
B	1	1	0	1	COM12
C	0	0	1	1	COM13
D	1	0	1	1	COM14
E	0	1	1	1	COM15
F	1	1	1	1	COM16

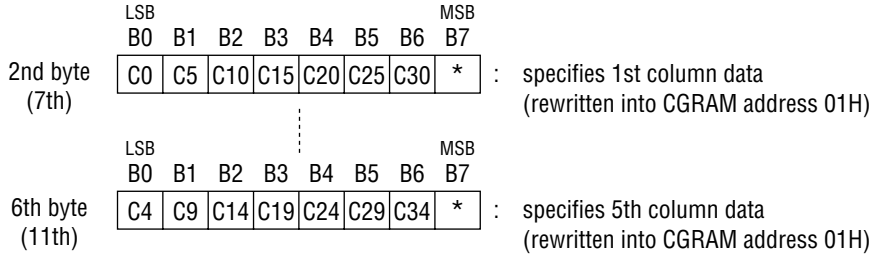
2. CGRAM data write
(Specifies the addresses of CGRAM and writes character pattern data.)

CGRAM (Character Generator RAM) has a 4-bit address to store 5×7 dot matrix character patterns.
A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCROM.
The address of CGRAM is assigned to 00H to 0FH. (All the other addresses are the CGROM addresses.)
(The CGRAM can store 16 types of character patterns.)

[Command format]



To specify character pattern data continuously to the next address, specify only character pattern data as follows.
The addresses of CGRAM are automatically incremented. Specification of an address is unnecessary.
The 2nd to 6th byte (character pattern data) are regarded as one data item, so 300 ns is sufficient for t_{DOFF} time between bytes.



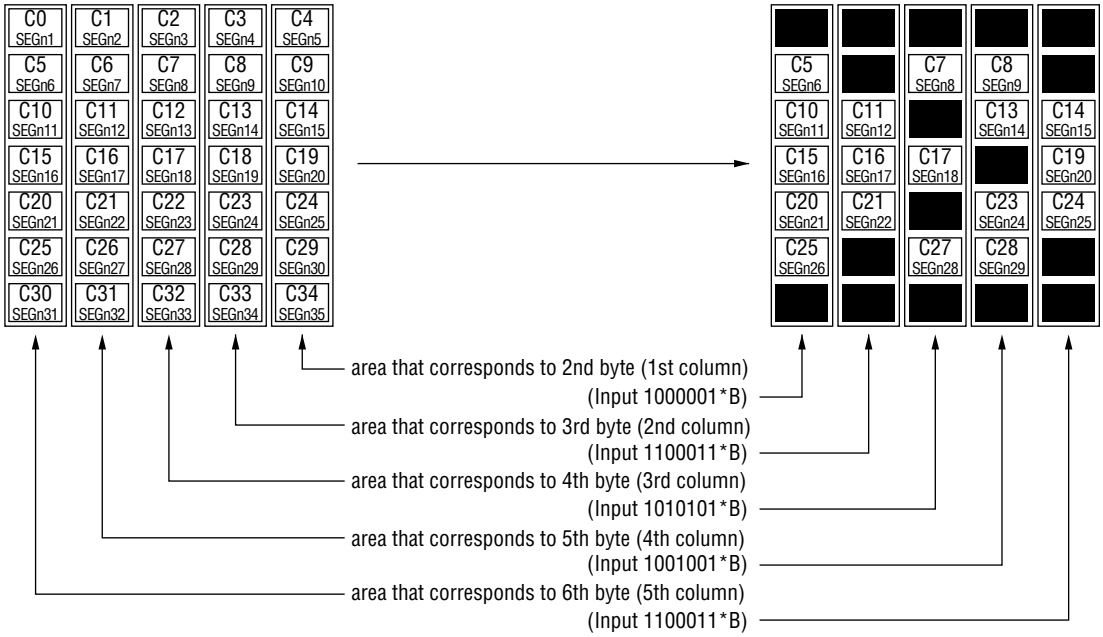
X0 (LSB) to X3 (MSB): CGRAM addresses (3 bits: 8 characters)
C0 (LSB) to C34 (MSB): Character pattern data (35 bits: 35 outputs per digit)
* : Don't care

[CGROM addresses and set CGRAM addresses]

Refer to ROM code tables.

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
0	0	0	0	0	RAM00(00000000B)	8	0	0	0	1	RAM08(00001000B)
1	1	0	0	0	RAM01(00000001B)	9	1	0	0	1	RAM09(00001001B)
2	0	1	0	0	RAM02(00000010B)	A	0	1	0	1	RAM0A(00001010B)
3	1	1	0	0	RAM30(00000011B)	B	1	1	0	1	RAM0B(00001011B)
4	0	0	1	0	RAM04(00000100B)	C	0	0	1	1	RAM0C(00001100B)
5	1	0	1	0	RAM05(00000101B)	D	1	0	1	1	RAM0D(00001101B)
6	0	1	1	0	RAM06(00000110B)	E	0	1	1	1	RAM0E(00001110B)
7	1	1	1	0	RAM70(00000111B)	F	1	1	1	1	RAM0F(00001111B)

Positional relationship between the output area of CGRAM

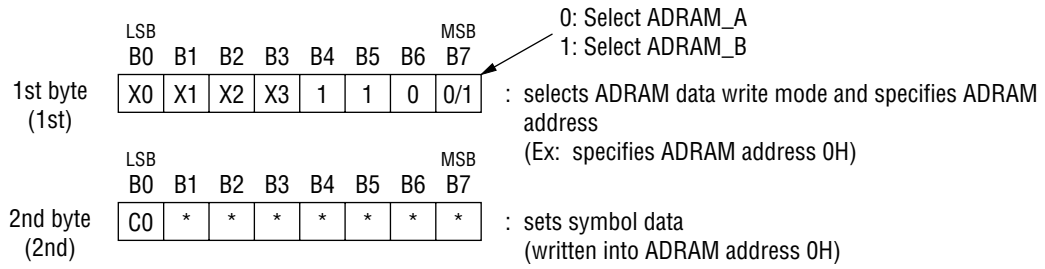


Note: CGROM_A and CGROM_B (Character Generator ROM A, B) have an 8-bit address to generate 5×7 dot matrix character patterns.
Each of CGROM_A and CGROM_B can store 240 types of character patterns.
The contents of CGROM_A and CGROM_B can be set separately.
General-purpose code -01 is available (see ROM code tables) and custom codes are provided on customer's request.

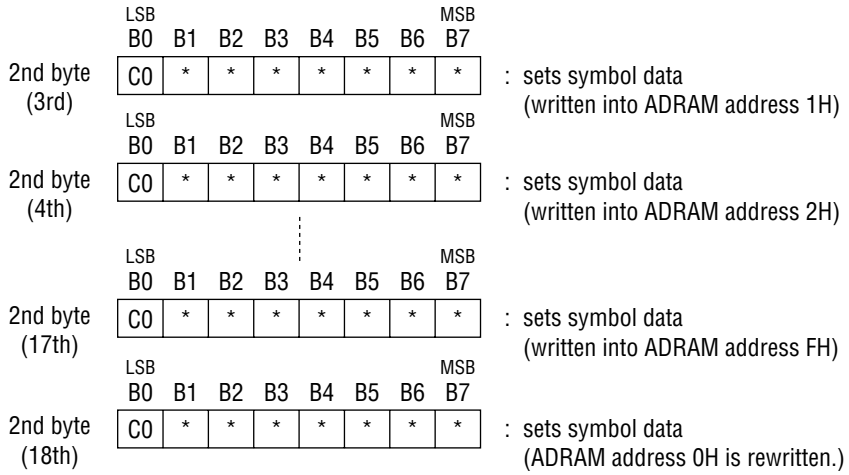
3. ADRAM data write
(specifies address of ADRAM and writes symbol data)

ADRAM (Additional Data RAM) has a 1-bit address to store symbol data.
Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
(The ADRAM can store 1 type of symbol patterns for each digit.)
The terminal to which the contents of ADRAM are output can be used as a cursor.

[Command format]



To specify symbol data continuously to the next address, specify only character data as follows. The address of ADRAM is automatically incremented. Specification of addresses is unnecessary.



X0 (LSB) to X3 (MSB) : ADRAM addresses (4 bits: 16 characters)
C0 : Symbol data (1 bit: 1-symbol data per digit)
* : Don't care

[COM positions and ADRAM addresses]

HEX	X0	X1	X2	X3	COM position
0	0	0	0	0	COM1
1	1	0	0	0	COM2
2	0	1	0	0	COM3
3	1	1	0	0	COM4
4	0	0	1	0	COM5
5	1	0	1	0	COM6
6	0	1	1	0	COM7
7	1	1	1	0	COM8
8	0	0	0	1	COM9
9	1	0	0	1	COM10
A	0	1	0	1	COM11
B	1	1	0	1	COM12
C	0	0	1	1	COM13
D	1	0	1	1	COM14
E	0	1	1	1	COM15
F	1	1	1	1	COM16

5. Display duty set
(writes display duty value to duty cycle register)

Display duty adjusts brightness in 1024 stages using 10-bit data.
When power is turned on or when the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". Always execute this instruction before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	D0	D1	*	*	1	0	1	0	: selects display duty set mode and sets duty value (lower 2 bits)
	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (2nd)	D2	D3	D4	D5	D6	D7	D8	D9	: sets duty value (upper 8 bits)

D0 (LSB) to D9 (MSB) : Display duty data (10 bits: 1024 stages)
* : Don't care

[Relation between setup data and controlled COM duty]

HEX	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	COM duty
000	0	0	0	0	0	0	0	0	0	0	0/1024
001	1	0	0	0	0	0	0	0	0	0	1/1024
002	0	1	0	0	0	0	0	0	0	0	2/1024
⋮											⋮
3CE	0	1	1	1	0	0	1	1	1	1	974/1024
3CF	1	1	1	1	0	0	1	1	1	1	975/1024
3D0	0	0	0	0	1	0	1	1	1	1	976/1024
3D1	1	0	0	0	1	0	1	1	1	1	976/1024
⋮											⋮
3FF	1	1	1	1	1	1	1	1	1	1	976/1024

The state when power is turned on or when $\overline{\text{RESET}}$ signal is input.

6. Number of digits set
(writes the number of display digits to the display digit register)

The number of digits set can display 1 to 16 digits using 4-bit data.
When power is turned on or when a $\overline{\text{RESET}}$ signal is input, the number of digit register value is "0". Always execute this instruction to change the number of digits before turning the dispaly on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	K0	K1	K2	K3	0	1	1	0	: selects the number of digit set mode and specifies the number of digit value

K0 (LSB) to K3 (MSB) : Number of digit data (4 bits: 16 digits)
* : Don't care

[Relation between setup data and controlled COM]

HEX	K0	K1	K2	K3	Number of digits of COM	HEX	K0	K1	K2	K3	Number of digits of COM
0	0	0	0	0	COM1 to 16	0	0	0	0	1	COM1 to 8
1	1	0	0	0	COM1	1	1	0	0	1	COM1 to 9
2	0	1	0	0	COM1 to 2	2	0	1	0	1	COM1 to 10
3	1	1	0	0	COM1 to 3	3	1	1	0	1	COM1 to 11
4	0	0	1	0	COM1 to 4	4	0	0	1	1	COM1 to 12
5	1	0	1	0	COM1 to 5	5	1	0	1	1	COM1 to 13
6	0	1	1	0	COM1 to 6	6	0	1	1	1	COM1 to 14
7	1	1	1	0	COM1 to 7	7	1	1	1	1	COM1 to 15

The state when power is turned on or when $\overline{\text{RESET}}$ signal is input.

7. All display lights ON/OFF set
(turns all dispaly lights ON or OFF)

All display lights ON is used primarily for display testing.
All display lights OFF is primarily used for display blink and to prevent malfunction when power is turned on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	1	1	1	0	: selects all display lights ON or OFF mode

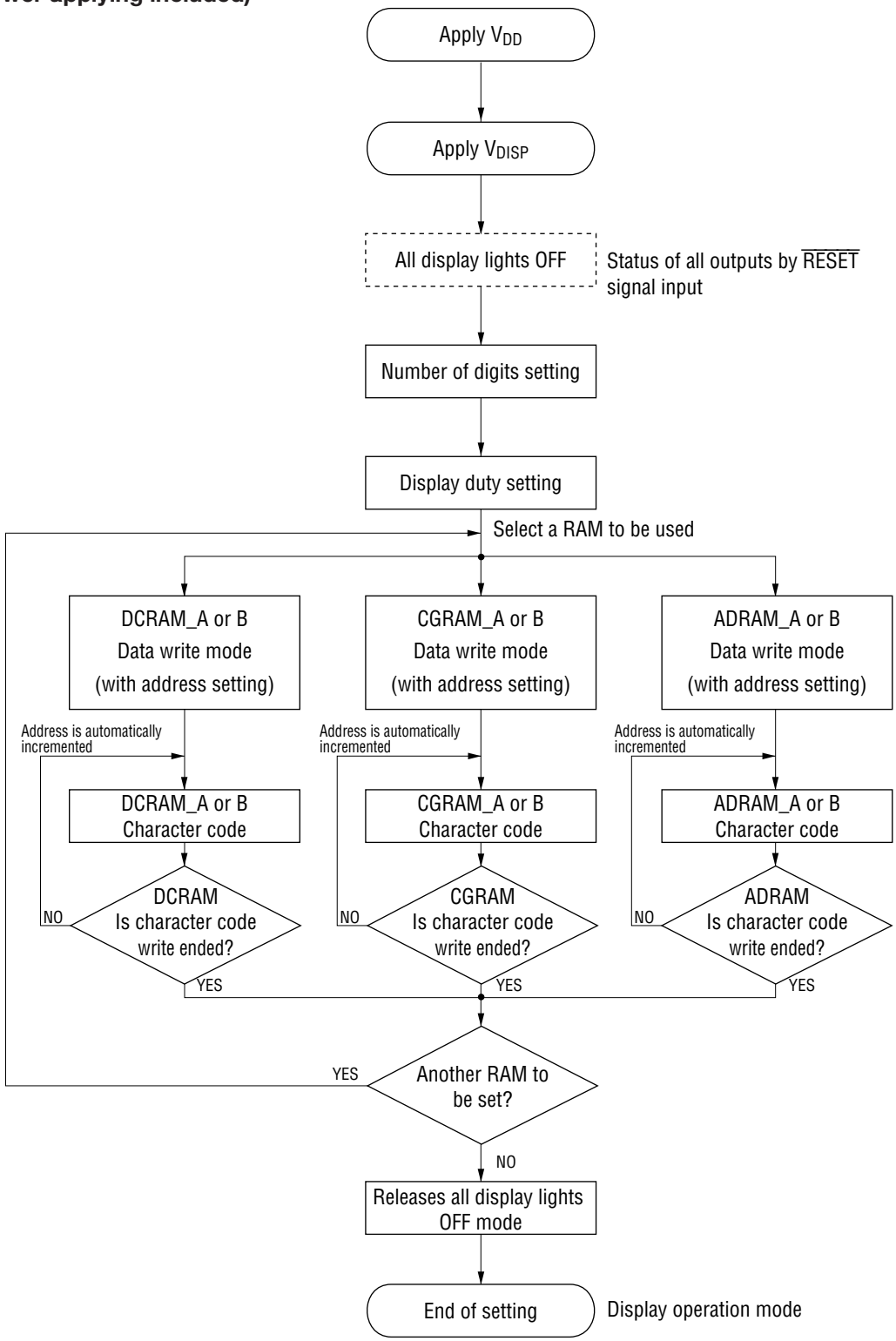
L, H: display operation data
*: Don't care

[Set data and display state of SEG and AD]

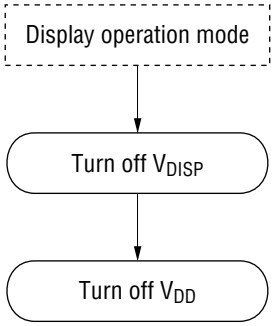
L	H	Display state of SEG and AD
0	0	Normal display
1	0	Sets all outputs to Low
0	1	Sets all outputs to High
1	1	Sets all outputs to High

(The state when power is applied or when $\overline{\text{RESET}}$ is input.)

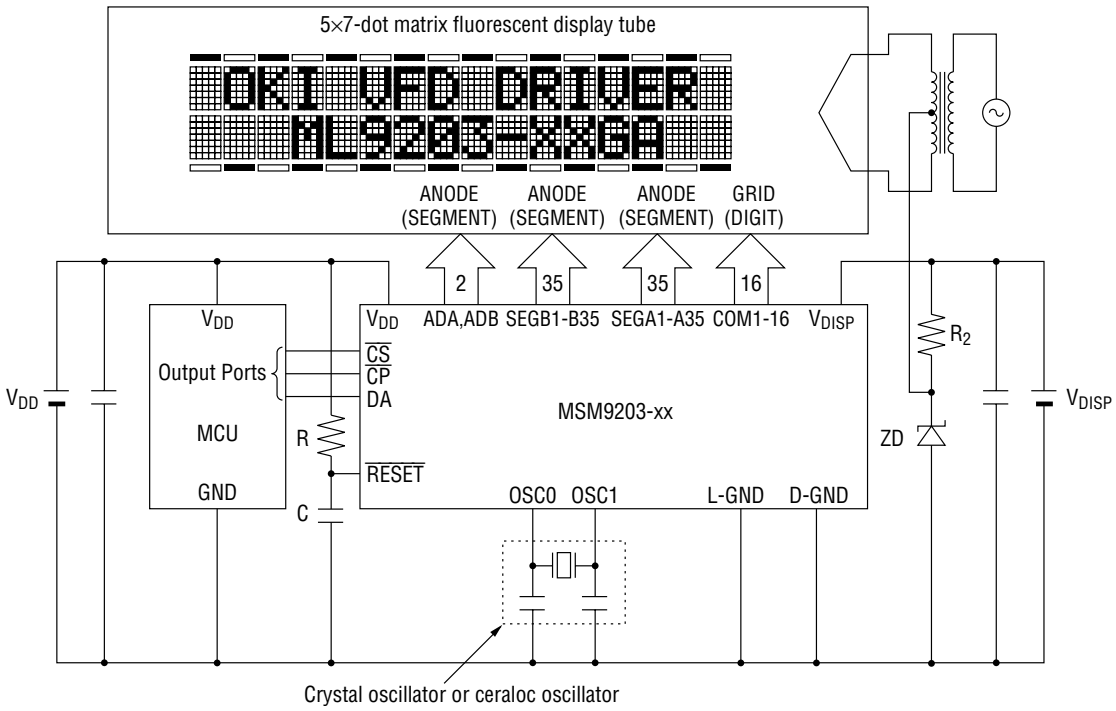
Setting Flowchart
(Power applying included)



Power-off Flowchart



APPLICATION CIRCUIT

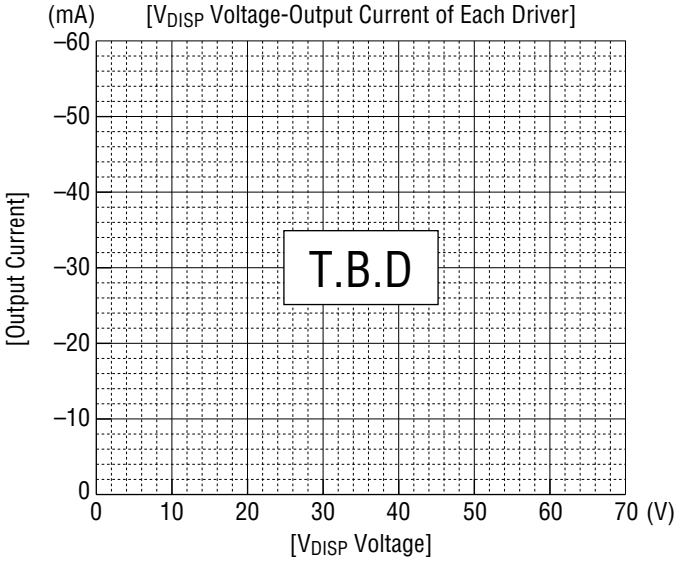


Notes: 1. The V_{DD} value depends on the power supply voltage of the microcontroller used. Adjust the values of the constants and C input to $\overline{RESET}$ to the power supply voltage used.

2. The V_{DISP} value depends on the fluorescent display tube used. Adjust the values of the constants R_2 and ZD to the power supply voltage used.

Reference data

The figure below shows the relationship between the V_{DISP} voltage and the output current of each driver.
Take care that the total power consumption to be used does not exceed the power dissipation.



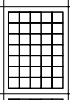
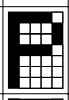
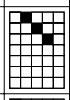
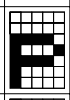
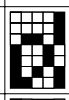
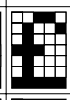
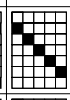
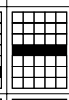
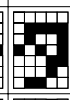
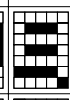
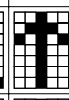
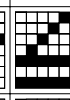
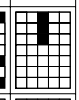
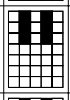
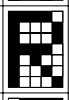
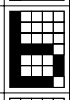
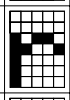
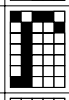
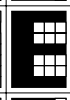
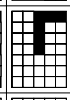
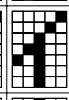
ML9203-01 CGROM_A Code

00000000B (00H) to 00000111B (0FH) are the CGRAM_A addresses.

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM00															
0001	RAM01															
0010	RAM02															
0011	RAM03															
0100	RAM04															
0101	RAM05															
0110	RAM06															
0111	RAM07															
1000	RAM08															
1001	RAM09															
1010	RAM0A															
1011	RAM0B															
1100	RAM0C															
1101	RAM0D															
1110	RAM0E															
1111	RAM0F															

ML9203-01 CGROM_B Code

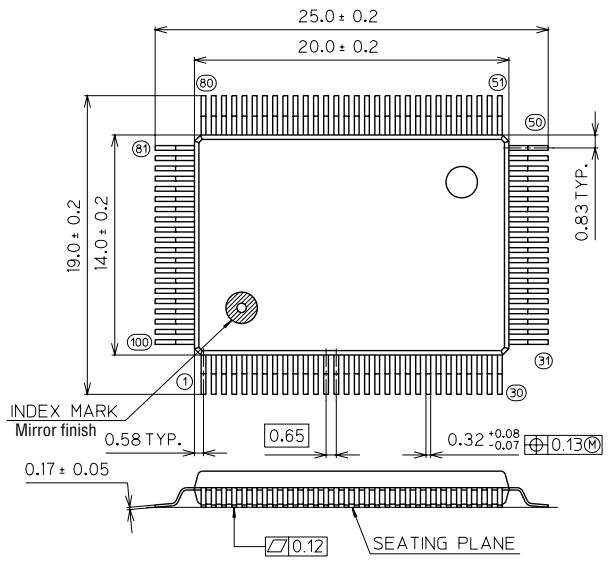
00000000B (00H) to 00000111B (0FH) are the CGRAM_B addresses.

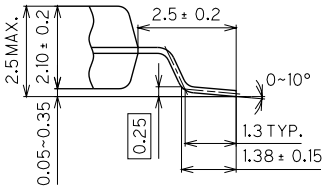
MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM00															
0001	RAM01															
0010	RAM02															
0011	RAM03															
0100	RAM04															
0101	RAM05															
0110	RAM06															
0111	RAM07															
1000	RAM08															
1001	RAM09															
1010	RAM0A															
1011	RAM0B															
1100	RAM0C															
1101	RAM0D															
1110	RAM0E															
1111	RAM0F															

PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-BK





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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