

ML9212

32-Bit Duplex/Triplex (1/2 duty / 1/3 duty) VF Controller/Driver with Digital Dimming

GENERAL DESCRIPTION

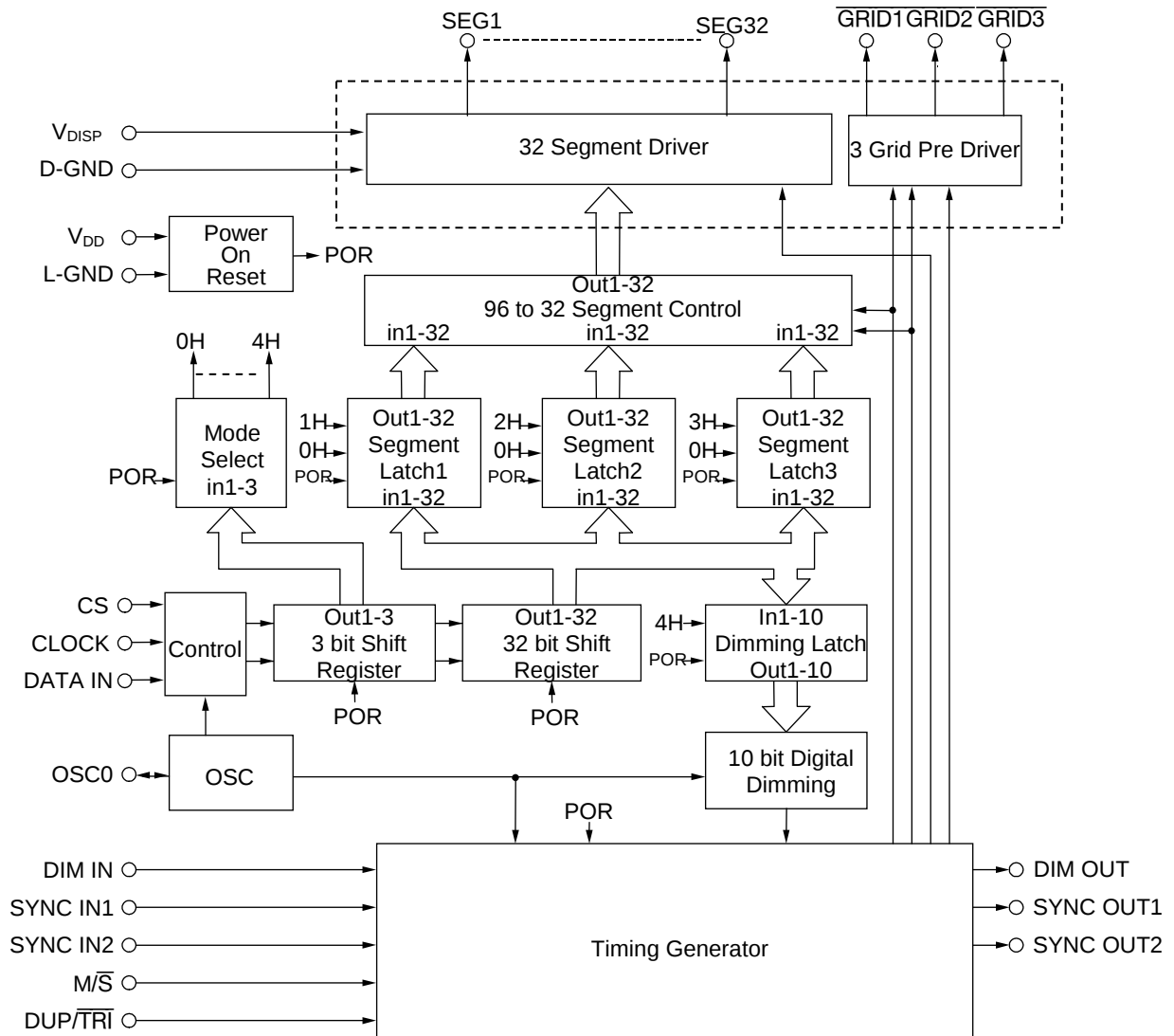
The ML9212 is a full CMOS controller/driver for Duplex or Triplex (1/2 duty or 1/3 duty) vacuum fluorescent display tube. It consists of a 32-segment driver multiplexed to drive up to 96 segments, and 10-bit digital dimming circuit.

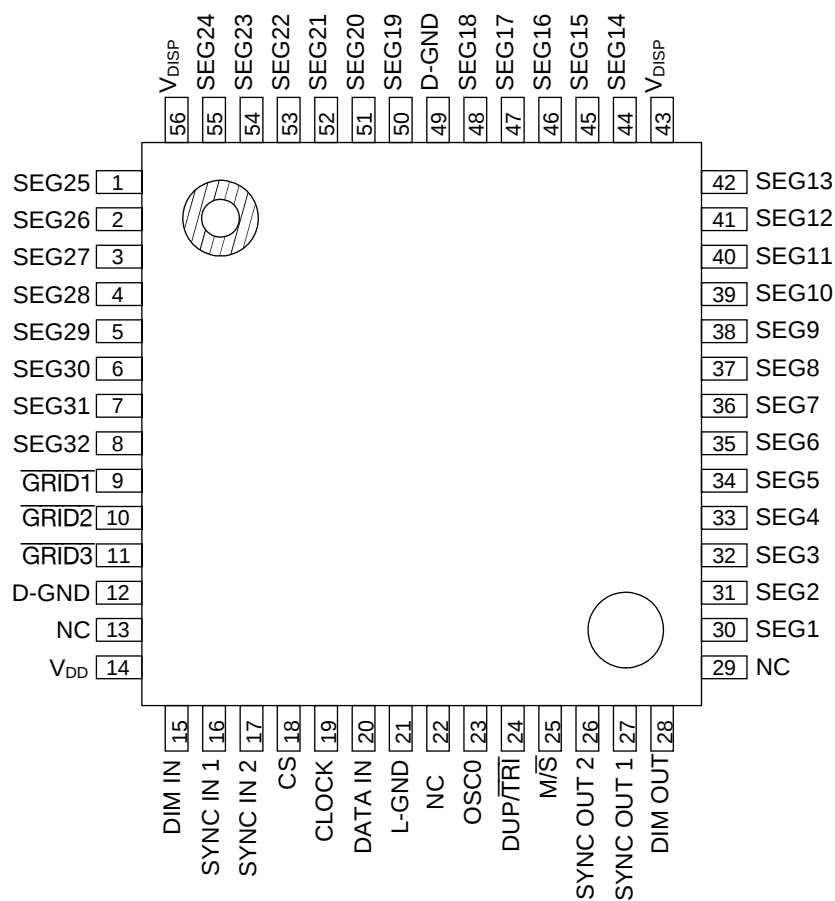
ML9212 features a selection of a master mode and a slave mode, and therefore it can be used to expand segments for the VFD driver with keyscan and A/D converter function.

ML9212 provides an interface with a microcontroller only by three signal lines: DATA IN, CLOCK and CS.

FEATURES

- Logic supply voltage (V_{DD}) : 4.5 to 5.5 V
- Driver supply voltage (V_{DISP}) : 8 to 18 V
- Duplex/Triplex (1/2 duty / 1/3 duty) selectable
 $DUP/\overline{TRI}$ = 1/2 duty selectable at "H" level
 $DUP/\overline{TRI}$ = 1/3 duty selectable at "L" level
- Number of display segments
 Max. 64-segment display (during 1/2 duty mode)
 Max. 96-segment display (during 1/3 duty mode)
- Master/Slave selectable
 $M/\overline{S}$ = Master mode selectable at "H" level
 $M/\overline{S}$ = Slave mode selectable at "L" level
- Interface with a microcontroller
 Three lines: CS, CLOCK, and DATA IN
- 32-segment driver outputs : $I_{OH} = -5 \text{ mA}$ at $V_{OH} = V_{DISP} - 0.8 \text{ V}$ (SEG1 to 22)
 (can be directly connected to VFD tube : $I_{OH} = -10 \text{ mA}$ at $V_{OH} = V_{DISP} - 0.8 \text{ V}$ (SEG23 to 32)
 and require no external resistors) : $I_{OL} = 500 \text{ } \mu\text{A}$ at $V_{OL} = 2 \text{ V}$ (SEG1 to 32)
- 3-grid pre-driver outputs : $I_{OH} = -5.0 \text{ mA}$ at $V_{OH} = V_{DISP} - 0.8 \text{ V}$
 (require external drivers) : $I_{OL} = 10 \text{ mA}$ at $V_{OL} = 2 \text{ V}$
- Logic outputs : $I_{OH} = -200 \text{ } \mu\text{A}$ at $V_{OH} = V_{DD} - 0.8 \text{ V}$
 $I_{OL} = 200 \text{ } \mu\text{A}$ at $V_{OL} = 0.8 \text{ V}$
- Built-in digital dimming circuit (10-bit resolution)
- Built-in oscillation circuit (external R and C)
- Built-in Power-On-Reset circuit
- Package options:
 56-pin plastic QFP (QFP56-P-910-0.65-2K)(ML9212GA)

BLOCK DIAGRAM

PIN CONFIGURATION (TOP VIEW)

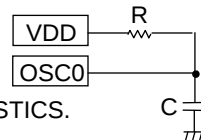
NC: No connection
(OPEN)

56-pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Pin	Type	Description
V_{DISP}	43, 56	—	Power supply pins for VFD driver circuit. 43 pin and 56 pin should be connected externally.
V_{DD}	14	—	Power supply pin for logic drive.
D-GND	12, 49	—	D-GND is ground pin for the VFD driver circuit. L-GND is ground pin for the logic circuit. 12 pin, 21 pin and 49 pin should be connected externally.
L-GND	21	—	
SEG1 to 22	30 to 42, 44 to 48, 50 to 53	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OHL} \leq -5 \text{ mA}$
SEG23 to 32	1 to 8, 54, 55	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OHL} \leq -10 \text{ mA}$
$\overline{\text{GRID1}}$ to $\overline{3}$	9, 10, 11	O	Inverted Grid signal output pins. For pre-driver, the external circuit is required. $I_{OL} \leq 10 \text{ mA}$
CS	18	I	Chip select input pin. Data is not transferred when CS is set to a Low level.
CLOCK	19	I	Shift clock input pin. Serial data shifts at the rising edge of the CLOCK.
DATA IN	20	I	Serial data input pin (positive logic). Data is input to the shift register at the rising edge of the CLOCK signal.
DUP/ $\overline{\text{TRI}}$	24	I	Duplex/Triplex operation select input pin. Duplex (1/2 duty) operation is selected when this pin is set to V_{DD} . Triplex (1/3 duty) operation is selected when this pin is set to L-GND.
$M/\overline{S}$	25	I	Master/Slave mode select input pin. Master mode is selected when this pin is set to V_{DD} . Slave mode is selected when this pin is set to L-GND.
DIM IN	15	I	Dimming pulse input. When the slave mode is selected, the pulse width of the all segment output are controlled by a input pulse width of DIM IN. Connect this pin to the master side DIM OUT pin at the slave mode. When the master mode is selected, the input level of this pin is ignored and the pulse width of the all grids and segment outputs are controlled by a built-in 10-bit dimming circuit. Connect this pin to V_{DD} or L-GND at the master mode.

Symbol	Pin	Type	Description
SYNC IN 1, 2	16, 17	I	Synchronous signal input. When the slave mode is selected, connect these pins to the master side SYNC OUT 1, and 2 pins. When the master mode is selected, the input level of these pins are ignored. Connect these pins to V _{DD} or L-GND at the master mode.
DIM OUT	28	O	Dimming pulse output. Connect this pin to the slave side DIM IN pin.
SYNC OUT 1, 2	26, 27	O	Synchronous signal output. Connect these pins to the slave side SYNC IN 1, and 2 pins.
OSC0	23	I/O	RC oscillator connecting pins. Oscillation frequency depends on display tubes to be used. For details refer to ELECTRICAL CHARACTERISTICS.
NC	13,22,29	-	OPEN pins.



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Ratings	Unit
Driver Supply Voltage	V _{DISP}	—	−0.3 to +20	V
Logic Supply Voltage	V _{DD}	—	−0.3 to +6.5	V
Input Voltage	V _{IN}	—	−0.3 to V _{DD} +0.3	V
Power Dissipation	P _D	T _a ≥ 105°C	233	mW
Storage Temperature	T _{STG}	—	−55 to +150	°C
Output Current	I _{o1}	SEG1 to 22	−10.0 to +2.0	mA
	I _{o2}	SEG23 to 32	−20.0 to +2.0	mA
	I _{o3}	$\overline{\text{GRID1}}$ to $\overline{3}$	−10.0 to +20.0	mA
	I _{o4}	DIM OUT, SYNC OUT1, SYNC OUT2	−2.0 to +2.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Driver Supply Voltage	V _{DISP}	—	8.0	13.0	18.0	V
Logic Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V
High Level Input Voltage	V _{IH}	All inputs except OSC0	0.8V _{DD}	—	—	V
Low Level Input Voltage	V _{IL}	All inputs except OSC0	—	—	0.2V _{DD}	V
Clock Frequency	f _C	—	—	—	2.0	MHz

Parameter	Symbol	Condition		Min	Typ.	Max.	Unit
Oscillation Frequency	f_{OSC}	R = 10 k Ω ±5%, C = 27 pF±5%		2.2	3.3	4.4	MHz
Frame Frequency	f_{FR}	R = 10 k Ω ±5%, C = 27 pF±5%	1/3 duty	179	269	358	Hz
			1/2 duty	268	403	538	
Operating Temperature	T_{OP}	—		−40	—	+105	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

$T_a = -40$ to $+105^{\circ}\text{C}$, $V_{\text{DISP}} = 8.0$ to 18.0 V , $V_{\text{DD}} = 4.5$ to 5.5 V

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V _{IH}	*1)	—		0.8V _{DD}	—	V
Low Level Input Voltage	V _{IL}	*1)	—		—	0.2V _{DD}	V
High Level Input Current	I _{IH}	*1)	V _{IH} = V _{DD}		−1.0	+1.0	μA
Low Level Input Current	I _{IL}	*1)	V _{IL} = GND		−1.0	+1.0	μA
High Level Output Voltage	V _{OH1}	SEG1-22	V _{DISP} = 9.5V	I _{OH1} = −5 mA	V _{DISP} − 0.8	—	V
	V _{OH2}	SEG23-32		I _{OH2} = −10 mA	V _{DISP} − 0.8	—	V
	V _{OH3}	GRID1-3		I _{OH3} = −5 mA	V _{DISP} − 0.8	—	V
	V _{OH4}	*2)	V _{DD} = 4.5 V	I _{OH4} = −200 μA	V _{DD} − 0.8	—	V
Low Level Output Voltage	V _{OL1}	SEG1-22	V _{DISP} = 9.5V	I _{OL1} = 500 μA	—	2.0	V
	V _{OL2}	SEG23-32		I _{OL2} = 500 μA	—	2.0	V
	V _{OL3}	GRID1-3		I _{OL3} = 10 mA	—	2.0	V
	V _{OL4}	*2)	V _{DD} = 4.5 V	I _{OL4} = 200 μA	—	0.8	V
Supply Current	I _{DISP}	V _{DISP}	R = 10 kΩ±5%, C = 27 pF±5% no load		—	100	uA
	I _{DD}	V _{DD}			—	5.0	mA

*1) CS, CLOCK, DATA IN, DIM IN, SYNC IN 1, SYNC IN 2, $\overline{\text{M/S}}$, $\overline{\text{DUP/TRI}}$

*2) DIM OUT, SYNC OUT 1, SYNC OUT 2

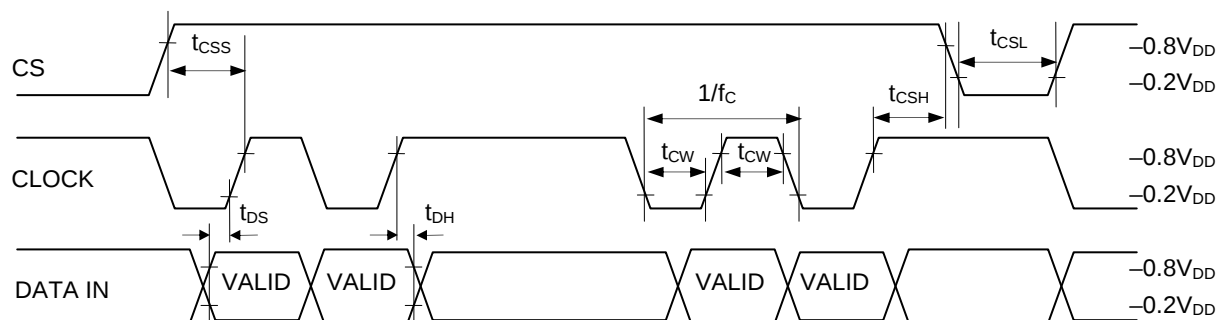
AC Characteristics

Ta = -40 to +105°C, V_{DISP} = 8.0 to 18.0 V, V_{DD} = 4.5 to 5.5 V

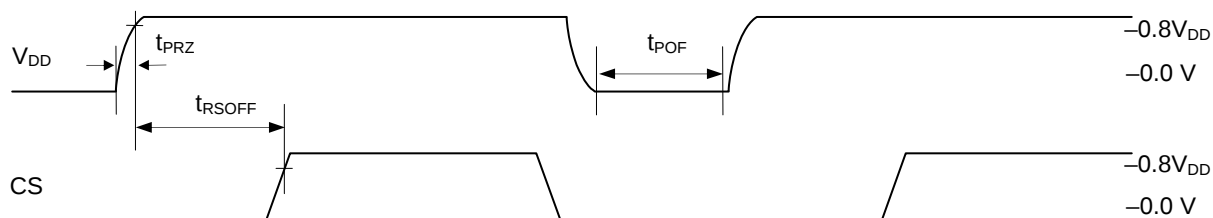
Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Frequency	f _C	—	—	2.0	MHz
Clock Pulse Width	t _{CW}	—	200	—	ns
Data Setup Time	t _{DS}	—	200	—	ns
Data Hold Time	t _{DH}	—	200	—	ns
CS Off Time	t _{CSL}	—	20	—	μs
CS Setup Time (CS-Clock)	t _{CSS}	—	200	—	ns
CS Hold Time (Clock-CS)	t _{CSH}	—	200	—	ns
CS Wait Time	t _{RSOFF}	—	400	—	ns
Output Slew Rate Time	t _R	C _L = 100 pF	—	2.0	μs
	t _F				
V _{DD} Rise Time	t _{PRZ}	Mounted in a unit	—	100	μs
V _{DD} Off Time	t _{POF}	Mounted in a unit, V _{DD} = 0.0 V	5.0	—	ms

TIMING DIAGRAM

Data Input Timing

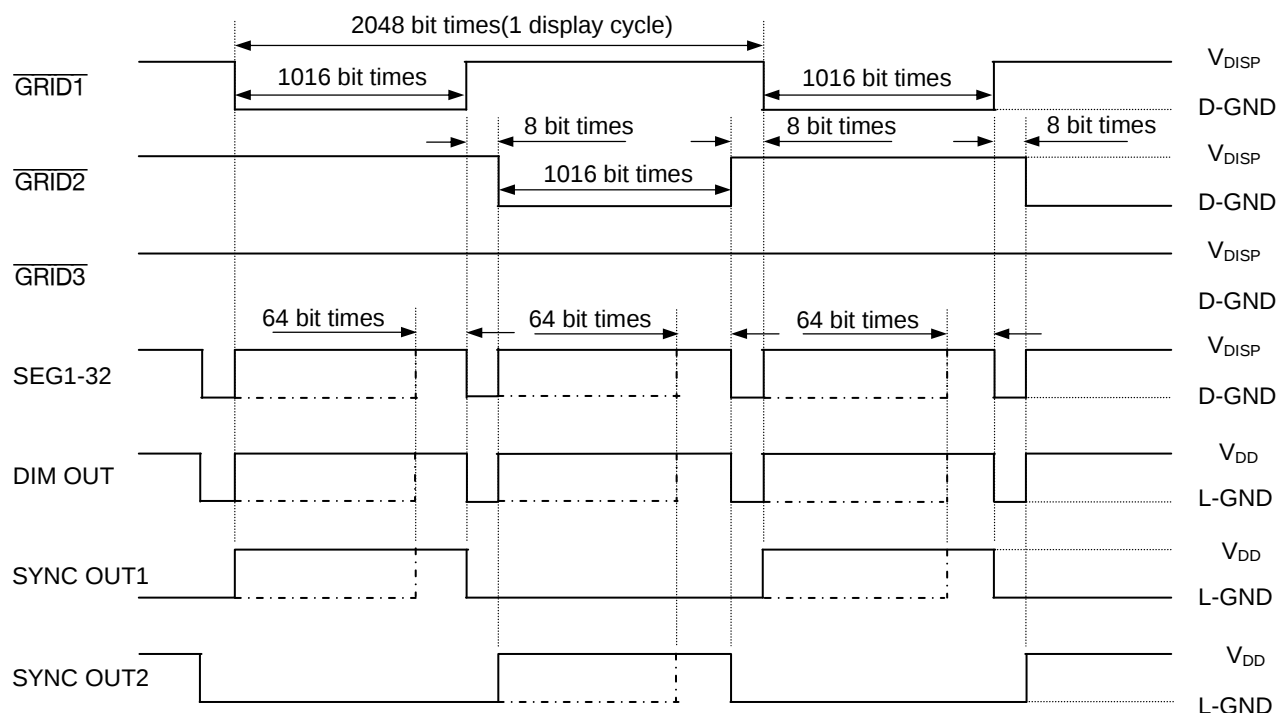
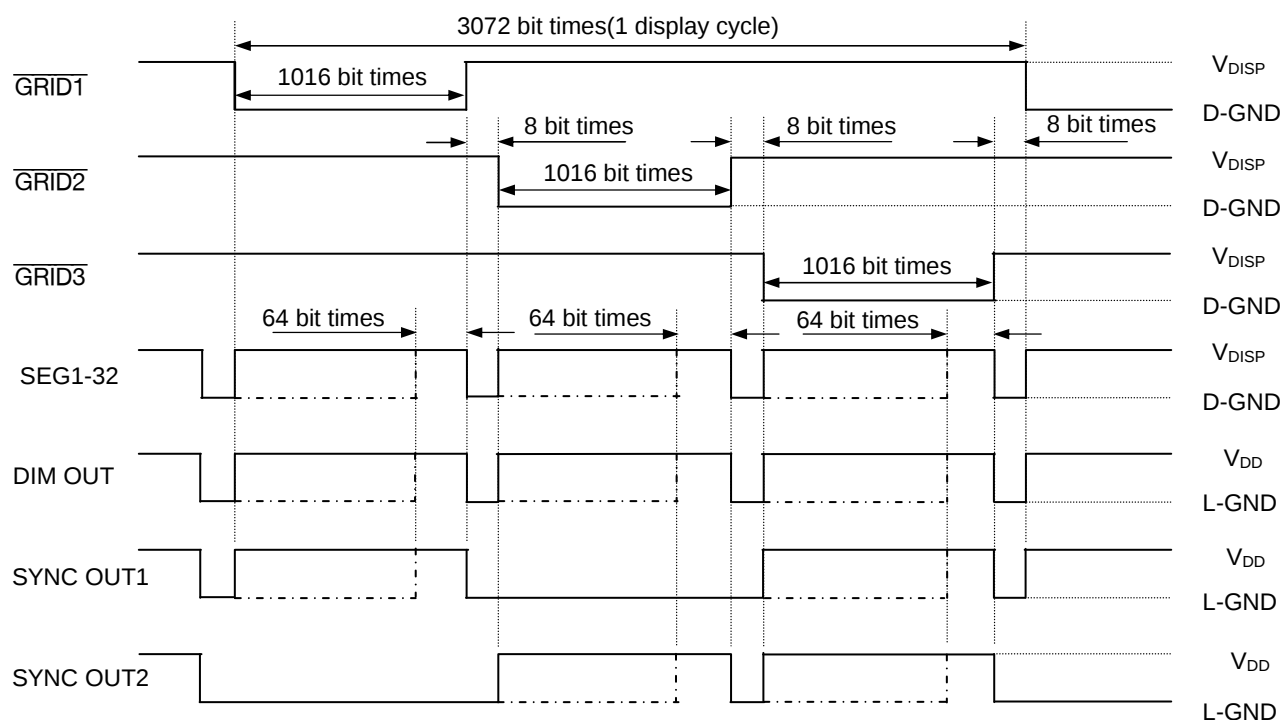


Reset Timing



Driver Output Timing



Output Timing (Duplex Operation) *1bit time = $4/f_{OSC}$ **Solid line : The dimming data is 1016/1024 at the master mode****Dotted line : The dimming data is 64/1024 at the master mode****Output Timing (Triplex Operation) *1bit time = $4/f_{OSC}$** **Solid line : The dimming data is 1016/1024 at the master mode****Dotted line : The dimming data is 64/1024 at the master mode**

FUNCTIONAL DESCRIPTION

Power-on Reset

When power is turned on, ML9212 is initialized by the internal power-on reset circuit.

The status of the internal circuit after initialization is as follows:

- The contents of the shift registers and latches are set to “0”.
- The digital dimming duty cycle is set to “0”.
- All segment outputs are set to Low level.
- $\overline{\text{GRID1}}$ outputs are set to Low level.
- $\overline{\text{GRID2}}$ to $\overline{3}$ outputs are set to High level.

Data Transfer Method

Data can be transferred between the rising edge and the next falling edge of chip select input.

The mode data, segment data and dimming data are written by a serial transfer method. The serial data is input to the shift register at the rising edge of a shift clock pulse.

The mode data (M0 to M2) must be transferred after the segment data and dimming data succeeding.

When the chip select input falls, an internal LOAD signal is automatically generated and data is loaded to the latches.

Function Mode

Function mode is selected by the mode data (M0 to M2). The relation between function mode and mode data is as follows:

FUNCTION MODE	OPERATING MODE	FUNCTION DATA		
		M0	M1	M2
0	Segment Data for $\overline{\text{GRID1-3}}$ Input	0	0	0
1	Segment Data for $\overline{\text{GRID1}}$ Input	1	0	0
2	Segment Data for $\overline{\text{GRID2}}$ Input	0	1	0
3	Segment Data for $\overline{\text{GRID3}}$ Input	1	1	0
4	Digital Dimming Data Input	0	0	1

Segment Data Input [Function Mode: 0 to 3]

- ML9212 receives the segment data when function mode 0 to 3 are selected.
- The same segment data is transferred to the 3 segment data latches corresponding to $\overline{\text{GRID1}}$ to $\overline{3}$ at the same time when the function mode 0 is selected.
- The segment data is transferred to only one segment data latch corresponding to the specified GRID when the function mode is 1, 2 or 3 is selected.
- Segment output (SEG1 to 32) becomes High level (lightning) when the segment data (S1 to S32) is set to “1”.

[Data Format]

Input Data : 35 bits
Segment Data : 32 bits
Mode Data : 3 bits

Bit	1	2	3	4	-----	29	30	31	32	33	34	35
Input DATA	S1	S2	S3	S4	-----	S29	S30	S31	S32	M0	M1	M2
← Segment Data (32 bits) →										← Mode Data (3 bits) →		

[Bit correspondence between segment output and segment data]

SEG n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Segment data	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
SEG n	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Segment data	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32

Digital Dimming Data Input [Function Mode: 4]

- ML9212 receives the digital dimming data when function mode 4 is selected.
- The output duty changes in the range of 0/1024 (0%) to 1016/1024 (99.2%) for each grid.
- The 10-bit digital dimming data is input from LSB.

[Data Format]

Input Data : 13 bits
 Digital Dimming Data : 10 bits
 Mode Data : 3 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13
Input DATA	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	M0	M1	M2
LSB Digital Dimming Data (10 bits) MSB Mode Data (3 bits)													

(LSB) Dimming Data (MSB)										Duty Cycle
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
0	0	0	0	0	0	0	0	0	0	0/1024
1	0	0	0	0	0	0	0	0	0	1/1024
⋮										⋮
1	1	1	0	1	1	1	1	1	1	1015/1024
0	0	0	1	1	1	1	1	1	1	1016/1024
1	0	0	1	1	1	1	1	1	1	1016/1024
⋮										⋮
1	1	1	1	1	1	1	1	1	1	1016/1024

Master Mode

Master Mode is selected when $M/\overline{S}$ pin is set at High level. The master mode operation is as follows:

- The input levels of DIM IN, SYNC IN1 and SYNC IN2 are ignored, and these pins should be connected to L-GND or V_{DD} .
- The pulse width of $\overline{GRID1}$ to $\overline{3}$ and SEG1 to 32 are controlled by the internal digital dimming circuit.
- The segment Latch1 to 3 corresponding to $\overline{GRID1}$ to $\overline{3}$ are selected by the internal timing generator.

Slave Mode

Slave Mode is selected when $\overline{M/\overline{S}}$ pin is set at Low level. The slave mode operation is as follows:

- The internal dimming circuit is ignored.
- The pulse width of SEG1 to 32 are controlled by the pulse width of DIM IN signal.
- The segment Latch1 to 3 corresponding to $\overline{GRID1}$ to $\overline{3}$ are selected by SYNC IN1 and SYNC IN2 signals.
- The output levels of $\overline{GRID1}$ to $\overline{3}$ are set at High level. The output levels of DIM OUT, SYNC OUT1 and SYNC OUT2 are set at Low level.

[Correspondence between SYNC IN1, 2 and Segment Latch1 to 3]

SYNC IN 1	SYNC IN 2	Segment Latch	GRID
0	0	No	No
1	0	Latch1	$\overline{GRID1}$
0	1	Latch2	$\overline{GRID2}$
1	1	Latch3	$\overline{GRID3}$

[Correspondence between DIM IN and SEG1 to 32]

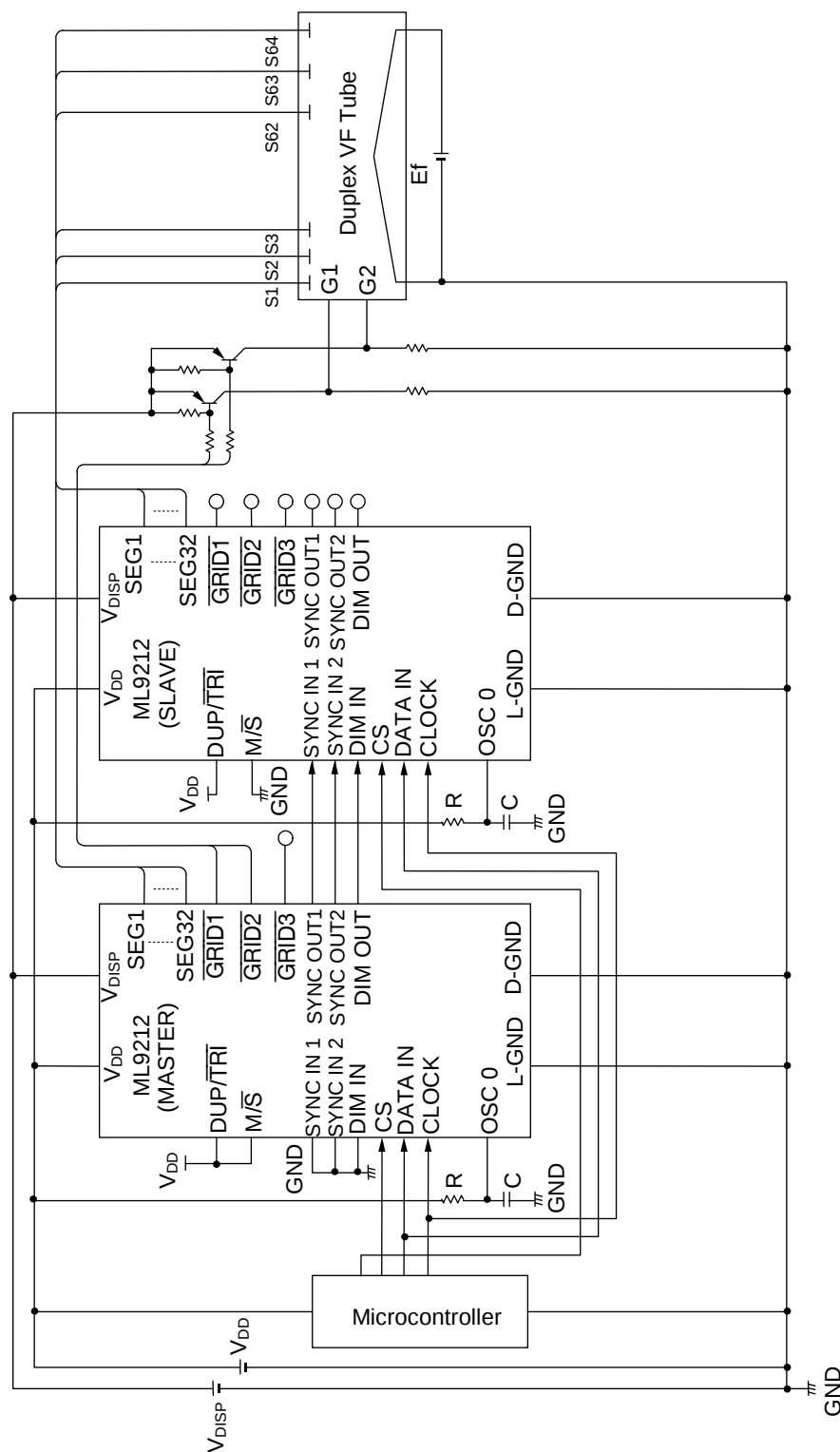
DIM IN	SEG1 to 32
0	Low
1	High

Note: Low: Lights OFF

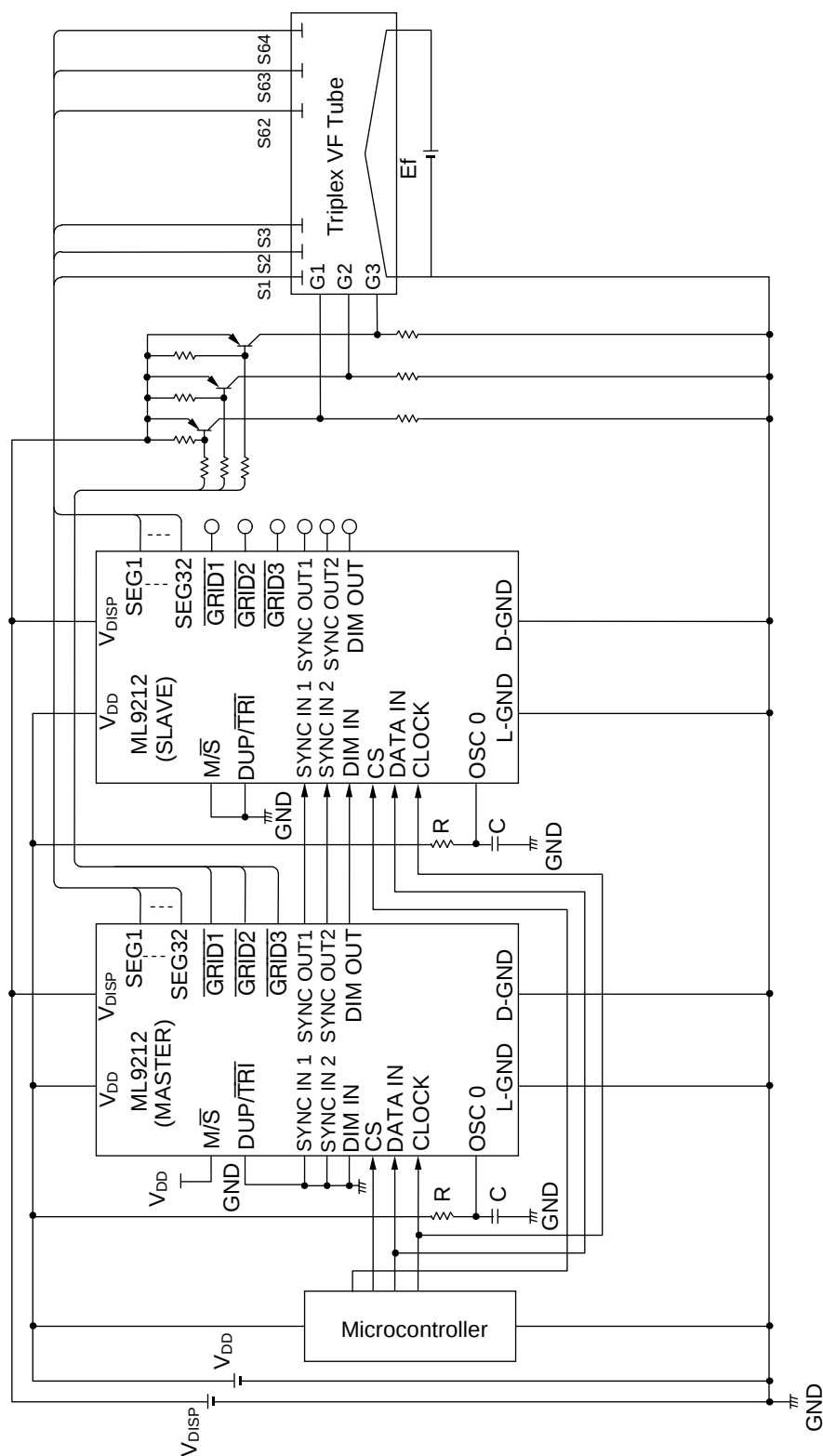
High: Lights ON

APPLICATION CIRCUITS

1. Circuit for the duplex VFD tube with 128 segments (2 Grid × 64 Anode)

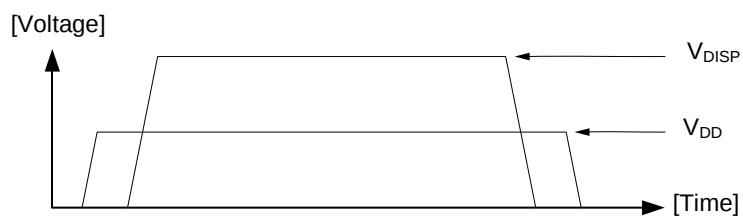


2. Circuit for the triplex VFD tube with 192 segments (3 Grid × 64 Anode)



NOTES ON TURNING POWER ON/OFF

- Connect L-GND and D-GND externally to be an equal potential voltage.
- To avoid wrong operations, turn on the driver power supply after turning on the logic power supply. Conversely, turn off the logic power supply after tuning off the driver power supply.



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9212-01	Nov., 26, 2002	–	–	Final edition 1

NOTICE

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

Copyright 2002 - 2011 LAPIS Semiconductor Co., Ltd.