ML9478C

Static, 1/2 Duty, 1/3 Duty, 1/4 Duty 80 Outputs LCD Driver

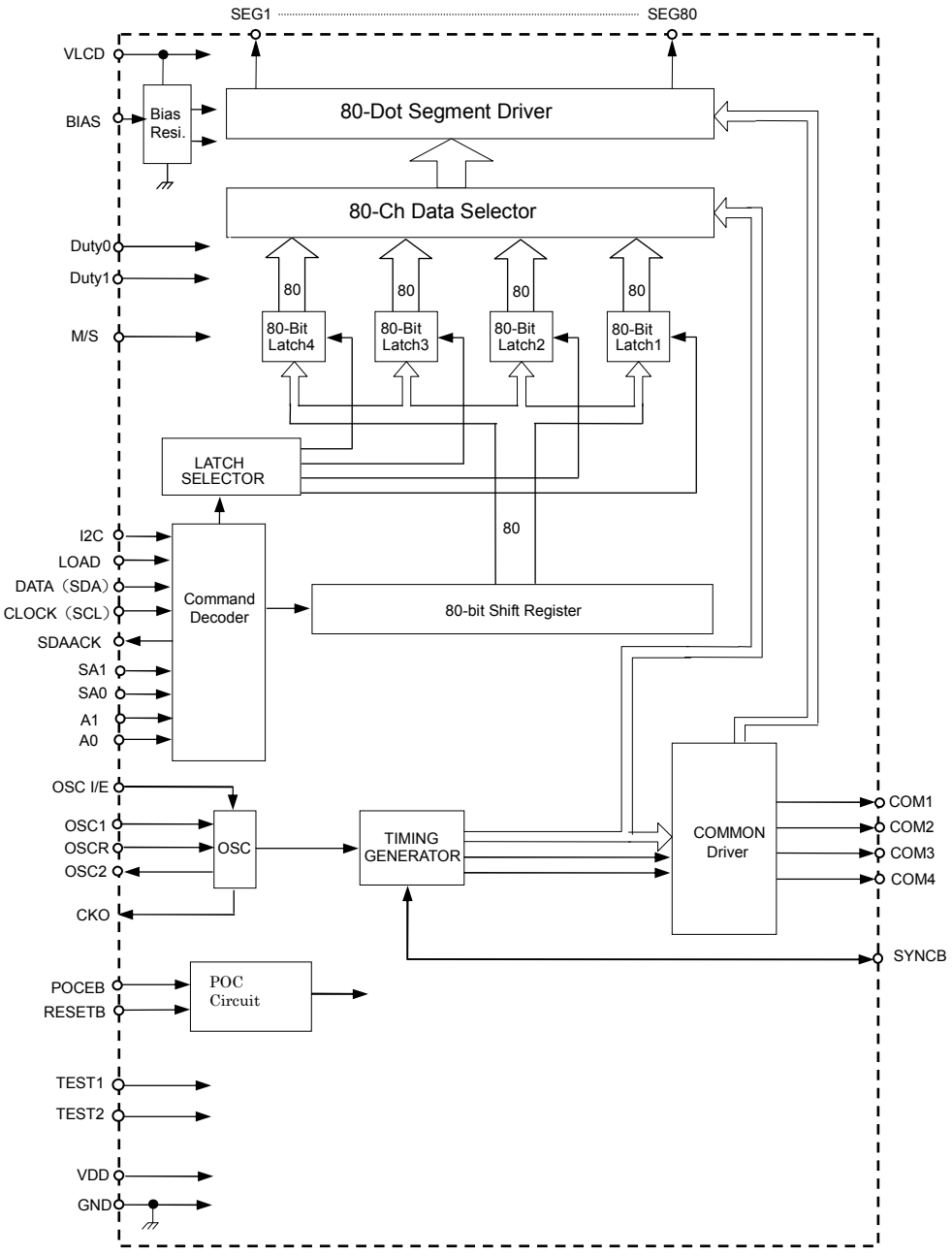
GENERAL DESCRIPTION

The ML9478C is an LCD driver LSI, consists of a 80-bit shift register, a 320-bit data latch, 80 sets of LCD drivers, and a common signal generation circuit.
It can directly drive an LCD up to 80 segments for static display, 160 segments for 1/2-duty display, 240 segments for 1/3-duty display, and 320 segments for 1/4-duty display.
The three-wire serial interface and I^2C interface are selectable.

FEATURES

- Logic power supply voltage : 2.7 to 5.5 V
- LCD drive power supply voltage : 4.5 to 5.5 V
- Maximum number of segments
  Static display : 80 segments
  1/2-duty display : 160 segments
  1/3-duty display : 240 segments
  1/4-duty display : 320 segments
- Interface with microcomputer :
  Serial interface : DATA, CLOCK, LOAD
  CLOCK transfer speed up to 1 MHz
  I^2C interface : SDA, SCL, SDAACK
  SCL transfer speed up to 400 kHz
- Built-in CR oscillator circuit using the internal resistor or External resistor
- Cascade connectable (up to sixteen chips)
- Built-in common signal generation circuit
- Built-in common output intermediate-value voltage generation circuit
- Built-in POC (Power On Clear) circuit
- Gold bump chip (ML9478CDVWA)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	Ta = 25°C	-0.3 to 6.0	V
LCD drive power supply voltage	V_{LCD}	Ta = 25°C	-0.3 to 6.0	V
Input voltage	V_I	Ta = 25°C	– 0.3 to V_{DD} + 0.3	V
Output short-circuit current	Is	Ta = 25°C	-2.0 to +2.0	mA
Chip temperature	Tc —		125 °C	
Storage temperature	T_{STG}	— -55	to +150	°C

Note: Do not use the ML9478C by short-circuiting one output pin to another output pin as well as to other pin (input pin, input/output pin, or power supply pin).

RECOMMENDED OPERATION CONDITIONS

Item	Symbol	Condition	Range	Unit
Logic power supply voltage	V_{DD}*	—	2.7 to 5.5	V
LCD drive power supply voltage	V_{LCD}*	—	4.5 to 5.5	V
OSC IN clock frequency	f_{CP1}	—	up to 10	kHz
Data clock frequency	f_{CP2}	—	up to 1.0	MHz
SCL clock frequency	f_{SCL}	—	up to 400	kHz
Operating temperature	T_a	—	-40 to +105	°C

Note(*): Use at $V_{DD} \leq V_{LCD}$.

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$f_{FRM} = f_{OSC} /24$

Recommended setting range for external component (oscillator circuit)

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta= –40 to +105°C)

Item	Symbol	Condition	Min T	YP	Max	Unit
Oscillation resistor	R_f	—	423	470	517	kΩ
Frame frequency	f_{FRM}	(F1,F0)=(0,1)	47	75	114	Hz

The relation between oscillation resistor and frame frequency is as the equation below.

$f_{FRM} = f_{OSC} /(16 \times 24)$

fosc = 1 / (Device coefficient x External resistor R_f)

Device coefficient = $73.8 \times 10^{-12} \pm 25\%$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta= -40 to +105°C)

Item		Symbol	Condition	Min. T	yp.	Max.	Unit	Applicable pin
"H" input voltage		V_{IH}	— 0.8V	DD	— V	DD V		(*1)
"L" input voltage		V_{IL}	— GND		—	0.2V_{DD}	V	(*1)
Input leakage current 1		I_{L1}	V_I = V_{DD} or 0 V	-1.0 —		1.0	µA	(*1)
Input leakage current 2		I_{L2}	V_I = V_{DD} or 0V POCEB="H"	-1.0	— 1.0		µA	RESET B
Pull-up current		I_{pu}	V_{DD} = 5.0V,V_I = 0 V POCEB = "L"	30	— 140		µA	RESET B
"H" output voltage		V_{OH}	I_O = -600uA	0.9V_{DD}	— —		V	CKO, SYNCB
"L" output voltage 1		V_{OL1}	I_O = 600uA	—	—	0.1V_{DD}	V	CKO, SYNCB
"L" output voltage 2		V_{OL2}	I_O = 600uA	—	—	0.1V_{DD}	V	SDAACK
Driver ON resistor	Segment	V_{OHS}	V_{LCD} = 5V	— 5		15	kΩ	SEG1 to SEG80
	Common	V_{OHC}	V_{LCD} = 5V	— 5		12	kΩ	COM 1 to COM4

(*1) : DATA(SDA), CLOCK(SCL), LOAD, M/S, SYNCB, Duty1, Duty0, BIAS, SA1,SA0, A1, A0, OSC1, OSC I/E, I2C, POCEB

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta= -40 to +105°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Static supply current	I_{DDS}	V_{DD}=V_{LCD}=5.5 V Input pin fixed to "H" or "L" Oscillation stopped, output no-load POCEB="L"		— 8		15	µA	VDD
	I_{LCDS}			— 9		15	µA	VLCD
Dynamic supply current 1	I_{DD1}	V_{DD}=V_{LCD}= 5.5 V (*2)(*3) Clock OSC1 external input f_{CP1}=1.8kHz	(*6)	— 10		18	µA	VDD
	I_{LCD1}		(*7)	— 9		15	µA	VLCD
Dynamic supply current 2	I_{DD2}	V_{DD}=V_{LCD}= 5.5 V (*2)(*3) Internal oscillation	(*6)	— 61		90	µA	VDD
	I_{LCD2}		(*7)	— 9		15	µA	VLCD
Dynamic supply current 3	I_{DD3}	V_{DD}=V_{LCD}= 5.5 V (*2)(*4)(*6) Internal oscillation At three-wire serial IF data input		—	130	250	µA	VDD
	I_{LCD3}			— 9		15	µA	VLCD
Dynamic supply current 4	I_{DD4}	V_{DD}=V_{LCD}= 5.5 V (*2)(*5)(*6) Internal oscillation At I^2C IF data input		—	202	330	µA	VDD
	I_{LCD4}			— 9		15	µA	VLCD

(*2) : M/S = "H", 1/4-duty, 1/3-bias, (F1,F0) = (1,1) 95 Hz, POCEB = "L", output pin no-load.
(*3) : Three-wire serial or I^2C interface. Input pin fixed to "H" or "L".
(*4) : Serial interface, data input frequency = 1 MHz.
(*5) : I^2C interface, data input frequency = 400 kHz.
(*6) : Alternately inputs "0" and "1" for LCD display data (checkered display).
(*7) : Inputs all "1s" for LCD display data (all illuminated).

Switching Characteristics

- OSC timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
OSC IN clock frequency (external input)	f_{CP1}	Clock input from OSC1. OSC2 and OSCR open. OSC I/E = "L"	—	1.8	10	kHz	OSC1
Clock pulse width (External input)	t_{WCP1}		40	—	—	µs	OSC1
Clock rise and fall time (external input)	t_{OSC}		—	— (*1)		µs	OSC1
External Rf clock frequency (Internal oscillation)	f_{OSC1}	Between OSC1 and OSC2 R_f = 470kΩ (F1,F0)=(0,1) OSCR open. OSC I/E = "H"	18	28.8	44	kHz	OSC1 , OSC2
Internal clock frequency (Internal oscillation)	f_{OSC2}	OSC1 open. (F1,F0)=(0,1) OSC2 and OSCR short-circuited. OSC I/E = "H"	18	28.8	44	kHz	OSC1, OSCR, OSC2

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$$f_{FRM} = f_{OSC} / 24$$

(*1) t_{OSC} is a reference value.
The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value. Make the rise as steep as possible. Reference value: max=2µs.

- Serial interface timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Data clock frequency	f_{CP2}		—	—	1	MHz	CLOCK
Data clock pulse width	t_{WCP2}		100	—	—	ns	CLOCK
Data setup time	t_{SU}		50	—	—	ns	DATA
Data hold time	t_{HD}		50	—	—	ns	CLOCK
CLOCK-LOAD timing	t_{CL}		100	—	—	ns	CLOCK
LOAD-CLOCK timing	t_{LC}		100	—	—	ns	LOAD
LOAD pulse width	t_{WLD}		100	—	—	ns	LOAD
Signal rise and fall time	tsr,tsf		—	—	(*2)	ns	CLOCK,DATA, LOAD

(*2) tsr and tsf shall be reference values.
The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value. Make the rise as steep as possible. Reference value: max=10ns.

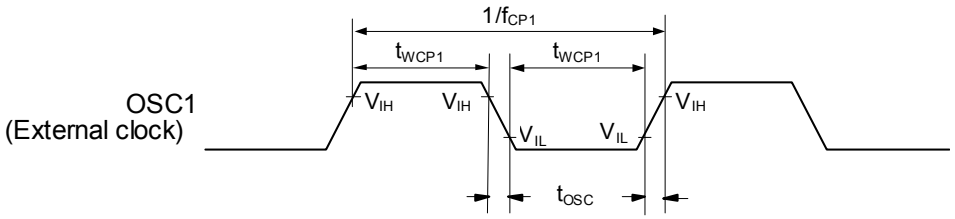
- I^2C interface timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

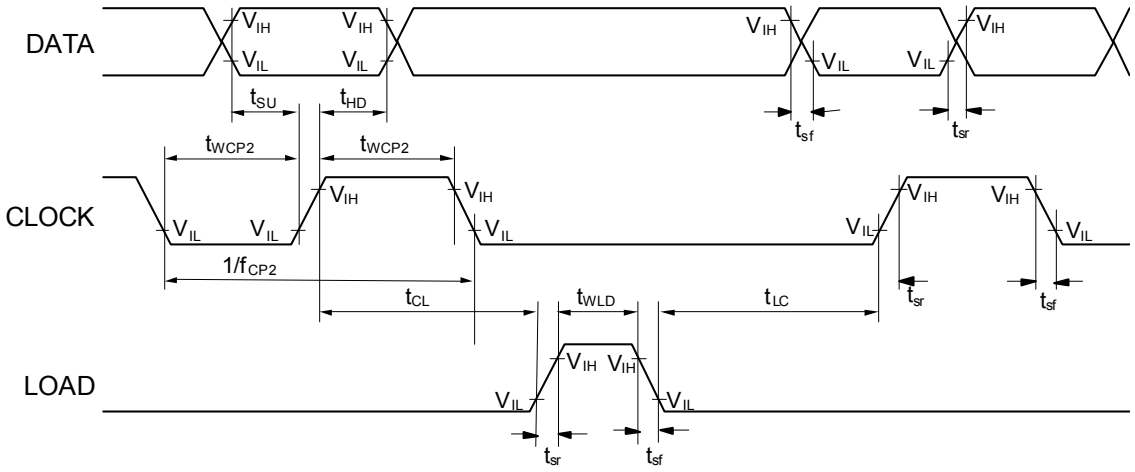
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
SCL clock frequency	f_{SCL}		—	—	400	kHz	SCL
Hold time (repeat) "STATRT" condition	$t_{HD,STA}$		0.6	—	—	µs	SCL,SDA
SCL "L" pulse width	t_{LOW}		1.3	—	—	µs	SCL
SCL "H" pulse width	t_{HIGH}		0.6	—	—	µs	SCL
Setup time for repeat "START" condition	$t_{SU,STA}$		0.6	—	—	µs	SCL,SDA
Data hold time	$t_{HD,DAT}$		0	—	—	ns	SCL,SDA
Data setup time	$t_{SU,DAT}$		200	—	—	ns	SCL,SDA
Setup time for "STOP" condition	$t_{SU,STO}$		0.6	—	—	µs	SCL,SDA
Bus free time between "STOP" condition and "START" condition	t_{BUF}		1.3	—	—	µs	SCL
Data valid acknowledge time	$t_{VD,ACK}$		—	—	1.2	µs	SCL,SDAAACK
Signal rise and fall time	tir,tif		—	—	(*3)	µs	SCL,SDA
Data bus load capacitance	Cb		—	—	400	pF	SDA,SDAACK
Noise pulse width tolerance	t_{wf}		—	—	50	ns	SCL,SDA

(*3) tir and tif shall be reference values.
The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value. Make the rise as steep as possible. Reference value: max=0.1µs.

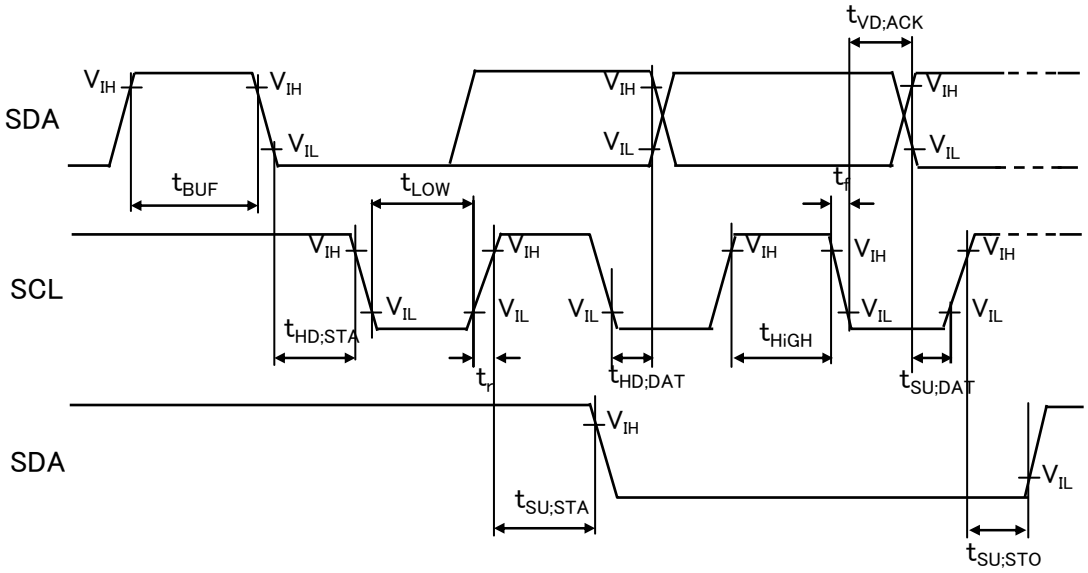
Timing chart (OSC1)



Timing chart (Serial interface)



Timing chart (I^2C interface)



REFERENCE DATA

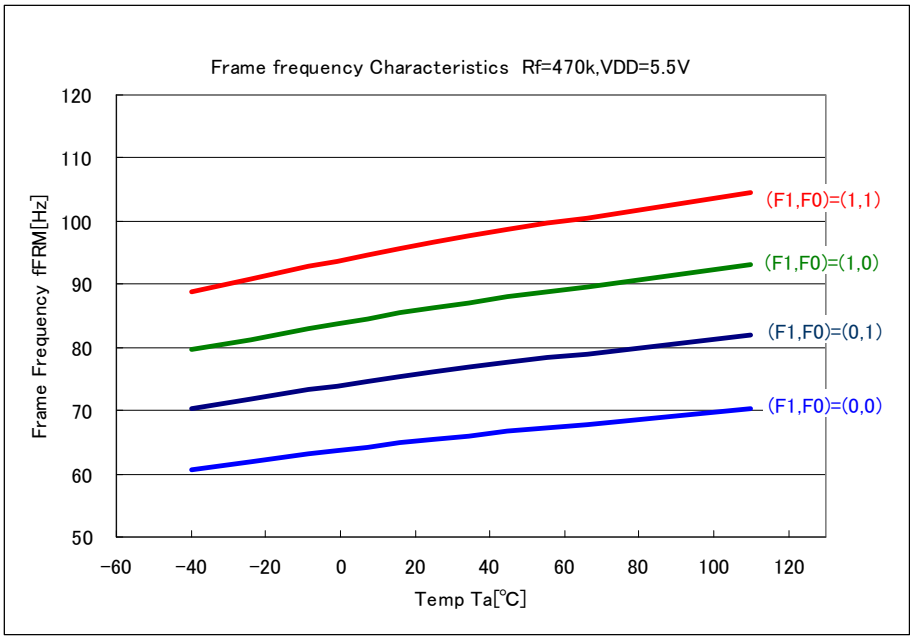
Frame frequency Characteristics

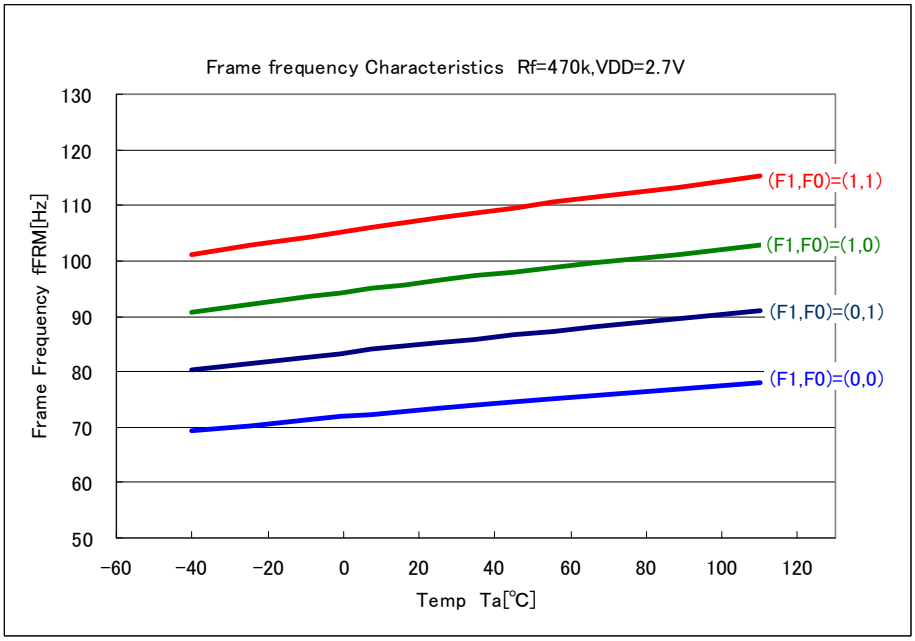
VDD=5.5V/2.7V Rf=470Ω

Frame frequency $f_{FRM} = f_{OSC} /(16 \times 24)$

fosc = 1 / (Device coefficient x External resistor R_f)

Device coefficient = $73.8 \times 10^{-12} \pm 25\%$

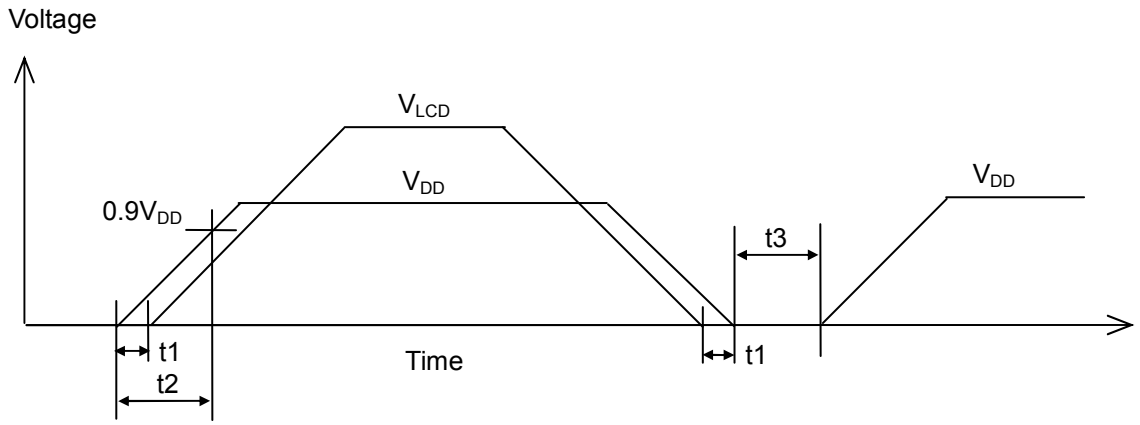




POWER ON/OFF TIMING

To turn on the power supply, raise the logic power supply first, then LCD drive power supply in order to prevent the IC from malfunctioning.
To fall the power supply, fall the LCD drive power supply first, then the logic power supply.
For a VDD pin ranging from 0 V to VDDmin, set VDD ≥ VLCD and t1 ≥ 0 [ns].

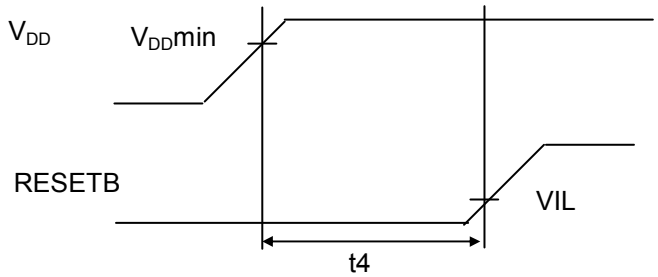
To enable the Internal POC circuit, the VDD power supply rise time t2 range needs to be 100 [µs] ≤ t2 ≤ 500 [ms].
For the VDD power supply to turn OFF then turn ON again, it is necessary to secure the POC discharge time t3 ≥ 100 [ms].



INITIALIZATION SIGNAL TIMING

When RESETB signal is externally input

The RESETB pin input is valid both for POCEB = "L" and "H". Usable in combination with the POC.
Keep the RESETB pin at "L" level until the VDD reaches VDDmin. (t4 ≥ 200[ns])



When Internal POC circuit is used

When using the Internal POC circuit in the initialization, set the POCEB pin to "L".
At this time, the power ON/OFF timing conditions are t1 to t3 above mentioned.

When RESETB pin POC circuit is used

If the power ON/OFF timing conditions t1 to t3 cannot be kept, the RESETB pin needs to have a capacitance to configure the POC circuit. For this case, connect a capacitance value according to the power supply rise time.
For the power supply rise time t2 and external capacitance value, use the following formula as a guide:

$$C_{RST}\ [F] \quad > t2\ [sec] / (30 \times 10^3)$$

PIN DESCRIPTIONS

Pad number	Symbol I/O		Description
67-68 M	/S	I	This is the input to switch between the master and slave modes. It has a schmitt circuit. When this pin is "H", the mode is master. When this pin is "L", the mode is slave.
6-7 4-5	Duty0 Duty1 *1	I	Display duty switch pins. These have schmitt circuits. Duty0="L", Duty1="L" : Static (COM1=COM2=COM3=COM4) Duty0="H", Duty1="L" : 1/2Duty (COM1=COM3, COM2=COM4) Duty0="L", Duty1="H" : 1/3Duty (COM2=COM4) Duty0="H", Duty1="H" : 1/4Duty
73-74 BIAS		I	This pin sets the LCD bias. It has a schmitt circuit. BIAS= "L": 1/3bias BIAS= "H": 1/2bias
14-15 12-13	SA1 SA0	I	Slave address input pins. These have schmitt circuits.
10-11 8-9	A1 A0	I	Sub address input pins. These have schmitt circuits.
71-72 O	SC I/E	I	This input selects whether to use the external clock input mode or to use the Internal oscillation mode or external oscillation mode. It has a schmitt circuit. When this pin is "H", the mode is the Internal or external Rf oscillation mode. When this pin is "L", the mode is the external clock input mode. Use the slave chip as it is connected to GND.
46-48 53-55 49-52	OSC1, OSCR, OSC2 *2	I I O	These pins are for the oscillator circuit to generate common signals. The OSC1 and OSCR pins are input pins and have a schmitt circuit. OSC2 is an output pin. It becomes an output when the OSC I/E pin = "H" and a high impedance when the OSC I/E pin = "L". 【In the master mode (M/S pin ="H") 】 Three types are selectable: Internal oscillation mode, external oscillation mode, and external clock input mode. •Internal oscillation mode: Set the OSC I/E pin to "H", short the OSCR and OSC2 pins, and open the OSC1 pin. •External Rf oscillation mode: Set the OSC I/E pin to "H", connect an oscillation resistor Rf between the OSC1 and OSC2 pins, and open the OSCR pin. •External clock input mode: Set the OSC I/E pin to "L", open the OSCR and OSC2 pins, and input the external clock to the OSC1 pin. 【 In the slave mode (M/S pin ="L") 】 Open the OSCR and OSC2 pins and connect the OSC1 pin to the ML9478C's CKO pin that has been set to the master mode.
56-56	CKO	O	Clock output pin. In the master mode (M/S pin = "H"), the 1/16 division signal of the oscillation frequency is output. In the slave mode (M/S pin = "L"), the output is fixed to "L". For a cascade connection, connect this pin to the OSC1 pin of the chip that has been set to the slave mode.

60-63 SY	NCB	I/O	Input/output pin for common synchronization. It has a schmitt circuit. It becomes the synchronization signal output pin in the master mode (M/S pin = "H"). It becomes the synchronization signal input pin in the slave mode (M/S pin = "L"). For cascade connection, connect all of the involved ML9478Cs' SYNC pins by the common line.
65-66	I2C	I	Interface switching pin. It has a schmitt circuit. When this pin is "H", the interface is I^2C. When this pin is "L", the interface is three-wire serial.
20-21	DATA (SDA)	I	Display data input pin. It has a schmitt circuit. I2C="L": Serial interface; DATA Input the display data in the order of SEG80, SEG79, ... , SEG2, and SEG1. The display data turns on at "H" and turns off at "L". I2C="H": I^2C interface; SDA Input the display data in units of 8 bits. The display data turns on at "H" and turns off at "L". This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
22-23	CLOCK (SCL)	I	Shift clock input pin for display data. It has a schmitt circuit. I2C="L": Serial interface; CLOCK The display data input to the DATA pin is serially input to the shift register at the CLOCK signal rise. I2C="H": I^2C interface; SCL The display data input to the SDA pin is serially input to the shift register at the SCL signal rise. This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
24-25	LOAD	I	Input pin for the load signal of display data. It has a schmitt circuit. I2C="L": Serial interface; LOAD The display data in the shift register is transmitted as is to the segment driver for the "H" duration. When this pin is brought into "L", the shift register is disconnected from the segment driver. The display data in the shift register immediately before it become "L" is held in the data latch and transmitted to the segment driver. I2C="H": I^2C interface Use this pin as it is connected to GND.
17-19	SDAACK	O	I2C="L": Serial interface Use this pin as it is opened. I2C="H": I^2C interface The I^2C bus acknowledge output signal. Normally, use it as it is connected with the SDA pin. Connect an external pull-up resistor whenever necessary, as it is an open drain pin. The pull-up connection destination supply voltage shall be the V_{DD} supply voltage or less.
69-70	POCEB	I	Internal POC circuit enable pin. It has a schmitt circuit. When this pin is "H", the POC circuit becomes OFF and the constant current (8µA) is cut. The RESETB pin pull-up resistor is cut as well. When this pin is "L", the POC circuit becomes ON. The RESETB pin is connected to a pull-up resistor.
44-45	RESETB *3	I	Reset signal input pin for initializing inside the IC. It has a schmitt circuit. The "L" level enables the reset. This pin has an Internal pull-up resistor. Open when POCEB = "H". Pull-up when POCEB = "L". The power-on reset operation is available by connecting an external capacitor.

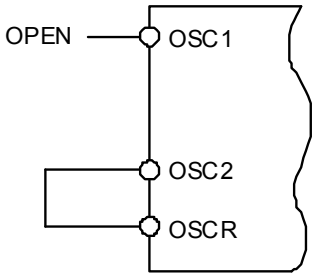
77-78 75-76	TEST1 TEST2	I	Pin for testing the IC. It has an Internal pull-down resistor. Use it as it is connected to GND.
95-134 139-178	SEG1 ~SEG80	O	Outputs for LCD display. Connected to the segment pins on the LCD panel. In the display off mode, all the outputs are fixed to GND.
85-88 135-138 183-186	COM1 ~COM4	O	Outputs for LCD display. Connected to the common pins on the LCD panel. The output pins are located at three positions: both ends of the chip and between SEG40 and SEG41. Each is connected inside the chip. Use the COM pins in accordance with the panel to be used. In the display off mode, all the outputs are fixed to GND. When the slave is set (M/S="L"), COM1 to COM4 outputs are GND level fixed.
32-37	VDD	-	Power supply pin for logic circuit.
38-43	VLCD	-	Power supply pin for LCD driver.
26-31 G	ND	-	Ground pin.
16 64	VDDO -		VDD output pin. Use this pin when fixing the mode setting input pin to "H" on the COG.
3 79	GNDO -		Ground output pin. Use this pin when fixing the mode setting input pin to "L" on the COG.
1-2 80-84 89-94 179-182 187-190	DUMMY -		Floating pin. At this time, avoid this pin from shorting with pins other than DUMMY in the wiring on the COG.

*1: For details of the COM /SEG waveform when a duty is selected, refer to "Common waveform" on page 18 and "Common Segment waveform" on page 19 to 23.

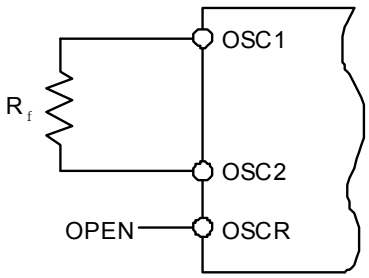
*2: Oscillator circuit configuration

• When M/S = "H", OSC I/E = "H"

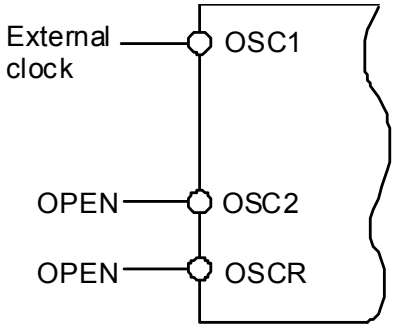
[Internal Rf oscillation mode]



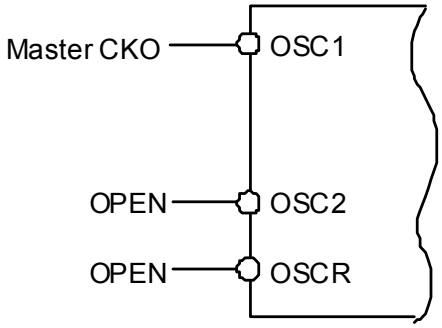
[External Rf oscillation mode]



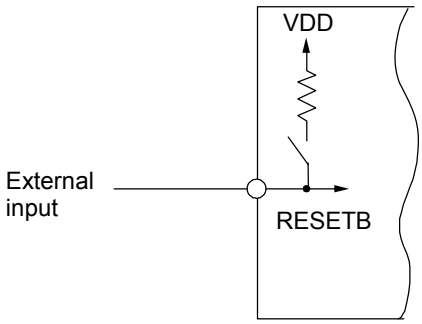
• External clock input mode when M/S = "H" and OSC I/E = "L"



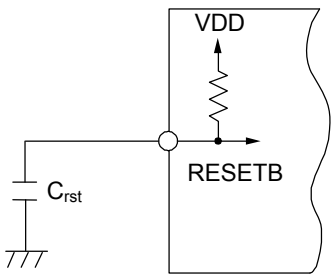
• M/S = "L", slave mode, external clock input mode



*3: Reset circuit configuration
• External input to RESTB when POCEB = "H"



• POC circuit configuration when POCEB = "L"

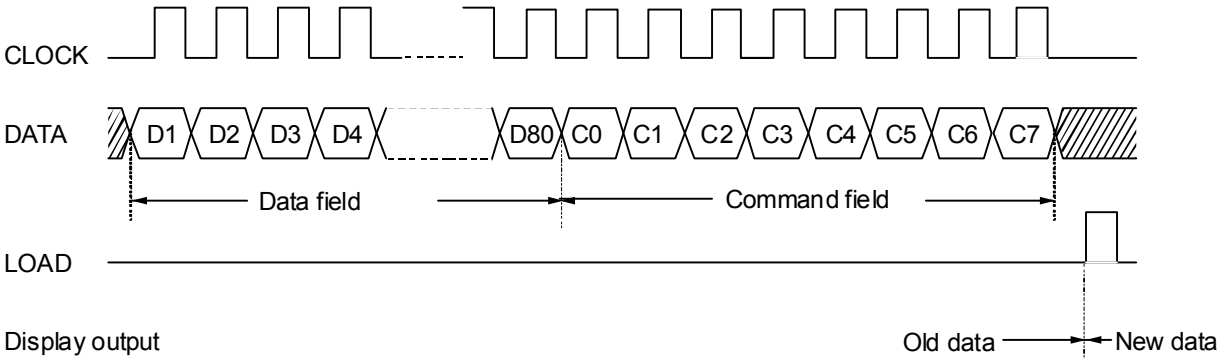


DESCRIPTION

Operation description (Serial interface)

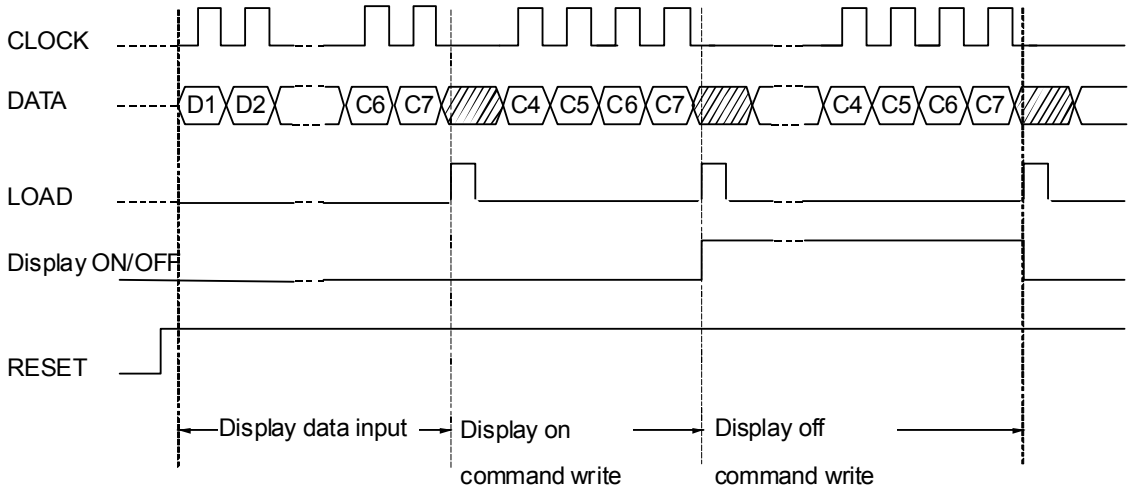
• Display data input

As described in the Data configuration section, the display data consists of the data field that corresponds to each segment on/off and the command field that indicates the display data input.
When inputting the display data, the "F3" command is set in the command field. When the "F1" or "F2" command is set in the command field, the display data in the data field becomes invalid.
The data input to the DATA pin is loaded to the shift register at the CLOCK pulse rise, transferred to the display data latch during the LOAD pulse at the "H" level, then output via the segment driver.



• Display on, Display off

The display becomes off at power-on reset. To display, write the display on command.
The display off is the command that makes all segments off. Writing the display off command turns off the lights regardless of the display data.
The display on is the command to release the display off. Writing the display on command returns the display to the original state.



List of Commands

Command name	C7	C6	C5	C4	C3	C2	C1	C0	Operation
F0	0	0	0	0	x	x	x	x	Disabled
F1	0	1	F1 (*2)	F0 (*2)	x	x	x	x	Frame frequency setting (F1,F0)=(0, 0): 65Hz (F1,F0)=(0, 1): 75Hz (F1,F0)=(1, 0): 85Hz (F1,F0)=(1, 1): 95Hz (valid for Internal CR oscillation)
F2	1	0	1	D (*2)	x	x	x	x	Display on/off "0" : Off (COM=SEG=GND) "1" : On
F3(*1)	1	1	SA1	SA0	A1	A0	Co1	Co0	Data write address setting (Co1,Co0)=(0, 0): Corresponding to common 1 (Co1,Co0)=(0, 1): Corresponding to common 2 (Co1,Co0)=(1, 0): Corresponding to common 3 (Co1,Co0)=(1, 1): Corresponding to common 4 SA1, SA0, A1, A0: Chip address

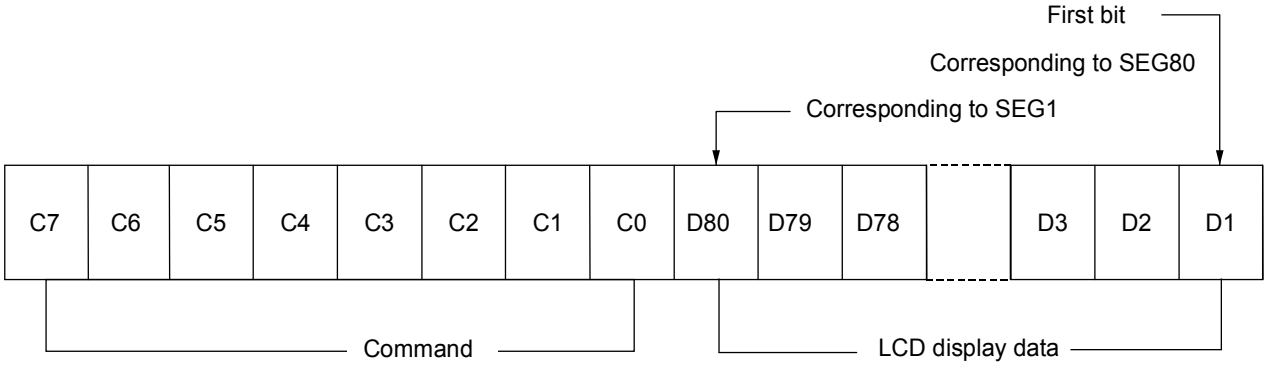
x : Don't care

(*1): For the I^2C interface, SA1 and SA0 are set at a slave address.
These bits become "Don't care".

(*2): The register is set to the following value by the RESETB = "L" input or by the power-on POC.
F1="0", F0="0", D="0"

Data configuration

• Data configuration (Serial interface)

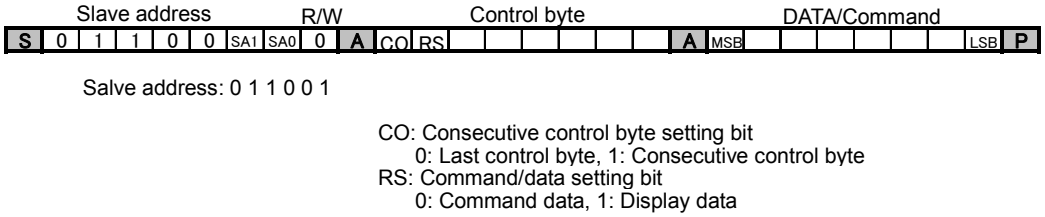


Note 1 : The commands F1 and F2 settings become valid when the least four bits of C4 to C7 are input.
(The bits from D1 to D80 and from C0 to C3 are not necessary.)

Note 2 : If the dummy bit is needed for the reason of number of transfer bits, put it on the first bit side.

Note 3 : The command execution follows the contents of the C7 to C0 registers immediately before the LOAD becomes "H".

• Data configuration (I^2C interface)



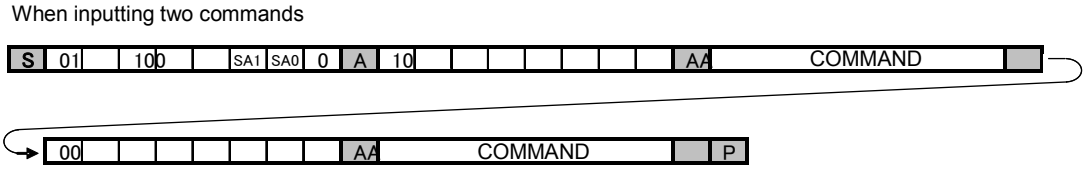
For the I^2C interface, each IC is assigned with a 7-bit slave address. The first one byte in the transfer consists of this 7-bit slave address and the R/W bit that indicates the data transfer direction. Always input "0" to the eighth R/W bit because the ML9478C is a write-only LSI.
The eight bits next to the slave address is a control byte. The first one bit is CO: consecutive command setting bit and the next one bit is RS: command/data setting bit (the remaining six bits are the Don't care bits).

When CO = "0": Means the last control byte.
When CO = "1": Means the control bytes are successively input.
When RS = "0": Means the data to be input next is the command data.
When RS = "1": Means the data to be input next is the display data.

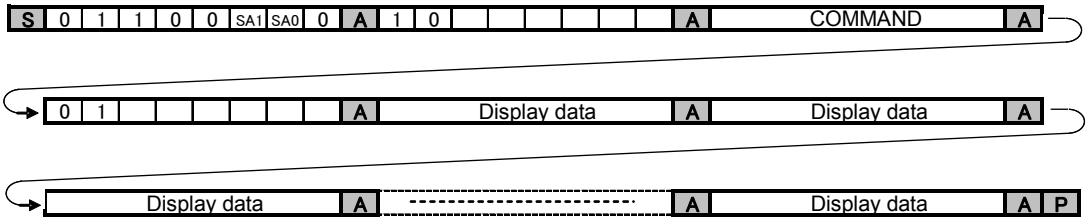
The display data can be successively input.

Example of Data Setting

- When inputting two commands



- When inputting the command and display data



Data write method

• Serial interface

The data is written to the address set by the data write setting command (F3).
For the Serial interface, the data is written in units of 80 bits.
Written from D80 to SEG1, D79 to SEG2, ... , D2 to SEG79, and D1 to SEG80.

	MSB Segment output												LSB
	1	2	3	4	32	33	34	35	36	37	38	39	40
COM1	D80	D79	D78	D77	D49	D48	D47	D46	D45	D44	D43	D42	D41
COM2	D80	D79	D78	D77	D49	D48	D47	D46	D45	D44	D43	D42	D41
COM3	D80	D79	D78	D77	D49	D48	D47	D46	D45	D44	D43	D42	D41
COM4	D80	D79	D78	D77	D49	D48	D47	D46	D45	D44	D43	D42	D41

	MSB Segment output											LSB
	41	42	43	44	72	173	74	75	76	77	78	79	80
COM1	D40	D39	D38	D37	D9	D8	D7	D6	D5	D4	D3	D2	D1
COM2	D40	D39	D38	D37	D9	D8	D7	D6	D5	D4	D3	D2	D1
COM3	D40	D39	D38	D37	D9	D8	D7	D6	D5	D4	D3	D2	D1
COM4	D40	D39	D38	D37	D9	D8	D7	D6	D5	D4	D3	D2	D1

• I^2C interface

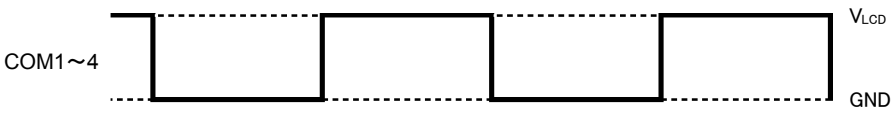
The data is written to the address set by the slave address.
For the I^2C interface, the data is written to the specified address starting with the LSB side in units of 8 bits.
(The data is written in the order from SEG73-80, SEG65-SEG72, ... , SEG9-16, and SEG1-SEG8.)

	LSB Segment output												MSB
	1	2	3	4	32	33	34	35	36	37	38	39	40
COM1	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8
COM2	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8
COM3	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8
COM4	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8

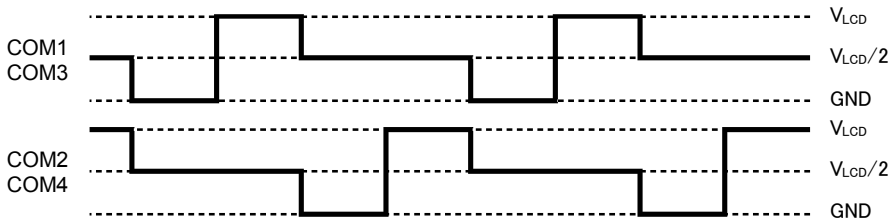
	LSB Segment output												MSB
	41	42	43	44	72	73	74	75	76	77	78	79	80
COM1	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8
COM2	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8
COM3	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8
COM4	D1	D2	D3	D4	D8	D1	D2	D3	D4	D5	D6	D7	D8

● Common waveforms

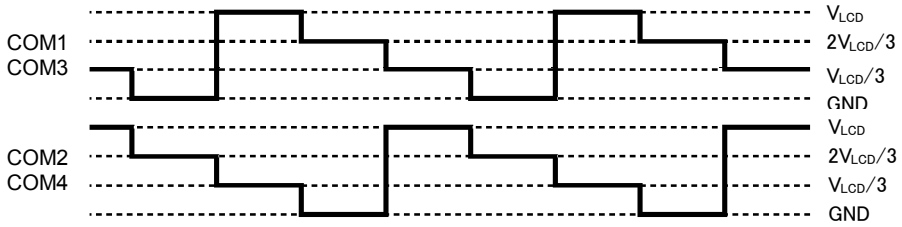
(1) At static



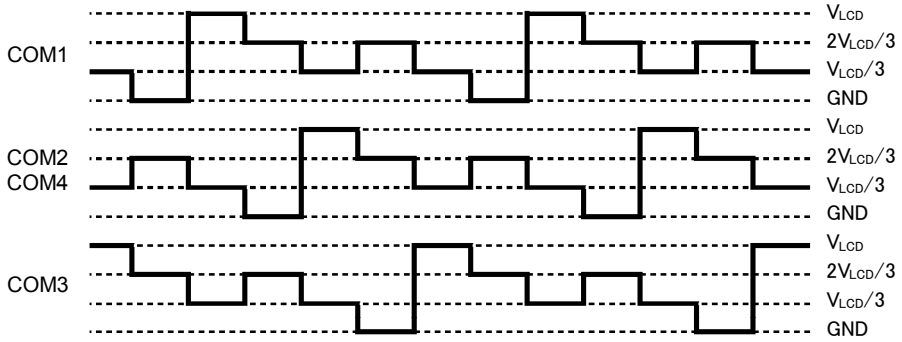
(2) At 1/2-duty
At 1/2-bias



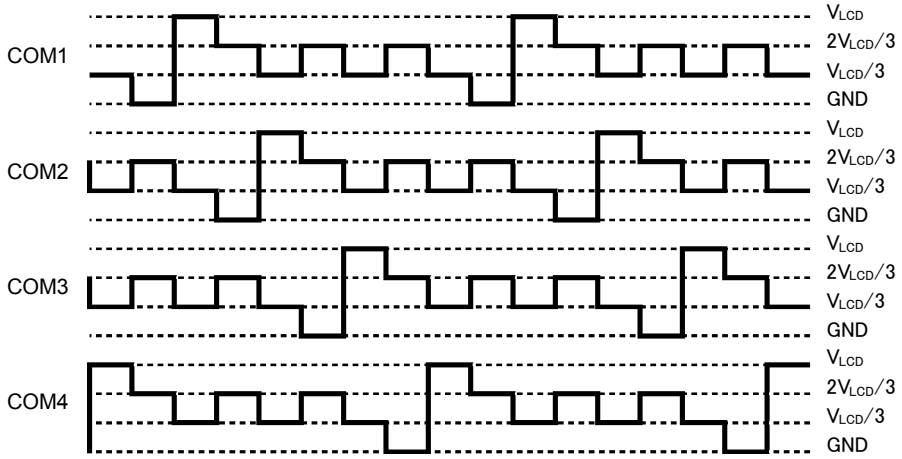
At 1/3-bias



(3) At 1/3-duty

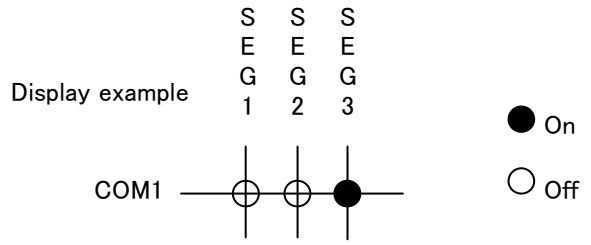


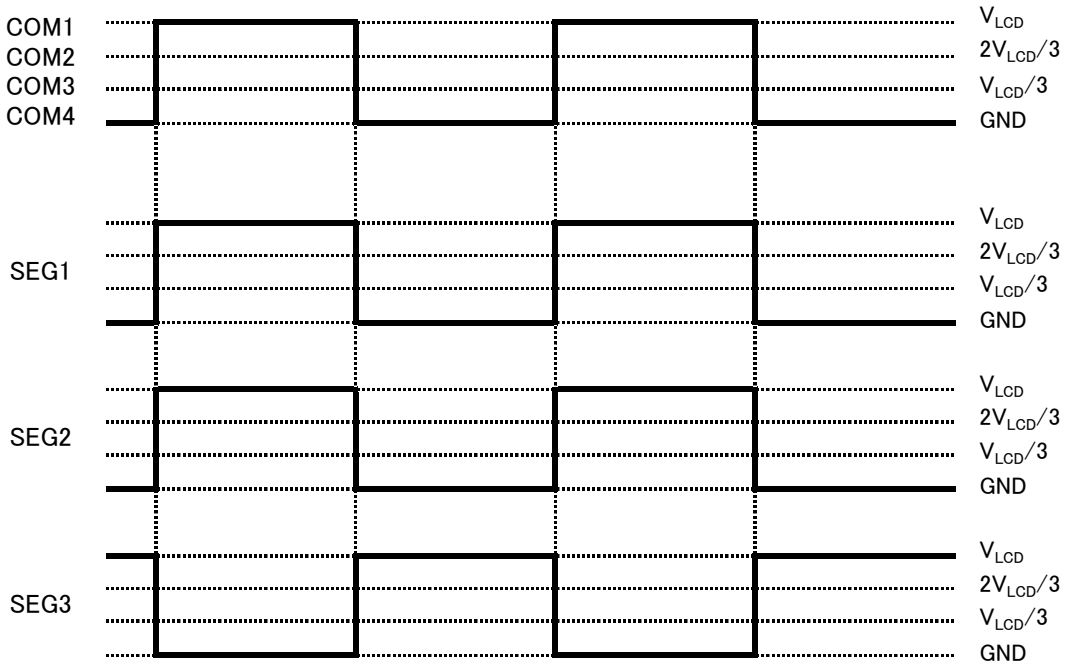
(4) At 1/4-duty



● Common segment output waveform

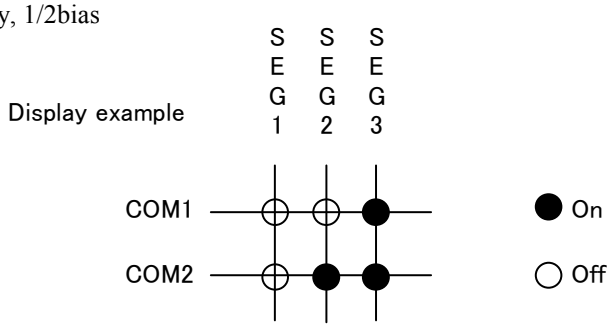
・At Static

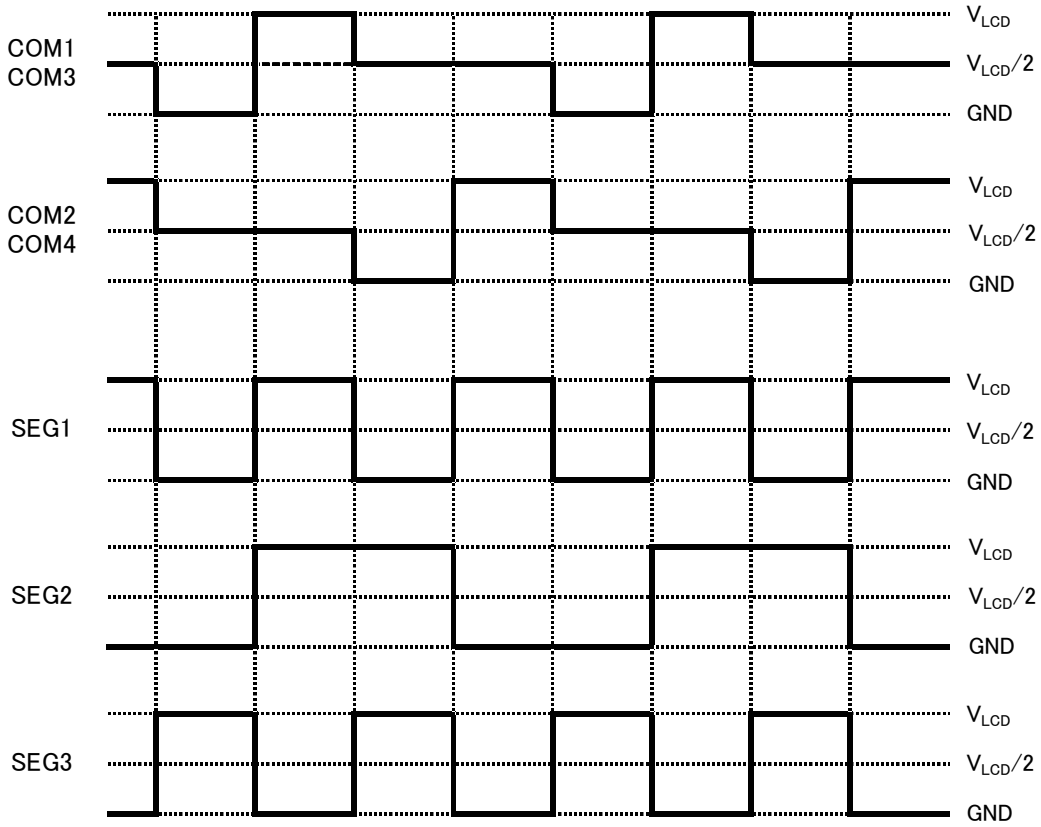




● Common and segment output waveforms

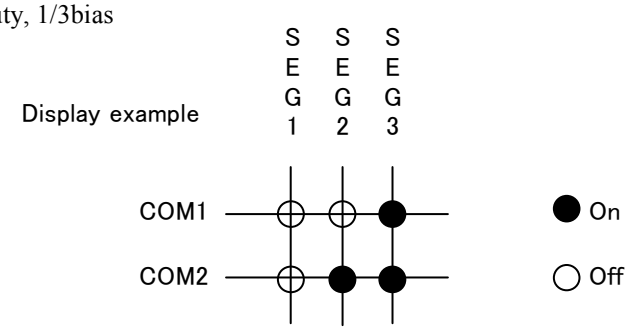
・At 1/2Duty, 1/2bias

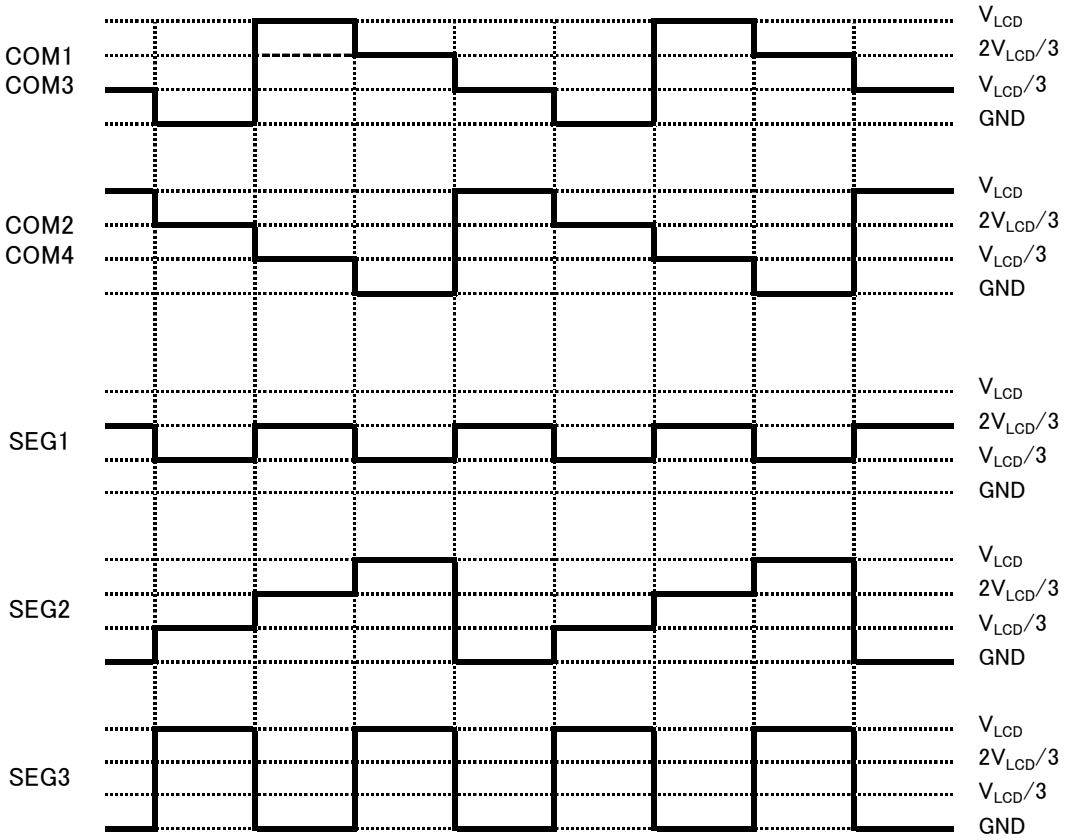




● Common and segment output waveforms

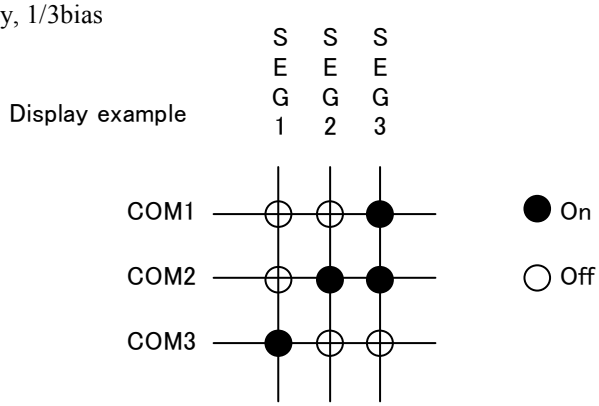
・At 1/2Duty, 1/3bias

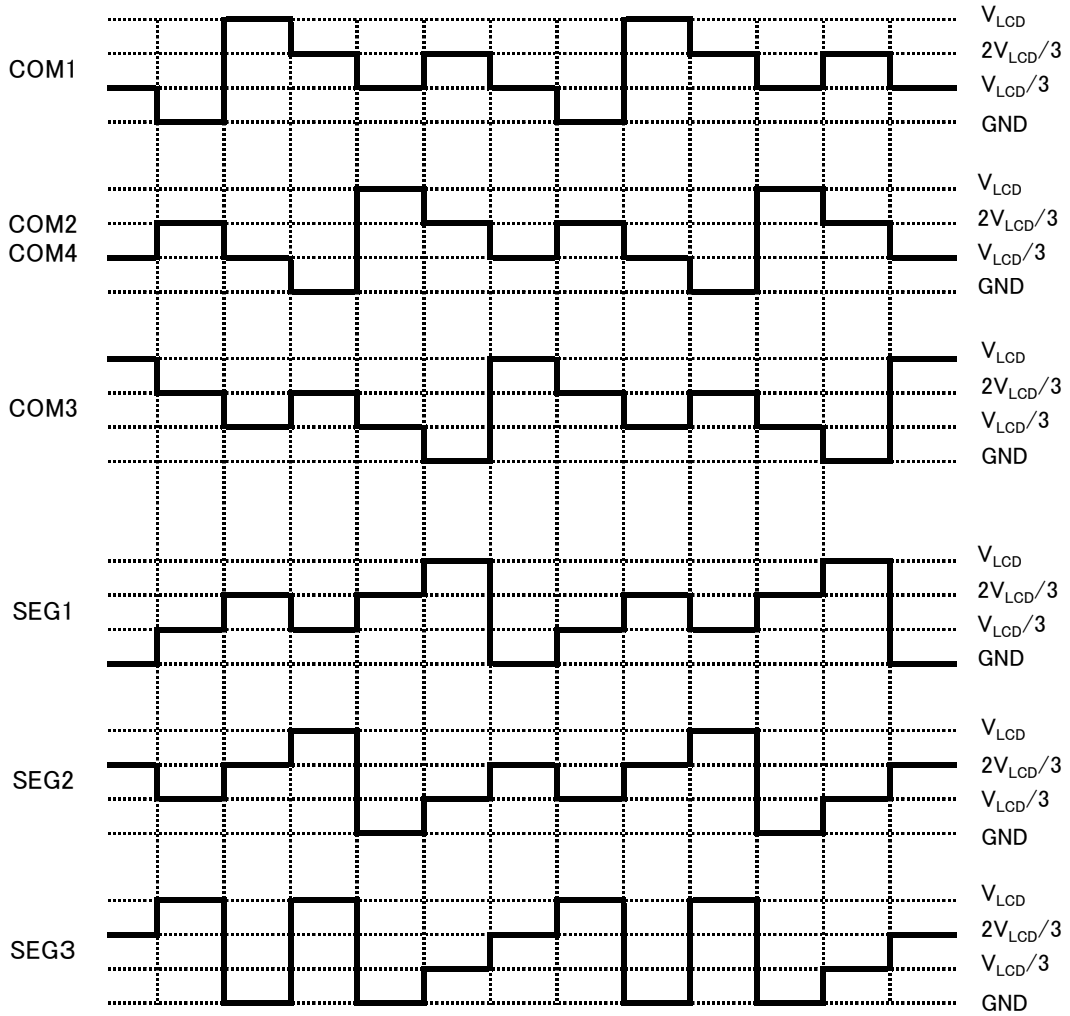




● Common and segment output waveforms

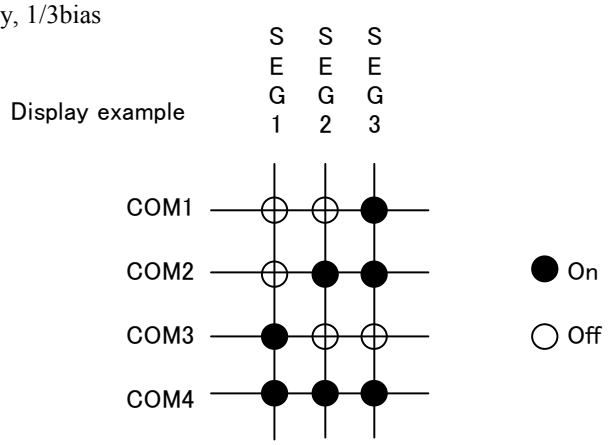
・At 1/3Duty, 1/3bias

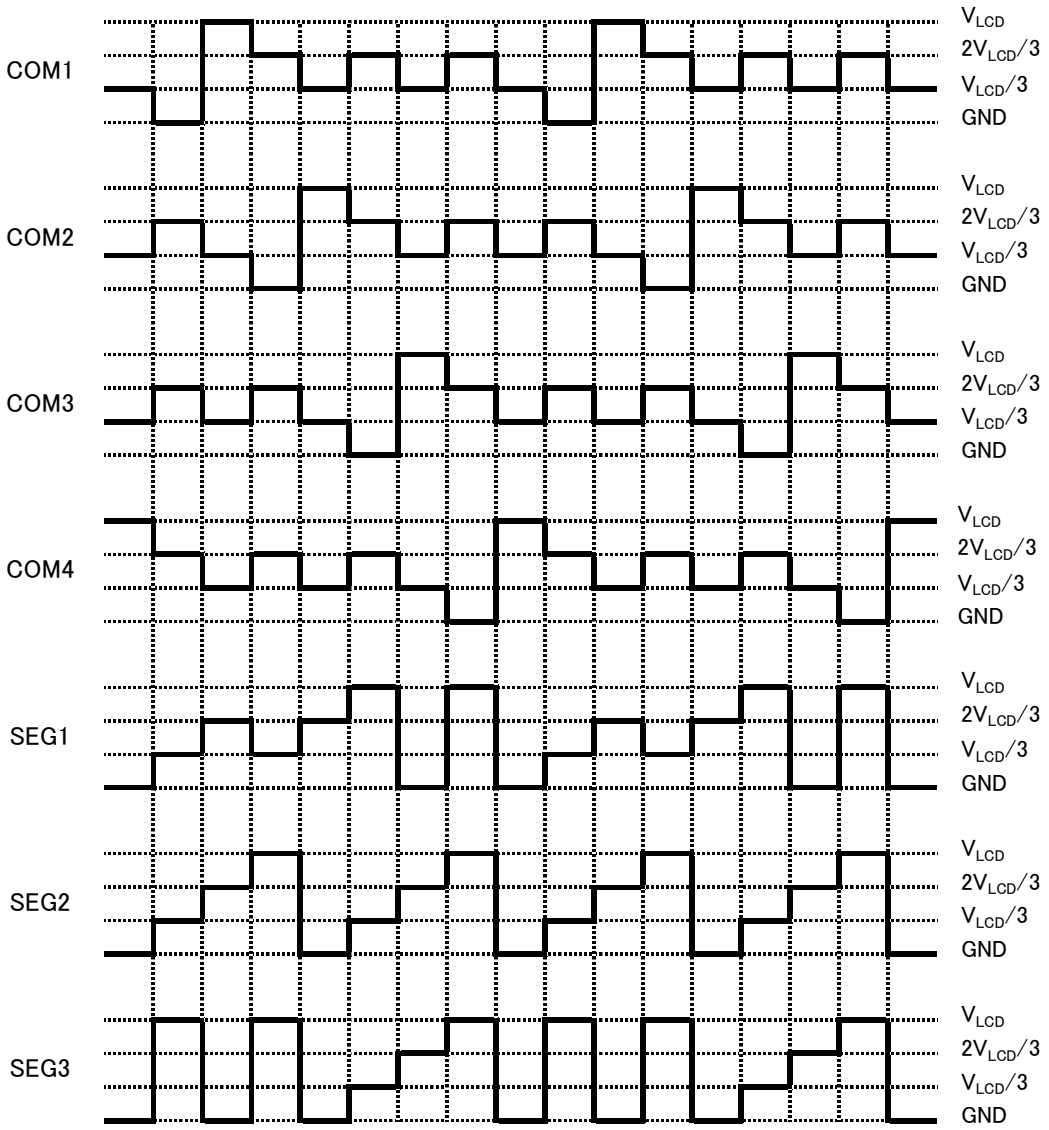




● Common and segment output waveforms

・At 1/4Duty, 1/3bias



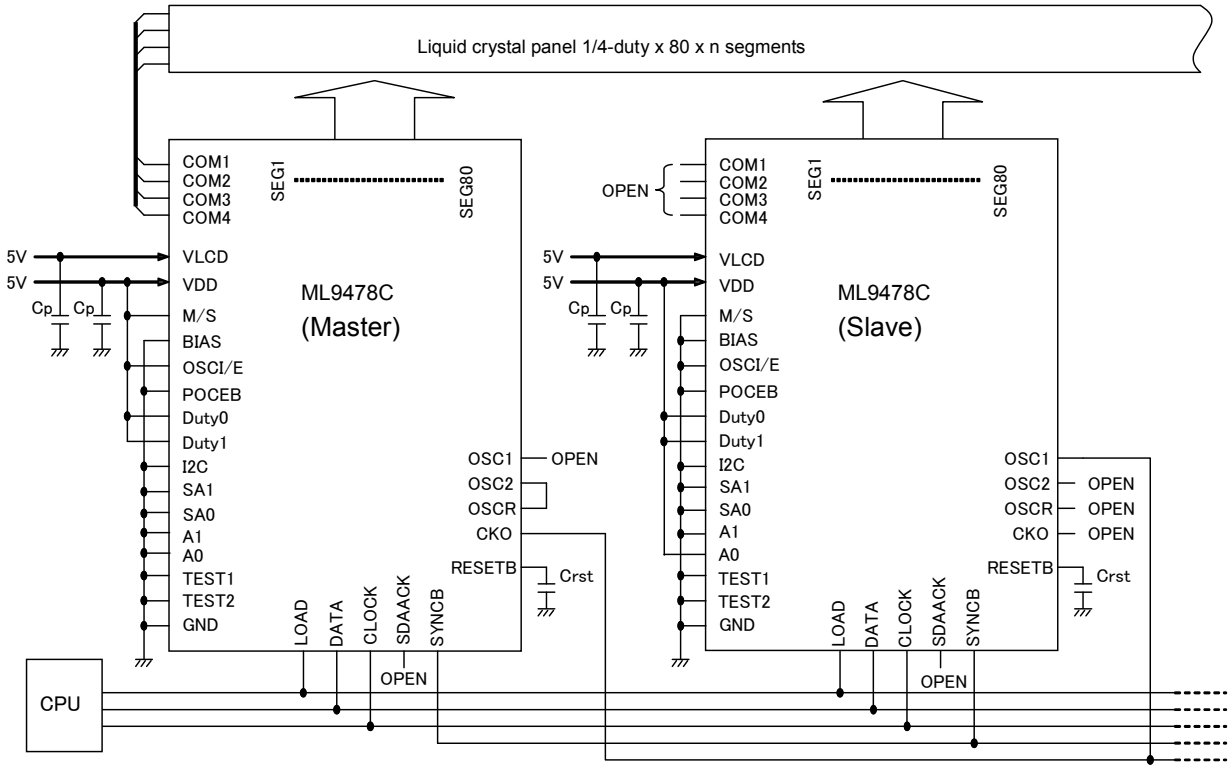


EXAMPLE OF APPLICATION CIRCUIT

Cascade configuration 1

Serial interface
Internal CR oscillator circuit used
1/4Duty
RESETB pin + external capacitance connection to configure POC circuit
The common outputs of the slave chip output GND-level. So Com1 to Com4 set to open.

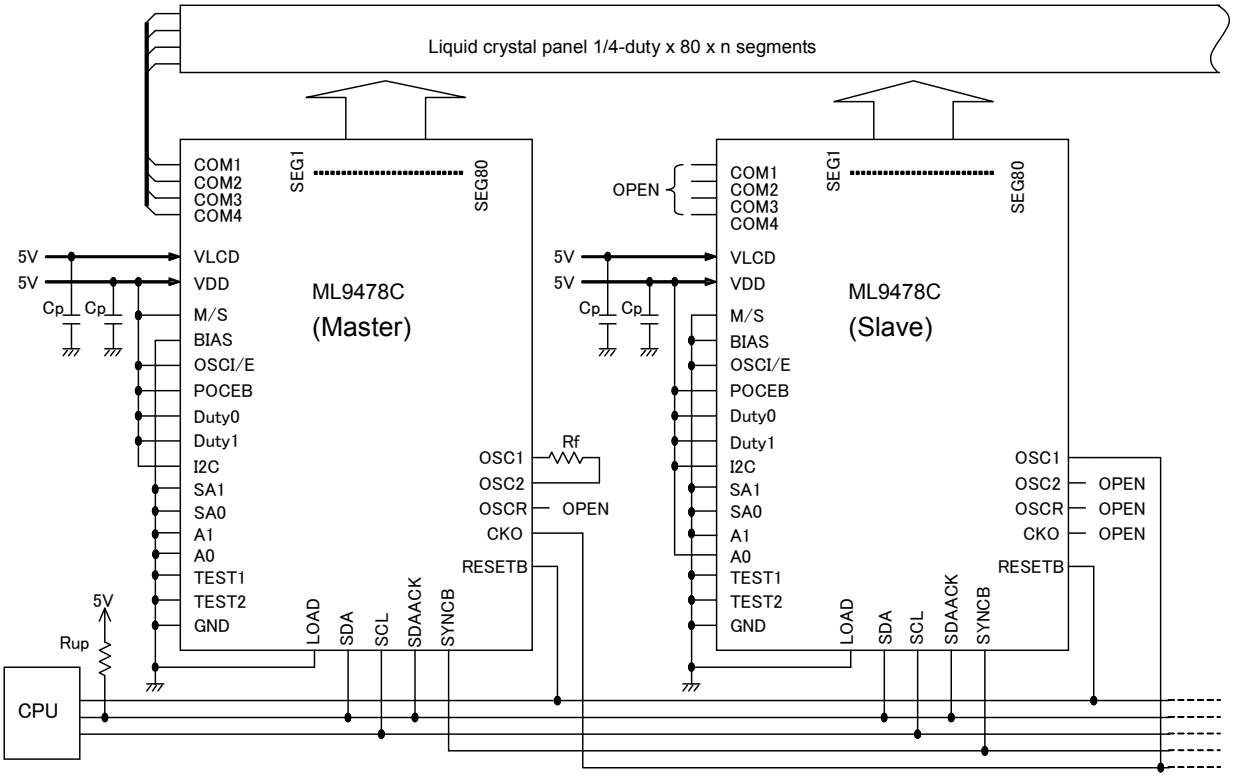
[External component]
Cp = 0.1 [µF] (bypass capacitor between power supplies)
Crst = 4.7 [µF] (capacitance for external POC circuit)



Cascade configuration 2

II^{2}C interface
External Rf-based CR oscillator circuit used
1/4Duty
External RESETB signal input
The common outputs of the slave chip output GND-level. So Com1 to Com4 set to open.

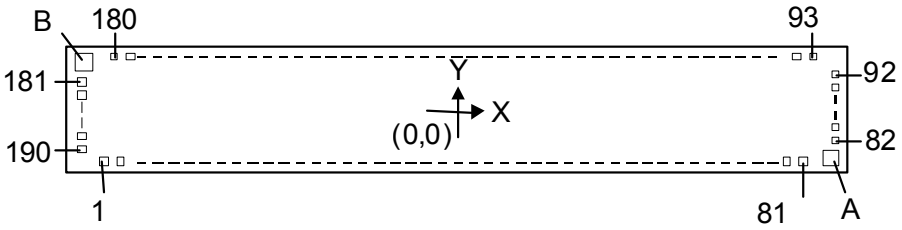
[External component]
Cp = 0.1 [μF] (bypass capacitor between power supplies),
Rf = 470 [kΩ] (external R, resistor for CR oscillator circuit),
Rup = Resistor for SDA data bus pull-up



PAD CONFIGURATION

Pad layout (pattern face)

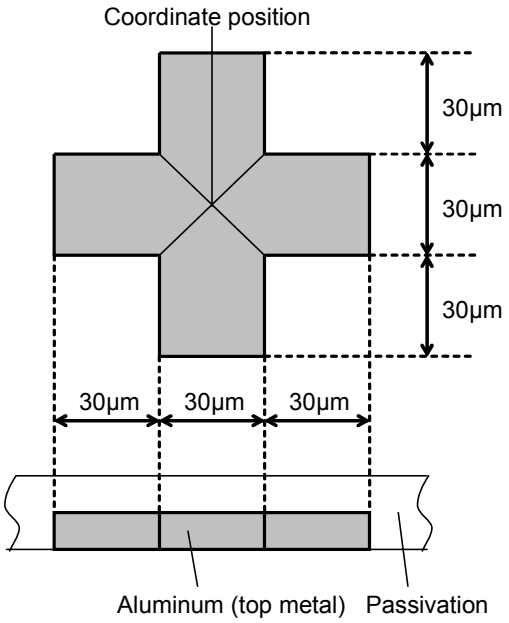
Chip size : 4.80 mm x 0.90 mm
Chip thickness : 400 μm ± 20 μm
Minimum bump pitch : 50 μm
Bump height : 15 μm ±3 μm



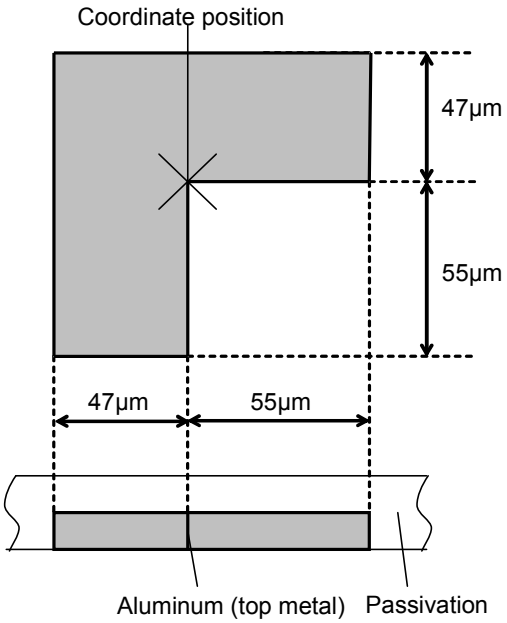
Bump and alignment mark dimensions (pattern face)

PAD No.1~81 : 32 μm x 80 μm
PAD No.82~190 : 30 μm x 84 μm
Alignment marks A and B : See below

[Mark A]



[Mark B]



Alignment mark	X-coordinate (μm) Y	-coordinate (μm)
Mark A	2289	-308
Mark B	-2289	309

Pad center coordinates

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
1	DUMMY	-2206	-308
2	DUMMY	-2149	-308
3	GNDO	-2092	-308
4	Duty1	-2035	-308
5	Duty1	-1978	-308
6	Duty0	-1921	-308
7	Duty0	-1869	-308
8	A0	-1815	-308
9	A0	-1763	-308
10	A1	-1709	-308
11	A1	-1657	-308
12	SA0	-1603	-308
13	SA0	-1549	-308
14	SA1	-1492	-308
15	SA1	-1436	-308
16	VDDO	-1379	-308
17	SDAACK	-1322	-308
18	SDAACK	-1265	-308
19	SDAACK	-1208	-308
20	DATA(SDA)	-1151	-308
21	DATA(SDA)	-1094	-308
22	CLOCK(SCL)	-1037	-308
23	CLOCK(SCL)	-980	-308
24	LOAD	-923	-308
25	LOAD	-866	-308
26	GND	-809	-308
27	GND	-752	-308
28	GND	-695	-308
29	GND	-638	-308
30	GND	-581	-308
31	GND	-524	-308
32	VDD	-467	-308
33	VDD	-412	-308
34	VDD	-357	-308
35	VDD	-302	-308
36	VDD	-247	-308
37	VDD	-192	-308
38	VLCD	-135	-308
39	VLCD	-81	-308
40	VLCD	-27	-308

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
41	VLCD	27	-308
42	VLCD	81	-308
43	VLCD	135	-308
44	RESETB	192	-308
45	RESETB	244	-308
46	OSC1	298	-308
47	OSC1	350	-308
48	OSC1	404	-308
49	OSC2	458	-308
50	OSC2	510	-308
51	OSC2	564	-308
52	OSC2	618	-308
53	OSCR	672	-308
54	OSCR	724	-308
55	OSCR	776	-308
56	CKO	830	-308
57	CKO	882	-308
58	CKO	934	-308
59	CKO	986	-308
60	SYNCB	1040	-308
61	SYNCB	1092	-308
62	SYNCB	1144	-308
63	SYNCB	1196	-308
64	VDDO	1250	-308
65	I2C	1304	-308
66	I2C	1356	-308
67	M/S	1413	-308
68	M/S	1465	-308
69	POCEB	1522	-308
70	POCEB	1574	-308
71	OSCI/E	1628	-308
72	OSCI/E	1680	-308
73	BIAS	1737	-308
74	BIAS	1789	-308
75	TEST2	1846	-308
76	TEST2	1900	-308
77	TEST1	1957	-308
78	TEST1	2014	-308
79	GNDO	2071	-308
80	DUMMY	2128	-308

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
81	DUMMY 2	185	-308
82	DUMMY 2	289	-232
83	DUMMY 2	289	-182
84	DUMMY 2	289	-132
85	COM1 2	289	-82
86	COM2 2	289	-32
87	COM3 2	289	18
88	COM4 2	289	68
89	DUMMY 2	289	118
90	DUMMY 2	289	168
91	DUMMY 2	289	218
92	DUMMY 2	289	268
93	DUMMY 2	185	309
94	DUMMY 2	135	309
95	SEG1 2	085	309
96	SEG2 2	035	309
97	SEG3 1	985	309
98	SEG4 1	935	309
99	SEG5 1	885	309
100	SEG6 1	835	309
101	SEG7 1	785	309
102	SEG8 1	735	309
103	SEG9 1	685	309
104	SEG10 1	635	309
105	SEG11 1	585	309
106	SEG12 1	535	309
107	SEG13 1	485	309
108	SEG14 1	435	309
109	SEG15 1	385	309
110	SEG16 1	335	309
111	SEG17 1	285	309
112	SEG18 1	235	309
113	SEG19 1	185	309
114	SEG20 1	135	309
115	SEG21 1	085	309
116	SEG22 1	035	309
117	SEG23	985	309
118	SEG24	935	309
119	SEG25	885	309
120	SEG26	835	309
121	SEG27	785	309
122	SEG28	735	309
123	SEG29	685	309
124	SEG30	635	309

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
125	SEG31	585	309
126	SEG32	535	309
127	SEG33	485	309
128	SEG34	435	309
129	SEG35	385	309
130	SEG36	335	309
131	SEG37	285	309
132	SEG38	235	309
133	SEG39	185	309
134	SEG40	135	309
135	COM1	85	309
136	COM2	35	309
137	COM3	-15	309
138	COM4	-65	309
139	SEG41	-115	309
140	SEG42	-165	309
141	SEG43	-215	309
142	SEG44	-265	309
143	SEG45	-315	309
144	SEG46	-365	309
145	SEG47	-415	309
146	SEG48	-465	309
147	SEG49	-515	309
148	SEG50	-565	309
149	SEG51	-615	309
150	SEG52	-665	309
151	SEG53	-715	309
152	SEG54	-765	309
153	SEG55	-815	309
154	SEG56	-865	309
155	SEG57	-915	309
156	SEG58	-965	309
157	SEG59	-1015	309
158	SEG60	-1065	309
159	SEG61	-1115	309
160	SEG62	-1165	309
161	SEG63	-1215	309
162	SEG64	-1265	309
163	SEG65	-1315	309
164	SEG66	-1365	309
165	SEG67	-1415	309
166	SEG68	-1465	309
167	SEG69	-1515	309
168	SEG70	-1565	309

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
169	SEG71	-1615	309
170	SEG72	-1665	309
171	SEG73	-1715	309
172	SEG74	-1765	309
173	SEG75	-1815	309
174	SEG76	-1865	309
175	SEG77	-1915	309
176	SEG78	-1965	309
177	SEG79	-2015	309
178	SEG80	-2065	309
179	DUMMY	-21 15	309
180	DUMMY	-2165	309
181	DUMMY	-2289	203
182	DUMMY	-2289	153
183	COM4	-2289	103
184	COM3	-2289	53
185	COM2	-2289	3
186	COM1	-2289	-47
187	DUMMY	-2289	-97
188	DUMMY	-2289	-147
189	DUMMY	-2289	-197
190	DUMMY	-2289	-247

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)

REVISION HISTORY

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
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