
ML9479E

Static, 1/2 Duty, 1/3 Duty, 1/4 Duty 160 Outputs LCD Driver

GENERAL DESCRIPTION

The ML9479E is an LCD driver LSI, consists of a 160-bit shift register, a 640-bit data latch, 160 sets of LCD drivers, and a common signal generation circuit.

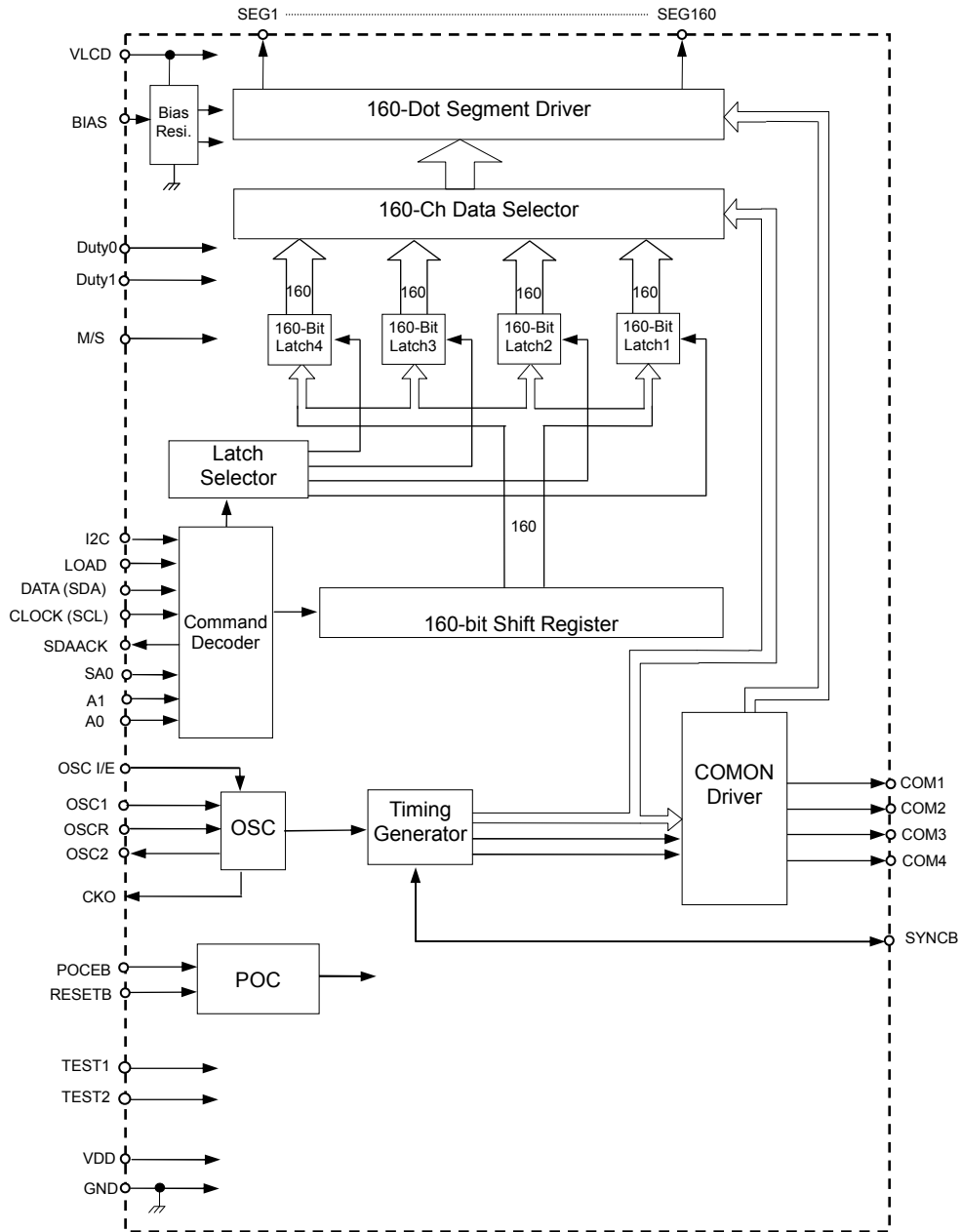
It can directly drive an LCD up to 160 segments for static display, 320 segments for 1/2-duty display, 480 segments for 1/3-duty display, and 640 segments for 1/4-duty display.

The three-wire serial interface and I²C interface are selectable.

FEATURES

- Logic power supply voltage : 2.7 to 5.5 V
- LCD drive power supply voltage : 4.5 to 5.5 V
- Maximum number of segments
 - Static display : 160 segments
 - 1/2-duty display : 320 segments
 - 1/3-duty display : 480 segments
 - 1/4-duty display : 640 segments
- Interface with microcomputer :
 - Serial interface : DATA, CLOCK, LOAD
 - CLOCK transfer speed up to 1 MHz
 - I²C interface : SDA, SCL, SDAACK
 - SCL transfer speed up to 400 kHz
- Built-in CR oscillator circuit using the internal resistor or External resistor
- Cascade connectable (up to eight chips)
- Built-in common signal generation circuit
- Built-in common output intermediate-value voltage generation circuit
- Built-in POC (Power On Clear) circuit
- Gold bump chip (ML9479EDVWA)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rating	Unit
Logic power supply voltage	V _{DD}	T _a = 25°C	-0.3 to 6.0	V
LCD drive power supply voltage	V _{LCD}	T _a = 25°C	-0.3 to 6.0	V
Input voltage	V _I	T _a = 25°C	- 0.3 to V _{DD} + 0.3	V
Output short-circuit current	I _S	T _a = 25°C	-2.0 to +2.0	mA
Chip temperature	T _c —		125 °C	
Storage temperature	T _{STG}	— -55	to +150	°C

Note: Do not use the ML9479E by short-circuiting one output pin to another output pin as well as to other pin (input pin, input/output pin, or power supply pin).

RECOMMENDED OPERATION CONDITIONS

Item	Symbol	Condition	Range	Unit
Logic power supply voltage	V _{DD} *	—	2.7 to 5.5	V
LCD drive power supply voltage	V _{LCD} *	—	4.5 to 5.5	V
OSC IN clock frequency	f _{CP1}	—	up to 10	kHz
Data clock frequency	f _{CP2}	—	up to 1.0	MHz
SCL clock frequency	f _{SCL}	—	up to 400	kHz
Operating temperature	T _a	—	-40 to +105	°C

Note(*): Use at V_{DD} ≤ V_{LCD}.

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$$f_{\text{FRM}} = f_{\text{OSC}} / 24$$

Recommended setting range for external component (oscillator circuit)

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, T_a = -40 to +105°C)

Item	Symbol	Condition	Min T	YP	Max	Unit
Oscillation resistor	R _f	—	423	470	517	kΩ
Frame frequency	f _{FRM}	(F1,F0)=(0,1)	47	75	114	Hz

The relation between oscillation resistor and frame frequency is as the equation below.

$$f_{\text{FRM}} = f_{\text{OSC}} / (16 \times 24)$$

$$f_{\text{OSC}} = 1 / (\text{Device coefficient} \times \text{External resistor } R_f)$$

$$\text{Device coefficient} = 73.8 \times 10^{-12} \pm 25\%$$

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$)

Item	Symbol	Condition	Min. T	yp.	Max.	Unit	Applicable pin	
"H" input voltage	V_{IH}	— 0.8V	V_{DD}	— V	V_{DD}	V	(*1)	
"L" input voltage	V_{IL}	— GND		—	$0.2V_{DD}$	V	(*1)	
Input leakage current 1	I_{L1}	$V_I = V_{DD}$ or 0 V	-1.0	—	1.0	μA	(*1)	
Input leakage current 2	I_{L2}	$V_I = V_{DD}$ or 0V POCEB="H"	-1.0	— 1.0		μA	RESET B	
Pull-up current	I_{pu}	$V_{DD} = 5.0\text{V}$, $V_I = 0$ V POCEB = "L"	30	— 140		μA	RESET B	
"H" output voltage	V_{OH}	$I_O = -600\mu\text{A}$	$0.9V_{DD}$	— —		V	CKO, SYNCB	
"L" output voltage 1	V_{OL1}	$I_O = 600\mu\text{A}$ —		—	$0.1V_{DD}$	V	CKO, SYNCB	
"L" output voltage 2	V_{OL2}	$I_O = 600\mu\text{A}$ —		—	$0.1V_{DD}$	V	SDAACK	
Driver ON resistor	Segment	V_{OHS}	$V_{LCD} = 5\text{V}$	— 5		15	$\text{k}\Omega$	SEG1 to SEG160
	Common	V_{OHC}	$V_{LCD} = 5\text{V}$	— 5		12	$\text{k}\Omega$	COM 1 to COM4

(*1): DATA(SDA), CLOCK(SCL), LOAD, M/S, SYNCB, Duty1, Duty0, BIAS, SA0, A1, A0, OSC1, OSC I/E, I2C, POCEB

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$)

Item	Symbol	Condition	Min.	Typ.	Max. U	nit	Applicable pin
Static supply current	I_{DD5}	$V_{DD}=V_{LCD}=5.5$ V Input pin fixed to "H" or "L"	— 8		15	μA	V_{DD}
	I_{LCD5}	Oscillation stopped, output no-load POCEB="L"	— 9		15	μA	V_{LCD}
Dynamic supply current 1	I_{DD1}	$V_{DD}=V_{LCD}= 5.5$ V (*2)(*3) Clock OSC1 external input	(*6)	— 10	18	μA	V_{DD}
	I_{LCD1}	$f_{CP1}=1.8\text{kHz}$	(*7)	— 9	15	μA	V_{LCD}
Dynamic supply current 2	I_{DD2}	$V_{DD}=V_{LCD}= 5.5$ V (*2)(*3) Internal oscillation	(*6)	— 65	90	μA	V_{DD}
	I_{LCD2}		(*7)	— 9	15	μA	V_{LCD}
Dynamic supply current 3	I_{DD3}	$V_{DD}=V_{LCD}= 5.5$ V (*2)(*4)(*6) Internal oscillation	—	200	300	μA	V_{DD}
	I_{LCD3}	At three-wire serial IF data input	— 9		15	μA	V_{LCD}
Dynamic supply current 4	I_{DD4}	$V_{DD}=V_{LCD}= 5.5$ V (*2)(*5)(*6) Internal oscillation	—	230	350	μA	V_{DD}
	I_{LCD4}	At I ² C IF data input	— 9		15	μA	V_{LCD}

(*2): M/S = "H", 1/4-duty, 1/3-bias, (F1,F0) = (1,1) 95 Hz, POCEB = "L", output pin no-load.

(*3): Three-wire serial or I²C interface. Input pin fixed to "H" or "L".

(*4): Serial interface, data input frequency = 1 MHz.

(*5): I²C interface, data input frequency = 400 kHz.

(*6): Alternately inputs "0" and "1" for LCD display data (checkered display).

(*7): Inputs all "1s" for LCD display data (all illuminated).

Switching Characteristics

- OSC timing

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
OSC IN clock frequency (external input)	f_{CP1}	Clock input from OSC1. OSC2 and OSCR open. OSC I/E = "L"	—	1.8	10	kHz	OSC1
Clock pulse width (External input)	t_{WCP1}		—	—	—	μs	SC1
Clock rise and fall time (external input)	t_{OSC}		—	— (*1)	—	μs	SC1
External Rf clock frequency (Internal oscillation)	f_{OSC1}	Between OSC1 and OSC2 $R_f = 470\text{k}\Omega$ (F1,F0)=(0,1) OSCR open. OSC I/E = "H"	18	28.8	44	kHz	OSC1, OSC2
Internal clock frequency (Internal oscillation)	f_{OSC2}	OSC1 open. (F1,F0)=(0,1) OSC2 and OSCR short-circuited. OSC I/E = "H"	18	28.8	44	kHz	OSC1, OSCR, OSC2

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$$f_{FRM} = f_{OSC} / 24$$

(*1) t_{OSC} is a reference value.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: $\text{max}=2\mu\text{s}$.

- Serial interface timing

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Data clock frequency	f_{CP2}		—	—	1	MHz	CLOCK
Data clock pulse width	t_{WCP2}		100	—	—	ns	CLOCK
Data setup time	t_{SU}		50	—	—	ns	DATA
Data hold time	t_{HD}		50	—	—	ns	CLOCK
CLOCK-LOAD timing	t_{CL}		100	—	—	ns	CLOCK
LOAD-CLOCK timing	t_{LC}		100	—	—	ns	LOAD
LOAD pulse width	t_{WLD}		100	—	—	ns	LOAD
Signal rise and fall time	t_{sr}, t_{sf}		—	—	(*2)	ns	CLOCK, DATA, LOAD

(*2) t_{sr} and t_{sf} shall be reference values.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: $\text{max}=10\text{ns}$.

- I²C interface timing

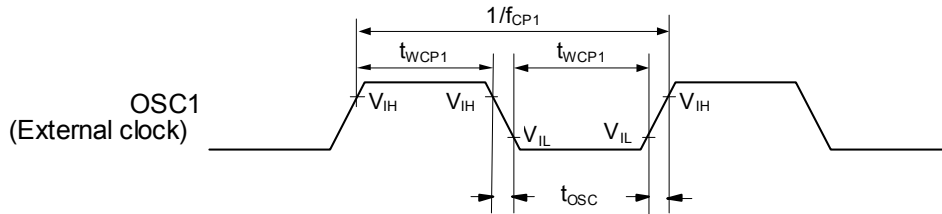
(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
SCL clock frequency	f _{SCL}		—	—	400	kHz	SCL
Hold time (repeat) "STATRT" condition	t _{HD,STA}		0.6	—	—	μs	SCL,SDA
SCL "L" pulse width	t _{LOW}		1.3	—	—	μs	SCL
SCL "H" pulse width	t _{HIGH}		0.6	—	—	μs	SCL
Setup time for repeat "START" condition	t _{SU,STA}		0.6	—	—	μs	SCL,SDA
Data hold time	t _{HD,DAT}		0	—	—	ns	SCL,SDA
Data setup time	t _{SU,DAT}		200	—	—	ns	SCL,SDA
Setup time for "STOP" condition	t _{SU,STO}		0.6	—	—	μs	SCL,SDA
Bus free time between "STOP" condition and "START" condition	t _{BUF}		1.3	—	—	μs	SCL
Data valid acknowledge time	t _{VD,ACK}		—	—	1.2	μs	SCL,SDAAACK
Signal rise and fall time	t _{ir,tif}		—	—	(*3)	μs	SCL,SDA
Data bus load capacitance	C _b		—	—	400	pF	SDA,SDAAACK
Noise pulse width tolerance	t _{wf}		—	—	50	ns	SCL,SDA

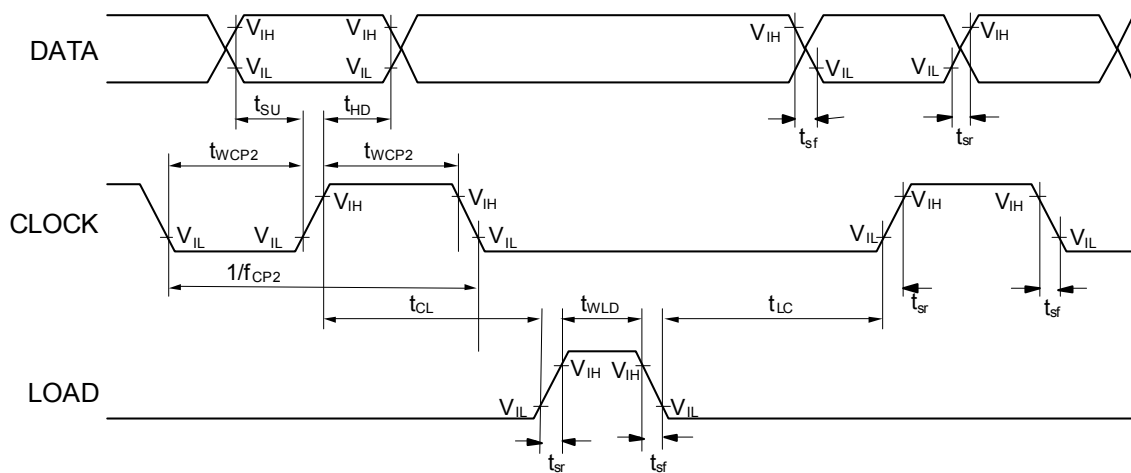
(*3) t_{ir} and t_{tif} shall be reference values.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: max=0.1μs.

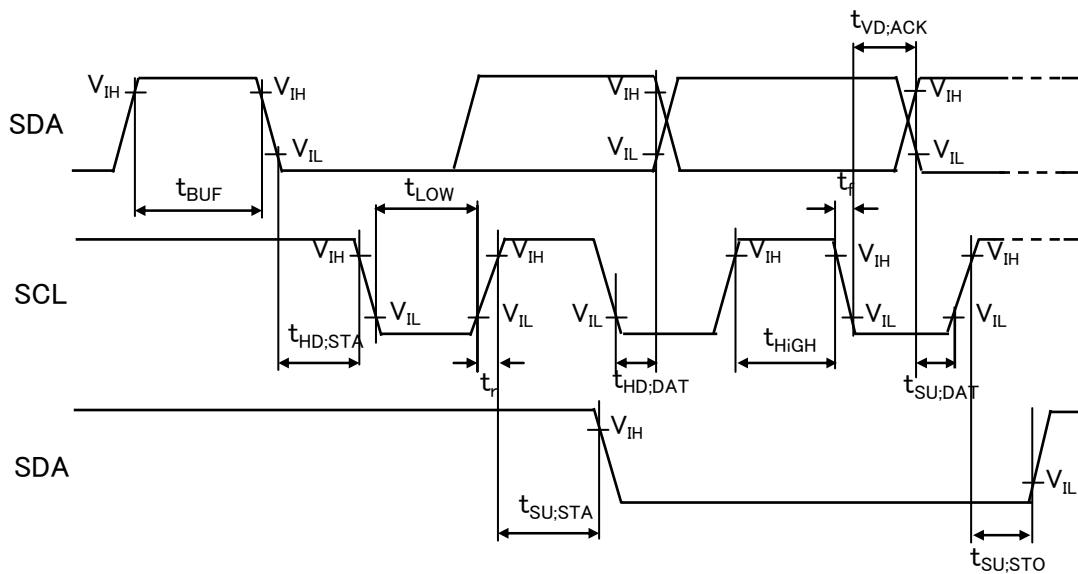
Timing chart (OSC1)



Timing chart (Serial interface)



Timing chart (I²C interface)



REFERENCE DATA

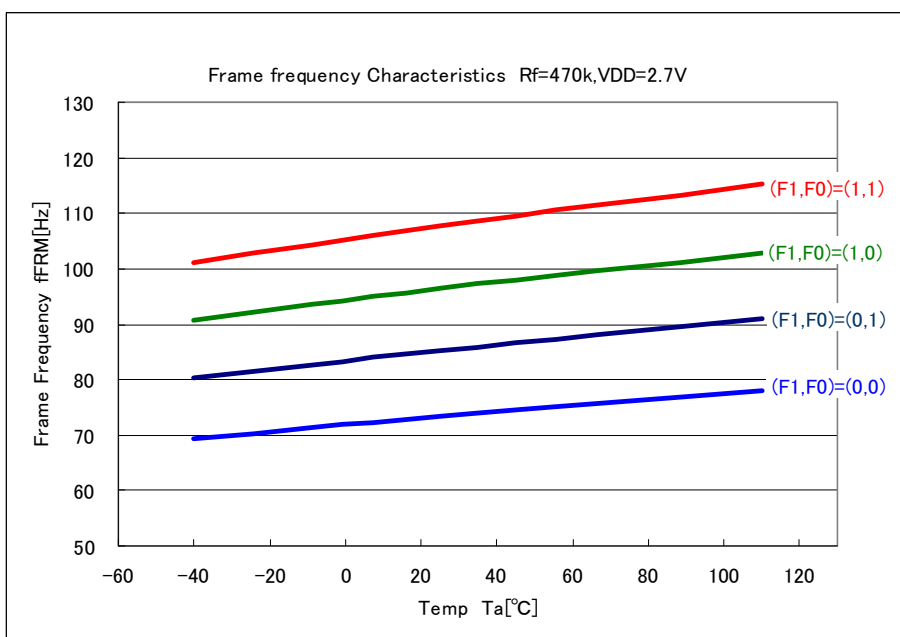
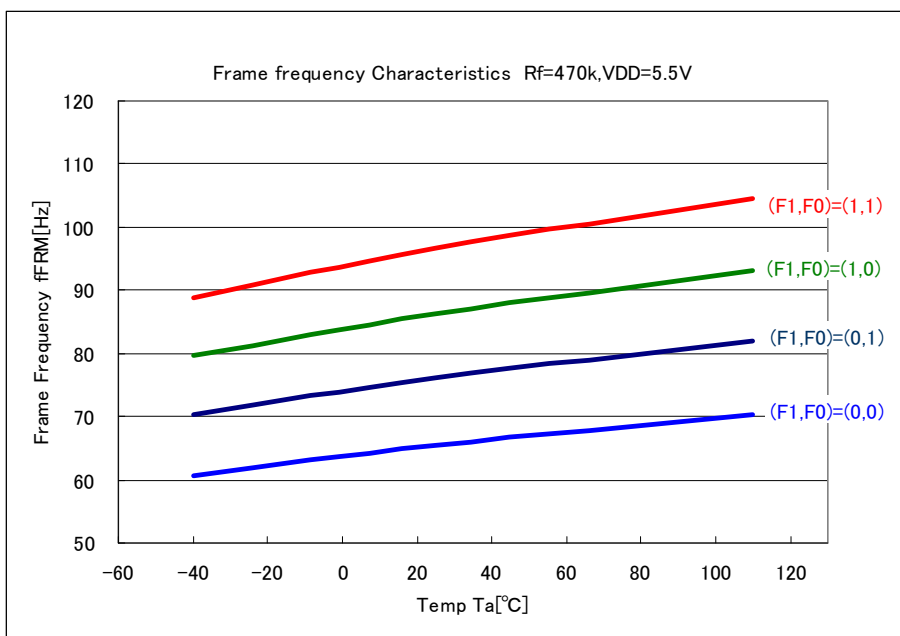
Frame frequency Characteristics

VDD=5.5V/2.7V Rf=470Ω

Frame frequency $f_{FRM} = f_{OSC} / (16 \times 24)$

$f_{OSC} = 1 / (\text{Device coefficient} \times \text{External resistor } R_f)$

Device coefficient = $73.8 \times 10^{-12} \pm 25\%$



POWER ON/OFF TIMING

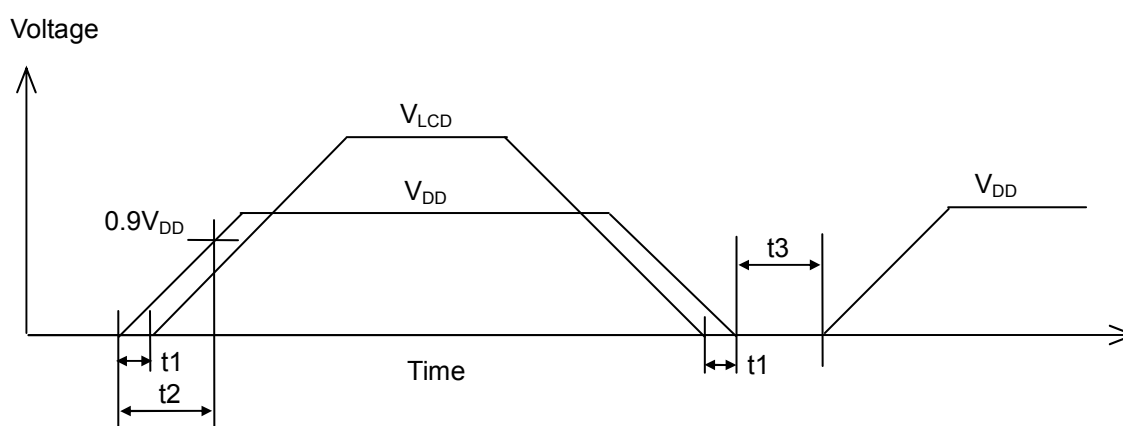
To turn on the power supply, raise the logic power supply first, then LCD drive power supply in order to prevent the IC from malfunctioning.

To fall the power supply, fall the LCD drive power supply first, then the logic power supply.

For a VDD pin ranging from 0 V to VDDmin, set $V_{DD} \geq V_{LCD}$ and $t_1 \geq 0$ [ns].

To enable the Internal POC circuit, the VDD power supply rise time t_2 range needs to be $100 [\mu\text{s}] \leq t_2 \leq 500 [\text{ms}]$.

For the VDD power supply to turn OFF then turn ON again, it is necessary to secure the POC discharge time $t_3 \geq 100$ [ms].

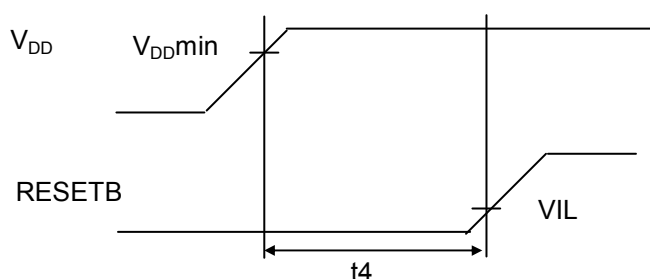


INITIALIZATION SIGNAL TIMING

When RESETB signal is externally input

The RESETB pin input is valid both for POCEB = "L" and "H". Usable in combination with the POC.

Keep the RESETB pin at "L" level until the VDD reaches VDDmin. ($t_4 \geq 200$ [ns])



When Internal POC circuit is used

When using the Internal POC circuit in the initialization, set the POCEB pin to "L".

At this time, the power ON/OFF timing conditions are t₁ to t₃ above mentioned.

When RESETB pin POC circuit is used

If the power ON/OFF timing conditions t₁ to t₃ cannot be kept, the RESETB pin needs to have a capacitance to configure the POC circuit. For this case, connect a capacitance value according to the power supply rise time.

For the power supply rise time t₂ and external capacitance value, use the following formula as a guide:

$$C_{RST} [\text{F}] > t_2 [\text{sec}] / (30 \times 10^3)$$

PIN DESCRIPTIONS

Pad number	Symbol I/O		Description
109-112 M	/S	I	This is the input to switch between the master and slave modes. It has a schmitt circuit. When this pin is "H", the mode is master. When this pin is "L", the mode is slave.
9-12 13-16	Duty0 Duty1 *1	I	Display duty switch pins. These have schmitt circuits. Duty0="L", Duty1="L" : Static (COM1=COM2=COM3=COM4) Duty0="H", Duty1="L" : 1/2Duty (COM1=COM3, COM2=COM4) Duty0="L", Duty1="H" : 1/3Duty (COM2=COM4) Duty0="H", Duty1="H" : 1/4Duty
121-124 BIAS		I	This pin sets the LCD bias. It has a schmitt circuit. BIAS= "L": 1/3bias BIAS= "H": 1/2bias
25-28	SA0	I	Slave address input pin. It has a schmitt circuit.
17-20 21-24	A1 A0	I	Sub address input pins. These have schmitt circuits.
117-120 C	SC I/E	I	This input selects whether to use the external clock input mode or to use the Internal oscillation mode or external oscillation mode. It has a schmitt circuit. When this pin is "H", the mode is the Internal or external Rf oscillation mode. When this pin is "L", the mode is the external clock input mode. Use the slave chip as it is connected to GND.
78-82 83-87 88-82	OSC1, OSCR, OSC2 *2	I I O	These pins are for the oscillator circuit to generate common signals. The OSC1 and OSC2 pins are input pins and have a schmitt circuit. OSC2 is an output pin. It becomes an output when the OSC I/E pin = "H" and a high impedance when the OSC I/E pin = "L". 【 In the master mode (M/S pin = "H") 】 Three types are selectable: Internal oscillation mode, external oscillation mode, and external clock input mode. •Internal oscillation mode: Set the OSC I/E pin to "H", short the OSC2 and OSC1 pins, and open the OSC1 pin. •External Rf oscillation mode: Set the OSC I/E pin to "H", connect an oscillation resistor Rf between the OSC1 and OSC2 pins, and open the OSC2 pin. •External clock input mode: Set the OSC I/E pin to "L", open the OSC2 and OSC1 pins, and input the external clock to the OSC1 pin. 【 In the slave mode (M/S pin = "L") 】 Open the OSC2 and OSC1 pins and connect the OSC1 pin to the ML9479E's CKO pin that has been set to the master mode.
93-97	CKO	O	Clock output pin. In the master mode (M/S pin = "H"), the 1/16 division signal of the oscillation frequency is output. In the slave mode (M/S pin = "L"), the output is fixed to "L". For a cascade connection, connect this pin to the OSC1 pin of the chip that has been set to the slave mode.

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98-102 SY	NCB	I/O	Input/output pin for common synchronization. It has a schmitt circuit. It becomes the synchronization signal output pin in the master mode (M/S pin = "H"). It becomes the synchronization signal input pin in the slave mode (M/S pin = "L"). For cascade connection, connect all of the involved ML9479Es' SYNC pins by the common line.
105-108 I2C		I	Interface switching pin. It has a schmitt circuit. When this pin is "H", the interface is I ² C. When this pin is "L", the interface is three-wire serial.
36-40	DATA (SDA)	I	Display data input pin. It has a schmitt circuit. I2C="L": Serial interface; DATA Input the display data in the order of SEG 160, SEG 159, ... , SEG 2, and SEG1. The display data turns on at "H" and turns off at "L". I2C="H": I ² C interface; SDA Input the display data in units of 8 bits. The display data turns on at "H" and turns off at "L". This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
41-45	CLOCK (SCL)	I	Shift clock input pin for display data. It has a schmitt circuit. I2C="L": Serial interface; CLOCK The display data input to the DATA pin is serially input to the shift register at the CLOCK signal rise. I2C="H": I ² C interface; SCL The display data input to the SDA pin is serially input to the shift register at the SCL signal rise. This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
46-50	LOAD	I	Input pin for the load signal of display data. It has a schmitt circuit. I2C="L": Serial interface; LOAD The display data in the shift register is transmitted as is to the segment driver for the "H" duration. When this pin is brought into "L", the shift register is disconnected from the segment driver. The display data in the shift register immediately before it become "L" is held in the data latch and transmitted to the segment driver. I2C="H": I ² C interface Use this pin as it is connected to GND.
31-35	SDAACK	O	I2C="L": Serial interface Use this pin as it is opened. I2C="H": I ² C interface The I ² C bus acknowledge output signal. Normally, use it as it is connected with the SDA pin. Connect an external pull-up resistor whenever necessary, as it is an open drain pin. The pull-up connection destination supply voltage shall be the V _{DD} supply voltage or less.
113-116	POCEB	I	Internal POC circuit enable pin. It has a schmitt circuit. When this pin is "H", the POC circuit becomes OFF and the constant current (8μA) is cut. The RESETB pin pull-up resistor is cut as well. When this pin is "L", the POC circuit becomes ON. The RESETB pin is connected to a pull-up resistor.
73-77	RESETB *3	I	Reset signal input pin for initializing inside the IC. It has a schmitt circuit. The "L" level enables the reset. This pin has an Internal pull-up resistor. Open when POCEB = "H". Pull-up when POCEB = "L". The power-on reset operation is available by connecting an external capacitor.

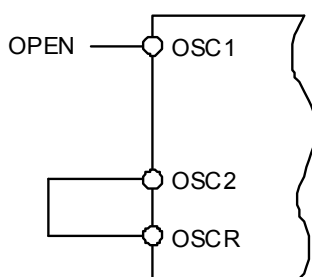
125-128 129-132	TEST1 TEST2	I	Pin for testing the IC. These have Internal pull-down resistors. Use it as it is connected to GND.
155-234 239-318	SEG1 ~SEG160	O	Outputs for LCD display. Connected to the segment pins on the LCD panel. In the display off mode, all the outputs are fixed to GND.
143-146 235-238 326-329	COM1 ~COM4	O	Outputs for LCD display. Connected to the common pin on the LCD panel. The output pins are located at three positions: both ends of the chip and between SEG 80 and SEG 81. Each is connected inside the chip. Use the COM pins in accordance with the panel to be used. In the display off mode, all the outputs are fixed to GND. When the slave is set (M/S="L"), connecting SY NCB signal enables the master chip to synchronize with common outputs.
59-65	VDD	-	Power supply pin for logic circuit.
66-72	VLCD	-	Power supply pin for LCD driver.
51-58 G	ND	-	Ground pin.
29-30 103-104	VDDO -		VDD output pin. Use this pin when fixing the mode setting input pin to "H" on the COG.
7-8 133-134	GNDO -		Ground output pin. Use this pin when fixing the mode setting input pin to "L" on the COG.
1-6 135-142 147-154 319-325 330-331	DUMMY	-	Floating pin. At this time, avoid this pin from shorting with pins other than DUMMY in the wiring on the COG.

*1: For details of the COM and SEG waveform when a duty is selected, refer to "Common waveform" on page 18 and "Common Segment waveform" on page 19 to 23.

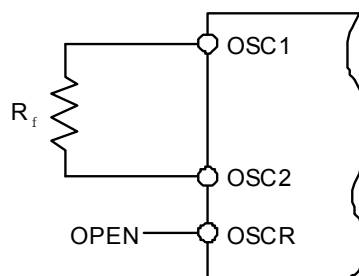
*2: Oscillator circuit configuration

- When M/S = "H", OSC I/E = "H"

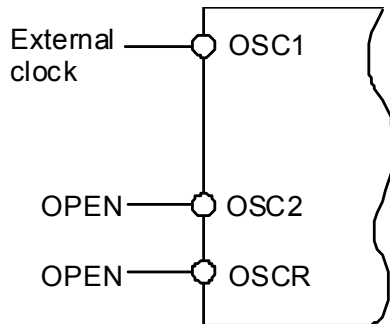
[Internal Rf oscillation mode]



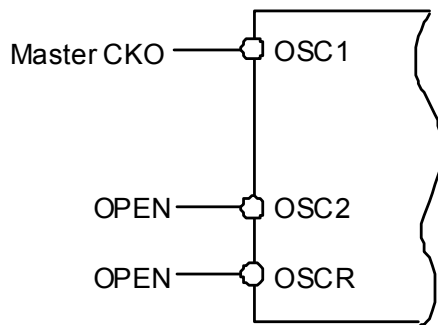
[External Rf oscillation mode]



- External clock input mode when M/S = "H" and OSC I/E = "L"

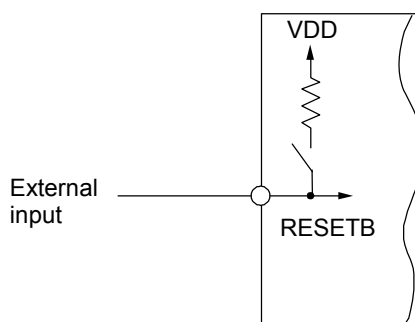


- M/S = "L", slave mode, external clock input mode

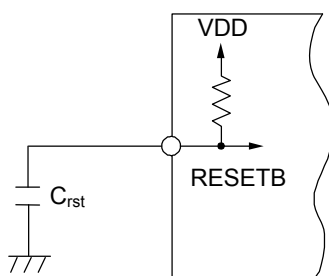


*3: Reset circuit configuration

- External input to RESETB when POCEB = "H"



- POC circuit configuration when POCEB = "L"



DESCRIPTION

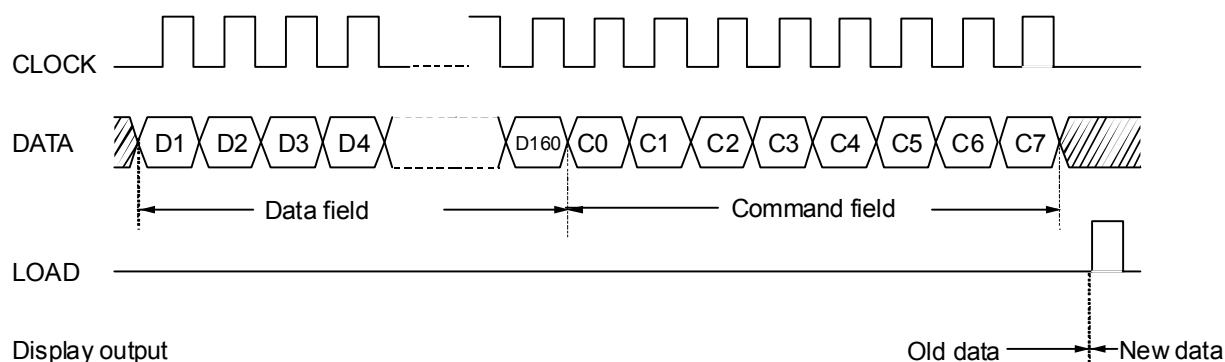
Operation description (Serial interface)

- Display data input

As described in the Data configuration section, the display data consists of the data field that corresponds to each segment on/off and the command field that indicates the display data input.

When inputting the display data, the "F3" command is set in the command field. When the "F1" or "F2" command is set in the command field, the display data in the data field becomes invalid.

The data input to the DATA pin is loaded to the shift register at the CLOCK pulse rise, transferred to the display data latch during the LOAD pulse at the "H" level, then output via the segment driver.

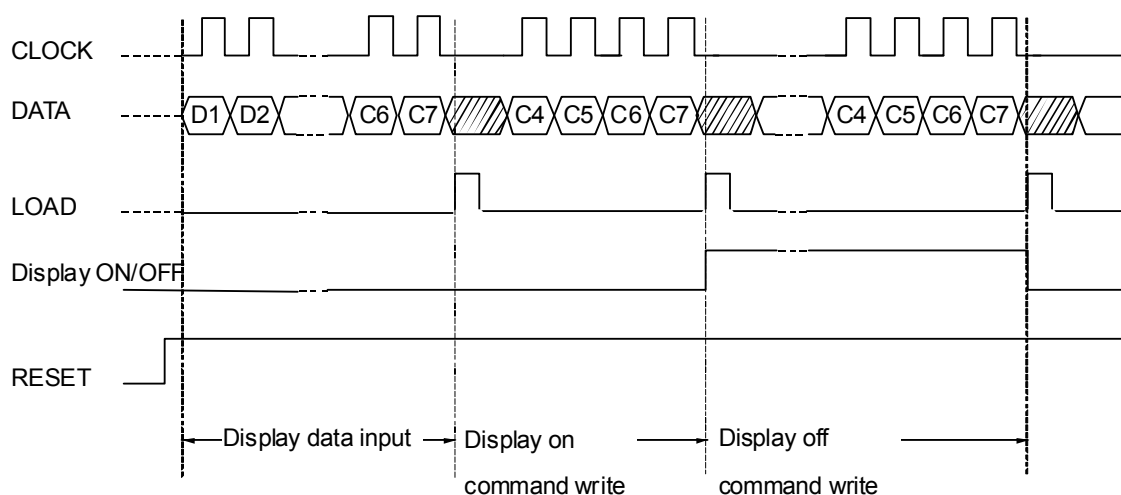


- Display on, Display off

The display becomes off at power-on reset. To display, write the display on command.

The display off is the command that makes all segments off. Writing the display off command, turns off the lights regardless of the display data.

The display on is the command to release the display off. Writing the display on command returns the display to the original state.



List of Commands

Command name	C7	C6	C5	C4	C3	C2	C1	C0	Operation
F0 0		0	0	0	x	x	x	x	Disabled
F1 0		1	F1 (*2)	F0 (*2)	x x		x	x	Frame frequency setting (F1,F0)=(0, 0): 65Hz (F1,F0)=(0, 1): 75Hz (F1,F0)=(1, 0): 85Hz (F1,F0)=(1, 1): 95Hz (valid for Internal CR oscillation)
F2 1		0	1	D (*2)	x x		x	x	Display on/off "0": O ff (COM=SEG=GND) "1": O n
F3(*1) 1		1	SA1	SA0	A1	A0	Co1	Co0	Data write address setting (Co1,Co0)=(0, 0): Corresponding to common 1 (Co1,Co0)=(0, 1): Corresponding to common 2 (Co1,Co0)=(1, 0): Corresponding to common 3 (Co1,Co0)=(1, 1): Corresponding to common 4 SA1, SA0, A1, A0: Chip address

x : Don't care

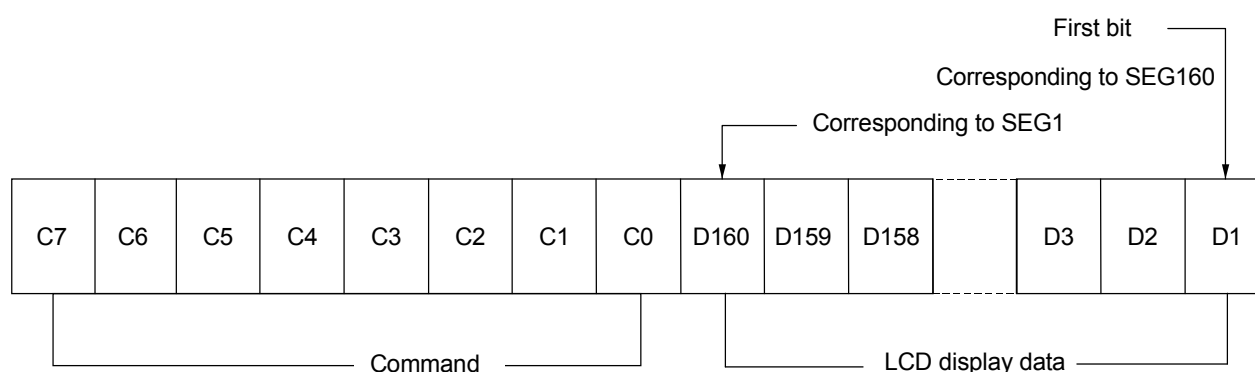
(*1): For the I²C interface, SA0 is set at a slave address.
These bits become "Don't care".

In the ML9479E, set the SA1 address to "1".

(*2): The register is set to the following value by the RESETB = "L" input or by the power-on POC.
F1="0", F0="0", D="0"

Data configuration

- Data configuration (Serial interface)

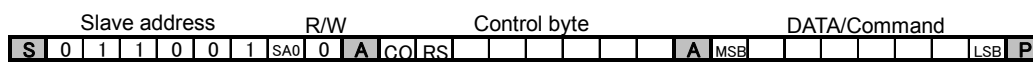


Note 1 : The commands F1 and F2 settings become valid when the least four bits of C4 to C7 are input.
(The bits from D1 to D160 and from C0 to C3 are not necessary.)

Note 2 : If the dummy bit is needed for the reason of number of transfer bits, put it on the first bit side.

Note 3 : The command execution follows the contents of the C7 to C0 registers immediately before the LOAD becomes "H".

• Data configuration (I²C interface)



Slave address: 0 1 1 0 0 1

CO: Consecutive control byte setting bit
 0: Last control byte, 1: Consecutive control byte
 RS: Command/data setting bit
 0: Command data, 1: Display data

For the I²C interface, each IC is assigned with a 7-bit slave address. The first one byte in the transfer consists of this 7-bit slave address and the R/W bit that indicates the data transfer direction. Always input "0" to the eighth R/W bit because the ML9479E is a write-only LSI.

The eight bits next to the slave address is a control byte. The first one bit is CO: consecutive command setting bit and the next one bit is RS: command/data setting bit (the remaining six bits are the Don't care bits).

When CO = "0": Means the last control byte.

When CO = "1": Means the control bytes are successively input.

When RS = "0": Means the data to be input next is the command data.

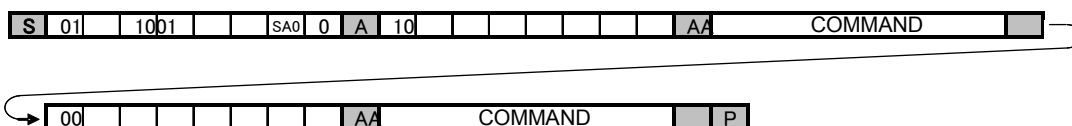
When RS = "1": Means the data to be input next is the display data.

The display data can be successively input.

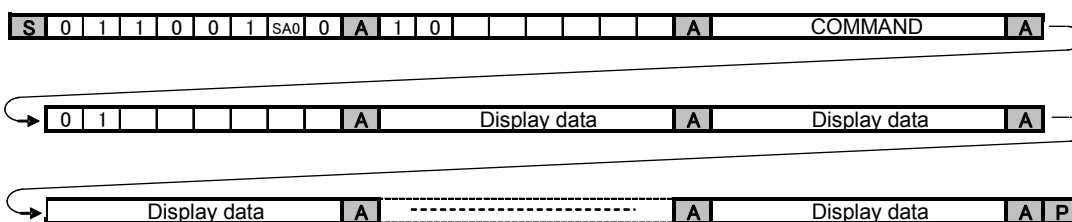
Example of Data Setting

- When inputting two commands

When inputting two commands



- When inputting the command and display data



Data write method

• Serial interface

The data is written to the address set by the data write setting command (F3).

For the Serial interface, the data is written in units of 160 bits.

Written from D160 to SEG1, D159 to SEG2, ..., D2 to SEG159, and D1 to SEG160.

	MSB Segm				ent output												LSB
	1234				72	73	74	75	76	77	78	79	80				
COM1	D160	D159	D158	D157	D89	D88	D87	D86	D85	D84	D83	D82	D81				
COM2	D160	D159	D158	D157	D89	D88	D87	D86	D85	D84	D83	D82	D81				
COM3	D160	D159	D158	D157	D89	D88	D87	D86	D85	D84	D83	D82	D81				
COM4	D160	D159	D158	D157	D89	D88	D87	D86	D85	D84	D83	D82	D81				

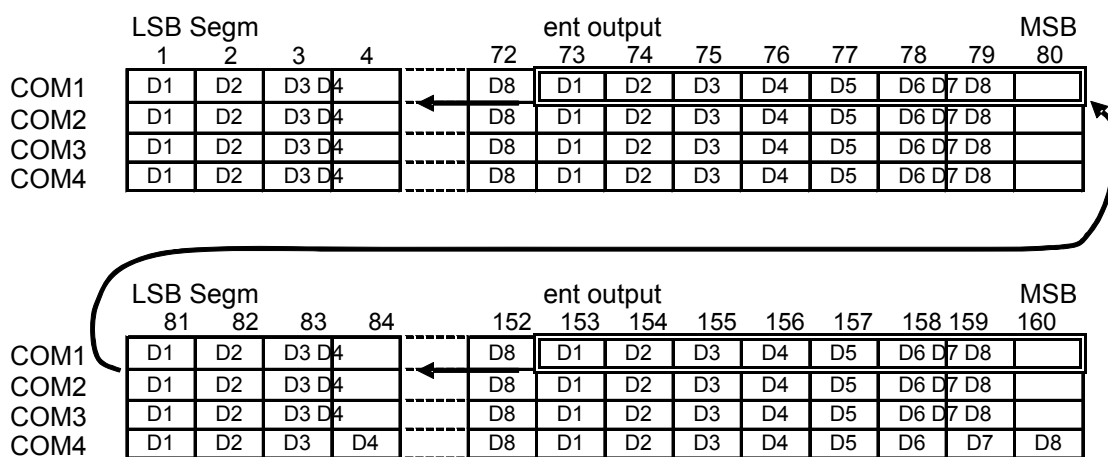
	MSB Segm				ent output												LSB
	81	82	83	84	152	153	154	155	156	157	158	159	160				
COM1	D80	D79	D78	D77	D9	D8	D7	D6	D5	D4	D3	D2	D1				
COM2	D80	D79	D78	D77	D9	D8	D7	D6	D5	D4	D3	D2	D1				
COM3	D80	D79	D78	D77	D9	D8	D7	D6	D5	D4	D3	D2	D1				
COM4	D80	D79	D78	D77	D9	D8	D7	D6	D5	D4	D3	D2	D1				

• I²C interface

The data is written to the address set by the slave address.

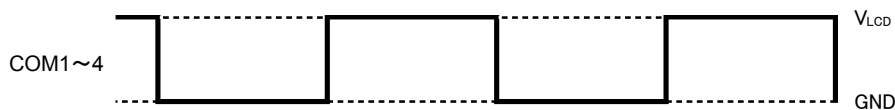
For the I²C interface, the data is written to the specified address starting with the LSB side in units of 8 bits.

(The data is written in the order from SEG153-160, SEG145-SEG152, ..., SEG9-16, and SEG1-SEG8.)



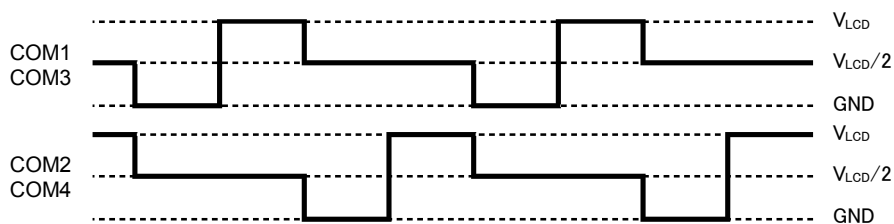
● Common waveforms

(1) At static

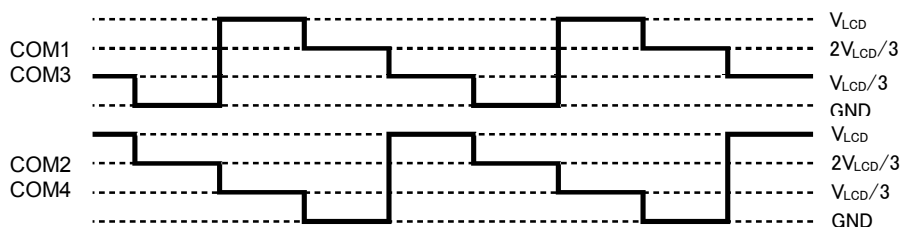


(2) At 1/2-duty

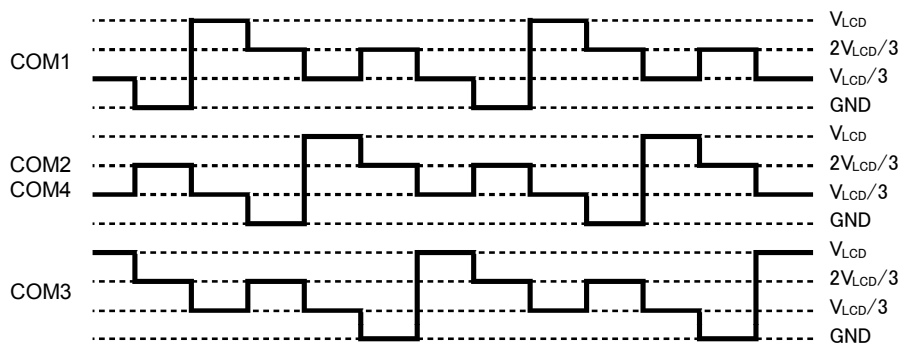
At 1/2-bias



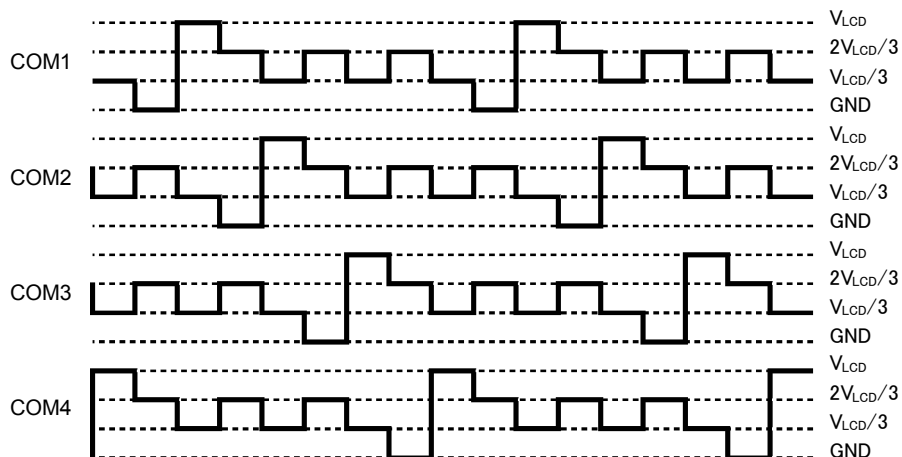
At 1/3-bias



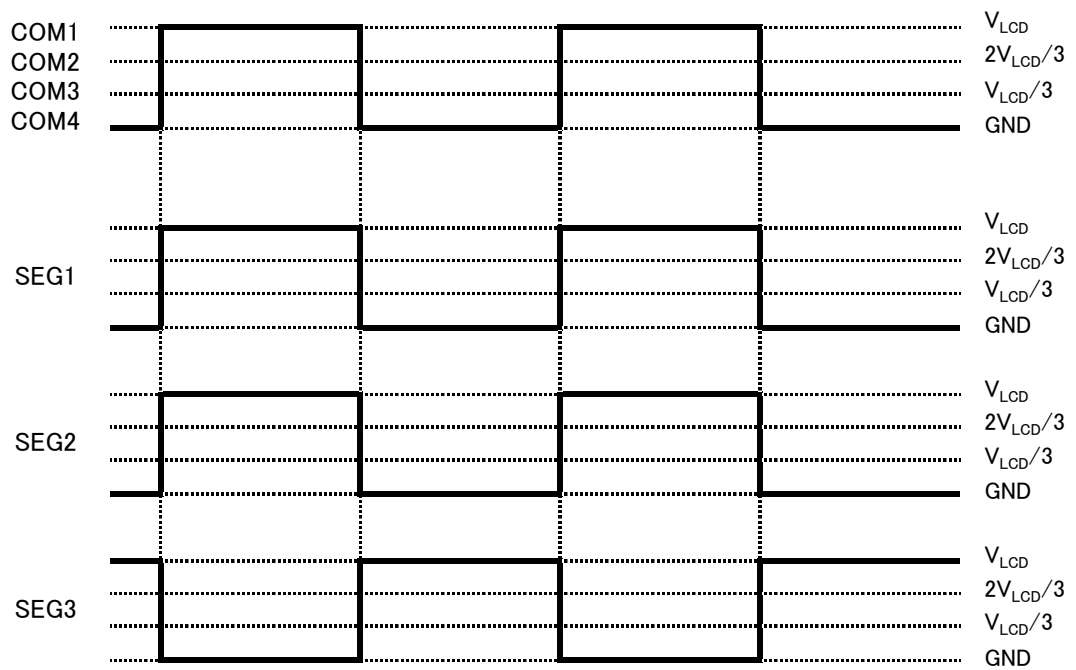
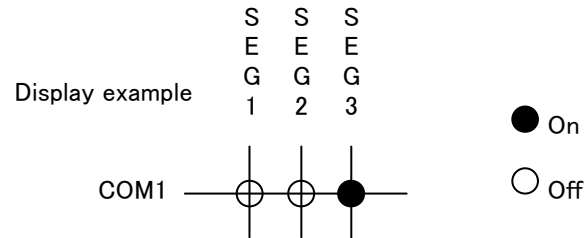
(3) At 1/3-duty



(4) At 1/4-duty

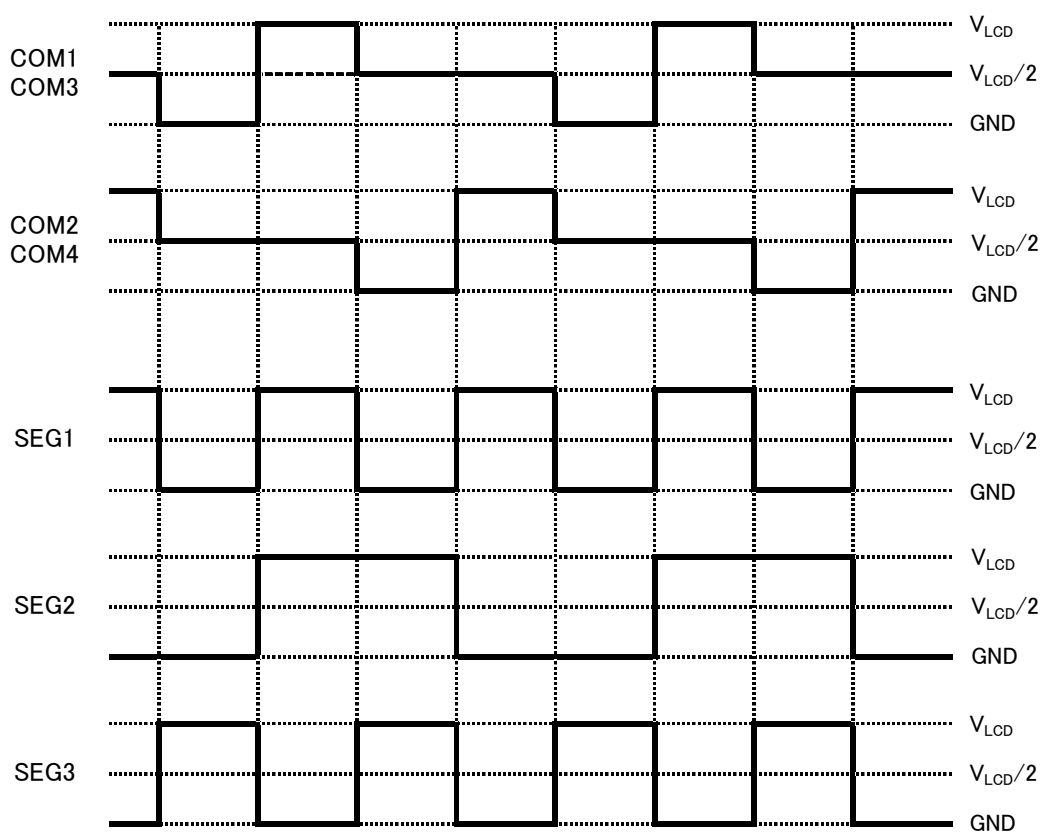
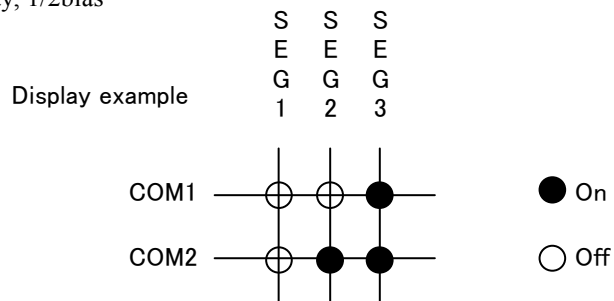


- Common segment output waveform
 - At Static



● Common and segment output waveforms

•At 1/2Duty, 1/2bias

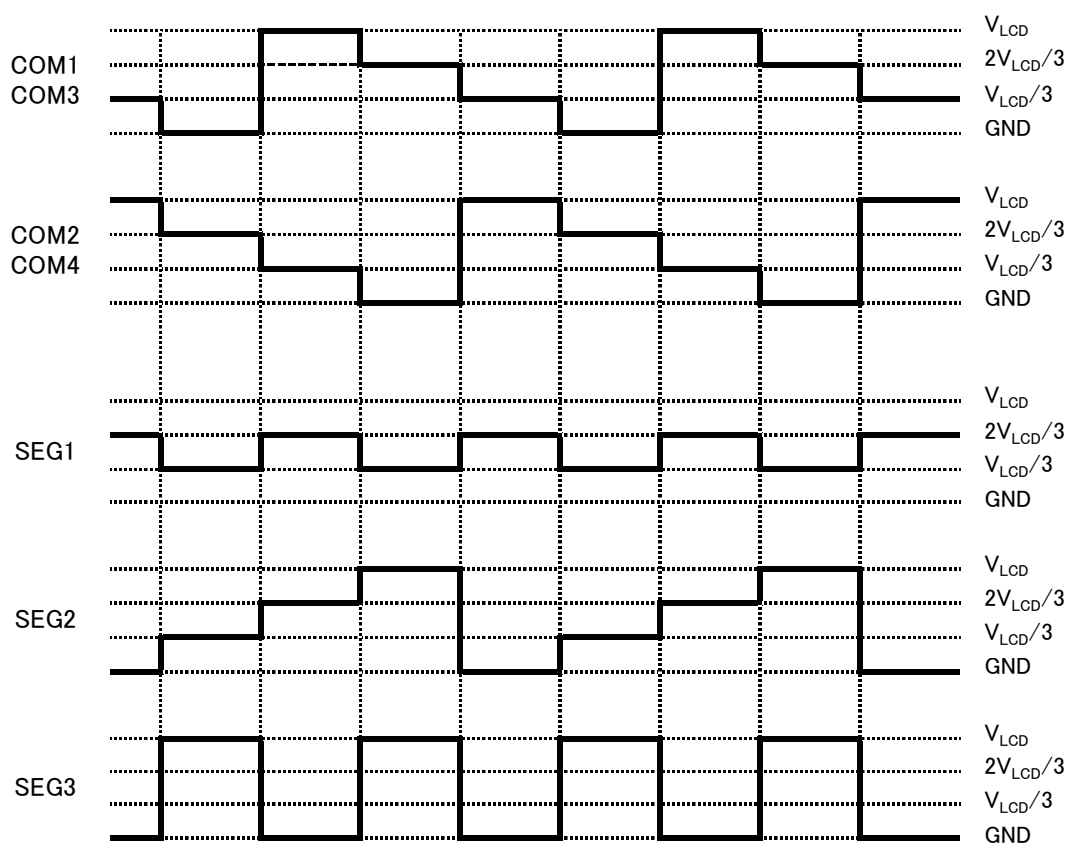
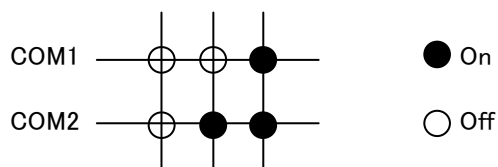


● Common segment output waveform

• At 1/2 Duty, 1/3bias

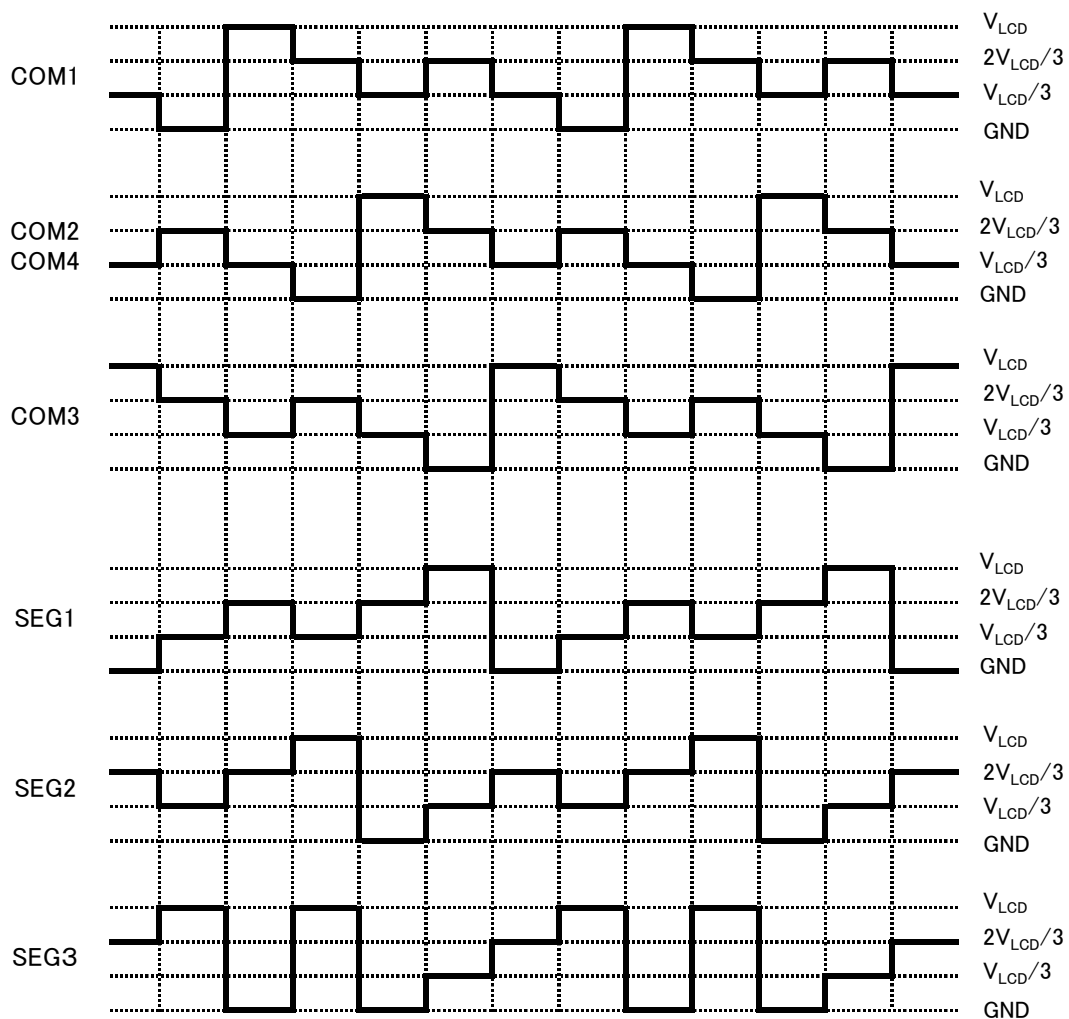
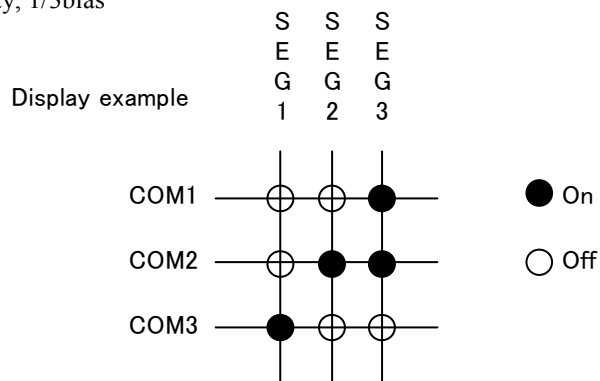
Display example

S	S	S
E	E	E
G	G	G
1	2	3



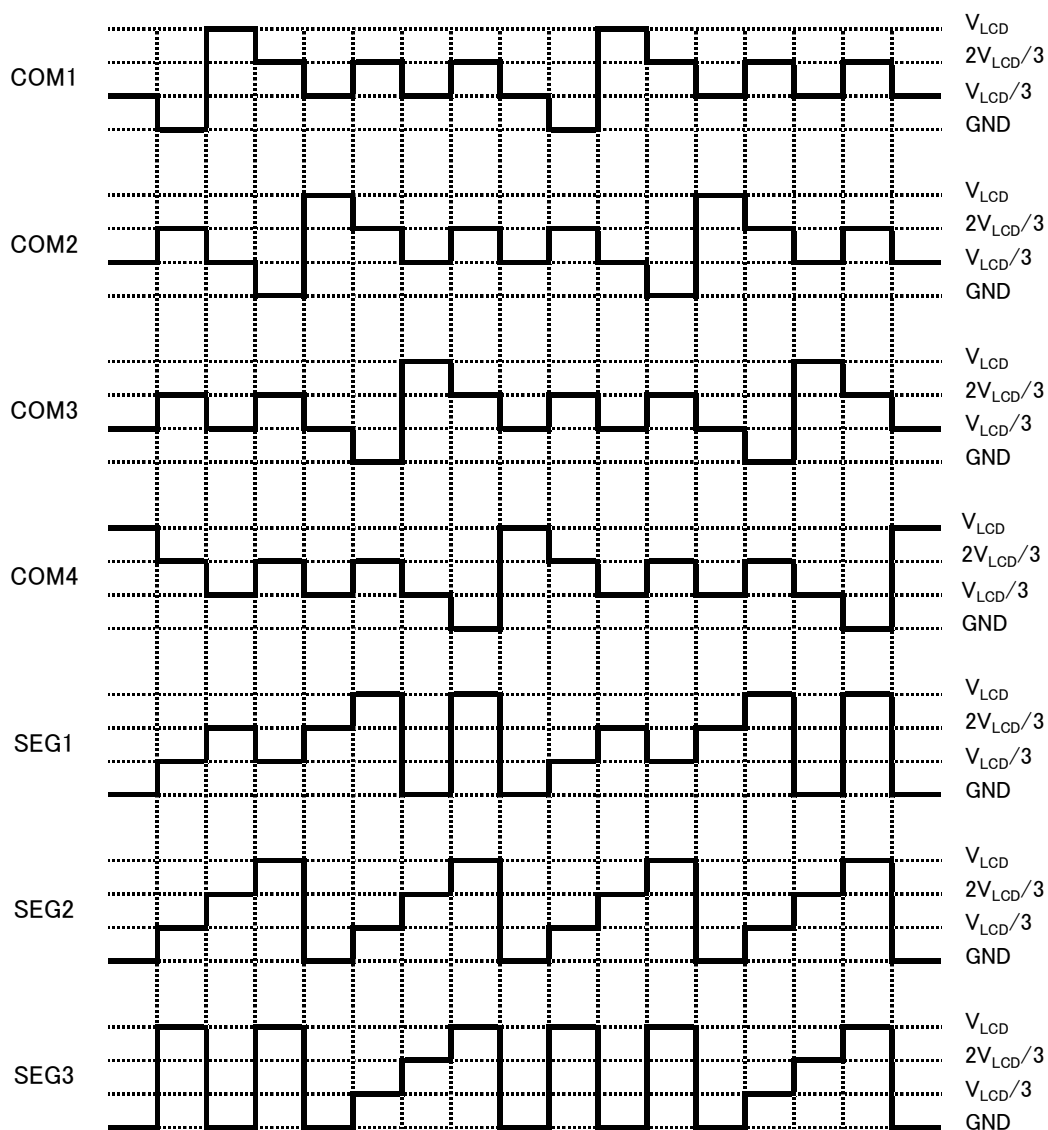
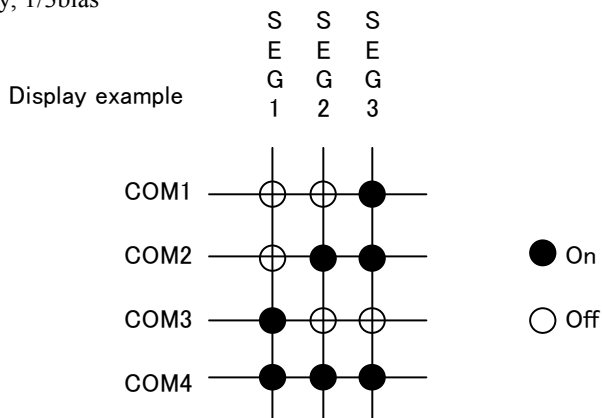
● Common and segment output waveforms

• At 1/3Duty, 1/3bias



● Common and segment output waveforms

• At 1/4Duty, 1/3bias



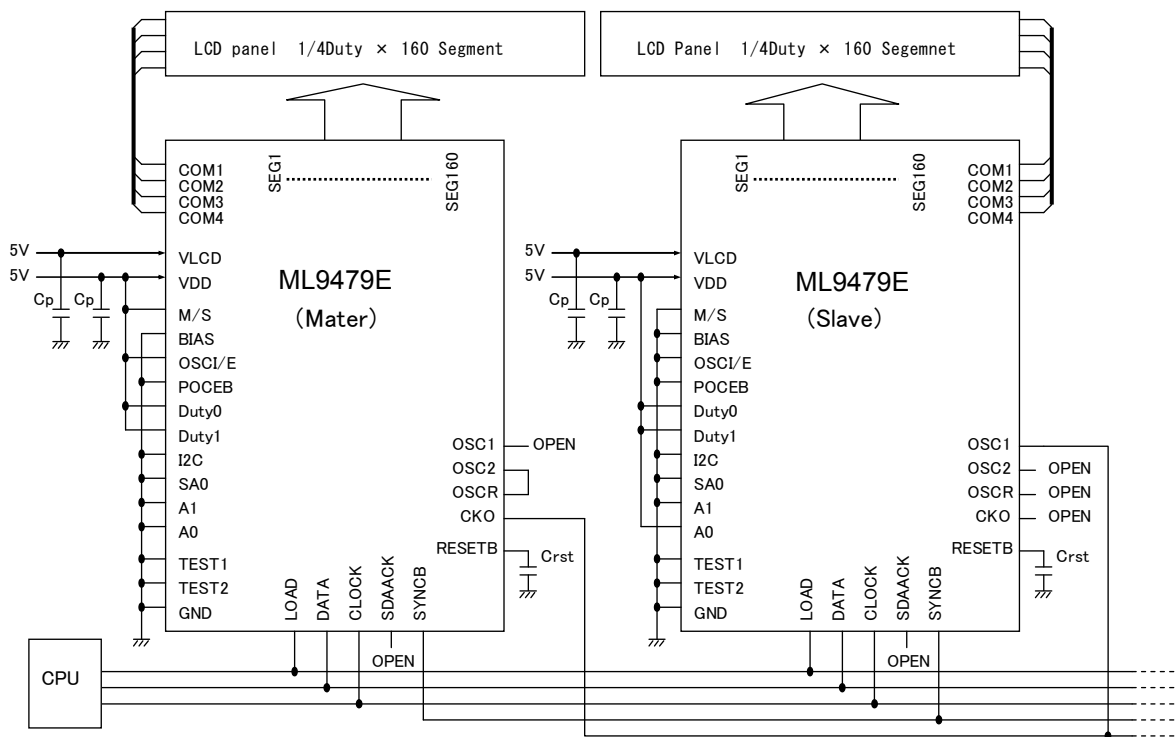
EXAMPLE OF APPLICATION CIRCUIT

Cascade configuration 1

Serial interface
 Internal CR oscillator circuit used
 1/4Duty
 RESETB pin + external capacitance connection to configure POC circuit
 The common waveform of master and slave chip is active.

[External component]

$C_p = 0.1 [\mu F]$ (bypass capacitor between power supplies)
 $Crst = 4.7 [\mu F]$ (capacitance for external POC circuit)

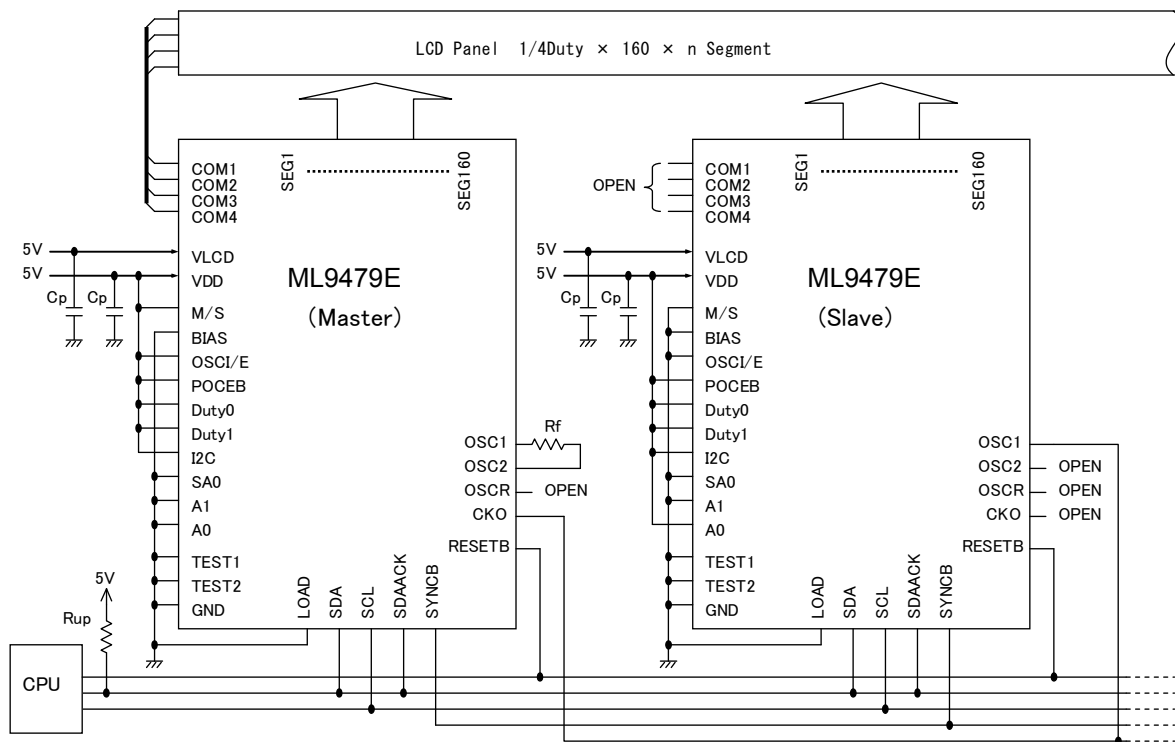


Cascade configuration 2

- I²C interface
- External Rf-based CR oscillator circuit used
- 1/4Duty
- External RESETB signal input
- The common waveform of slave chip is open.

[External component]

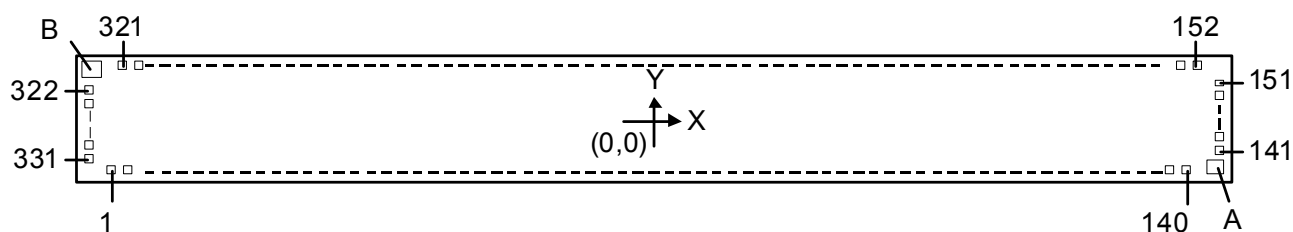
- Cp = 0.1 [μF] (bypass capacitor between power supplies),
- Rf = 470 [kΩ] (external R, resistor for CR oscillator circuit),
- Rup = Resistor for SDA data bus pull-up



PAD CONFIGURATION

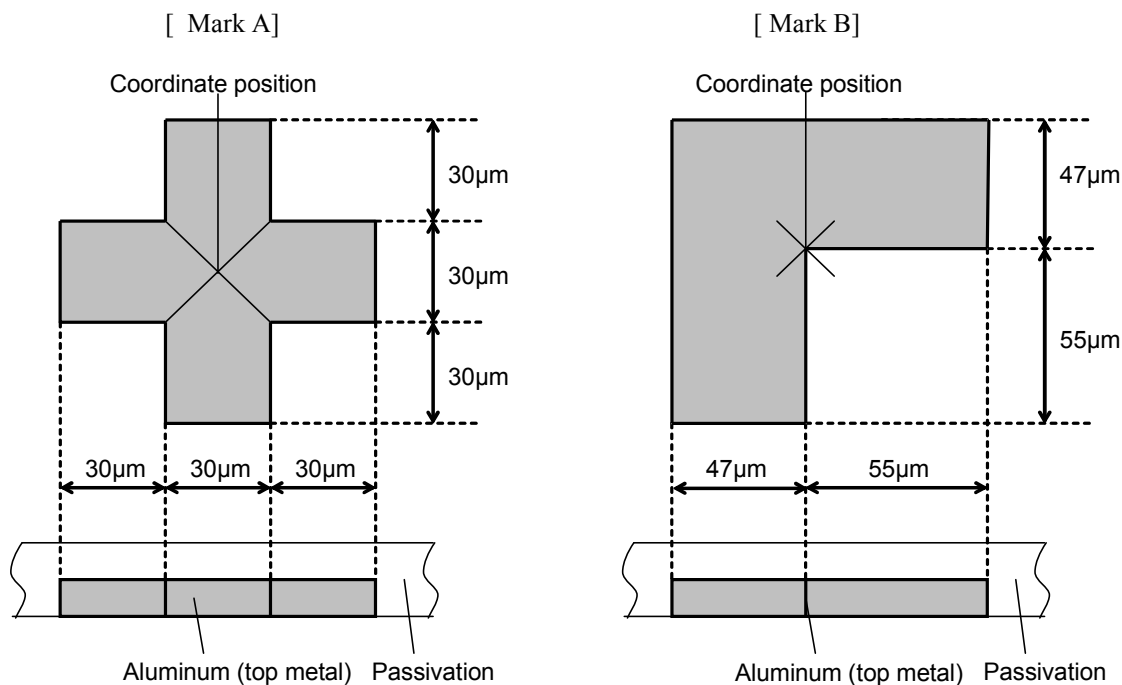
Pad layout (pattern face)

Chip size : 8.84 mm x 0.90 mm
 Chip thickness : 400 μm ± 20 μm
 Minimum bump pitch : 50 μm
 Bump height : 15 μm ± 3 μm



Bump and alignment mark dimensions (pattern face)

PAD No.1~140 : 35 μm x 72 μm
 PAD No.141~331 : 30 μm x 84 μm
 Alignment marks A and B : See below



Alignment mark	X-coordinate (μm)	Y-coordinate (μm)
Mark A	4308.9	-312.1
Mark B	-4305.9	305.9

Pad center coordinates

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
1 D	UMMY	-4236.2	-312.1	40	DATA(SDA)	-1863	-312.1
2 D	UMMY	-4176.2	-312.1	41	CLOCK(SCL)	-1767.8	-312.1
3 D	UMMY	-4116.2	-312.1	42	CLOCK(SCL)	-1711.8	-312.1
4 D	UMMY	-4056.2	-312.1	43	CLOCK(SCL)	-1655.8	-312.1
5 D	UMMY	-3996.2	-312.1	44	CLOCK(SCL)	-1599.8	-312.1
6 D	UMMY	-3936.2	-312.1	45	CLOCK(SCL)	-1543.8	-312.1
7 G	NDO	-3871	-312.1	46	LOAD	-1448.6	-312.1
8 G	NDO	-3815	-312.1	47	LOAD	-1392.6	-312.1
9 D	uty1	-3749	-312.1	48	LOAD	-1336.6	-312.1
10 D	uty1	-3693	-312.1	49	LOAD	-1280.6	-312.1
11 D	uty1	-3637	-312.1	50	LOAD	-1224.6	-312.1
12 D	uty1	-3581	-312.1	51	GND	-1154.4	-312.1
13 D	uty0	-3510.4	-312.1	52	GND	-1084.2	-312.1
14 D	uty0	-3454.4	-312.1	53	GND	-1028.2	-312.1
15 D	uty0	-3398.4	-312.1	54	GND	-972.2	-312.1
16 D	uty0	-3342.4	-312.1	55	GND	-916.2	-312.1
17 A	0	-3272	-312.1	56	GND	-860.2	-312.1
18 A	0	-3216	-312.1	57	GND	-804.2	-312.1
19 A	0	-3160	-312.1	58	GND	-748.2	-312.1
20 A	0	-3104	-312.1	59	VDD -653		-312.1
21 A	1	-3033.8	-312.1	60	VDD	-597	-312.1
22 A	1	-2977.8	-312.1	61	VDD	-541	-312.1
23 A	1	-2921.8	-312.1	62	VDD	-485	-312.1
24 A	1	-2865.8	-312.1	63	VDD	-429	-312.1
25 S	A0	-2795.6	-312.1	64	VDD	-373	-312.1
26 S	A0	-2739.6	-312.1	65	VDD	-317	-312.1
27 S	A0	-2683.6	-312.1	66	VLCD	-221.8	-312.1
28 S	A0	-2627.6	-312.1	67	VLCD	-165.8	-312.1
29 V	DDO	-2557.4	-312.1	68	VLCD	-109.8	-312.1
30 V	DDO	-2501.4	-312.1	69	VLCD	-53.8	-312.1
31 S	DAACK	-2406.2	-312.1	70	VLCD	2.2	-312.1
32 S	DAACK	-2350.2	-312.1	71	VLCD	58.2	-312.1
33 S	DAACK	-2294.2	-312.1	72	VLCD	114.2	-312.1
34 S	DAACK	-2238.2	-312.1	73	RESETB	209.6	-312.1
35 S	DAACK	-2182.2	-312.1	74	RESETB	265.6	-312.1
36 D	ATA(SDA)	-2087	-312.1	75	RESETB	321.6	-312.1
37 D	A(SDA)	-2031	-312.1	76	RESETB	377.6	-312.1
38 D	ATA(SDA)	-1975	-312.1	77	RESETB	433.6	-312.1
39 D	A(SDA)	-1919	-312.1	78	OSC1	503.8	-312.1

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Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
79 O	SC1	559.8	-312.1	124	BIAS	3251.4	-312.1
80 O	SC1	615.8	-312.1	125	TEST2	3321.6	-312.1
81 O	SC1	671.8	-312.1	126	TEST2	3377.6	-312.1
82 O	SC1	727.8	-312.1	127	TEST2	3433.6	-312.1
83 O	SC2	790.4	-312.1	128	TEST2	3489.6	-312.1
84 O	SC2	846.4	-312.1	129	TEST1	3559.8	-312.1
85 O	SC2	902.4	-312.1	130	TEST1	3615.8	-312.1
86	OSC2	958.4	-312.1	131	TEST1	3671.8	-312.1
87	OSC2	1014.4	-312.1	132	TEST1	3727.8	-312.1
88 O	SCR	1090.4	-312.1	133	GNDO	3798	-312.1
89 O	SCR	1146.4	-312.1	134	GNDO	3854	-312.1
90 O	SCR	1202.4	-312.1	135	DUMMY	3924.2	-312.1
91 O	SCR	1258.4	-312.1	136	DUMMY	3984.2	-312.1
92 O	SCR	1314.4	-312.1	137	DUMMY	4044.2	-312.1
93 C	KO	1389.8	-312.1	138	DUMMY	4104.2	-312.1
94 C	KO	1445.8	-312.1	139	DUMMY	4164.2	-312.1
95 C	KO	1501.8	-312.1	140	DUMMY	4224.2	-312.1
96 C	KO	1557.8	-312.1	141	DUMMY	4308.9	-232.2
97 C	KO	1613.8	-312.1	142	DUMMY	4308.9	-182.2
98 S	YNCB	1694	-312.1	143	COM1	4308.9	-132.2
99 S	YNCB	1750	-312.1	144	COM2	4308.9	-82.2
100 S	YNCB	1806	-312.1	145	COM3	4308.9	-32.2
101 S	YNCB	1862	-312.1	146	COM4	4308.9	17.8
102 S	YNCB	1918	-312.1	147	DUMMY	4308.9	67.8
103 V	DDO	2004.4	-312.1	148	DUMMY	4308.9	117.8
104 V	DDO	2060.4	-312.1	149	DUMMY	4308.9	167.8
105 I2C		2130.6	-312.1	150	DUMMY	4308.9	217.8
106 I2C		2186.6	-312.1	151	DUMMY	4308.9	267.8
107 I2C		2242.6	-312.1	152	DUMMY 4225		308.9
108 I2C		2298.6	-312.1	153	DUMMY 4175		308.9
109	M/S	2368.8	-312.1	154	DUMMY 4125		308.9
110 M	/S	2424.8	-312.1	155	SEG1	4075	308.9
111 M	/S	2480.8	-312.1	156	SEG2	4025	308.9
112 M	/S	2536.8	-312.1	157	SEG3	3975	308.9
113 P	OCEB	2607	-312.1	158	SEG4	3925	308.9
114 P	OCEB	2663	-312.1	159	SEG5	3875	308.9
115 P	OCEB	2719	-312.1	160	SEG6	3825	308.9
116 P	OCEB	2775	-312.1	161	SEG7	3775	308.9
117 O	SCI/E	2845.2	-312.1	162	SEG8	3725	308.9
118 O	SCI/E	2901.2	-312.1	163	SEG9	3675	308.9
119 O	SCI/E	2957.2	-312.1	164	SEG10	3625	308.9
120 O	SCI/E	3013.2	-312.1	165	SEG11	3575	308.9
121 B	IAS	3083.4	-312.1	166	SEG12	3525	308.9
122 B	IAS	3139.4	-312.1	167	SEG13 3475		308.9
123 B	IAS	3195.4	-312.1	168	SEG14 3425		308.9

ML9479E

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
169 S	EG15	3375	308.9	214 S	EG60	1125	308.9
170 S	EG16	3325	308.9	215 S	EG61	1075	308.9
171 S	EG17	3275	308.9	216 S	EG62	1025	308.9
172 S	EG18	3225	308.9	217 S	EG63	975	308.9
173 S	EG19	3175	308.9	218 S	EG64	925	308.9
174 S	EG20	3125	308.9	219 S	EG65	875	308.9
175 S	EG21	3075	308.9	220 S	EG66	825	308.9
176	SEG22 3025		308.9	221 S	EG67	775	308.9
177	SEG23 2975		308.9	222 S	EG68	725	308.9
178 S	EG24	2925	308.9	223 S	EG69	675	308.9
179 S	EG25	2875	308.9	224 S	EG70	625	308.9
180 S	EG26	2825	308.9	225 S	EG71	575	308.9
181 S	EG27	2775	308.9	226 S	EG72	525	308.9
182 S	EG28	2725	308.9	227 S	EG73	475	308.9
183 S	EG29	2675	308.9	228 S	EG74	425	308.9
184 S	EG30	2625	308.9	229 S	EG75	375	308.9
185 S	EG31	2575	308.9	230 S	EG76	325	308.9
186 S	EG32	2525	308.9	231 S	EG77	275	308.9
187 S	EG33	2475	308.9	232 S	EG78	225	308.9
188 S	EG34	2425	308.9	233 S	EG79	175	308.9
189 S	EG35	2375	308.9	234 S	EG80	125	308.9
190 S	EG36	2325	308.9	235 C	OM1	75	308.9
191 S	EG37	2275	308.9	236 C	OM2	25	308.9
192 S	EG38	2225	308.9	237 C	OM3	-25	308.9
193 S	EG39	2175	308.9	238 C	OM4	-75	308.9
194 S	EG40	2125	308.9	239 S	EG81	-125	308.9
195 S	EG41	2075	308.9	240 S	EG82	-175	308.9
196 S	EG42	2025	308.9	241 S	EG83	-225	308.9
197 S	EG43	1975	308.9	242 S	EG84	-275	308.9
198 S	EG44	1925	308.9	243 S	EG85	-325	308.9
199 S	EG45	1875	308.9	244	SEG86 -375		308.9
200 S	EG46	1825	308.9	245 S	EG87	-425	308.9
201 S	EG47	1775	308.9	246 S	EG88	-475	308.9
202 S	EG48	1725	308.9	247 S	EG89	-525	308.9
203 S	EG49	1675	308.9	248 S	EG90	-575	308.9
204 S	EG50	1625	308.9	249 S	EG91	-625	308.9
205 S	EG51	1575	308.9	250 S	EG92	-675	308.9
206 S	EG52	1525	308.9	251	SEG93 -725		308.9
207 S	EG53	1475	308.9	252	SEG94 -775		308.9
208 S	EG54	1425	308.9	253 S	EG95	-825	308.9
209 S	EG55	1375	308.9	254 S	EG96	-875	308.9
210 S	EG56	1325	308.9	255 S	EG97	-925	308.9
211 S	EG57	1275	308.9	256 S	EG98	-975	308.9
212	SEG58 1225		308.9	257 S	EG99	-1025	308.9
213	SEG59 1175		308.9	258 S	EG100	-1075	308.9
259 S	EG101	-1125	308.9	304 S	EG146	-3375	308.9
260 S	EG102	-1175	308.9	305 S	EG147	-3425	308.9
261 S	EG103	-1225	308.9	306 S	EG148	-3475	308.9
262 S	EG104	-1275	308.9	307 S	EG149	-3525	308.9

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Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
263 S	EG105	-1325	308.9	308 S	EG150	-3575	308.9
264 S	EG106	-1375	308.9	309 S	EG151	-3625	308.9
265 S	EG107	-1425	308.9	310 S	EG152	-3675	308.9
266 S	EG108	-1475	308.9	311 S	EG153	-3725	308.9
267 S	EG109	-1525	308.9	312 S	EG154	-3775	308.9
268 S	EG110	-1575	308.9	313 S	EG155	-3825	308.9
269 S	EG111	-1625	308.9	314 S	EG156	-3875	308.9
270 S	EG112	-1675	308.9	315 S	EG157	-3925	308.9
271 S	EG113	-1725	308.9	316 S	EG158	-3975	308.9
272 S	EG114	-1775	308.9	317 S	EG159	-4025	308.9
273 S	EG115	-1825	308.9	318 S	EG160	-4075	308.9
274 S	EG116	-1875	308.9	319 D	UMMY	-4125	308.9
275 S	EG117	-1925	308.9	320 D	UMMY	-4175	308.9
276 S	EG118	-1975	308.9	321 D	UMMY	-4225	308.9
277 S	EG119	-2025	308.9	322 D	UMMY	-4308.9	203.2
278 S	EG120	-2075	308.9	323 D	UMMY	-4308.9	153.2
279 S	EG121	-2125	308.9	324 D	UMMY	-4308.9	103.2
280 S	EG122	-2175	308.9	325 D	UMMY	-4308.9	53.2
281 S	EG123	-2225	308.9	326 C	OM4	-4308.9	3.2
282 S	EG124	-2275	308.9	327 C	OM3	-4308.9	-46.8
283 S	EG125	-2325	308.9	328 C	OM2	-4308.9	-96.8
284 S	EG126	-2375	308.9	329 C	OM1	-4308.9	-146.8
285 S	EG127	-2425	308.9	330 D	UMMY	-4308.9	-196.8
286 S	EG128	-2475	308.9	331 D	UMMY	-4308.9	-246.8
287 S	EG129	-2525	308.9				
288 S	EG130	-2575	308.9				
289 S	EG131	-2625	308.9				
290 S	EG132	-2675	308.9				
291 S	EG133	-2725	308.9				
292 S	EG134	-2775	308.9				
293 S	EG135	-2825	308.9				
294 S	EG136	-2875	308.9				
295 S	EG137	-2925	308.9				
296 S	EG138	-2975	308.9				
297 S	EG139	-3025	308.9				
298 S	EG140	-3075	308.9				
299 S	EG141	-3125	308.9				
300 S	EG142	-3175	308.9				
301 S	EG143	-3225	308.9				
302	SEG144 -3275		308.9				
303	SEG145	-3325	308.9				

REVISION HISTORY

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEDL9479E-01 M	May. 28,2012	–	–	Final edition 1 issued
FEDL9479E-02	Apr. 3,2013	10	10	BIAS="L": 1/2bias → BIAS="H": 1/2bias

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