

ML9488

Static, 1/2 Duty, 1/3 Duty, 1/4 Duty 80 Outputs LCD Driver

GENERAL DESCRIPTION

The ML9488 is an LCD driver LSI, consists of a 80-bit shift register, a 320-bit data latch, 80 sets of LCD drivers, and a common signal generation circuit.

It can directly drive an LCD up to 80 segments for static display, 160 segments for 1/2-duty display, 240 segments for 1/3-duty display, and 320 segments for 1/4-duty display.

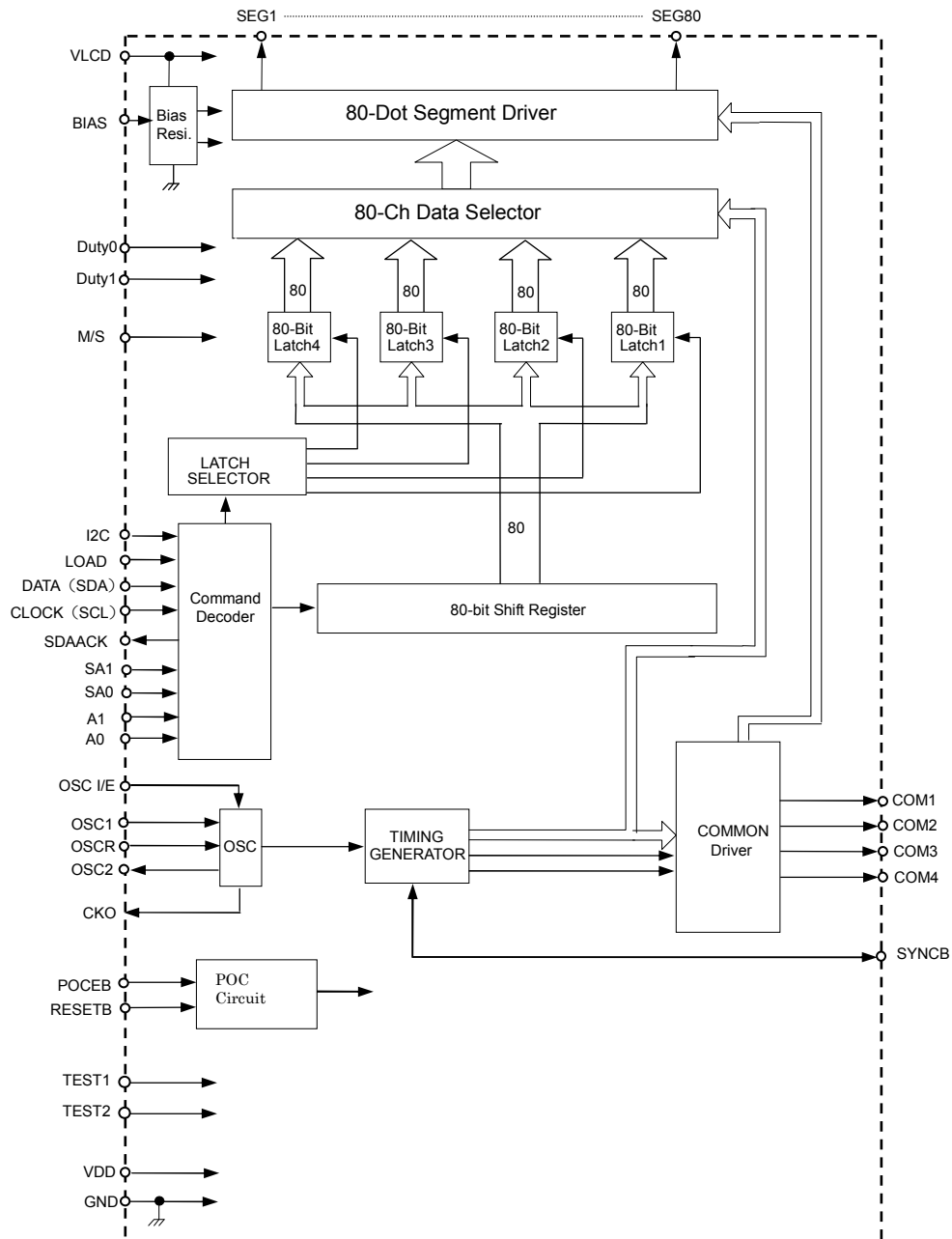
The three-wire serial interface and I²C interface are selectable.

FEATURES

- Logic power supply voltage : 2.7 to 5.5 V
- LCD drive power supply voltage : 4.5 to 5.5 V
- Maximum number of segments
 - Static display : 80 segments
 - 1/2-duty display : 160 segments
 - 1/3-duty display : 240 segments
 - 1/4-duty display : 320 segments
- Interface with microcomputer :
 - Serial interface : DATA, CLOCK, LOAD
 - CLOCK transfer speed up to 1 MHz
 - I²C interface : SDA, SCL, SDAACK
 - SCL transfer speed up to 400 kHz
- Built-in CR oscillator circuit using the internal resistor or External resistor
- Cascade connectable (up to sixteen chips)
- Built-in common signal generation circuit
- Built-in common output intermediate-value voltage generation circuit
- Built-in POC (Power On Clear) circuit
- Gold bump chip (ML9488DVWA)
- Comparison table

Item ML	9478CDVWA	ML9488DVWA
Frame Frequency (Internal oscillation)	65Hz/75Hz/85Hz/95Hz (programmable)	130Hz/150Hz/170Hz/190Hz (programmable)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	$T_a = 25^{\circ}\text{C}$	-0.3 to 6.0	V
LCD drive power supply voltage	V_{LCD}	$T_a = 25^{\circ}\text{C}$	-0.3 to 6.0	V
Input voltage	V_I	$T_a = 25^{\circ}\text{C}$	- 0.3 to $V_{DD} + 0.3$	V
Output short-circuit current	I_S	$T_a = 25^{\circ}\text{C}$	-2.0 to +2.0	mA
Chip temperature	T_c —		125 °C	
Storage temperature	T_{STG}	— -55	to +150	°C

Note: Do not use the ML9488 by short-circuiting one output pin to another output pin as well as to other pin (input pin, input/output pin, or power supply pin).

RECOMMENDED OPERATION CONDITIONS

Item	Symbol	Condition	Range	Unit
Logic power supply voltage	V_{DD}^*	—	2.7 to 5.5	V
LCD drive power supply voltage	V_{LCD}^*	—	4.5 to 5.5	V
OSC IN clock frequency	f_{CP1}	—	up to 10	kHz
Data clock frequency	f_{CP2}	—	up to 1.0	MHz
SCL clock frequency	f_{SCL}	—	up to 400	kHz
Operating temperature	T_a	—	-40 to +105	°C

Note(*): Use at $V_{DD} \leq V_{LCD}$.

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$$f_{FRM} = f_{OSC} / 24$$

Recommended setting range for external component (oscillator circuit)

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^{\circ}\text{C}$)

Item	Symbol	Condition	Min T	YP	Max	Unit
Oscillation resistor	R_f	—	423	470	517	kΩ
Frame frequency	f_{FRM}	(F1,F0)=(0,1)	47	75	114	Hz

The relation between oscillation resistor and frame frequency is as the equation below.

$$f_{FRM} = f_{OSC} / (8 \times 24)$$

$$f_{osc} = 1 / (\text{Device coefficient} \times \text{External resistor } R_f)$$

$$\text{Device coefficient} = 73.8 \times 10^{-12} \pm 25\%$$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min. T	yp.	Max.	Unit	Applicable pin
"H" input voltage	V _{IH}	— 0.8V	DD	— V	DD V		(*1)
"L" input voltage	V _{IL}	— GND		—	0.2V _{DD}	V	(*1)
Input leakage current 1	I _{L1}	V _I = V _{DD} or 0 V	-1.0	—	1.0	μA	(*1)
Input leakage current 2	I _{L2}	V _I = V _{DD} or 0V POCEB = "H"	-1.0	— 1.0		μA	RESET B
Pull-up current	I _{pu}	V _{DD} = 5.0V, V _I = 0 V POCEB = "L"	30	— 140		μA	RESET B
"H" output voltage	V _{OH}	I _O = -600μA	0.9V _{DD}	— —		V	CKO, SYNCB
"L" output voltage 1	V _{OL1}	I _O = 600μA	—	—	0.1V _{DD}	V	CKO, SYNCB
"L" output voltage 2	V _{OL2}	I _O = 600μA	—	—	0.1V _{DD}	V	SDAACK
Driver ON resistor	Segment	V _{OHS}	V _{LCD} = 5V	— 5		15	kΩ SEG1 to SEG80
	Common	V _{OHC}	V _{LCD} = 5V	— 5		12	kΩ COM 1 to COM4

(*1): DATA(SDA), CLOCK(SCL), LOAD, M/S, SYNCB, Duty1, Duty0, BIAS, SA1, SA0, A1, A0, OSC1, OSC I/E, I2C, POCEB

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max. U	nit	Applicable pin
Static supply current	I _{DD5}	V _{DD} =V _{LCD} =5.5 V Input pin fixed to "H" or "L"	— 8		15	μA	VDD
	I _{LCD5}	Oscillation stopped, output no-load POCEB="L"	— 9		15	μA	VLCD
Dynamic supply current 1	I _{DD1}	V _{DD} =V _{LCD} = 5.5 V (*2)(*3) Clock OSC1 external input f _{CP1} =1.8kHz	(*6) — 11		20	μA	VDD
	I _{LCD1}		(*7) — 10		17	μA	VLCD
Dynamic supply current 2	I _{DD2}	V _{DD} =V _{LCD} = 5.5 V (*2)(*3) Internal oscillation	(*6) — 62		92	μA	VDD
	I _{LCD2}		(*7) — 10		17	μA	VLCD
Dynamic supply current 3	I _{DD3}	V _{DD} =V _{LCD} = 5.5 V (*2)(*4)(*6) Internal oscillation	— 131		252	μA	VDD
	I _{LCD3}	At three-wire serial IF data input	— 10		17	μA	VLCD
Dynamic supply current 4	I _{DD4}	V _{DD} =V _{LCD} = 5.5 V (*2)(*5)(*6) Internal oscillation	— 203		332	μA	VDD
	I _{LCD4}	At I ² C IF data input	— 10		17	μA	VLCD

(*2): M/S = "H", 1/4-duty, 1/3-bias, (F1,F0) = (1,1) 190 Hz, POCEB = "L", output pin no-load.

(*3): Three-wire serial or I²C interface. Input pin fixed to "H" or "L".

(*4): Serial interface, data input frequency = 1 MHz.

(*5): I²C interface, data input frequency = 400 kHz.

(*6): Alternately inputs "0" and "1" for LCD display data (checkered display).

(*7): Inputs all "1s" for LCD display data (all illuminated).

Switching Characteristics

- OSC timing

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
OSC IN clock frequency (external input)	f_{CP1}	Clock input from OSC1. OSC2 and OSCR open. OSC I/E = "L"	—	1.8	10	kHz	OSC1
Clock pulse width (External input)	t_{WCP1}		—	—	—	μs	SC1
Clock rise and fall time (external input)	t_{OSC}		—	— (*1)	—	μs	SC1
External Rf clock frequency (Internal oscillation)	f_{OSC1}	Between OSC1 and OSC2 $R_f = 470\text{k}\Omega$ (F1,F0)=(0,1) OSCR open. OSC I/E = "H"	18	28.8	44	kHz	OSC1, OSC2
Internal clock frequency (Internal oscillation)	f_{OSC2}	OSC1 open. (F1,F0)=(0,1) OSC2 and OSCR short-circuited. OSC I/E = "H"	18	28.8	44	kHz	OSC1, OSCR, OSC2

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$$f_{FRM} = f_{OSC} / 24$$

(*1) t_{OSC} is a reference value.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: $\text{max}=2\mu\text{s}$.

- Serial interface timing

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Data clock frequency	f_{CP2}		—	—	1	MHz	CLOCK
Data clock pulse width	t_{WCP2}		100	—	—	ns	CLOCK
Data setup time	t_{SU}		50	—	—	ns	DATA
Data hold time	t_{HD}		50	—	—	ns	CLOCK
CLOCK-LOAD timing	t_{CL}		100	—	—	ns	CLOCK
LOAD-CLOCK timing	t_{LC}		100	—	—	ns	LOAD
LOAD pulse width	t_{WLD}		100	—	—	ns	LOAD
Signal rise and fall time	t_{sr}, t_{sf}		—	—	(*2)	ns	CLOCK, DATA, LOAD

(*2) t_{sr} and t_{sf} shall be reference values.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: $\text{max}=10\text{ns}$.

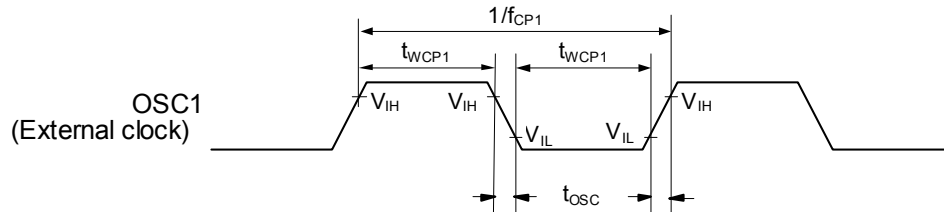
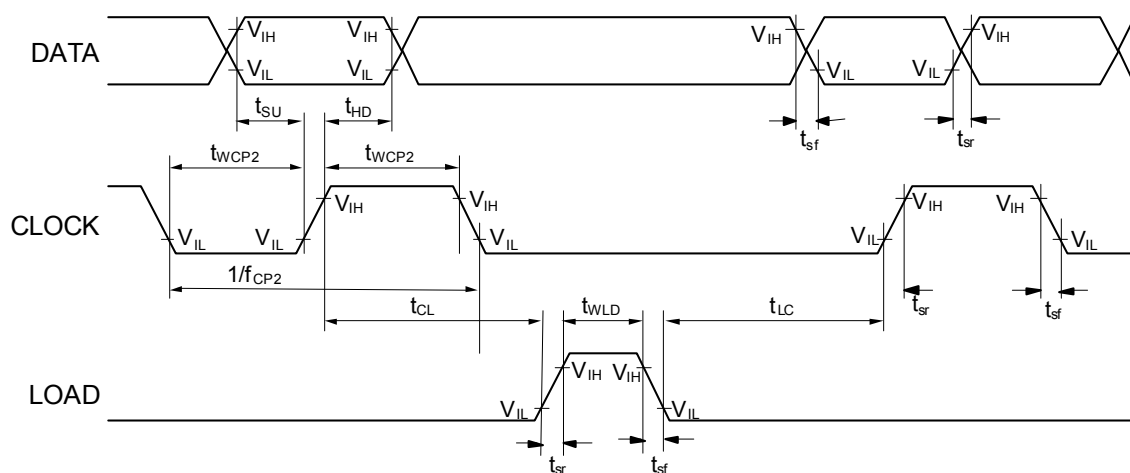
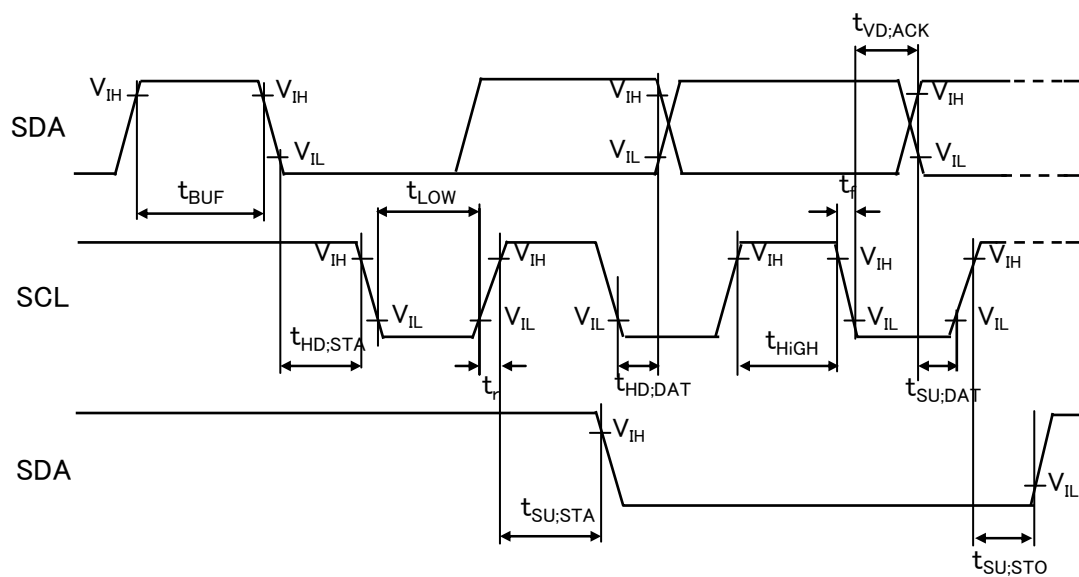
- I²C interface timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
SCL clock frequency	f _{SCL}		—	—	400	kHz	SCL
Hold time (repeat) "STATRT" condition	t _{HD,STA}		0.6	—	—	μs	SCL,SDA
SCL "L" pulse width	t _{LOW}		1.3	—	—	μs	SCL
SCL "H" pulse width	t _{HIGH}		0.6	—	—	μs	SCL
Setup time for repeat "START" condition	t _{SU,STA}		0.6	—	—	μs	SCL,SDA
Data hold time	t _{HD,DAT}		0	—	—	ns	SCL,SDA
Data setup time	t _{SU,DAT}		200	—	—	ns	SCL,SDA
Setup time for "STOP" condition	t _{SU,STO}		0.6	—	—	μs	SCL,SDA
Bus free time between "STOP" condition and "START" condition	t _{BUF}		1.3	—	—	μs	SCL
Data valid acknowledge time	t _{VD,ACK}		—	—	1.2	μs	SCL,SDAAACK
Signal rise and fall time	t _{ir,tif}		—	—	(*3)	μs	SCL,SDA
Data bus load capacitance	C _b		—	—	400	pF	SDA,SDAACK
Noise pulse width tolerance	t _{wf}		—	—	50	ns	SCL,SDA

(*3) t_{ir} and t_{tif} shall be reference values.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: max=0.1μs.

Timing chart (OSC1)**Timing chart (Serial interface)****Timing chart (I²C interface)**

REFERENCE DATA

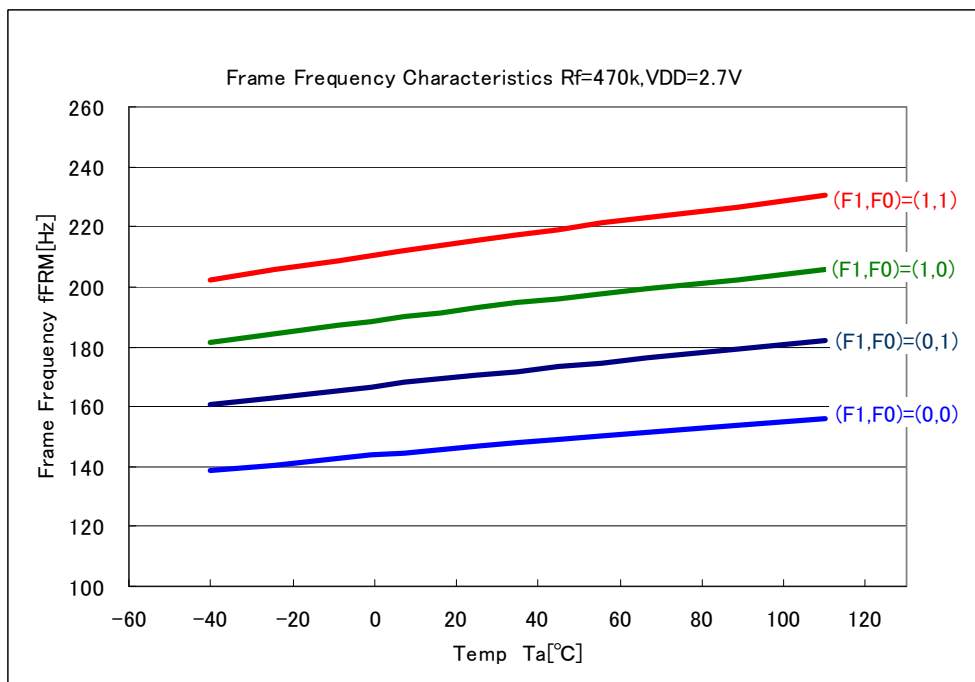
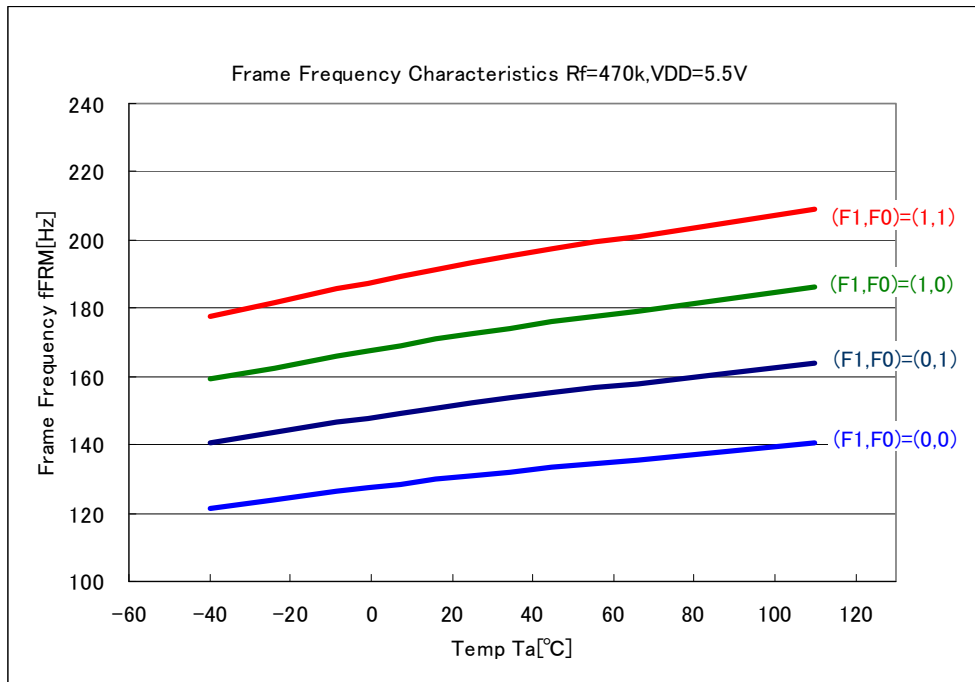
Frame frequency Characteristics

VDD=5.5V/2.7V Rf=470kΩ

Frame frequency $f_{\text{FRM}} = f_{\text{OSC}} / (8 \times 24)$

$f_{\text{osc}} = 1 / (\text{Device coefficient} \times \text{External resistor } R_f)$

Device coefficient = $73.8 \times 10^{-12} \pm 25\%$



POWER ON/OFF TIMING

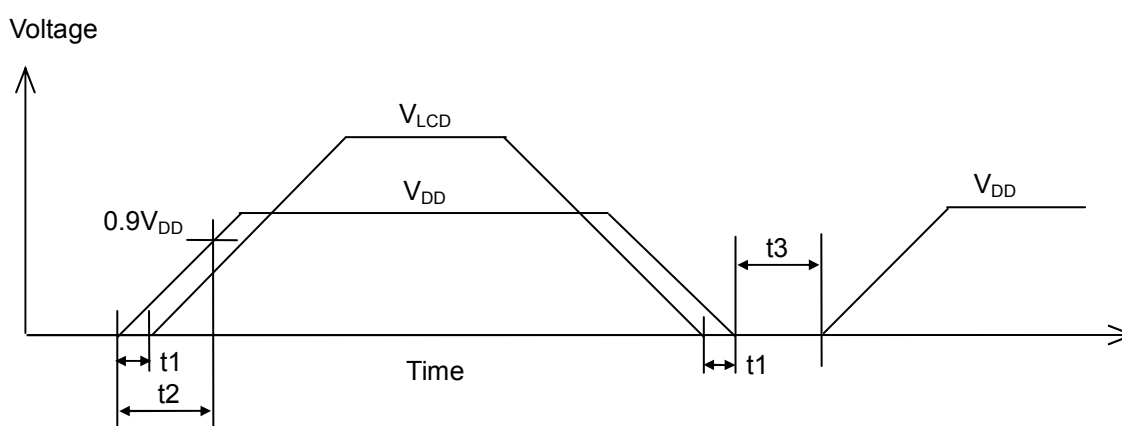
To turn on the power supply, raise the logic power supply first, then LCD drive power supply in order to prevent the IC from malfunctioning.

To fall the power supply, fall the LCD drive power supply first, then the logic power supply.

For a VDD pin ranging from 0 V to VDDmin, set $VDD \geq V_{LCD}$ and $t1 \geq 0$ [ns].

To enable the Internal POC circuit, the VDD power supply rise time $t2$ range needs to be $100 [\mu s] \leq t2 \leq 500$ [ms].

For the VDD power supply to turn OFF then turn ON again, it is necessary to secure the POC discharge time $t3 \geq 100$ [ms].

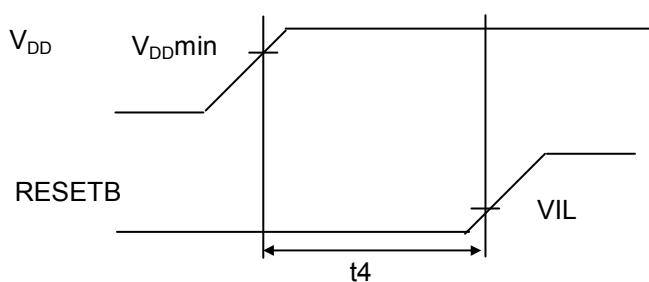


INITIALIZATION SIGNAL TIMING

When RESETB signal is externally input

The RESETB pin input is valid both for POCEB = "L" and "H". Usable in combination with the POC.

Keep the RESETB pin at "L" level until the VDD reaches VDDmin. ($t4 \geq 200$ [ns])



When Internal POC circuit is used

When using the Internal POC circuit in the initialization, set the POCEB pin to "L".

Leave the RESETB pin open.

PIN DESCRIPTIONS

Pad number	Symbol I/O		Description
67-68 M	/S	I	This is the input to switch between the master and slave modes. It has a schmitt circuit. When this pin is "H", the mode is master. When this pin is "L", the mode is slave.
6-7 4-5	Duty0 Duty1 *1	I	Display duty switch pins. These have schmitt circuits. Duty0="L", Duty1="L" : Static (COM1=COM2=COM3=COM4) Duty0="H", Duty1="L" : 1/2Duty (COM1=COM3, COM2=COM4) Duty0="L", Duty1="H" : 1/3Duty (COM2=COM4) Duty0="H", Duty1="H" : 1/4Duty
73-74 BIAS		I	This pin sets the LCD bias. It has a schmitt circuit. BIAS= "L": 1/3bias BIAS= "H": 1/2bias When the static mode selection, fix this pin at "H" or "L" level.
14-15 12-13	SA1 SA0	I	Slave address input pins. These have schmitt circuits.
10-11 8-9	A1 A0	I	Sub address input pins. These have schmitt circuits.
71-72 O	SC I/E	I	This input selects whether to use the external clock input mode or to use the Internal oscillation mode or external oscillation mode. It has a schmitt circuit. When this pin is "H", the mode is the Internal or external Rf oscillation mode. When this pin is "L", the mode is the external clock input mode. Use the slave chip as it is connected to GND.
46-48 53-55 49-52	OSC1, OSCR, OSC2 *2	I I O	These pins are for the oscillator circuit to generate common signals. The OSC1 and OSC2 pins are input pins and have a schmitt circuit. OSC2 is an output pin. It becomes an output when the OSC I/E pin = "H" and a high impedance when the OSC I/E pin = "L". 【 In the master mode (M/S pin = "H") 】 Three types are selectable: Internal oscillation mode, external oscillation mode, and external clock input mode. •Internal oscillation mode: Set the OSC I/E pin to "H", short the OSC2 and OSC1 pins, and open the OSC1 pin. •External Rf oscillation mode: Set the OSC I/E pin to "H", connect an oscillation resistor Rf between the OSC1 and OSC2 pins, and open the OSC2 pin. •External clock input mode: Set the OSC I/E pin to "L", open the OSC2 and OSC1 pins, and input the external clock to the OSC1 pin. 【 In the slave mode (M/S pin = "L") 】 Open the OSC2 and OSC1 pins and connect the OSC1 pin to the ML9488's CKO pin that has been set to the master mode.
56-56	CKO	O	Clock output pin. In the master mode (M/S pin = "H"), the 1/16 division signal of the oscillation frequency is output. In the slave mode (M/S pin = "L"), the output is fixed to "L". For a cascade connection, connect this pin to the OSC1 pin of the chip that has been set to the slave mode.

60-63 SY	NCB	I/O	Input/output pin for common synchronization. It has a schmitt circuit. It becomes the synchronization signal output pin in the master mode (M/S pin = "H"). It becomes the synchronization signal input pin in the slave mode (M/S pin = "L"). For cascade connection, connect all of the involved ML9488s' SYNC pins by the common line.
65-66	I2C	I	Interface switching pin. It has a schmitt circuit. When this pin is "H", the interface is I ² C. When this pin is "L", the interface is three-wire serial.
20-21	DATA (SDA)	I	Display data input pin. It has a schmitt circuit. I2C="L": Serial interface; DATA Input the display data in the order of SEG80, SEG79, ... , SEG2, and SEG1. The display data turns on at "H" and turns off at "L". I2C="H": I ² C interface; SDA Input the display data in units of 8 bits. The display data turns on at "H" and turns off at "L". This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
22-23	CLOCK (SCL)	I	Shift clock input pin for display data. It has a schmitt circuit. I2C="L": Serial interface; CLOCK The display data input to the DATA pin is serially input to the shift register at the CLOCK signal rise. I2C="H": I ² C interface; SCL The display data input to the SDA pin is serially input to the shift register at the SCL signal rise. This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
24-25	LOAD	I	Input pin for the load signal of display data. It has a schmitt circuit. I2C="L": Serial interface; LOAD The display data in the shift register is transmitted as is to the segment driver for the "H" duration. When this pin is brought into "L", the shift register is disconnected from the segment driver. The display data in the shift register immediately before it become "L" is held in the data latch and transmitted to the segment driver. I2C="H": I ² C interface Use this pin as it is connected to GND.
17-19	SDAACK	O	I2C="L": Serial interface Use this pin as it is opened. I2C="H": I ² C interface The I ² C bus acknowledge output signal. Normally, use it as it is connected with the SDA pin. Connect an external pull-up resistor whenever necessary, as it is an open drain pin. The pull-up connection destination supply voltage shall be the V _{DD} supply voltage or less.
69-70	POCEB	I	Internal POC circuit enable pin. It has a schmitt circuit. When this pin is "H", the POC circuit becomes OFF and the constant current (8μA) is cut. The RESETB pin pull-up resistor is cut as well. When this pin is "L", the POC circuit becomes ON. The RESETB pin is connected to a pull-up resistor.
44-45	RESETB *3	I	Reset signal input pin for initializing inside the IC. It has a schmitt circuit. The "L" level enables the reset. This pin has an Internal pull-up resistor. When POCEB = "H", input the external reset signal to this pin. When POCEB = "L", the power-on reset operation is available by open this pin.

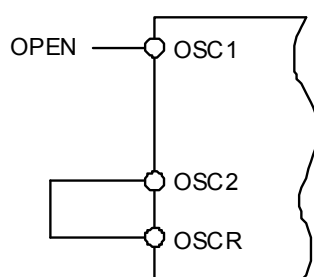
77-78 75-76	TEST1 TEST2	I	Pin for testing the IC. It has an Internal pull-down resistor. Use it as it is connected to GND.
95-134 139-178	SEG1 ~SEG80	O	Outputs for LCD display. Connected to the segment pins on the LCD panel. In the display off mode, all the outputs are fixed to GND.
85-88 135-138 183-186	COM1 ~COM4	O	Outputs for LCD display. Connected to the common pins on the LCD panel. The output pins are located at three positions: both ends of the chip and between SEG40 and SEG41. Each is connected inside the chip. Use the COM pins in accordance with the panel to be used. In the display off mode, all the outputs are fixed to GND. When the slave is set (M/S="L"), COM1 to COM4 outputs are GND level fixed.
32-37	VDD	-	Power supply pin for logic circuit.
38-43	VLCD	-	Power supply pin for LCD driver.
26-31 G	ND	-	Ground pin.
16 64	VDDO -		VDD output pin. Use this pin when fixing the mode setting input pin to "H" on the COG.
3 79	GNDO -		Ground output pin. Use this pin when fixing the mode setting input pin to "L" on the COG.
1-2 80-84 89-94 179-182 187-190	DUMMY -		Floating pin. At this time, avoid this pin from shorting with pins other than DUMMY in the wiring on the COG.

*1: For details of the COM /SEG waveform when a duty is selected, refer to "Common waveform" on page 18 and "Common Segment waveform" on page 19 to 23.

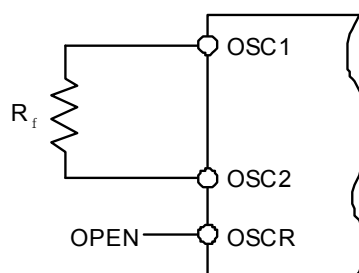
*2: Oscillator circuit configuration

- When M/S = "H", OSC I/E = "H"

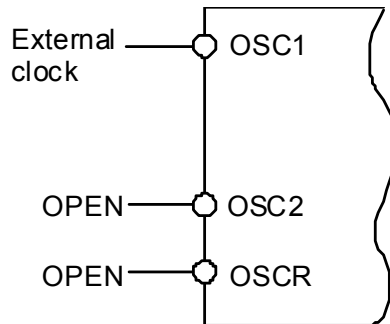
[Internal Rf oscillation mode]



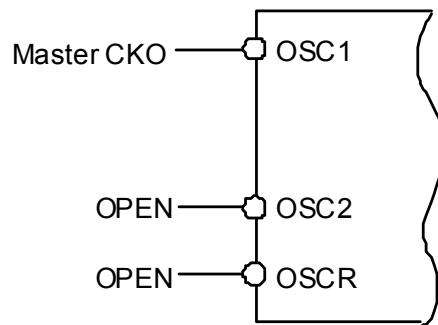
[External Rf oscillation mode]



- External clock input mode when M/S = "H" and OSC I/E = "L"

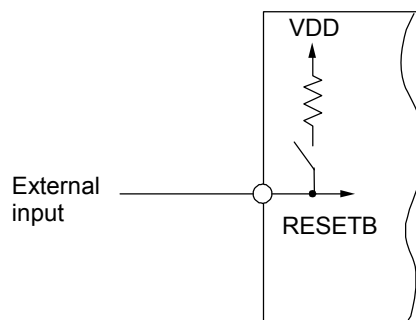


- M/S = "L", slave mode, external clock input mode

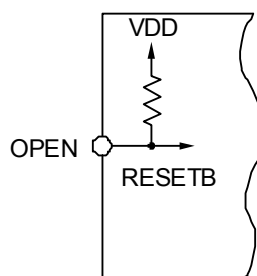


*3: Reset circuit configuration

- External input to RESTB when POCEB = "H"



- POC circuit configuration when POCEB = "L"



DESCRIPTION

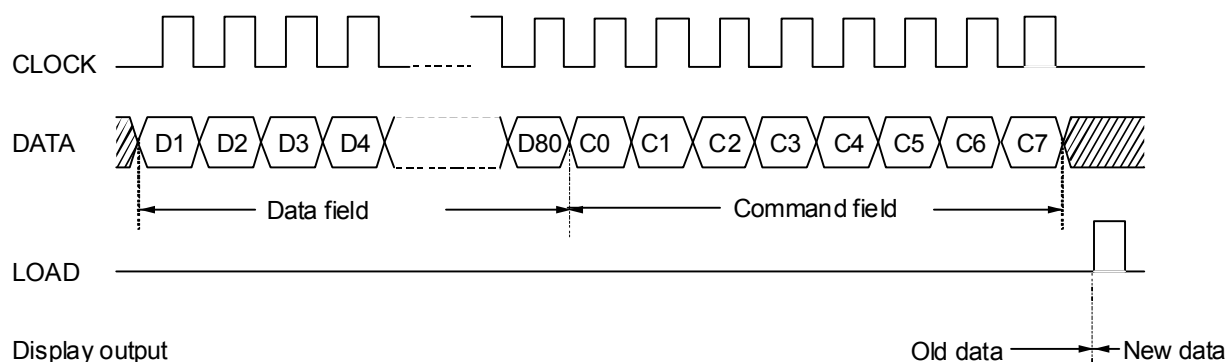
Operation description (Serial interface)

• Display data input

As described in the Data configuration section, the display data consists of the data field that corresponds to each segment on/off and the command field that indicates the display data input.

When inputting the display data, the "F3" command is set in the command field. When the "F1" or "F2" command is set in the command field, the display data in the data field becomes invalid.

The data input to the DATA pin is loaded to the shift register at the CLOCK pulse rise, transferred to the display data latch during the LOAD pulse at the "H" level, then output via the segment driver.

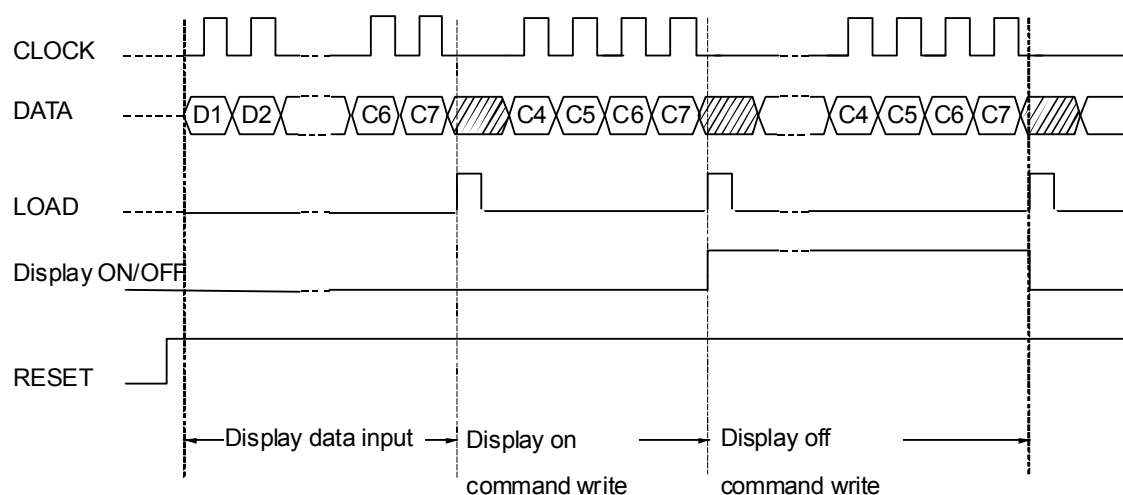


• Display on, Display off

The display becomes off at power-on reset. To display, write the display on command.

The display off is the command that makes all segments off. Writing the display off command turns off the lights regardless of the display data.

The display on is the command to release the display off. Writing the display on command returns the display to the original state.



List of Commands

Command name	C7	C6	C5	C4	C3	C2	C1	C0	Operation
F0 0		0	0	0	x	x	x	x	Disabled
F1 0		1	F1 (*2)	F0 (*2)	x x		x	x	Frame frequency setting (F1,F0)=(0, 0): 130Hz (F1,F0)=(0, 1): 150Hz (F1,F0)=(1, 0): 170Hz (F1,F0)=(1, 1): 190Hz (valid for Internal CR oscillation)
F2 1		0	1	D (*2)	x x		x	x	Display on/off "0": O ff (COM=SEG=GND) "1": O n
F3(*1) 1		1	SA1	SA0	A1	A0	Co1	Co0	Data write address setting (Co1,Co0)=(0, 0): Corresponding to common 1 (Co1,Co0)=(0, 1): Corresponding to common 2 (Co1,Co0)=(1, 0): Corresponding to common 3 (Co1,Co0)=(1, 1): Corresponding to common 4 SA1, SA0, A1, A0: Chip address

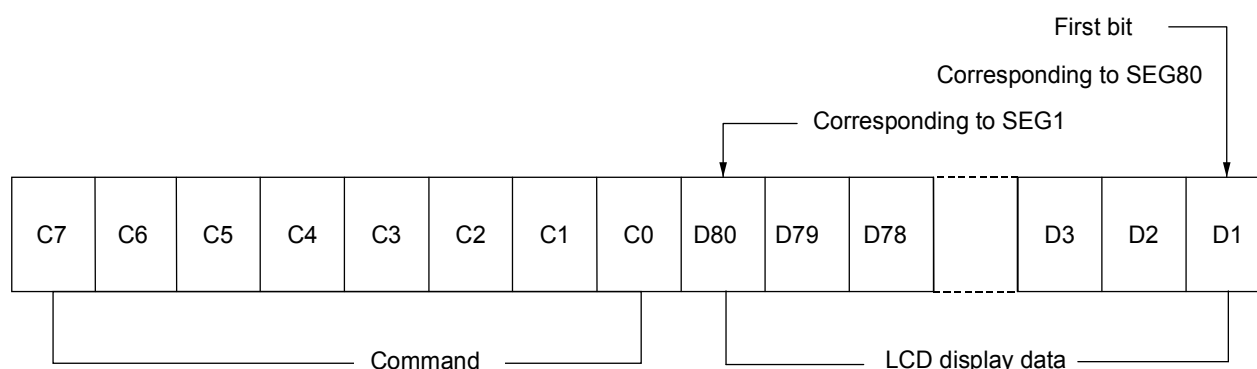
x : Don't care

(*1): For the I²C interface, SA1 and SA0 are set at a slave address.
These bits become "Don't care".

(*2): The register is set to the following value by the RESETB = "L" input or by the power-on POC.
F1="0", F0="0", D="0"

Data configuration

• Data configuration (Serial interface)

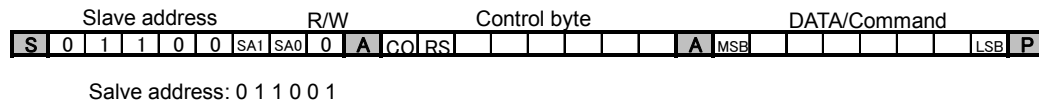


Note 1 : The commands F1 and F2 settings become valid when the least four bits of C4 to C7 are input.
(The bits from D1 to D80 and from C0 to C3 are not necessary.)

Note 2 : If the dummy bit is needed for the reason of number of transfer bits, put it on the first bit side.

Note 3 : The command execution follows the contents of the C7 to C0 registers immediately before the LOAD becomes "H".

- Data configuration (I²C interface)



CO: Consecutive control byte setting bit
 0: Last control byte, 1: Consecutive control byte
 RS: Command/data setting bit
 0: Command data, 1: Display data

For the I²C interface, each IC is assigned with a 7-bit slave address. The first one byte in the transfer consists of this 7-bit slave address and the R/W bit that indicates the data transfer direction. Always input "0" to the eighth R/W bit because the ML9488 is a write-only LSI.

The eight bits next to the slave address is a control byte. The first one bit is CO: consecutive command setting bit and the next one bit is RS: command/data setting bit (the remaining six bits are the Don't care bits).

When CO = "0": Means the last control byte.

When CO = "1": Means the control bytes are successively input.

When RS = "0": Means the data to be input next is the command data.

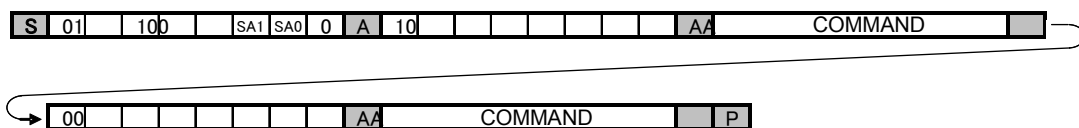
When RS = "1": Means the data to be input next is the display data.

The display data can be successively input.

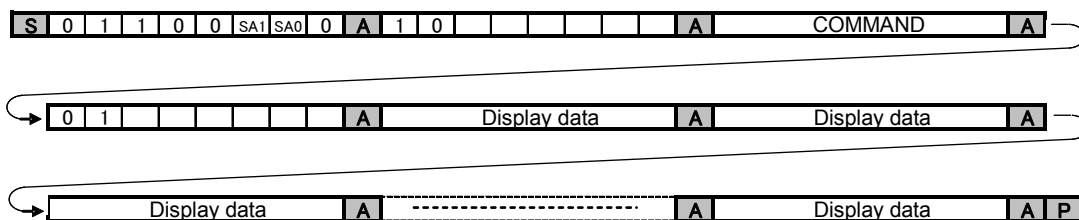
Example of Data Setting

- When inputting two commands

When inputting two commands



- When inputting the command and display data



Data write method

• Serial interface

The data is written to the address set by the data write setting command (F3).

For the Serial interface, the data is written in units of 80 bits.

Written from D80 to SEG1, D79 to SEG2, ... , D2 to SEG79, and D1 to SEG80.

	MSB Segm				ent output								LSB
	1234				32	33	34	35	36	37	38	39	40
COM1	D80	D79	D78	D77		D49	D48	D47	D46	D45	D44	D43	D42
COM2	D80	D79	D78	D77		D49	D48	D47	D46	D45	D44	D43	D42
COM3	D80	D79	D78	D77		D49	D48	D47	D46	D45	D44	D43	D42
COM4	D80	D79	D78	D77		D49	D48	D47	D46	D45	D44	D43	D42

	MSB Segm				ent output								LSB
	41	42	43	44	72	73	74	75	76	77	78	79	80
COM1	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2
COM2	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2
COM3	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2
COM4	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2

• I²C interface

The data is written to the address set by the slave address.

For the I²C interface, the data is written to the specified address starting with the LSB side in units of 8 bits.

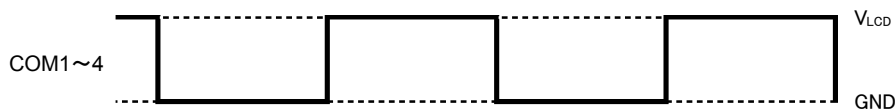
(The data is written in the order from SEG73-80, SEG65-SEG72, ... , SEG9-16, and SEG1-SEG8.)

	LSB Segm				ent output								MSB
	1	2	3	4	32	33	34	35	36	37	38	39	40
COM1	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7
COM2	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7
COM3	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7
COM4	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7

	LSB Segm				ent output								MSB
	41	42	43	44	72	73	74	75	76	77	78	79	80
COM1	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7
COM2	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7
COM3	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7
COM4	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7

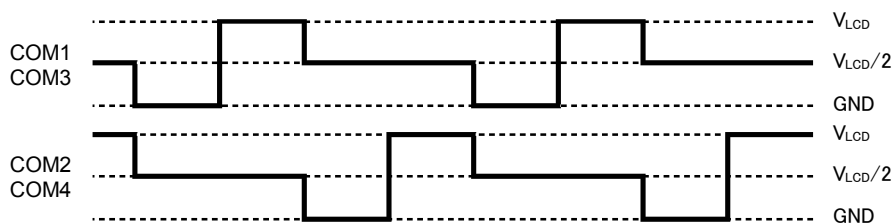
● Common waveforms

(1) At static

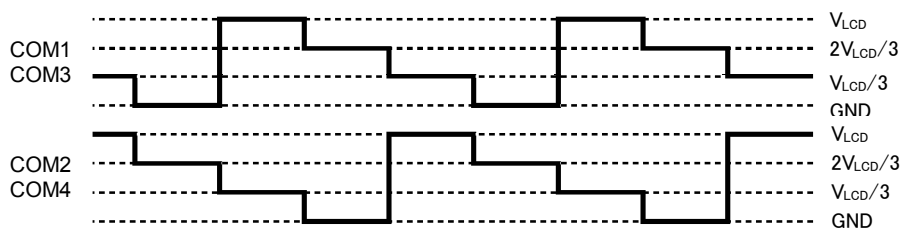


(2) At 1/2-duty

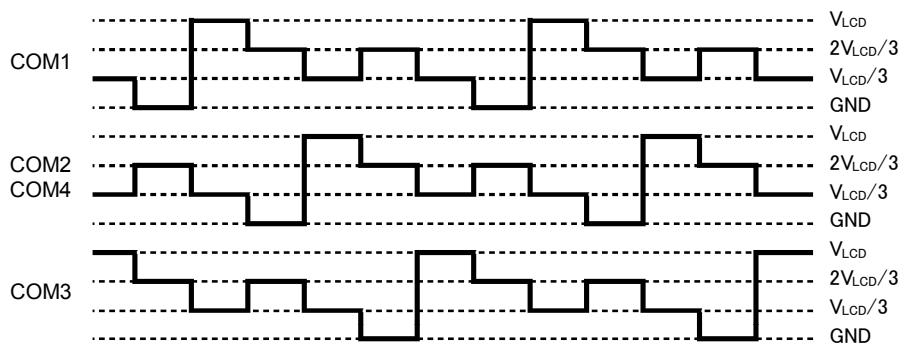
At 1/2-bias



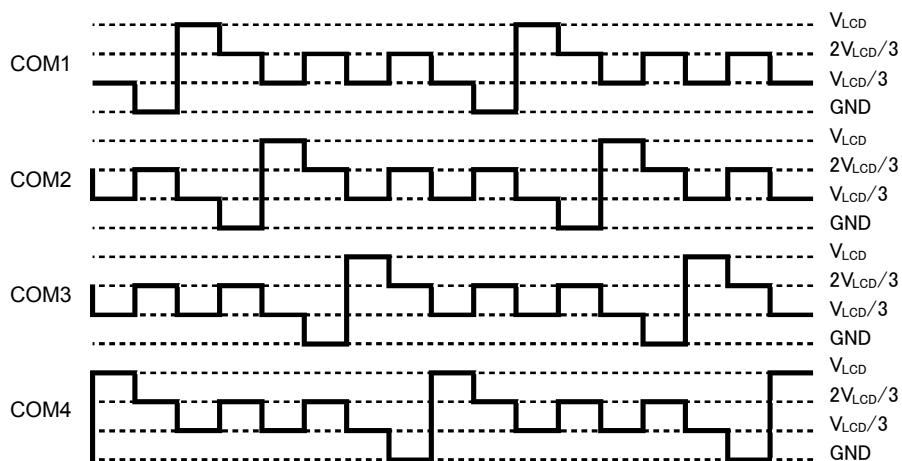
At 1/3-bias



(3) At 1/3-duty

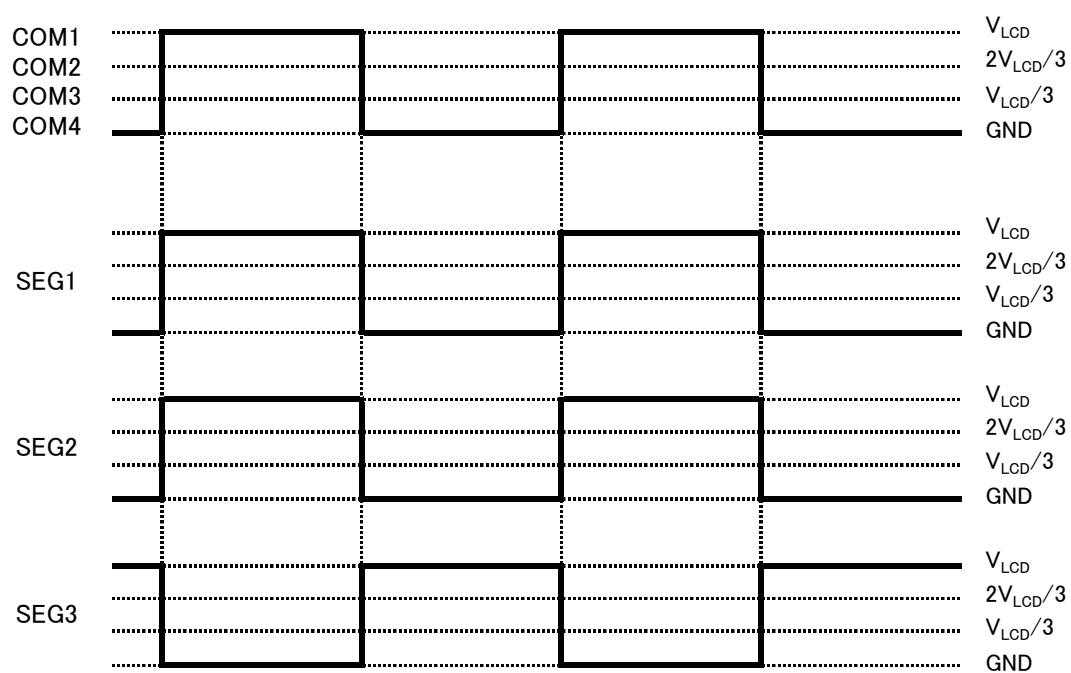
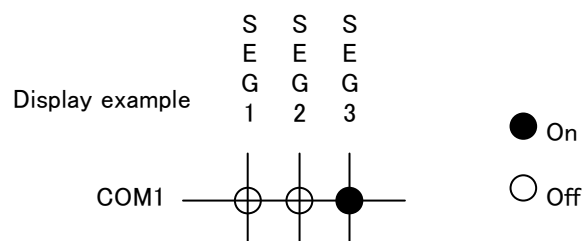


(4) At 1/4-duty



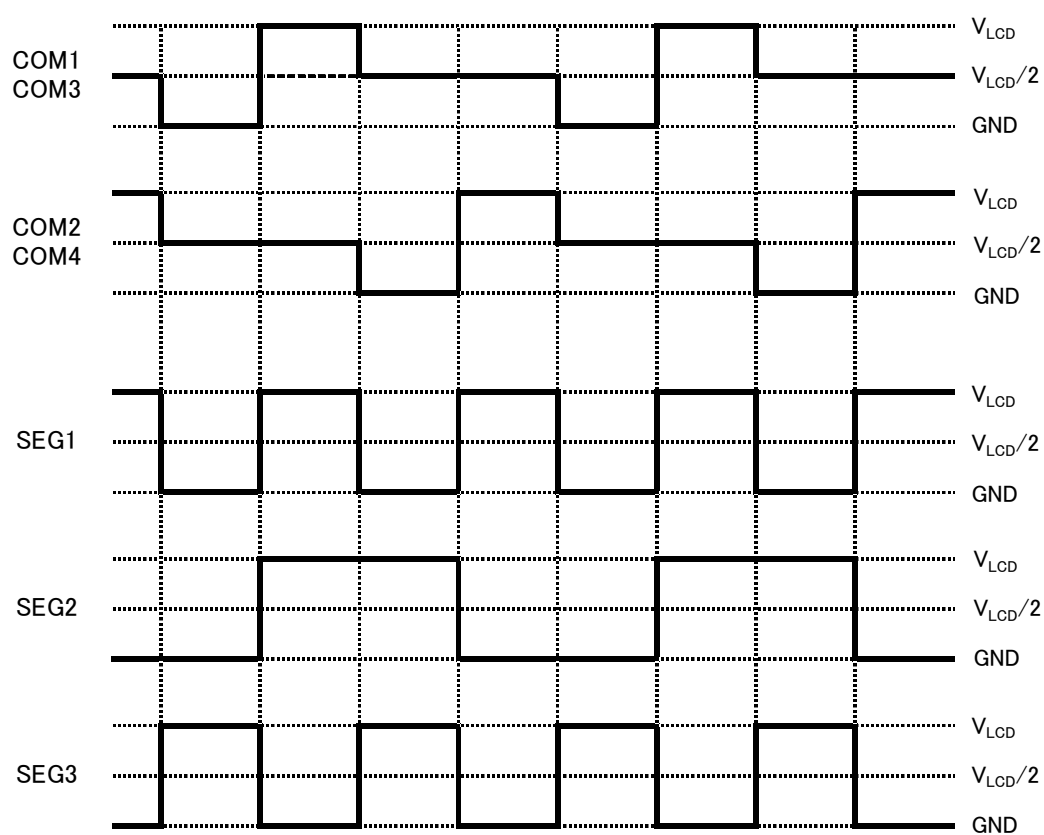
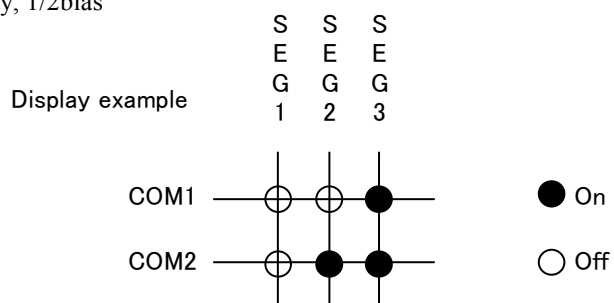
● Common segment output waveform

•At Static



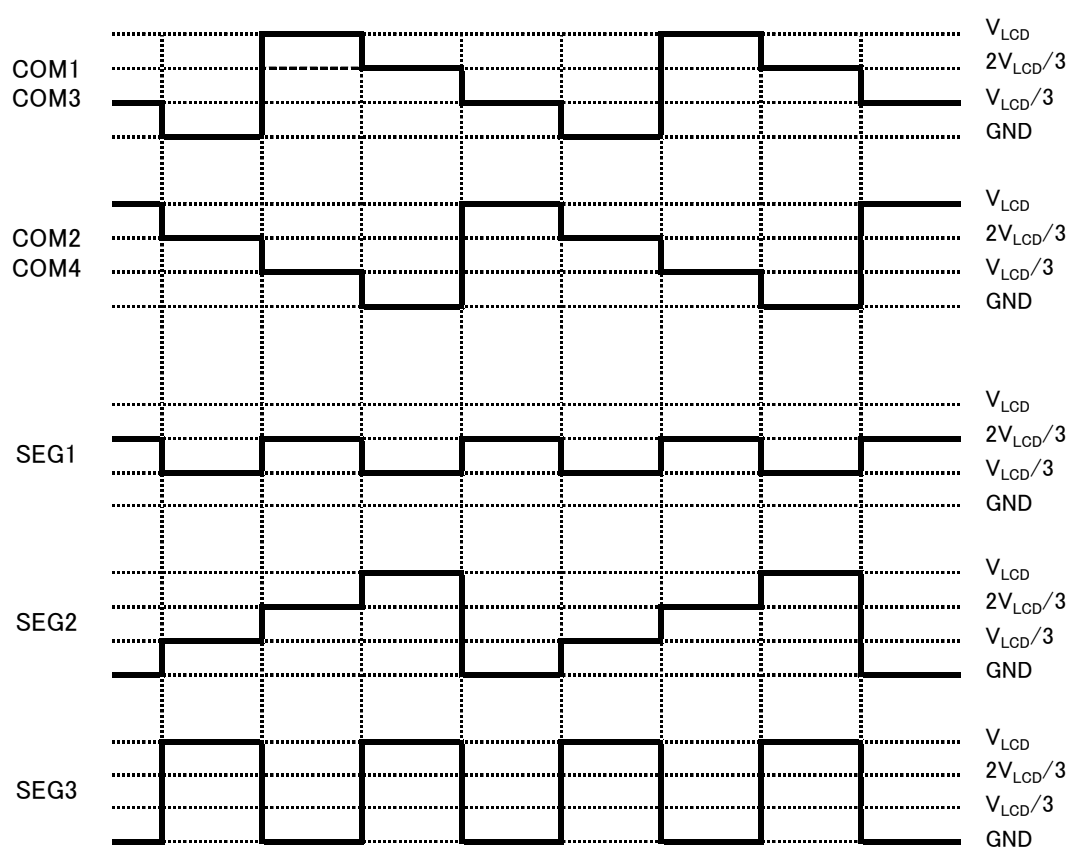
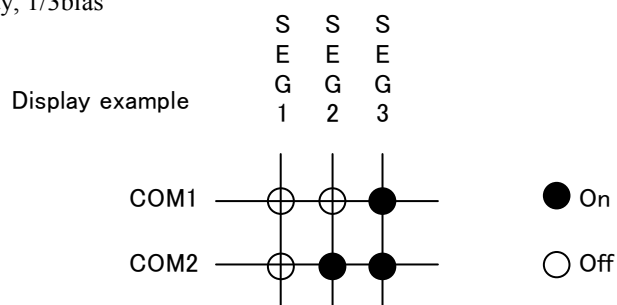
● Common and segment output waveforms

• At 1/2Duty, 1/2bias



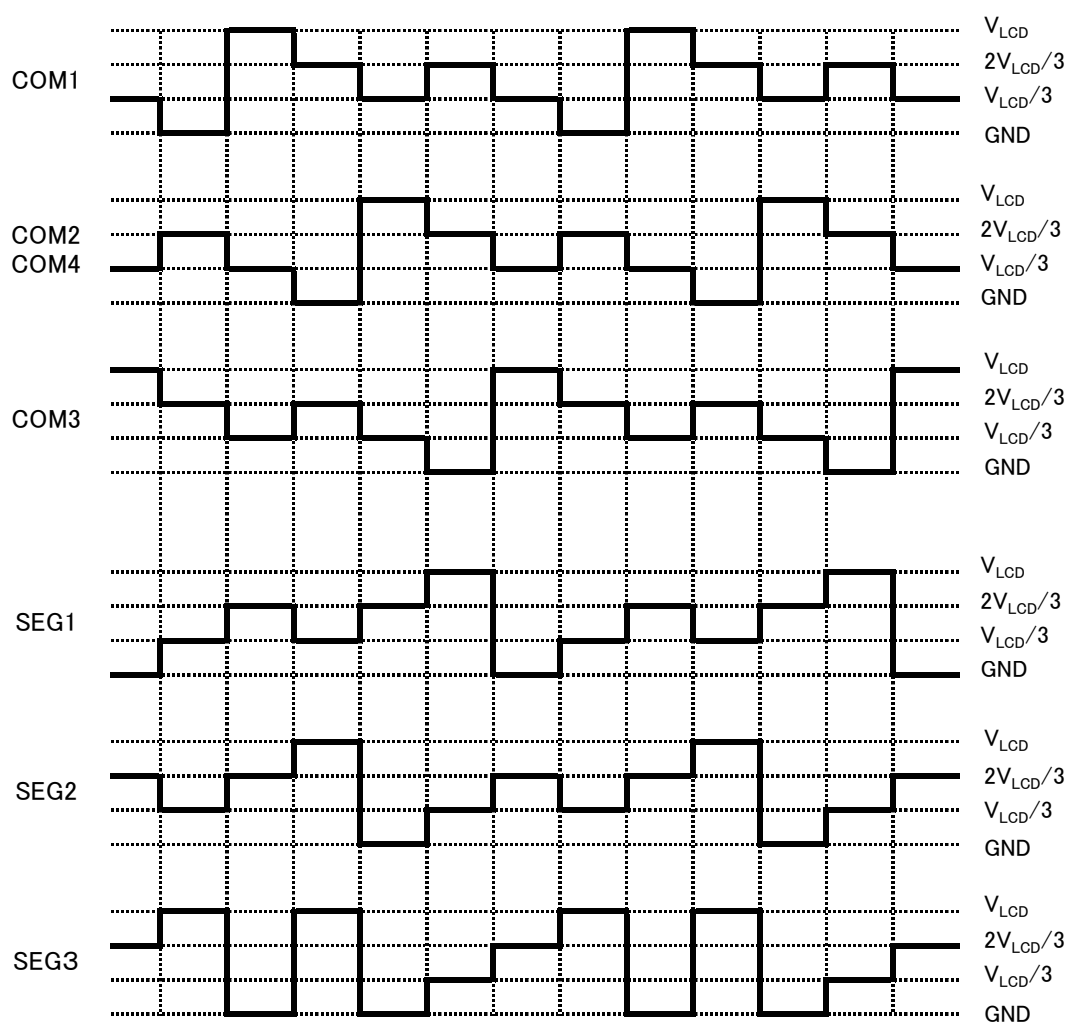
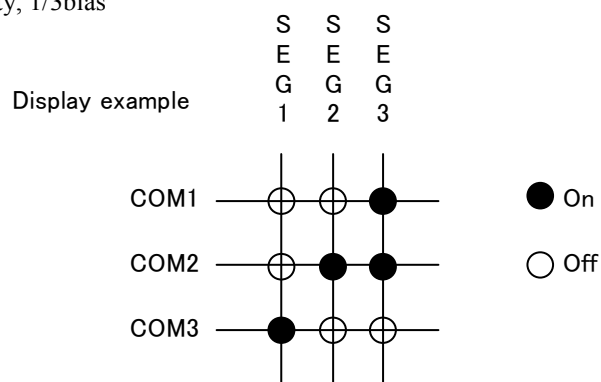
● Common and segment output waveforms

• At 1/2Duty, 1/3bias



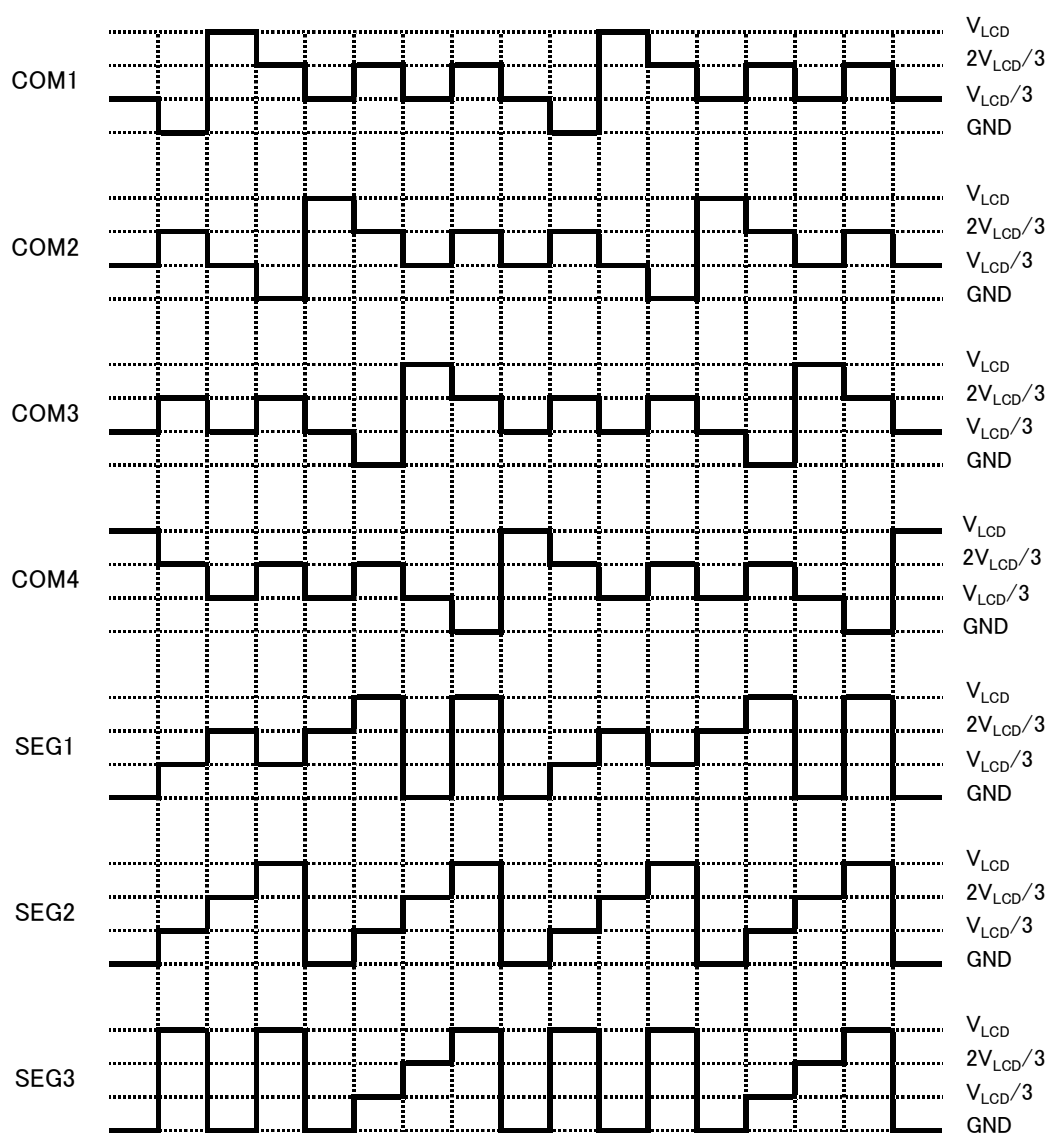
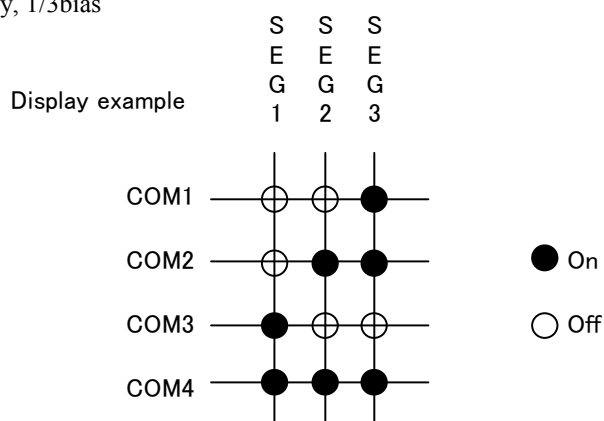
● Common and segment output waveforms

• At 1/3Duty, 1/3bias



● Common and segment output waveforms

• At 1/4Duty, 1/3bias



Cascade configuration 1

The common outputs of the slave chip output GND-level. So Com1 to Com4 set to open.

$C_p = 0.1$ [μF] (bypass capacitor between power supplies)



Cascade configuration 2

I²C interface

External R_f-based CR oscillator circuit used

1/4Duty

External RESETB signal input

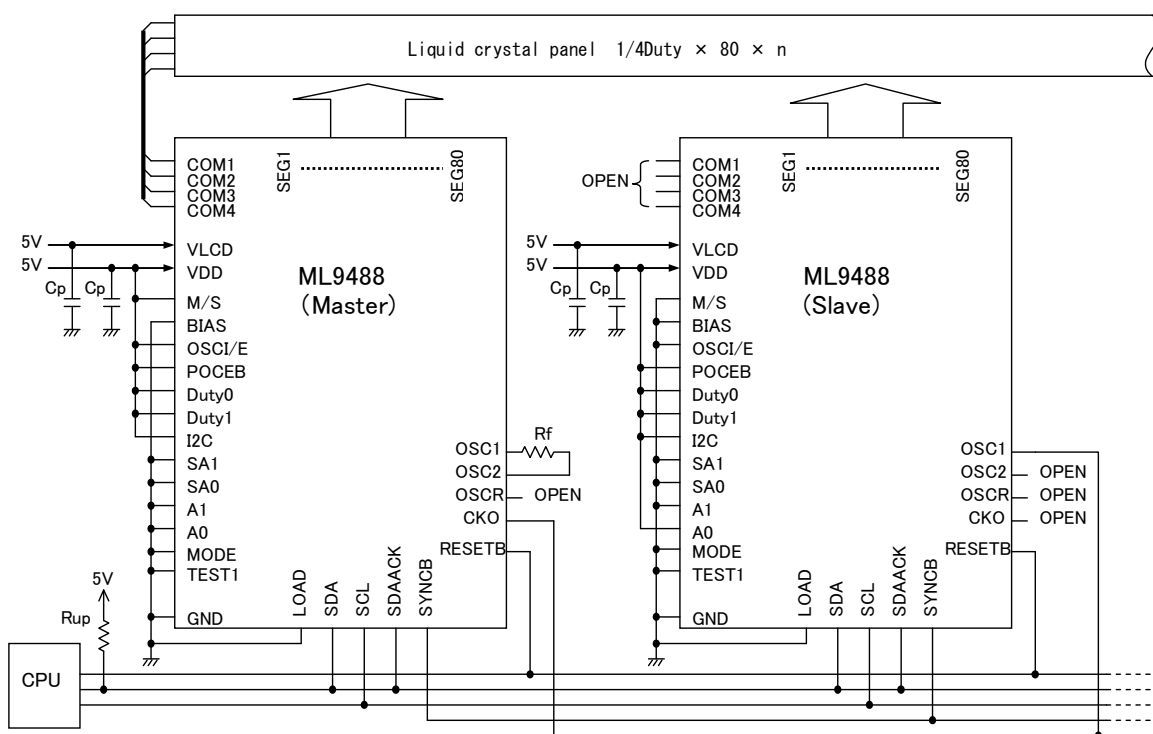
The common outputs of the slave chip output GND-level. So Com1 to Com4 set to open.

[External component]

C_p = 0.1 [μF] (bypass capacitor between power supplies),

R_f = 470 [kΩ] (external R, resistor for CR oscillator circuit),

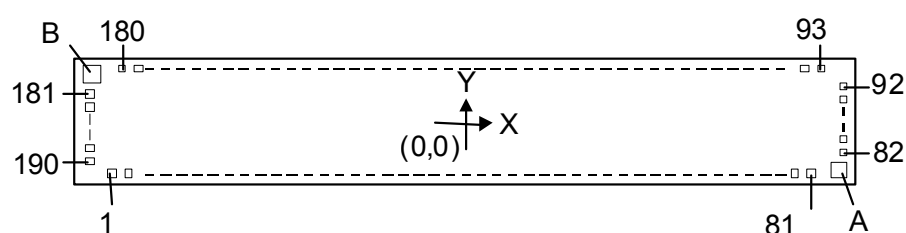
R_{up} = Resistor for SDA data bus pull-up



PAD CONFIGURATION

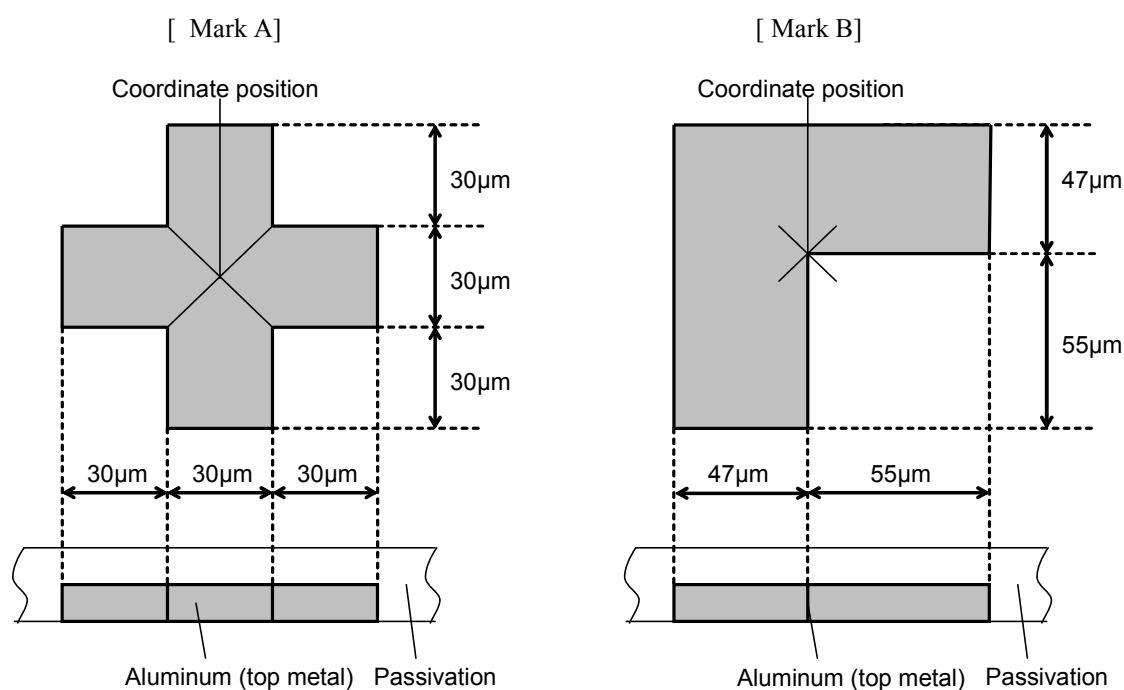
Pad layout (pattern face)

Chip size : 4.80 mm x 0.90 mm
 Chip thickness : $400\ \mu\text{m} \pm 20\ \mu\text{m}$
 Minimum bump pitch : $50\ \mu\text{m}$
 Bump height : $15\ \mu\text{m} \pm 3\ \mu\text{m}$



Bump and alignment mark dimensions (pattern face)

PAD No.1~81 : $32\ \mu\text{m} \times 80\ \mu\text{m}$
 PAD No.82~190 : $30\ \mu\text{m} \times 84\ \mu\text{m}$
 Alignment marks A and B : See below



Alignment mark	X-coordinate (μm)	Y-coordinate (μm)
Mark A	2289	-308
Mark B	-2289	309

Pad center coordinates

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
1	DUMMY -2206		-308	41	VLCD 27		-308
2	DUMMY -2149		-308	42	VLCD 81		-308
3	GNDO -2092		-308	43	VLCD 135		-308
4	Duty1 -2035		-308	44	RESETB 192		-308
5	Duty1 -1978		-308	45	RESETB 244		-308
6	Duty0 -1921		-308	46	OSC1 298		-308
7	Duty0 -1869		-308	47	OSC1 350		-308
8	A0 -1815		-308	48	OSC1 404		-308
9	A0 -1763		-308	49	OSC2 458		-308
10	A1 -1709		-308	50	OSC2 510		-308
11	A1 -1657		-308	51	OSC2 564		-308
12	SA0 -1603		-308	52	OSC2 618		-308
13	SA0 -1549		-308	53	OSCR 672		-308
14	SA1 -1492		-308	54	OSCR 724		-308
15	SA1 -1436		-308	55	OSCR 776		-308
16	VDDO -1379		-308	56	CKO 830		-308
17	SDAACK -1322		-308	57	CKO 882		-308
18	SDAACK -1265		-308	58	CKO 934		-308
19	SDAACK -1208		-308	59	CKO 986		-308
20	DATA(SDA) -1151		-308	60	SYNCB 1040		-308
21	DATA(SDA) -1094		-308	61	SYNCB 1092		-308
22	CLOCK(SCL) -1037		-308	62	SYNCB 1144		-308
23	CLOCK(SCL) -980		-308	63	SYNCB 1196		-308
24	LOAD -923		-308	64	VDDO 1250		-308
25	LOAD -866		-308	65	I2C 1304		-308
26	GND -809		-308	66	I2C 1356		-308
27	GND -752		-308	67	M/S 1413		-308
28	GND -695		-308	68	M/S 1465		-308
29	GND -638		-308	69	POCEB 1522		-308
30	GND -581		-308	70	POCEB 1574		-308
31	GND -524		-308	71	OSCI/E 1628		-308
32	VDD -467		-308	72	OSCI/E 1680		-308
33	VDD -412		-308	73	BIAS 1737		-308
34	VDD -357		-308	74	BIAS 1789		-308
35	VDD -302		-308	75	TEST2 1846		-308
36	VDD -247		-308	76	TEST2 1900		-308
37	VDD -192		-308	77	TEST1 1957		-308
38	VLCD -135		-308	78	TEST1 2014		-308
39	VLCD -81		-308	79	GNDO 2071		-308
40	VLCD -27		-308	80	DUMMY 2128		-308

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
81	DUMMY 2185		-308	125	SEG31 585		309
82	DUMMY 2289		-232	126	SEG32 535		309
83	DUMMY 2289		-182	127	SEG33 485		309
84	DUMMY 2289		-132	128	SEG34 435		309
85	COM1 2289		-82	129	SEG35 385		309
86	COM2 2289		-32	130	SEG36 335		309
87	COM3 2289		18	131	SEG37 285		309
88	COM4 2289		68	132	SEG38 235		309
89	DUMMY 2289		118	133	SEG39 185		309
90	DUMMY 2289		168	134	SEG40 135		309
91	DUMMY 2289		218	135	COM1 85		309
92	DUMMY 2289		268	136	COM2 35		309
93	DUMMY 2185		309	137	COM3 -15		309
94	DUMMY 2135		309	138	COM4 -65		309
95	SEG1 2085		309	139	SEG41 -115		309
96	SEG2 2035		309	140	SEG42 -165		309
97	SEG3 1985		309	141	SEG43 -215		309
98	SEG4 1935		309	142	SEG44 -265		309
99	SEG5 1885		309	143	SEG45 -315		309
100	SEG6 1835		309	144	SEG46 -365		309
101	SEG7 1785		309	145	SEG47 -415		309
102	SEG8 1735		309	146	SEG48 -465		309
103	SEG9 1685		309	147	SEG49 -515		309
104	SEG10 1635		309	148	SEG50 -565		309
105	SEG11 1585		309	149	SEG51 -615		309
106	SEG12 1535		309	150	SEG52 -665		309
107	SEG13 1485		309	151	SEG53 -715		309
108	SEG14 1435		309	152	SEG54 -765		309
109	SEG15 1385		309	153	SEG55 -815		309
110	SEG16 1335		309	154	SEG56 -865		309
111	SEG17 1285		309	155	SEG57 -915		309
112	SEG18 1235		309	156	SEG58 -965		309
113	SEG19 1185		309	157	SEG59 -1015		309
114	SEG20 1135		309	158	SEG60 -1065		309
115	SEG21 1085		309	159	SEG61 -1115		309
116	SEG22 1035		309	160	SEG62 -1165		309
117	SEG23 985		309	161	SEG63 -1215		309
118	SEG24 935		309	162	SEG64 -1265		309
119	SEG25 885		309	163	SEG65 -1315		309
120	SEG26 835		309	164	SEG66 -1365		309
121	SEG27 785		309	165	SEG67 -1415		309
122	SEG28 735		309	166	SEG68 -1465		309
123	SEG29 685		309	167	SEG69 -1515		309
124	SEG30 635		309	168	SEG70 -1565		309

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REVISION HISTORY

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEDL9488-01	Jan .15, 2013	–	–	Final edition 1 issued

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