MLC510PA

8-bit micro-controller with 160 dots LCD driver

Features

- Single chip 8-bit micro-controller
- Operating voltage: 2.2V to 5.5V
- Memory :
  - Program ROM : 8K Bytes
  - Data RAM : 128 Bytes
  - LCD display RAM : 20 Bytes
- 18 input/output pins:
  - Dedicated I/O pins: P0[0:3] ,P2[0:1]
  - Shared input or output pins:
    - P0[4:5]/TMin
    - P1[0:1]/IR
    - P3[0:7]/Segment
- LCD driver output:
  - Max 32 segment × 5 common
  - 1/4 or 1/5 duty 1/3 bias driving mode
- Two re-loadable 8-bit timers
- Build-in Watch-Dog timer
- Build-in dual oscillation circuit:
  - Single or dual clock operation is selected by code option
  - RC type main oscillator
  - Crystal type sub-oscillator
  - Oscillator up to 4MHz @ 2.4V and 6MHz @ 3.6V

Application Field

Timepiece, sport meter

2007/10 version A1

MEGAWIN

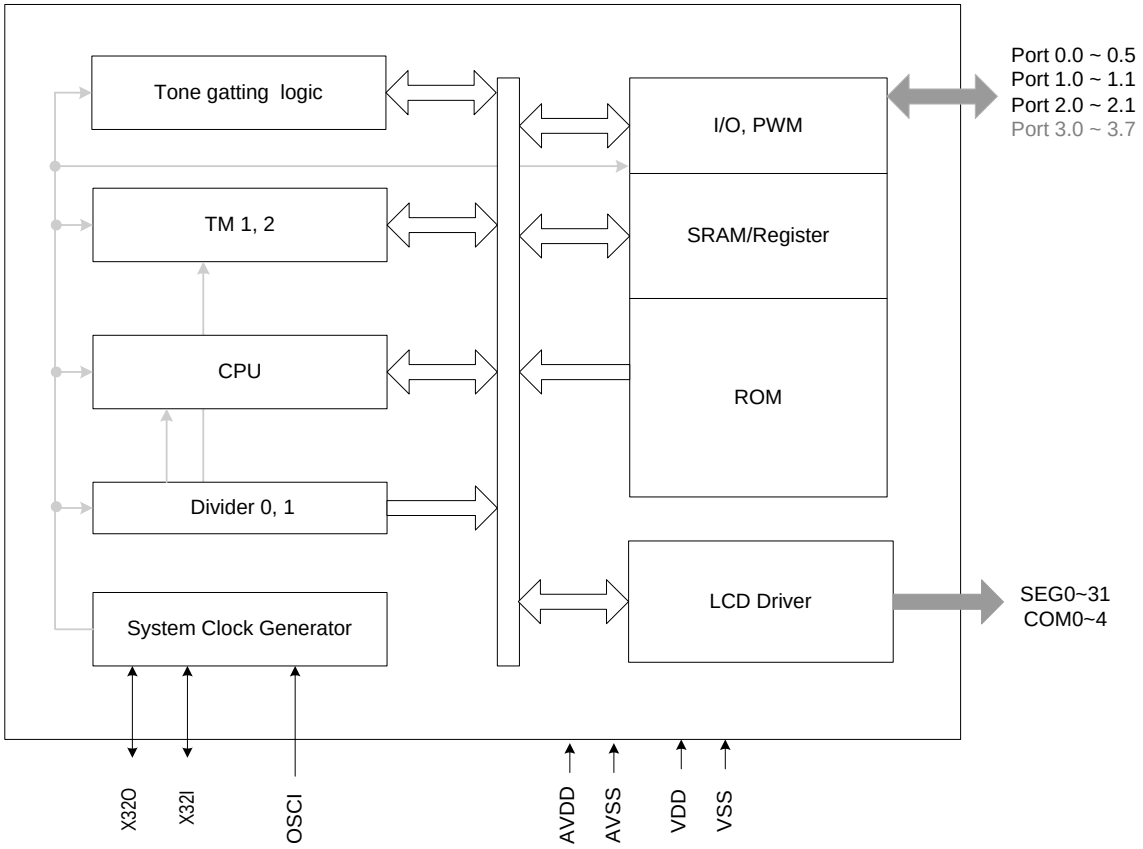
General Description

MLC510PA is a low-cost, high-performance 8-bit micro-controller of MEGAWIN, which integrates an 8-bit RISC CPU core, ROM, RAM, timers, LCD driver, I/O ports, radio frequency counter and system control circuits. The ROM can store data table and program. The MLC510PA provides two build-in oscillators, which allows the chip to operate in dual-clock or single-clock operation mode. User can arrange the clock mode to minimize the power consumption. The MLC510PA is suitable for timepiece, sport meter, toy controllers, and other products.

Pad Description (61 pads)

Pad No.	Pad Name	I/O	Description
P37 ~P6	SEG0 ~ SEG31	O	LCD segment signal output pins. SEG24~SEG31 share pads with P3[7:0].
P38 ~P42	COM0 ~ COM4	O	LCD common signals output pins.
P43 ~P48	P0.0 ~ P0.5	I/O	Programmable I/O ports with interrupt function. Port0.4, 0.5 can be the input of timers.
P49,P50	P1.0 ~ P1.1	I/O	Programmable I/O ports. Port P1.0, 1.1 can be output with IR carrier.
P57,P59	P2.0 ~ P2.1	I/O	Programmable input or output port.
P53 ~P51	SCLK SDA CMD_B	I/O	OTP interface pins
P1	OSCI	I	RC oscillator input pin.
P2,P3	X32O, X32I	O/I	32.768KHz crystal oscillator pins.
P58,P60	VSS, AVSS	P	Ground pins
P56,P55	AVDD, VDD	P	Positive power pins
P61	/RESB	I	System reset pin (low active)
P4,P5	V1, V2	I	LCD voltage external input pins.
P54	VPP	I	High voltage pin for OTP programming

Block Diagram



Function Description

Registers

	A
	Y
	X
	P
PCH	PCL
1	S

Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words that are used in these operations.

Index Register (X, Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

Processor Status Register (P)

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled by both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive

V: Overflow flag, 1 = true, 0 = false

B: BRK interrupt command, 1 = BRK, 0 = IRQB

D: Decimal mode, 1 = true, 0 = false

I: IRQB disable flag, 1 = disable, 0 = enable

Z: Zero flag, 1 = true, 0 = false

C: Carry flag, 1 = true, 0 = false

Program Counter (PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time when an instruction or data is fetched from program memory.

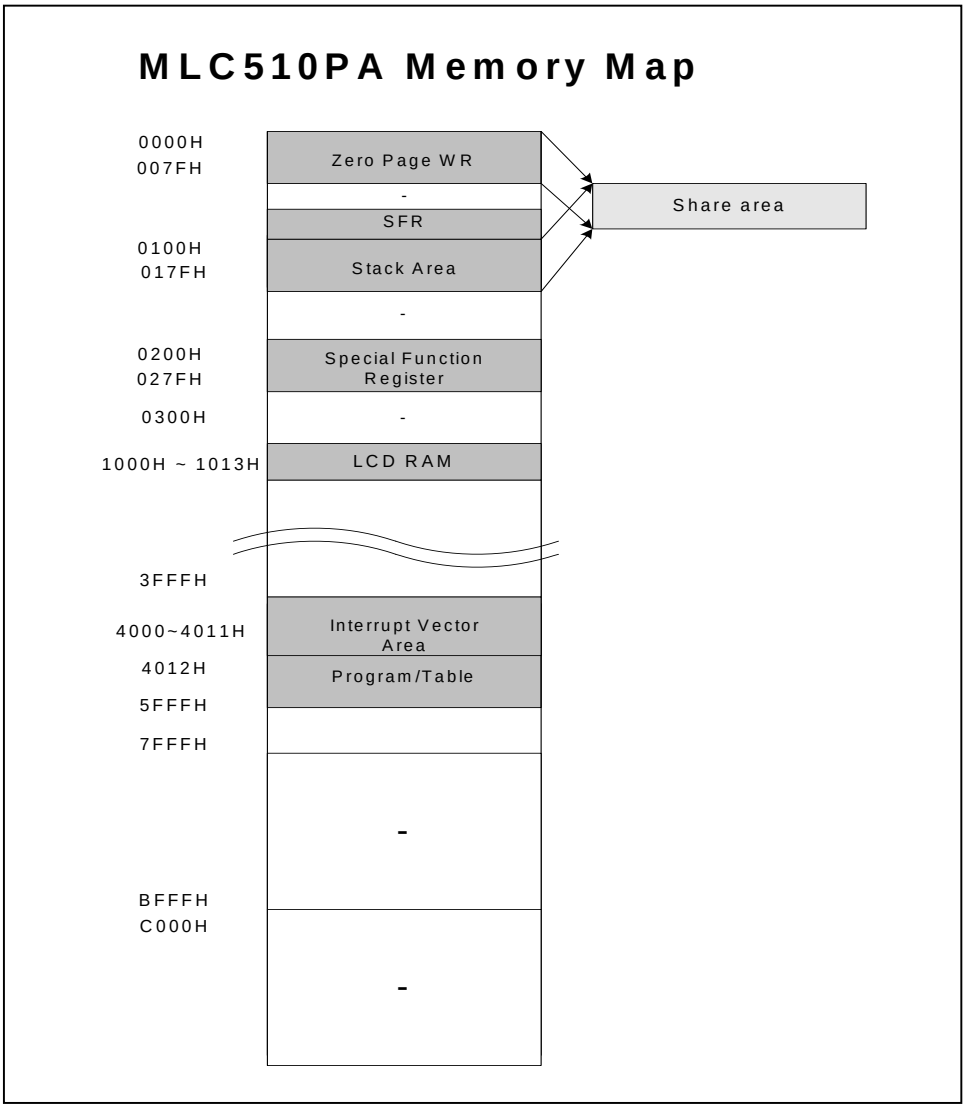
Stack Pointer (S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's software.

Memory Map

There are 128 bytes SRAM in MLC510PA. They are located at both 0000H to 007FH and 0100H to 017FH regions. The address 0000H to 007FH and 0100H to 017FH share the same RAM block. The address 00C0H to 00FFH and 0200H to 027FH are special function register area. For LCD function, there are 20 bytes LCD RAM (1000H to 1013H) in MLC510PA. They can also be used as a general purpose RAM when LCD function is unused.

There are 8K bytes program/data ROM in MLC510PA. The ROM address ranges from 4000H to 5FFFH. It can store program and data. The address mapping of MLC510PA is shown below.



Special Function Register (SFR)

The address 00C0H to 00FFH and 0200H to 027FH are reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

SFR (special function register): 00C0H ~ 00FFH (page 0 area)

Address	Content	Default	Address	Content	Default
00C0		X	00D0		X
00C1		X	00D1		X
00C2	IRQ_EN / IRQ_ST	00	00D2		X
00C3	IRQ_CLR	00	00D3		X
00C4		00	00D4		X
00C5		00	00D5	P1_MFR	00
00C6		00	00D6	P2_MFR	00
00C7		00	00D7	P3_MFR	X
00C8	TM1L	00	00D8	P0	00
00C9		00	00D9	P1	00
00CA	TM1_CTL	00	00DA	P2	00
00CB		X	00DB	P3	X
00CC	DIV1_ICLR	00	00DC		X
00CD	DIV1_IST/ DIV1_IEN	00	00DD		X
00CE	SCK_SEL	00	00DE	WDT_CTL	00
00CF	DIV1_H	00	00DF		X

Address	Content	Default	Address	Content	Default
00E0		00	00F0		0F
00E1		00	00F1		X
00E2		X	00F2		00
00E3		00	00F3		X
00E4		X	00F4		X
00E5		00	00F5		X
00E6		X	00F6		X
00E7		X	00F7		X
00E8	TM2_L	00	00F8		X
00E9	TM2_H	00	00F9		X
00EA	TM2_CTL	00	00FA		00
00EB		X	00FB		X
00EC		X	00FC		X
00ED		X	00FD		00
00EE		X	00FE		X
00EF		X	00FF		X

SFR (special function register): 0200H ~ 027FH

Address	Content	Default	Address	Content	Default
0200	PWR_CR	00	0210		X
0201		X	0211		X
0202	RLH_EN	00	0212		X
0203		X	0213		X
0204		X	0214		X
0205		X	0215		X
0206		X	0216		X
0207		X	0217		X
0208		X	0218		X
0209		X	0219		X
020A		X	021A		X
020B		X	021B		X
020C		X	021C		X
020D		X	021D		X
020E		X	021E		X
020F		X	021F		X

Address	Content	Default	Address	Content	Default
0220		X	0230		X
0221		X	0231		X
0222		X	0232		X
0223		X	0233		X
0224		X	0234		X
0225		X	0235		X
0226		X	0236		X
0227		X	0237		X
0228		X	0238		X
0229		X	0239		X
022A		X	023A		X
022B		X	023B		X
022C		X	023C		X
022D		X	023D		X
022E		X	023E		X
022F		X	023F		X

Special Function Register, Continued

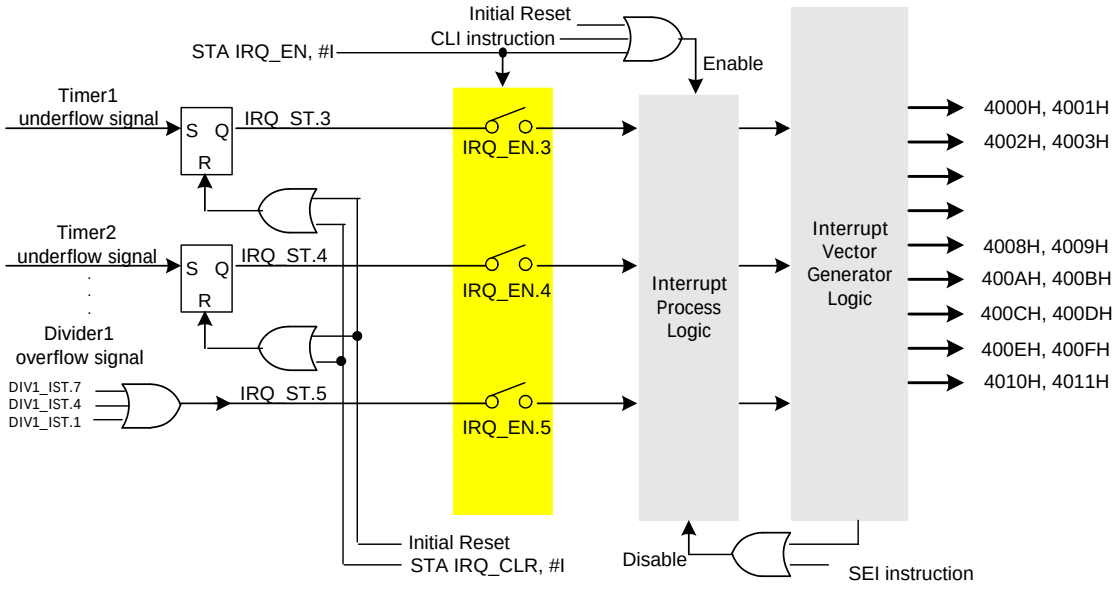
Address	Content	Default	Address	Content	Default
0240	P0DIR	00	0250	LCD_CR	00
0241	P0CFG	00	0251		00
0242			0252	STB_CTL	00
0243			0253	STB_COM	00
0244	P1DIR	00	0254	P01_LTH	00
0245	P1CFG	00	0255		X
0246		X	0256		X
0247		X	0257		X
0248	P2DIR	00	0258		X
0249	P2CFG	00	0259		X
024A		X	025A		X
024B		X	025B		X
024C	P3DIR	X	025C		X
024D		X	025D		X
024E		X	025E		X
024F		X	025F		X

Address	Content	Default	Address	Content	Default
0260		X	0270		X
0261		X	0271		X
0262		X	0272		X
0263		X	0273		X
0264		X	0274		X
0265		X	0275		X
0266		X	0276		X
0267		X	0277		X
0268		X	0278		X
0269		X	0279		X
026A		X	027A		X
026B		X	027B		X
026C		X	027C		X
026D		X	027D		X
026E		X	027E		X
026F		X	027F		X

Interrupt Vectors

Vector Address	Item	Priority	Properties	Memo
4000H, 4001H	BRK	2	Int.	Software BRK interrupt vector (internal used)
4002H, 4003H	RESET	1	Ext.	Initial reset
4004H, 4005H				
4006H, 4007H				
4008H, 4009H	KEY	3	Int.	Key strobe interrupt
400AH, 400BH	P0	4	Ext.	Port P0 interrupt vector
400CH, 400DH	TM1	5	Int.	Timer 1 overflow interrupt
400EH, 400FH	TM2	6	Int.	Timer 2 overflow interrupt
4010H, 4011H	DIV1x	7	Int.	Selectable divider 1 carry out interrupt

There are five kinds of interrupt sources are provided in MLC510PA. The flag IRQ_EN and IRQ_ST are used to control the interrupts. When flag IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, #I instruction is invoked. Executing the SEI instruction can also disable the interrupts.



Interrupt Registers

IRQ enable flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_EN	-	-	DIV1x	TM2	TM1	P0	KEY	-	-	√

Program can enable or disable the ability of triggering IRQ through this register.

0: Disable (default “0” at initialization)

1: Enable

KEY: Key strobe occurs at COM scan mode

P0: Falling or Rising edge occurs at port 0.0 or P0.4 input

TM1, TM2: Timer 1 / Timer 2 underflow

DIV1x: Divider 1 selected interrupt frequency occurred

IRQ status flag (same address with IRQ_EN)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C2H	IRQ_ST	-	-	DIV1x	TM2	TM1	P0	KEY	-	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ. The hardware would not clear the bits of IRQ_ST register automatically. If the interrupt triggering is enabled and the interrupt event is accepted, the correspond IRQ status flag should be cleared by firmware writing ‘1’ to the corresponding bit of IRQ_CLR register.

The controlling mechanism of DIV1x interrupt is slightly different from the other interrupt sources. The DIV1x interrupt status is the OR-gated output of DIV1_IST bits. When the DIV1x interrupt occurs, program must clear the DIV1x bit of IRQ_ST register and all DIV1_IST bits to enable the next DIV1x interrupt event. For the detailed description of DIV1_IST register, please refer to the **DIV1 interrupt selector** section.

IRQ clear flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	IRQ_CLR	-	-	DIV1x	TM2	TM1	P0	KEY	-	-	√

Program can clear the interrupt event in the IRQ_ST register by writing ‘1’ into the corresponding bit of the IRQ_CLR.

System Control Registers

System clock selector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CEH	SCK_SEL	CKS7	-	-	-	-	-	-	CKS0	-	√

CKS0: F_{CPU} clock source select. 0:F_{X32}, 1: F_{OSC}

CKS7: select the input clock source of divider 1. 0: F_{X32}, 1: F_{OSC}

DIV1 interrupt selector (The frequency of DIV1_H clock source is F_{DIV1_IN}/256)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CFH	DIV1_H	F_{DIV1_IN} /65536	F_{DIV1_IN} /32768	F_{DIV1_IN} /16384	F_{DIV1_IN} /8192	F_{DIV1_IN} /4096	F_{DIV1_IN} /2048	F_{DIV1_IN} /1024	F_{DIV1_IN} /512	√	-

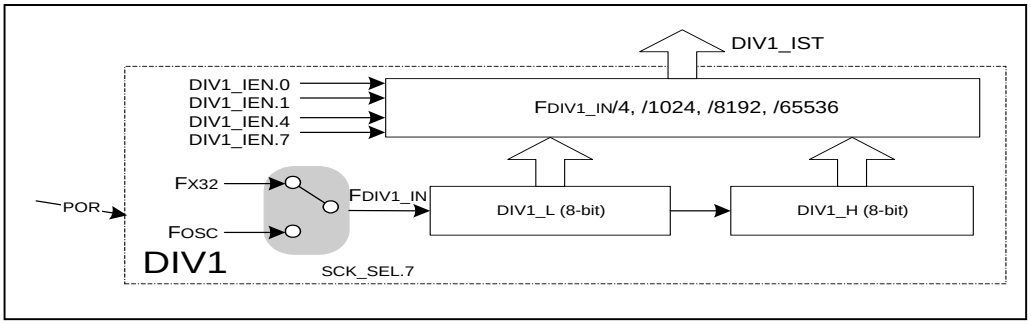
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
-	-	F_{DIV1_IN} /65536	-	-	F_{DIV1_IN} /8192	-	-	F_{DIV1_IN} /1024	F_{DIV1_IN} /4	-	-
00CDH	DIV1_IEN	IEN7	-	-	IEN4	-	-	IEN1	IEN0	-	√
00CDH	DIV1_IST	IST7	-	-	IST 4	-	-	IST 1	IST0	√	-
00CCH	DIV1_ICLR	CLI7	-	-	CLI 4	-	-	CLI 1	CLI0	-	√

Program can enable or disable the ability of triggering DIV1x interrupt through DIV1_IEN register, and read the DIV1_IST to know which source trigging the DIV1x interrupt. The DIV1_L/H and DIV1_IST can be reset to 00H by POR, reset and waken from STOP mode. Program can clear the DIV1 interrupt event by writing '1' into the corresponding bit of DIV1_ICLR. The clock source of DIV1 can be selected by setting the bit 7 of SCK_SEL register.

Please note that the bits of DIV1_IST register are independent. When DIV1_EN register enable, there is only one individual trigging source be set. User can read the DIV1_IST know which source trigging the DIV1x interrupt, program must clear the CLIx bit of DIV1_ICLR register to enable the next DIV1x interrupt event.

DIV1_IST	DIV1 interrupt occurs status
IST 0 = 1	F_{DIV1_IN} / 4
IST 1 = 1	F_{DIV1_IN} / 1024
IST 4 = 1	F_{DIV1_IN} / 8192
IST 7 = 1	F_{DIV1_IN} / 65536

DIV1_IEN	Selected DIV1 interrupt enable source
IEN 0 = 1	F_{DIV1_IN} / 4
IEN 1 = 1	F_{DIV1_IN} / 1024
IEN 4 = 1	F_{DIV1_IN} / 8192
IEN 7 = 1	F_{DIV1_IN} / 65536



Power saving control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
0200H	PWR_CR	-	-	-	-	-	CKC1	CKC0	HALT	-	√

CKC1	CKC0	System clock control
0	0	F_{OSC} enable, F_{X32} enable (Dual mode)
0	1	F_{OSC} enable, F_{X32} disable (Single mode)
1	0	F_{OSC} disable, F_{X32} enable (Slow mode)
1	1	F_{OSC} disable, F_{X32} disable (Stop mode)

Note: PWR_CR.CKC0 is inhibited when single clock mode is selected by code option.

HALT: F_{CPU} off-line control bit. 1: F_{CPU} off-line, 0: F_{CPU} on-line

Program can switch the normal operation mode to the power-saving mode for saving power consumption through this register. There are three power saving modes in this system.

Slow mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 0)*

The main uC clock (F_{OSC}) stops oscillating. Only very low power is needed for uC to keep running.

Stop mode: *(PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 1)*

Both system clocks stop oscillating. The uC can be awakened from stop mode by 3-ways: port 0 interrupt (IRQ_EN.2=1 and IRQ_ST.2=1), hardware reset, or power-on reset. When the stop mode is released, only the oscillator, which is providing the uC clock, will be enabled again.

For the applications using KEY-STROBE function, the P0.0 and/or P0.4 is set to KEY-STROBE function instead of normal I/O port. Therefore, the IC cannot be waken up by the port 0. Please follow the procedures below to solve this problem:

1. Before entering STOP mode, set port 0.0 and/or port 0.4 to normal port function.
2. Enable P0 interrupt by setting IRQ_EN [2]
3. Disable LCD function.

4. Enter STOP mode. Thereby, the IC can be waken up by the status change of P0.0 or P0.4.
5. After the STOP mode is released, enable LCD function again.
6. Disable P0 interrupt by clearing IRQ_EN [2]
7. Set P0.0 and/or P0.4 to KEY-STROBE function again.

Halt mode: *(PWR_CR.HALT = 1)*

The F_{CPU} clock in off-line status. The oscillator(s) still oscillating if the PWR_CR.CKC1, PWR_CR.CKC0 keep low. The uC can be awakened from halt mode by 3-ways: the interrupt events which RLH_EN bits are set, hardware reset, or power-on reset.

Release halt mode enables flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
0202H	RLH_EN	-	-	DIV1x	TM2	TM1	P0	KEY	-	-	√

The register that controls the sources, shown as above table, could release the MLC510PA from halt mode. Program can read the IRQ_ST register to know which source release halt mode, and clear the halt release event by writing '1' into the corresponding bit of IRQ_CLR register.

Watchdog Timer (WDT)

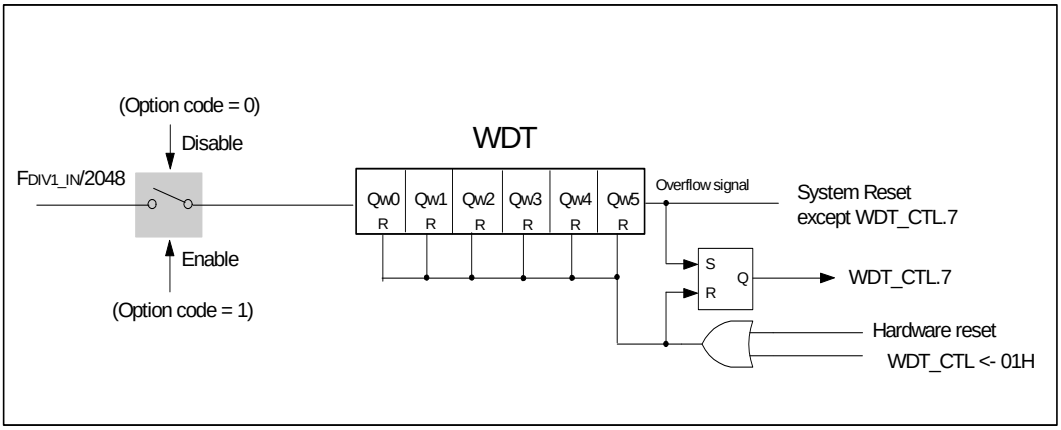
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DEH	WDT_CTL	RSTS	-	-	-	-	-	-	CLR	√	√

RSTS: WDT reset status, set by hardware when WDT overflows, clear by hardware reset or set WDT_CTL.0 to one to clear this bit (this bit is read only)

CLR: RSTS clear control bit, program can clear RSTS by program "1" into this bit (this bit is write only)

The watchdog timer (WDT) is composed of a 6-bit counter. It is designed to prevent the program from unknown errors. The WDT is enabled by code option. If the WDT overflows, the WDT reset function will be performed, and the uC would execute the program from the reset address. The watchdog-timer-control register (WDT_CTL) controls the WDT reset function. When the WDT overflows, RSTS bit (WDT_CTL.7) would be set by hardware. The RSTS bit would be cleared when firmware writes "1" to the bit 0 of WDT_CTL register or hardware reset occurs. The WDT overflow event would cause a 'hot reset' process. The behavior of the 'hot reset' is same as that of hardware reset except that the WDT_CTL.7 would be set to 1. Writing "1" to the bit 0 of WDT_CTL register could reset the contents of the WDT. In normal operation, the application program must reset WDT before it overflows.

The organization of the watchdog timer is shown as below.



Timers/Counters

Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C8H	TM1	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00CAH	TM1_CTL	STC	RL/S	TKES	-	-	-	TKI1	TKI0	-	√

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM1 input frequency
1	0	F_{X32}
1	1	P0.4

Timer 1 is an 8-bit down-count counter. The counter underflow frequency of timer 1 can be calculated with the equation:

$$F_{TM1\_UV} = F_{TM1} / (TM1+1)$$

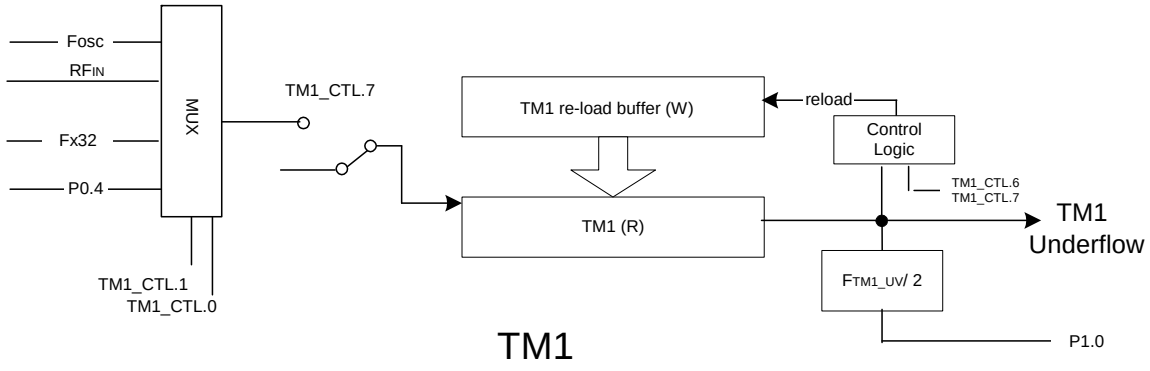
For example: (if F_{TM1} = 2.048MHz)

TM1	Frequency
00H	Invalid
01H	1.024MHz
02H	683KHz
…	…
FFH	8KHz

The timer 1 also can be used as tone generator. It generates specific frequency of tone with square wave, but the frequency of specific tone is half of the overflow frequency. The example frequency table is shown as below:

Set TM1_CTL to be 82H (enable counting and auto reload, source clock = Fx32)

TM1	Clock Source	Tone frequency	Relative scale of tone
7CH	32768	131.072	C3 (130.81)
75H	32768	138.847	C#3 (138.59)
6FH	32768	146.28	D3 (146.83)
…	…	…	…
20H	32768	496.484	B4 (493.88)
1EH	32768	528.516	C5 (523.25)



TM1

Timer2

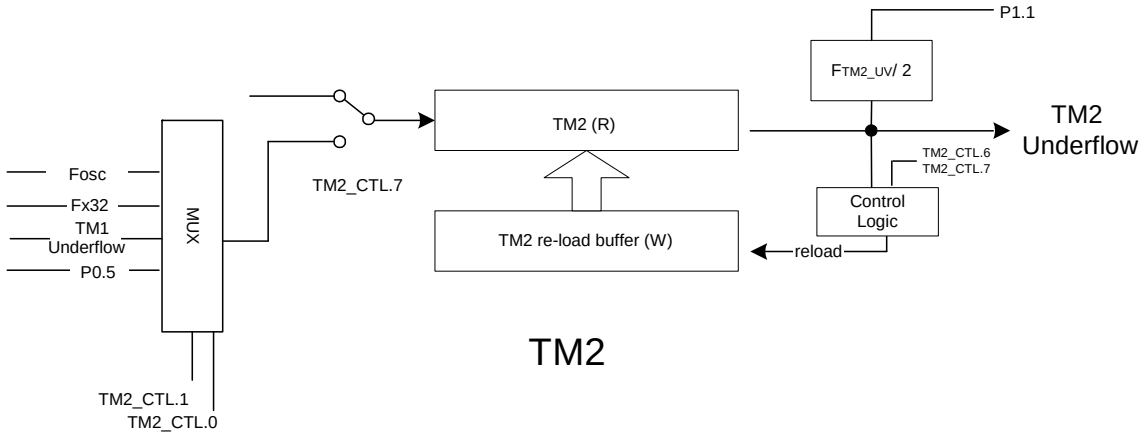
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	TM2	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00EAH	TM2_CTL	STC	RL/S	TKES	-	-	-	TKI1	TKI0	-	√

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event clock-in trigger edge selector; 0: rising edge, 1: falling edge

TKI1	TKI0	Selected TM2 input frequency
1	0	F_{X32}
1	1	P0.5



TM2

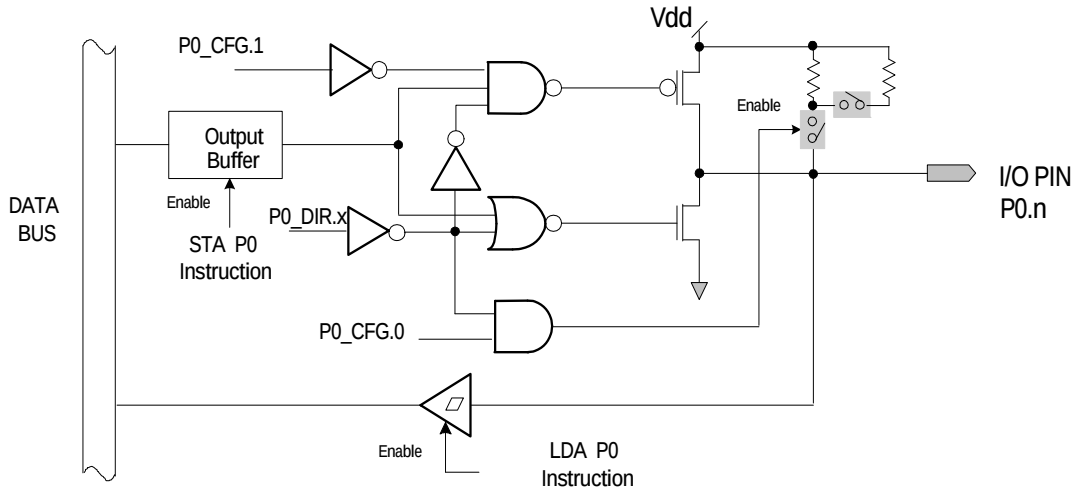
I/O Ports

Port 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D8H	P0	-	-	P05	P04	P03	P02	P01	P00	√	√
0240H	P0_DIR	-	-	DR05	DR04	DR03	DR02	DR01	DR00	√	√
0241H	P0_CFG	CF07	CF06	CF05	CF04	CF03	CF02	CF01	CF00	√	√

Port 0 is a 6-bit I/O port; each pin can be programmed as input or output individually. When port0.n is configured as an output pin, the port0.n pin would output the logic content of P0.n. However, reading from the output pins would always read logic '1'. When the port0.n is configured as an input pin, reading P0.n would read the logic value from pad.

Input/Output Pin of the P0



P0.4 and P0.5 could be the input clock sources of timer 1 and timer 2 respectively.

P0_DIR (Port 0 Direction)

P0_DIR.n = 0: P0.n is configured as an input pin. (Default)

1: P0.n is configured as an output pin.

P0_CFG (Port 0 pull-high/CMOS/NMOS/strobe setting)

P0_CFG.0: P0.0 ~ P0.3 Pull-high control, 0: disable, 1:enable

P0_CFG.1: P0.0 ~ P0.3 CMOS/NMOS selector, 0: CMOS, 1:NMOS

P0_CFG.2: P0.0 ~ P0.3 Pull-high resistor value control, 0: strong (50K Ohm), 1: weak (250K Ohm)

P0_CFG.3: P0.0 ~ P0.3 Key strobe function control, 0: disable, 1:enable

P0_CFG.4: P0.4 ~ P0.5 Pull-high control, 0: disable, 1:enable

P0_CFG.5: P0.4 ~ P0.5 CMOS/NMOS selector, 0: CMOS, 1:NMOS

P0_CFG.6: P0.4 ~ P0.5 Pull-high resistor value control, 0: strong (50K Ohm), 1: weak (250K Ohm)

P0_CFG.7: P0.4 ~ P0.5 Key strobe function control, 0: disable, 1:enable

At initial reset, all ports of P0 are in input mode. Each pin of port P0 can be specified as input or output mode independently by the P0DIR registers. When P0 is used as output port, CMOS or NMOS open drain output type can be selected by the P0_CFG register. Port P0 has the internal pull-high resistors that can be enabled/disabled by specifying the P0_CFG.0 respectively. The pull-high resistor would be disabled automatically if the port is specified as output mode. When P0.0 or P0.4 are used as input mode and the RLH_EN, and IRQ_EN corresponding to the P0 port are set, a signal change at the P0.0 or P0.4 will execute the hold mode release or interrupt subroutine. Both the raising or falling signal of P0.0/P0.4 will set the port P0 event. The Schmitt trigger circuit is added in the input port part of all I/O pins.

Please set port 0 as output high before set it as input mode, if the internal pull-high effect needs to be speeded up. If the I/O ports are not used in your application, please set them as input with pull-high or output mode to avoid unnecessary power consumption.

When the internal pull-high register is enabled and the P0_CFG.3 is 0, the P0.0 ~ P0.3 is always pulled high. When a. internal pull-high register is enabled, b. the P0_CFG.3 is 1 and c. LCD function is enabled, the P0.0 ~ P0.3 is pulled high only for the last 30 microseconds of the low-active period of each LCD COM.

Key Strobe function

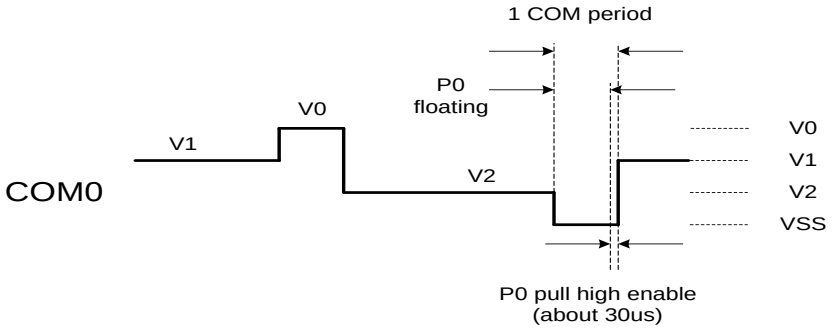
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
0252H	STB_CTL	-	-	-	-	-	-	STB_ CLR	SEG_ MASK	-	√
0253H	STB_COM	-	-	-	-	-	SC2	SC1	SC0	√	-
0254H	P01_LTH	P11	P10	P05	P04	P03	P02	P01	P00	√	-

STB_CTL (Key strobe control)

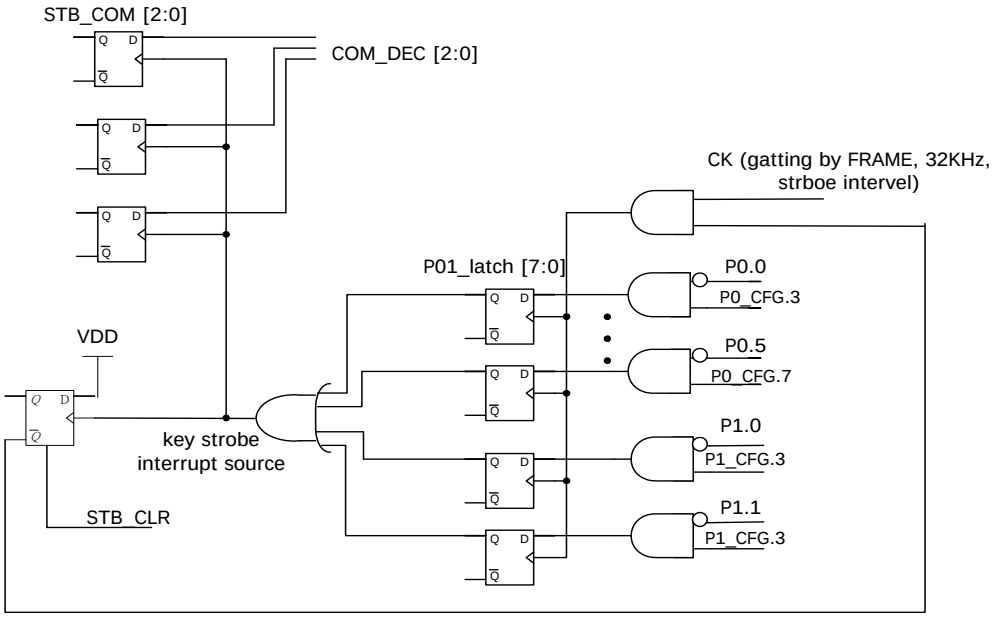
STB_CLR: setting this bit would enable STB_COM and P01_LTH update process

SEG_MASK = 0: LCD output the content of LCD RAM.

1: LCD output data '0's



When P0CFG.3 (or P0CFG.7 and P1CFG.3) is set to 1 and LCD function is turned on, the key strobe function is enabled. When a P0.n (or P1.n) pin which key strobe function is enabled senses logic low, the corresponding bit of P01_LTH would be set, and the current COM number, 0 ~ 4 (or 0 ~ 3), would be latched to register STB_COM. The content of P01_LTH and STB_COM would not be updated until the STB_CLR bit of STB_CTL register is set. Program could judge which key of the key-matrix being pressed by decoding the STB_COM and P01_LTH registers. Note that when the STB_CLR is set, the content of P01_LTH will be cleared to 00H.



Port 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D9H	P1	-	-	-	-	-	-	P11	P10	√	√
0244H	P1_DIR	-	-	-	-	-	-	DR11	DR10	√	√
0245H	P1_CFG	-	-	-	-	CF13	CF12	CF11	CF10	√	√

Port 1 is a 2-bit I/O port; each pin can be programmed as input or output individually. When port1.n is configured as an output pin, the port1.n pin would output the logic content of P1.n. However, reading from the output pins would always read logic '1'. Whether the port1.n is configured as an input, reading P1.n would always read the logic value from pad.

Port 1 has multiple functions. P1.0 / P1.1 could be timer 1 / timer 2 IR carrier output pins.

P1_DIR (Port 1 Direction)

P1_DIR.n = 0: P1.n is configured as an input pin. (Default)

1: P1.n is configured as an output pin.

P1_CFG (Port 1 pull-high/CMOS/NMOS/strobe setting)

P1_CFG.0: P1.0 ~ P1.1 Pull-high control, 0: disable, 1:enable

P1_CFG.1: P1.0 ~ P1.1 CMOS/NMOS selector, 0: CMOS, 1:NMOS

P1_CFG.2: P1.0 ~ P1.1 Pull-high resistor value control, 0: strong (50K Ohm) 1weak (250K Ohm)

P1_CFG.3: P1.0 ~ P1.1 Key strobe function control, 0: disable, 1:enable

When a pin is configured as an output pin, the setting of P1_CFG.0 is ignored and the corresponding pull-high resistor is disabled.

Only P1.0 and P1.1 support key strobe function. When internal pull-high register is enabled and the P1_CFG.3 is 0, the P1.0 ~ P1.1 is always pulled high. When internal pull-high register is enabled

and the P1_CFG.3 is 1, P1.0 ~ P1.1 is pulled high only for the last 30 microseconds of the low-active period of each LCD COM. For more detail, please refer to the port0 key strobe function.

Port 1 multi-function selector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	P1_MFR	-	-	-	-	-	-	PS1	PS0	-	√

The port 1 can be programmed to special function via P1_MFR register.

PS0 = 0: P1.0 is a normal I/O

1: P1.0 is TM1 carrier output

PS1 = 0: P1.1 is a normal I/O

1: P1.1 is TM2 carrier output

Port 2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DAH	P2	-	-	-	-	-	-	P21	P20	√	√
0248H	P2_DIR	-	-	-	-	-	-	DR21	DR20	√	√
0249H	P2_CFG	-	-	-	-	CF23	CF22	CF21	CF20	√	√

Port 2 is a 2-bit I/O port; each pin can be programmed as input or output individually. When port2.n is configured as an output pin, the port2.n pin would output the logic content of P2.n. However, reading from the output pins would always read logic '1'. When the port2.n is configured as an input pin, reading P2.n would always read the logic value from pad. P2.1 is a 3K Ohm pull low resistor during power-on reset.

P2_DIR (Port 2 Direction)

P2_DIR.n = 0: P2.n is configured as an input pin. (Default)

1: P2.n is configured as an output pin.

P2_CFG (Port 2 pull-high/CMOS/NMOS setting)

P2_CFG.0: P2.0 Pull-high (50K Ohm) control, 0: disable, 1:enable

P2_CFG.1: P2.1 Pull-high (50K Ohm) control, 0: disable, 1:enable

P2_CFG.2: P2.0 CMOS/NMOS selector, 0: CMOS, 1:NMOS

P2_CFG.3: P2.1 CMOS/NMOS selector, 0: CMOS, 1:NMOS

Port 2 multi-function selector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	P2_MFR	-	-	-	-	-	-	0	0	-	√

The port 2 can be programmed to special function via P2_MFR register. (Reserve function)

PS0: 0: P2.0 is a normal I/O (default)

PS1: 0: P2.1 is a normal I/O (default)

Port 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DBH	P3	P37	P36	P35	P34	P33	P32	P31	P30	√	√
024CH	P3_DIR	-	-	-	-	-	-	DR31	DR30	√	√

Port 3 is an 8-bit I/O port. It share the pins with LCD SEG [24:31]. The pins can be programmed as input or output by nibble. When port3.n is configured as an output pin, the port3.n pin would be a CMOS type output pin and outputs the logic content of P3.n. However, reading from the output pins would always read logic '0'. Whether the port3.n is configured as an input pin, it would be a floating input pin, and reading P3.n would always read the logic value from pad.

P3_DIR (Port 3 Direction)

P3_DIR.0 = 0: P3 [0: 3] is configured as an input pin. (Default)

1: P3 [0: 3] is configured as an output pin.

P3_DIR.1 = 0: P3 [4: 7] is configured as an input pin. (Default)

1: P3 [4: 7] is configured as an output pin.

Port 3 multi-function selector

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D7H	P3_MFR	-	-	-	-	-	-	PS1	PS0	-	√

The port 3 can be programmed to special function via P3_MFR register.

PS0: 0: P3 [0:3] are disabled, the pins are used as LCD SEG [31:28] (default);

1: P3 [0:3] are enabled

PS1: 0: P3 [4:7] are disabled, the pins are used as LCD SEG [27:24] (default);

1: P3 [4:7] are enabled

LCD Controller/Driver

The MLC510PA can directly drive an LCD with 32 segment output pins and 4 or 5 common output pins for a total of 32 × 4 or 32 x 5 dots. LCD control register can be used to select LCD display configuration. LCD driving mode is 1/3 bias 1/4 duty or 1/5 duty and frame frequency is about 81.38Hz (or 65.10Hz at 1/5 duty). When CPU access the LCD RAM area, the access path of the LCD RAM will be transferred from LCD driver to CPU automatically.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
0250H	LCD_CR	LIT	DT_S	CKS1	CKS0	DI3	DI2	DI1	DI0	√	√

LIT: LCD on/off control bit. 0: off (default), 1:on

DT_S: LCD common number selector. 0: 5 (default), 1:4

DI3~DI0: LCD driving current select. The recommended value is 0111B.

LCD scan rate, FCOM, is derived from the clock source of Divider 1. The relation between the

CKS1, CKS0, FCOM and FDIV1_IN is shown in the following table.

CKS1	CKS0	Selected F_{COM} frequency
0	0	F_{DIV1_IN} / 96
0	1	F_{DIV1_IN} / 6144
1	0	F_{DIV1_IN} / 12288
1	1	F_{DIV1_IN} / 24576

The LCD frame rate can be calculated with the equation:

$F_{FRAME} = F_{COM}$ / (COM No.)

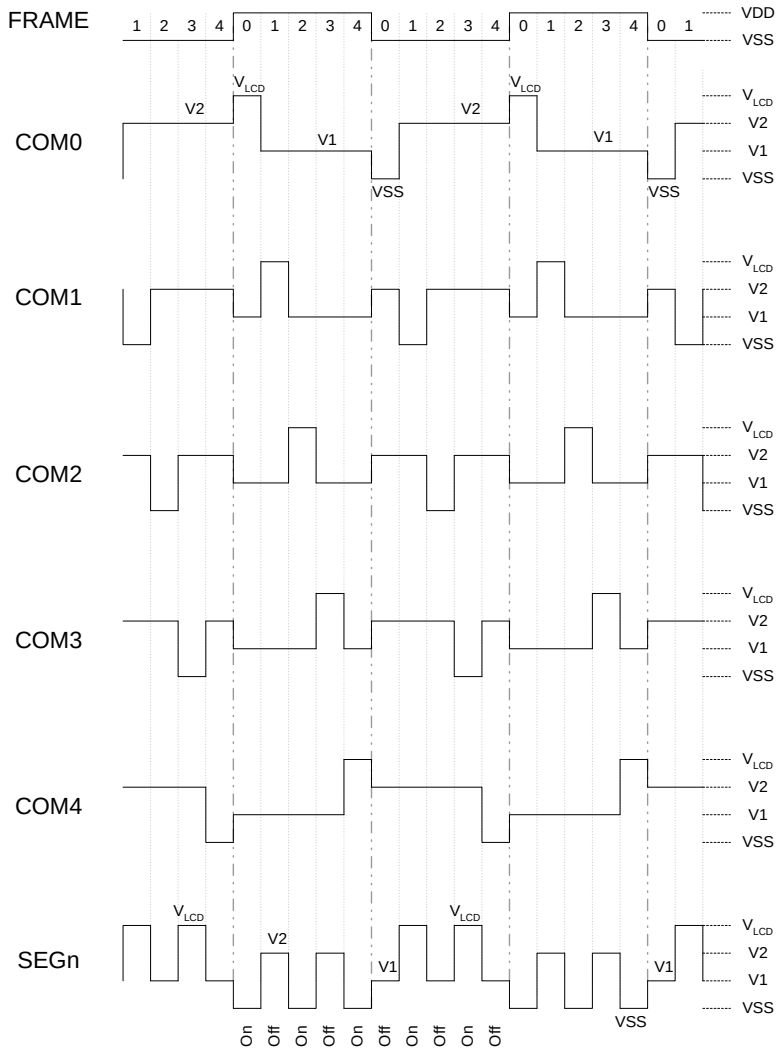
Typical selection combination for 1/4 duty and 1/5 duty are shown below:

COM No.	F_{DIV1_IN}	Selected F_{COM} frequency	F_{FRAME}
4	6M	F_{DIV1_IN} / 24576	61.04
4	4M	F_{DIV1_IN} / 12288	81.38
4	2M	F_{DIV1_IN} / 6144	81.38
4	32K	F_{DIV1_IN} / 96	85.33
5	6M	F_{DIV1_IN} / 12288	97.66
5	4M	F_{DIV1_IN} / 12288	65.10
5	2M	F_{DIV1_IN} / 6144	65.10
5	32K	F_{DIV1_IN} / 96	68.27

There are 20 LCD data RAM in MLC510PA. When the bit value of LCD data RAM is “1”, the LCD is turned on. When the bit value of LCD data RAM is “0”, the LCD is turned off. The contents of the LCD data RAM are sent out through the segment 0 to segment 31 pins by a direct memory access. The relationship between the LCD data RAM and segment/common pins is shown below.

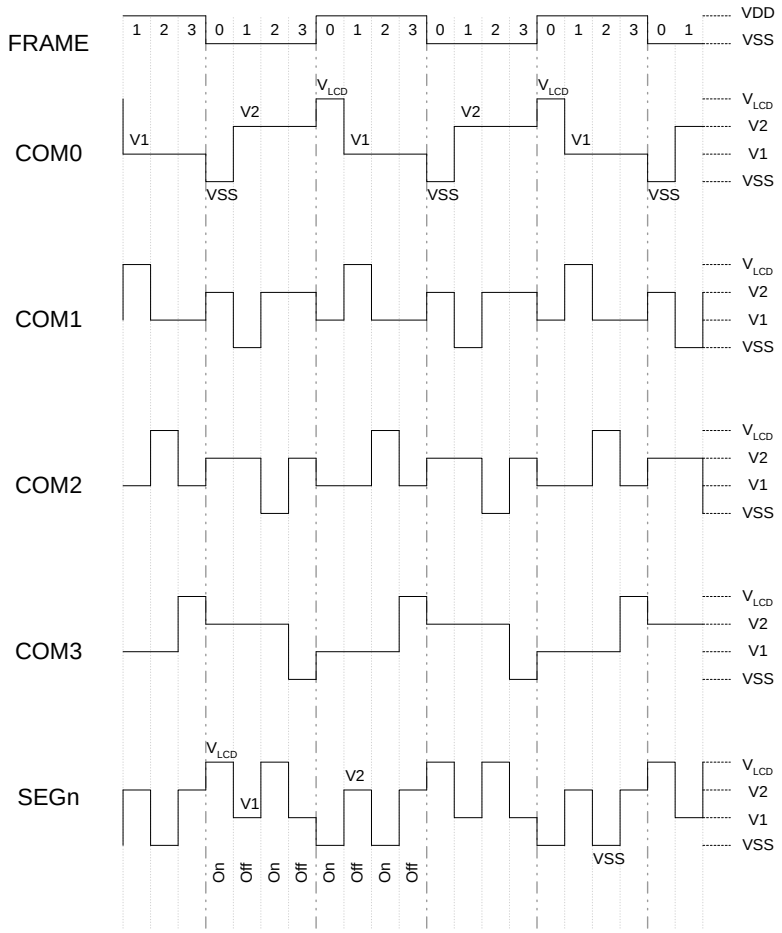
LCD Data RAM	Common	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1000H	COM 0	0/1 (07)	0/1 (06)	0/1 (05)	0/1 (04)	0/1 (03)	0/1 (02)	0/1 (01)	0/1 (00)
1001H		0/1 (0F)	0/1 (0E)	0/1 (0D)	0/1 (0C)	0/1 (0B)	0/1 (0A)	0/1 (09)	0/1 (08)
1002H		0/1 (17)	0/1 (16)	0/1 (15)	0/1 (14)	0/1 (13)	0/1 (12)	0/1 (11)	0/1 (10)
1003H		0/1 (1F)	0/1 (1E)	0/1 (1D)	0/1 (1C)	0/1 (1B)	0/1 (1A)	0/1 (19)	0/1 (18)
1004H	COM 1	0/1 (07)	0/1 (06)	0/1 (05)	0/1 (04)	0/1 (03)	0/1 (02)	0/1 (01)	0/1 (00)
1005H		0/1 (0F)	0/1 (0E)	0/1 (0D)	0/1 (0C)	0/1 (0B)	0/1 (0A)	0/1 (09)	0/1 (08)
1006H		0/1 (17)	0/1 (16)	0/1 (15)	0/1 (14)	0/1 (13)	0/1 (12)	0/1 (11)	0/1 (10)
1007H		0/1 (1F)	0/1 (1E)	0/1 (1D)	0/1 (1C)	0/1 (1B)	0/1 (1A)	0/1 (19)	0/1 (18)
1008H	COM 2	0/1 (07)	0/1 (06)	0/1 (05)	0/1 (04)	0/1 (03)	0/1 (02)	0/1 (01)	0/1 (00)
1009H		0/1 (0F)	0/1 (0E)	0/1 (0D)	0/1 (0C)	0/1 (0B)	0/1 (0A)	0/1 (09)	0/1 (08)
100AH		0/1 (17)	0/1 (16)	0/1 (15)	0/1 (14)	0/1 (13)	0/1 (12)	0/1 (11)	0/1 (10)
100BH		0/1 (1F)	0/1 (1E)	0/1 (1D)	0/1 (1C)	0/1 (1B)	0/1 (1A)	0/1 (19)	0/1 (18)
100CH	COM 3	0/1 (07)	0/1 (06)	0/1 (05)	0/1 (04)	0/1 (03)	0/1 (02)	0/1 (01)	0/1 (00)
100DH		0/1 (0F)	0/1 (0E)	0/1 (0D)	0/1 (0C)	0/1 (0B)	0/1 (0A)	0/1 (09)	0/1 (08)
100EH		0/1 (17)	0/1 (16)	0/1 (15)	0/1 (14)	0/1 (13)	0/1 (12)	0/1 (11)	0/1 (10)
100FH		0/1 (1F)	0/1 (1E)	0/1 (1D)	0/1 (1C)	0/1 (1B)	0/1 (1A)	0/1 (19)	0/1 (18)
1010H	COM 4	0/1 (07)	0/1 (06)	0/1 (05)	0/1 (04)	0/1 (03)	0/1 (02)	0/1 (01)	0/1 (00)
1011H		0/1 (0F)	0/1 (0E)	0/1 (0D)	0/1 (0C)	0/1 (0B)	0/1 (0A)	0/1 (09)	0/1 (08)
1012H		0/1 (17)	0/1 (16)	0/1 (15)	0/1 (14)	0/1 (13)	0/1 (12)	0/1 (11)	0/1 (10)
1013H		0/1 (1F)	0/1 (1E)	0/1 (1D)	0/1 (1C)	0/1 (1B)	0/1 (1A)	0/1 (19)	0/1 (18)

1/5 duty 1/3 bias



1/4 duty 1/3 bias

note: In this mode, the signal of COM4 is same as the 'FRAME' signal shown below.



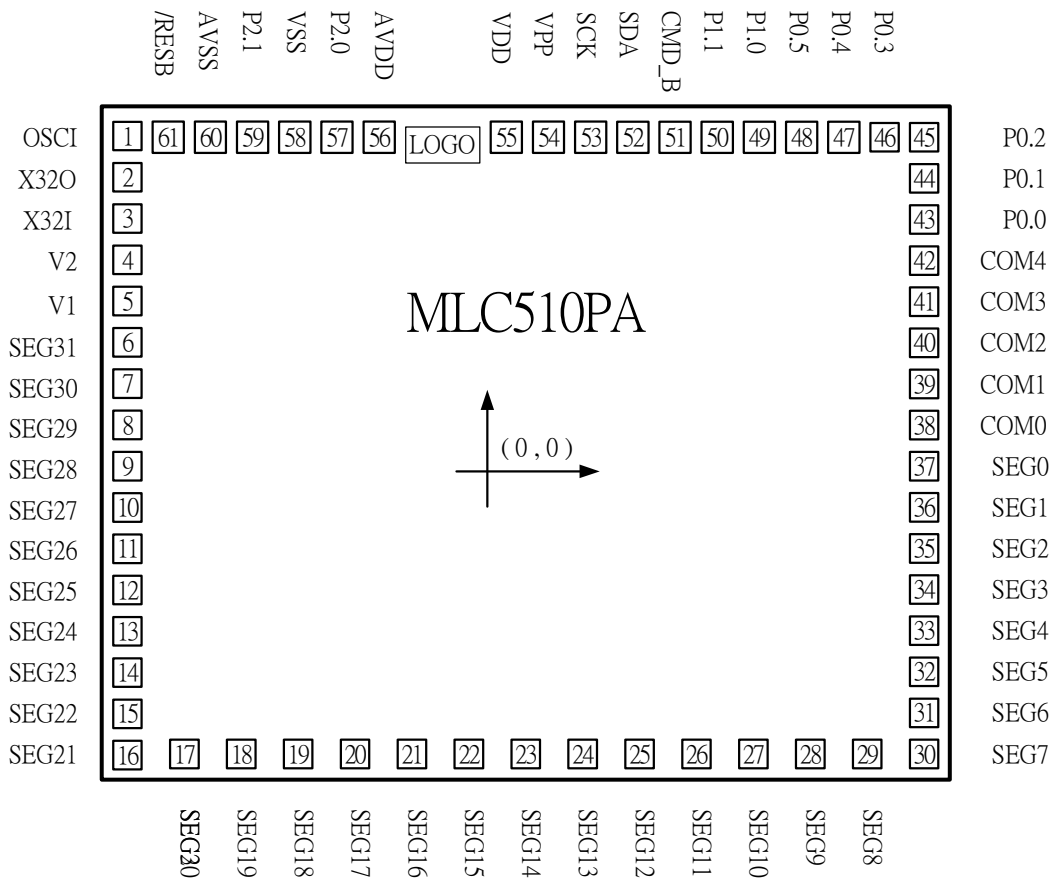
Programming Notice

The status after different reset condition is listed below:

	Power on reset	CPU /RST pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

Application Circuit

Pad Assignment



Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +5.0	V
Applied Input / Output Voltage	-0.3 to V_{DD} + 0.3	V
Power Dissipation	60	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C
ESD Protection	-3 to +3	KV

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

(V_{DD}-V_{SS} = 3.0 V, F_{OSC} = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	2.2	-	5.5	V
Op. Current 1	I_{OP1}	Fast mode, No load Fcpu=4Mhz, LCD on	-	1.8	5.6	mA
Op. Current 2	I_{OP2}	Slow mode, No load Fcpu=32768Hz, LCD on	-	20	30	uA
Standby Current	I_{STB1}	Stop mode, No load, LCD off	-	1	3	μA
	I_{STB2}	Halt mode, No load, LCD on, Fcpu=32768Hz, DIV1x INT on	-	10	20	μA
Input High Voltage	V_{IH}	-	0.8 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.4	V
Port 0, 1, 2, 3 drive current	I_{OH0}	V_{OH} = 2.4V, V_{DD} = 3.0V	-	1.8	-	mA
Port 0, 1, 2 sink current	I_{OL0}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	3.0	-	mA
Port 3 sink current	I_{OL1}	V_{OL} = 0.4V, V_{DD} = 3.0V	-	1.5	-	mA
SEG0 ~ SEG31 drive current	I_{OH1}	V_{OH} = 2.4V, V_{LCD} = 3.0V	0.3	-	-	μA
SEG0 ~ SEG31 sink current	I_{OL1}	V_{OL} = 0.4V, V_{LCD} = 0.0V	0.4	-	-	μA
Internal Pull-high Resistor (strong)	R_{PH1}	V_{IL} = 0V	-	50K	-	Ω
Internal Pull-high Resistor (weak)	R_{PH2}	V_{IL} = 0V	-	250K	-	Ω

AC Characteristics

(Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CPU Op. Frequency	F_{CPU}	R, V_{DD} = 3.0V	-	2	6	MHz
Frequency Deviation by Voltage Drop for RC Oscillator	$\frac{\Delta f}{f}$	$\frac{f(3.6V) - f(3.0V)}{f(3.0V)}$	-	7	10	%
POR duration	T_{POR}	F_{OSC} = 32768	-	600	1000	mS

Vision History

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 2007		Initial issue