MLP1N06CL

Preferred Device

SMARTDISCRETES™ MOSFET
1 Amp, 62 Volts, Logic Level
N–Channel TO–220

These SMARTDISCRETES devices feature current limiting for short circuit protection, an integral gate–to–source clamp for ESD protection and gate–to–drain clamp for over–voltage protection. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal gate–to–source and gate–to–drain clamps allow the devices to be applied without use of external transient suppression components. The gate–to–source clamp protects the MOSFET input from electrostatic gate voltage stresses up to 2.0 kV. The gate–to–drain clamp protects the MOSFET drain from drain avalanche stresses that occur with inductive loads. This unique design provides voltage clamping that is essentially independent of operating temperature.

- Temperature Compensated Gate–to–Drain Clamp Limits Voltage Stress Applied to the Device and Protects the Load From Overvoltage
- Integrated ESD Diode Protection
- Controlled Switching Minimizes RFI
- Low Threshold Voltage Enables Interfacing Power Loads to Microprocessors

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	Clamped	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	Clamped	Vdc
Gate–to–Source Voltage – Continuous	V_{GS}	±10	Vdc
Drain Current – Continuous – Single Pulse	I_D I_{DM}	Self–limited 1.8	Adc
Total Power Dissipation	P_D	40	Watts
Electrostatic Discharge Voltage (Human Body Model)	ESD	2.0	kV
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–50 to 150	°C

THERMAL CHARACTERISTICS

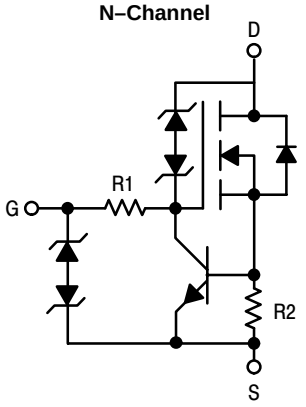
Thermal Resistance, Junction to Case Thermal Resistance, Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case	T_L	260	°C

ON Semiconductor™

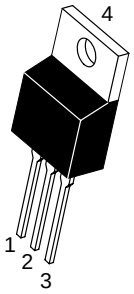
http://onsemi.com

1 AMPERE
62 VOLTS (Clamped)
$R_{DS(on)}$ = 750 mΩ

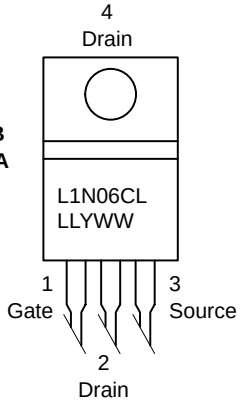
N–Channel



MARKING DIAGRAM & PIN ASSIGNMENT



TO–220AB
CASE 221A
STYLE 5



L1N06CL	= Device Code
LL	= Location Code
Y	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
MLP1N06CL	TO–220AB	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

Rating	Symbol	Value	Unit
Single Pulse Drain–to–Source Avalanche Energy (Starting T_J = 25°C, I_D = 2.0 A, L = 40 mH) (Figure 6)	E_{AS}	80	mJ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Sustaining Voltage (Internally Clamped) (I_D = 20 mA, V_{GS} = 0) (I_D = 20 mA, V_{GS} = 0, T_J = 150°C)	$V_{(BR)DSS}$	 59 59	 62 62	 65 65	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 45 V, V_{GS} = 0) (V_{DS} = 45 V, V_{GS} = 0, T_J = 150°C)	I_{DSS}	 – –	 0.6 6.0	 5.0 20	μAdc
Gate–Body Leakage Current (V_G = 5.0 V, V_{DS} = 0) (V_G = 5.0 V, V_{DS} = 0, T_J = 150°C)	I_{GSS}	 – –	 0.5 1.0	 5.0 20	μAdc
ON CHARACTERISTICS (Note 1.)					
Gate Threshold Voltage (I_D = 250 μA, V_{DS} = V_{GS}) (I_D = 250 μA, V_{DS} = V_{GS}, T_J = 150°C)	$V_{GS(th)}$	 1.0 0.6	 1.5 –	 2.0 1.6	Vdc
Static Drain–to–Source On–Resistance (I_D = 1.0 A, V_{GS} = 4.0 V) (I_D = 1.0 A, V_{GS} = 5.0 V) (I_D = 1.0 A, V_{GS} = 4.0 V, T_J = 150°C) (I_D = 1.0 A, V_{GS} = 5.0 V, T_J = 150°C)	$R_{DS(on)}$	 – – – –	 0.63 0.59 1.1 1.0	 0.75 0.75 1.9 1.8	Ohms
Forward Transconductance (I_D = 1.0 A, V_{DS} = 10 V)	g_{FS}	1.0	1.4	–	mhos
Static Source–to–Drain Diode Voltage (I_S = 1.0 A, V_{GS} = 0)	V_{SD}	–	1.1	1.5	Vdc
Static Drain Current Limit (V_{GS} = 5.0 V, V_{DS} = 10 V) (V_{GS} = 5.0 V, V_{DS} = 10 V, T_J = 150°C)	$I_{D(lim)}$	 2.0 1.1	 2.3 1.3	 2.75 1.8	A
RESISTIVE SWITCHING CHARACTERISTICS (Note 1.)					
Turn–On Delay Time	(V_{DD} = 25 V, I_D = 1.0 A, V_{GS} = 5.0 V, R_G = 50 Ohms)	$t_{d(on)}$	–	1.2	2.0	μs
Rise Time		t_r	–	4.0	6.0	
Turn–Off Delay Time		$t_{d(off)}$	–	4.0	6.0	
Fall Time		t_f	–	3.0	5.0	

1. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

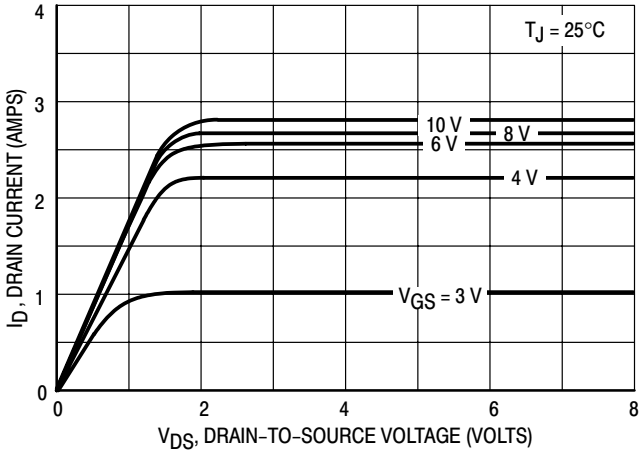


Figure 1. Output Characteristics

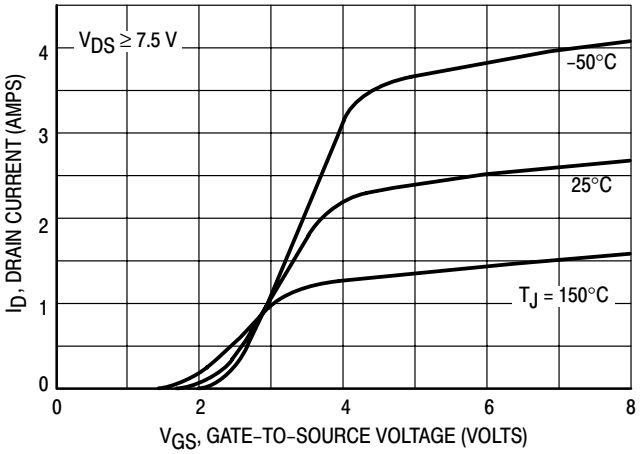


Figure 2. Transfer Function

THE SMARTDISCRETES CONCEPT

From a standard power MOSFET process, several active and passive elements can be obtained that provide on–chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability as well as system cost reduction. The SMARTDISCRETES device functions can now provide an economical alternative to smart power ICs for power applications requiring low on–resistance, high voltage and high current.

These devices are designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontroller unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

OPERATION IN THE CURRENT LIMIT MODE

The amount of time that an unprotected device can withstand the current stress resulting from a shorted load before its maximum junction temperature is exceeded is dependent upon a number of factors that include the amount of heatsinking that is provided, the size or rating of the device, its initial junction temperature, and the supply voltage. Without some form of current limiting, a shorted load can raise a device's junction temperature beyond the maximum rated operating temperature in only a few milliseconds.

Even with no heatsink, the MLP1N06CL can withstand a shorted load powered by an automotive battery (10 to 14 Volts) for almost a second if its initial operating temperature is under 100°C. For longer periods of operation in the current–limited mode, device heatsinking can extend operation from several seconds to indefinitely depending on the amount of heatsinking provided.

SHORT CIRCUIT PROTECTION AND THE EFFECT OF TEMPERATURE

The on–chip circuitry of the MLP1N06CL offers an integrated means of protecting the MOSFET component from high in–rush current or a shorted load. As shown in the schematic diagram, the current limiting feature is provided by an NPN transistor and integral resistors R1 and R2. R2 senses the current through the MOSFET and forward biases the NPN transistor's base as the current increases. As the NPN turns on, it begins to pull gate drive current through R1, dropping the gate drive voltage across it, and thus lowering the voltage across the gate–to–source of the power MOSFET and limiting the current. The current limit is temperature dependent as shown in Figure 3, and decreases from about 2.3 Amps at 25°C to about 1.3 Amps at 150°C.

Since the MLP1N06CL continues to conduct current and dissipate power during a shorted load condition, it is important to provide sufficient heatsinking to limit the device junction temperature to a maximum of 150°C.

The metal current sense resistor R2 adds about 0.4 ohms to the power MOSFET's on–resistance, but the effect of temperature on the combination is less than on a standard MOSFET due to the lower temperature coefficient of R2. The on–resistance variation with temperature for gate voltages of 4 and 5 Volts is shown in Figure 5.

Back–to–back polysilicon diodes between gate and source provide ESD protection to greater than 2 kV, HBM. This on–chip protection feature eliminates the need for an external Zener diode for systems with potentially heavy line transients.

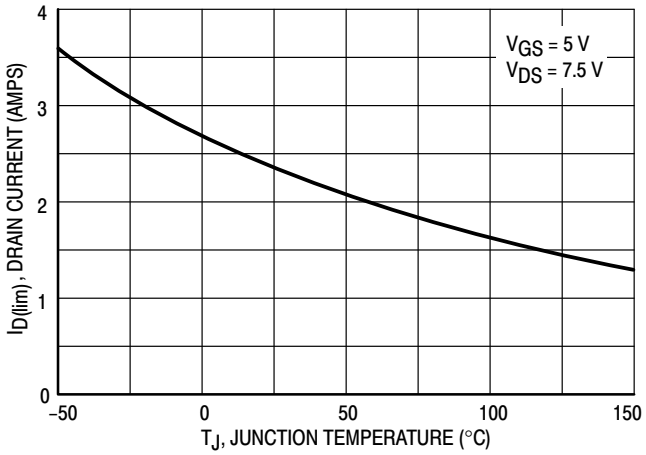


Figure 3. $I_{D(lim)}$ Variation With Temperature

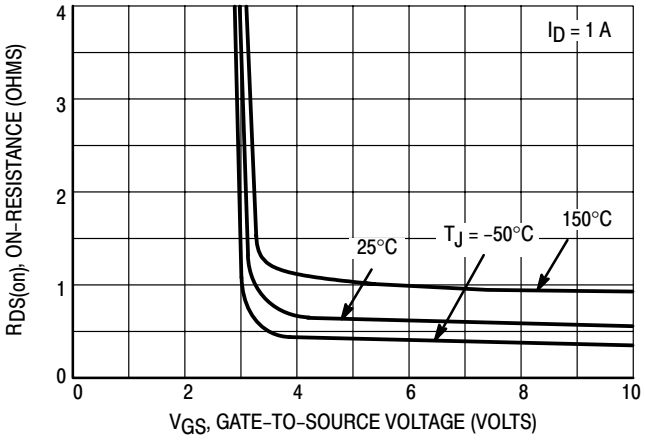


Figure 4. $R_{DS(on)}$ Variation With Gate−To−Source Voltage

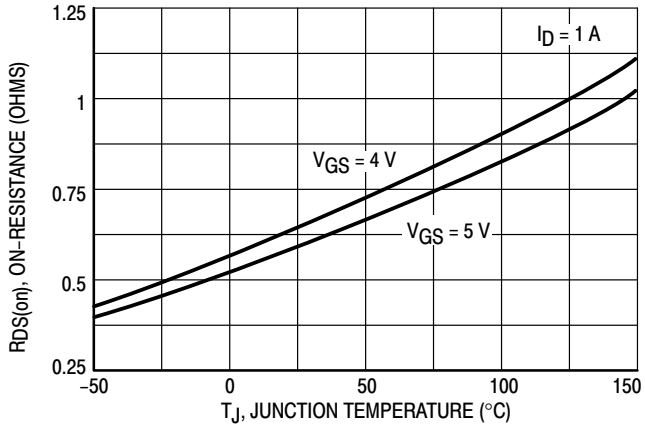


Figure 5. On−Resistance Variation With Temperature

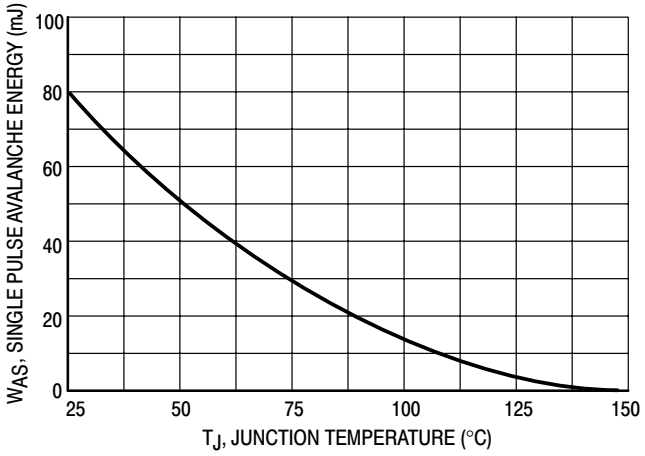


Figure 6. Single Pulse Avalanche Energy versus Junction Temperature

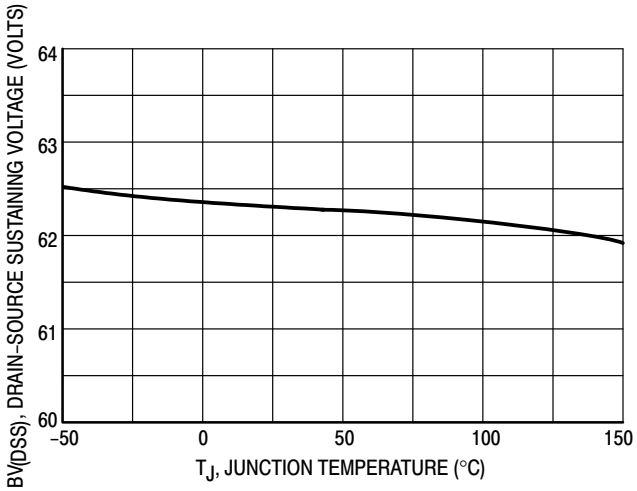


Figure 7. Drain−Source Sustaining Voltage Variation With Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance – General Data and Its Use” provides detailed instructions.

MAXIMUM DC VOLTAGE CONSIDERATIONS

The maximum drain–to–source voltage that can be continuously applied across the MLP1N06CL when it is in current limit is a function of the power that must be dissipated. This power is determined by the maximum current limit at maximum rated operating temperature (1.8 A at 150°C) and not the $R_{DS(on)}$. The maximum voltage can be calculated by the following equation:

$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)} (R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of V_{DS} applied when operating in a duty cycle mode can be approximated by:

$$V_{DS} = \frac{150 - T_C}{I_{D(lim)} \times DC \times R_{\theta JC}}$$

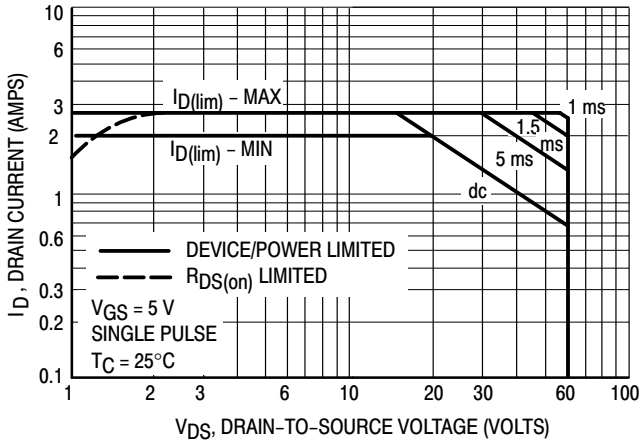


Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLP1N06CL)

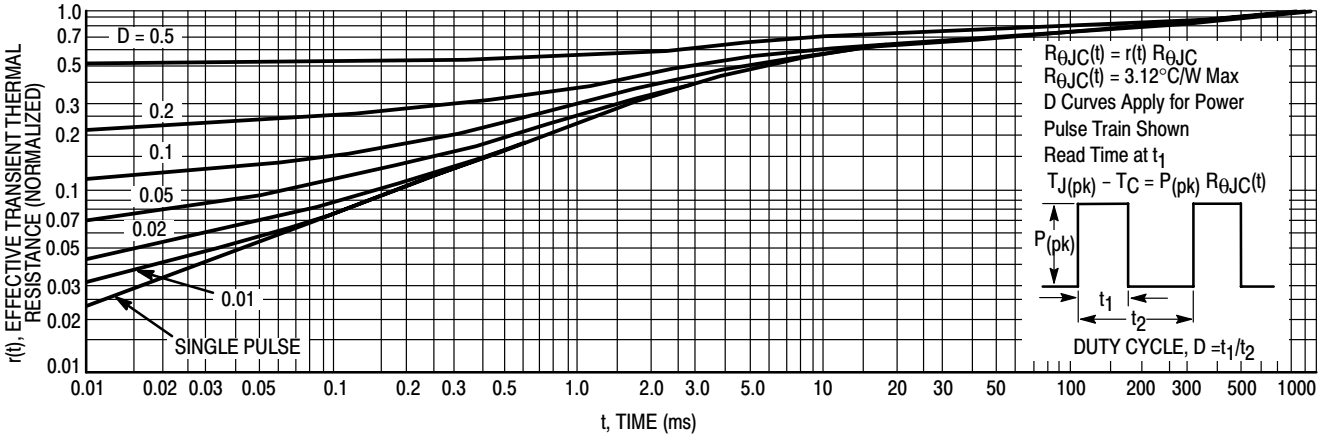


Figure 9. Thermal Response (MLP1N06CL)

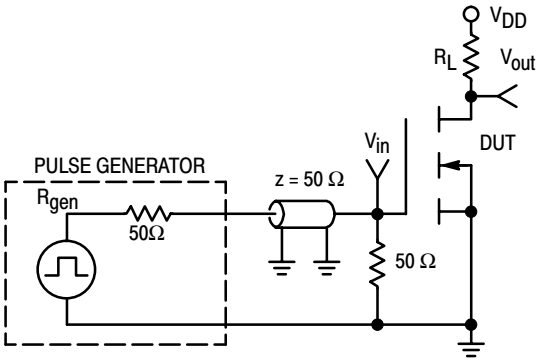


Figure 10. Switching Test Circuit

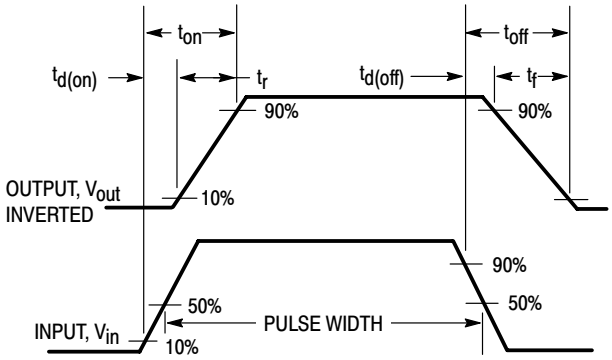


Figure 11. Switching Waveforms

ACTIVE CLAMPING

SMARTDISCRETES technology can provide on–chip realization of the popular gate–to–source and gate–to–drain Zener diode clamp elements. Until recently, such features have been implemented only with discrete components which consume board space and add system cost. The SMARTDISCRETES technology approach economically melds these features and the power chip with only a slight increase in chip area.

In practice, back–to–back diode elements are formed in a polysilicon region monolithicly integrated with, but electrically isolated from, the main device structure. Each back–to–back diode element provides a temperature compensated voltage element of about 7.2 volts. As the polysilicon region is formed on top of silicon dioxide, the diode elements are free from direct interaction with the conduction regions of the power device, thus eliminating parasitic electrical effects while maintaining excellent thermal coupling.

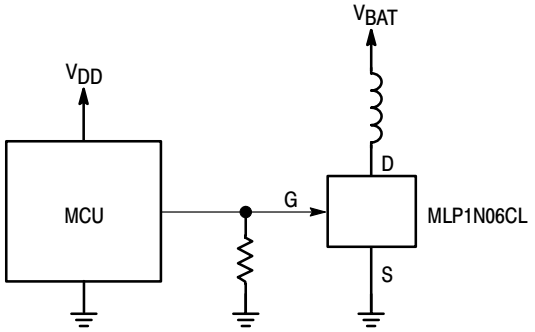
To achieve high gate–to–drain clamp voltages, several voltage elements are strung together; the MLP1N06CL uses 8 such elements. Customarily, two voltage elements are used to provide a 14.4 volt gate–to–source voltage clamp. For the MLP1N06CL, the integrated gate–to–source voltage elements provide greater than 2.0 kV electrostatic voltage protection.

The avalanche voltage of the gate–to–drain voltage clamp is set less than that of the power MOSFET device. As soon as the drain–to–source voltage exceeds this avalanche voltage, the resulting gate–to–drain Zener current builds a gate voltage across the gate–to–source impedance, turning on the power device which then conducts the current. Since virtually all of the current is carried by the power device, the gate–to–drain voltage clamp element may be small in size. This technique of establishing a temperature compensated drain–to–source sustaining voltage (Figure 7) effectively removes the possibility of drain–to–source avalanche in the power device.

The gate–to–drain voltage clamp technique is particularly useful for snubbing loads where the inductive energy would otherwise avalanche the power device. An improvement in ruggedness of at least four times has been observed when inductive energy is dissipated in the gate–to–drain clamped conduction mode rather than in the more stressful gate–to–source avalanche mode.

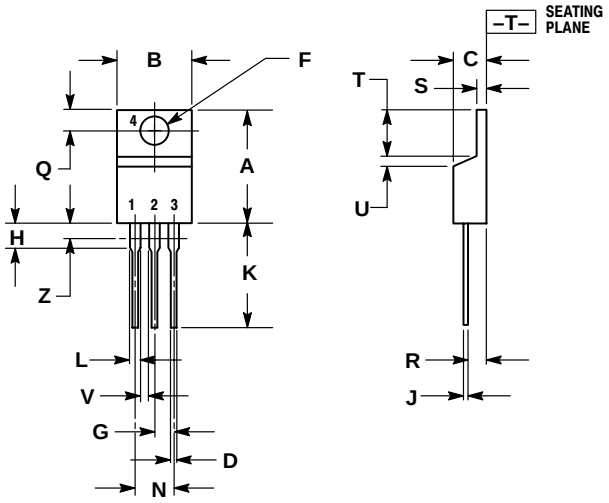
TYPICAL APPLICATIONS: INJECTOR DRIVER, SOLENOIDS, LAMPS, RELAY COILS

The MLP1N06CL has been designed to allow direct interface to the output of a microcontrol unit to control an isolated load. No additional series gate resistance is required, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition in the event of an MCU failure. The internal clamps allow the device to be used without any external transistent suppressing components.



PACKAGE DIMENSIONS

TO–220 THREE–LEAD
TO–220AB
CASE 221A–09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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