Datasheet MLX16201-Jxx

Intelligent relay driver for automotive applications
ROM version for series production

1. Features

CPU and Interrupts

- WORD- (16 Bit), BYTE- (8 Bit), and BIT- (1Bit) Operations possible
- 11 different user interrupt sources (including RESET)

Memories

- 8k*8 user ROM
- 256*8 RAM
- 128*16 EEPROM

Periphery

- 1 On-Chip-Timer
- 1 Timer-Capture-Register (16 bits)
- 2 Timer-Compare-Register (16 bits)
- Window watch dog (5ms/10ms)
- 1 PWM output 20.8 kHz, 7-Bit+1 (duty cycle from 0 to 100%)
- 1 A/D converter (8 bits, 16µs) internal and external reference possible
- 8 ADC-channels analogue multiplexer
- On-Chip-Temperature-Sensor
- 2 Relay driver outputs, integrated free wheel function
- 2 voltage outputs for driving external circuitry
- 8 bi-directional ports with different possible thresholds, 5V output function
- 2 Interrupt inputs for timer capture

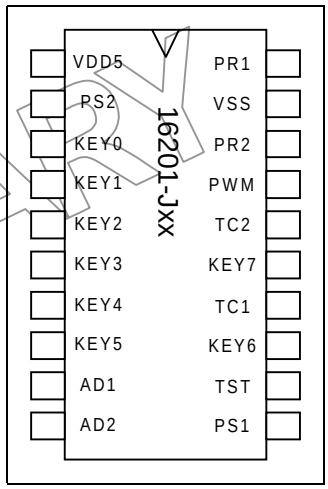
Additional features

- On-Chip-8 MHz-Oscillator (No external components)
- 4V to 26V voltage range, 80V load dump protected,
- typical 150 µA sleep mode current
- Small SO20 package

Development tools

- Development Environment available with the 10108xy:
  - Assembler, Linker, Object-File-Generator, HEX-File Generator, C-Compiler
  - ROM-Emulator, In-Circuit-Emulator
  - PLCC68 for external ROM-Possibility, ROM-Emulation and In-Circuit-Emulation
  - SO24 as OTP for SW development and SW evaluation
  - MLX-Programmer for OTPs

Figure 1



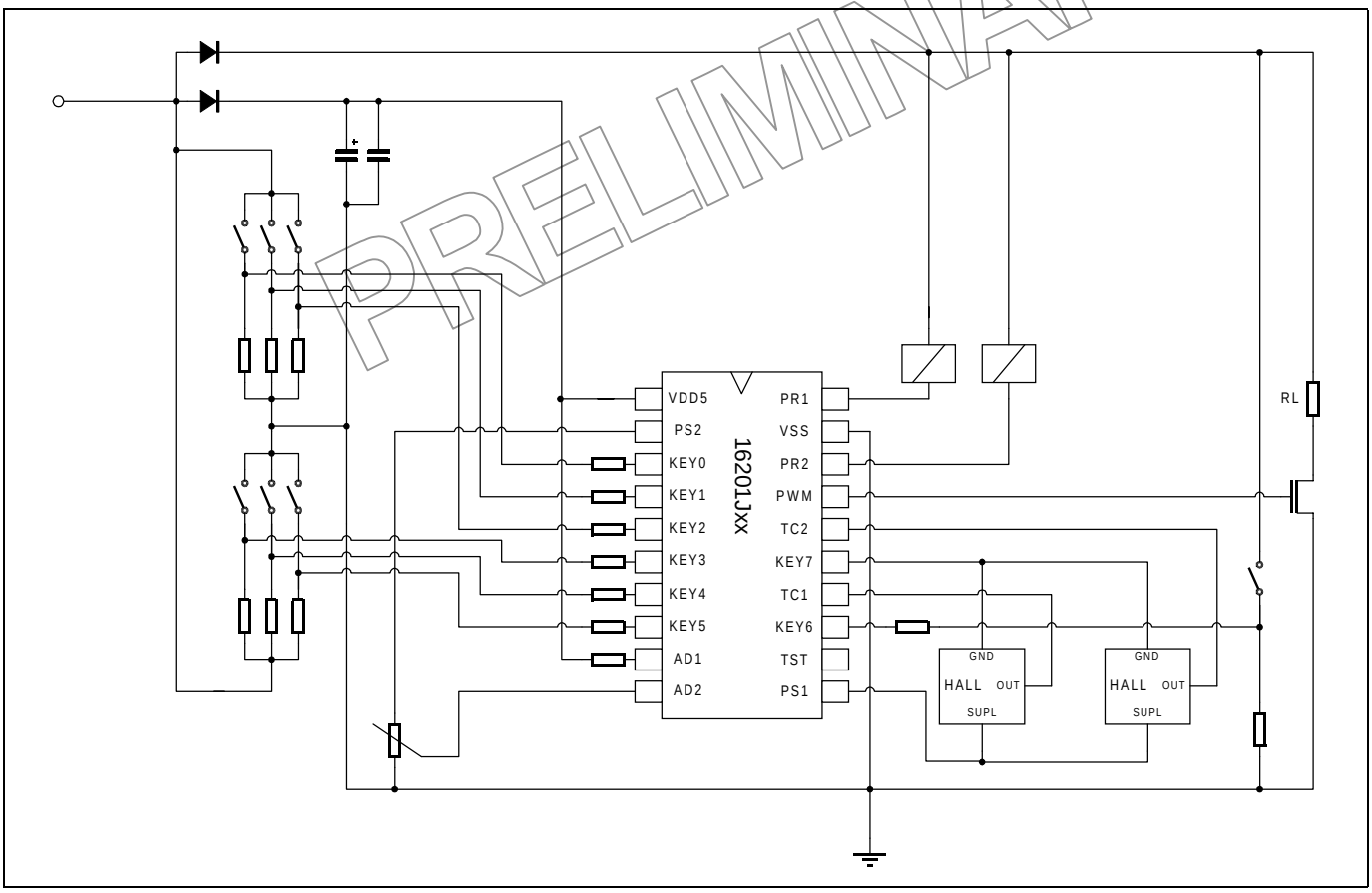
The 16201-Jxx is a multiple purpose intelligent relay driver ASIC designed for automotive applications. It uses the RX16000-16 Bit parallel µC of Melexis.
A lot of integrated analogue and digital features allow to design different automotive applications using only a few external components.
10 different interrupts allow to act on real time events, 4 interrupts are accessible via the pins.
The circuit is load dump protected for a 80V load dump pulse.
Due to License agreements with Melexis customers, the 16201Jxx is not free to use in electronic window lifter applications.

2. Table of contents

3. Typical Application

Figure 2 shows a typical application.

Figure 2



4. Device coding encryption

The coding of the device is encrypted in the following way:

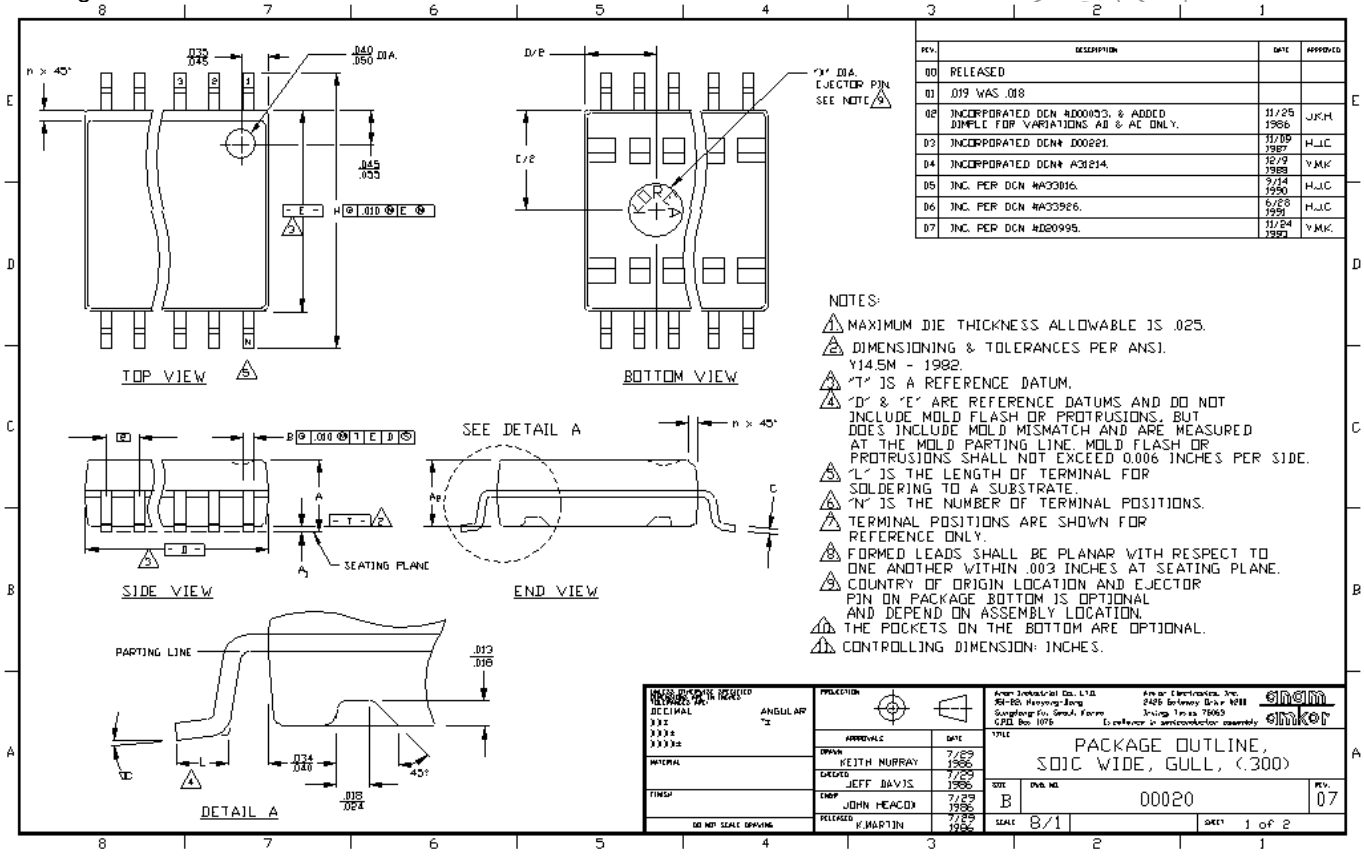
16202Jxx

with:

16201:	Chip name
J:	Hardware version, Melexis counts this letter up, in case of a major change in the chip design
xx:	Internal SW- (ROM-) version, encryption is linked to a given application and to a given customer

5. Mechanical data

Package: P-DSO20 in accordance to the JEDEC MS-013.



THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	NOM.	MAX.	N
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
ɸ	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	NOM.	MAX.	N
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
ɸ	0°	5°	8°						
X	2.16	2.36	2.54						

SIZE	DWG. NO.	REV.
B	00020	07
SCALE		SHEET 2 of 2

6. Pinout: SO20 package

Pin	Name	Function
Pin 1	VDD5	• Supply voltage pin • Connected to 3V-Reset (WBB) • Connected to Power On Reset (CBB) • Connected to Load Dump Interrupt
Pin 2	PS2	• 5V-supply output for external components, together with software short circuit protected • ADC-input with 6V-range for diagnosis • External ADC-reference input • Digital input
Pin 3	KEY0	• Bi-directional port pin • Input function with different thresholds, debounced and undebounced available • Push pull output with 5V • Connected to key interrupt
Pin 4	KEY1	• Bi-directional port pin • Input function with different thresholds, debounced and undebounced available • Push pull output with 5V • Connected to key interrupt
Pin 5	KEY2	• Bi-directional port pin • Input function with different thresholds, debounced and undebounced available • Push pull output with 5V • Connected to key interrupt
Pin 6	KEY3	• Bi-directional port pin • Input function with different thresholds, debounced and not debounced available • Push pull output with 5V • Connected to key interrupt
Pin 7	KEY4	• Bi-directional port pin • Input function with different thresholds, debounced and not debounced available • Push pull output with 5V • Connected to key interrupt
Pin 8	KEY5	• Bi-directional port pin • Input function with different thresholds, debounced and not debounced available • Push pull output with 5V • Connected to key interrupt
Pin 9	AD1	• ADC-input with 22V range • Reference for all ratio-metric threshold levels of the KEY-inputs • Digital input • Connected to 7V-Interrupt
Pin 10	AD2	• ADC-input with 6V range • Digital input
Pin 11	PS1	• Supply output for external components, follows VDD5 but max. 23V, short circuit protected • ADC-input with 22V range for diagnosis • Digital input
Pin 12	TST	• Test pin, internally pulled down
Pin 13	KEY6	• Bi-directional port pin • Input function with different thresholds, debounced and undebounced available

		• Push pull output with 5V • Connected to key interrupt
Pin 14	TC1	• Digital input , internally pulled up to 5V • Capture interrupt
Pin 15	KEY7	• Bi-directional port pin • Input function with different thresholds, debounced and undebounced available • Open drain output • Connected to key interrupt
Pin 16	TC2	• Digital input, internally pulled up to 5V • Capture interrupt
Pin 17	PWM	• PWM 5V push pull output • Digital input
Pin 18	PR1	• Open drain relay driver output with free wheel function, together with software short circuit protected • ADC-input with 22V range for diagnosis
Pin 19	VSS	• Ground pin
Pin 20	PR2	• Open drain relay driver output with free wheel function, together with software short circuit protected • ADC-input with 22V range for diagnosis

7. Absolute maximum ratings

Parameter	Symbol	Condition	Min	Max	Unit
Power supply	VDD5	DC max. 0.5s		26 80	V V
Maximum input current in any pin	Iin		-10	10	mA
Maximum input voltage on any pin	Vin		-0.3	VDD5+0.3	V
Maximum input voltage on PS2, in case external input voltage is used	Vinps2			12	V
Maximum input voltage on PS1, in case external input voltage is used	Vinps1			12	V
Maximum input voltage on KEY[7:0], in case they are **not** protected with external 100k protection resistor	Vinkey			22	V
Maximum input voltage on AD1, in case it is **not** protected with external 50k protection resistor	Vinad1			22	V
Maximum input voltage on pins TC[2:1]	Vintc			18	V
Thermal resistance SO20 (Junction to Ambient)	Rtrj-a			86	K/W
Maximum junction temperature	Tjunc			150	ºC
Maximum junction temperature in case of EEPROM WRITE	Tjunc/EE			140	ºC
Maximum power dissipation SO20	Ptot	at 85 ºC		755	mW
Maximum storage temperature	Tstor		-55	155	ºC
Maximum soldering temperature (t=10s), the manufacturing requirements defined in the „General Specification for Semiconductor Devices“ of Bosch are met	Tsold			300	ºC

8. Electrical characteristics

Following characteristics are valid over the full temperature range of T = -40°C to +105°C and a supply range of 26V ≥ VDD5 > 5V unless otherwise noted.

With 5V ≥ VDD5 > v3vreset the controller works correctly, analogue parameters can not be guaranteed.
RAM content is guaranteed till vpor < VDD5.
If several pins are charged with transients above VDD5 and below VSS, the summary of all substrate currents of the influenced pins should not exceed 20mA for correct work of the device.

Parameter	Symbol	Conditions		Limits		Units
			Min	Typ	Max	
Global parameters						
Working current during 80V load dump	iddhvn	VDD5=80V, all pins are inputs		20	40	mA
Normal working current	iddn	VDD5=13V, all pins are inputs, trimmed PLL to 8MHz	1.5	4	8	mA
Sleep mode current	idds	VDD5=13V, all pins are inputs, trimmed main oscillator to 125kHz, T=25°C		150	200	µA
Sleep mode current	iddsht	VDD5=13V, all pins are inputs, trimmed main oscillator to 125kHz			300	µA
Frequencies						
Frequency of the trimmed main oscillator	fmain	main oscillator is trimmed	118.75	125	131.25	kHz
Frequency of the PLL	fpll	main oscillator is trimmed	7.6	8	8.4	MHz
Frequency of the PWM	fpwm	main oscillator is trimmed	19.76	20.8	21.84	kHz
ADC related parameters						
relative error of DAC	relerrdac		-1/2		+1/2	LSB
relative monotonic error of DAC and ADC	monerrdac		0		0	LSB
Accuracy of temperature measurement with internal sensor	terr	sensor is calibrated on edge temperatures	-10	0	+10	°C
Accuracy of ADC measurement on AD1 (22V range)	ad1err	V(AD1) max. 16.5V, ADC is trimmed on AD1, ADC correction factor at 4001h is used	-7	0	7	% of full range
Accuracy of ADC measurements on PS1, PR1, PR2, SUPPLY	adc22verr	V (channel) max. 16.5V, ADC is trimmed on PR1,	-10	0	10	% of full range

(22V range)		ADC correction factor at 4004h is used				
Accuracy of ADC measurements on PS2, AD2 (6V range)	adc6verr	V (channel) max. 4.5V, ADC is trimmed on AD2, correction factor at 4005h is used	-10	0	10	% of full range
Accuracy ratiometric measurement on AD2 in case external DAC reference on PS2 is used	ad2raterr		-5	0	5	% of fraction between PS2 and AD2
AD1 related parameters						
Input resistance on AD1	rinad1		0.85	2	4	MΩ
Digital input threshold level H => L	vipnomlad1	VDD5>7V	0.75	1	1.25	V
Digital input threshold level L => H	vipnomhad1	VDD5>7V	3.75	4	4.25	V
Hysteresis	vhystnomad1	VDD5>7V	2.5	3	3.5	V
AD2 related parameters						
Leakage current in AD2	ileakad2				2	µA
Digital input threshold level H => L	vipnomlad2	VDD5>7V	0.75	1	1.25	V
Digital input threshold level L =>H	vipnomhad2	VDD5>7V	3.75	4	4.25	V
Hysteresis	vhystnomad2	VDD5>7V	2.5	3	3.5	V
PS2 related parameters						
Voltage on PS2 in case of short circuit (short circuit protection)	vps2sh	PS2 loaded with 100mA, tmax=10ms			1	V
Input resistance on PS2	rinps2		30	150	450	kΩ
Output voltage on PS2	vps2h	VDD5>7V, PS2 loaded with 5mA	3.2	5	5.5	V
Digital input threshold level H => L	vipnomlps2	VDD5>7V	0.75	1	1.25	V
Digital input threshold level L => H	vipnomhps2	VDD5>7V	3.75	4	4.25	V
Hysteresis	vhystnomps2	VDD5>7V	2.5	3	3.5	V
Maximum analogue input voltage for external ADC reference	viadcref				6	V
PS1 related parameters						
Short circuit protection on PS1	ips1prot		100		200	mA
Input resistance on PS1	rinps1		183	550	1650	kΩ
Maximum output voltage on PS1	vps1h	VDD5=26V	13		23	V
Maximum voltage drop on PS1 seen to VDD5	vdiffps1	13V>VDD5>5V PS1 loaded with 20mA			800	mV
Digital input threshold	vipnomlps1	VDD5>7V	0.75	1	1.25	V

level H => L						
Digital input threshold level L => H	vipnomhps1	VDD5>7V	3.75	4	4.25	V
Hysteresis	vhystnomps1	VDD5>7V	2.5	3	3.5	V
TST related parameters						
Pull down resistance on TST	rtst		0.5	1	2.5	kΩ
TC[2:1] related parameters						
Output voltage of TC[2:1]	vtc[2:1]	VDD5>7V	4.2	5	7	V
Pull up current of TC[2:1]	itc[2:1]	VDD5>7V TC[2:1] connected to VSS	1.0	2.5	4.3	mA
Digital input threshold level H => L	vipnomltc[2:1]	VDD5>7V	0.75	1	1.25	V
Digital input threshold level L => H	vipnomhtc[2:1]	VDD5>7V	3.75	4	4.25	V
Hysteresis	vhystnomtc[2:1]	VDD5>7V	2.5	3	3.5	V
PWM related parameters						
Leakage current in PWM in case PWM is as input	ileakpwm				2	µA
Voltage on PWM in case of H output	vhpwm	VDD5>7V PWM loaded with 5mA	4	5.0	6.5	V
Voltage on PWM in case of L output	vlpwm	VDD5>7V, PWM loaded with 5mA			0.5	V
Digital input threshold level H => L	vipnomlpwm	VDD5>7V	0.75	1	1.25	V
Digital input threshold level L => H	vipnomhpwm	VDD5>7V	3.75	4	4.25	V
Hysteresis	vhystnompwm	VDD5>7V	2.5	3	3.5	V
KEY[7:0] related parameters						
Leakage current in case KEY[7:0] are inputs	ileakkey[7:0]				2	µA
Voltage in case of H output	vhkey[6:0]	VDD5>7V, KEY[6:0] loaded with 1mA	4	5.0	5.5	V
Voltage in case of L output	vlkey[7:0]	VDD5>7V, KEY[6:0] loaded with 1mA, KEY7 loaded with 20mA,			0.5	V
Nominal input threshold level H => L	vipnomlkey[7:0]	VDD5>7V	0.75	1	1.25	V
Nominal input threshold level L => H	vipnomhkey[7:0]	VDD5>7V	3.75	4	4.25	V
Nominal hysteresis	vhystnomkey[7:0]	VDD5>7V	2.5	3	3.5	V
Special threshold level H => L in case of external pull down	vippdlkey[7:0]	V(AD1)<18V	0.5* V(AD1)	0.63* V(AD1)	0.8* V(AD1)	V
Special threshold level	vippdhkey[7:0]	V(AD1)<18V	0.5*	0.66*	0.8*	V

L => H in case of external pull down			V(AD1)	V(AD1)	V(AD1)	
Special hysteresis in case of external pull down	vhystsppdkey[7:0]	V(AD1)<18V	0.01* V(AD1)	0.03* V(AD1)	0.06* V(AD1)	V
Special threshold level H => L in case of external pull up	vippulkey[7:0]	V(AD1)<18V	0.2* V(AD1)	0.37* V(AD1)	0.5* V(AD1)	V
Special threshold level L => H in case of external pull up	vippuhkey[7:0]	V(AD1)<18V	0.2* V(AD1)	0.4* V(AD1)	0.5* V(AD1)	V
Special hysteresis in case of external pull up	vhystsppukey[7:0]	V(AD1)<18V	0.01* V(AD1)	0.03* V(AD1)	0.06* V(AD1)	V
7V-interrupt related parameters						
7V-interrupt level 1	7vint1		5.0		7.275	V
7V-interrupt level 2	7vint2		4.9		7.15	V
7V-interrupt level 3	7vint3		4.8		7.025	V
7V-interrupt level 4	7vint4		4.7		6.9	V
7V-interrupt level 5	7vint5		4.6		6.775	V
7V-interrupt level 6	7vint6		4.5		6.65	V
7V-interrupt level 7	7vint7		4.4		6.625	V
7V-interrupt level 8	7vint8		4.3		6.4	V
Hysteresis level for 7V-interrupt	v7vhyst		7.3V		7.9V	V
RESET related parameters						
Power on reset level (CBB)	vpor		1.5	2.0	3	V
3V-reset level (WBB), if VDD5 is ramped up	v3vupreset		3.0	3.5	4.2	V
Hysteresis on 3V-reset	v3vhyst		0.2	0.5	1.2	V
Load-dump-interrupt related parameters						
Level for load dump interrupt	vldi		27		40	V
PR[2:1] related parameters						
Input leakage of PR[2:1] in case of sleep	ileakpr[2:1]				2	µA
On resistance of PR[2:1]	rdson[2:1]	VDD5>7V			8 13(tmax)	Ω Ω
Free wheel diode voltage	vwheel[2:1]		24		31	V
Short circuit current in PR[2:1]	ish[2:1]	VPR[2:1]=3V, tmax=10ms	200 180 (tmax)		500 650	mA mA

9. Eeprom characteristics

Temperature	Warranty
Max. cycles	
25°C	100,000
105°C	10,000
Data retention	
25°C	20 years
55°C	20 years
85°C	10 years
125°C	1 year

10. Quality and Reliability targets

Melexis is following the „General Specification for Semiconductor Devices“ by BOSCH.
According to that requirements Melexis aims:

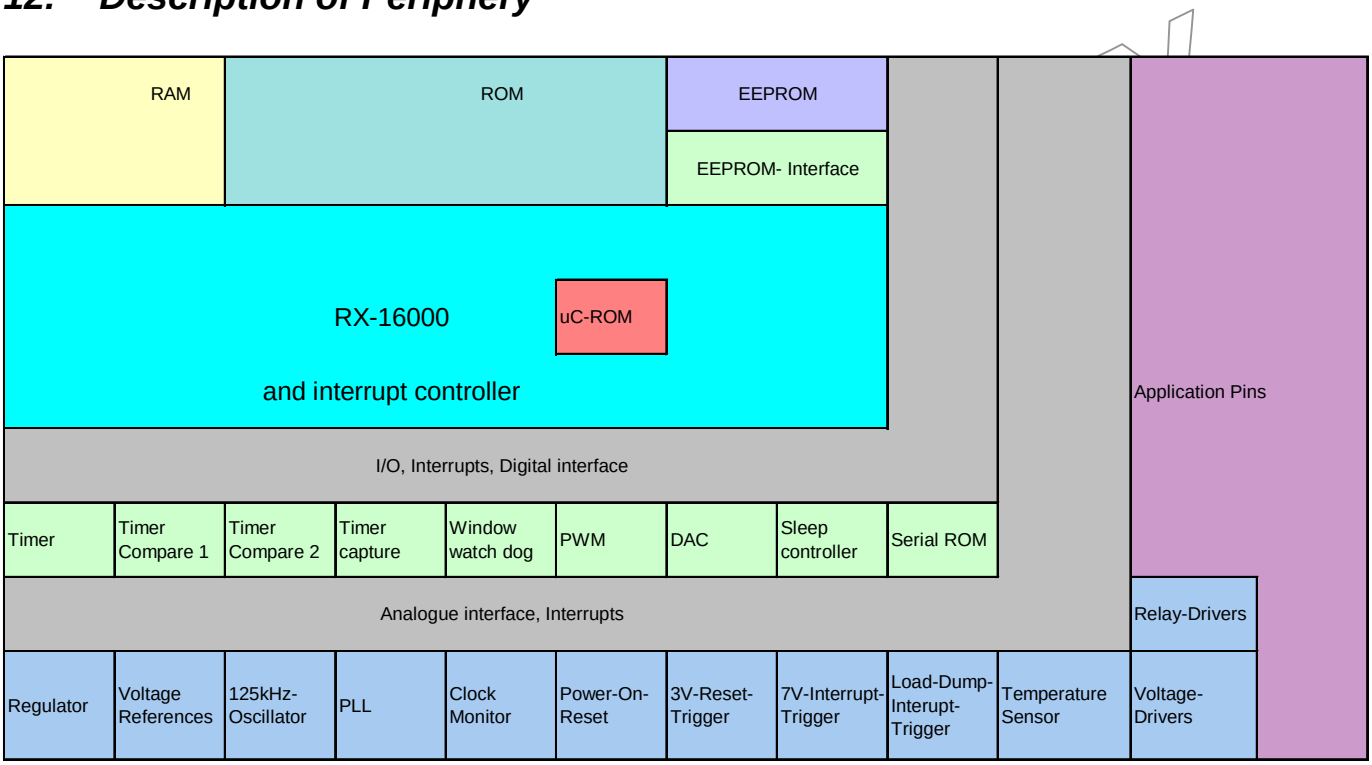
- Incoming quality: 0 failures
- Field failures during the first warranty year <1ppm

In order to reach these values, sensitive data has to be stored twice in the EEPROM with a CRC on each data field. Software algorithms have to handle this, possible failure routines should correct and act on single bit failures.

11. CPU-core description

16201J is designed with the Melexis 16-Bit-Risk-CPU.
CPU architecture, instruction set, register set, dressing modes are described in the „16 Bits RISC RX16000 DATA BOOK“ of Melexis. It will not be scope of this document.

12. Description of Periphery



12.1. Memory mapping

Internal ROM use 16201J	Adress
RAM (256 bytes)	start 0000
	stop 00FF
Unused	start 0100
	stop 0FFF
EEPROM (128 words)	start 1000
	stop 10FF
Unused	start 1100
	stop 1FFF
I/O	start 2000
	stop 201F
Unused	start 2020
	stop 3BFF
MLX-ROM (1 kbytes)	start 3C00
	stop 3FFF
MLX-Serial ROM (16 kbytes)	start 4000
	stop 7FFF
Unused	start 8000
	stop DFFF
ROM (8 kbytes)	start E000
	stop FFFF

12.2. ROM

12.2.1.ROM-allocation table and Far-Pages

Internal ROM 16201J	Adress	Far Pages	Adress
User Area	start E000	Far Page 0	start 3F00
	stop FFAF		stop 3FFF
User Interrupts	start FFB0	Far Page 1	start 7F00
	stop FFFF		stop 7FFF
		Far Page 2	start BF00
			stop BFFF
		Far Page 3	start FF00
			stop FFFF

12.2.2.Interrupt vectors and Interrupt description

Interrupt Function	Id	Soft Priority	Hard Priority(1)	Type	Active	Clear Pendings (3)	Reset Priority	Can be disabled	Far Page	Address(LSB)	Absolute address	Test Tracking	Segement Area (bytes)	Segement Usage (bytes)	Comments
Elex Test Reset	0	0	0	Jump	Level	Yes	Yes		0	F8	3FF8	No	4	4	
Elex Test Interrupt	1	0	1	Call	Edge				0	F0	3FF0	-	8	6	Default
									1	F0	7FF0	-	16	6	Upon request
Unused	2	0	2	Jump	Level	Yes	Yes		0	FC	3FFC	No	4	4	OTP/PROM Loader
User Reset	3	0	3	Jump	Level	Yes	Yes		3	F8	FFF8	N.A(4)	6	4	(9)
Watch-Dog Reset	4	0	4	Call	Edge	Yes	(2)		3	F0	FFF0	Yes	8	6	(10)
Program Error	5	0	5	Call	Edge				3	FE	FFFE	Yes	2	2	Also Software crash (6)
Eeprom Error	6	1	1	Call	Edge				3	A0	FFA0	Yes	8	0	Space can be re-allocated (6)
Ready Time-out	7	1	0	Call	Edge				3	A8	FFA8	Yes	8	0	Space can be re-allocated(6)
Load Dump	8	2	0	Call	Edge			Yes	3	B0	FFB0	Yes	8	6	
7V Threshold	9	2	1	Call	Edge			Yes	3	B8	FFB8	Yes	8	6	(7)
Timer Compare 1	10	3	0	Call	Edge			Yes	3	C0	FFC0	Yes	8	6	
Timer Compare 2	11	3	1	Call	Edge			Yes	3	C8	FFC8	Yes	8	6	
Timer Capture	12	3	2	Call	Edge			Yes	3	D0	FFD0	Yes	8	6	
Timer Overflow	13	3	3	Call	Edge			Yes	3	D8	FFD8	Yes	8	6	
Eeprom Ready	14	4	-	Call	Edge			Yes	3	E0	FFE0	Yes	8	6	
Key Input	15	5	-	Call	Edge			(5)	3	E8	FFE8	Yes	8	6	(8)
						Total user Interrupt area (bytes) :						96			
						Minimum user Interrupt area (bytes) :						80			
						Used interrupt area (bytes) :							60		

Far Pages	
Id	Page
3	FF
2	BF
1	7F
0	3F

Notes:

(1) : Conflict resolver
(2) : Should be done by software if necessary
(3) : Clears all other pending interrupts excepted Melexis Test Interrupt (Test mode)
(4) : Not Available :
(5) : Disable only possible in test mode
(6) : Not used
(7) : 7V Treshold Interrupt occurs, if selected level is reached, a new interrupt can occur, if V(AD1)>v7vhyst
(8) : Debounced with 1ms…2ms
(9) : CBB (Power on Reset) and WBB (3V-Reset) have to be detected via flags
(10) : Watch dog Interrupt can have the watch dog or the clock monitor as source, identification via flags

Interrupts can be enabled or disabled by Flags, or changing priority. In case priority 0 is selected, only interrupts with that priority will occur. Changing the priority to a value of N enables all interrupts with a priority <= N, in case they are enabled with their enable flag.
The Key Interrupt can only be enabled/disabled with a change in the priority in user mode.

Attention:

1.)
In case interrupts are:
- enabled with the enable flag
- disabled by priority
the interrupt sources are still active! An interrupt is memorised only one time, and it will be performed, when CPU runs on a priority again, which enables this interrupt. This is also valid for the sleep mode.

2.)
In case CPU is in an interrupt routine and a second enabled interrupt with a higher priority occurs, CPU jumps to this new interrupt, performs the routine and jumps back to the 1st interrupt.
Conflict resolver determines, what interrupt is performed at first, in case two interrupts with the same priority levels arrive at the same time.

3.)
If the chip is in sleep, all interrupts can wake up the chip, in case they are enabled.

4.)
In order to give Melexis the possibility to test the User Reset, the user software should have the following sequence:

```
SEGMENT  'Io'
.pb
.pb_l           DS.B
.pb_h           DS.B

#define         OIB_P_B7        io:pb_l.7
#define         O_P_B7          io:pb_h.7

.RESET          clrb    O_P_B7          ;gives "0" on KEY7 out
                setb    OIB_P_B7        ;in order to indicate Melexis-Tester the user-reset
                mov     cx,#0ah
res1            djnz    cx,res1
                clrb    OIB_P_B7
```

This sequence generates for 10us a logic L on KEY7, which is used by Melexis for testing the user reset.
All other interrupts are tested by means of the Melexis test interrupt.

5.)
In order to give Melexis the possibility to test the user interrupts, the user software should have the following sequence:

```
SEGMENT 'TimerComp1'
psp msw,2
nop
jumpf ITC1
```

12.3. Portsmap description

The ports map consists of an input and an output section which are separated.
On one and the same address can be completely different devices, they are accessed and selected by reading and writing to that certain address.

Outputs

Byte Address	Access mode(0)	Word Bit	Byte Bit	Name	Reseted by	Function: Bit cleared	Function: Bit set			
2000	WBb	0	0							
		1	1							
		2	2	OIB_PWM	CBB, WBB	Pin PWM is a digital input	Pin PWM is the PWM output			
		3	3							
		4	4							
		5	5	OIB_PS1	CBB, WBB, High current	PS1 pin is input of port 01 bit 5 PS1 pin is ADC input (channel 4)	PS1 pin outputs PS1 voltage			
		6	6	OIB_PS2	CBB, WBB	PS2 pin is input of port 01 bit 6 PS2 pin is ADC input (channel 5)	PS2 pin outputs PS2 voltage			
		7	7							
2001	Bb	8	0	N0	CBB, WBB, EE access	00	01	10	11	Bank
		9	1	N1	CBB, WBB, EE access	Protected	Protected	Protected	Opened	00-3F
		10	2			Protected	Protected	Opened	Opened	40-7F
		11	3			Protected	Opened	Opened	Opened	80-BF
		12	4			Opened	Opened	Opened	Opened	C0-FF
		13-15	5-7							

Notes : (0) Access modes

Symbol	Meaning
W	Word accessible
B	Byte accessible
b	Bit accessible
Na	Not Accessible
Nu	Not Used

Outputs

Byte Address	Access mode	Word Bit	Byte Bit	Name	Reseted by	Function: Bit cleared	Function: Bit set	
2002	WBb	0	0	O_PR1	CBB, WBB	Relay 1 is OFF	Relay 1 is ON	
		1	1	O_PR2	CBB, WBB	Relay 2 is OFF	Relay 2 is ON	
		2	2					
		3	3	CONTRV0	CBB	DAC voltage control		
		4	4	CONTRV1	CBB	000	5.4V	
		5	5	CONTRV2	CBB	111	7.0V	
		6	6	CKTEST	CBB	Software Test Clock		(1)
		7	7	DRTEST	CBB	Timing Test Data or Reset		(1)
2003	Bb	8	0	ENTCMPI1	CBB	Disable Timer compare 1 interrupt	Enable timer compare 1 interrupt	
		9	1	ENTCMPI2	CBB	Disable Timer compare 2 interrupt	Enable Timer compare 2 interrupt	
		10	2	ENEDGEI	CBB	Disable Edge detect interrupt	Enable Edge detect interrupt	
		11	3	ENOVFLI	CBB	Disable Counter overflow interrupt	Enable Counter overflow interrupt	
		12	4	ENLDI	CBB	Disable Load-dump interrupt	Enable Load-dump interrupt	
		13	5	EN7VI	CBB	Disable 7V detection interrupt	Enable 7V detection interrupt	
		14	6	ENEEI	CBB	Disable Eeprom Write end interrupt	Enable Eeprom Write end interrupt	
		15	7					
2004	WBb	0-7	0-7	OIB_P_B[7:0]	CBB	Pins KEY[7:0] (port B) are inputs	Pins KEY[7:0] (port B) are outputs	
2005	Bb	8-15	0-7	O_P_B[7:0]	None	Pins KEY[7:0] are port B data outputs		
2006	W	0-7	0-7	NO_SPB_P_B[7:0]	CBB	Special Threshold for Port B inputs	Normal Threshold for Port B inputs	
2007	Na	8-15	0-7	UDB_P_B[7:0]	CBB	Port B uses external pull-downs	Port B uses external pull-ups	

Notes: (1) Only in test mode

Outputs

Byte Address	Access mode	Word Bit	Byte Bit	Name	Reseted by	Function: Bit cleared	Function: Bit set	
2008	WBb	0	0	SOC	CBB, Conversion started	Idle ADC	Start ADC conversion request	
		1	1	SEL2VREFB	CBB	ADC uses internal Ref	ADC uses External Ref (From PS2)	
		2	2	SEL_ADC0	CBB	Analog MUX for ADC		
		3	3	SEL_ADC1	CBB	000 : Internal power supply	100 : PS1	
		4	4	SEL_ADC2	CBB	001 : Temperature sensor	101 : PS2	
						010 : AD1	110 : PR1	
						011 : AD2	111 : PR2	
		5	5	AWD	CBB, WBB	A rising edge on AWD will acknowledge watch-dog if WDSETF is high		
		6	6	R_CBFB	CBB	A rising edge sets CBFB flag		
		7	7	R_WBFB	CBB, WBB	A rising edge sets WBFB flag		
2009	Bb	8	0	EDSEL	CBB	Falling edge selection for capture	Rising edge selection for capture	
		9	1	TC1CPTDIR	CBB	TC1 xor TC2 input for capture	Direct TC1 input for capture	
		10	2	ENCM	CBB	Disable Clock monitor control	Enable Clock monitor control	
							TP1=0 (4) / -	TP1=1 (4) / Clock monitor reset
		11	3	EBE	CBB	Eeprom block erase disabled	Eeprom block erase enabled	(4)
		12	4	EBW	CBB	Eeprom block write disabled	Eeprom block write enabled	(4)
		13	5	VEE1	CBB	00	01 / 10 / 11	(4)
		14	6	VEE2	CBB	Read at predifined Internal normal level	Read at predifined Internal low level / Read with external Vs and Vcg levels on KEY2, KEY6 / Read at predifined Intenal high level	(4)
		15	7					
200A-200B	W	0-15	-	TCMPXP[15:0]	None	Timer Compare 1 reference value		
200C-200D	W	0-15	-	TCMPYP[15:0]	None	Timer Compare 2 reference value		
200E	B	0-6	0-6	OCONTR[6:0]	CBB	Oscillator control register		
		7	7					
200F	B	8-15	0-7	PWM[7:0]	None	For PWM from 0 to 127, duty cylce is PWM/128, then duty cycle is 1		

Outputs

Byte Address	Access mode	Word Bit	Byte Bit	Name	Reseted by	Function: Bit cleared	Function: Bit set	
2010	WB	0	0	DIV0	CBB	Free running counter in normal mode	Free running counter in SLEEP mode	
						0 / 1	0 / 1	
						1 MHz / 250KHz	15.62Khz / 7.813Khz	
	Nu	1-7	1-7					
2011	Nu	8-15	0-7					
2012	WB	0	0	TP1	CBB	00 / 01 / 10 / 11		(4)
		1	1	TP2	CBB	Normal mode: 01 = 125Khz on KEY3 8Mhz PLL on KEY4; 10 = DAC ref on KEY3; 11 = 7V interrupt voltage (5)		(4)
						Normal mode: 01 = SEL_ADC=xx0 =>VDD1 on ADC; 10 = DAC output on KEY4; 11 = Bandgap voltage on KEY4		
						Normal mode: 01 = SEL_ADC=xx1 =>VDD2 on ADC; 10 = ADC input voltage on KEY5 (6)		
		2	2	TP3	CBB	Normal mode	Power down disabled	(4)
		3	3	IDDTEST	CBB	Normal mode	Enable IDDQ acquisition	(4)
							I_AD2=0 Normal / I_AD2=1 Memories in precharge IDDQ acquisition	
							TP3=0 Normal internal supply (Typicaly 5V) / TP3=1 High internal supply (Typicaly 7V)	
		4	4	TMTEST	CBB,TEST	Timing tests disabled	Timing tests enabled	(3, 4)
		5	5	ELEXITPG1	CBB,TEST	Elex Interrupt in FP0	Elex Interrupt in FP1	(4)
		6	6	ENKEYITB	CBB,TEST	Key interrupts enabled	Key interrupts disabled	(4)
		7	7	ABORTBUSY	CBB,TEST	Normal mode	Abort Busy Eeprom	(4)

Notes :
(3) Timing Devices are : Free-running counter, Timer Compare 1 and 2, Timer Capture and PWM
(4) Melexis reserved for test purpose, only accessible in test mode
(5) Negative input of the comparator
(6) Positive input of the comparator

Inputs

Byte Address	Access mode	Word Bit	Byte Bit	Name	Reseted by	Function: Bit cleared	Function: Bit set	
2000	WBb	0	0	EQUAL1	Not applicable	Timer Compare1 equality not found	Timer Compare1 equality found	(6.1)
		1	1	EQUAL2	Not applicable	Timer Compare2 equality not found	Timer Compare2 equality found	(6.1)
		2	2	DET	Not applicable	Capure not done	Capture done	(6.1)
		3	3	OVF	Not applicable	No timer overflow	Timer overflow	(6.1)
		4	4	7VTHRESHOLD	Not applicable	7V threshold not found	7V threshold found	(6.1),(7)
		5	5	LDTHRESHOLD	Not applicable	Load Dump threshold not found	Load Dump threshold found	(6.1),(7)
		6	6	KEYPRESSED	Not applicable	No key is pressed	One or more keys are pressed	(6.1),(8)
		7	7	O_PWM	Not applicable	PWM output is LOW	PWM output is HIGH	(6.1),(9)
2001	Bb	8	0	I_TC1	Not applicable	Data on TC1 pin		
		9	1	I_TC2	Not applicable	Data on TC2 pin		
		10	2	I_PWM	Not applicable	PWM output used as digital input (if OIB_PWM is cleared)		
		11	3	I_AD1	Not applicable	Data from external pin AD1		
		12	4	I_AD2	Not applicable	Data from external pin AD2		
		13	5	I_PS1	Not applicable	Data from external pin PS1		
		14	6	I_PS2	Not applicable	Data from external pin PS2		
		15	7					
2002	WBb	0-7	0-7	ADC[7:0]	Not applicable	ADC inputs		
2003	Bb	8	0					
		9	1					
		10	2					
		11	3					
		12	4	LDIF	CBB, Read of port 2003	Load-dump memory		
		13	5	7VIF	CBB, Read of port 2003	7V threshold memory		
		14	6	COMPOUTB	Not applicable	ADC Comparator output (Inverted)		
		15	7	CMRES	CBB, Read of port 2003	Clock monitor error detection (Valid even if ENCM flag is low)		
2004	WBb	0-7	0-7	I_P_B[7:0]	Not applicable	Undebounced Port B inputs		
2005	Bb	8-15	0-7	I_P_DB_B[7:0]	Not applicable	2ms…3ms debounced Port B inputs		

(6.1) Only for Melexis test purposes

Notes :
(7) Undebounced input
(8) Debounced input
(9) Same as I_PWM

Inputs

Byte Address	Access mode	Word Bit	Byte Bit	Name	Reseted by	Function: Bit cleared	Function: Bit set	
2008	WBb	0	0	EOC	SOC	End Of Conversion : Set by ADC when conversion is completed		
		1	1	TEST1	Not applicable	00 : Normal mode	10 : Test mode 2, external oscillator	(6.1)
		2	2	TEST2	Not applicable	01 : Test mode 1, internal oscillator	11 : Do not exist	(6.1)
		3	3	EEBUSY	Not applicable	Eeprom not busy	Eeprom busy (write or erase)	
		4	4	CPTF	CBB, Read of Port 200A	Capture not done	Capture done	
		5	5	WDSETF	Automatic by watch-dog	Watch-dog window not opened	Watch-dog window opened	
		6	6	CBFB	Set by R_CBFB	A cold boot has occured	No reset occured	
		7	7	WBFB	Set by R_WBFB	A warm or a cold boot has occured	No reset occured	
2009	Bb	8	0	LDPI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
		9	1	7VPI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
		10	2	TCOMP1PI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
		11	3	TCOMP2PI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
		12	4	TCAPTPI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
		13	5	TOVFPI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
		14	6	EERDYPI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
		15	7	KEYPI	Not possible	No pending interrupt	Pending interrupt	(6.1),(10)
200A-200B	WBb	0-15	-	CPT[15:0]	None	Capture register		
200C-200D	WBb	0-15	-	CNT[15:0]	CBB	Free running counter		

Notes : (10) Taken from Interrupt Controller

12.4. Periphery access, Timing

Access time of periphery:

All devices addressable by the RX16000 are with a READY management. The CPU will wait, until an addressed periphery device will have valid data. Because timing of peripheral devices is dependent on temperature and supply, we can only give
the following typical access time (CPU at 8MHz):

RAM:	250ns	from address to data
ROM:	250ns	from address to data
I/O:	250ns	from address to data
EEPROM:	4us...6us	from address to data in case of READ
	4ms...5ms	from address to written data in case of WRITE
Instruction length:	1us	

Addressing modes of periphery

Memory read/write addressing modes for RX16000
NOTE that every address in the tables below is a byte address

Data in memory

Offset	Data
0	AA
1	BB
2	CC
3	DD
4	EE
5	FF

Result in register after MOV instruction

Word addressing modes

Offset	RAM	ROM (*)	I/O	EEPROM
0	AABB	AABB	AABB	AABB
1	BBCC	do not use	do not use	do not use
2	CCDD	CCDD	CCDD	CCDD
3	DDEE	do not use	do not use	do not use
4	EEFF	EEFF	EEFF	EEFF

Example:
RAM start address = 0000
mov a,dp:01
result : a = BBCC

Example:
R0M start address = E000
x = E002
mov a,[x]
result : a = CCDD

Byte addressing modes

Offset	RAM	ROM (*)	I/O	EEPROM
0	AA	AA	AA	do not use
1	BB	BB	BB	do not use
2	CC	CC	CC	do not use
3	DD	DD	DD	do not use
4	EE	EE	EE	do not use

Example:
RAM start address = 0000
mov al,dp:01
result : al = BB

Example:
R0M start address = E000
x = E003
mov al,[x]
result : al = DD

Bit addressing modes

Offset	RAM	ROM (*)	I/O	EEPROM
0	offset 0; bit 0	offset 0; bit 0	offset 0; bit 0	do not use
2	offset 0; bit 2	offset 0; bit 2	offset 0; bit 2	do not use
7	offset 0; bit 7	offset 0; bit 7	offset 0; bit 7	do not use
8	offset 1; bit 0	offset 1; bit 0	offset 1; bit 0	do not use
F	offset 1; bit 7	offset 1; bit 7	offset 1; bit 7	do not use
1F	offset 3; bit 7	offset 3; bit 7	offset 3; bit 7	do not use

Example :
RAM start address = 0000
Offset = 000A =(1010)b
Bit 2 of address 0001 is read

Example :
ROM start address = E000
Offset = 0019 =(00011001)b
Bit 1 of address E003 is read.

(*) - only read

Beside this:
- The limitations for bit addressing modes and additional addressing modes (i.g.:y:page), which are described in the „16 Bits RISC RX16000 DATA BOOK“ of Melexis are valid.
- For word, byte and bit addressing modes of I/O the spec. of 8.3 are valid.
- CPU can run code from ROM and RAM.

12.5. Description of important peripheral blocks

12.5.1.Eeprom interface

The EEPROM is controlled by an interface logic, which takes care about the following:

- Divides the EEPROM into 4 pages, which can be individually protected.
- Protects the 1st 4 words, with the trimming parameters against a write access.
- In case the EEPROM is busy with writing the CPU can perform code, the interface latches address and data and performs the write instruction.
- If a 2nd write cycle is started, while a 1st cycle is running, the 2nd cycle is discarded.

In case writing data to an certain address of the EEPROM, this address has to be erased before.
Erasing is done by writing 0000h to a certain address.
While a write instruction is running and a sleep command is performed from the CPU, the chip will wait, until the EEPROM write operation is finished. After that the chip will go in sleep mode.

12.5.2. Window Watch dog

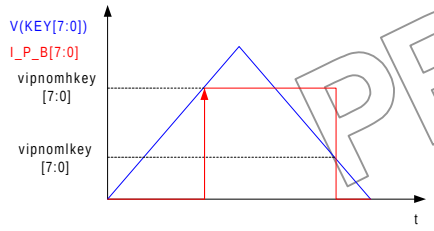
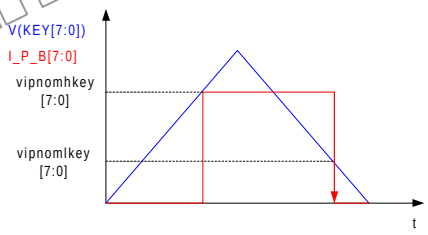
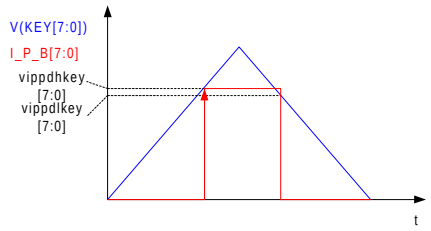
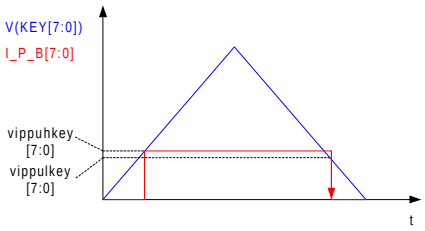
16201J uses a window watch dog.
In case CPU is running on 8MHz, the window opens 5ms after a reset of the watch dog timer (according 9.1.) and closes 10ms after a reset of the watch dog timer.
Resolution of that window is 8us, the watch dog has to be acknowledged in that window. Every acknowledge outside generates a watch dog interrupt.
The opened window is seen and the acknowledged is done via ports 8.3.

12.5.3.Clock monitor, oscillator concept

The main oscillator is a 125kHz RC oscillator which is trimmed via software.
This oscillator output is multiplied by 64 with a PLL so that a CPU clock of 8MHz can be derived.
The PLL has a settling time of ca. 240us after start up, in that phase and also during sleep the 125kHz is used as main clock for the complete system.
The PLL is observed by a clock monitor. If the PLL becomes unlocked over a time between 40us...160us, a clock monitor reset (9.1.) is performed, in case it is enabled. The clock monitor has a settling time of 240us after the PLL is settled.

Attention:
- Clock monitor should only be enabled by software, if the system is stable, means PLL is settled, clock monitor is settled (complete settling time 240us+240us)
- Clock monitor has to be disabled in sleep mode.

12.5.4.The configuration possibilities of the Key-Thresholds and the Key-Interrupt

- Port NO_SPB_P_B[7:0]=FFh - Port UDB_P_B[7:0]=00h - External pull down, KEY0 is high active - Key interrupt will be generated on a 1ms…2ms debounced L-H transient of I_P_B[7:0] - UDB_P_B[7:0] has no influence on the comperator digital input threshold level  The key interrupt is not defined during a change of UDB_P_B[7:0].	- Port NO_SPB_P_B[7:0]=FFh - Port UDB_P_B[7:0]=FFh - External pull up,KEY0 is low active - Key interrupt will be generated on a 1ms…2ms debounced H-L transient of I_P_B[7:0] - UDB_P_B[7:0] has no influence on the comperator digital input threshold level  The key interrupt is not defined during a change of UDB_P_B[7:0].
- Port NO_SPB_P_B[7:0]=00h - Port UDB_P_B[7:0]=00h - External pull down, KEY0 is high active - Key interrupt will be generated on a 1ms…2ms debounced L-H transient of I_P_B[7:0] - High ratiometric to V(AD1) input threshold level is used  The key interrupt is not defined during a change of UDB_P_B[7:0].	- Port NO_SPB_P_B[7:0]=00h - Port UDB_P_B[7:0]=FFh - External pull up, Key is low active - Key interrupt will be generated on a 1ms…2ms debounced H-L transient of I_P_B[7:0] - Low ratiometric to V(AD1) input threshold level is used  The key interrupt is not defined during a change of UDB_P_B[7:0].

13. Special conditions

13.1. Reset of the periphery

Source	Reset CPU	Reset Periphery	Reset watchdog timer	Note
Power On Reset	yes	yes	yes	CPU uses 125kHz for 240us, after Reset disappeared
3V-Reset	yes	according ports map description	yes	RAM contend can be guarantied
Watch-Dog-Interrupt	no	yes	yes	In case of Watch-Dog-Interrupt: • The watchdog has to be acknowledged 2 times until relay driver can be switched on. • The 3V-Reset level is switched to its hysteresis level
Clock-Monitor	no	yes	yes	CPU uses 125kHz for 240us, after Reset disappeared
Sleep	no	no, only components which consume current	yes	CPU uses 125kHz for 240us after CPU is waked up

13.2. Load dump protection

The 16201J is protected against 80V load dump. In case of Load-dump:
- Both relay drivers are switched on.
- The pin PWM is switched to H in case PWM is in output function.

13.3. Trimming

In the EEPROM there are the following parameters, when 16201J is delivered to the user:

EEPROM address	Contend	scope
1000h	Oscillator control word ocontrnom[6:0]	only accessible in test mode, trimmed values
1001h	ADC correction factor for AD1 eps(AD1)	
1002h	Temperature sensor tmin	
1003h	Temperature sensor tmax	
1004h	ADC correction factor for PR1, PR2, PS1, SUPPLY eps(PR1)	
1005h	ADC correction factor for AD2, PS2, eps(AD2)	
1006h	Identity	
1007h	Identity	

1008h	00	
1009h	00	
100Ah	00	
100Bh	00	
100Ch	Lotnumber	Security values, will not be overwritten by the user
100Dh	Lotnumber	
100Eh	Difference between nominal and trimmed frequency as signed BYTE freqdiff	
100Fh	Checksum for addresses 1000h...1007h as BYTE	
1010h... 10FFh	00 00	

Address 1000h to 1007h are write protected in normal user mode. The parameters should be used by the user software in order to trim 16201J.

EEPROM checksum calculation:

$$Checksum16 = \left(\sum_{l=1000h...1007h,\ 100Ch,\ 100Dh,\ 100Eh} EE[l] + EE(100Eh) \right) \bmod (2^{11})$$

Addresses 1000h...1007h, 100Ch, 100Dh, 100Eh are read and summed as unsigned BYTES and stored on 100Fh, overflow is thrown away

Trimming of the oscillator:

The data of address 1000h has to be written to the oscillator control register at 200Eh.
After that the main oscillator is running at 125kHz, the PLL is at 8MHz.

ADC correction:

The ADC is trimmed on channels
- AD1 at a voltage of vin=13V via 50k on the pin AD1,
- PR1 at a voltage of vin=13V on the pin PR1.
- AD2 at a voltage of vin=3V on the pin AD2.

These trimming factors should be used according the EEPROM allocation table of this chapter.

This trimming is used in order to get common mode errors out. The ADC correction values at address 1001h, 1004h, 1005h are calculated in the following way:

ADC correction factor eps:

-idea: calibration is on CHANNEL, measurement on CHANNEL gives one result called adce, which has an error.
In order to get the right value called adcr, the following equation has to be applied:

adcr=ratio*adce

-format: ADC correction factor eps=00h ratio=0.75
ADC correction factor eps=FFh ratio=1.25
between there is an linear interpolation

-measuring eps: select CHANNEL with internal reference and give the

ADC value adc2[7:0] out, measure V(CHANNEL) with the internal ADC,
following equation is valid with vin (trimming voltage from above), CHANNEL connected (in case CHANNEL=AD1 via 50k) to vin, range(AD1, PR1)=22V and range(AD2)=6V:

adcr=255*vin/range
ratio=adcr/adc2[7:0]
eps=hex(round[(ratio-0.75)*255/0.5]),

With this method the 3 ADC calibration factors are derived.

- back calculation: select ADC channel x, which as a range of rangex
with internal reference and give the ADC value adcx[7:0] out,

read eps from 1001h, 1004h or 1005h dependent on the selected channel x
ratio=0.5/255*[dez (eps)]+0.75
vadcx=adcx[7:0]*ratio*rangex/255

Temperature sensor:

The temperature sensor is calibrated on its edge temperatures -40°C and 105°C. These values are written into the EEPROM.
Between these temperatures there is an linear interpolation.

13.4. Short circuit protection on application pins

On the PS2, PR[2:1] pins we have a short circuit protection, which is realised together with software. During a certain time we allow a short circuit protection current, which is specified in 4.
These pins can be observed with via internal ADC-channels, if the voltage on these pins is out of range because of a short circuit, software has to switch off this driver.

The short circuit protection in PS1:

If the current exceeds on PS1 the maximum possible current specified in 4 during a time of 60us...120us, hardware switches this driver off. It is up to the user to observe this channel with the internal ADC or the digital input on PS1 in order to see this fault.
If driver was switched of du due a short circuit on that pin, software can switch it on again by setting OIB_PS1 to „1“.

14. Debugging facilities

Hardware and software debugging tools are available for the RX16000 family.
Debugging of 16201J should be done on the MLX standard product 10108xy.
The description of the available tool set is not a part of this document.

15. History record

Rev.	No.	Change	Date
1.0	1	Creation	03.01.99
1.1	1	Spec error in special threshold mode had been removed	12.12.99
1.2	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	Chapter: Table of content added Chapter: Mechanical package data added Chapter: Device coding encryption added Chapter: History record added Chapter: The configuration possibilities of the Key-Thresholds and the Key-Interrupt added Remark: Key interrupt is debounced with 1ms…2ms Remark: Debounced Key inputs are with 2ms…3ms debounced Maximum input voltage Vintc=18V on TC[2:1] added Links to other docs have been adjusted Typing mistakes have been removed iddn min, typ, max changed to smaller values ileakad2 max, ileakpwm max, ileakkey[7:0] max, ileakpr[2:1] max changed from 4uA to 2uA rinps2min changed from 50kOhm to 30kOhm vhpwm min, vhkey[6:0] min changed from 4.2V to 4V vlkey[7:0] max changed from 0.4V to 0.5V vpor max changed from 2.5V to 3V v3vupreset max changed from 4V to 4.2V v3vhyst changed from 1V to 1.2V vwheel[2:1] min (max) changed from 27V (36V) to 24V (31V) ish[2:1] max specified to 650mA	06.06.01
1.3	1 2 3	Reformating due to MLX standart for datasheets Exchange of the package drawings from scanned versions to digital pictured versions Remarks added in the portsmap for bits, which are only valid in Melexis test mode	26.06.01

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