

### **Features**

#### **CPU**

- MelexCM CPU (Dual RISC CPU – 5MIPS)
  - LIN protocol controller
  - 16-bit application CPU90
- Internal RC-Oscillator

#### **Memories**

- 2kbyte RAM, 30kbyte Flash, 128 byte EEPROM
- Flash for series production

#### **Periphery**

- Three 16-bit timer with capture and compare
- Full duplex SPI interface
- 100-kBaud UART
- 2 high and 2 low side FET driver with protection
  - Over temperature control
  - Short circuit protection
  - Current control
- 8-bit PWM control with programmable base frequency of 100Hz to 100kHz
- 8 high voltage I/Os
- 16-channel 10-bit ADC with high voltage option
- Independent analog watchdog
- Temperature sensor

#### **Voltage Regulator**

- Direct powered from 12V boardnet with low voltage detection
- Operating voltage  $V_S = 7.3V$  to 18V
- External Load transistor for higher 5V loads or higher ambient temperature possible
- Very low standby current, < 50 $\mu$ A in sleep mode

#### **Bus Interface**

- LIN transceiver
- Supporting of LIN 2.x and SAE J2602
- LIN protocol software provided by Melexis
- Wake up by LIN traffic or local sources

#### **Additional Features**

- On-chip CPU debugger
  - Jump start and 45V load dump protected
  - Available in two package variants QFN 6x6 40 and TQFP EP 48L
-

### Applications

LIN slaves for all kind of high current DC Motor with full bridge FET control like

- Wiper control
- Valve control
- Seat movement
- Pumps

### Ordering Information

Order Code	Temp. Range (K)	Package (LQ or PF)	Delivery Option (RE, TU, TR)
MLX81100KLQ - BAA - 000 - TU	- 40°C ... 125°C	QFN40 6x6	Tube
MLX81100KLQ - BAA - 000 - RE	- 40°C ... 125°C	QFN40 6x6	Reel
MLX81100KPF - BAA - 000 - TR	- 40°C ... 125°C	TQFP48 7x7 EP	Tray
MLX81100KPF - BAA - 000 - RE	- 40°C ... 125°C	TQFP48 7x7 EP	Reel

**Ordering example:**

**MLX81100KLQ-BAA-000-TU**

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## 1. Functional Diagram

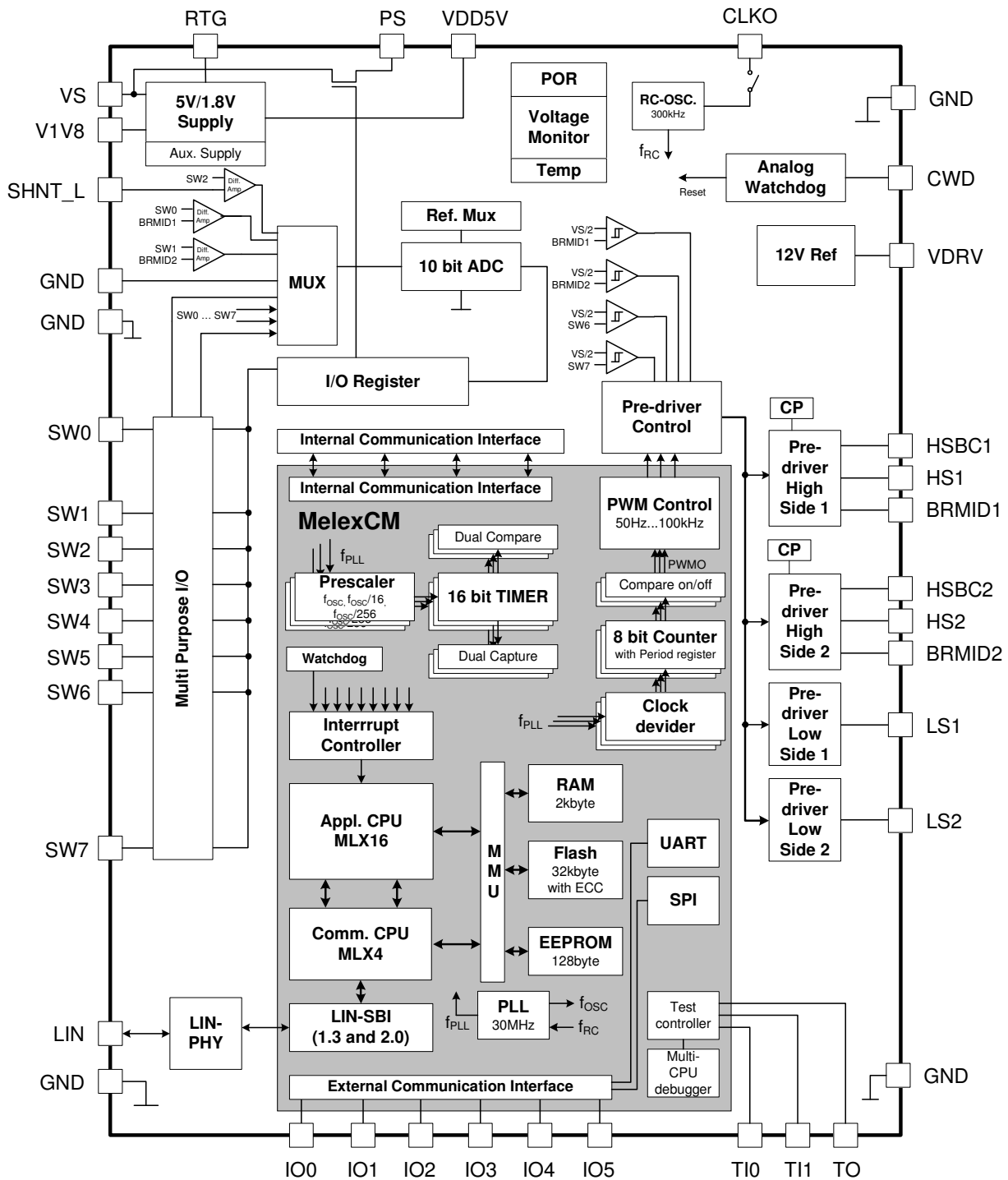


Figure 1- Block diagram

## 2. Electrical Characteristics

### 2.1 Operating Conditions

Following characteristic is valid over the temperature  $-40\text{deg C} < \text{TA} < 125\text{deg C}$  and supply voltage range of  $7.3 < \text{VS} < 18\text{V}$ , unless otherwise noted. With  $\text{VS} \leq \text{VS}_{\text{min}}$  but above reset state or inside a temperature range  $125\text{deg C} < \text{TA} < 150\text{deg C}$  the controller works correctly, analogue parameters can not be fully guaranteed. If several pins are charged with transients above VS and below VSS, the summary of all substrate currents of the influenced pins must not exceed 10mA for correct operation of the device. All voltages refer to ground of IC, which is built by short of all existing ground pins, which were split to meet EMC performance and lowest possible noise influence.

Parameter	Symbol	Condition/Remark	Limit			Unit
			Min	Typical	Max	
Supply Voltage Range	VS		7.3		18	V
Ambient Temperature	TA	see note (*) below	-40		125 (150*)	deg C
Operation current	I_VS	No DC-load on pins		15	30	mA
Stand by current	I_SBY	VS=13V, TA≤ 85deg VS=18V, TA≤ 85deg			50	uA
					120	uA
Max. voltage difference between SHNT_L and GND	SHNT_L	to be minimized for optimum ADC accuracy			400	mV

**Table 1 - Operating Conditions**

(\*) Target temperature after qualification: With temperature applications at  $\text{TA} > 125\text{deg C}$  a reduction of chip internal power dissipation with external supply transistor is obligatory. The extended temperature range is only allowed for a limited periods of time, customers mission profile has to be agreed by Melexis as an obligatory part of the Part Submission Warrant (PSW). Some analogue parameter will drift out of limits, but chip function can be guaranteed.

### 2.2 Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods will affect device reliability.

Parameter	Symbol	Condition	Limit		Unit
			Min	Max	
Battery supply voltage	VBAT	Before reverse polarity protection	-0.5	20	V
	VBAT	Load dump, t<500ms	-0.5	45	
	VBAT	Jump start, t< 2min <sup>[1]</sup>	-0.5	28	
Input Supply voltage	VS	After reverse polarity protection	-0.5	18	
Input voltage	VDD5V		-0.5	6.5	
Output voltage	V1V8		-0.5	2.2	
Output Voltage	RTG		-0.5	6.5	
SHUNT Measurement	SHNT_L		-0.5	VDD5V+0.5V	
Switch inputs	SW[7:0]		-0.5	VBAT	
LIN Bus	LIN	t<500ms	-24	VBAT	
Driver Voltage	VDRV		-0.5	VBAT	
Digital IO's	IO[5:0], TI[1:0], TO,CLKO		-0.5	VDD5V+0.5V	
Watchdog cap	CWD		-0.5	VDD5V+0.5V	
High side driver Bridge	HS1,HS2		-0.5	VBAT+ VDRV	
High side bridge cap	HSBC1,HSBC2		-0.5	VBAT+ VDRV	
Midpoints of bridge	BRMID1,BRMID2		-0.5	VBAT	
Low side driver Bridge	LS1,LS2		-0.5	VDRV	
Storage temperature	Tstg		-55	150	deg C
Junction Temperature	TJ	see text note (*) below	-40	150 (155*)	
Thermal resistance QFN40 6x6	Rth		40		K/W
Thermal resistance TQFP EP48L	Rth		40		

[1] Jumpstart Voltage: This operation condition needs careful handling of power dissipation by application software, to prevent chips overheating, see also Jumpstart interrupt description

**Table 2 - Absolute Maximum Ratings**

### 3. Application Circuitry

#### 3.1 Single DC-Motor Drive

In this sample application the IC can drive a DC motor via an external power N-FET's bridge. The high side N-FET drive is done by a bootstrap output stage. Current control of the motor is done via shunt measurement; the reverse polarity protection of the bridge has to be realized with an external power FET connected to the ground line. Short circuits of the bridge will be detected from fast comparators and in this case the bridge will be switched off. Weak short circuits should be monitored with the help of an external temperature sensor.

The actual position can be read with hall sensors, which are connected to the timer capture inputs. The hall sensors are switched off during standby mode via a switch-able battery voltage output PS. Optional it is possible to connect an external serial EEPROM via serial interface in case the usage of an integrated MEMORY is forbidden by safety reasons.

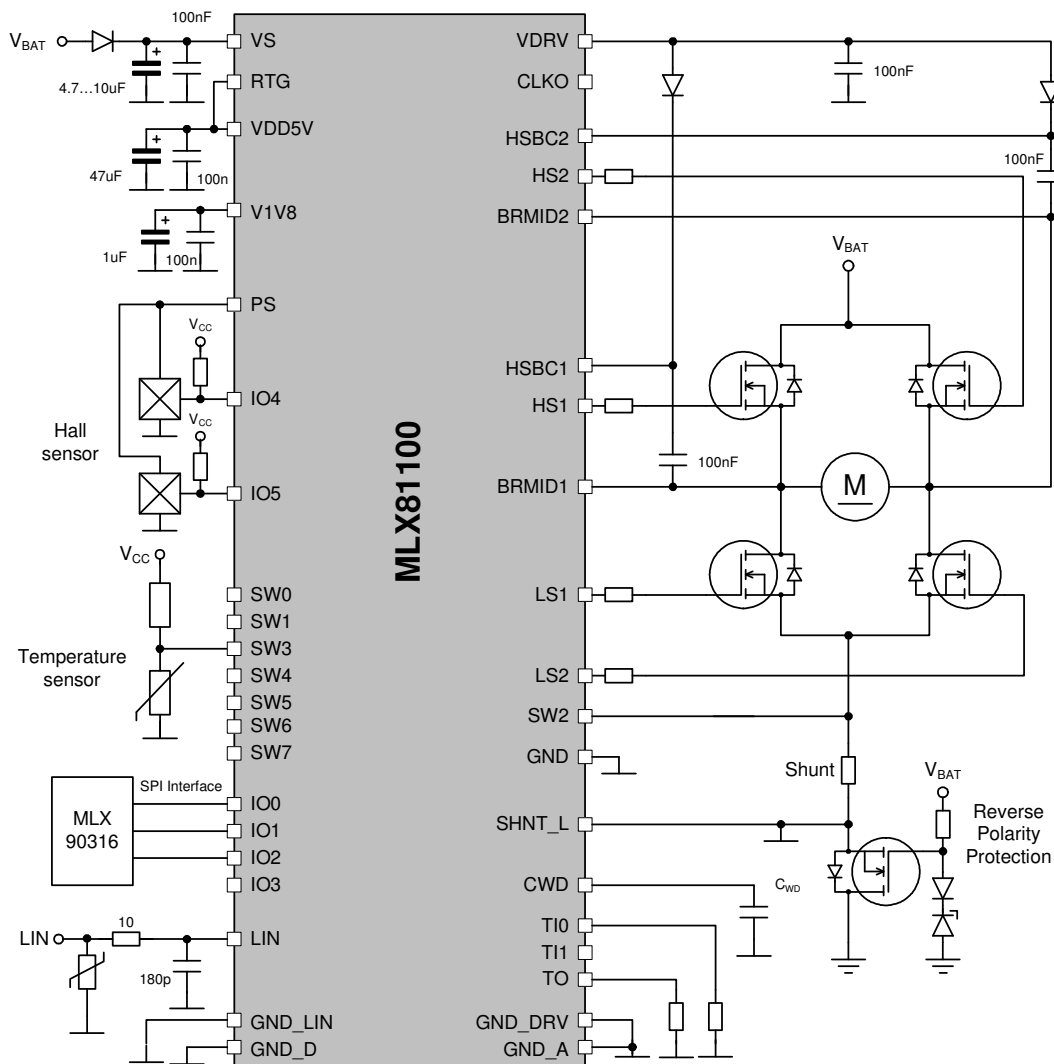


Figure 2 - Application circuitry for single DC-motor control

### 3.2 Higher VCC Loads and higher Ambient Temperatures

For higher power consumption caused by higher VBAT or higher ambient temperatures, an external regulator transistor can bring the main power consumption which is caused by regulator, outside of the MLX81100 - so maximum chip temperature can be decreased to meet application needs.

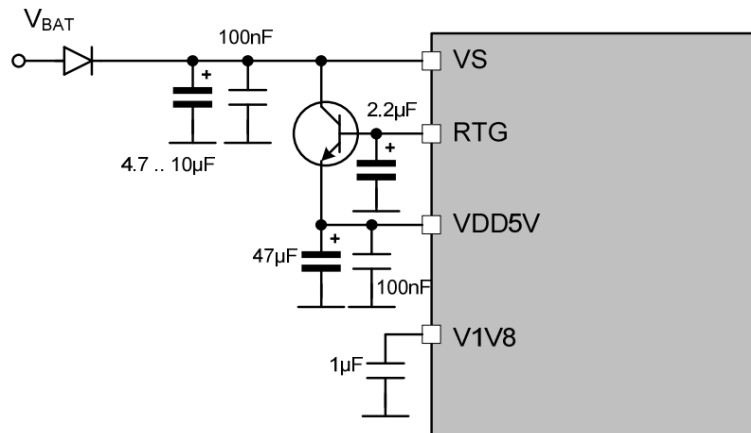


Figure 3 - Application for higher VCC loads and higher ambient temperatures

### 3.3 High Side Reverse Polarity Protection

A high side full bridge reverse polarity protection can also be realised using the below schematics.

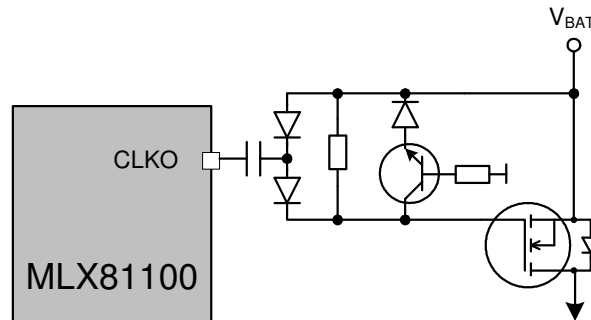


Figure 4 - High side N-FET reverse polarity protection

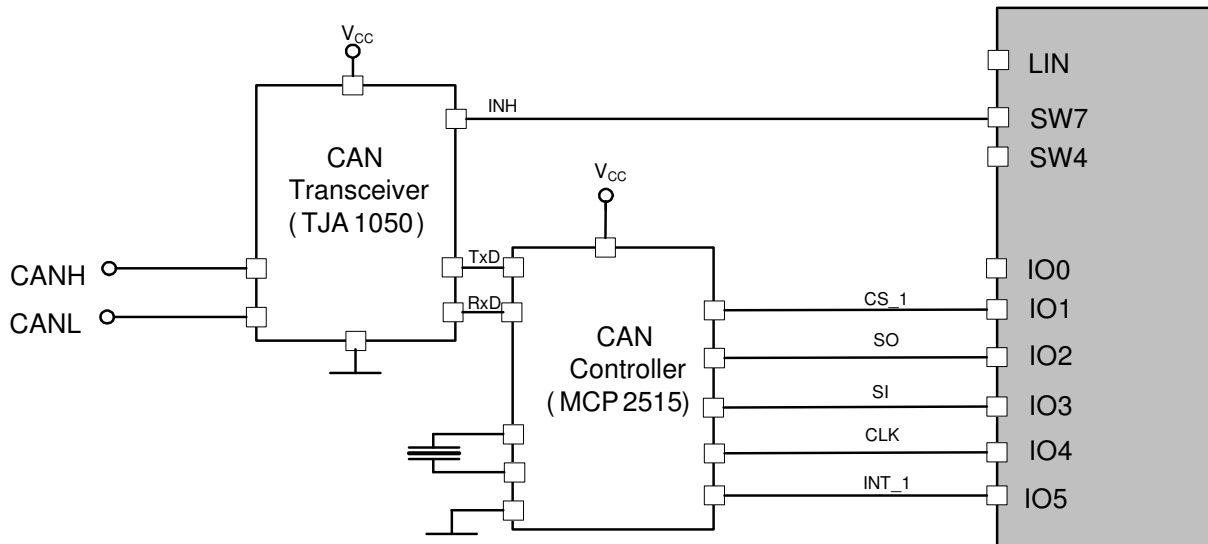


### 3.4 Connection to External CAN Controller

If the application requires a connection to the CAN network it can be realized with the help of an external CAN communication CPU. The following circuitry shows a sample how to implement this together with our MLX81100.

The communication between MLX81100 and external CAN controller is done via the SPI interface of the MelexCM.

A bus wake-up will be signalled at the INH pin of the CAN transceiver. This signal will be used from a normal HV-IO pin to wake-up the MLX81100.



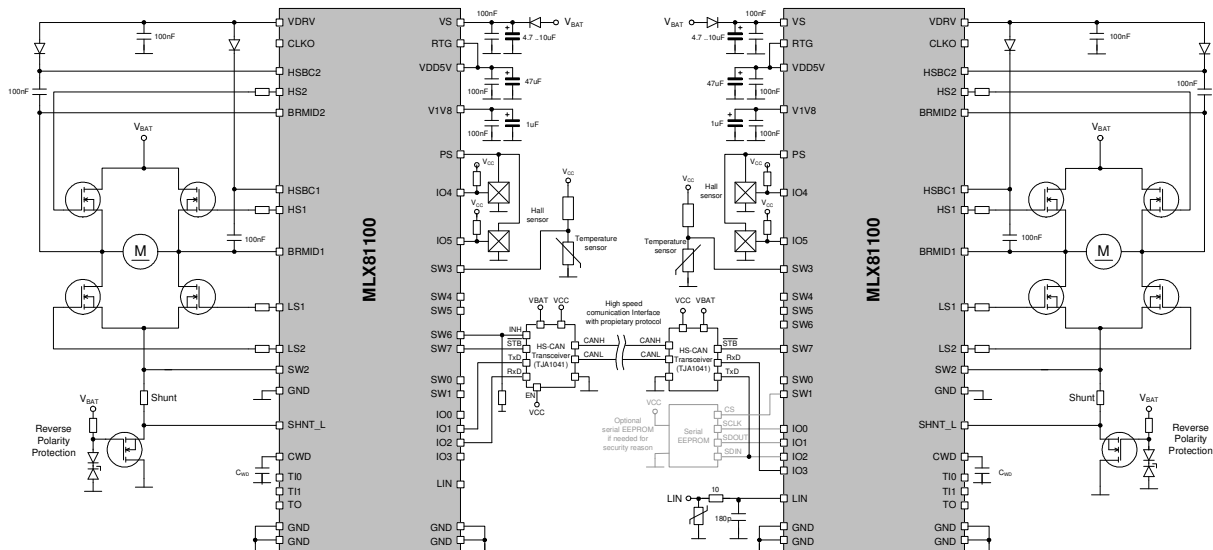
**Figure 5 - Connection to external CAN controller**

### 3.5 Dual DC-Motor Drive

In this sample application the IC realizes driving of 2 DC motor via an external power N-FETs bridge. The high side N-FET driving is done with a bootstrap output stage. The current control of the motor is done via shunt measurement; the reverse polarity protection of the bridge must be realized with an external power FET connected to ground. Short circuit of the bridge will be detected with internal fast comparators and in this case the bridge will be switched off.

Weak short circuits are monitored with an external temperature sensor. The actual position can be read with hall sensors, which are connected to the timer capture inputs. The hall sensors are switched off during standby mode via a switch-able battery voltage output VS. If there is a need to synchronize the motor movement via longer distances it can be done via the serial interface connected to an external high speed CAN transceiver as a physical layer.

Via this interface together with a proprietary protocol it is possible that both motor drivers exchange real time position information. Optional it is possible to connect an external EEPROM via serial interface, if the application can not use internal memories. This external memory will be completely stay under API control by using pins of a digital port to create needed signal waveforms for EEPROM.



Application example for Dual DC motor driver

Figure 6 - Application circuitry for a dual DC-motor system

### 3.6 Human Interface Device with DC-Motor

In this sample application the IC can realize the driving of a feedback DC motor via an external power N-FET bridge. The high side N-FET driver is created with a bootstrap output stage. The current control of the motor is done via shunt measurement and the reverse polarity protection of the bridge must be realized with an external power FET connected to the ground line.

Short circuits of the bridge will be detected from fast comparators and in this case the bridge will be switched off. Weak short circuits are monitored with an external temperature sensor. Detecting rotation direction and positions of a rotating encoder can be easy done via the timer capture inputs. The 6 high voltage pins SW[n] make it possible to implement a switch matrix up to 3x3 or 6 single switches.

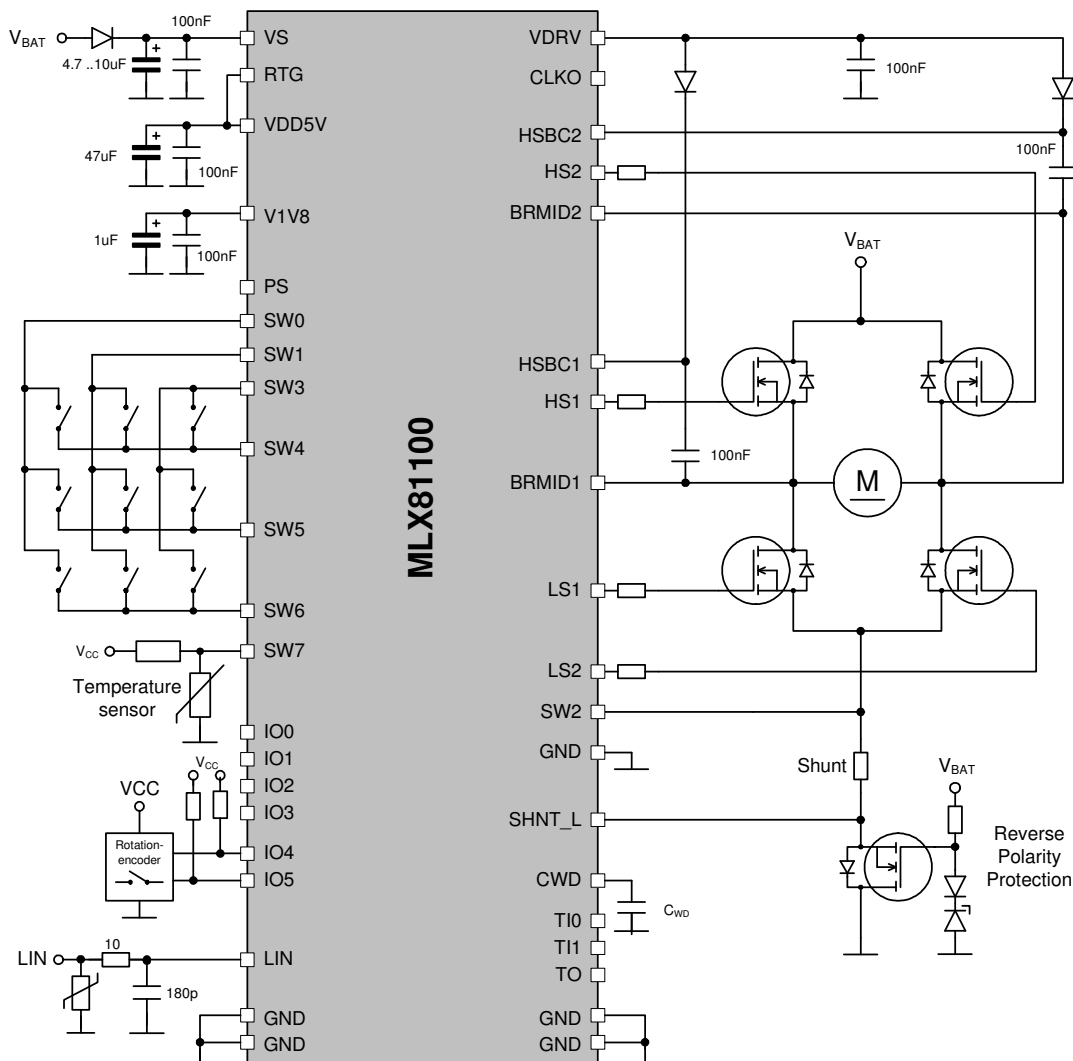


Figure 7 - Application circuitry for human interface device with DC-motor

### 3.7 Seat Heating and Climatization

In this sample application the IC drives 2 separate heat elements via high side drivers and 2 motors via the low side drivers. The high side N-FET driving is done with a bootstrap output stage. The current control of the high side FET is realized via shunt measurement and the shunt voltage is amplified with a differential amplifier connected to the ADC.

The reverse polarity protection of the low side FET must be realized with an external power FET connected to the ground line. Short circuits of the single FET will be detected with integrated comparators and in this case the FET will be switched off. Weak short circuits must be monitored with an external temperature sensor.

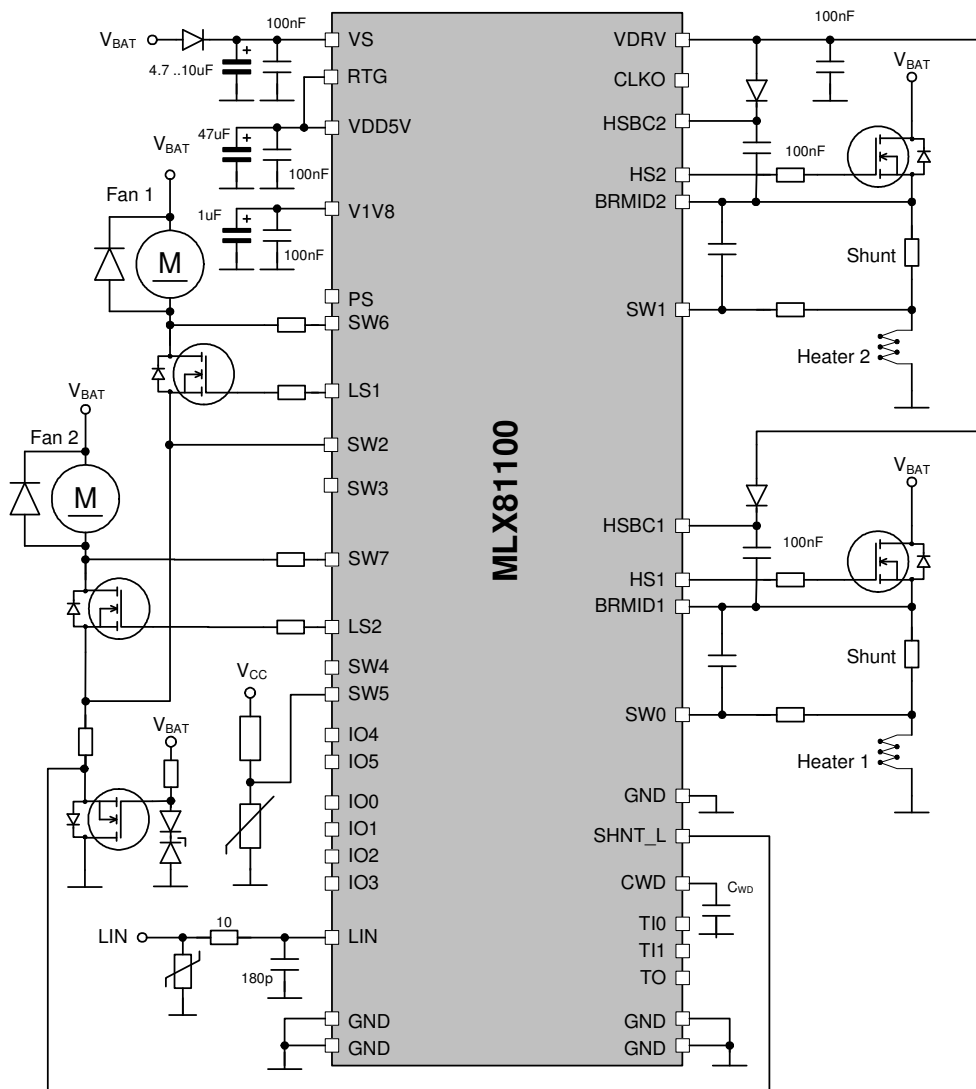
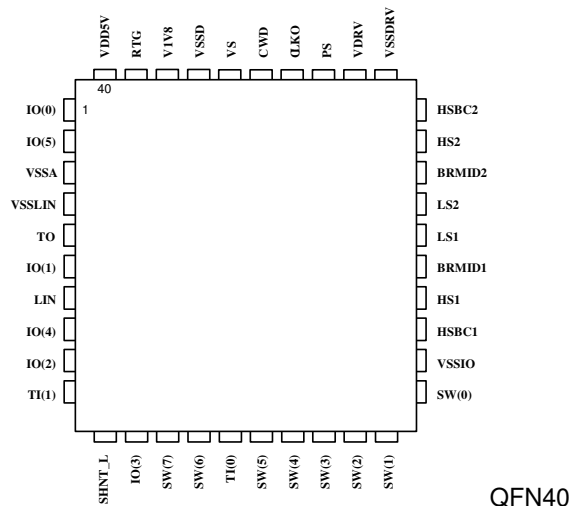


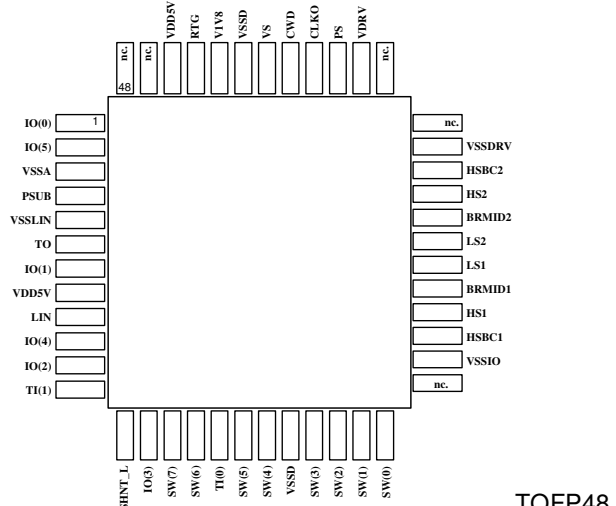
Figure 8 - Application circuitry for seat heating and seat climatization

### 4. Pin Description

Pin of QFN	Package Pins	Analog IC Pads	Digital IC Pads	Pin name	voltage range	remarks and description	Pin of TQFP
36	1	1	0	VS	Pwr HV	Battery supply voltage; external protection against reverse polarity needed	42
4,31,22,3,37	5	6	2	GND	Pwr HV	Ground: Digital, Analogue, LIN, Driver, Pads: VSSLIN, VSSDRV, VSSIO, VSSA, VSSD / (PSUB at TQFP only)	5,35,26,20,43,3,4
40	1	2	1	VDD5V	Pwr LV	Input from Regulator (5 V), external blocking capacitors	46
38	1	1	2	V1V8	Pwr LV	Regulator output (about 1.8 V), external blocking capacitors	44
39	1	1	0	RTG	An HV	External regulator transistor control output, to be connected to VDD5V or external n-type Transistor	45
33	1	1	0	PS	Pwr HV	Switch-able supply (VS) output voltage, internal clamped	39
13,14,16-21	8	8	0	SW[7:0]	Multifunc HV	High voltage I/O port with wake-up function, configurable	15,17-19,21-24
35	1	1	0	CWD	An LV	Watch dog load capacitor	41
11	1	1	0	SHNT_L	An LV	Shunt measurement connection for ADC	13
26,27	2	2	0	LS1, LS2	An HV	Gate driver for external N-channel MOSFET in low-side configuration	30,31
24,29	2	2	0	HS1, HS2	An HV	Gate driver for external N-channel MOSFET in high-side configuration	28,33
32	1	1	0	VDRV	An HV	Regulator output, internal clamped, for pre-charging of bootstrap capacitors of the high side gate driver	38
23,30	2	2	0	HSBC1, HSBC2	An HV	Connection of bootstrap capacitors	27,34
25,28	2	2	0	BRMID1, BRMID2	An HV	Midpoint of a full bridge (usually the source of high-side FET and drain of it's low-side FET)	29,32
7	1	1	0	LIN	An HV	LIN transceiver BUS pin	9
34	1	1	0	CLKO	Dig 5V	Clock 307kHz for possible external charge pump or Chip select/input	40
2,8,12,9,6,1	6	0	6	IO[5:0]	Dig LV	Digital IO (MelexCM)	2,10,14,11,7,1
10,15	2	0	2	TI[1:0]	Test input	Test inputs for Melexis (MelexCM) - connect to GND	12,16
5	1	0	1	TO	Test output	Test output for Melexis (MelexCM), unconn. in application	6



QFN40



TQFP48

Pin of QFN	Package Pins	Analog IC Pads	Digital IC Pads	Pin name	voltage range	remarks and description	Pin of TQFP
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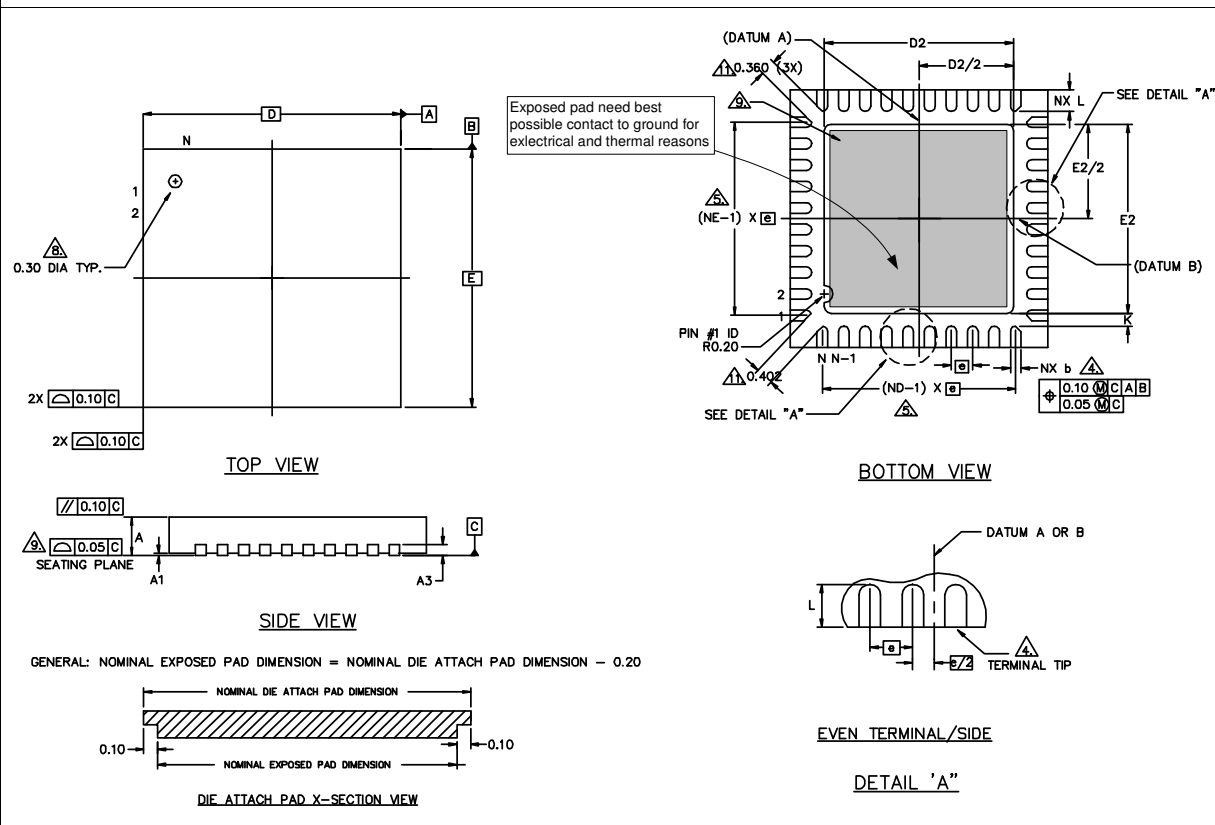
Dig= digital input, output, bidir / An= analogue pin / Pwr= power/supply pin  
 Multifunc= multifunctional pin (configurable pin) / Test= pin for test purposes  
 LV= low volt, vdd5v or v1v8 related / HV= high voltage, VBAT or VS related

### 5. Mechanical Specification

#### 5.1 QFN 6x6 40 sawn

	A	A1	A3	d	D	D2	E	E2	e	L	N	ND	NE	K	
min	0.80	0.00	0.20	0.18	6.00	4.00	6.00	4.30	0.50	0.45	40	10	10	0.20	
nom	0.85	0.02		0.25		4.40		4.40		0.50				0.50	-
max	0.90	0.05		0.30		4.50		4.50		0.55				-	

1. Dimensions and tolerances conform to ASME Y14.5M-1994
  2. All dimensions are in Millimeters. All angels are in degrees
  3. N is the total number of terminals
  - Δ4. Dimension b applies to metallic terminal and is measured between 0.15 and 0.30mm from terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area
  - Δ5. ND and NE refer to the number of terminals on each D and E side respectively
- Depopulation is possible in a symmetrical fashion



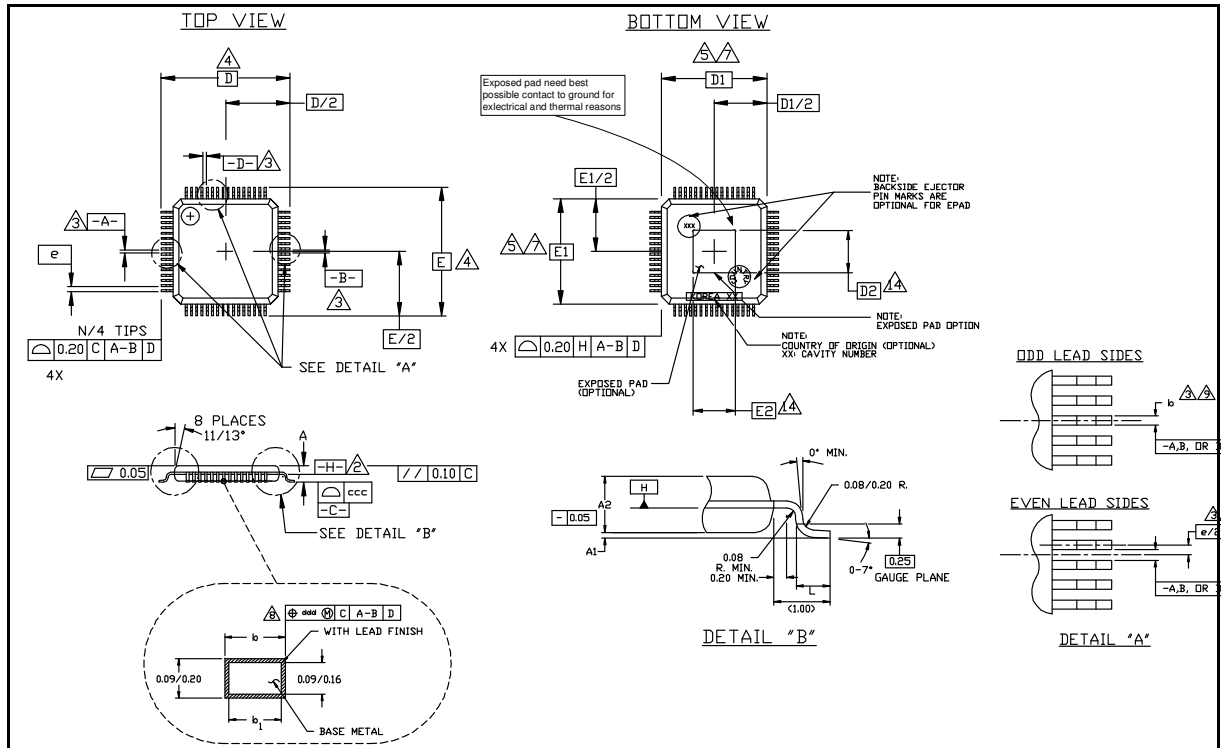
### 5.2 TQFP 7x7 EP 48L

	A	A1	A2	b	b1	D	D1	D2	E	E1	E2	e	L	N	ccc	ddd
<b>min</b>	-	0.05	0.95	0.17	0.17	9.00	7.00	5.00	9.00	7.00	5.00	0.50	0.45	48	-	-
<b>nom</b>	-	-	1.00	0.22	0.20								0.60		-	-
<b>max</b>	1.20	0.15	1.05	0.27	0.23								0.75		0.08	0.08

**Notes:**

1. All Dimensioning and Tolerances conform to ASME Y14.5M-1994,
2. Datum Plane [-|-] located at Mould Parting Line and coincident with Lead, where Lead exists, plastic body at bottom of parting line.
3. Datum [A-B] and [-D-] to be determined at centreline between leads where leads exist, plastic body at datum plane [-|-]
4. To be determined at seating plane [-C-]
5. Dimensions D1 and E1 do not include Mould protrusion. Dimensions D1 and E1 do not include mould protrusion. Allowable mould protrusion is 0.254 mm on D1 and E1 dimensions.
6. 'N' is the total number of terminals
7. These dimensions to be determined at datum plane [-|-]
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dam bar protrusion, allowable dam bar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition, dam bar can not be located on the lower radius of the foot.
10. Controlling dimension millimetre.
11. maximum allowable die thickness to be assembled in this package family is 0.38mm
12. This outline conforms to JEDEC publication 95 Registration MS-026, Variation ABA, ABC & ABD.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
14. Dimension D2 and E2 represent the size of the exposed pad. The actual dimensions are specified ion the bonding diagram, and are independent from die size.
1. 15. Exposed pad shall be coplanar with bottom of package within 0.05.





## 6. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

### Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020  
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113  
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

### Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20  
Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15  
Resistance to soldering temperature for through-hole mounted devices

### Iron Soldering THD's (Through Hole Devices)

- EN60749-15  
Resistance to soldering temperature for through-hole mounted devices

### Solderability SMD's (Surface Mount Device) and THD's (Through Hole Device)

- EIA/JEDEC JESD22-B102 and EN60749-21  
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:  
<http://www.melexis.com/quality.aspx>

### 7. *Disclaimer*

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