MLX90288

SMD Programmable Linear Hall Sensor IC
Featuring Analog Ratiometric Output

Features and Benefits

- Surface mounted device
- Analog ratiometric output
- Measurement range from 6mT to 650mT bipolar full scale
- Digital IIR filtering for accurate bandwidth
- Offset trimming possible outside output range
- 1st and 2nd order magnet TC compensation
- Reverse polarity and overvoltage protection
- Extensive diagnostic features

Application Examples

- Rotary position sensor
- Linear position sensor
- Proximity sensor

Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90288	L	DC	CAA-000	TU
MLX90288	L	DC	CAA-000	RE
MLX90288	K	DC	CAA-000	TU
MLX90288	K	DC	CAA-000	RE

Legend:

Temperature Code:	L for Temperature Range -40°C to 150°C K for Temperature Range -40°C to 125°C
Package Code:	DC for SOIC150Mil
Option Code:	AAA-xxx: Die version xxx-000: Standard version
Packing Form:	RE for Reel, TU for Tube
Ordering example:	MLX90288LDC-CAA-000-TU

-

1 Functional Diagram

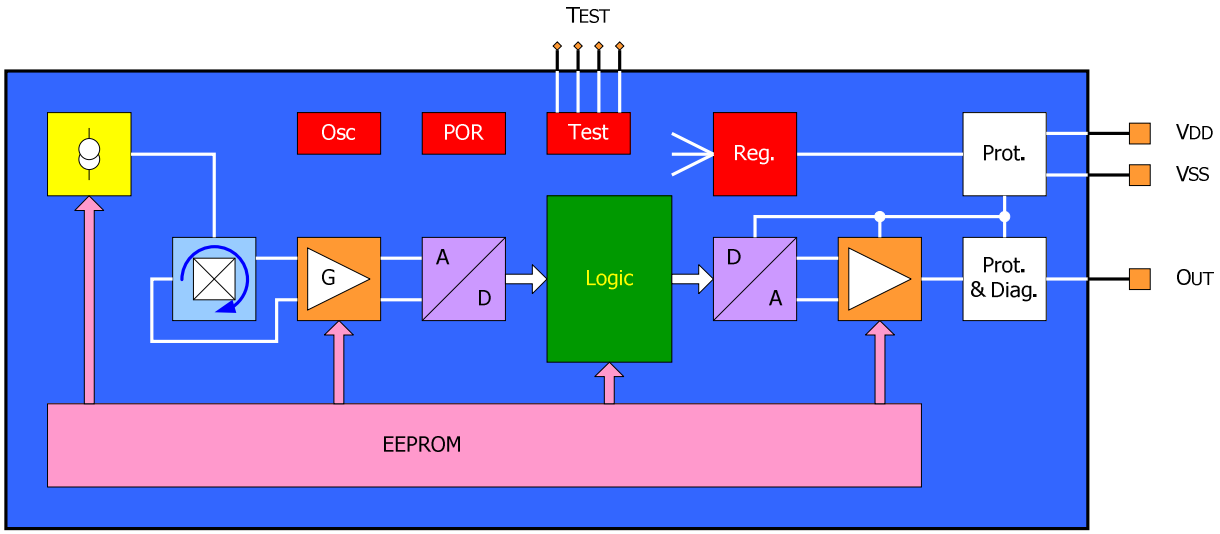

Figure 1: Block diagram of the MLX90288

2 Table of Contents

3 General Description

The MLX90288 is a cost-effective monolithic programmable linear Hall sensor which provides an analog ratiometric output signal proportional to the magnetic flux density that is applied perpendicular to the die surface. The MLX90288 is fully programmable (offset, sensitivity, clamping levels, magnet temperature drift, digital IIR filtering …) through the connector, using the PTC-04 programming tool. It supports both linear and quadratic magnet TC compensation.

4 Glossary of Terms

Tesla (T)	Unit for the magnetic flux density, 1 mT = 10 Gauss
TC	Temperature Coefficient (in ppm/°C)
IC	Integrated Circuit
SMD	Surface Mounted Device
N/C	Not Connected
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
PTC	Programming Through Connector
ECU	Engine Control Unit
POR	Power on Reset
INL	Integral Non Linearity
DNL	Differential Non Linearity
CRC	Cyclic Redundancy Check
ESD	Electro-Static Discharge
EMC	Electro-Magnetic Compatibility
OBD	On-Board Diagnostics

5 Specification

5.1 Absolute Maximum Ratings

Item	Symbol	Rating
Supply Forward-Voltage	V_{DDFWD}	+ 30 V (continuous) (Breakdown at + 40 V)
Supply Forward-Current	I_{DDFWD}	+ 20 mA
Supply Reverse-Voltage	V_{DDREV}	– 14.5 V (continuous) (Breakdown at – 19 V)
Supply Reverse-Current	I_{DDREV}	– 2 mA
Output Forward-Voltage	V_{OUTFWD}	+ 18 V
Output Forward-Current	I_{OUTFWD}	– 60 mA
Output Reverse-Voltage	V_{OUTREV}	– 14 V
Output Reverse-Current	I_{OUTREV}	+ 20 mA
Storage Temperature Range (Non Operating)	T_S	-55°C to +165°C
Operating Ambient Temperature Range	T_A	-40°C to +150°C
Junction Temperature	T_J	+165°C
Package Thermal Resistance	R_{TH}	100 K/W
Maximum Flux Density	B_{MAX}	2T

Table 1: Absolute Maximum Ratings

Exposing a part to absolute maximum ratings for extended periods of time may affect device reliability.

5.2 Electrical Specification

Operating parameter valid for T_A = – 40°C to + 150°C & V_{DD} = + 4.5V to + 5.5V (unless specified otherwise).

Item	Symbol	Remark	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	Guaranteed spec operation	4.5	5	5.5	V
Supply Current	I_{DD}	Worst case (min R_{PD}, max VDD)	-	8.8	10	mA
Regulated Voltage	V_{REG}	Internal voltage	3.0	3.3	3.6	V
Reset Voltage	$V_{PORRISE}$	Output is high impedant for $V_{POR} < V_{DD} < V_{UNDER}$	2.5		3.4	V
	$V_{PORFALL}$		2.4		3.3	V
Undervoltage Threshold	$V_{UNDERRISE}$	Operating if $V_{DD} > V_{UNDER}$	3.4		4.4	V
	$V_{UNDERFALL}$		3.3		4.3	V
Programming Voltage(1)	$V_{PROGRISE}$	Device not locked	6.2		7.2	V
	$V_{PROGFALL}$		6.1		7.1	V
Overvoltage Threshold(2)	V_{OVER}	Disconnect V_{PROT} from V_{DD}	8.4		14	V
Load Resistance Range	R_{PD}	Pull-down to GND	8	10	330	kΩ
Load capacitor range	C_L	Between OUT and GND	47		1000	nF
Output Saturation Voltage(3)	V_{SATHI}	Including R_{PD}	96		100	$\%V_{DD}$
	V_{SATLO}	Including R_{PD}	0		2	$\%V_{DD}$
Output Current Limitation(4)	$I_{OUTLIMGND}$	Output amplifier sourcing strength	2	5	8	mA
	$I_{OUTLIMVDD}$	Output amplifier sinking strength	2	5	8	mA
Supply Current Limitation	I_{VDDLIM}	Same condition as above	5		18	mA
Output Diagnostic Band Leakage Current(5)	I_{DIAGLO}	Leakage current over T_A V_{DD}=5V			500	nA
Output Diagnostic Level	V_{DIAGLO}	Leakage current over T_A and V_{DD} span			R_{PD} x I_{DIAGLO}	V

Table 2: Electrical Specification

(1) The programming voltage defines the threshold at which the ASIC goes into PTC mode, where the output pin becomes bidirectional. Write access is eventually defined by the locking bits as described in Section 6.1

(2) The overvoltage threshold will disconnect all internal supplies (Vana, Vdig & Vprot) from V_{DD}; the output becomes high impedant.

(3) The saturation voltage is the rail voltage the output amplifier can reach actively with R_{PD} connected.

(4) The maximum current the output stage can deliver to keep its DC value, in case the output is pulled to one of the rails by means of an external power supply, while V_{DD} = 5V.

(5) The leakage current is in fact the current sourced by the output in case of an OBD detection (broken ground), where the output goes into high-Z mode. For better contacting at the connectors over lifetime and bigger rail-to-rail operation, the smaller pull-down resistors from this specification are recommended at ECU side.

5.3 Timing Specification

Operating parameter valid for T_A = – 40°C to + 150°C & V_{DD} = + 4.5V to + 5.5V (unless specified otherwise).

Item	Symbol	Remark	Min	Typ	Max	Unit
Power Supply Slew Rate	VDDSR	External supply VDD	5e-6		5	V/µs
Startup time(1)	$t_{STARTUP}$		200	500	800	µs
Main Oscillator Frequency	F_{OSC}	Tolerance ± 10%	900	1000	1100	kHz
Conversion Rate	t_{CONV}	Acquisition of Hall and Temperature signals (no digital filtering)	130	144	158	µs
	f_{CONV}		6.33	7	7.7	kHz
Programmable Filtering(2)	BW	Tempsensor enabled	0.004		1.114	kHz
Output Amplifier Rise Time (10%-90%)(3)	t_{RISEPP}	R_L = 8 kΩ to Ground C_L = 330 nF to Ground		300		µs
Output Amplifier Fall Time (90%-10%)(3)	t_{FALLPP}	R_L = 330 kΩ to Ground C_L = 330 nF to Ground		200		µs
Calibration Time(4)	t_{CALIB}	EE Full Erase + Write			6	ms
		EE Full Read		180		ms
		RAM Write			3	ms

Table 3: Timing Specification

(1) Startup time is defined as the time between crossing the POR level and having the first DAC output update. It includes loading of the parameters from EEPROM, checking the CRC validity, initializations and the signal latency between the first Hall plate acquisition and the DAC output update.
(2) Filtering is programmable with the FILTCODE parameter in EEPROM. The filter consists of an IIR filter in the digital. For more details about the corresponding bandwidths, see Section 6.3.3.
(3) Rise and fall times are measured for worst case conditions, hence the difference in Rload for both parameters. These specifications are only defined by the output amplifier and its load. The output amplifier (Gain=2) is given a step response at the input from 5%V_{DD} to 45%V_{DD} and the rise/fall times are measured as the time between reaching 10% and 90% of the step response DC output voltages (10%V_{DD} to 90%V_{DD}).
(4) Calibration times measured at room temperature with PTC-04 and DB-HALL03 daughterboard, FIR090288AAMLX firmware loaded onto the PTC-04 and on a MLX90288 in the recommended application diagram from Section 10 at 10kbit/s.

5.4 Transfer Characteristic Specification

Operating parameter valid for T_A = – 40°C to + 150°C & V_{DD} = + 4.5V to + 5.5V (unless specified otherwise).

Item	Symbol	Remark	Min	Typ	Max	Unit
Output Clamping Range	CLAMPLO	9 bits(1)	0		50	%V_{DD}
	CLAMPHI	10 bits (1)	0		100	%V_{DD}
Output Quiescent (Offset) Voltage Range	V_{OQ}	14 bits (YA setting) (1)	– 200		200	%V_{DD}
Sensitivity Range	S	RG[2] = 1 (1) For full-scale output(2)	±0.04		±0.4	%V_{DD}/G

Table 4: Transfer Characteristic Specification

(1) Please refer to Section 6.2 for more detailed information.
(2) The full-scale output corresponds to 100%Vdd output range. This corresponds to 100% of the ADC range when FINEGAIN is set to 1 (1024LSB) in a bipolar application.

5.5 Accuracy Specification

Operating parameter valid for T_A = – 40°C to + 150°C & V_{DD} = + 4.5V to + 5.5V (unless specified otherwise).

Item	Symbol	Remark	Min	Typ	Max	Unit
Output DAC Resolution	LSB_{DAC}	12 bits		0.0244		$\%V_{DD}$
Output DAC Linearity	DNL_{DAC}		– 1		+ 1	LSB_{DAC}
	INL_{DAC}		– 2		+ 2	LSB_{DAC}
Ratiometric Error(1)	OUT_{ratiom}	with TEMPTC=0	– 0.1		+ 0.1	$\%V_{DD}$
		with TEMPTC=128	– 0.2		+ 0.2	$\%V_{DD}$
Output Noise(2)	OUT_{noise}	RG = 4, FG = 800 FILTCODE = 4		0.12	0.18	mV_{RMS}
		RG = 7, FG = 800 FILTCODE = 4		0.13	0.2	mV_{RMS}
		RG = 4, FG = 4095 FILTCODE = 4		0.75	1.1	mV_{RMS}
		RG = 7, FG = 4095 FILTCODE = 4		1	1.5	mV_{RMS}
Thermal Output Quiescent (Offset) Drift	$\Delta^T V_{OQ}$	RG = 4	– 10		+ 10	LSB_{DAC}
		RG = 5	– 10		+ 10	LSB_{DAC}
		RG = 6	– 15		+ 15	LSB_{DAC}
		RG = 7	– 20		+ 20	LSB_{DAC}
Thermal Sensitivity Drift(3)	$\Delta^T S$	No magnet TC	– 150	0	+ 150	ppm/°C
		Using 1st and 2nd order magnet TC	– 200	0	+ 200	ppm/°C
Sensitivity Thermal Hysteresis	$\Delta^H S$	After full thermal excursion	– 0.5	± 0.2	+ 0.5	%

Table 5: Accuracy Specification

(1) Ratiometric performance of the IC is measured as a difference in output voltage (expressed as $\%V_{DD}$) between the nominal case with V_{DD} = 5V and the limits of the supply ratiometric operating range (4.5V and 5.5V). The difference between TEMPTC = 0 (or TEMPSENSOR disabled altogether) and TEMPTC = 128 originates in the fact that the on-chip temperature is also a function of the supply voltage. Since the TEMPTC changes the gain of the IC to compensate for the magnet TC, and it relies on the fact that the on-chip temperature is the same as the magnet temperature, an extra error occurs compared to TEMPTC = 0 case.

(2) The noise measurements are performed on the recommended application diagram depicted under Section 10, with a supply voltage of 5V at room temperature. Increased capacitance values compared to the recommended application diagram, contribute to lower output noise. For peak-to-peak values, the RMS value is typically multiplied by a factor of 6.

(3) The Sensitivity Thermal Drift is within these boundaries for all ICs with the default setting for gain compensation i.e. fixed to 1, which is obtained by setting TEMPTC to 0, but leaving the TEMPSENSOR bit set (see Section 7). If the value is not fixed to 1, the sensitivity of the IC will exhibit a sensitivity thermal drift curve such as the one shown in Figure 3 (if SECONDORDERTC is set) or with a linear temperature coefficient (if SECONDORDERTC is cleared) depending on the setting of TEMPTC, but ±150ppm/°C. The total system sensitivity drift is specified as ±200ppm/°C to cover resolution errors and non-linearities.

5.6 Diagnostic Specification

Operating rating valid for T_A = – 40°C to + 85°C & V_{DD} = + 4.5V to + 5.5V (unless specified otherwise).

Item	Symbol	Remarks	Min	Typ	Max	Unit
ADC Clipping Signaling(1)	$DIAG_{CLIP}$	DIAGINFAULT = 0	-	-	V_{SATLO}	$\%V_{DD}$
		DIAGINFAULT = 1	V_{SATHI}	-	-	$\%V_{DD}$
ADC Clipping Criterion(1)	N_{CLIP}	ADC clipping count before Diagnostic is set	-	4	-	Count
CRC Fail Signaling	$DIAG_{PAR}$	DIAGINFAULT = 0	-	-	V_{SATLO}	$\%V_{DD}$
		DIAGINFAULT = 1	V_{SATHI}	-	-	$\%V_{DD}$
CRC Fail Criterion	N_{CRC}	CRC Fail count before Diagnostic is set	-	3	-	Count
Broken V_{SS}(2)	$V_{OUTbrVSS}$	Over R_{PD} range	-	-	V_{DIAGLO}	$\%V_{DD}$
Broken V_{DD}(2)	$V_{OUTbrVDD}$	Over R_{PD} range	-	-	V_{DIAGLO}	$\%V_{DD}$

Table 6: Diagnostic Specification

(1) ADC clipping is only flagged if the FAULTONCLIP bit in EEPROM is set. If the bit is cleared, the ADC will clamp at either the maximum code or the minimum code, depending on the clipping condition. Reporting after 4 sequential clipping conditions is required for an EMC robust design. Clipping reporting does not apply to ADC values of the temperature signal.

(2) Diagnostics that are the result of a passive settling because the output stage becomes high impedant (such as broken wire) are governed by the RC time constant of the capacitive load on the output and the R_{PD} resistor at ECU side. The OBD detection time is negligible in comparison to the settling time in case of a broken wire. The settling time should be taken as 4 times the RC time constant. E.g. with a load of 330nF and 330kOhm, the RC time constant equals 109ms. Settling time then corresponds to 4 RC time constants, i.e. 436ms.

5.7 Startup, Undervoltage, Overvoltage and Reset Specification

During power-up (supply rising from 0V upwards) the MLX90288 remains in a zone where the output is undefined (grey triangular area in the plot) because there is no active circuitry putting the output stage in a specific condition. Most likely the output remains close to the low rail because of the passive external pull-down, but it can not be predicted what happens exactly inside the IC at this point. This is also depicted in the signal waveforms of Figure 2.

The POR phase is the phase where the supply is still below $V_{PORRISE}$, but above the undefined region. In this case the digital is in a reset state, which puts all flip-flops in a known state, and the output is high impedant. Due to the external pull-down resistive load, the output is at the low rail.

When the supply rises above the $V_{PORRISE}$ threshold (which has built-in hysteresis: for the falling edge, $V_{PORFALL}$), an initialization occurs which includes loading all EEPROM settings into RAM. After this initialization phase, the chip will start its FSM program and provide a valid output signal, for as long as the supply voltage is above the $V_{UNDERRISE}$ threshold (which has built-in hysteresis: for the falling edge, $V_{UNDERFALL}$). If the supply is below this threshold, the output remains in high impedant state, corresponding to an output voltage at the low rail.

Whenever the MLX90288 goes from normal operation to undervoltage or via undervoltage to reset state, and vice versa, the output has a settling time which is a function of both the output load and the driving capability. On top of this, there is a startup time ($t_{STARTUP}$) in case the chip comes out of reset.

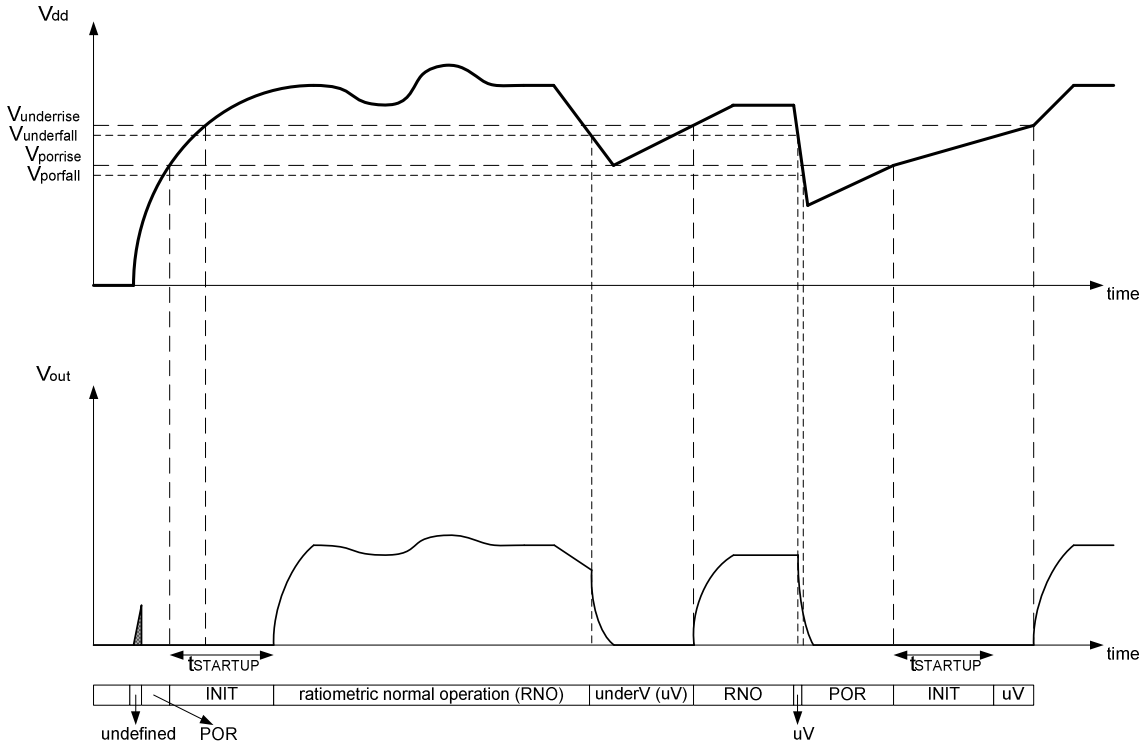

Figure 2: Operating, undervoltage and reset functionality

In case the supply is raised above the $V_{PROGRISE}$ threshold (which has built-in hysteresis: for the falling edge, $V_{PROGFALL}$), but below the V_{OVER} threshold, the IC goes in programming mode: the output becomes high impedant and after proper commands coming from the programming unit (PTC04), the IC can respond on the output pin as well. The communication protocol on the output (PTC-04 communication) is bi-directional. If the supply is higher than the V_{OVER} threshold, the internal regulated supply is disconnected from the external supply, as are most blocks of the IC. A reset will be the result when the supply is restored.

5.8 EMC/ESD Specification

Operating parameter valid for T_A = – 40°C to + 150°C & V_{DD} = + 4.5V to + 5.5V (unless specified otherwise).

Item	Symbol	Remarks	Min	Typ	Max	Unit
Micro-interrupt without reset(1)	µI		-	-	0.1	µs
ESD Human Body Model(2)	ESD_{HBM}			± 2		kV
ESD Charged Device Model(3)	ESD_{CDM}			± 500		V

Table 7: EMC/ESD Specification

(1) If the digital regulated voltage drops below POR level, the ASIC will reset nearly immediately; this is a necessity from a DFMEA point of view. The only way to make the ASIC immune for longer micro-interrupts is to have external components (Rseries and Csupply) filtering these micro-interrupts for the ASIC. Introducing an Rseries in the supply line will have a negative impact on ratiometricity.
(2) ESD HBM test performed on all pins according to JEDEC-22-A-114 standard.
(3) ESD CDM test performed on all pins according to AEC-Q100-011 standard.

6 EEPROM Mapping

6.1 EEPROM Description

All calibration parameters on the MLX90288 are stored in a 32 x 16bit non-volatile EEPROM.

The EEPROM parameters from the first 29 addresses are stored with triple redundancy, to correct if any EEPROM bit would loose its content, by using majority voting. Consequently, an EEPROM word in this part of EEPROM only holds the information of 5 calibration bits + 1 locking bit at index 15. The EEPROM word stored at address 0 thus looks like this:

{LOCK0,PARAM[4:0],PARAM[4:0],PARAM[4:0]}

If bit index 15 is set, the EEPROM word is permanently locked, making it impossible to overwrite the given address in PTC mode.

ID bits from the last 3 addresses are not stored with redundancy. The MLXID is not programmable in PTC mode, hence guaranteeing traceability of the parts.

There are no constraints on the EEPROM readout in PTC mode.

6.2 Melexis Programmable Parameters

6.2.1 OSCTRIM [4:0]

- Will be calibrated at MLX production
- Trims oscillator frequency around 1 MHz

6.2.2 TRIMCTAT [4:0]

- Will be calibrated at MLX production
- Trims PTAT and CTAT to have both current sources at the same level at 25°C
- This calibration is necessary to allow correct TC1 trimming with a single measurement at either hot or cold
- The calibration compensates mismatch in both PTAT and CTAT current sources

6.2.3 ITRIM[2:0]

- Will be calibrated at MLX production
- Trims the current reference used throughout the analog part to a predefined value

6.2.4 IPLATE[3:0]

- Will be calibrated at MLX production
- Defines the current through the Hall plates, impacting the total gain

6.2.5 TC1ST[6:0]

- Will be calibrated at MLX production
- Programming first order sensitivity temperature drift compensation
- Piecewise linear compensation between hot and cold temperatures = TC1ST

6.2.6 TC2ND[5:0]

- Will be calibrated at MLX production
- Programming piecewise linear sensitivity temperature drift compensation
- It is like an additional TC1 starting at 25 °C +/-30 °C
- Piecewise linear compensation for hot temperatures = TC1ST + TC2ND

6.2.7 TC3RD[2:0]

- Will be calibrated at MLX production
- Programming piecewise linear sensitivity temperature drift compensation
- It is like an additional TC1 starting at - 5 °C
- Piecewise linear compensation for cold temperatures = TC1ST + TC2ND + 2*TC3RD

6.2.8 PLATEPOL

- Will be calibrated at MLX production
- Changes the polarity of the Hall plates, inverting the sensing nodes
- Changing the plate polarity will make the MLX production calibration void
- Changing the polarity of the output signal is recommended to be achieved by changing the FINEGAIN MSB

6.2.9 OFFCST[4:0]

- Will be calibrated at MLX production
- Residual offset calibration (at Integrator stage) to make sure that the ADC input is at half of the ADC span when no field is applied
- Analog compensation, sign magnitude number

6.2.10 OFFDRIFT[5:0]

- Will be calibrated at MLX production
- Compensates linearly for residual offset temperature drift at the Integrator stage
- Analog compensation, sign magnitude number

6.2.11 ROUGHGAIN[2]

- Set by default to 1 by Melexis

6.2.12 XA[13:0]

- Will be calibrated at MLX production
- Gain-dependent offset, should not be modified after calibration
- Removes the residual offset of the ADC output when no field is applied

6.2.13 MLXID[31:0]

- Melexis ID bits for traceability
- Can no be overwritten in PTC mode

6.2.14 CRC[9:0]

- Standard CRC10 for data integrity
- Polynomial is $x^{10}+x^9+x^5+x^4+x^1+1$
- EEPROM data is fed LSB first, per address (5bits, after majority voting) sequentially
- The CRC integrity will be preserved by the PSF software when using the PTC04. It could not be changed manually.

6.3 End User Programmable Parameters

6.3.1 FAULTONCLIP

- Enable error reporting if ADC is clipping for 4 or more successive times
- The diagnostic side for this error is defined by DIAGINFAULT

6.3.2 DIAGINFAULT

- Defines to which side the output will go in case of an active error such as CRC fail or ADC clipping, the latter only in case FAULTONCLIP is set
- The thresholds are specified under Section 5.6

6.3.3 FILTCODE[3:0]

- The digital IIR filter offers noise reduction and low pass filtering with programmable cut off frequency

FILTCODE[3:0]	Cut-off frequency [Hz]
0	1114
1	557
2	279
3	139
4	70
5	35
6	17
7	9
8	4

Table 8: Filter cut-off frequencies

- For Filter code from 9 to 15, the rounding error becomes too high versus the resolution so those codes are not to be used.
- This table only applies in case the temperature sensor is enabled, otherwise the cut-off frequency should be multiplied by a factor of 2 since no more temperature ADC's are performed anymore.

6.3.4 TEMPSENSOR

- Enables digital gain compensation over temperature (GainMag)
- Requires proper calibration of TEMPOFF and TEMPTC, as well as the SECONDORDERTC

6.3.5 SECONDORDERTC

- Chooses between linear gain compensation over temperature (cleared) and ROM based 2nd order compensation (set) as described under Section 5.5

6.3.6 TEMPOFF[9:0]

- Will be calibrated at MLX production
- Defines the offset of the GainMag temperature compensation as described under Section 5.5

6.3.7 TEMPTC[7:0]

- Will be calibrated at MLX production
- Defines the slope of the GainMag temperature compensation as described under Section 5.5

6.3.8 CLPLow[8:0]

- Low clamp level programmability range from 0% to 50% of VDD
- Resolution is 1/4th of the outDAC resolution, i.e. 0.098% of VDD

6.3.9 CLPHigh[9:0]

- High clamp level programmability range from 0% to 100% of VDD
- Resolution is 1/4th of the outDAC resolution, i.e. 0.098% of VDD

6.3.10 ROUGHGAIN[1:0]

- These 2 bits control the gain of the MAIN AMPLIFIER

6.3.11 ATTN2P5

- Enables the attenuation in the analog chain by a factor of 4.5

6.3.12 FINEGAIN[12:0]

- Sign-magnitude 13bit digital fine gain (not 2's complement!)
- The code 1024 (400h) corresponds to a gain of 1
- The code 5120 (1400h) corresponds to a gain of -1
- The MSB is a sign bit
- FINEGAIN range is therefore from -4095 (1FFFh) to +4095 (FFFh), which corresponds to a gain range of -3.999 to +3.999

6.3.13 YA[13:0]

- Output offset programming, not gain dependent
- Defines the offset on the output in case no field is applied, inside a range of -200%Vdd to +200% Vdd with the 12-bit resolution of the output DAC, i.e. 0.0244% of VDD

6.3.14 CSTID[15:0]

- Customer ID bits for traceability

7 Thermal Sensitivity Drift Compensation

7.1 Introduction

The embedded temperature sensor is digitized via the main path ADC before each analog amplified Hall sensor voltage ADC in case TEMPSENSOR is enabled. This temperature information is used to generate either an address for a ROM Look-up Table in order to obtain a quadratic temperature compensation (SECONDORDERTC=1), or a value proportional to the temperature that allows a linear IC gain compensation (SECONDORDERTC=0). Both compensations rely on the TEMPOFF and TEMPTC parameters.

7.2 Linear Compensation (1st Order)

The conventional linear temperature compensation proves to be adequate for small application temperature ranges and/or small magnet temperature coefficients. In such cases the error induced by the linear approach are limited and prove to be good enough for the desired system sensitivity drift.

7.3 Quadratic Compensation (2nd Order)

This look up table is stored in ROM and contains the inverse transfer function of a specific magnetic flux density over temperature. It should be used for magnets with temperature coefficients lower than -1500 ppm/degC, as is typically the case for plastic bonded magnets. Such magnet temperature coefficients can not optimally be compensated by the linear method (see Application Note “Temperature Compensation for Linear Programmable Hall effect sensors” on the Melexis webpage). By multiplying the output of the ROM table with the amplified magnetic flux density signal in the digital domain, the magnet temperature drift is compensated for, resulting in a (nearly) temperature independent sensitivity of the whole system (magnet + IC).

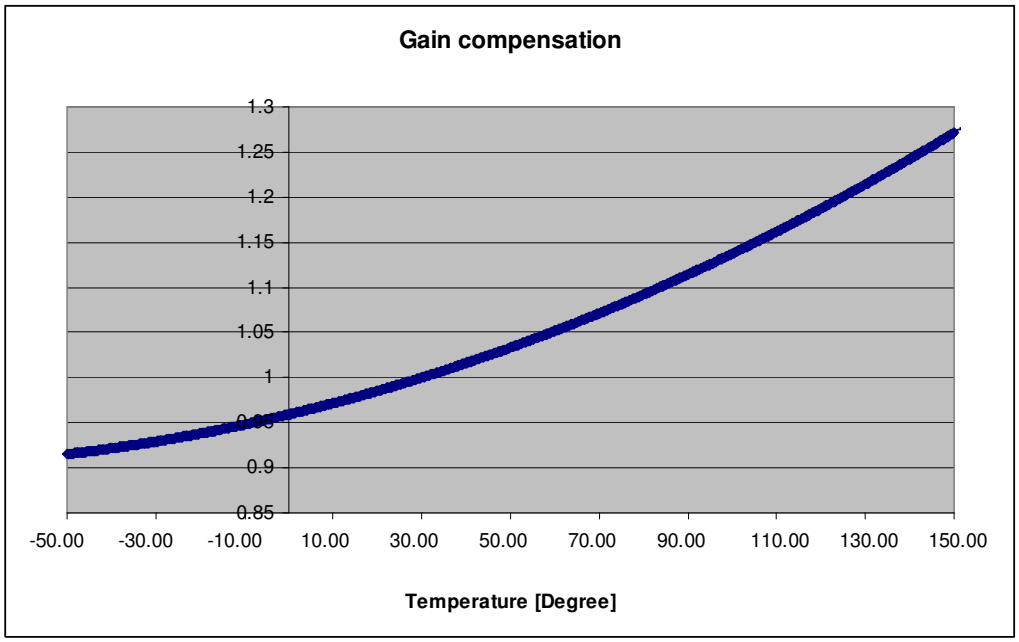

Figure 3: ROM table - 2nd order gain compensation

The factory calibration performed by Melexis targets a specific magnet TC, which serves as accurate basis for any delta calibration that should be performed when using a magnet with a different TC. This is performed via the solver software provided by Melexis. The TEMPOFF parameter defines for which temperature the gain compensation should be 1 (i.e. no compensation), whereas the TEMPTC parameter defines which temperature range of the curve presented in Figure 3 is mapped onto the application temperature range. Higher TEMPTC codes will use a bigger range, which corresponds to more gain compensation and thus bigger magnet temperature coefficients.

7.4 Additional Information

Please refer to the application note “Thermal Sensitivity Drift Compensation on MLX90288” on http://www.melexis.com (coming soon).

8 Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.aspx

9 Package Specification

9.1 Package Dimensions

- Package Type: **SOIC-8 (8-pin Small Outline Integrated Circuit Package)**
- Die placement accuracy is ± 2 mils = ± 50 microns.

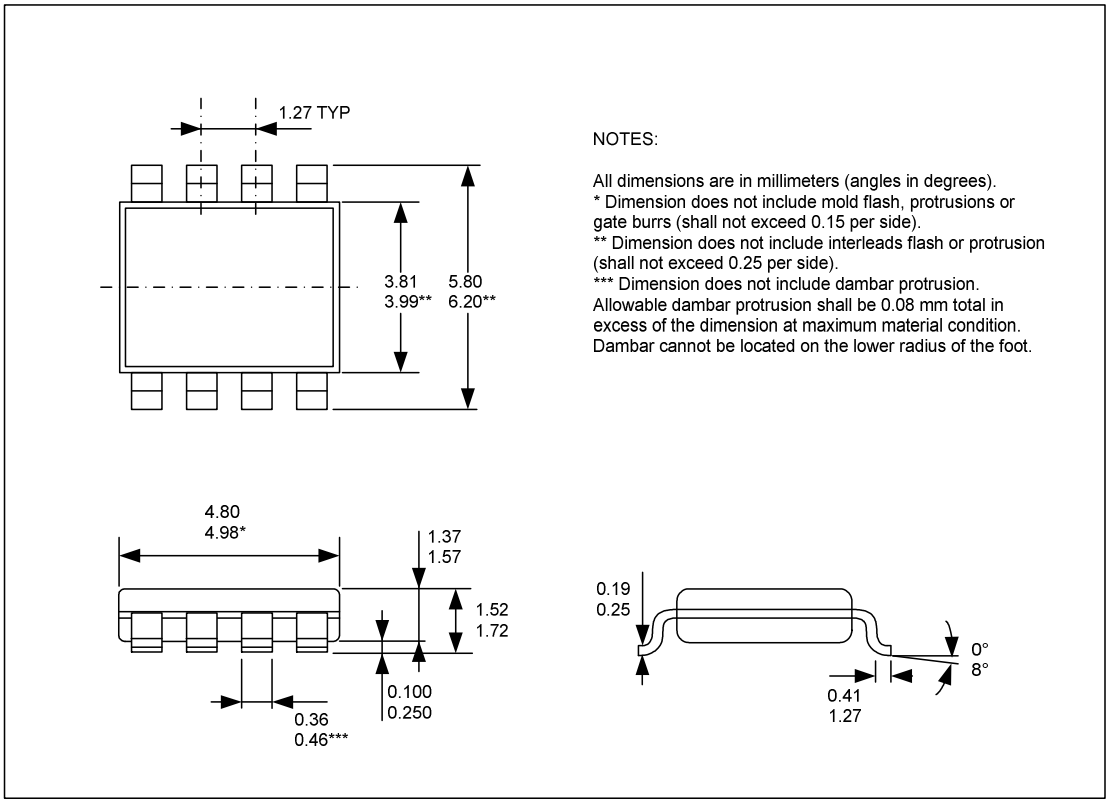

Figure 4: Package Dimensions

9.2 Package Marking

The package is labelled for traceability purposes, as depicted in Figure 5.

The first line is reserved for the project number at Melexis, 90288 followed by the ASIC silicon version. The line below refers to the wafer fab. The bottom line is the date code indicating when the bare dies were packaged at the assembly house. The black dot indicates the position of pin #1.

- MXXXXX = 5-digit lot number (M = wafer fab)
- YYWW = last 2 digits of the year, followed by the calendar week

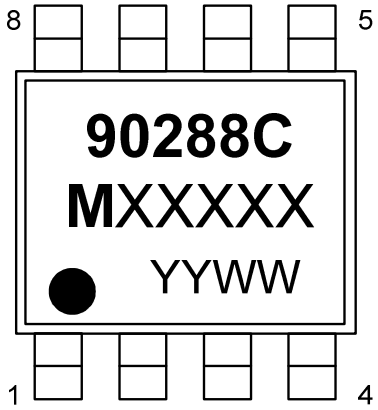

Figure 5: Package markings

9.3 Pinout

Pin #	Name	Direction	Type
1	VDD	POWER	Supply
2	VSS	GND	Ground
3	N/C	/	Not connected
4	OUT	OUT/IN	Analog + PTC communication
5	IDDQ	OUT/IN	Test
6	TESTOUT	OUT	Test
7	MUST0	IN	Test
8	MUST1	IN	Test

Table 9: Pinout

The pinout of the MLX90288 of the global pins is identical to that of the MLX90291 (PWM output), making drop-in replacements possible for multi-protocol applications. Both ICs have differences in architecture, apart from the protocol only.

10 Recommended Application Diagram

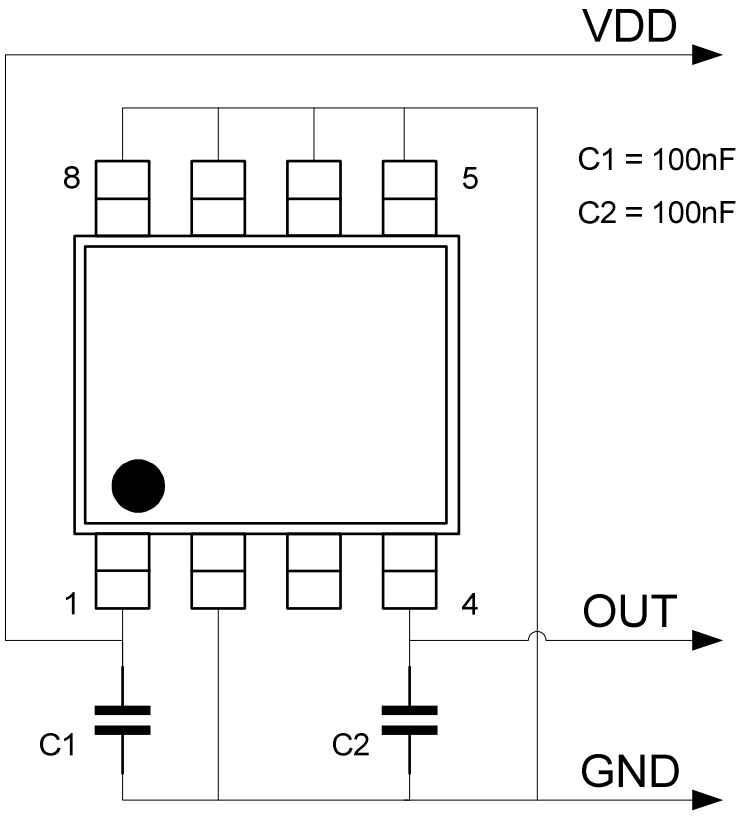

Figure 6: Recommended Application Diagram

The testpins (#5, #6, #7, #8) need to be grounded to avoid the risk of the chip going into testmode because of RF/noise entering the test controller on these pins. The test input pins have an internal pull-down resistor.

The recommended application diagram is not a mandatory design guide. For better ESD and EMC performance external components can be modified for as long as the electrical specifications are followed under Section 5.2. For good EMC performance the components should be placed as close as possible to the IC.

11 Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.
The information furnished by Melexis is believed to be correct and accurate. However, Melexis shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Melexis' rendering of technical or other services.

For the latest version of this document, go to our website at
www.melexis.com

Or for additional information contact Melexis Direct:

Europe, Africa, Asia:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

America:
Phone: +1 248 306 5400
E-mail: sales_usa@melexis.com

ISO/TS 16949 and ISO14001 Certified