

# Video Signal Driver for DVD Player Monolithic IC MM1623XFBE

## Outline

This 6ch video driver IC was developed for use in DVD players/recorders.

The LPF that attenuates the DAC noise element has a built-in switching function to handle both progressive and interlace signals. In addition, the driver structure is 6db, 75Ω x 2 lines.

Also, the number of external ESD protection diodes has been reduced thanks to the S1/S2 DC superimpose function and reinforced output pin ESD protection element.

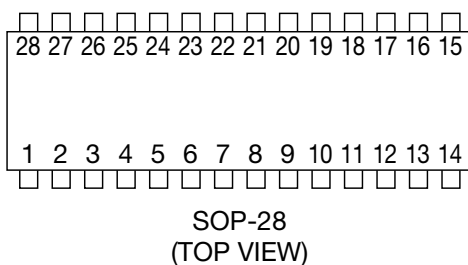
## Features

1. 75W driver can drive 2 lines.
2. S/N=83dB typ.
3. Built-in 6dB amp.
4. Built-in filter switching function for progressive/interlace signal
5. Built-in high performance 4th LPF.
6. 6.75MHz/100kHz max. ±1.0dB 27MHz/100kHz typ. -40dB
7. +/- 15KV ESD for aerial discharge.
8. S1/S2 Built-in DC superimpose function.
9. Control pin allows component circuit to handle RGB signals.

## Package

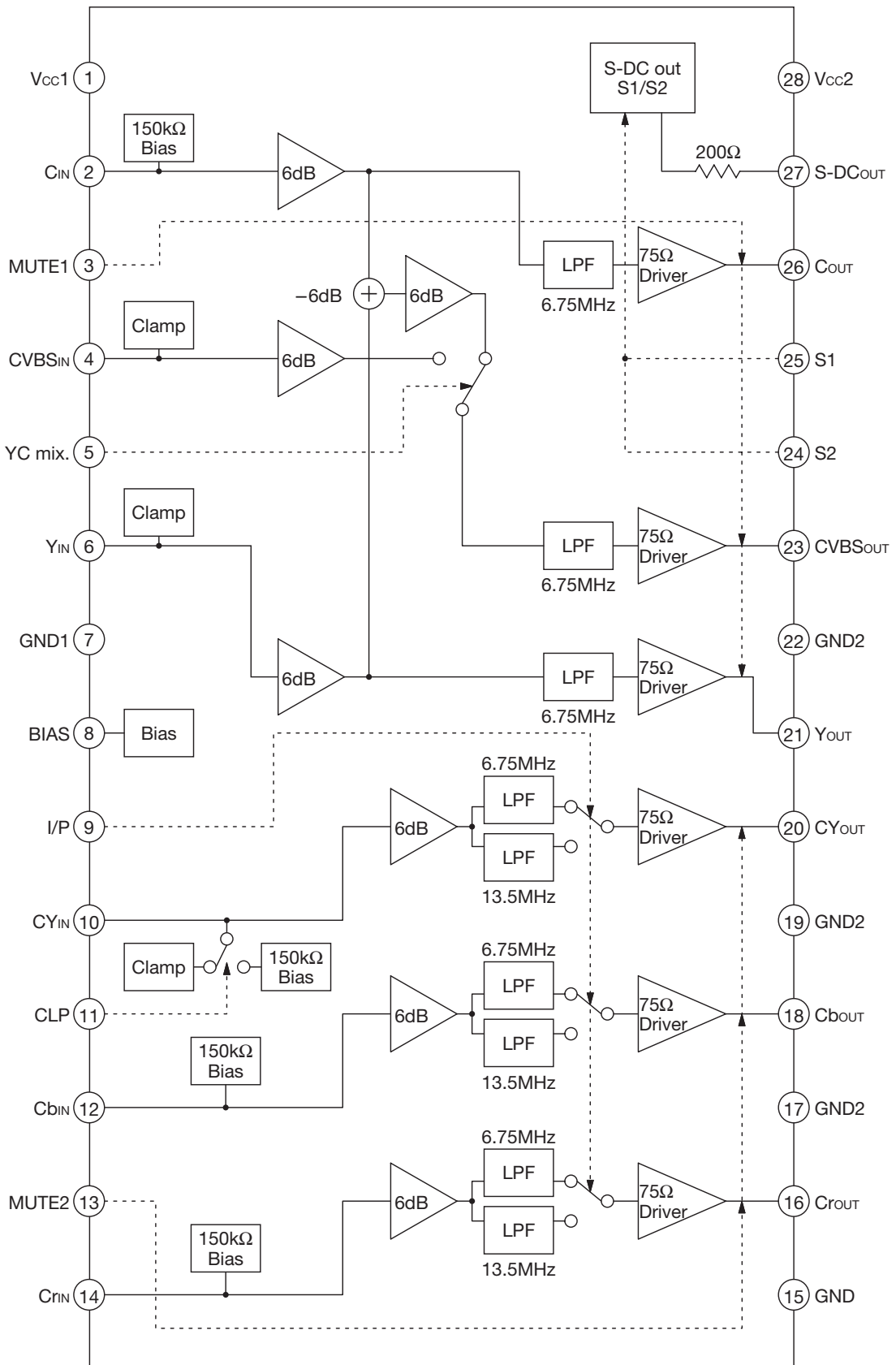
SOP-28

## Pin Assignment



1	V <sub>CC1</sub>	15	GND2
2	C <sub>IN</sub>	16	C <sub>ROUT</sub>
3	MUTE1	17	GND2
4	CVBS <sub>IN</sub>	18	C <sub>bOUT</sub>
5	YC MIX.	19	GND2
6	Y <sub>IN</sub>	20	CY <sub>OUT</sub>
7	GND1	21	Y <sub>OUT</sub>
8	BIAS	22	GND2
9	I/P	23	CVBS <sub>OUT</sub>
10	CY <sub>IN</sub>	24	S2
11	CLP	25	S1
12	C <sub>bIN</sub>	26	C <sub>OUT</sub>
13	MUTE2	27	S-DC <sub>OUT</sub>
14	C <sub>IN</sub>	28	V <sub>CC2</sub>

Block Diagram



Pin Description

Pin no.	Pin name	Function	Internal equivalent circuit diagram
1 28	Vcc1 Vcc2	Vcc Vcc2 is power supply for 75Ω driver.	
2	CIN	Croma signal input	
3 13	MUTE1 MUTE2	Mute select Using of MUTE and POWER-SAVING.	
4 6	CVBSIN YIN	Video signal input (Composite video or Y) Sync tip clamp input	
5	YC mix.	YC MIX select	
7 15 17 19 22	GND1 GND2 GND2 GND2 GND2	GND GND2 is ground for 75Ω driver.	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
8	BIAS	Bias	
9	I/P	Interlace / Progressive select	
10	CY <sub>IN</sub>	Luminance input The input can select Sync tip clamp or Bias.  Input signal : Y or G	
11	CLP	Input clamp select	
12 14	Cb <sub>IN</sub> Cr <sub>IN</sub>	Component input Input signal : Cb or B Cr or R	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
16 18 20 21 23 26	C <sub>OUT</sub> Cb <sub>OUT</sub> CY <sub>OUT</sub> Y <sub>OUT</sub> CVBS <sub>OUT</sub> C <sub>OUT</sub>	Signal output	
24 25	S1 S2	S1/S2 select	
27	S-DC <sub>OUT</sub>	S1/S2 DC output	

**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-65~+150	°C
Operating temperature	T <sub>OPR</sub>	-40~+85	°C
Supply Voltage	V <sub>CC max.</sub>	7	V
Allowable loss *	P <sub>d</sub>	1.4	W

\* Board mounting power dissipation. Board size 100 X100 X1.6mm

**Recommended Operating Conditions**

Item	Symbol	Ratings	Units
Operating temperature	T <sub>OPR</sub>	-40~+85	°C
Operating voltage	V <sub>CCOP</sub>	4.5~5.5	V

**Electrical Characteristics** (Except where noted otherwise, Ta=25°C, V<sub>CC</sub>=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
Supply current 1	I <sub>CC1</sub>	No signal	77	110	143	mA		
Supply current 2	I <sub>CC2</sub>	No signal, Mute1: ON	39	56	73	mA		
Supply current 3	I <sub>CC3</sub>	No signal, Mute2: ON	39	56	73	mA		
Supply current 4	I <sub>CC4</sub>	No signal, Mute1 and Mute2: ON	1	3	5	mA		
Croma input	V <sub>CIN</sub>	2 PIN	1.9	2.4	2.9	V		
Composite video input	V <sub>CVBSIN</sub>	4 PIN	0.9	1.1	1.3	V		
Luminance input	V <sub>YIN, CYIN</sub>	6, 10 PIN	0.9	1.1	1.3	V		
Component input	V <sub>CBIN, CHIN</sub>	12, 14 PIN	1.9	2.4	2.9	V		
Croma output	V <sub>COUT</sub>	26 PIN		2.4		V		
Composite video output	V <sub>CVBSOUT</sub>	23 PIN		1.1		V		
Luminance output	V <sub>YOUT, CYOUT</sub>	21, 20 PIN		1.1		V		
Component output	V <sub>CbOUT, cOUT</sub>	18, 16 PIN		2.4		V		
Control terminal input current	H	I <sub>IHm</sub> (*1)	3, 5, 9, 11, 13, 24, 25 PIN V <sub>H</sub> =4.5V		350	μA		
	L	I <sub>ILm</sub> (*1)	3, 5, 9, 11, 13, 24, 25 PIN V <sub>L</sub> =0.4V		35	μA		
Control terminal input voltage	H	V <sub>thHm</sub> (*1)	2.1			V		
	L	V <sub>thLm</sub> (*1)			0.7	V		
S-DC out terminal output voltage	L	V <sub>DcOUTL</sub>	R <sub>L</sub> =10kΩ+100kΩ		0.1	0.5	V	
	M	V <sub>DcOUTM</sub>	R <sub>L</sub> =10kΩ+100kΩ		1.6	2.1	2.4	V
	H	V <sub>DcOUTH</sub>	R <sub>L</sub> =10kΩ+100kΩ		4.3	4.6	V	
Input impedance	Z <sub>CIN, cBIN, cHIN</sub>	2, 12, 14 PIN	100	150	200	kΩ		
Output impedance	Z <sub>S-DCOUT</sub>	27 PIN		200		Ω		
Voltage gain	G <sub>1n</sub> (*2)	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB		

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Frequency characteristic 1 (C, CVBS, Y)	f <sub>1-5</sub> (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 6.75MHz/100kHz	-1.5	-0.5	0.5	dB
	f <sub>2-5</sub> (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 27MHz/100kHz		-33	-27	dB
Frequency characteristic 2 (CY, Cb, Cr) at Interlace select	f <sub>3-8</sub> (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 6.75MHz/100kHz	-0.5	0.5	1.5	dB
	f <sub>4-8</sub> (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 27MHz/100kHz		-28	-22	dB
Frequency characteristic 3 (CY, Cb, Cr) at Progressive select	f <sub>5-8</sub> (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 13.5MHz/100kHz	-1.5	-0.5	0.5	dB
	f <sub>6-8</sub> (*2)	100 (IRE) SIN wave+40 (IRE) SYNC 54MHz/100kHz		-28	-22	dB
Differential gain	DG <sub>1-3</sub> (*2)	Staircase signal 1V		1.0	1.5	%
Differential phase	DP <sub>1-3</sub> (*2)	Staircase signal 1V		1.0	1.5	°
Output dynamic range	DR <sub>1,4,7,8</sub> (*2)	SIN wave; 100kHz, THD=1.0%	2.6	3.0		V
	DR <sub>2,3,5,6</sub> (*2)	SIN wave; 100kHz, THD=1.0%	2.6	2.8		V
Crosstalk	CT <sub>n</sub> (*2)	f=4.43MHz, 1V		-60	-55	dB
S/N1	SN <sub>14-8</sub> (*2)	BW: 100k~6MHz		-83		dB
S/N2	SN <sub>21-3</sub> (*2)	BW: 100k~6MHz at mix. OUT		-77		dB
Group delay 1	t <sub>1GD1-5</sub> (*2)	at 100kHz		40	80	ns
Group delay 2	t <sub>2GD6-8</sub> (*2)	Interlace select at 100kHz		35	80	ns
Group delay 3	t <sub>3GD6-8</sub> (*2)	Progressive select at 100kHz		22	50	ns
Group delay deviation 1 (C, CVBS Y)	$\Delta$ t <sub>1GD1-5</sub> (*2)	to 3.58MHz		4	10	ns
		to 4.42MHz		6	10	ns
		to 6MHz		12	20	ns
Group delay deviation 2 (CY, Cb Cr) at Interlace select	$\Delta$ t <sub>2GD6-8</sub> (*2)	to 1MHz		1	10	ns
		to 4MHz		4	10	ns
		to 6MHz		10	20	ns
Group delay deviation 3 (CY, Cb Cr) at Progressive select	$\Delta$ t <sub>3GD6-8</sub> (*2)	to 2MHz		1	10	ns
		to 8MHz		4	10	ns
		to 12MHz		10	20	ns
Between channel Group delay deviation 1	$\Delta$ t <sub>1chGD</sub>	Between C and Y at 3.58MHz		1	10	ns
Between channel Group delay deviation 2	$\Delta$ t <sub>2chGD</sub>	Between CY and Cb (Cr) at 1MHz (Interlace)		1	10	ns
Between channel Group delay deviation 3	$\Delta$ t <sub>3chGD</sub>	Between CY and Cb (Cr) at 2MHz (Progressive)		1	10	ns

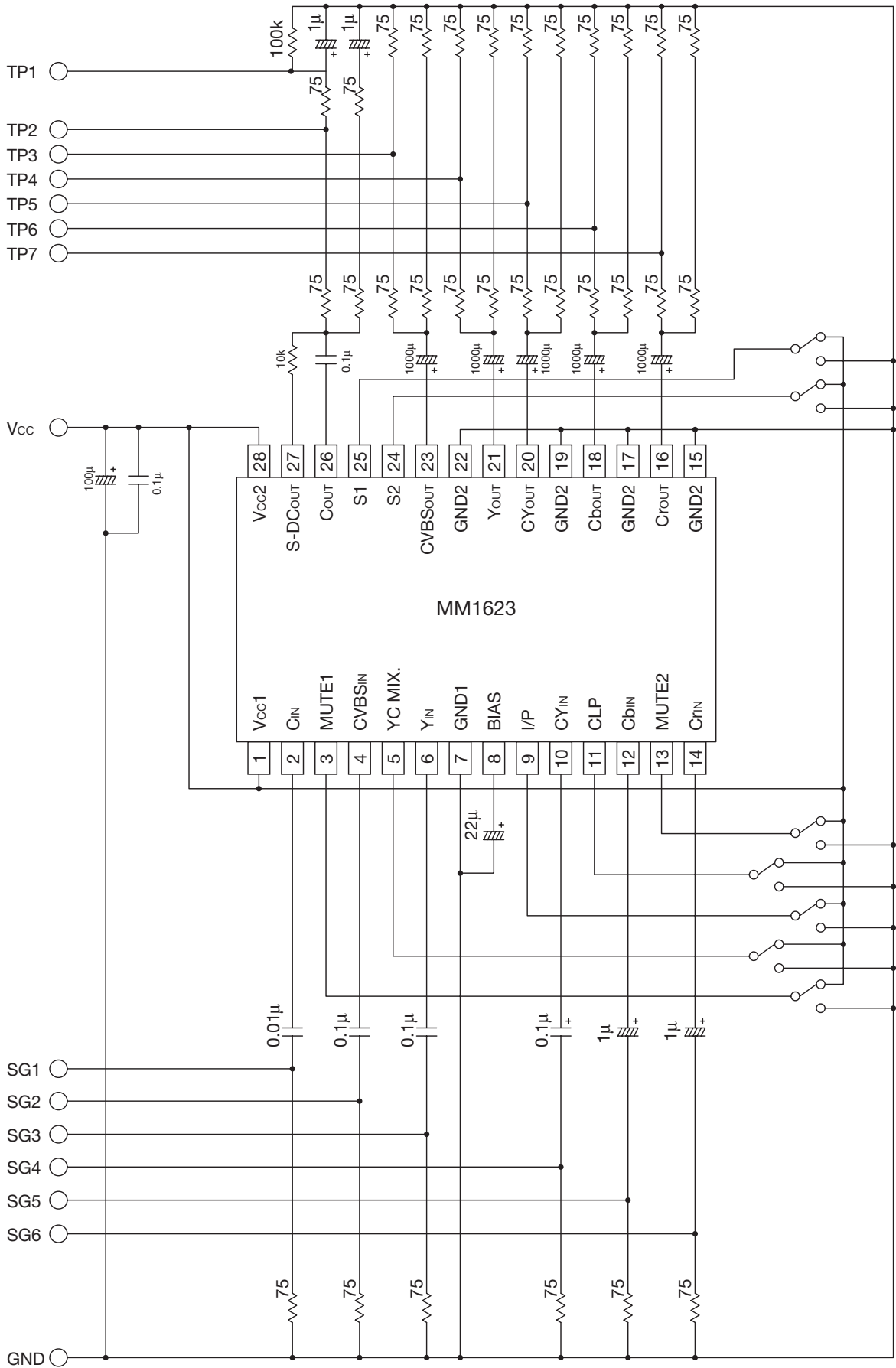
Note: \*1 The subscript number "m" is the terminal of right table.

m	Terminal
1	MUTE1
2	MUTE2
3	YC mix.
4	I/P
5	CLP
6	S1
7	S2

Note: \*2 The subscript number "n" is the combination of right table.

n	Input	Output
1	CIN	CVBSOUT
2	CVBSIN	
3	YIN	
4	CIN	COOUT
5	YIN	YOUT
6	CYIN	CYOUT
7	CbIN	CbOUT
8	CrIN	CrOUT

Measuring Circuit





Switch Control Table

Input select	Output terminal	Control terminal			
		MUTE1	YC MIX.	MUTE2	CLP
MUTE	C <sub>OUT</sub>	Low	*	*	*
C <sub>IN</sub>		High	*	*	*
MUTE	CVBS <sub>OUT</sub>	Low	*	*	*
Y <sub>IN</sub> +C <sub>IN</sub>		High	Low	*	*
CVBS <sub>IN</sub>			High	*	*
MUTE	Y <sub>OUT</sub>	Low	*	*	*
Y <sub>IN</sub>		High	*	*	*
MUTE	CY <sub>OUT</sub>	*	*	Low	*
CY <sub>IN</sub> (CLAMP)		*	*	High	Low
CY <sub>IN</sub> (Bias)		*	*		High
MUTE	Cb <sub>OUT</sub>	*	*	Low	*
Cb <sub>IN</sub>		*	*	High	*
MUTE	Cr <sub>OUT</sub>	*	*	Low	*
Cr <sub>IN</sub>		*	*	High	*

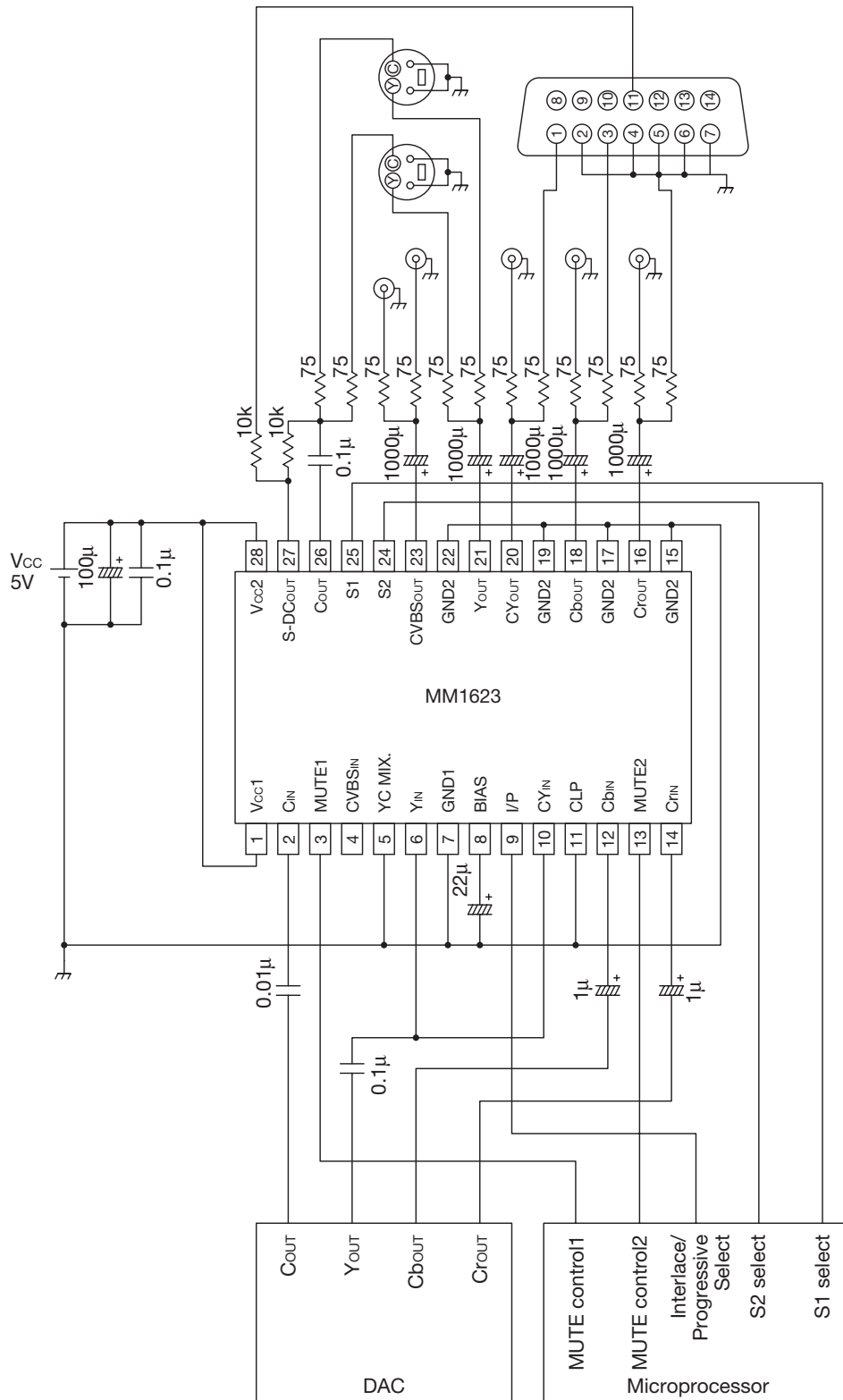
\*: Don't care

Control terminal	Status	CY, Cb, Cr LPF Bandwidth
I/P	Low	13.5MHz (Progressive)
	High	6.75MHz (Interlace)

Control terminal		S-DC <sub>OUT</sub>	Signal Mode
S1	S2	Output Voltage	
Low	Low	0V	4:3 Normal
Low	High	2.1V	4:3 Letter box
High	High		
High	Low	4.6V	16:9 Squeeze

\*: R<sub>L</sub>=10kΩ+100kΩ

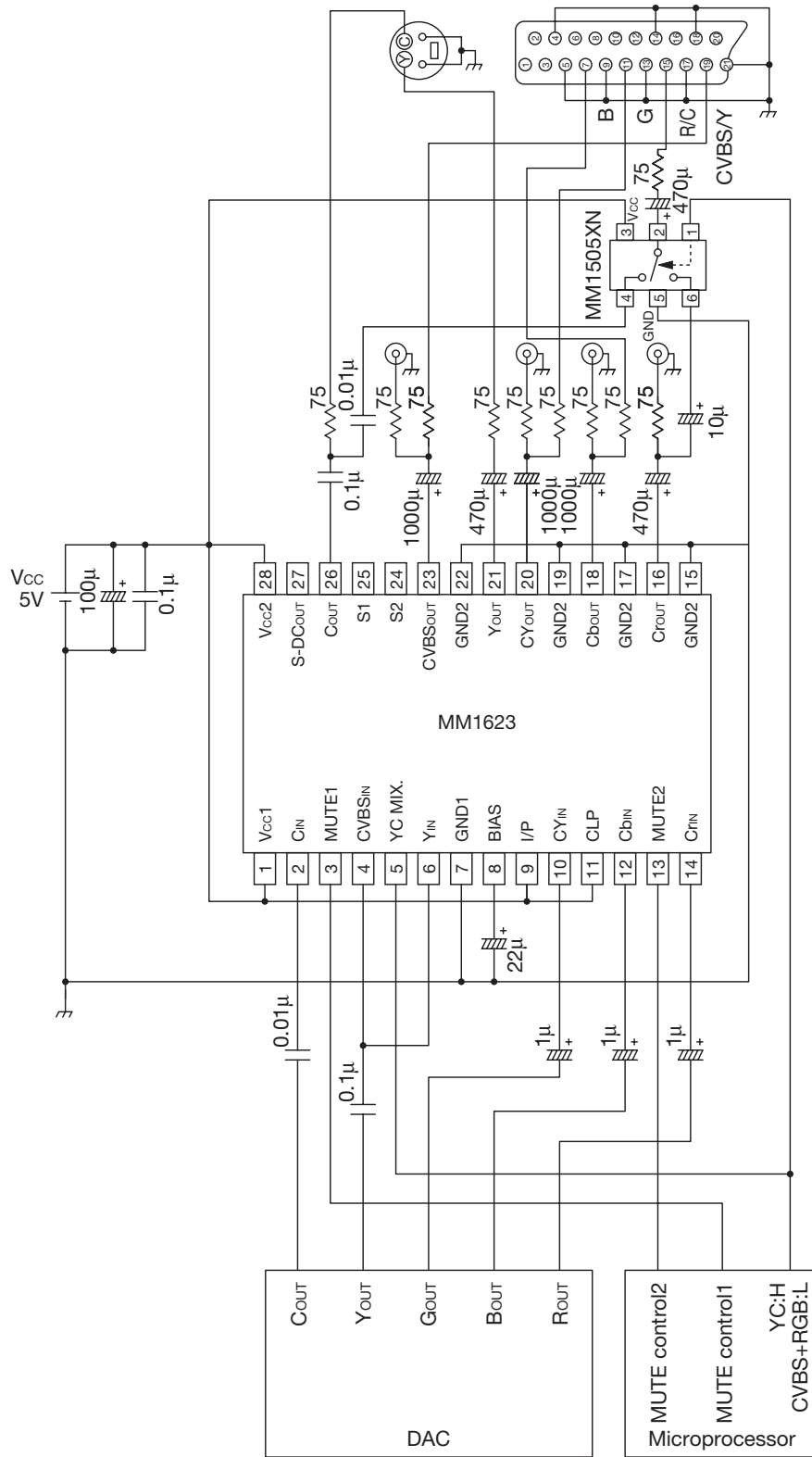
Application Circuit 1



Note 1 Please arrange power supply bypass capacitor near the Vcc2 terminal (28pin).

Note 2 Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

Application Circuit 2

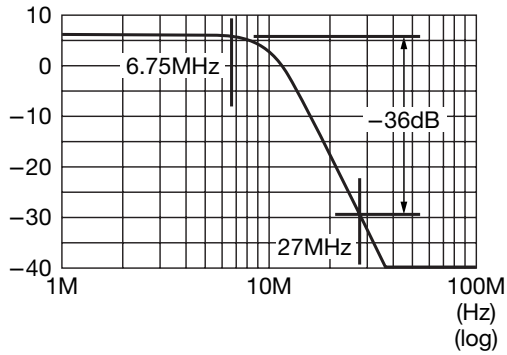


Note 1 Please arrange power supply bypass capacitor near the Vcc2 terminal (28pin).

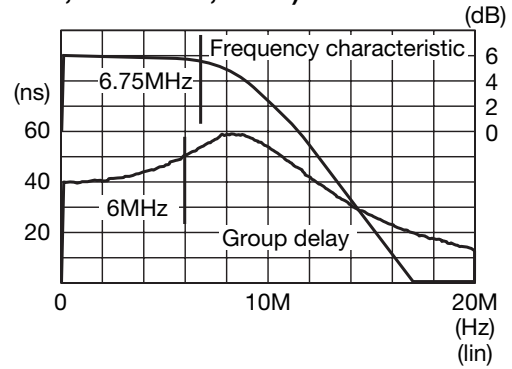
Note 2 Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

**Characteristics**

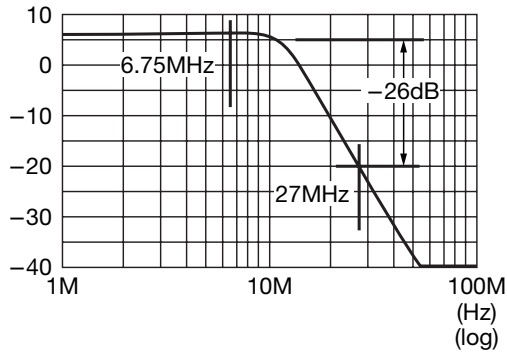
**Frequency characteristic (COUT, CVBSout, Yout)**



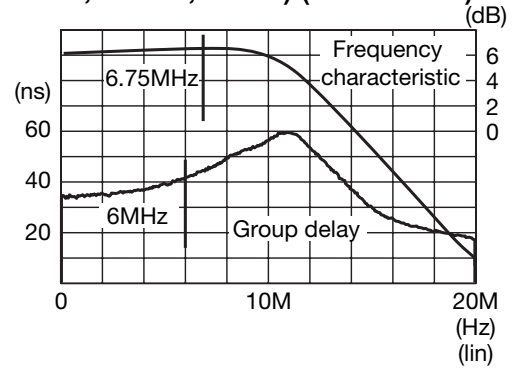
**Group delay (COUT, CVBSout, Yout)**



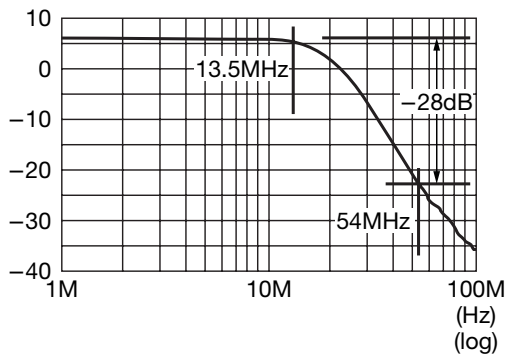
**Frequency characteristic (CYout, Cbout, CrouT) (at Interlace)**



**Group delay (CYout, Cbout, CrouT) (at Interlace)**



**Frequency characteristic (CYout, Cbout, CrouT) (at Progressive)**



**Group delay (CYout, Cbout, CrouT) (at Progressive)**

