Data Sheet

MM32SPIN040C

32-bit Microcontroller Based on Arm®Cortex®-M0

Version：Rev1.07

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1 General Introduction

1.1 Introduction

This product incorporates a high-performance 32-bit microcontroller with Arm® Cortex®-M0 as the core, a LDO regulator with 5V of output voltage, and three sets of integrated PN gate drivers and two operational amplifiers. The highest operating frequency is up to 48MHz. It has built-in high-speed memory, rich I/O ports and peripherals which are connected to the external bus. This product contains one 12-bit ADC, one 16-bit general-purpose timer, one 16-bit basic timer and one 16-bit advanced control timer. It also contains standard communication interfaces: one I2C interface, two UART interfaces and two operational amplifiers.

The operating voltage supported by this product is 7V～36V. The operating temperature range (ambient temperature) includes -40℃～+85℃ industrial type and -40℃ ～ +105℃ extendable type. Multiple power-down modes are provided to ensure the requirements of low-power applications.

Rich peripherals make the microcontroller suitable for a variety of applications:

- Three-phase permanent brushless motor
- Power tools

This product offers TSSOP28 and QFN28 package.

Refer to MM32F0010 User Manual and Errata Sheet for specific instructions.

1.2 Product Characteristics

- Core and system
  - Arm® Cortex®-M0 32 bit MCU
  - Highest operating frequency up to 48MHz
  - Single instruction cycle 32-bit hardware multiplier
- Memory
  - Flash program memory up to 16KB
  - SRAM up to 2KB
  - CRC calculation unit
- Clock, reset, and power management
  - Power supply 2.0V ～ 5.5V
  - Power-on reset/Power down reset (POR/PDR), programmable voltage detector (PVD)
  - POR reset voltage is down to 1.7V
  - PVD voltage threshold can be as low as 1.8V
  - External 2~24MHz high speed crystal oscillator

  - Embedded 48 MHZ high speed oscillator with factory calibration
- Low power
  - Sleep mode, Stop mode and Standby mode
- Six timers
  - One 16-bit 4-channel advanced control timer providing 4-channel PWM output, with dead time generation and emergency stop functions
  - One 16-bit timer providing up to 3 input captures/output compares, which can be used for IR control decoding
  - One 16-bit timer providing one input capture/output compare
  - Two watchdog timers (IWDG and WWDG)
  - One Systick timer: 24-bit downcounter
- Up to three communication interfaces
  - Two UART interfaces
  - One I2C interface
- Up to 10 fast I/O ports
  - All I/O ports can be mapped to 16 external interrupts
  - All ports can input and output V_{DD} signals
- One 12-bit analog-to-digital converter, 1μS transit time (up to 8 input channels)
  - Conversion range: 0~V_{DD}
  - Support the configuration of sampling time and resolution
  - On-chip voltage sensor
- Debug mode
  - Serial wire debug (SWD)
- Triple PN-type half-bridge gate drivers (refer to Chapter 5 of the Datasheet for more information)
  - Working voltage 7V~ 36V
  - Built-in 5V LDO
  - Built-in two operational amplifiers
- Adopt TSSOP28 and QFN28 package

2 Specification

2.1 Model List

2.1.1 Ordering Information

Table 1 Ordering information

Peripheral interface \ Model		MM32SPIN040C
FLASH memory KB		16
SRAM KB		2
Timer	General-purpose (16 bit)	1
	Basic	1
	Advanced	1
Communication interface	UART	2
	I2C	1
Number of GPIO		10
12-bit ADC	Number	1
	Number of channel	5
Operational amplifier		2
CPU frequency		48 MHz
Working voltage		7V ~ 36V
Working temperature		-40℃ ~ +105℃
Package		TSSOP28, QFN28

2.1.2 Marking Information

Figure 1 TSSOP28 package marking

TSSOP package has the following topside marking:

- 1st line: SPIN040C
- 2nd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision
- 3rd line: Company logo+yyww
  - Date code, “yy” means year and “ww” means week in date code

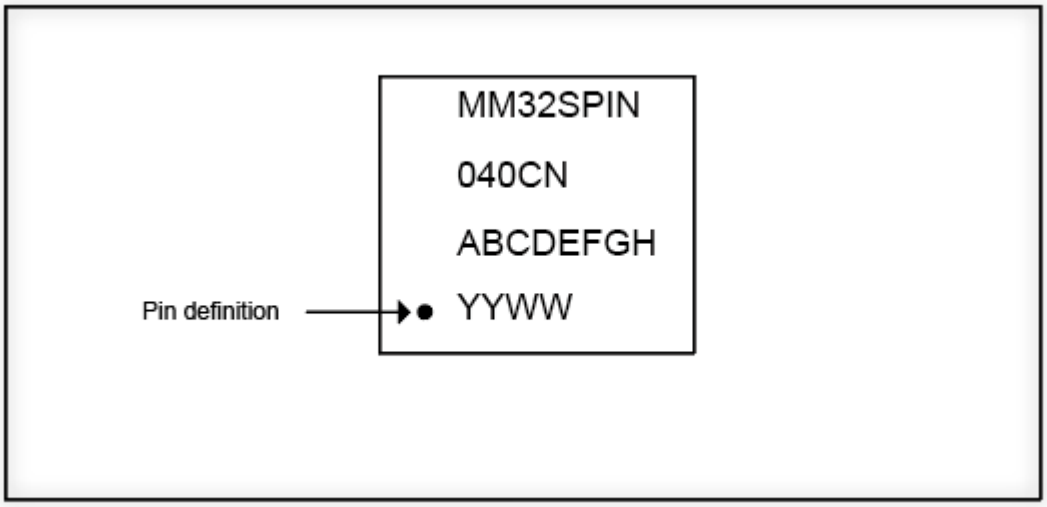

Figure 2 QFN20 package marking

QFN20 package has the following topside marking:

- 1st line and 2nd line: MM32SPIN040CN
- 3rd line: ABCDEFGH
  - Trace code
- 4th line: YYWW
  - Date code, “yy” means year and “ww” means week

2.1.3 System Block Diagram

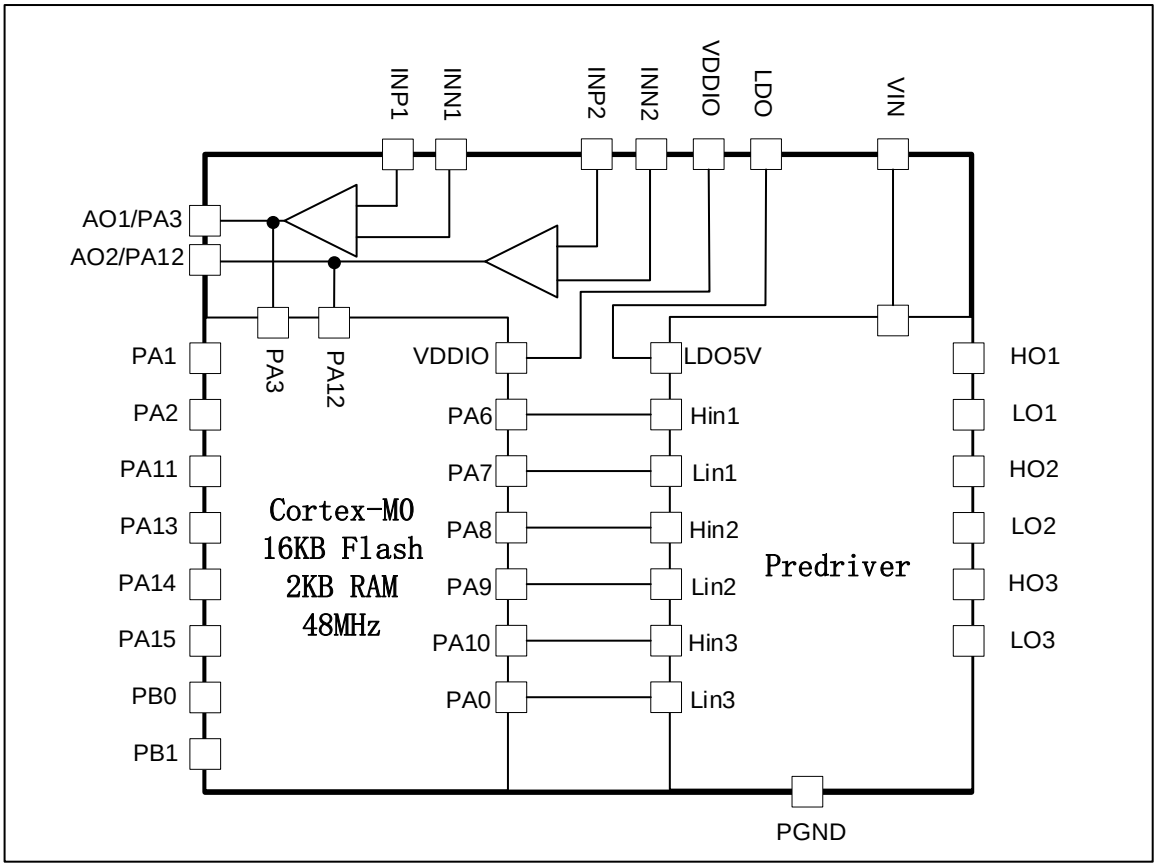

Figure 3 Block diagram

2.2 Functional Description

2.2.1 Core Introduction

The Arm® Cortex®-M0 processor is a configurable and has multilevel pipeline 32-bit reduced instruction set processor, and characterized by high performance and low power consumption.

2.2.2 Memory Mapping

Table 2 Memory mapping

Bus	Address range	Size	Peripheral	Remarks
Flash	0x0000 0000–0x0000 3FFF	16 KB	Mapped to Main Flash memory	
	0x0000 4000–0x07FF FFFF	~ 127 MB	Reserved	
	0x0800 0000–0x0800 3FFF	16 KB	Main Flash memory	
	0x0800 0000–0x1FFD FFFF	~ 383 MB	Reserved	
	0x1FFE 0000–0x1FFE 1BFF	7 KB	Reserved	
	0x1FFE 1C00–0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400–0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800–0x1FFF F80F	16 B	Option bytes	
SRAM	0x2000 0000–0x2000 07FF	2 KB	SRAM	
	0x2000 0700–0x2FFF FFFF	~ 255 MB	Reserved	

Bus	Address range	Size	Peripheral	Remarks
APB1	0x4000 0000–0x4000 03FF	1 KB	Reserved	
	0x4000 0400–0x4000 07FF	1 KB	TIM3	
	0x4000 0800–0x4000 0BFF	1 KB	Reserved	
	0x4000 2800–0x4000 2BFF	1 KB	Reserved	
	0x4000 2C00–0x4000 2FFF	1 KB	WWDG	
	0x4000 3000–0x4000 33FF	1 KB	IWDG	
	0x4000 3400–0x4000 37FF	1 KB	Reserved	
	0x4000 3800–0x4000 3BFF	1 KB	Reserved	
	0x4000 4000–0x4000 43FF	1 KB	Reserved	
	0x4000 4400–0x4000 47FF	1 KB	UART2	
	0x4000 4800–0x4000 4BFF	3 KB	Reserved	
	0x4000 5400–0x4000 57FF	1 KB	I2C1	
	0x4000 5800–0x4000 6BFF	5 KB	Reserved	
	0x4000 6C00–0x4000 6FFF	1 KB	Reserved	
	0x4000 7000–0x4000 73FF	1 KB	PWR	
	0x4000 7400–0x4000 FFFF	35 KB	Reserved	
APB1	0x4001 0000–0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400–0x4001 07FF	1 KB	EXTI	
	0x4001 0800–0x4001 23FF	7 KB	Reserved	
	0x4001 2400–0x4001 27FF	1 KB	ADC1	
	0x4001 2800–0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00–0x4001 2FFF	1 KB	TIM1	
	0x4001 3000–0x4001 33FF	1 KB	SPI1	
	0x4001 3400–0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800–0x4001 3BFF	1 KB	UART1	
	0x4001 3C00–0x4001 3FFF	1 KB	Reserved	
	0x4001 4000–0x4001 43FF	1 KB	TIM14	
	0x4001 4400–0x4001 47FF	1 KB	Reserved	
	0x4001 4800–0x4001 4BFF	1 KB	Reserved	
	0x4001 4C00–0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000–0x4002 03FF	1 KB	Reserved	
	0x4002 0400–0x4002 0FFF	3 KB	Reserved	
	0x4002 1000–0x4002 13FF	1 KB	RCC	
	0x4002 1400–0x4002 1FFF	3 KB	Reserved	
	0x4002 2000–0x4002 23FF	1 KB	Flash Interface	
	0x4002 2400–0x4002 2FFF	3 KB	Reserved	
	0x4002 3000–0x4002 33FF	1 KB	CRC	
	0x4002 3400–0x47FF FFFF	~ 127 MB	Reserved	
	0x4800 0000–0x4800 03FF	1 KB	GPIOA	

Bus	Address range	Size	Peripheral	Remarks
	0x4800 0400–0x4800 07FF	1 KB	GPIOB	
	0x4800 0800–0x4800 0BFF	1 KB	Reserved	
	0x4800 0C00–0x4800 0FFF	1 KB	Reserved	
	0x4800 1000–0x5FFF FFFF	~ 384 MB	Reserved	

2.2.3 Embedded Flash Memory

Embedded flash memory up to 16KB for storing programs and data.

2.2.4 Embedded SRAM

Embedded SRAM up to 2KB.

2.2.5 Cyclical Redundancy Check Computing Unit (CRC)

The CRC (Cyclic Redundancy check) computing unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. The CRC-based technology is used to verify the consistency of data transfer or storage in its numerous applications. Within the scope of the EN/IEC60335-1 standard, it provides a method of detecting flash memory errors. CRC computing unit can be used to calculate the software signature in real time and compare it to the signature generated when linking to and generating the software.

2.2.6 Nested Vectored Interrupt Controller (NVIC)

This product has a built-in nested vectored interrupt controller, which can process multiple maskable interrupting channels (excluding 16 Cortex®-M0 interrupt lines) and 4 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry addresses directly enters into the core
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Handle higher-priority interrupts that arrive late
- Support tail link of interrupts
- Automatically save the processor state
- Offer automatic recovery when the interrupt returns with no additional instruction

This module provides flexible interrupt management with minimal interrupt latency.

2.2.7 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains multiple edge detectors which are used to capture level changes from IO pins so as to generate interrupt/event requests. All IO pins can be connected to 16 external interrupt line. Each interrupt line can be independently configured with its trigger event (rising edge or falling edge or double edge) and can be screened separately. A pending register maintains the states of all interrupt requests.

EXTI can detect level changes with pulse widths less than the internal AHB bus clock period.

2.2.8 Clock and Startup

Multiple prescalers are used to configure the frequency of the AHB, and the high-speed APB area. The maximum frequency of the AHB and the high-speed APB is 48MHz. Refer to the figure below for the clock tree.

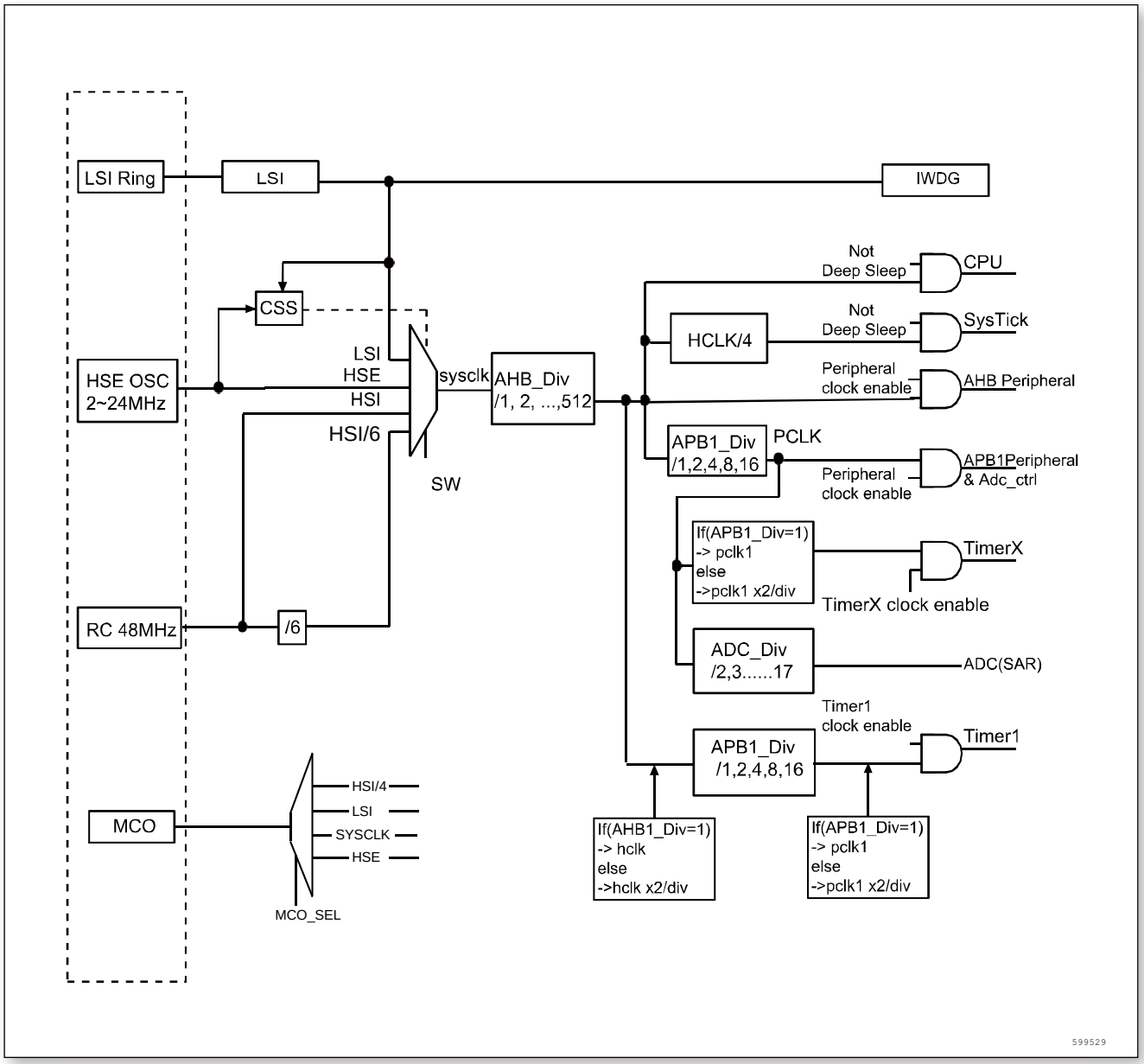

Figure 4 Clock tree

2.2.9 Power Supply Schemes

V_{DD} = 2.0V ~ 5.5V: power supply for I/O pins and the internal regulator via V_{DD} pin.

2.2.10 Power Supply Supervisors

This product is integrated with power on reset (POR)/power down reset (PDR) circuit. The circuit remains in the working state to ensure the system works when the power supply exceeds 2.0V. When V_{DD} is below the set threshold ($V_{POR/PDR}$), the device will be placed in the reset state. An external reset circuit is not necessary.

Additionally, there is a programmable voltage monitor (PVD) in the device that monitors the

V_{DD} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, the device will be interrupted. The interrupt handler will send a warning message or switch the microcontroller to safe mode. The PVD function should be enabled by a program.

2.2.11 Voltage Regulator

The on-chip voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.12 Low Power Mode

The product supports low power mode to achieve the best compromise among low power, short startup time, and multiple wake-up events.

Table 3 Low power mode list

Mode	Entry	Wake-up	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator
Sleep Mode (SLEEP NOW or SLEEP ON EXIT)	WFI (Wait for Interrupt)	Any arbitrary interrupt	CPU clock off, no influence on other clock and ADC clock	Off	On
	WFE (Wait for Event)	Wake-up event			
Stop Mode	PDDS=0 LPDS =0 OR 1 (1); SLEEPDEEP= 1; WFI or WFE;	Any arbitrary interrupt (set in the external interrupt register)	All 1.5V area clocks are off	HSI and HSE oscillator off	On
Standby Mode	PDDS=1; SLEEPDEEP= 1 WFI or WFE;	te rising edge on WKUP pin, the external reset on NRST pin, IWDG reset			Off

1) Lower power consumption can be obtained when LPDS = 1, please refer to Table 5 for details.

Table 4 Table of IP states corresponding to different power consumption modes

Module/Mode	Run	Sleep	Stop (LPDS=0)	Stop (LPDS=1)	Standby
RCC	ON	ON	ON	ON	Power Down
EXTI	ON	ON	ON	ON	Power Down
CORTEXM0	ON	OFF	OFF	OFF	Power Down
UARTx	Optional	Optional	OFF	OFF	Power Down
I2Cx	Optional	Optional	OFF	OFF	Power Down
WWDG	Optional	Optional	OFF	OFF	Power Down
SPIx	Optional	Optional	OFF	OFF	Power Down
CRC	Optional	Optional	OFF	OFF	Power Down

Module/Mode	Run	Sleep	Stop (LPDS=0)	Stop (LPDS=1)	Standby
TIMERx	Optional	Optional	OFF	OFF	Power Down
FLASH	ON	Standby	Standby	Deep Standby	Power Down
SRAM	ON	ON	Retention	Retention	Power Down
HSE (2-24MHz)	Optional	Optional	OFF	OFF	OFF
HSI RC 48M	ON	Optional	ON	ON	Power Down
LSI RC (40Khz)	Optional	Optional	Optional	Optional	Optional
IWDG	Optional	Optional	Optional	Optional	Optional
PVD	Optional	Optional	Optional	Optional	OFF
PWR	ON	ON	ON	ON	ON
ADC	Optional	Optional	OFF	OFF	OFF
GPIO_CTRL	Optional	Optional	Optional	Optional	Power Down
IO	ON	ON	ON	ON	ON

1) Power Down: The module is powered down and data is lost
2) Optional: The software can be configured on or off
3) ON: working
4) OFF: function off
5) Retention: Data is retained but inoperable

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

The Stop mode permits to achieve the lowest power consumption while keeping the SRAM and register contents intact. In the Stop mode, the HSI oscillator and the HSE crystal oscillator are switched off. The microcontroller can wake up from the Stop mode by any signal configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of PVD.

Standby mode

The Standby mode is used to achieve the lowest power consumption. In the Standby mode, the voltage regulaor is switched off when the CPU is in the deep sleep mode. All internal power supply areas in the 1.5V section are disconnected. HSI and HSE oscillators are turned off and can be woken up by the rising edge of WKUP pin, external reset of NRST pin, and IWDG reset. They can also be woken up and reset by the watchdog timer. The contents of SRAM and registers will be lost.

2.2.13 TIM & WDG

The device includes one advanced control timer, one general-purpose timer, one basic timer, two watchdog timers and one SysTick timer.

The table below compares the features of the advanced control, general-purpose and basic timers:

Table 5 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	Capture/compare channels	Complem -entary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Interger from 1 ~ 65536	4	Yes
General-purpose	TIM3	16-bit	Up, down, up/down	Interger from 1 ~ 65536	4	No
Basic	TIM14	16-bit	Up	Interger from 1 ~ 65536	No	No

Advanced-control timer (TIM1)

Advanced-control timer is composed of one 16-bit counter, 4 capture/compare channels and three-phase complementary PWM generator. It has complementary PWM outputs with dead time insertion and can also be used as a complete general-purpose timer. The four independent channels can be used for：

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

When it is configured as a 16-bit general-purpose timer, it has the same function as the TIM3 timer. When it is configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In the debug mode, the counter can be frozen and the PWM output is disabled. Therefore, switches controlled by these outputs are cut off.

Many features are shared with those of the general-purpose timers which have the same architecture, the advanced-control timer can therefore work together with the TIM timer via the Timer Link feature for synchronization or event chaining.

General-purpose timer (TIM3)

The product has a built-in general-purpose timer (TIM3) that can run synchronously. This timer has one 16-bit auto-load up/down counter, one 16-bit prescaler and three independent channels. Each channel can be used for input capture, output compare, PWM and single-pulse mode output.

The timers can work together with the advanced control timer via the Timer Link feature for synchronization or event chaining. The counters can be frozen in debug mode. Any general-purpose timer can be used to produce PWM output. Each timer has an independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1

to 3 Hall sensors. Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

Basic timer (TIM14)

This timer is based on one 16-bit auto-reload upcounter and one 16-bit prescaler. It has a single channel for input capture/output compare, PWM or single pulse mode output. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on one 12-bit downcounter and one 8-bit prescaler. It is clocked from an independent 40 KHz internal clock oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used to reset the system when a problem occurs, or as a free running timer for application timeout management. It can be configured to software or hardware enable wachdog through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog has one 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the entire system when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard down counter. It features:

- One 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.14 Universal Asynchronous Receiver/Transmitter (UART)

UART supports LIN master-slave function and it is compatible with ISO7816 smart card mode. The supported length of output data from UART interface can be configured for 5 bit, 6 bit, 7 bit, 8 bit, and 9 bit. The largest baud rate can be 3Mbps.

2.2.15 I2C Bus

The I2C interface can operate in the multi-master or mode slave mode and it supports Standard Mode and Fast Mode.

The I2C interface supports 7-bit and 10-bit addressing.

The slave mode supports multiple address response.

2.2.16 SPI Interface

The SPI interface can be configured as 1 ~ 32 bits per frame in the slave or master mode. SPI supports up to 24MHz clock frequency in the master mod and 12 MHz clock frequency in the slave mode.

2.2.17 General-purpose Inputs/Outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as alternate peripheral function port. Most of the GPIO pins are shared with digital or analog alternate peripherals.

The peripheral function of the I/O pin can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.18 Analog-to-digital Converter (ADC)

The device embeds one 12-bit analog-to-digital converter (ADC), with up to 8 external channels available for single shot, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog input.

The analog watchdog allows the application to monitor one or all selected channels precisely. An interrupt occurs when the monitored signal exceeds a preset threshold.

Events generated by general-purpose timer (TIM3) and advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize ADC conversion with the clock.

2.2.19 Serial Wire Debug (SWD)

The device embeds an Arm standard two-wire serial debug interface (SW-DP).

Arm SW-DP interface allows connection to the microcontroller via the serial wire debug tool.

3 Pin Definition and Alternate Function

3.1 Pinout Diagram

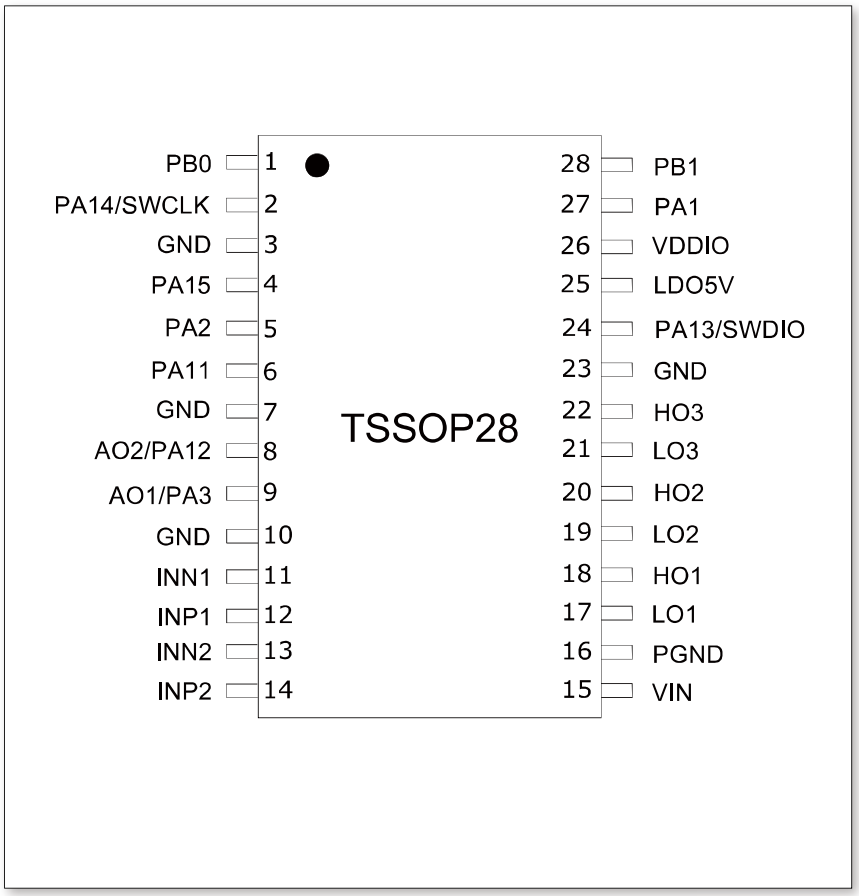

Figure 5 TSSOP28 pinout diagram

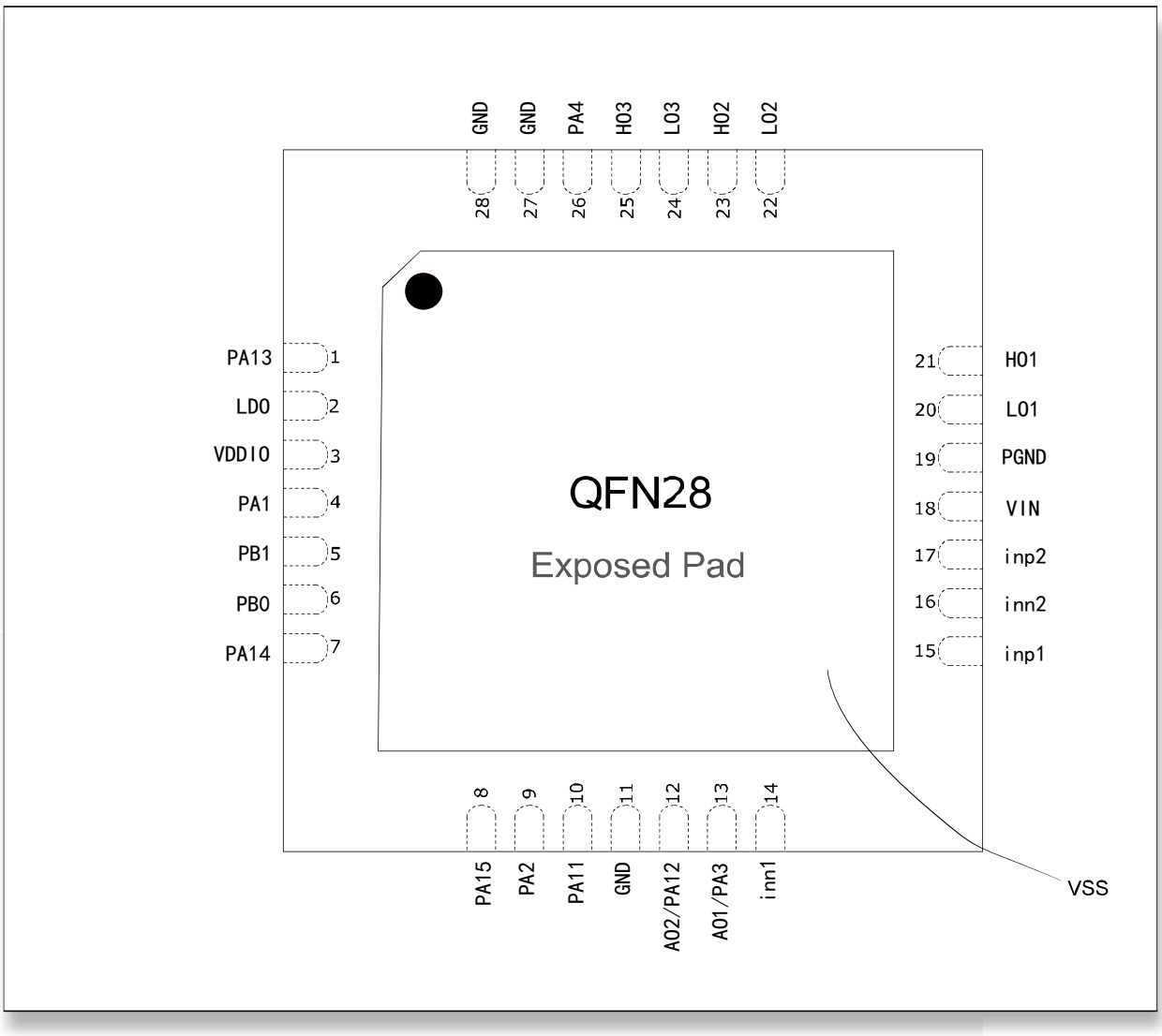

Figure 6 QFN28 pinout diagram

3.2 Pin Assignment Table

Table 6 Pin assignment table

Pin ID		Name	Type (1)	I/O level(2)	Main function	Alternate function	Additional function
QFN28	TSSOP28						
6	1	PB0 OSC_IN	I/O	TC	PB0		ADC1_VIN[1]
7	2	PA14	I/O	TC	PA14	SWDCLK/ UART1_TX	nRST(3)
27	3	VSS	S		VSS		
8	4	PA15	I/O	TC	PA15	SPI_NSS TIM1_CH3N TIM3_CH3	ADC1_VIN[6]
9	5	PA2	I/O	TC	PA2	TIM1_CH2N TIM3_CH2	ADC1_VIN[5]
10	6	PA11	I/O	TC	PA11	TIM1_CH2 TIM14_CH1/ TIM3_CH1	ADC1_VIN[4]

11	7	VSS	S		VSS		
12	8	AO2/PA12	I/O	TC	PA12	UART1_TX	ADC1_VIN[3]
13	9	AO1/PA3	I/O	TC	PA3	UART1_RX	ADC1_VIN[2]
	10	VSS	S		VSS		
14	11	INN1	I	-	INN1		
15	12	INP1	I	-	INP1		
16	13	INN2	I	-	INN2		
17	14	INP2	I	-	INP2		
18	15	VIN	S	-	VIN		
19	16	PGND	S	-	PGND		
20	17	LO1	-	-	LO1		
21	18	HO1	-	-	HO1		
22	19	LO2	-	-	LO2		
23	20	HO2	-	-	HO2		
24	21	LO3	-	-	LO3		
25	22	HO3	-	-	HO3		
26		PA4	I/O	TC	PA4	TIM1_BKIN I2C_SDA	
28	23	VSS	S		VSS		
1	24	PA13	I/O	TC	PA13	SWDIO UART1_RX UART2_RX I2C1_SCL	
2	25	LDO	S		LDO-5V		
3	26	VDDIO	S		VDD		
4	27	PA1	I/O	TC	PA1	UART2_TX I2C1_SDA	
5	28	PB1 OSC_OUT	I/O	TC	PB1		ADC1_VIN[0]
		PA0	I/O	TC	PA0	TIM1_CH3N	
		PA6	I/O	TC	PA6	TIM1_CH1	
		PA7	I/O	TC	PA7	TIM1_CH1N	
		PA9	I/O	TC	PA9	TIM1_CH2N	
		PA8	I/O	TC	PA8	TIM1_CH2	
		PA10	I/O	TC	PA10	TIM1_CH3	

1) I = input, O = output, S = power pins, HiZ = high resistance
2) TC: standard IO, input signal level should not exceed V_{DD}
3) When the SFT_NRST_RMP bit of RCC_SYSCFG is set to 1, the PA14 is mapped to an external reset of nRST and the reset is held low for at least 4us.

3.3 Multiplex Function Table

Table 7 Multiplex function for PA port

Pin	AF0	AF1	AF2	AF3	AF4
PA0	SPI1_NSS	UART1_RX	TIM1_CH3N	I2C1_SCL	TIM3_CH3

Pin Definition and Alternate Function

PA1			UART2_TX	I2C1_SDA	
PA2			TIM1_CH2N		TIM3_CH2
PA3		UART1_RX			
PA4			TIM1_BKIN	I2C1_SDA	
PA6	SPI1_MOSI	TIM1_CH1	TIM1_CH1N		TIM1_CH3
PA7	SPI1_MISO	TIM1_CH1N	TIM1_CH2N	MCO	TIM1_CH4
PA8	SPI1_SCK	TIM1_CH2			TIM3_CH1
PA9	SPI1_MOSI	TIM1_CH2N	TIM1_CH1	TIM14_CH1	
PA10	SPI1_MISO	TIM1_CH3	TIM1_CH2		
PA11			TIM1_CH2	TIM14_CH1	TIM3_CH1
PA12		UART1_TX			
PA13	SWDIO	UART1_RX	UART2_RX	I2C1_SCL	
PA14	SWDCLK	UART1_TX			
PA15	SPI_NSS	TIM1_CH3N			TIM3_CH3

Table 8 Gate Driver pin description

Pin number		**Pin name**	**Pin function**
QFN28	**TSSOP28**		
12	8	AO2	OP2 output is connected to PA12. When used as an ADC, it cannot be sampled directly, but needs to be connected to a voltage follower or an amplifier circuit for sampling.
13	9	AO1	OP1 output is connected to PA3. When used as an ADC, it cannot be sampled directly, but needs to be connected to a voltage follower or an amplifier circuit for sampling.
14	11	INN1	OP1 negative input
15	12	INP1	OP1 positive input
16	13	INN2	OP2 negative input
17	14	INP2	OP2 positive input
18	15	VIN	Power input, 1uF capacitor needs to be connected to GND
19	16	PGND	Gate driver's GND
20	17	LO1	The lower bridge arm output 1 of the gate driver, whose input corresponds to PA7
21	18	HO1	The higher bridge arm output 1 of the gate driver, whose input corresponds to PA6
22	19	LO2	The lower bridge arm output 2 of the gate driver, whose input corresponds to PA9
23	20	HO2	The higher bridge arm output 2 of the gate driver, whose input corresponds to PA8
24	21	LO3	The lower bridge arm output 3 of the gate driver, whose input corresponds to PA0
25	22	HO3	The higher bridge arm output 3 of the gate driver, whose input corresponds to PA10
2	25	LDO5V	5V LDO output to supply the internal VDD power supply 5V system. 1uF and 0.1uF capacitors are needed to be connected to GND

3.4 Functional Block Diagram

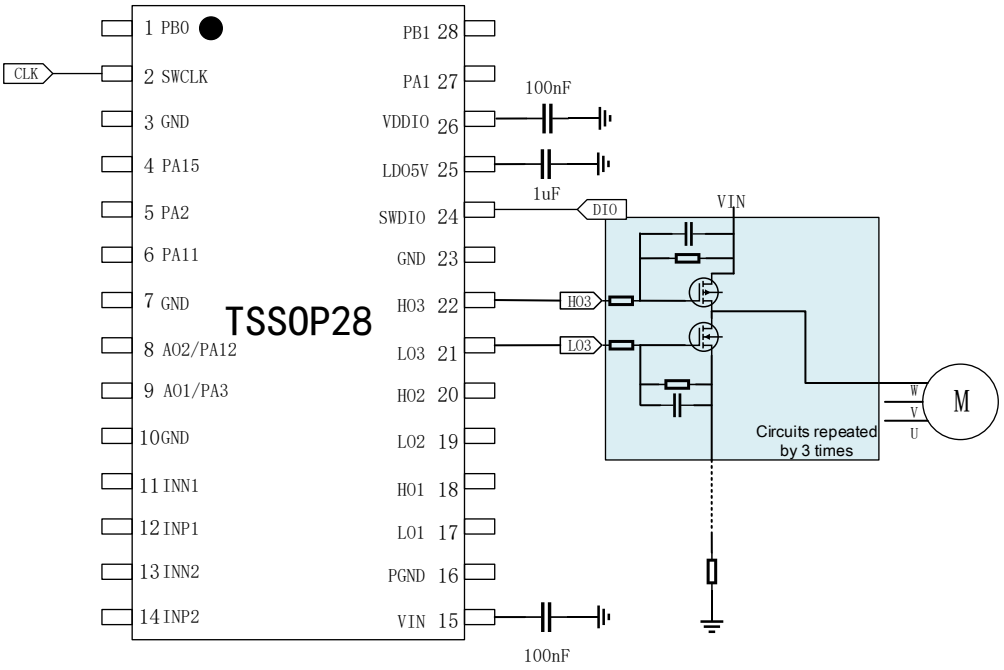

Figure 7 Functional block diagram

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Load Capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

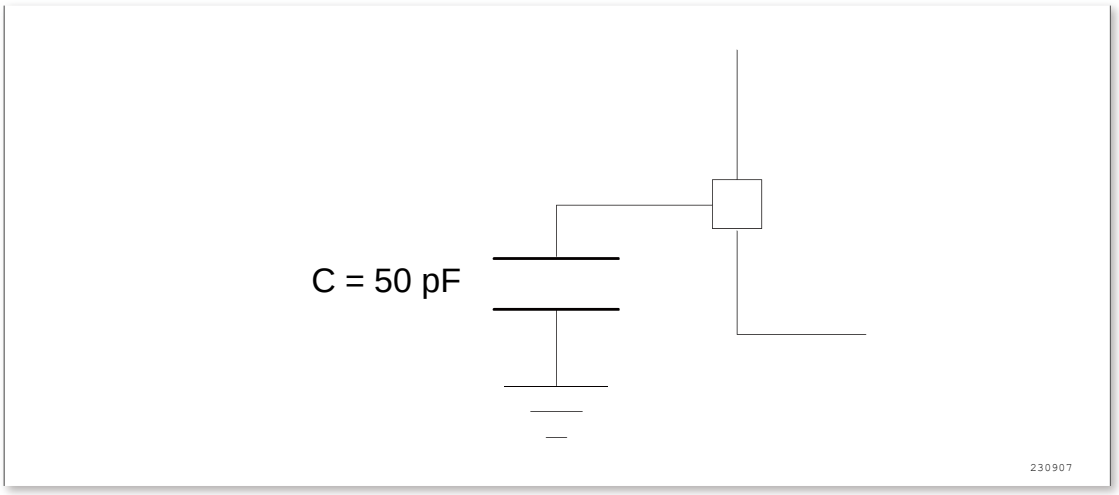

Figure 8 Pin loading conditions

4.1.2 Pin Input Voltage

The input voltage measurement on a pin is described in the figure below.

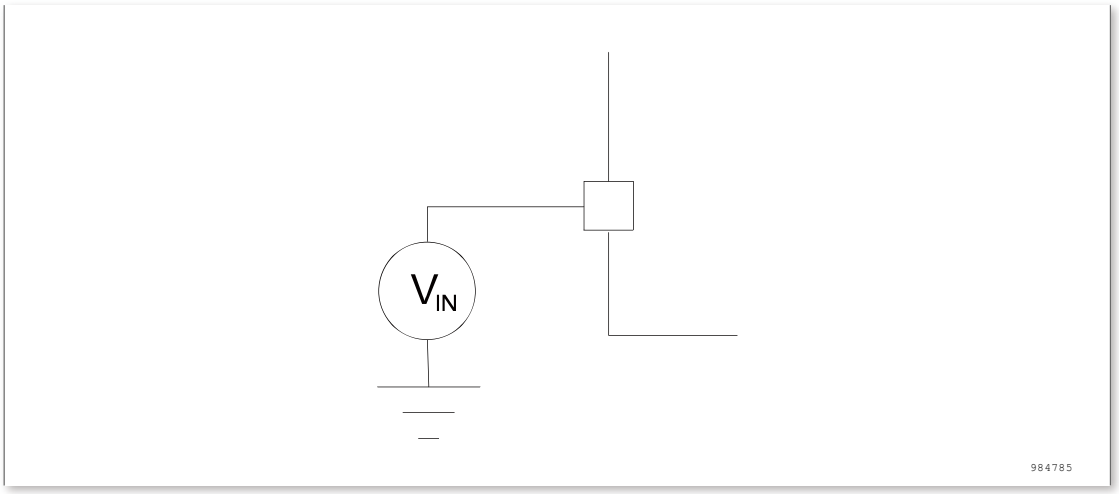

Figure 9 Pin input voltage

4.1.3 Power Supply Scheme

The power supply scheme is shown in the figure below.

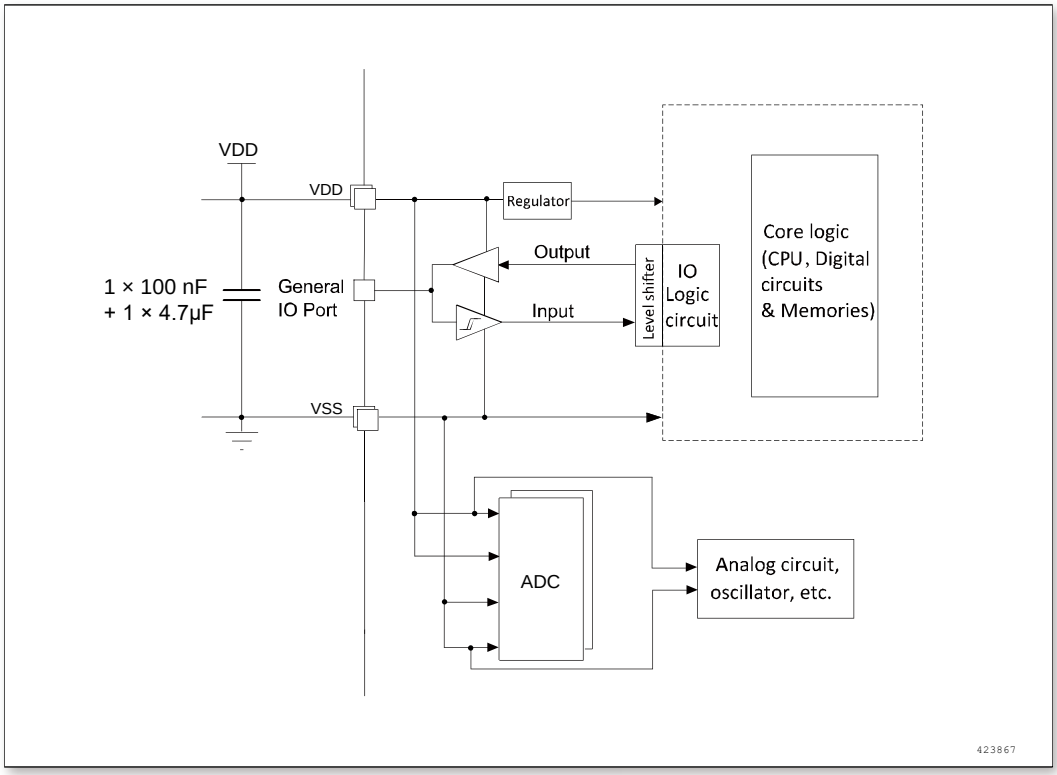

Figure 10 Scheme of power supply

4.1.4 Current Consumption Measurement

The current consumption measurement on a pin is shown in the figure below.

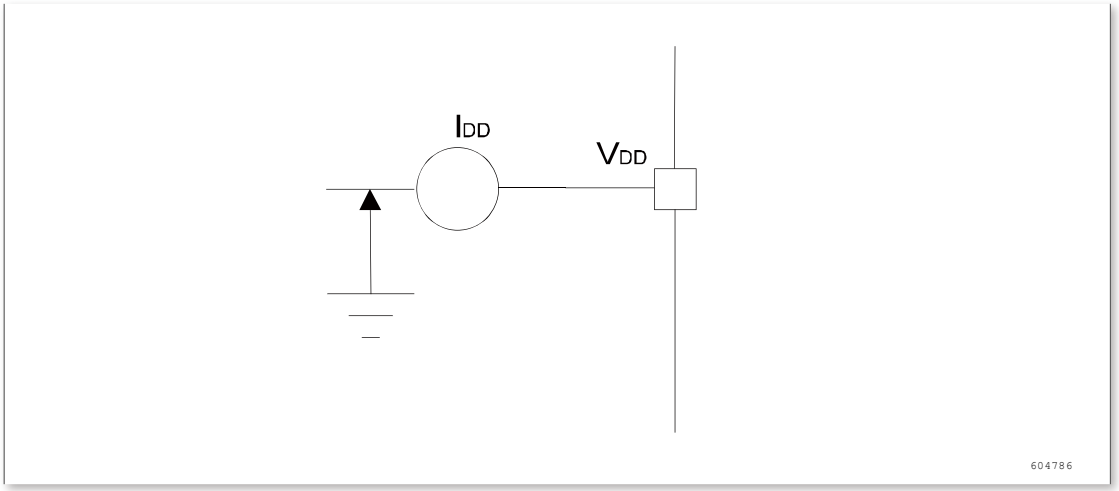

Figure 11 Current consumption measurement scheme

4.2 Absolute Maximum Ratings

Stresses above “the absolute maximum ratings” listed in (Table 10 and Table 11) may cause permanent damage to the device. These are stress maximum ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9 Voltage characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (1)	- 0.3	5.8	V
V_{IN}	Input voltage on other pins (2)	Vss-0.3	V_{DD}+0.3	

1) All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.
2) V_{IN} maximum must always be respected. Refer to the table below for the maximum allowed injected current values.

Table 10 Current characteristics

Symbol	Parameter	Min	Max	Unit
I_{VDD}	Total current into sum of all V_{DD} power lines (source) (1)	-	+60	mA
I_{VSS}	Total current out of sum V_{SS} ground lines (sink) (1)	-	-60	
I_{IO}	Output current sunk by any I/O and control pins	-	+25	
	Output current sunk by any I/O and control pins	-	-25	
$I_{INJ\ (PIN)}$ (2) (3)	Injected current on NRST pin	-	±5	
	Injected current on OSC_IN pin of HSE	-	±5	
$\sum I_{INJ\ (PIN)}$ (4)	Total injected current on other pins	-	±25	

1) All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supplies, in the permitted range.
2) $I_{INJ\ (PIN)}$ must never exceed its limit, i.e. ensure that V_{IN} does not exceed its maximum value. If V_{IN} cannot be ensured to not exceed its maximum value, then $I_{INJ\ (PIN)}$ must be guaranteed to not be externally limited to its maximum value. When $V_{IN} > V_{DD}$, a positive injected current is induced; when $V_{IN} < V_{SS}$, a negative injected current is induced.
3) The negative injected current will interfere with the analog performance of the device.
4) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). The result is based on the characteristic of the maximum value of $\Sigma I_{INJ\ (PIN)}$ on all I/O ports of the device.

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 11 General operating conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	-	48	MHz

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	48	
V_{DD}	Standard working voltage	-	2.0	-	5.5	V
P_D	Power dissipation Temperature: T_A = 105℃ (1)	QFN28		377.4		mW
		TSSOP28		307.7		
T_A	T_A=85℃	Maximum power dissipation	-40	-	85	℃
	T_A=105℃	Maximum power dissipation	-40	-	105	℃
T_J	Junction temperature range (2)	Extendable (T_A=105℃)	-40	-	125	℃

1) If T_A is low, higher PD values are allowed as long as T_J does not exceed T_{Jmax}.

2) At lower states of power dissipation, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

4.3.2 Operating Conditions at Power-up/Power-down

The parameters given in table below are derived from tests performed under the general operating conditions.

Table 12 Operating conditions at power-up/power-down (1) (2)

Symbol	Conditions	Min	Typical	Max	Unit
t_{VDD}	V_{DD} rise time t_r	10	-	500000	us
	V_{DD} fall time t_f	50	-	∞	
V_{ft} (3)	Threshold voltage at power-down	-	0	-	mV

1) Drawn by comprehensive evaluation, not tested in production.

2) The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phases in the following waveform diagram, and no power-down is allowed during power-on process.

3) Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

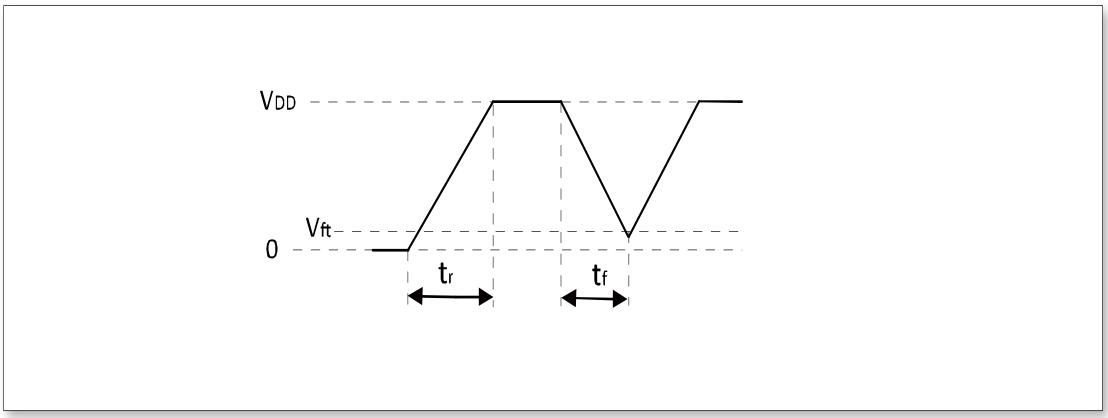

Figure 12 Power-up and power-down waveform

4.3.3 Embedded Reset and Power Control Block Characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and VDD supply voltage conditions listed in Table 11.

Table 13 Embedded reset and power control block characteristics (1)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{PVD}	Level selection of the programmable voltage detector	PLS[3:0]=0000 (rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (falling edge)	-	1.7	-	
		PLS[3:0]=0001 (rising edge)	-	2.1	-	
		PLS[3:0]=0001 (falling edge)	-	2.0	-	
		PLS[3:0]=0010 (rising edge)	-	2.4	-	
		PLS[3:0]=0010 (falling edge)	-	2.3	-	
		PLS[3:0]=0011 (rising edge)	-	2.7	-	
		PLS[3:0]=0011 (falling edge)	-	2.6	-	
		PLS[3:0]=0100 (rising edge)	-	3.0	-	
		PLS[3:0]=0100 (falling edge)	-	2.9	-	
		PLS[3:0]=0101 (rising edge)	-	3.3	-	
		PLS[3:0]=0101 (falling edge)	-	3.2	-	
		PLS[3:0]=0110 (rising edge)	-	3.6	-	
		PLS[3:0]=0110 (falling edge)	-	3.5	-	
		PLS[3:0]=0111 (rising edge)	-	3.9	-	
		PLS[3:0]=0111 (falling edge)	-	3.8	-	
		PLS[3:0]=1000 (rising edge)	-	4.2	-	
		PLS[3:0]=1000 (falling edge)	-	4.1	-	
		PLS[3:0]=1001 (rising edge)	-	4.5	-	
		PLS[3:0]=1001 (falling edge)	-	4.4	-	
		PLS[3:0]=1010 (rising edge)	-	4.8	-	
		PLS[3:0]=1010 (falling edge)	-	4.7	-	
$V_{PVDhyst}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/down reset threshold	Flip point	-	1.65	-	V
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	4.6	-	ms

1) Guaranteed by design, not tested in production.

2) Note: Reset duration is measured from the power-on moment (POR reset) to the moment the first IO is read by the user's application code.

4.3.4 Supply Current Characteristics

The current consumption is a function of several parameters and factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed code.

The current consumption readings in all running modes given in this section are under the execution of a set of simple codes.

```
int main ()
{
SystemInit ();
. . . . . .
        while (1){}
}
```

Current Consumption

The microcontroller is placed under the following conditions:

- All I/O pins are in input mode and connected to a static level-V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state at 0~24 MHz; 1 wait state at 24~48 MHz).
- The ambient temperature and V_{DD} supply voltage conditions are listed in Table 11.
- The instruction prefetch function is enabled. When the peripherals are enabled: f_{HCLK} = f_{PCLK1}.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 14 Typical supply current at high and low temperature in operating mode (1) (2)

Symbol	Parameter	Conditions	f_{HCLK} (HZ)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply Current in Run mode	Internal Clock	48M	6.77	6.94	7.12	7.20	4.02	4.16	4.32	4.40	mA
			24M	4.19	4.32	4.49	4.56	2.54	2.64	2.80	2.87	
			8M	1.86	1.98	2.17	2.23	1.40	1.52	1.71	1.77	
			4M	1.37	1.48	1.64	1.72	1.10	1.20	1.37	1.45	
			2M	1.08	1.18	1.33	1.40	0.95	1.05	1.19	1.26	
			1M	0.94	1.04	1.17	1.24	0.87	0.97	1.11	1.17	
			500K	0.87	0.96	1.10	1.16	0.84	0.93	1.07	1.13	
			125K	0.82	0.91	1.05	1.11	0.81	0.90	1.03	1.10	

Table 15 Typical supply current at high and low temperature in sleep mode (1) (2)

Symbol	Parameter	Conditions	f_{HCLK} (HZ)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply Current in Sleep mode	Internal Clock	48M	4.60	4.73	4.90	4.97	1.83	1.94	2.08	2.15	mA
			24M	3.00	3.12	3.26	3.34	1.33	1.43	1.57	1.63	
			8M	1.43	1.53	1.67	1.73	0.97	1.06	1.20	1.26	
			4M	1.16	1.26	1.39	1.46	0.88	0.98	1.11	1.18	
			2M	0.98	1.07	1.21	1.27	0.84	0.94	1.07	1.13	
			1M	0.89	0.98	1.12	1.18	0.82	0.91	1.05	1.11	
			500K	0.84	0.94	1.07	1.13	0.81	0.90	1.04	1.10	
			125K	0.81	0.91	1.04	1.10	0.80	0.89	1.03	1.09	

1) Typical values are obtained when V_{DD}=3.3V.

2) When HCLK frequency is lower than 8MHz, the system clock is obtained by HIS division

Table 16 Typical supply current at high and low temperature in stop and standby mode

Symbol	Parameter	Conditions	Typical				Max	Unit
			-40℃	25℃	85℃	105℃	25℃	
I_{DD}	Supply current in Stop mode	PWR->CR register bit0 is set to 1	1.3	2.1	12.6	31.0	15.0	μA
	Supply current in Standby mode	LSI, IWDG on	1.0	1.1	2.4	6.2	-	
	Supply current in Standby mode	IWDG off	0.4	0.4	1.7	5.5	1.0	

1) Typical values are obtained when VDD=3.3V and TA=25℃.

2) Drawn by comprehensive evaluation, not tested in production. The I/O state is an analog input.

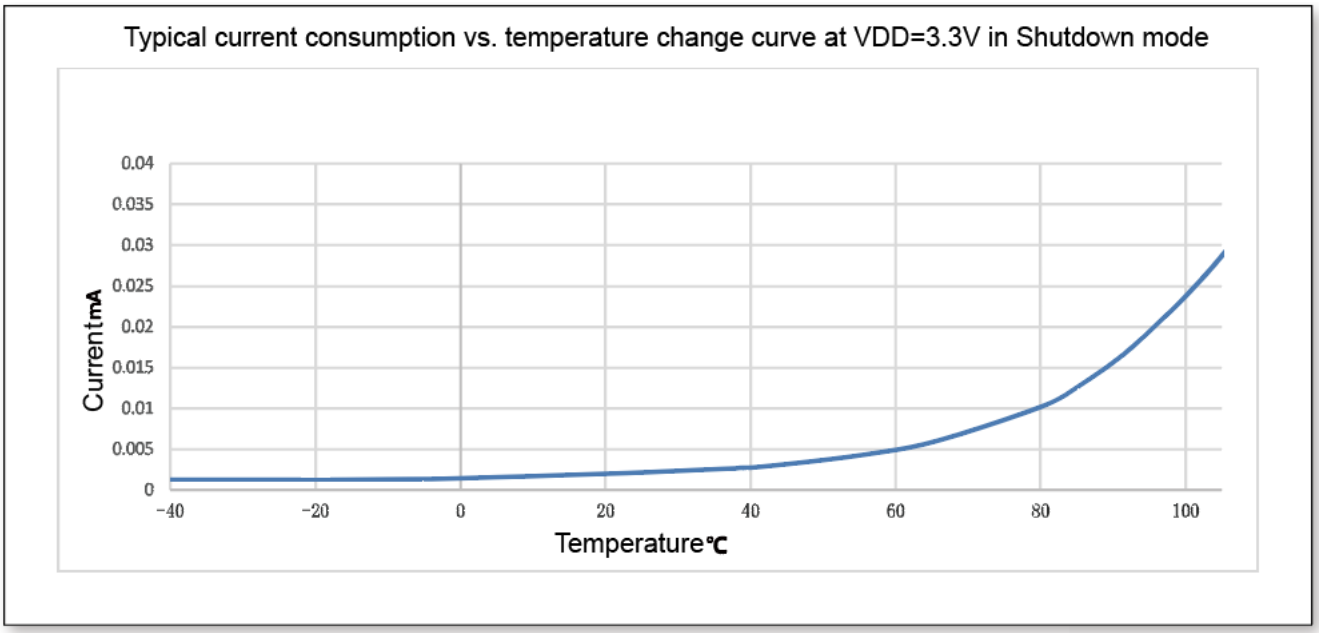

Figure 13 Typical current consumption vs. temperature at V_{DD} = 3.3V in Stop mode

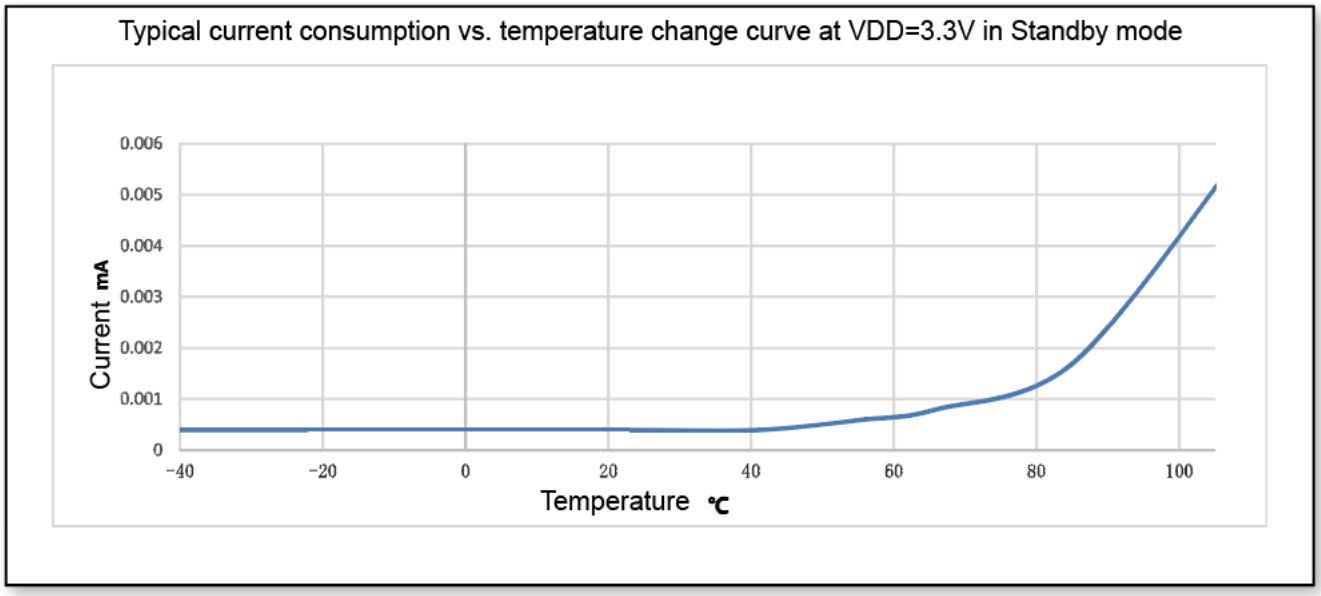

Figure 14 Typical current consumption vs. temperature at V_{DD} = 3.3V in Standby mode

Built-in Peripheral Current Consumption

The built-in peripheral current consumption is presented in Table 17. The MCU is placed under the following working conditions:

- All I/O pins are in input mode and connected to a static level-VDD or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The given value is calculated by measuring current consumption
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 11.

Table 17 Built-in peripheral current consumption

Bus	Built-in peripheral	Typical	Unit
AHB	CRC	1.4	uA/MHz
	GPIOA	0.8	
	GPIOB	0.6	
APB1	SYSCFG	0.3	
	ADC1	1.5	
	TIM1	12.3	
	SPI1	7.7	
	UART1	7.2	
	TIM14	3.0	
	DBG	0.2	
	TIM3	8.0	
	WWDG	0.5	

Bus	Built-in peripheral	Typical	Unit
	UART2	6.7	
	I2C1	10.0	
	PWR	0.5	

1) f_{HCLK} = 48MHz, f_{APB1} = f_{HCLK}/2, the prescaler coefficient of each peripheral is the default value.

Wake-up Time from Low-power Mode

The wake-up time given in the following table is measured in the wake-up phase of the internal clock HSI. The used clock source for wake-up is determined according to the present operation mode:

- Stop or Standby mode: Clock source is the oscillator
- Sleep mode: The clock source is the one used in the Sleep mode and the time is measured under the ambient temperature and supply voltage conforming to the general operating conditions.

Table 18 Low-power mode wake-up time

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$ (1)	Wake-up from Sleep mode	The system clock is HSI	2.81	μS
t_{WUSTOP} (1)	Wake-up from Stop mode (voltage regulator in operation mode)	The system clock is HSI	9.69	
t_{WUSTOP} (1)	Wake up from Stop mode (voltage regulator in low-power mode)	The system clock is HSI	7.65	
$t_{WUSTDBY}$ (1)	Wake up from Standby mode	PWR->CR[15:14] = 0x0	400	
$t_{WUSTDBY}$ (1)	Wake up from Standby mode	PWR->CR[15:14] = 0x1	342	
$t_{WUSTDBY}$ (1)	Wake up from Standby mode	PWR->CR[15:14] = 0x2	299	
$t_{WUSTDBY}$ (1)	Wake up from Standby mode	PWR->CR[15:14] = 0x3	217	

1) Wake-up time is from waking up edge to program executing IO flip.

4.3.5 External Clock Source Characteristics

High-speed external user clock generated from an external oscillator source

The parameters of characteristics given in the following table are measured by a high-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions.

Table 19 High-speed external user clock characteristics

Symbol	Parameter	Min	Typical	Max	Unit
f_{HSE_ext}	User external clock frequency (1)	-	8	32	MHz

Symbol	Parameter	Min	Typical	Max	Unit
V_{HSEH}	OSC_IN input pin high level voltage	0.7VDD	-	VDD	V
V_{HSEL}	OSC_IN input pin low level voltage	VSS	-	0.3	VDD
$t_{w\ (HSE)}$	OSC_IN high or low time (1)	15	-	-	ns
$C_{in\ (HSE)}$	OSC_IN input resistance (1)	-	5	-	pF
DuCy (HSE)	Duty cycle	-	50	-	%

1) Guaranteed by design, not tested in production.

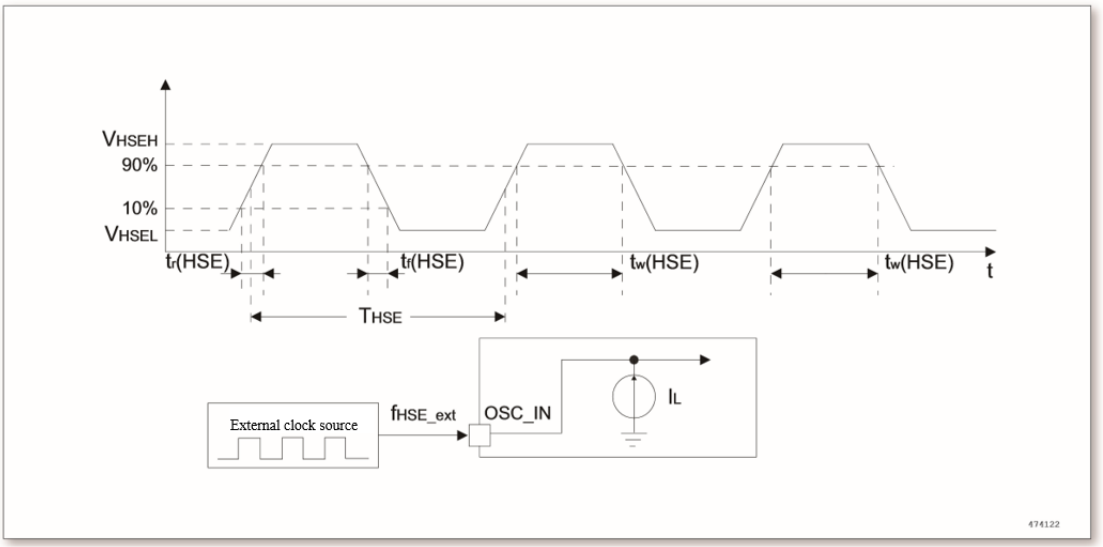

Figure 15 AC timing diagram of external high-speed clock source

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be generated by an oscillator composed of an 8 ~ 24MHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.).

Table 20 HSE 8 ~ 24MH oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{OSC_IN}	Oscillator frequency	2V<VDD<3.6V	2	8	12	MHz
		3.0V<VDD<5.5V	8	16	24	MHz
R_F	Feedback resistance (3)	-	-	500	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2} (4) is 16pF)	f_{OSC_IN} =24M VDD=3V	-	-	60	Ω
		f_{OSC_IN} =12M VDD=2V	-	-	150	Ω

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
I_2	HSE drive current	f_{OSC_IN} =24M ESR=30 V_{DD} = 3.3V， C_{L1} C_{L2} (3) is 20pF	-	1.5	-	mA
g_m	Oscillator transconductance	Startup	-	9	-	mA/V
$t_{SU\ (HSE)}$ (5)	Startup time	V_{DD} is stablized	-	3	-	mS

1) Resonator characteristics are given by the crystal/ceramic resonator manufacturer.
2) Drawn from comprehensive evaluation, not tested in production.
3) The relatively low RF resistance value can provide protection and avoid problems occurred when operating in a humid environment. Changes have been made to leakage and bias conditions generated in this environment. However, if the MCU is used in harsh humid conditions, such parameters need to be considered in designing.
4) For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5pF to 25pF range (typical value) designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10pF can be used as a rough estimate of the combined pin and board capacitance) when choosing choosing C_{L1} and C_{L2}.
5) $t_{SU(HSE)}$ is the startup time, measured from the time HSE is enabled by software until a stable 8 MHz oscillation is reached. This value is measured from a standard crystal resonator and it can vary significantly with the crystal manufacturer.

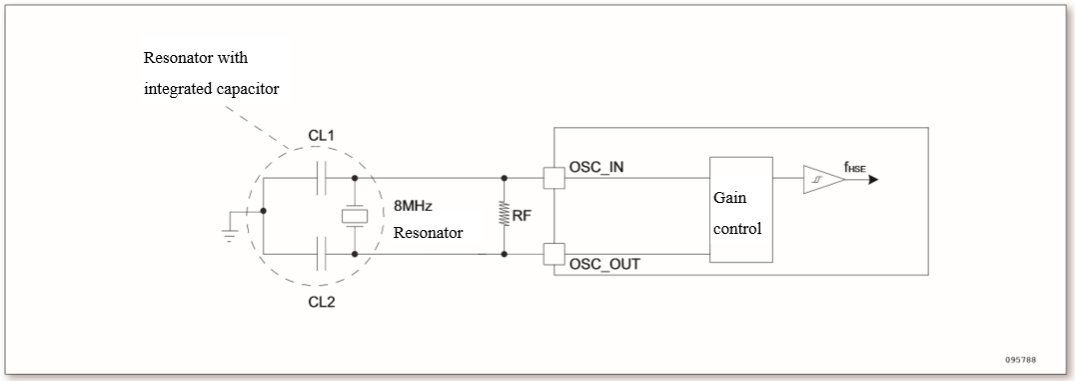

Figure 16 Typical application using 8MHz crystal

4.3.6 Internal Clock Source Characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and supply voltage conforming to the general operating conditions.

High-speed internal (HSI) oscillator

Table 21 HSI oscillator characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
ACC_{HSI}	HSI oscillator accuracy	T_A = -40℃~ 85℃	-2.5	-	+2.5	%
		T_A = -40℃~ 105℃	-3	-	+3	%

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
		T_A = 25°C	-1	-	+1	%
$t_{SU\ (HSI)}$	HSI oscillator startup time	-	-	12	16	μS
$I_{DD\ (HSI)}$	HSI oscillator power consumption	-	-	519	-	μA

1) VDD = 3.3V, unless otherwise specified.

2) Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 22 LSI oscillator characteristics (1) (2)

Symbol	Parameter	Min	Typical	Max	Unit
f_{LSI} (2)	Frequency	-	40	-	KHz
$t_{SU\ (LSI)}$ (2)	LSI oscillator startup time	-		100	μS

1) V_{DD} = 3.3V, T_A = 40℃~ 85℃, unless otherwise specified.

2) Drawn from comprehensive evaluation, not tested in production.

4.3.7 Memory Characteristics

Table 23 FLASH memory characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
t_{prog}	16-bit programming time	-		26	-	μS
f_{EWCLK}	Erase frequency	-	8	-	-	MHz
t_{ERASE}	Page (1024K bytes) erase time	-	8	-	10	mS
t_{ME}	Mass erase time	-	20	-	40	mS
I_{DD}	Current	Read mode 40MHz	-	3	4.5	mA
		Write mode	-	-	3.5	mA
		Erase mode	-	-	2	mA
V_{prog}	Programming voltage	-	-	1.5	-	V

Table 24 Flash memory endurance and data retention period (1) (2)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
N_{END}	Erase time		20000	-	-	Times
T_{DR}	Data retention	T_A = 125℃	10	-	-	Years
		T_A = 25℃	100	-	-	

1) Drawn from comprehensive evaluation, not tested in production.

2) The cycle tests are conducted over the entire temperature range.

4.3.8 EMC Characteristics

Susceptibility tests are performed on a sample basis during device comprehensive evaluation.

Functional EMS (Electromagnetic Susceptbility)

When a simple application is executed (toggling two LEDs through I/O ports), the test sample is stressed by one electromagnetic interference until an error occurs. The error is indicated by the flashing LEDs.

- EFT: In V_{DD} and V_{SS}, impose a pulse group (forward and backward) with a transient voltage by a 100 pF capacitor until a functional error is generated. This test complies with the IEC61000-4-4 standard.

Chip reset can restore normal operation of the system. The test results are listed in the table below.

A indicates normal operation.

B indicates normal operation after the chip produced a reset.

Table 25 EMS characteric (1)

Symbol	Parameter	Conditions	Level/class
V_{EFT}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-4	4A
V_{ESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-2	2B

1) Drawn from comprehensive evaluation, not tested in production.

Designing hardened software to avoid noise problems

EMC evaluation and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and qualification tests in relation with the EMC.

Software recommendations

The software flowchart must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or the crystal oscillator pins for 1 second.

To complete ESD test, a voltage can be applied directly on the chip, over the range of application requirements. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.3.9 Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU), using specific measurement methods, the chip is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive then a negative pulse separated by 1 second) are applied to the all pins of each sample. The sample size depends on the number of supply pins on the chip (3 parts x (n + 1) supply pins). This test conforms to the ESDA/JEDEC JS-001-2017/ JS-002-2018 standard.

Static latchup

Two complementary static latchup tests are required on six samples to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin. This test is compliant with the EIA/JESD78E IC latchup standard.

Table 26 ESD characteristics (1)

Symbol	Parameter	Conditions	Level	Max	Unit
$V_{ESD\ (HBM)}$	Electrostatic discharge voltage (mannequin)	TA = 25◦C, conforming to ESDA/JEDEC JS-001-2017	3B	±8000	V
$V_{ESD\ (CDM)}$	Electrostatic discharge voltage (charging device model)	TA = 25◦C, conforming to ESDA/JEDEC JS-002-2018	C3	±2000	V
I_{LU}	Electrostatic latchup (Latchup current)	TA = 25◦C, conforming to JESD78E	I,A	+150/-200	mA

1) Drawn from comprehensive evaluation, not tested in production.

2) This note is only for the main chip, not for the gate driver.

4.3.10 I/O Port Characteristics

GPIO port general input/output characteristics

Unless otherwise specified, the parameters listed in the table below are derived from tests performed under the conditions summarized in Table 11. All I/O ports are CMOS-compliant.

Table 27 IO static characteristics (1)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{IL}	Input low level voltage	3.3V CMOS端口	-0.3	-	0.8	V
V_{IL}	Input low level voltage	5V CMOS端口	-0.3	-	0.3*VDD	V
V_{IH}	Input high level voltage	3.3V CMOS端口	2	-	3.3	V
V_{IH}	Input high level voltage	5V CMOS端口	0.7*VDD	-	5	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (2)	3.3V	0.1*VDD	-	-	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (2)	5V	0.1*VDD	-	-	V
I_{lkg}	Input leakage current (2)	3.3V	-	-	1	μA
I_{lkg}	Input leakage current (2)	5V	-	-	1	μA

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
R_{PU}	Weak pull-up equivalent resistance (3)	3.3V $V_{IN} = V_{SS}$	22	-	100	kΩ
R_{PU}	Weak pull-up equivalent resistance (3)	5V $V_{IN} = V_{SS}$	22	-	100	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	3.3V $V_{IN} = V_{DD}$	20	-	50	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	5V $V_{IN} = V_{SS}$	20	-	50	kΩ
C_{IO}	I/O pin capacitor	3.3V	-	-	10	pF
C_{IO}	I/O pin capacitor	5V	-	-	10	pF

1) Drawn from comprehensive evaluation, not tested in production.
2) Hysteresis voltage of the Schmitt trigger switching level.
3) In case of a negative current back flow in the adjacent pin, the leakage current may be higher than the maximum value.
4) The pull-up and pull-down resistors are MOS resistors.

Output drive current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA current.

In user application, the number of I/O pin must ensure that the drive current must be limited to respect the absolute maximum rating specified in Section 5.2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum running current of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents absorbed and sunk by all the I/O pins on V_{SS}, plus the maximum running current of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS}.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are shown in Figure 18 and Table 28, respectively. Unless otherwise specified, the parameter listed in Table 28 is measured by the ambient temperature and supply voltage in accordance with the condition in Table 11.

Table 28 Output AC characteristics (1) (2)

MODEx[1：0] configuration	Symbol	Parameter	Conditions	Typical	Unit
11	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50pF VDD=3.3V	7.2	ns
	$t_{r(IO)out}$	Output low to high level rise time		7.2	ns
10	$t_{f(IO)out}$	Output high to low level fall time		4.4	ns
	$t_{r(IO)out}$	Output low to high level rise time		4.4	ns
01	$t_{f(IO)out}$	Output high to low level fall time		3.73	ns
	$t_{r(IO)out}$	Output low to high level rise time		3.73	ns

1) I/O port speed can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in the Chip Reference Manual.
2) Guaranteed by design, not tested in production.

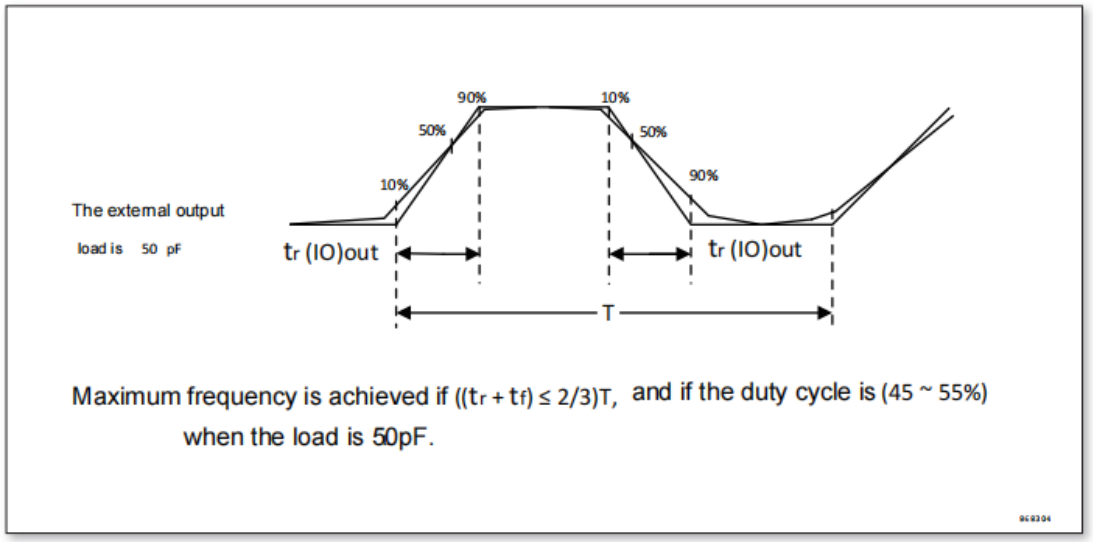

Figure 17 Definition of input and output AC characteristics

4.3.11 NRST Pin Characteristics

NRST pin input driver uses CMOS technology, and it is connected with a pull-up resistor, R_{PU}.

Table 29 NRST pin characteristics (1)

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IL\ (NRST)}$	NRST input low level voltage	-0.3	-	0.8	V
$V_{IH\ (NRST)}$ (2)	NRST input high level voltage	2	-	V_{DD}	V
$V_{hys\ (NRST)}$	NRST Schmitt trigger voltage hysteresis	0.1*VDD	-	-	V
$V_{F\ (NRST)}$ (3)	NRST input filtered pulse	-	-	1.0	uS
$V_{NF\ (NRST)}$ (3)	NRST input unfiltered pulse	4.0	-	-	uS

1) Guaranteed by design, not tested in production.

2) The pull-up and pull-down resistors are MOS resistors.

3) 5.1KΩ pull-up resistor is required externally when the NRST function is used.

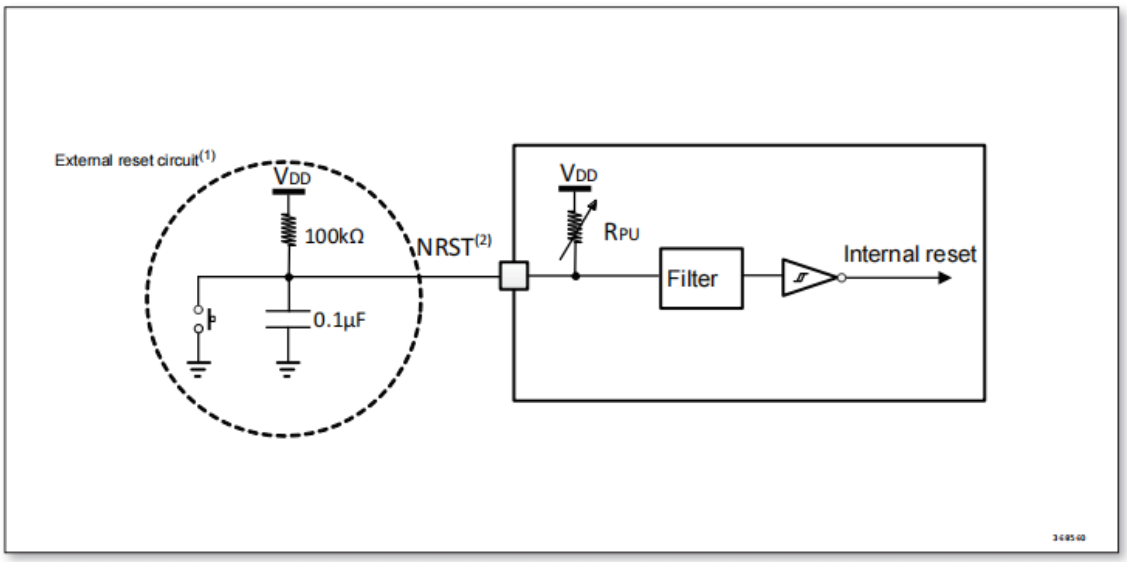

Figure 18 Recommended NRST pin protection

1) The reset network is to prevent parasitic reset.
2) The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 30 , otherwise the MCU cannot be reset.

4.3.12 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), refer to section 4.3.10.

Table 30 TIMx (1)characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res\ (TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$ (2)
		$f_{TIMxCLK}$ = 48MHz	20.8	-	nS
f_{EXT}	External clock frequency of channel 1 to 4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	位
$t_{COUNTER}$	16-bit counter period when choosing the internal clock	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1365	µS
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	-	1365	uS

1) TIMx is a generic name.
2) $f_{TIMxCLK}$ value varies linearly with f_{EXT}, $t_{COUNTER}$ and t_{MAX_COUNT}.

4.3.13 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table 31 are derived from tests

performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in Table 11.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I2C characteristics are listed in Table 31. Refer to section 4.3.10 for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 31 I2C interface characteristics (1) (2)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w\ (SCLL)}$	SCL clock low time	8*t_{PCLK}	-	8*t_{PCLK}	-	μs
$t_{w\ (SCLH)}$	SCL clock high time	6*t_{PCLK}	-	6*t_{PCLK}	-	μs
$t_{su\ (SDA)}$	SDA setup time	2*t_{PCLK}	-	2*t_{PCLK}	-	ns
$t_{h\ (SDA)}$ (3)	SDA data hold time	0	-	0	875	ns
$t_{r\ (SDA)}$ $t_{r\ (SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f\ (SDA)}$ $t_{f\ (SCL)}$ (4)	SDA and SCL fall time	-	300	-	300	ns
$t_{h\ (STA)}$	Start condition hold time	8*t_{PCLK}	-	8*t_{PCLK}	-	μs
$t_{su\ (STA)}$	Repeated start condition setup time	6*t_{PCLK}	-	6*t_{PCLK}	-	μs
$t_{su\ (STO)}$	Stop condition setup time	6*t_{PCLK}	-	6*t_{PCLK}	-	μs
$t_{w\ (STO:STA)}$	Time from Stop condition to Start condition (bus idle)	5*t_{PCLK}	-	5*t_{PCLK}	-	μs
C_b	Capacitive load of each bus	-	400	-	400	pF

1) Guaranteed by design, not tested in production.

2) f_{PCLK1} must be greater than 3MHz to achieve standard mode I2C frequencies. It must be greater than 12MHz to achieve fast mode I2C frequencies.

3) If the low level time of the SCL signal is not required to be stretched, only the maximum hold time for the start condition needs to be met.

4) In order to cross the undefined area of SCL falling edge, a hold time of at least 300nS must be guaranteed on the SDA signal within the MCU.

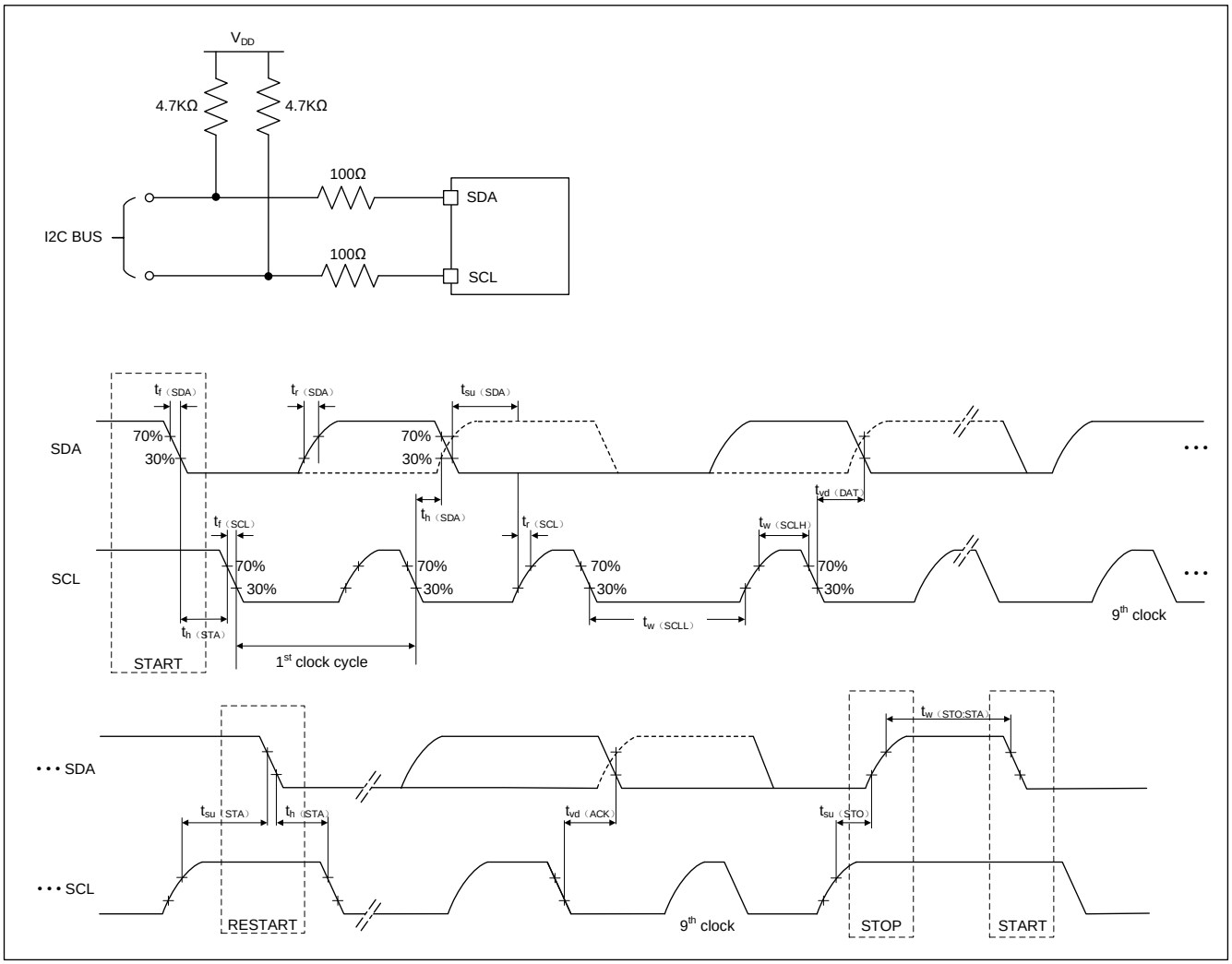

Figure 19 I2C I2C bus AC waveform and measurement circuit (1)

1) Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in Table 32 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 11

Refer to section 4.3.10 for more details on the input/output alternate function pin characteristics (NSS, SCK, MOSI and MISO).

Table 32 SPI characteristics

Symbol	Parameter	Conditions	Min (2)	Max (3)	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	24	MHz
		Slave mode		12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	nS
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	1Tpclk	-	nS

Symbol	Parameter	Conditions	Min (2)	Max (3)	Unit
$t_{h\ (NSS)}$ (1)	NSS hold time	Slave mode	1Tpclk	-	nS
$t_{w\ (SCKH)}$ (1)	Time when SCK level is high	-	$t_{c\ (SCK)/2}$ - 6	$t_{c\ (SCK)/2}$ - 6	nS
$t_{w\ (SCKL)}$ (1)	Time when SCK level is low	-	$t_{c\ (SCK)/2}$ - 6	$t_{c\ (SCK)/2}$ - 6	nS
$t_{su\ (MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	12	-	nS
$t_{su\ (SI)}$ (1)		Slave mode	5	-	nS
$t_{h\ (MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	0	-	nS
$t_{h\ (SI)}$ (1)		Slave mode	6	-	nS
$t_{a\ (SO)}$ (1) (2)	Data output valid time	Slave mode (after the enable edge) Non-high speed mode	-	34	nS
		Slave mode (after enable edge) high speed mode	-	13	nS
$t_{v\ (MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-0.6	-	nS

1) Drawn by comprehensive evaluation.

2) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

3) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

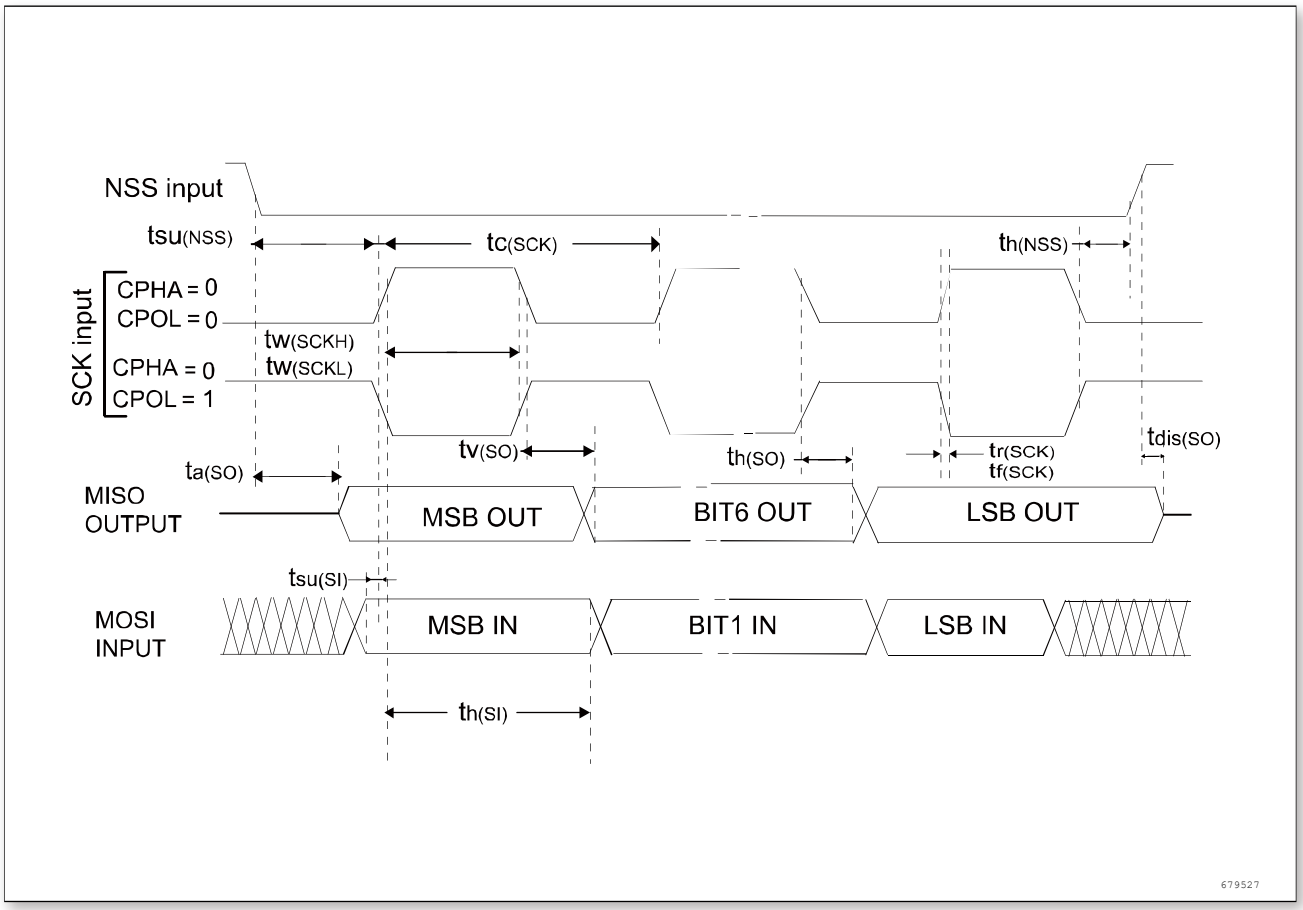

Figure 20 I2C slave mode waveform and CPHA = 0, SPI_CCTL.CPHASEL=1

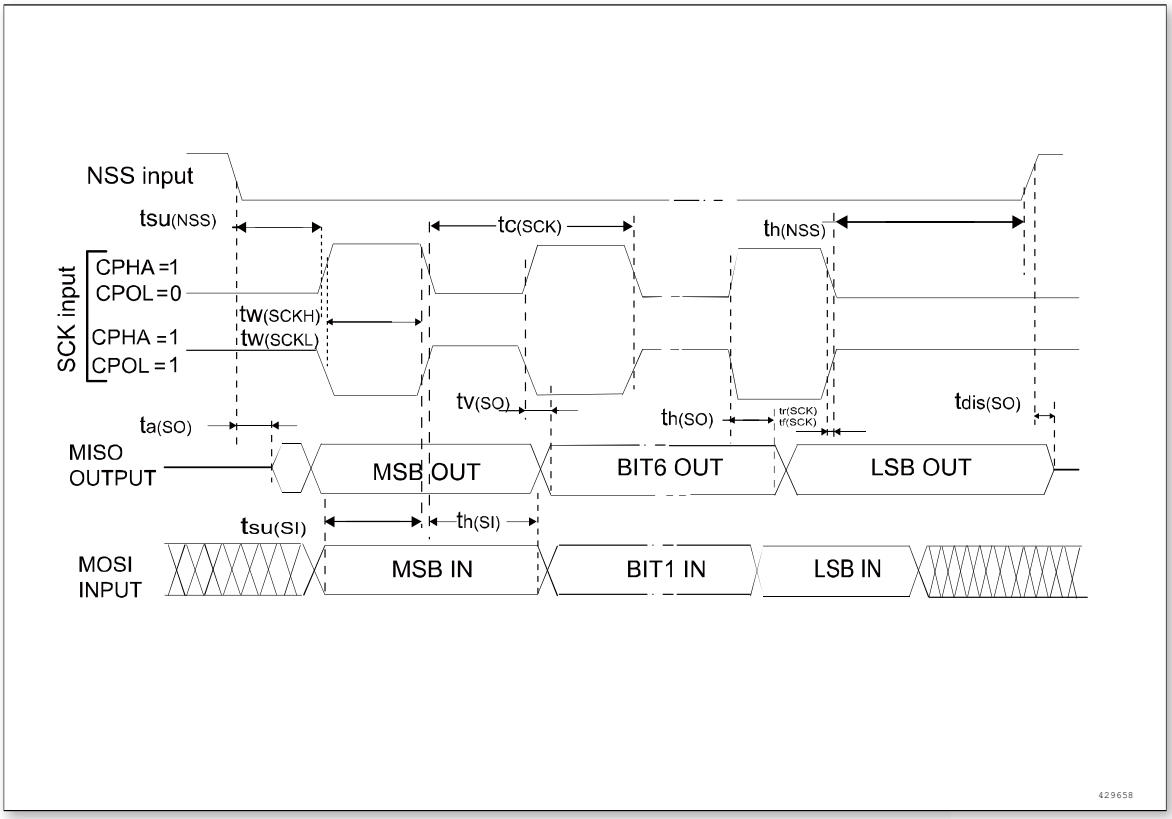

Figure 21 SPI timing diagram-slave mode and CPHA = 1 (1), SPI_CCTL.CPHASEL=1

1) Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

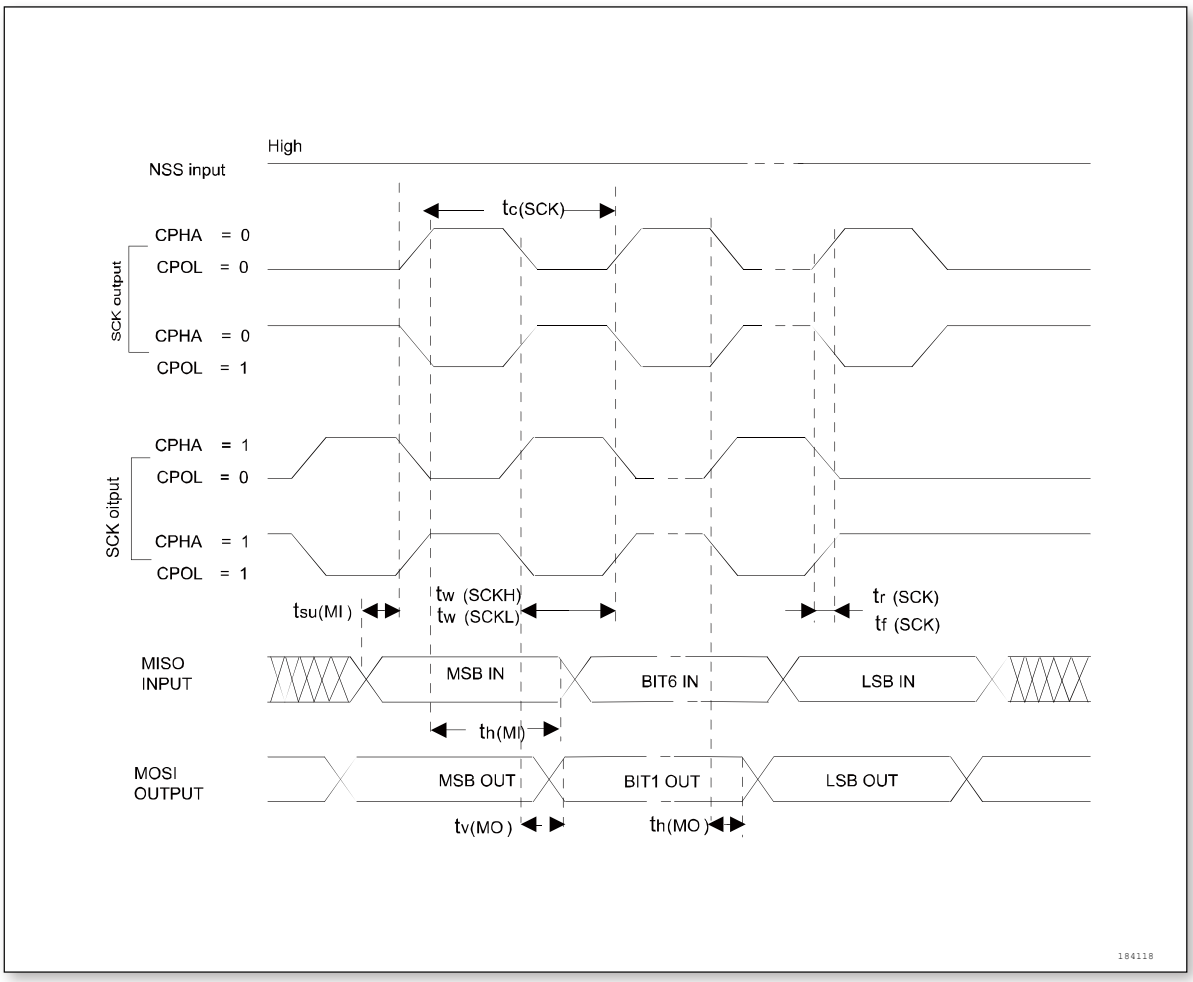

Figure 22 SPI timing diagram-slave mode and CPHA = 1 (1), SPI_CCTL.CPHASEL=1

1) Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$

4.3.14 ADC Characteristics

Unless otherwise specified, the parameters in the following table are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage specified in Table 11.

Table 33 ADC characteristics (1)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
VDD	Supply voltage	-	2.5	-	5.5	V
f_{ADC} (3)	ADC clock frequency	-	-	-	16	MHz
f_S (3)	Samping rate	-	-	-	1	MHz
f_{TRIG}	External trigger frequency (3)	fADC = 16MHz	-	-	941	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN} (2)	Conversion voltage range	-	0	-	VDD	V
R_{AIN}	External input impedance	-	See the table below and equation 1			kΩ
R_{ADC}	Sampling switch resistance	-	-	-	1.5	kΩ

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	-	10	pF
t_S	Sampling time	fADC = 16MHz	0.156	-	15.031	μS
		-	2.5	-	240.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	fADC = 16MHz	1	-	15.875	μS
		-	15 ~ 253 (sampling tS + successive approximation 12.5)			$1/f_{ADC}$

1) Guaranteed by comprehensive evaluation, not tested in production.

2) Guaranteed by design, not tested in production.

3) For external trigger, a delay of $1/f_{ADC}$ must be added.

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

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Table 34 Maximum R_{AIN} at f_{ADC}=15MHz (1)

T_S (cycles)	t_S (μS)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1) Guaranteed by design, not tested in production.

Table 35 ADC accuracy (1) (2)

Symbol	Parameter	Conditions	Typical	Max	Unit
Resoluion	Resolution		12	-	Bit
ET	Comprehensive error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	+2/-7	-	LSB
EO	Offset error		4.5	-	
EG	Gain error		-2	-	
ED	Differential linearity error		3/-0.8	-	
EL	Integral linearity error		+4.5/-3.5	-	

1) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the range specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ does not affect the ADC accuracy.

2) Guaranteed by comprehensive evaluation, not tested in production.

3) ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission

curves.

4) EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
5) EG = Gain error: The deviation between the last ideal transition and the last actual transition.
6) ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
7) EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

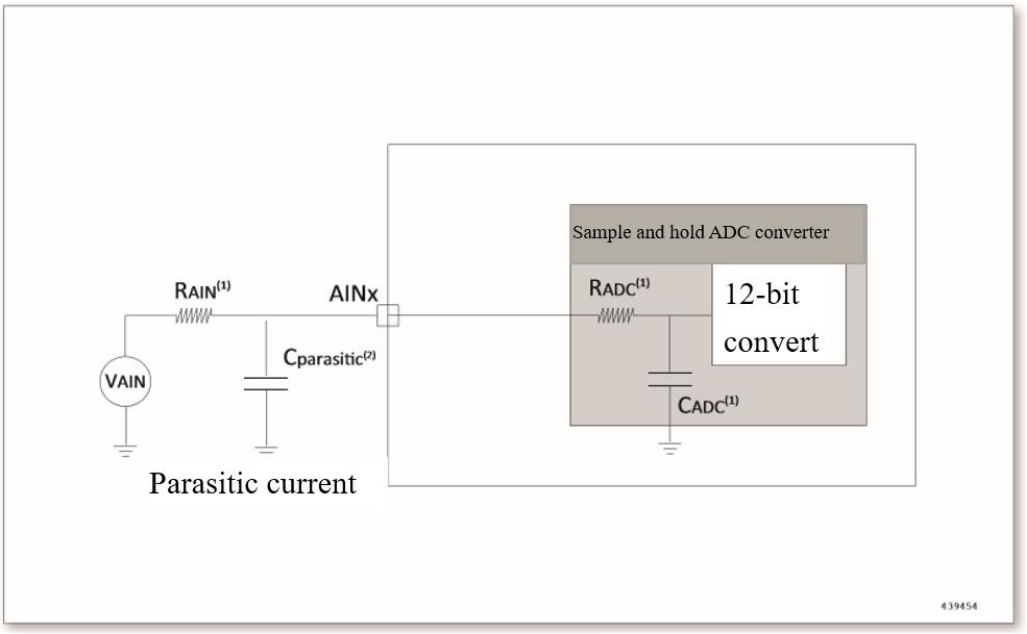

Figure 23 Typical connection diagram using ADC

1) Refer to Table 34 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2) Cparasitic represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high Cparasitic value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The decoupling of power supply must be connected as shown below. The 10nF capacitor in the figure must be ceramic, and it should be as close as possible to the MCU chip.

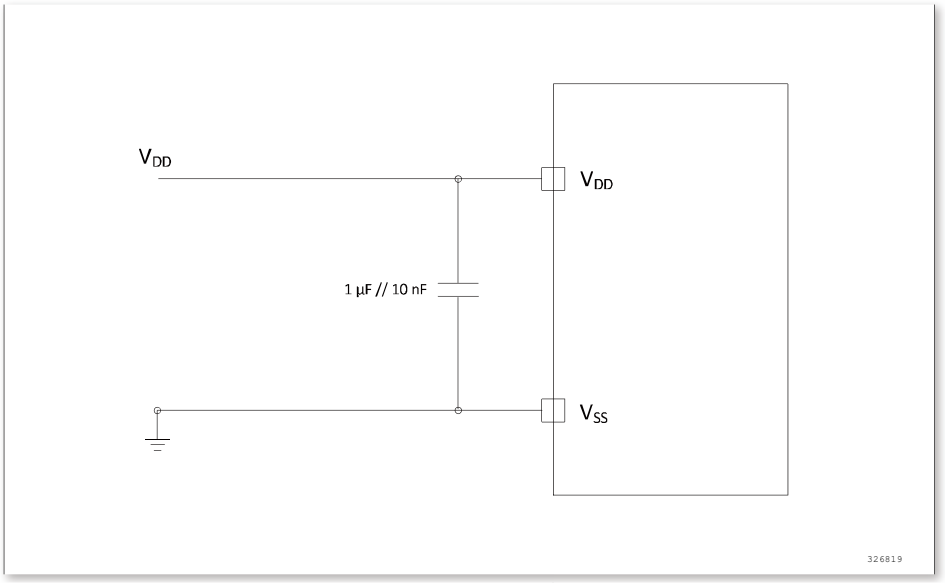

Figure 24 Power supply and reference power supply decoupling circuit

5 Gate Driver

5.1 Operating Conditions

Table 36 Gate driver absolute maximum ratings

Symbol	Description	Min	Max	Unit
V_{VIN}	Input voltage of bus voltage	-0.3	45	V
$V_{HIN1,2,3}$	High-side control input voltage	-0.3	V_{LDO}	
$V_{LIN1,2,3}$	Low-side control input voltage	-0.3	V_{LDO}	
$V_{INP1,2}$	OP positive input	-0.3	V_{LDO}	
$V_{INN1,2}$	OP negative input	-0.3	V_{LDO}	
T_{jmax}	Junction temperature	-40	150	℃
T_{stg}	Memory temperature	-60	150	
ESD	HBM	±2000		V
	CDM	±1000		

Table 37 Gate driver recommended working range

Symbol	Description	Min	Max	Unit
V_{VIN}	Input voltage of bus voltage	7	36	V
V_{LDO}	5V LDO output voltage	4.5	5.5	
$V_{HIN1,2,3}$	High-side control input voltage	0	V_{LDO}	
$V_{LIN1,2,3}$	Low-side control input voltage	0	V_{LDO}	
$V_{HO1,2,3}$	Gate driver upper bridge arm output	V_{VIN} - 12	36	
$V_{LO1,2,3}$	Gate driver lower bridge arm output	0	12	
$V_{AO1,2}$	OP input	0	V_{LDO}	
$V_{INP1,2}$	OP positive input	0	V_{LDO}	
$V_{INN1,2}$	OP negative input	0	V_{LDO}	
Tj	Junction temperature	-40	125	℃

1) External LDO is recommended *for 24V motor system when the ambient temperature is above 85°C.*

5.2 Electrical characteristics

Table 38 Gate driver electrical characteristics

Symbol	Descriptions	Min	Typical	Max	Unit
Power supply					
V_{VIN}	Input voltage of bus voltage	7		36	V
I_{VIN}	Static supply current		500	1000	μA
V_{UVLO}	Undervoltage lockout (V_{VIN} falling)		5.1		V
$V_{STARTUP}$	Undervoltage release (V_{VIN} rising)		5.5		
LDO regulator					
I_{OUT}	LDO input capability (V_{OUT} >95% V_{LDO})			50	mA
V_{DROP}	Drop voltage (I_{OUT} = 50mA)		0.84		V
ΔV_{OUT}	Load regulation (1mA < I_{OUT} < 50mA)		0.5	1	%

Symbol	Descriptions	Min	Typical	Max	Unit
Linear regulation	7V<V_{VIN}<36V		0.1	0.2	%/V
3-phase gate driver					
V_{IL}	Logic input low voltage			0.4	V
V_{IH}	Logic input high voltage	1.6			
R_{INPD}	Input pull-down resistor		9.3		KΩ
I_{OH}	High-level output short-circuit pulse current		300		mA
I_{OL}	Low-level output short-circuit pulse current		300		mA
R_{PULLUP}	High-side driver output pull-up PMOS resistor IOUT=20mA, VIN=8V		8.5		Ω
	Low-side driver output pull-up PMOS resistor IOUT=20mA, VIN=8V		16		
$R_{PULLDOWN}$	High-side driver output pull-down NMOS resistor IOUT=20mA, VIN=8V		15		
	Low-side driver output pull-down NMOS resistor IOUT=20mA, VIN=8V		7.5		
V_{PCLAMP}	Vgs clamp voltage for driving external PMOS	-12	-10	-9	V
V_{NCLAMP}	Vgs clamp voltage for driving external NMOS	9	10	12	
t_{DT}	Dead time	300	500	800	ns
t_r	Output rise ime		70	150	
t_f	Output fall time		70	150	
T_{on}	Output rising edge transfer time		50	100	
T_{OTP}	Overheat protection threshold to switch off the whole chip		160		℃
T_{OTPHYS}	Overheat protection hysteresis		20		℃
Low-offset amplifier					
V_{OP}	Operating voltage of operational amplifier		5		V
V_{OFFSET}	Bias voltage, Vinp and Vinn is close to 0		3		mV
VC_{RANGE}	Input common mode voltage range	0.2		V_{OP}-0.2	V
I_{IN}	Input bias current			1	μA
I_{SOURCE}	Output current	1000			μA
I_{SINK}	Input current	1000			
V_{SW}	Output voltage swing	0		V_{OP}	V
A_V	Open loop gain		10		kV/V
GBW	Band width		6		MHz

1) Unless otherwise stated, test conditions are V_{IN}=24V, C_L=1000pF, T_A=25°C

Table 39 PWM input and output state table

LINx	HINx	Lox	Hox	Output state
0	0	GND	VIN	Both external NMOS and PMOS are switched off
0	1	GND	VIN-10V	External NMOS is switched off and PMOS on
1	0	10V	VIN	External NMOS is switched on and PMOS off
1	1	GND	VIN	Both external NMOS and PMOS are switched off

6 Package Dimensions

6.1 Package TSSOP28

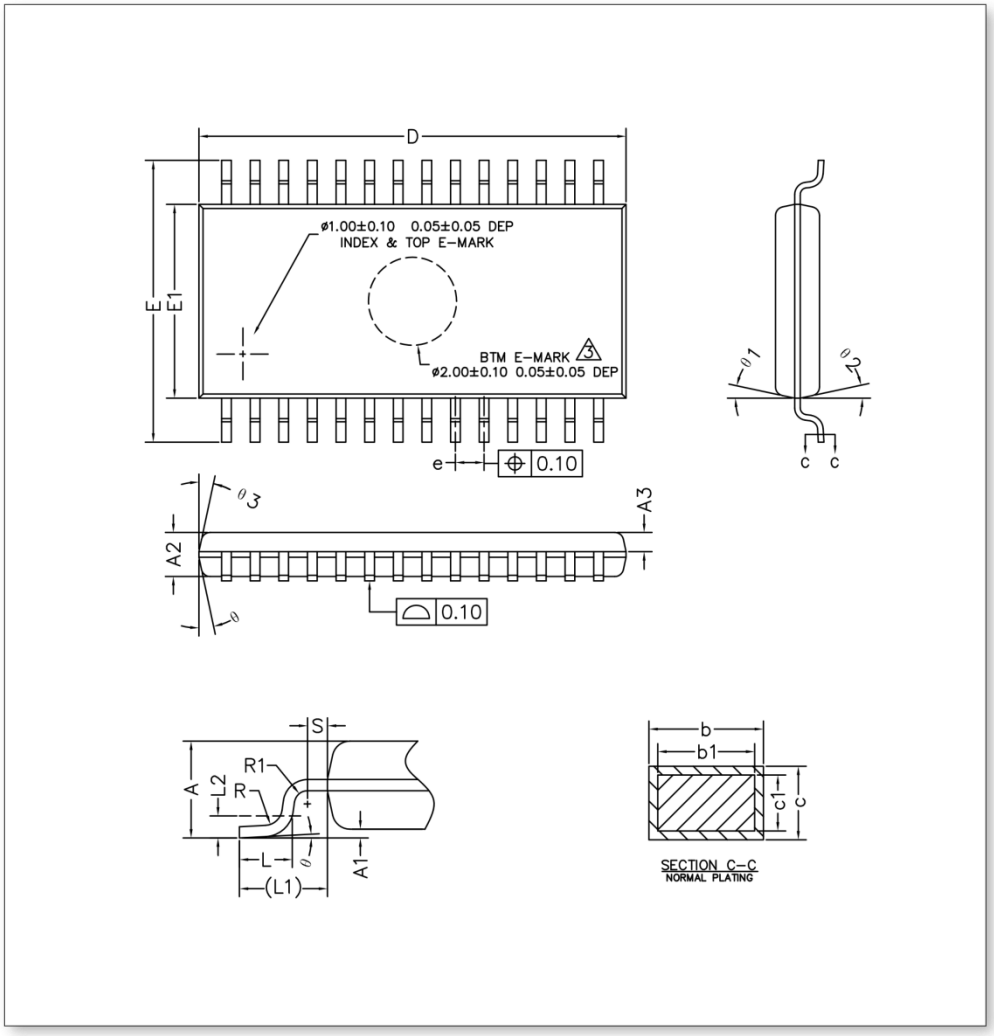

Figure 25 TSSOP28, 28-pin low-profile quad square flat package

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 40 TSSOP28 size description

Label	MM		
	Min	Typical	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.29

b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ	0°	-	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°

6.2 Package QFN28

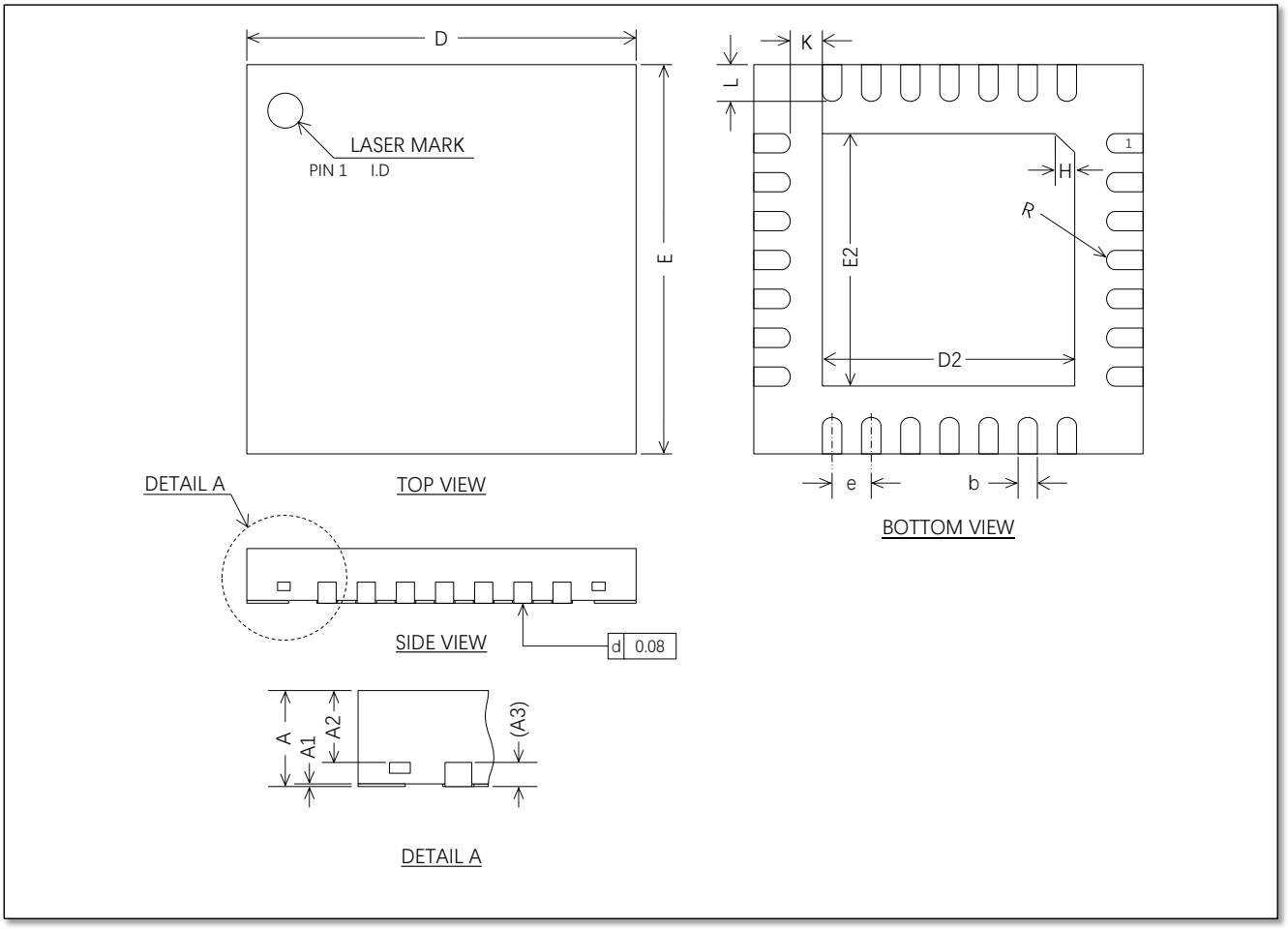

Figure 26 QFN28, 28-pin low-profile quad square flat no-lead package outline

1. Drawing is not to scale.
2.Dimensions are expressed in millimeters.

Table 41 QFN28 size description

Label	MM		
	Min	Typical	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70

Package Dimensions

Label	MM		
	Min	Typical	Max
E2	2.50	2.60	2.70
e	-	0.40	-
H	0.35REF		
K	0.30REF		
L	0.35	0.40	0.45
R	0.075	-	-

7 Product Naming Rule

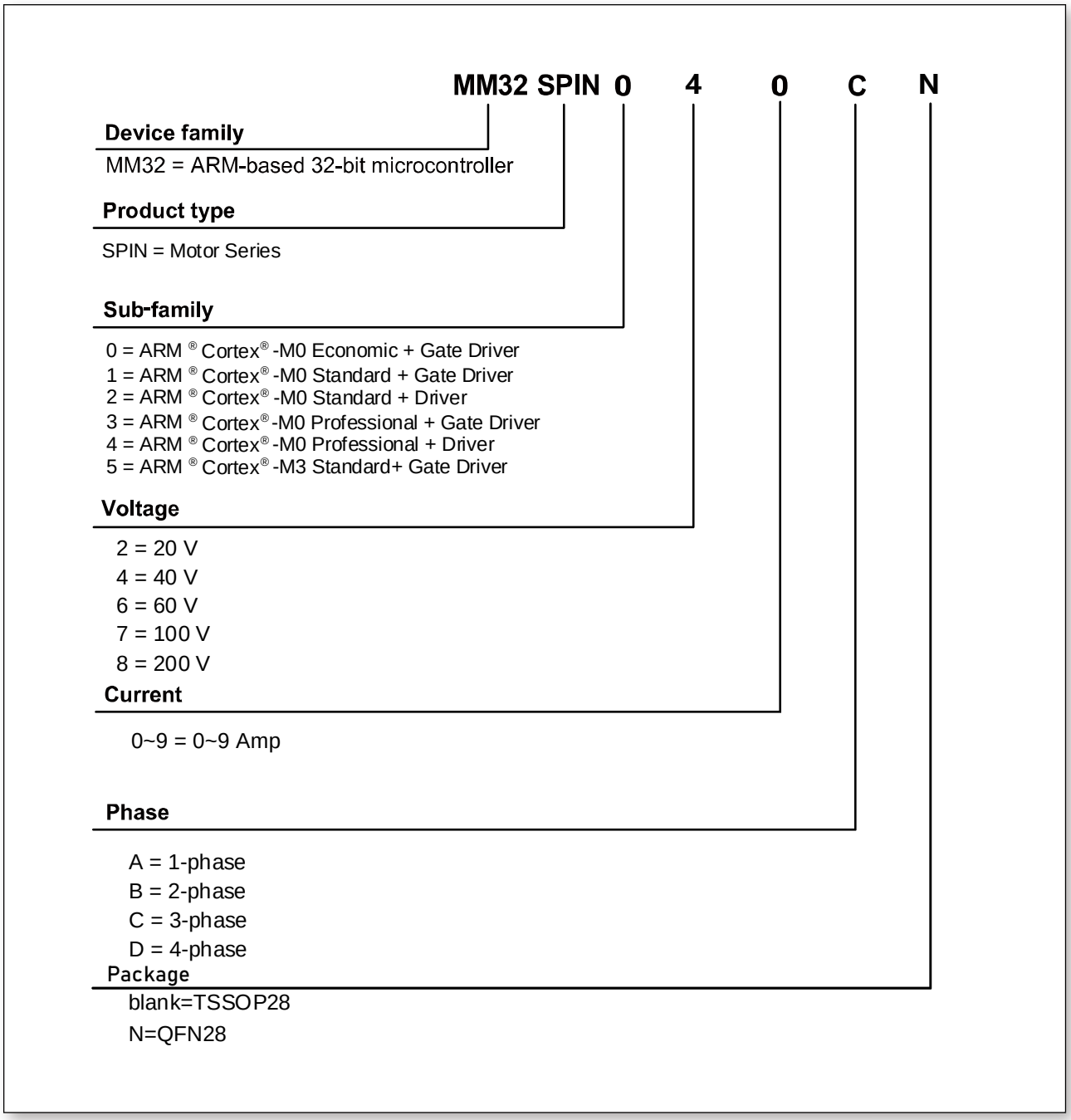

Figure 27 MM32 model naming

8 Abbreviation

ADC	Analog Digital Converter
CRC	Cyclic Redundancy Check
EXTI	External Interrupt Event Controller
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FLASH	Flash Memory
GPIO	General Power Input/Output
HSE	External High Speed Clock
HSI	Internal High Speed Clock
I2C	Internal Integrated Circuit
IWDG	Independent Watchdog
LP	Low Power
LSI	Internal Low Speed Clock
NVIC	Nested Vectored Interrupt Controller
PWR	Power Reset
POR	Power On Reset
PDR	Power Down Reset
PVD	Voltage Detector
RCC	Reset Clock Controller
SRAM	Static Random Access Memory
SPI	Serial Periphery Interface
SWD	Serial Debugging Interface
SysTick	System Tick Timer
Sleep	Sleep
Stop	Stop
Standby	Standby
TIM	Timer
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

9 Revision History

Table 42 Revision history

Date	Version	Content
2022/02/06	Rev1.00	First public release
2022/03/11	Rev1.01	Updated functional block diagram and circuit diagram
2022/03/29	Rev1.02	Newly added QFN28 silk mark, pinout and package information
2022/03/29	Rev1.03	Updated some electrical parameters
2022/06/22	Rev1.04	Modified product naming rule
2022/10/09	Rev1.05	Newly added QFN28 power dissipation
2022/10/26	Rev1.06	Deleted the maximum and minimum values of pin space and circuit schematic, modified auxiliary chip information
2023/01/18	Rev1.07	Added PA4 pin definition and updated pre-drive information