National Semiconductor

MM53107 Series 17-Stage Oscillator/Divider

General Description

The MM53107 is a low threshold voltage CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from a 2.097152 MHz quartz crystal. An internal pulse is generated by the combinations of stages 1–4, 16 and 17 to set or reset the individual stages. The MM53107 is advanced one count on the positive transition of each clock pulse. One buffered output is available: the 17th stage 60 Hz output. The MM53107 is available in an 8-lead dual-in-line epoxy package.

Features

- Input frequency—2.097152 MHz
- Output frequency—60Hz
- Crystal oscillator
- High speed (2 MHz at V_{DD} = 2.5V)
- Wide supply range 2.5V–6V
- Low power (0.5 mW @ 2 MHz/2.5V)
- Fully static operation
- 8-lead dual-in-line package

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Block and Connection Diagrams

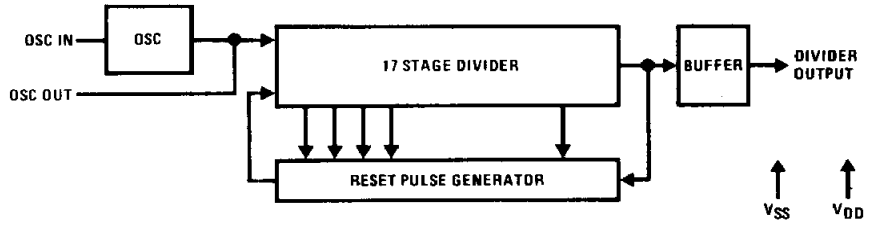

FIGURE 1

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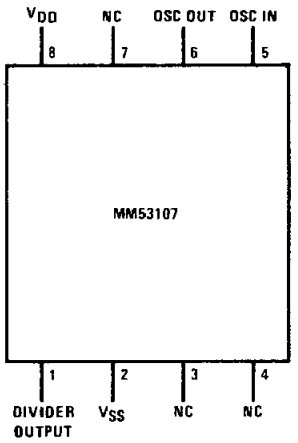
Dual-In-Line Package



TOP VIEW

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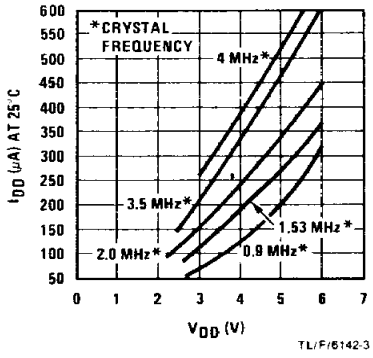
FIGURE 2

Order Number MM53107N
See NS Package N08E

Typical Performance Characteristics

Typical Current Drain vs Oscillator Frequency



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Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Maximum V_{CC} Voltage	7V
Operating V_{CC} Range	2.5V to 6V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating temperature range, V_{SS} = Gnd, 2.5V $\leq V_{DD} \leq$ 6V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 6V			10	μA
Operating Current Drain	V_{DD} = 2.5V, f_{IN} = 2.1 MHz			200	μA
Frequency of Oscillation	V_{DD} = 2.4V	dc		2.1	MHz
	V_{DD} = 6V	dc		4.0	MHz
Output Current Levels					
Logical "1" Source	V_{DD} = 4V,	100			μA
Logical "0" Sink	V_{OUT} = 2V	100			μA
Output Voltage Levels					
Logical "1"	V_{DD} = 6V I_OSource = 10μA	5.0			V
Logical "0"	I_OSink = −10μA			1.0	V

Functional Description

A connection diagram for the MM53107 is shown in *Figure 2* and a block diagram is shown in *Figure 1.*

TIME BASE

A precision time base is provided by the interconnection of a 2,097,152 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the Osc In and the Osc Out terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

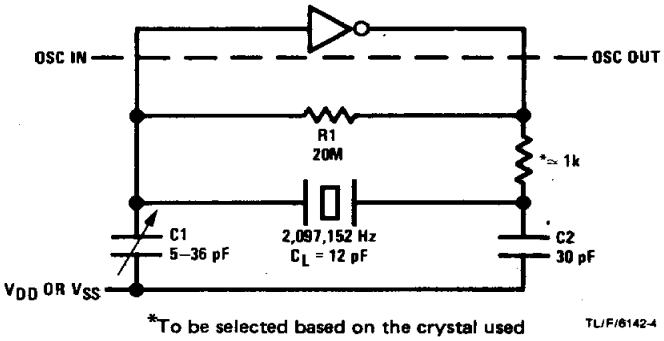
The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

DIVIDER

A pulse is generated when divider stages 1–4, 16 and 17 are in the correct state. This pulse is used to set or reset individual stages of the counter, the modulus of the counter is 34,952 to provide 60 Hz.

OUTPUT

The Divide Output is the input frequency divided by 34,952. The output is a push-pull output.



*To be selected based on the crystal used

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FIGURE 3. Crystal Oscillator Network

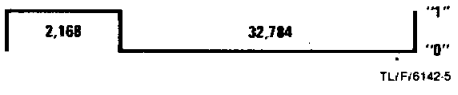

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FIGURE 4. Duty Cycle for MM53107