National Semiconductor

T-46-07-11

MM54HCT373/MM74HCT373 TRI-STATE® Octal D-Type Latch MM54HCT374/MM74HCT374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT373/MM74HCT373 octal D-type latches and MM54HCT374/MM74HCT374 Octal D-type flip flops advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The TRI-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT373/MM74HCT373 LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT374/MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

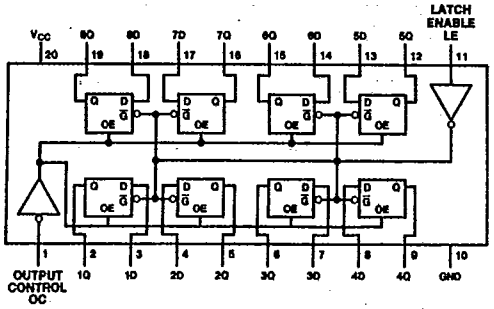
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



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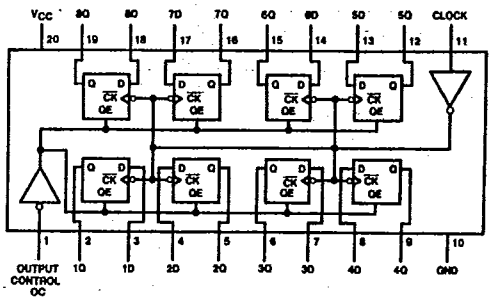
Top View

'HC373

Order Number MM54HCT373* or MM74HCT373*



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Top View

'HC374

Order Number MM54HCT374* or MM74HCT374*

*Please look into Section 8, Appendix D for availability of various package types.

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)		1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

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AC Electrical Characteristics MM54HCT373/MM74HCT373

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 45 pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 45 pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 5 pF R_L = 1 kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT373/MM74HCT373

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 50 pF C_L = 150 pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 50 pF C_L = 150 pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF C_L = 150 pF R_L = 1 kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC = V_{CC} OC = GND		5 52			pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table

'373

Output Control	LE	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

'374

Output Control	Clock	Data	Output (374)
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level

X = Don't Care

↑ = Transition from low-to-high

Z = High Impedance state

Q_0 = The level of the output before steady state input conditions were established.

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AC Electrical Characteristics MM54HCT374/MM74HCT374

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT374/MM74HCT374

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=50$ pF $C_L=150$ pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	8	12	15	18	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=V_{CC} OC=GND		5 58			pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

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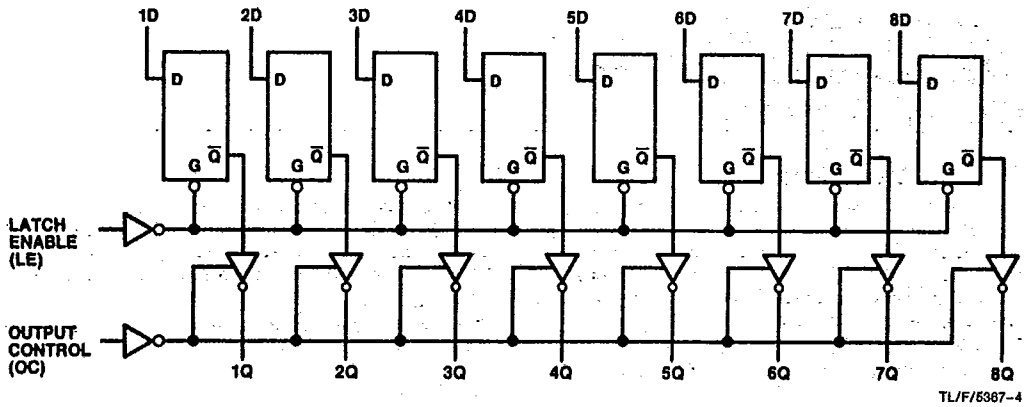
Logic Diagrams

MM54HCT373/MM74HCT373



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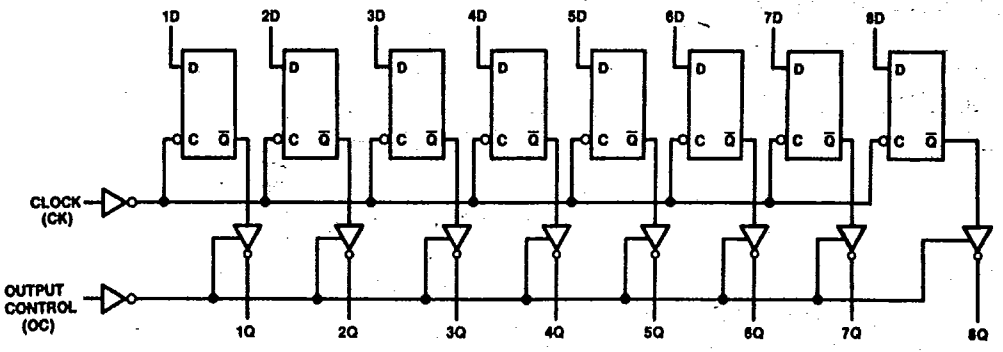

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