National Semiconductor

MILITARY DATA SHEET

MN100314-X REV 1A0

Original Creation Date: 10/30/95
Last Update Date: 08/28/96
Last Major Revision Date: 08/21/96

LOW POWER QUINT DIFFERENTIAL LINE RECEIVER

General Description

The 100314 is a monolithic quint differential line receiver with emitter-follower outputs. An internal reference supply (Vbb) is available for single-ended reception. When used in single-ended operation, the only mode allowed is to connect the complementary inputs to Vbb. Unlike other F100K ECL devices, the inputs do not have input pull-down resistors. Active current sources provide common-mode rejection of 1.0V in either the positive or negative direction. A defined output state exists if both inverting and non-inverting inputs are at the same potential between Vee and Vcc. The defined state is logic HIGH on the $\overline{Oa}$-$\overline{Oe}$ outputs.

Industry Part Number

100314

Prime Die

F314

NS Part Numbers

100314DMQB
100314FMQB
100314J-QMLV
100314W-QMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 35% power reduction of the F100114
- 2000V ESD protection
- Pin/function compatible with 100114
- Voltage compensated operating range = -4.2V to -5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

(Absolute Maximum Ratings)
(Note 1)

Storage Temperature (Tstg)	-65 C to +150 C
Maximum Junction Temperature (Tj)	
Ceramic	+175 C
Plastic	+150 C
Vee Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	Vee to +0.5V
Output Current (DC Output HIGH)	-50mA
ESD (Note 2)	$\geq$ 2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Military	-55 C to +125 C
Industrial	-40 C to +85 C
Supply Voltage (Vee)	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -5.7V, Tc= -55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	Vee= -5.7V, VM= -0.87V	1, 3	INPUTS		50	uA	1, 2
			1, 3	INPUTS		70	uA	3
ICBO	Input Leakage Current	Vee= -4.2V, VM= -4.2V	1, 3	INPUTS	-10		uA	1, 2, 3
VOH	Output HIGH Voltage	Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms To -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, LOADING:50 Ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VBBX	Output Reference Voltage	Vee=-4.2V, IM=0uA	1, 3	VBB		-1260	mV	1, 2, 3
VBBN	Output Reference Voltage	Vee=-5.7V, IM=-250uA	1, 3	VBB	-1380		mV	1, 2
		Vee=-5.7V, IM=-350uA	1, 3	VBB	-1396		mV	3
VIH	Input HIGH Voltage	$\overline{Dn}$ AT VBB	1, 3, 7	Dn	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage	$\overline{Dn}$ AT VBB	1, 3, 7	Dn	-1830	-1475	mV	1, 2, 3
VCM	Common Mode Voltage	VEE= -4.2/-5.7V	1, 3, 7	INPUTS	-2000	-500	mV	1, 2, 3
VDIFF	Input Voltage Differential	VEE= -4.2/-5.7V	1, 3, 7	INPUTS	150		mV	1, 2, 3
IEE	Power Supply Current	Vee= -4.2/-5.7V, VIN=VBB	1, 3	VEE	-65	-25	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vee Range: -4.2V to -5.7V, VCC=VCCA=GND, LOADING: 50 Ohms To -2.0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH/tPHL	Propagation Delay	Vee= -4.2/-5.7V	2, 4	Dn/$\overline{Dn}$ to On/$\overline{On}$	0.6	2.2	ns	9
			2, 4	Dn/$\overline{Dn}$ to On/$\overline{On}$	0.6	2.7	ns	10
			2, 4	Dn/$\overline{Dn}$ to On/$\overline{On}$	0.4	2.3	ns	11
tTLH/tTHL	Transition Time	Vee= -4.2/-5.7V	6	On/$\overline{On}$	0.2	1.4	ns	9, 10, 11

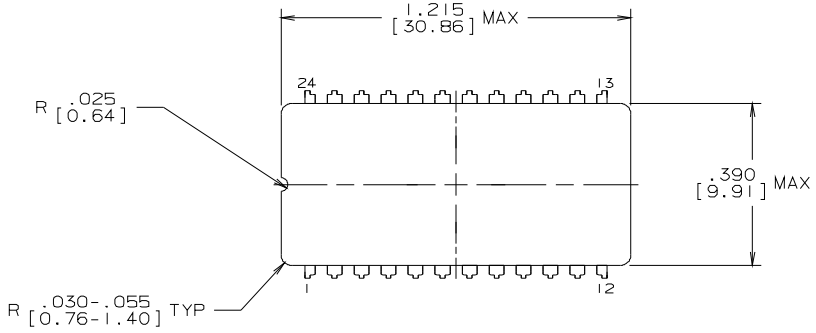
Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.
Note 2: For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A9, 10 & 11.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

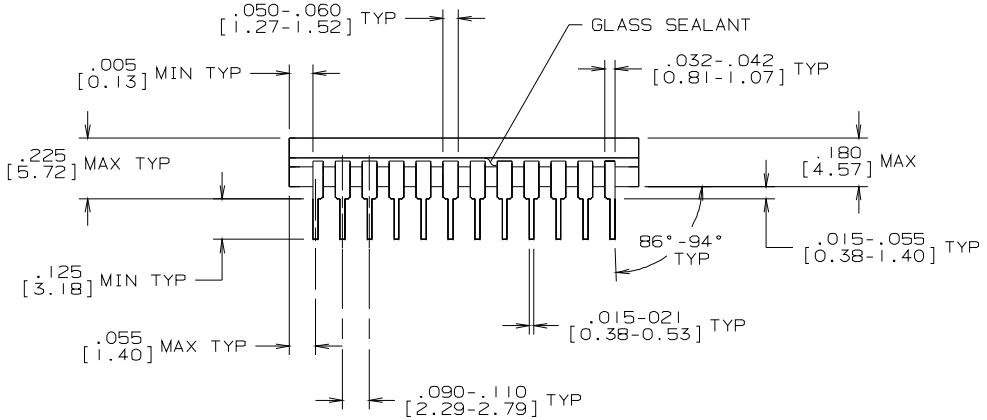
Graphics and Diagrams

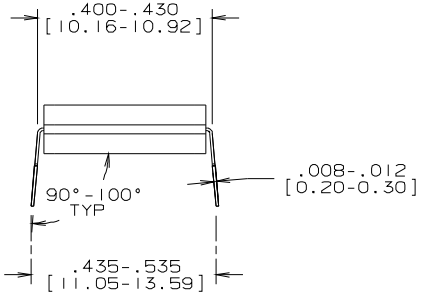
GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP(J), 24LD .400 CENTERS (P/P DWG)
P000043A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000044A	CERPAC, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPAC, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	REVISE AND REDRAW	09044	03/05/92	DEG/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
3. BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
4. NO JEDEC REGISTRATION AS OF 2/17/92.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN D.E.GRADY	03/05/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
MM

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 24 LEAD, .400 CENTERS

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-J24E	J

FORMERLY: N/A

SHEET 1 OF 1