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MICROCOMPUTER MN101C

MN101C38A/38C
LSI User's Manual

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Panasonic

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About This Manual

The MN101C38 series offers a variety of RAM and ROM combinations covering a wide range of applications. It also offers a choice of masked ROM version or user-programmable EPROM version.

ROM		RAM
32 K	MN101C38A	1536
48 K	MN101C38C	2048
48 K	MN101CP38C	2048

Unit: byte

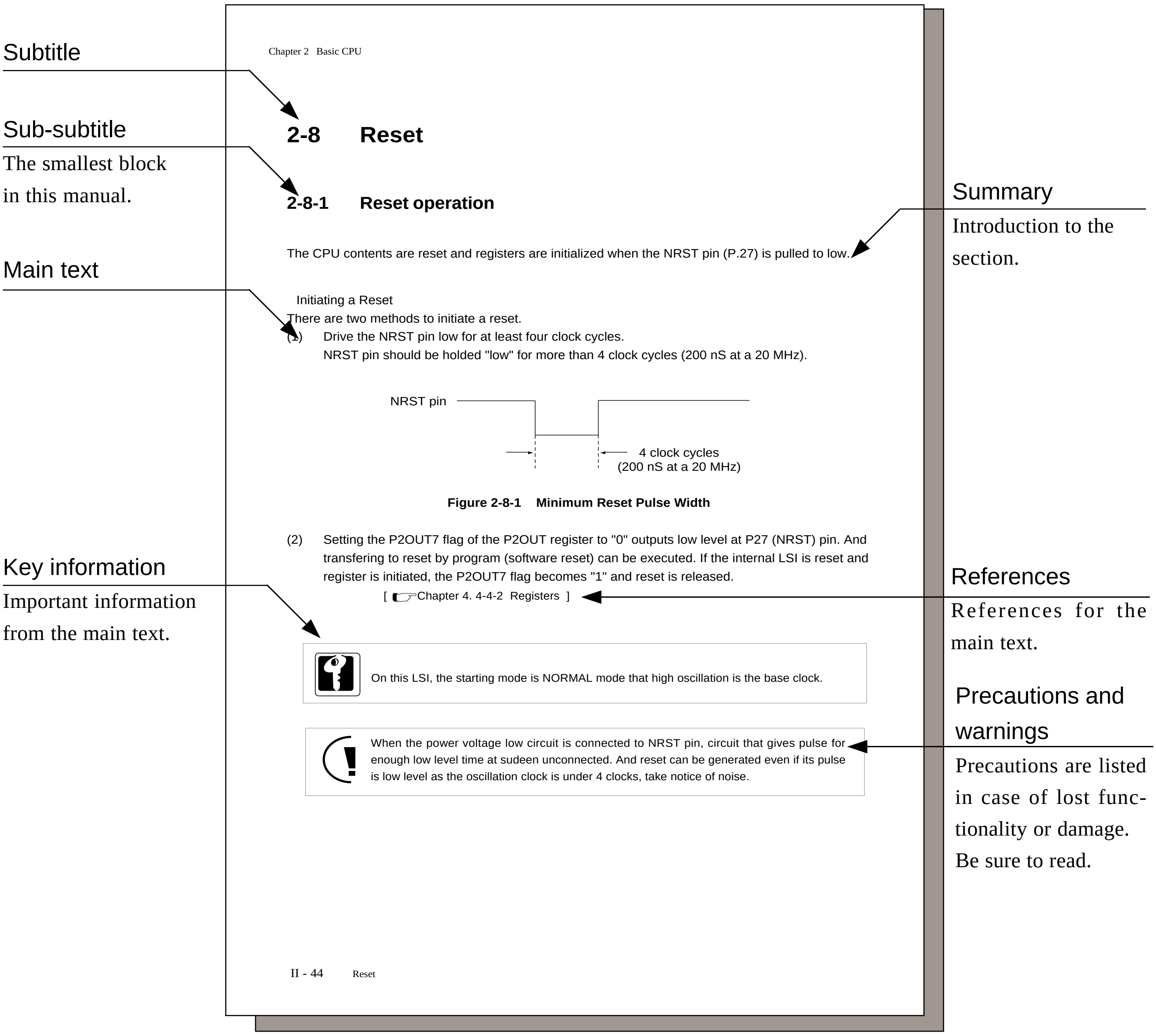
■Organization

In this LSI manual, the LSI functions are presented in the folowing order : overview, CPU basic functions, interrupt functions, port functions, timer functions, serial interface functions, and other peripheral hardware functions. Each section contains overview of function, block diagram, control register, operation, and setting example.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.

The layout and definition of each section are shown below.



■Finding Desired Information

This manual provides three methods for finding desired information quickly and easily.

(1) Consult the index at the front of the manual to locate the beginning of each section.

(2) Consult the table of contents at the front of the manual to locate desired titles.

(3) Chapter names are located at the top outer corner of each page, and section titles are located at the bottom outer corner of each page.

■Related Manuals

Note that the following related documents are available.

"MN101C Series LSI User's Manual"
<Describes the device hardware.>

"MN101C Series Instruction Manual"
<Describes the instruction set.>

"MN101C Series Cross-assembler User's Manual"
<Describes the assembler syntax and notation.>

"MN101C Series C Compiler User's Manual: Usage Guide"
<Describes the installation, the commands, and options of the C Compiler.>

"MN101C Series C Compiler User's Manual: Language Description"
<Describes the syntax of the C Compiler.>

"MN101C Series C Compiler User's Manual: Library Reference"
<Describes the standard library of the C Compiler.>

"MN101C Series C Source Code Debugger User's Manual"
<Describes the use of C source code debugger.>

"MN101C Series PanaX Series Installation Manual"
<Describes the installation of C compiler, cross-assembler and C source code debugger and the procedure for bringing up the in-circuit emulator.>

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Chapter 1 Overview

1-1 Overview

1-1-1 Overview

The MN101C series of 8-bit single-chip microcontrollers incorporate multiple types of peripheral functions. This chip series is well suited for VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC remote control, fax machine, musical instrument, and other applications.

The MN101C38 series brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. The MN101C38C has an internal 48 KB of ROM and 2,048 bytes of RAM. Peripheral functions include 5 external interrupts, 9 internal interrupts including NMI, 5 timer counters, 2 sets of serial interfaces, A/D converter, watchdog timer, synchronous output, buzzer output, and remote control output. The configuration of this microcontroller is well suited for application such as a system controller in a VCR selection timer, CD player, MD, or portable terminal.

With two oscillation systems (max. 20 MHz/32 kHz) contained on the chip, the system clock can be switched to high speed oscillation (**NORMAL mode**), or to low speed oscillation (**SLOW mode**). The system clock is generated by dividing the oscillation clock.

For example, in case of NORMAL mode, when the oscillation source (fosc) is 8 MHz, **minimum instructions execution time** is for 250 ns, and when fosc is 20 MHz, it is 100 ns.

2 types of packages available: 100-pin LQFP (under development) and 100-pin QFP

1-1-2 Product Summary

This manual describes the following models of the MN101C38 series. These products have same peripheral functions.

Table 1-1-1 Product Summary

Model	ROM Size	RAM Size	Classification
MN101C38A	32 KB	1.5 KB	Mask ROM version
MN101C38C	48 KB	2 KB	Mask ROM version
MN101CP38C	48 KB	2 KB	EPROM version

1-2 Hardware Functions

CPU Core **MN101C Core**

- LOAD-STORE architecture (3-stage pipeline)
- Half-byte instruction set / Handy addressing
- Memory addressing space is 256 KB
- Minimum instruction execution time

High speed mode	0.10 µs /	20 MHz	(4.5 V to 5.5 V)
	0.25 µs /	8 MHz	(2.7 V to 5.5 V)
	1.00 µs /	2 MHz	(2.0 V to 5.5 V) *1
Low speed mode	125 µs /	32.768 kHz	(2.0 V to 5.5 V) *1

*1 : EPROM vers. is 2.3 V to 5.5 V.

- Operation modes

NORMAL mode	(High speed oscillation)
SLOW mode	(Low speed oscillation)
HALT mode	
STOP mode	

Memory modes **<Single chip mode>**

Internal ROM *2	48 KB *3
Internal RAM *2	2 KB

<Memory expansion mode>

Internal ROM *2	48 KB *3
Internal RAM *2	2 KB
External ROM	128 KB
External RAM	4 KB

*2 : Differs depending upon the model. [Chapter 1. 1-1-2 Product Summary]

*3 : 1 byte of internal ROM is reserved for ROM option.
[Chapter 1. 1-6-1 ROM Option]

Interrupts

9 Internal interrupts

< Non-maskable interrupt (NMI) >

- Incorrect code execution interrupt and Watchdog timer interrupt

< Timer interrupts >

- Timer 2 interrupt
- Timer 3 interrupt
- Timer 4 interrupt
- Timer 5 interrupt
- Time base interrupt

< Serial interface interrupts >

- Serial interface 0 interrupt (Synchronous + Half-duplex UART)
- Serial interface 1 interrupt (Synchronous)

< A/D interrupt >

- A/D converter interrupt

< Automatic transfer controller (ATC) interrupt >

- Automatic transfer interrupt

5 External interrupts

- IRQ0 : Edge selectable. With / Without noise filter.
- IRQ1 : Edge selectable. With / Without noise filter.
  AC zero cross detector
- IRQ2 : Edge selectable. Synchronous output event.
- IRQ3 : Edge selectable.
- IRQ4 : Edge selectable. Key interrupt function.

Timers

5 timers (4 can operate independently)

- 8-bit timer for general use	1 set
- 8-bit timer for general use (UART baud rate timer)	1 set
- 8-bit free-running timer	1 set
Time base timer	1 set
- 16-bit timer for general use	1 set

Timer 2 (8-bit timer for general use)

- Square wave output (Timer pulse output), PWM output, Event count, Synchronous output event
- Clock source
  fs, fs/4, fx, TM2IO pin input

Timer 3 (8-bit timer for general use or UART baud rate timer)

- Square wave output (Timer pulse output), Event counter, Serial interface transfer clock output, 16-bit cascade connection function (connect to timer 2), Remote control carrier output
- Clock source
  fosc, fs/4, fs/16, TM3IO pin input

Timer 4 (16-bit timer for general use)

- Square wave output (Timer pulse output), PWM output, Event count Synchronous output event, Input capture function
- Clock source

  fosc, fs/4, fs/16, TM4IO pin input

Timer 5 (8-bit free-running timer, Time base timer)

❑ **8-bit free-running timer**

- Clock source

  fosc, fs/4, fx, fosc/2^{13}, fx/2^{13}

❑ **Time base timer**

- Interrupt generation cycle

  fosc/2^{7}, fosc/2^{8}, fosc/2^{9}, fosc/2^{10}, fosc/2^{13},

  fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}

at 32.768 kHz for low speed oscillation input
can be set to measure one minute intervals

Watchdog timer

- Watchdog timer frequency can be selected from fs/2^{16}, fs/2^{18}, fs/2^{20} as ROM option.

Remote control output

Based on the timer 0, and timer 3 output, a remote control carrier with duty cycle of 1/2 or 1/3 can be output.

Synchronous output

Timer synchronous output, Interrupt synchronous output

- Port 7 outputs the latched data, on the event timing of the synchronous output signal of timer 2 or 4, or of the external interrupt 2 (IRQ 2).

Buzzer output Output frequency can be selected from fs/2^{9}, fs/2^{10}, fs/2^{11}, fs/2^{12}.

A/D converter **10 bits × 8 channels input**

Serial interface **2 types**

Serial interface 0 (Half-duplex UART / Synchronous serial interface)

❑ **Synchronous serial interface**
- Transfer clock source
  fs/2, fs/4, fs/16, UART baud rate timer (timer 3) output,
  External clock
- MSB/LSB can be selected as the first bit to be transferred. Any transfer size from 1 to 8 bits can be selected.

❑ **Half-duplex UART (Baud rate timer : Timer 3)**
- Parity check, overrun error, framing error detection
- Transfer size 7 to 8 bits can be selected.
- When using timer 3, the transfer rate for a 12 MHz oscillation are 19200/9600/4800/2400/1200/300 bps.

Serial interface 1 (Synchronous serial interface)
- Transfer clock source
  fs/2, fs/8, fs/64, Timer 3 output, External clock
- MSB/LSB can be selected as the first bit to be transferred. Any transfer size 1 to 8 bits can be selected.

LED driver **5 pins**

LED driver

-LCD driver pins
  Segment output: 52 pins max. (SEG0 to 51)
    SEG 26 to 51 can be switched in 4-pin units to I/O ports.
    (Segments 26/30/34/38/42/46/50/52)
    Note: At reset, SEG 26 to 51 are input ports.
  Common output pins: 4 pins

-Display mode selection
  Static
  1/2 duty, 1/2 bias
  1/3 duty, 1/3 bias
  1/4 duty, 1/3 bias

-LCD driver clock
  The source clock is the main clock (fosc):
  $1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$
  The source clock is the sub-clock (fx):
  $1/2^{9}$, $1/2^{8}$, $1/2^{7}$, $1/2^{6}$

-LCD power supply
  Each of the V_{LC1}, V_{LC2}, and V_{LC3} pins supply power to the LCD.

Port	**I/O ports**	**45 pins (41 have dual functions)**
	- LED (large current) driver pins	5 pins (push-pull configuration)
	- Pins with dual function for external expansion mode	30 pins
	Input ports	**13 pins (all have dual functions)**
	- dual function for External interrupt	5 pins
	(One of which can also be used for zero-cross input.)	
	- dual function for A/D input	8 pins
	Special pins	
	- Analog reference voltage input pin	2 pins
	- Operation mode input pin	1 pin
	- Reset input pin	1 pin
	- Power pin	2 pins
	- Oscillation pin	4 pins
Package	**100-pin QFP (18 mm square / 0.65 mm pitch)** code name : QFP100-P-1818B **100-pin LQFP (14 mm square / 0.5 mm pitch)** code name : LQFP100-P-1414 *4 *4: under development	

1-3 Pin Description

1-3-1 Pin Configuration

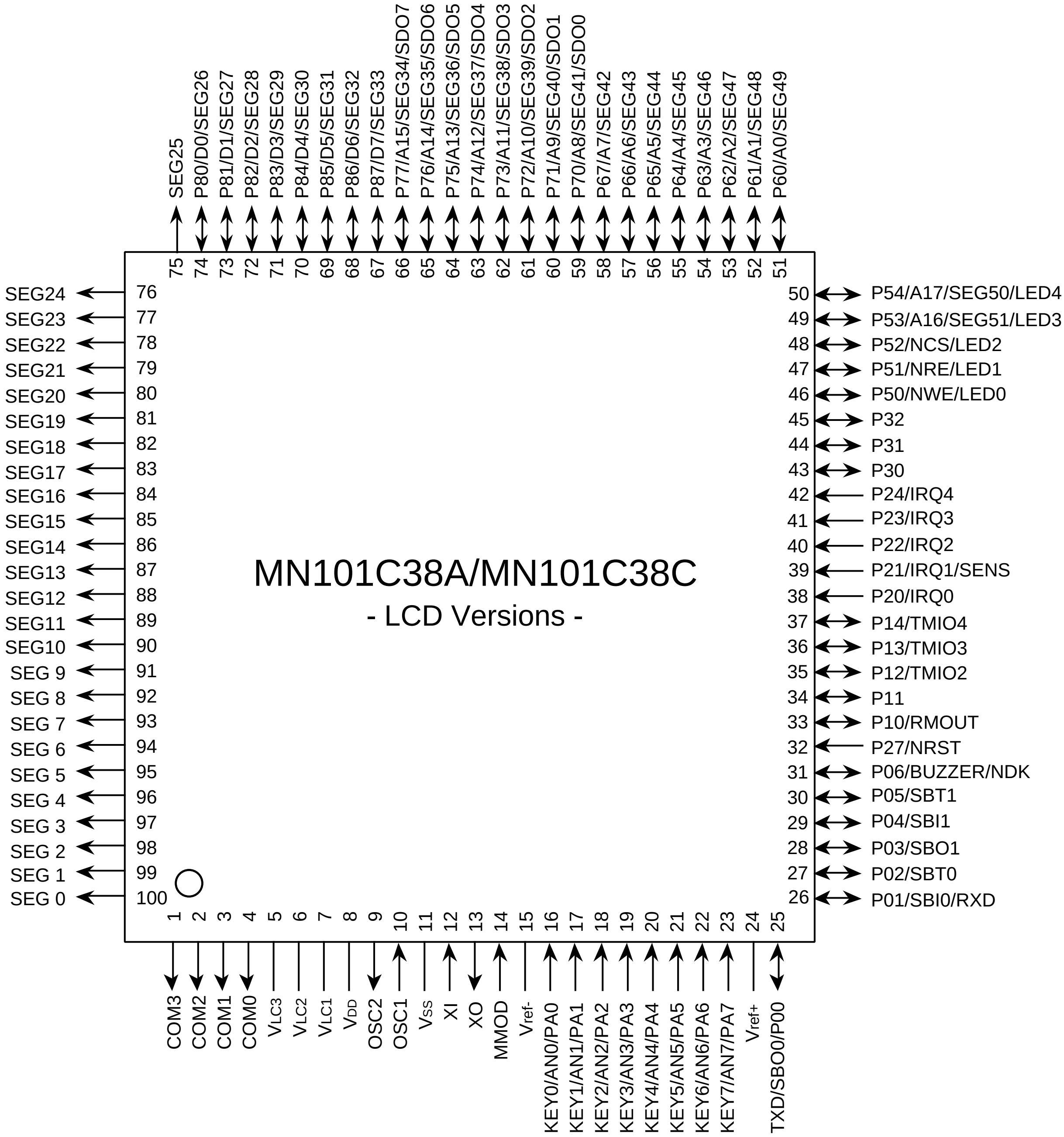


Figure 1-3-1 Pin Configuration (100QFP/LQFP : Top view)

1-3-2 Pin Specification

Table 1-3-1 Pin Specification (1/3)

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P00	SBO0	TXD	in/out	P0DIR0	P0PLU0	SBO0 : Serial Interface 0 transmission data output	TXD : UART transmission data output
P01	SBI0	RXD	in/out	P0DIR1	P0PLU1	SBI0 : Serial Interface 0 reception data input	RXD : UART reception data input
P02	SBT0		in/out	P0DIR2	P0PLU2	SBT0 : Serial Interface 0 clock I/O	
P03	SBO1		in/out	P0DIR3	P0PLU3	SBO1 : Serial Interface 1 transmission data output	
P04	SBI1		in/out	P0DIR4	P0PLU4	SBI1 : Serial Interface 1 reception data input	
P05	SBT1		in/out	P0DIR5	P0PLU5	SBT1 : Serial Interface 1 clock I/O	
P06	NDK	BUZZER	in/out	P0DIR6	P0PLU6	NDK : Data acknowledge signal	BUZZER : Buzzer output
P10	RMOUT		in/out	P1DIR0	P1PLU0	RMOUT : Remote control carrier output	
P11			in/out	P1DIR1	P1PLU1		
P12	TM2IO		in/out	P1DIR2	P1PLU2	TM2IO : Timer 2 I/O	
P13	TM3IO		in/out	P1DIR3	P1PLU3	TM3IO : Timer 3 I/O	
P14	TM4IO		in/out	P1DIR4	P1PLU4	TM4IO : Timer 4 I/O	
P20	IRQ0		in	-	P2PLU0	IRQ0 : External interrupt 0	
P21	IRQ1	SENS	in	-	P2PLU1	IRQ1 : External interrupt 1	SENS : Zero-cross input
P22	IRQ2		in	-	P2PLU2	IRQ2 : External interrupt 2	
P23	IRQ3		in	-	P2PLU3	IRQ3 : External interrupt 3	
P24	IRQ4		in	-	P2PLU4	IRQ4 : External interrupt 4	
P27	NRST		in	-	-	NRST : Reset	
P30			in/out	P3DIR0	P3PLU0		
P31			in/out	P3DIR1	P3PLU1		
P32			in/out	P3DIR2	P3PLU2		
P50	NWE	LED0	in/out	P5DIR0	P5PLU0	NWE : Write enable signal	LED : driving pin 0
P51	NRE	LED1	in/out	P5DIR1	P5PLU1	NRE : Read enable signal	LED : driving pin 1
P52	NCS	LED2	in/out	P5DIR2	P5PLU2	NCS : Chip select signal	LED : driving pin 2
P53	A16	LED3 SEG51	in/out	P5DIR3	P5PLU3	A16 : Address output (bp16)	LED : driving pin 3 SEG51 : LCD segment output 51
P54	A17	LED4 SEG50	in/out	P5DIR4	P5PLU4	A17 : Address output (bp17)	LED : driving pin 4 SEG50 : LCD segment output 50

Table 1-3-2 Pin Specification (2/3)

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P60	A0	SEG49	in/out	P6DIR0	P6PLU0	A0 : Address output (bp0)	SEG49 : LCD segment output 49
P61	A1	SEG48	in/out	P6DIR1	P6PLU1	A1 : Address output (bp1)	SEG48 : LCD segment output 48
P62	A2	SEG47	in/out	P6DIR2	P6PLU2	A2 : Address output (bp2)	SEG47 : LCD segment output 47
P63	A3	SEG46	in/out	P6DIR3	P6PLU3	A3 : Address output (bp3)	SEG46 : LCD segment output 46
P64	A4	SEG45	in/out	P6DIR4	P6PLU4	A4 : Address output (bp4)	SEG45 : LCD segment output 45
P65	A5	SEG44	in/out	P6DIR5	P6PLU5	A5 : Address output (bp5)	SEG44 : LCD segment output 44
P66	A6	SEG43	in/out	P6DIR6	P6PLU6	A6 : Address output (bp6)	SEG43 : LCD segment output 43
P67	A7	SEG42	in/out	P6DIR7	P6PLU7	A7 : Address output (bp7)	SEG42 : LCD segment output 42
P70	A8	SEG41 SDO0	in/out	P7DIR0	P7PLUD0	A8 : Address output (bp8)	SEG41 : LCD segment output 41 SDO0 : Synchronous output 0
P71	A9	SEG41 SDO1	in/out	P7DIR1	P7PLUD1	A9 : Address output (bp9)	SEG40 : LCD segment output 40 SDO1 : Synchronous output 1
P72	A10	SEG41 SDO2	in/out	P7DIR2	P7PLUD2	A10 : Address output (bp10)	SEG39 : LCD segment output 39 SDO2 : Synchronous output 2
P73	A11	SEG41 SDO3	in/out	P7DIR3	P7PLUD3	A11 : Address output (bp11)	SEG38 : LCD segment output 38 SDO3 : Synchronous output 3
P74	A12	SEG41 SDO4	in/out	P7DIR4	P7PLUD4	A12 : Address output (bp12)	SEG37 : LCD segment output 37 SDO4 : Synchronous output 4
P75	A13	SEG41 SDO5	in/out	P7DIR5	P7PLUD5	A13 : Address output (bp13)	SEG36 : LCD segment output 36 SDO5 : Synchronous output 5
P76	A14	SEG41 SDO6	in/out	P7DIR6	P7PLUD6	A14 : Address output (bp14)	SEG35: LCD segment output 35 SDO6 : Synchronous output 6
P77	A15	SEG41 SDO7	in/out	P7DIR7	P7PLUD7	A15 : Address output (bp15)	SEG34 : LCD segment output 34 SDO7 : Synchronous output 7
P80	D0	SEG26	in/out	P8DIR0	P8PLU0	D0 : Data I/O (bp0)	SEG26 : LCD segment output 26
P81	D1	SEG27	in/out	P8DIR1	P8PLU1	D1 : Data I/O (bp1)	SEG27 : LCD segment output 27
P82	D2	SEG28	in/out	P8DIR2	P8PLU2	D2 : Data I/O (bp2)	SEG28 : LCD segment output 28
P83	D3	SEG29	in/out	P8DIR3	P8PLU3	D3 : Data I/O (bp3)	SEG29 : LCD segment output 29
P84	D4	SEG30	in/out	P8DIR4	P8PLU4	D4 : Data I/O (bp4)	SEG30 : LCD segment output 30
P85	D5	SEG31	in/out	P8DIR5	P8PLU5	D5 : Data I/O (bp5)	SEG31 : LCD segment output 31
P86	D6	SEG32	in/out	P8DIR6	P8PLU6	D6 : Data I/O (bp6)	SEG32 : LCD segment output 32
P87	D7	SEG33	in/out	P8DIR7	P8PLU7	D7 : Data I/O (bp7)	SEG33 : LCD segment output 33
PA0	AN0	KEY0	in	-	PAPLUD0	AN0 : Analog 0 input	KEY0 : KEY interrupt input 0
PA1	AN1	KEY1	in	-	PAPLUD1	AN1 : Analog 1 input	KEY1 : KEY interrupt input 1
PA2	AN2	KEY2	in	-	PAPLUD2	AN2 : Analog 2 input	KEY2 : KEY interrupt input 2
PA3	AN3	KEY3	in	-	PAPLUD3	AN3 : Analog 3 input	KEY3 : KEY interrupt input 3
PA4	AN4	KEY4	in	-	PAPLUD4	AN4 : Analog 4 input	KEY4 : KEY interrupt input 4
PA5	AN5	KEY5	in	-	PAPLUD5	AN5 : Analog 5 input	KEY5 : KEY interrupt input 5
PA6	AN6	KEY6	in	-	PAPLUD6	AN6 : Analog 6 input	KEY6 : KEY interrupt input 6
PA7	AN7	KEY7	in	-	PAPLUD7	AN7 : Analog 7 input	KEY7 : KEY interrupt input 7

Table 1-3-2 Pin Specification (3/3)

Pins	Special Functions	I/O	Direction Control	Pin Control	Functions Description
	SEG0	out	-	-	SEG0 : LCD segment output 0
	SEG1	out	-	-	SEG1 : LCD segment output 1
	SEG2	out	-	-	SEG2 : LCD segment output 2
	SEG3	out	-	-	SEG3 : LCD segment output 3
	SEG4	out	-	-	SEG4 : LCD segment output 4
	SEG5	out	-	-	SEG5 : LCD segment output 5
	SEG6	out	-	-	SEG6 : LCD segment output 6
	SEG7	out	-	-	SEG7 : LCD segment output 7
	SEG8	out	-	-	SEG8 : LCD segment output 8
	SEG9	out	-	-	SEG9 : LCD segment output 9
	SEG10	out	-	-	SEG10: LCD segment output 10
	SEG11	out	-	-	SEG11 : LCD segment output 11
	SEG12	out	-	-	SEG12 : LCD segment output 12
	SEG13	out	-	-	SEG13 : LCD segment output 13
	SEG14	out	-	-	SEG14 : LCD segment output 14
	SEG15	out	-	-	SEG15 : LCD segment output 15
	SEG16	out	-	-	SEG16 : LCD segment output 16
	SEG17	out	-	-	SEG17 : LCD segment output 17
	SEG18	out	-	-	SEG18 : LCD segment output 18
	SEG19	out	-	-	SEG19 : LCD segment output 19
	SEG20	out	-	-	SEG20 : LCD segment output 20
	SEG21	out	-	-	SEG21 : LCD segment output 21
	SEG22	out	-	-	SEG22 : LCD segment output 22
	SEG23	out	-	-	SEG23 : LCD segment output 23
	SEG24	out	-	-	SEG24 : LCD segment output 24
	SEG25	out	-	-	SEG25 : LCD segment output 25
	COM0	out	-	-	COM0 : LCD common output 0
	COM1	out	-	-	COM1 : LCD common output 1
	COM2	out	-	-	COM2 : LCD common output 2
	COM3	out	-	-	COM3 : LCD common output 3

1-3-3 Pin Functions

Table 1-3-3 Pin Function Summary (1/7)

sName	No. (100 pin)	I/O	Other Function	Function	Description
V_{SS} V_{DD}	11 8			Power supply pin	Supply 2.0 V to 5.5 V to V_{DD} and 0 V to V_{SS}.
OSC1 OSC2	10 9	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	12 13	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. The chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to V_{SS} and leave XO open.
NRST	32	Input	P27	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ.35 kΩ). Setting this pin low initializes the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if "0" is written to P27 and the reset is initiated by software, a low level will be output. The output has an N-ch open-drain configuration. If a capacitor is to be inserted between NRST and V_{SS}, it is recommended that a discharge diode be placed between NRST and V_{DD}.
P00 P01 P02 P03 P04 P05 P06	25 26 27 28 29 30 31	I/O	SBO0, TXD SBI0, RXD SBT0 SBO1 SBI1 SBT1 NDK, BUZZER	I/O port 0	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P10 P11 P12 P13 P14	33 34 35 36 37	I/O	RMOUT TM2IO TM3IO TM4IO	I/O port 1	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

Table 1-3-4 Pin Function Summary (2/7)

Name	No. (80 pin)	I/O	Other Function	Function	Description
P20 P21 P22 P23 P24	38 39 40 41 42	Input	IRQ0 IRQ1, SENS IRQ2 IRQ3 IRQ4	Input port 2	5-bit input port. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, pull-up resistors are disabled.
P27	32	Input	NRST	Input port 2	P27 has an n-channel open-drain configuration. When "0" is written and the reset is initiated by software, a low level will be output.
P30 P31 P32	43 44 45	I/O		I/O port 3	3-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P50 P51 P52 P53 P54	46 47 48 49 50	I/O	NWE, LED0 NRE, LED1 NCS, LED2 A16, LED3, SEG51 A17, LED4, SEG50	I/O port 5	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, when single chip mode is selected, the input mode is selected and pull-up resistors for P50 to P54 are disabled (high impedance output). When configured as outputs, P50 to P54 can drive LED directly, and also, P53 and P54 can drive segments.
P60 P61 P62 P63 P64 P65 P66 P67	51 52 53 54 55 56 57 58	I/O	A0, SEG49 A1, SEG48 A2, SEG47 A3, SEG46 A4, SEG45 A5, SEG44 A6, SEG43 A7, SEG42	I/O port 6	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, when single chip mode is selected, the input mode is selected and pull-up resistors for P60 to P67 are disabled (high impedance output). When configured as outputs, these pins can drive segments.
P70 P71 P72 P73 P73 P75 P76 P77	59 60 61 62 63 64 65 66	I/O	A8, SD0O, SEG41 A9, SDO1, SEG40 A10, SDO2, SEG39 A11, SDO3, SEG38 A12, SDO4, SEG37 A13, SDO5, SEG36 A14, SDO6, SEG35 A15, SDO7, SEG34	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up or pull-down resistor for each bit can be selected individually by the P7PLUD register. However, pull-up and pull-down resistors cannot be mixed. This port contains a synchronous output function for external 2 interrupt, timer 1 interrupt, timer 2 interrupt and timer 4 interrupt. At reset, when single-chip mode is selected, the input mode is selected and pull-up resistors for P70 to P77 are disabled (high impedance output). When configured as outputs, these pins can drive segments.

Table 1-3-5 Pin Function Summary (3/7)

Name	No. (80 pin)	I/O	Other Function	Function	Description
P80 P81 P82 P83 P84 P85 P86 P87	74 73 72 71 70 69 68 67	I/O	D0, SEG26 D1, SEG27 D2, SEG28 D3, SEG29 D4, SEG30 D5, SEG31 D6, SEG32 D7, SEG33	I/O port 8	8-bit CMOS tri-state I/O port. Each individual bit can be switched to an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, when single-chip mode is selected, the input mode is selected and pull-up resistors for P80 to P87 are disabled (high impedance output). When configured as outputs, these pins can drive segments.
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	16 17 18 19 20 21 22 23	Input	AN0, KEY0 AN1, KEY1 AN2, KEY2 AN3, KEY3 AN4, KEY4 AN5, KEY5 AN6, KEY6 AN7, KEY7	Input port A	8-bit input port. A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD resister. However, pull-up and pull-down resistors cannot be mixed. At reset, the PA0 to PA7 input mode is selected and pull- up resistors are disabled.
SBO0 SBO1	25 28	Output	P00, TXD P03	Serial interface transmission data output pins	Transmission data input pins for serial interfaces 0 to 1. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistors can be selected by the P0PLU register. Select output mode by the P0DIR register and serial data output mode by serial mode register (SC0MD3 and SC1MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0 SBI1	26 29	Input	P01, RXD P04	Serial interface received data input pins	Receive data input pins for serial interfaces 0 to 1. Pull-up resistors can be selected by the P0PLU register Select input mode by the P0DIR register, and serial input mode by the serial mode register (SC0MD3 and SC1MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0 SBT1	27 30	I/O	P02 P05	Serial interface clock I/O pins	Clock I/O pins for serial interfaces 0 to 1. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Push-pull resistors can be selected by the P0PLU register. Select clock I/O for each communication mode by the P0DIR register and serial mode register (SC0MD3 and SC1MD1). These can be used as normal I/O pins when the serial interface is not used.

Table 1-3-6 Pin Function Summary (4/7)

Name	No. (80 pin)	I/O	Other Function	Function	Description
TXD	25	Output	SBO0, P00	UART transmission data output pin	In the serial interface in UART mode, this pin is configured as the transmission data output pin. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistors can be selected by the P0PLU resister. Select output mode by the P0DIR register, and serial data output by serial 0 mode register 3 (SC0MD3). This can be used as normal I/O pin when the serial interface is not used.
RXD	26	Input	SBI0, P01	UART received data input pin	In the serial interface in UART mode, this pis is configured as the received data input pin. Pull-up resistors can be selected by the P0PLU register. Set this pin to the input mode by the P0DIR register, and to the serial input mode by the serial 0 mode register 3 (SC0MD3). This can be used as normal I/O pin when the serial interface is not used.
TM2IO TM3IO	35 36	I/O	P12 P13	Timer I/O pins	Event counter clock input pins, timer output and PWM signal output pins for 8-bit timers 2 to 3. To use these pins as event clock inputs, configure them as inputs by the P1DIR register. When the pins are used as inputs, pull-up resistors can be specified by the P1PLU register. For timer output, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. When not used for timer I/O, these can be used as normal I/O pins.
RMOUT	33	I/O	P10, TM0IO	Remote control transmission signal output pin	Output pin for remote control transmission signal with a carrier signal. For remote control carrier output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. Also, set to the remote control carrier output by the remote control carrier output control register (RMCTR). This can be used as a normal I/O pin when remote control is not used.
BUZZER	31	Output	P06, NDK	Buzzer output	Piezoelectric buzzer driver pin. The driving frequency can be selected by the DLYCTR register. Select output mode by the P0DIR register and select P06 buzzer output by the DLYCTR register. When not used for buzzer output, this pin can be used as a normal I/O pin.

Table 1-3-7 Pin Function Summary (5/7)

Name	No. (80 pin)	I/O	Other Function	Function	Description
TM4IO	37	I/O	P14	Timer I/O pin	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer 4. To use this pin as event clock input, configure this as input by the P1DIR register. In the input mode, pull-up resistors can be selected by the P1PLU register. For timer output, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD), and set to the output mode by the P1DIR register. When not used for timer I/O, this can be used as normal I/O pin.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	59 60 61 62 63 64 65 66	Output	P70, A8, SEG41 P71, A9, SEG40 P72, A10, SEG39 P73, A11, SEG38 P74, A12, SEG37 P75, A13, SEG36 P76, A14, SEG35 P77, A15, SEG34	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the synchronous output control register (SYSMD). Set to the output mode by the P1DIR register. When not used for synchronous output, these pins can be used as a normal I/O pins.
V_{REF+} V_{REF-}	24 15	- -		+power supply for A/D converter - power supply for A/D converter	Reference power supply pins for the A/D converter. Normally, the values of V_{REF+}=V_{DD} and V_{REF-}=V_{SS} are used.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	16 17 18 19 20 21 22 23	Input	PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	Analog input pins	Analog input pins for an 8-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	38 39 40 41 42	Input	P20 P21, SENS P22 P23 P24	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 4 can be selected through the IRQnICR register. IRQ1 is an external interrupt pin that is able to deternine AC zero crossings. When these are not used for interrupts, these can be used as normal input pins.
SENS	39	Input	P21, IRQ1	AC zero-cross detection input pin	An input pin for an AC zero-cross detection circuit. The AC zero-cross detection circuit outputs a high level when the input is at an intermediate level. Otherwise, it outputs a low level voltage all the times. SENS input signal is connected to the P21 input circuit and the IQR1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as a normal P21 input. The selection is set by the P21IM flag of the FLOAT1 register.

Table 1-3-8 Pin Function Summary (6/7)

Name	No. (80 pin)	I/O	Other Function	Function	Description
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	16 17 18 19 20 21 22 23	Input	PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	Key interrupt input pins	Input pins for interrupt based on ORed result of pin inputs. Key input pin for 2 bits can be selected individually by the key interrupt control register (P4IMD). When not used for KEY input, these pins can be used as normal I/O pins.
V_{LC1} V_{LC2} V_{LC3}	7 6 5			LCD power supply	These pins supply power to the LCDs. V_{DD} is normally devided by resistors to supply this voltage.
COM0 COM1 COM2 COM3	1 2 3 4	Output		LCD common outputs	These pins output a common signal with the required timing to the LCD display. Also, they may be connected to the common pins on the LCD panel.
LED0 LED1 LED2 LED3 LED4	46 47 48 49 50	Output	P50, NWE P51, NRE P52, NCS P53, A16, SEG51 P54, A17, SEG50	LED (large current) output	LED driving pins.
SEG51 SEG50 SEG49 SEG48 SEG47 SEG46 SEG45 SEG44 SEG43 SEG42 SEG41 SEG40 SEG39 SEG38 SEG37 SEG36 SEG35 SEG34 SEG33 SEG32 SEG31 SEG30 SEG29 SEG28 SEG27 SEG26	49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74	Output	P53, A16, LED3 P54, A17, LED4 P60, A0 P61, A1 P62, A2 P63, A3 P64, A4 P65, A5 P66, A6 P67, A7 P70, A8, SDO0 P71, A9, SDO1 P72, A10, SDO2 P73, A11, SDO3 P74, A12, SDO4 P75, A13, SDO5 P76, A14, SDO6 P77, A15, SDO7 P87, D7 P86, D6 P85, D5 P84, D4 P83, D3 P82, D2 P81, D1 P80, D0	LCD segment output	Connect to segment pins on the LCD panel. These pins are allocated to PORT53, 54, 60 to 67, 70 to 77, 80 to 87. When segments are not used, these pins can be used as normal I/O pins. At reset, all pins are set to the input mode.

Table 1-3-9 Pin Function Summary (7/7)

Name	No. (80 pin)	I/O	Other Function	Function	Description
SEG25 SEG24 SEG23 SEG22 SEG21 SEG20 SEG19 SEG18 SEG17 SEG16 SEG15 SEG14 SEG13 SEG12 SEG11 SEG10 SEG9 SEG8 SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 SEG0	75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100	Output		LCD segment output	Connect to segment pins on the LCD panel.
MMOD	14	Input		Memory mode switch input pin	This pin sets the memory expansion mode. Set the input low. Do not change the setup after reset.
NWE NRE NCS NDK A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 D0 D1 D2 D3 D4 D5 D6 D7	46 47 48 31 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 49 50 74 73 72 71 70 69 68 67	Output Output Output Input Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output I/O I/O I/O I/O I/O I/O I/O I/O	P50 P51 P52 P06, BUZZER P60, SEG49 P61, SEG48 P62, SEG47 P63, SEG46 P64, SEG45 P65, SEG44 P66, SEG43 P67, SEG42 P70, SDO0, SEG41 P71, SDO1, SEG40 P72, SDO2, SEG39 P73, SDO3, SEG38 P74, SDO4, SEG37 P75, SDO5, SEG36 P76, SDO6, SEG35 P77, SDO7, SEG34 P53, SEG51, LED3 P54, SEG50, LED4 P80, SEG26 P81, SEG27 P82, SEG28 P83, SEG29 P84, SEG30 P85, SEG31 P86, SEG32 P87, SEG33	Write enable pin (Active low) Read enable pin (Active low) Chip select pin (Active low) Data acknowledge pin (Active low) Address pin Data pin	Memory control signals for an expanded memory space external to this LSI. NWE is a strobe signal that is output for writing to external memory. NRE is a strobe signal that is output for reading from external memory. NCS is a chip select signal that is output when external memory is accessed. NDK is an acknowledge signal that indicates the external memory access is complete. A0 to A17 are address signals output to external memory. D0 to D7 are data signals that input data to and output data from external memory.

1-4 Block Diagram

1-4-1 Block Diagram

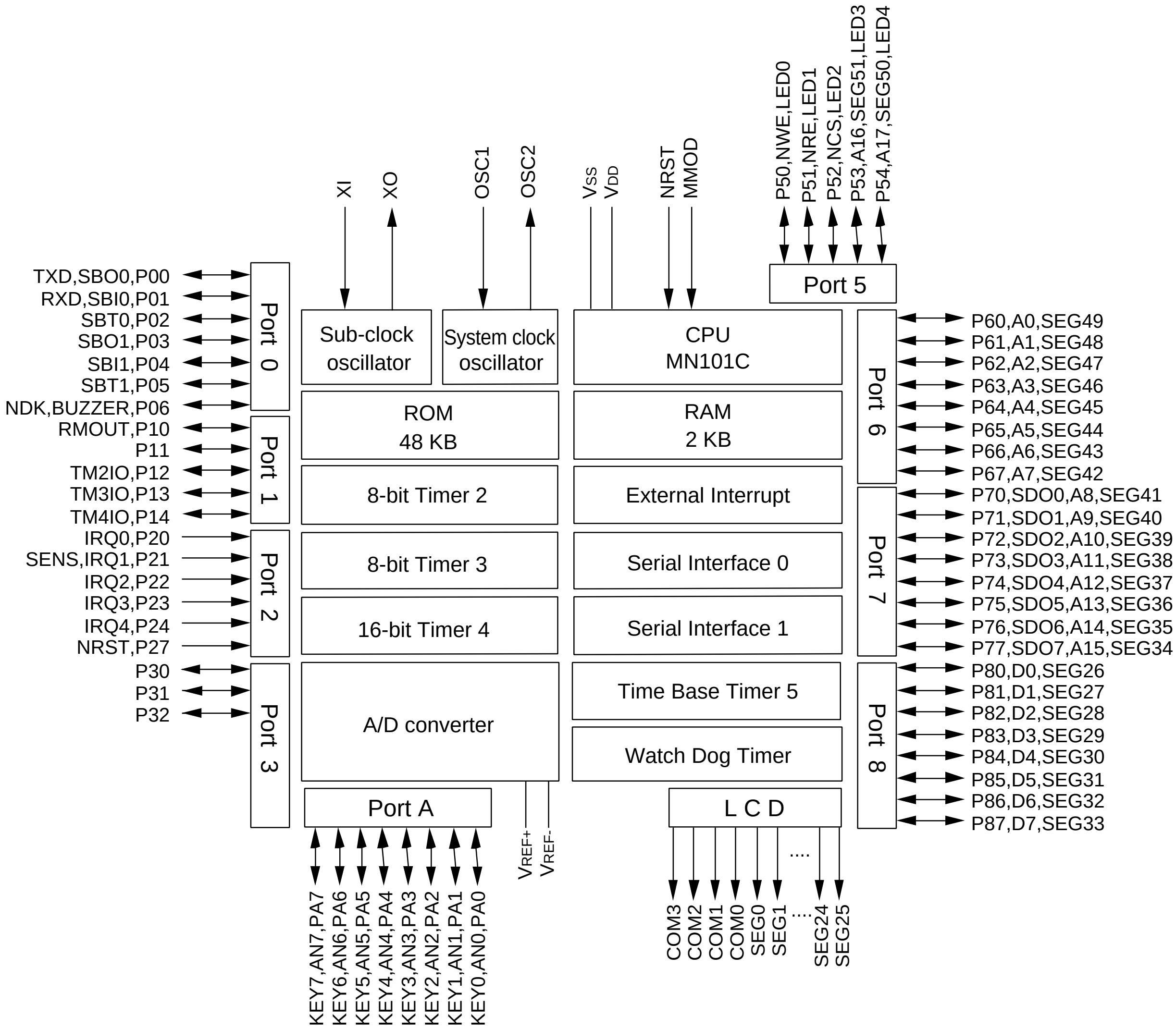


Figure 1-4-1 Block Diagram

1-5 Electrical Characteristics

This LSI user's manual describes the standard specification. System clock (fs) is : 1/2 of high speed oscillation at NORMAL mode, or 1/4 of low speed oscillation at SLOW mode. Please ask our sales offices for its own product specifications.

Model / Contents	MN101C38 series
Structure	CMOS integrated circuit
Application	General purpose
Function	8-bit single-chip microcontroller

1-5-1 Absolute Maximum Ratings

V_{SS} = 0 V

No.	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD}	- 0.3 to +7.0	V
2	Input clamp current (SENS)		I_C	- 500 to +500	µA
3	Input pin voltage		V_I	- 0.3 to V_{DD} +0.3	V
4	Output pin voltage		V_O	- 0.3 to V_{DD} +0.3	
5	I/O pin voltage		V_{IO1}	- 0.3 to V_{DD} +0.3	
6	Peak output current	Port 5	I_{OL1} (peak)	40	mA
7		Other than port 5	I_{OL2} (peak)	20	
8		All pins	I_{OH} (peak)	- 10	
9	Average output current *1	Port 5	I_{OL1} (avg)	20	
10		Other than port 5	I_{OL2} (avg)	15	
11		All pins	I_{OH} (avg)	- 5	
12	Power dissipation		P_D	400 (Ta = 85°C)	mW
13	Operating ambient temperature		T_{opr}	- 40 to +85	°C
14	Storage temperature		T_{stg}	- 55 to +125	

*1 Applied to any 100 ms period.

Connect at least one bypass capacitor of 0.1 µF or larger between the power supply pin and the ground for latch-up prevention.

The absolute maximum ratings are the limit values beyond which the LSI may be damaged and proper operation is not assured.

1-5-2 Operating Conditions [NORMAL mode : fs=fosc/2, SLOW mode : fs=fx/4]

Ta = -40 °C to +85 °C V_{SS} = 0 V
EPROM vers. is in ( ).

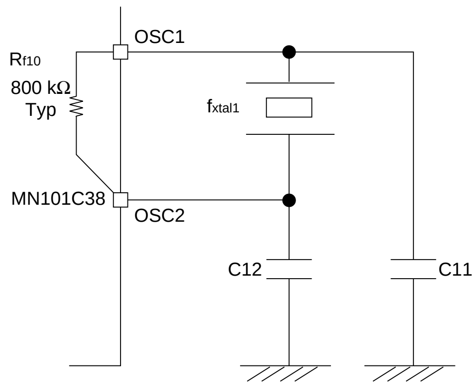
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *2							
1	Power supply voltage	V_{DD1}	1.0 MHz ≤ fosc ≤ 20.0 MHz	4.5		5.5	V
2		V_{DD2}	1.0 MHz ≤ fosc ≤ 8.00 MHz	2.7		5.5	
3		V_{DD3}	1.0 MHz ≤ fosc ≤ 4.20 MHz	2.3		5.5	
4		V_{DD4}	1.0 MHz ≤ fosc ≤ 2.00 MHz	2.0 (2.3)		5.5	
5		V_{DD5}	32.768 kHz ≤ fx ≤ 100 kHz	2.0 (2.3)		5.5	
6	Voltage to maintain RAM data	V_{DD6}	During STOP mode	1.8		5.5	
Operation speed *3							
7	Miniumum instruction execution time	t_{c1}	V_{DD} = 4.5 V to 5.5 V	0.100		2.00	µs
8		t_{c2}	V_{DD} = 2.7 V to 5.5 V	0.250		2.00	
9		t_{c3}	V_{DD} = 2.3 V to 5.5 V	0.480		2.00	
10		t_{c4}	V_{DD} = 2.0 V (2.3 V) to 5.5 V	1.00		2.00	
11		t_{c5}	V_{DD} = 2.0 V (2.3 V) to 5.5 V	40.0		122.1	

*2 fosc: the input clock frequency to OSC1
fx: the input clock frequency to XI

*3 tc1, tc2, tc3, tc4 : where OSC1 is the CPU clock
tc5 : where XI is the CPU clock

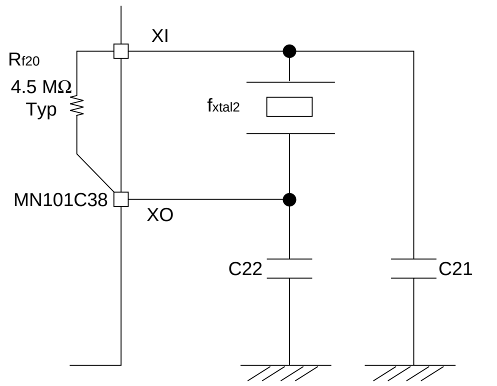
Ta = -40 °C to +85 °C V_{SS} = 0 V
EPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Crystal oscillator 1 Fig. 1-5-1							
12	Crystal frequency	f_{xtal1}	V_{DD} = depending on operating voltage *4	2.0		20.0	MHz
13	External capacitors *	C_{11}			20		pF
14		C_{12}			20		
15	Internal feedback resistor	R_{f10}	V_{DD} = 5.0 V		800		kΩ
Crystal oscillator 2 Fig. 1-5-2							
16	Crystal frequency	f_{xtal2}	V_{DD} = 2.0 V (2.3 V) to 5.5 V		32.768		kHz
17	External capasitors *	C_{21}			20		pF
18		C_{22}			20		
19	Internal feedback resistor	R_{f20}	V_{DD} = 5.0 V		4.5		MΩ



The instruction cycle is twice the clock cycle.
The feedback resistor is built-in.

Figure 1-5-1 Crystal Oscillator 1



The instruction cycle is twice the clock cycle.
The feedback resistor is built-in.

Figure 1-5-2 Crystal Oscillator 2

*4 Refer to the values of Operating Conditions 1 to 4 on supply voltage during operation.

* Note that you should determine the optimum value after a sample product is evaluated by the oscillator manufacturer, because the optimum value of the external capacitors C11, C12, C21 and C22 differ on the oscillator which is used. Especially when the micro-computer is used on low voltage, you must implement enough matching evaluation with the oscillator.

Ta = -40 °C to +85 °C V_{DD} = 5.0 V V_{SS} = 0 V
EPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
External clock input 1 OSC1 (OSC2 is unconnected)							
20	Clock frequency	f_{osc}		1.0		20.0	MHz
21	High level pulse width	t_{wh1}	*5 Fig. 1-5-3				ns
22	Low level pulse width	t_{wl1}	*5 Fig. 1-5-3				ns
23	Rising time	t_{wr1}	Fig. 1-5-3	0		5.0	ns
24	Falling time	t_{wf1}	Fig. 1-5-3	0		5.0	ns
25	Input high voltage	V_{IH1}	Fig. 1-5-3	0.8 V_{DD}		V_{DD}	V
26	Input low voltage	V_{IL1}	Fig. 1-5-3	V_{SS}		0.1 V_{DD}	V
External clock input 2 XI (XO is unconnected)							
27	Clock frequency	f_x		32.768		100	kHz
28	High level pulse width	t_{wh2}	*5 Fig. 1-5-4				µs
28	Low level pulse width	t_{wl2}	*5 Fig. 1-5-4				µs
30	Rising time	t_{wr2}	Fig. 1-5-4	0		20	ns
31	Falling time	t_{wf2}	Fig. 1-5-4	0		20	ns
32	Input high voltage	V_{IH2}	Fig. 1-5-4	0.8 V_{DD}		V_{DD}	V
33	Input low voltage	V_{IL2}	Fig. 1-5-4	V_{SS}		0.1 V_{DD}	V

*5 The clock duty rate should be 45% to 55%.

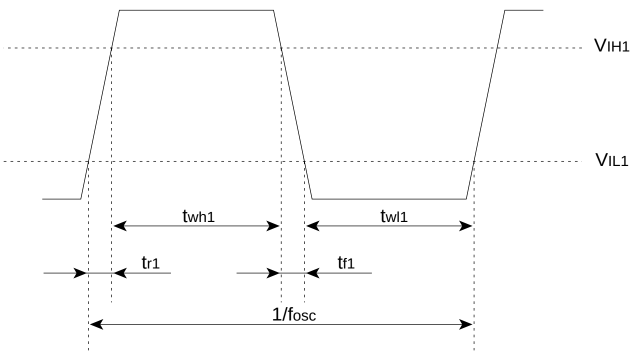


Figure 1-5-3 OSC1 Timing Chart

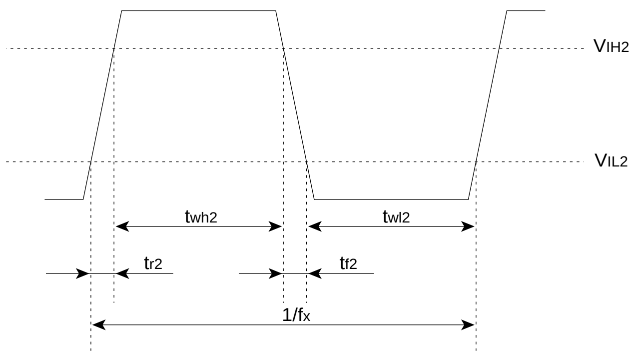


Figure 1-5-4 XI Timing Chart

1-5-3 DC Characteristics

Ta = -40 °C to +85 °C V_{SS} = 0 V
EPROM vers. is in ( ).

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
Power supply current (no load at output pin) *6							
1	Power supply current	I_{DD1}	fosc = 20.0 MHz V_{DD} = 5 V		25	60	mA
2		I_{DD2}	fosc = 8.00 MHz V_{DD} = 5 V		10	25	
3		I_{DD3}	fosc = 4.20 MHz V_{DD} = 5 V		6	16	
4		I_{DD4}	fx = 32.768 kHz V_{DD} = 5 V		100	250	µA
5		I_{DD5}	fx = 32.768 kHz V_{DD} = 3 V		30	100	
6	Supply current during HALT0 mode	I_{DD6}	fosc = 20.0 MHz V_{DD} = 5 V		3.0	7.5	mA
7		I_{DD7}	fosc = 8.00 MHz V_{DD} = 5 V		1.2	3.0	
8		I_{DD8}	fosc = 4.20 MHz V_{DD} = 5 V		1.0	2.5	
9	Supply current during HALT1 mode	I_{DD9}	fx = 32.768 kHz V_{DD} = 3 V Ta = 25 °C		4	8	µA
10		I_{DD10}	fx = 32.768 kHz V_{DD} = 3 V Ta = 85 °C			24	
11	Supply current during STOP mode	I_{DD11}	V_{DD} = 5 V Ta = 25 °C			1	
12		I_{DD12}	V_{DD} = 5 V Ta = 85 °C			20	

*6 Measured under conditions of no load. (Pull-up and pull-down are unconnected.)

- The supply current during operation, I_{DD1}, I_{DD2} and I_{DD3} are measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 20-MHz (8.00 MHz, 4.20 MHz) square wave of V_{DD} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD4} and I_{DD5} are measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 32.768-kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT0 mode, I_{DD6}, I_{DD7} and I_{DD8} are measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <HALT0 mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 20-MHz (8.00 MHz, 4.20 MHz) square wave of V_{DD} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during HALT1 mode, I_{DD9} and I_{DD10} are measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <HALT1 mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 32.768-kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD11} and I_{DD12} are measured under the following conditions : After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and the OSC1 and XI pins are unconnected.

Ta = -40 °C to +85 °C V_{DD} = 2.0 V (2.3 V) to 5.5 V V_{SS} = 0 V
EPROM vers. is in ( ).

No.	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
Input pin 1 MMOD							
13	Input high voltage 1	V_{IH1}		0.8 V_{DD}		V_{DD}	V
14	Input high voltage 2	V_{IH2}	V_{DD} = 2.3 V to 5.5 V	0.7 V_{DD}		V_{DD}	
15	Input low voltage 1	V_{IL1}		0		0.2 V_{DD}	
16	Input low voltage 2	V_{IL2}	V_{DD} = 2.3 V to 5.5 V	0		0.3 V_{DD}	
17	Input leakage current	I_{LK1}	V_I = 0 V to V_{DD}			± 2	μA
Input pin 2 P20 to P24 (Schmitt trigger input)							
18	Input high voltage	V_{IH3}		0.8 V_{DD}		V_{DD}	V
19	Input low voltage	V_{IL3}		0		0.2 V_{DD}	
20	Input leakage current	I_{LK3}	V_I = 0 V to V_{DD}			± 2	μA
21	Input high current	I_{IH3}	V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor ON	-30	-100	-300	
Input pin 3 PA0 to PA7 (Schmitt trigger input)							
22	Input high voltage	V_{IH4}		0.8 V_{DD}		V_{DD}	V
23	Input low voltage	V_{IL4}		0		0.2 V_{DD}	
24	Input leakage current	I_{K4}	V_I = 0 V to V_{DD}			± 2	μA
25	Input current 1	I_{IH4}	V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor ON	-30	-100	-300	
26	Input current 2		V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor ON	30	100	300	
I/O pin 1 P27 (NRST) (Schmitt trigger input)							
27	Input high voltage	V_{IH5}		0.9 V_{DD}		V_{DD}	V
28	Input low voltage	V_{IL5}		0		0.15 V_{DD}	
29	Input leakage current	I_{LK5}	V_{DD}			± 10	μA
30	Input current	I_{IH5}	V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor built-in	-30	-100	-300	
I/O pin 2 P00 to P06, P10 to P14, P30 to P32 (Schmitt trigger input)							
31	Input high voltage	V_{IH6}		0.8 V_{DD}		V_{DD}	V
32	Input low voltage	V_{IL6}		0		0.2 V_{DD}	
33	Input leakage current	I_{LK6}	V_I = 0 V to V_{DD}			±2	μA
34	Input current	I_{IH6}	V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor ON	-30	-100	-300	
35	Output high voltage	V_{OH6}	V_{DD} = 5.0 V I_{OH} = -0.5 mA	4.5			V
36	Output low voltage	V_{OL6}	V_{DD} = 5.0 V I_{OL} = 1.5 mA			0.5	

Ta = -40 °C to +85 °C V_{DD} = 2.0 V (2.3 V) to 5.5 V V_{SS} = 0 V
EPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 3 P50 to P54							
37	Input high voltage 1	V_{IH7}		0.8 V_{DD}		V_{DD}	V
38	Input high voltage 2	V_{IH8}	V_{DD} = 2.3 V to 5.5V	0.7 V_{DD}		V_{DD}	
39	Input low voltage 1	V_{IL7}		0		0.2 V_{DD}	
40	Input low voltage 2	V_{IL8}	V_{DD} = 2.3 V to 5.5V	0		0.3 V_{DD}	
41	Input leakage current	I_{LK7}	V_I = 0 V to V_{DD}			± 2	µA
42	Input high current	I_{IH7}	V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor ON	-30	-100	-300	
43	Output high current	V_{OH7}	V_{DD} = 5.0 V I_{OH} = -0.5mA	4.5			V
44	Output low current	V_{OL7}	V_{DD} = 5.0 V I_{OL} = 15 mA			1.0	
I/O pin 4 P60 to P67, P80 to P87							
45	Input high voltage 1	V_{IH9}		0.8 V_{DD}		V_{DD}	V
46	Input high voltage 2	V_{IH10}	V_{DD} = 2.3 V to 5.5 V	0.7 V_{DD}		V_{DD}	
47	Input low voltage 1	V_{IL9}		0		0.2 V_{DD}	V
48	Input low voltage 2	V_{IL10}	VDD = 2.3 V to 5.5 V	0		0.3 V_{DD}	
49	Input leakage current	I_{LK9}	V_I = 0 V to V_{DD}			± 2	µA
50	Input current	I_{IH9}	V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor ON	-30	-100	-300	
51	Output high voltage	V_{OH9}	V_{DD} = 5.0 V I_{OH} = -0.5 mA	4.5			V
52	Output low voltage	V_{OL9}	V_{DD} = 5.0 V I_{OL} = 1.5 mA			0.5	
I/O pin 5 P70 to P77							
53	Input high voltage 1	V_{IH11}		0.8 V_{DD}		V_{DD}	V
54	Input high voltage 2	V_{IH12}	V_{DD} = 2.3 V to 5.5 V	0.7 V_{DD}		V_{DD}	
55	Input low voltage 1	V_{IL11}		0		0.2 V_{DD}	
56	Input low voltage 2	V_{IL12}	V_{DD} = 2.3 V to 5.5 V	0		0.3 V_{DD}	
57	Input leakage current	I_{LK11}	V_I = 0 V to V_{DD}			± 2	µA
58	Input current 1	I_{IH11}	V_{DD} = 5.0 V V_I = 1.5 V Pull-up resistor ON	-30	-100	-300	
59	Input current 2	I_{IL11}	V_{DD} = 5.0 V V_I = 3.5 V Pull-up resistor ON	30	100	300	
60	Output high voltage	V_{OH11}	V_{DD} = 5.0 V I_{OH} = -0.5 mA	4.5			V
61	Output low voltage	V_{OL11}	V_{DD} = 5.0 V I_{OL} = 1.5 mA			0.5	

Ta = -40 °C to +85 °C V_{DD} = 2.0 V (2.3 V) to 5.5 V V_{SS} = 0 V
EPROM vers. is in ( ).

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
Input pin 4 P21 (when used as SENS) *V_{DD} = 5.0 V for P21 (SENS)							
62	Input high voltage 1	V_{DHH}	Fig. 1-5-5	4.5		V_{DD}	V
63	Input high voltage 2	V_{DHL}		1.5		V_{DD}	
64	Input low voltage 1	V_{DLH}		V_{SS}		3.5	
65	Input low voltage 2	V_{DLL}		V_{SS}		0.5	
66	Input leakage current	I_{LKS}	V_{IN} =0 V to V_{DD}			± 2	µA
67	Input high current	I_{C1}	V_{IN} > V_{DD}, V_{IN} < 0 V			± 400	
Display output pin 1 COM0 to COM3							
68	Output impedance	Z_{OCOM1}	V_{DD} = 5 V ± 0.5 V		3	6	kΩ
69		Z_{OCOM2}	V_{DD} = 3 V ± 0.3 V		8	15	
Display output pin 2 SEG0 to SEG51 *7							
70	Output impedance	Z_{OSEG1}	V_{DD} = 5 V ± 0.5 V		15	30	kΩ
71		Z_{OSEG2}	V_{DD} = 5 V ± 0.3 V		30	60	

*7 SEG26 to SEG51 also function as P53, P54, P60 to P67, P70 to P77, P80 to P87.

1-5-4 AC Characteristics

Ta = -40°C to +85 °C V_{DD} = 2.0 V (2.3 V) to 5.5 V V_{SS} = 0 V
EPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
SENS pin							
1	Rising time	t_r	Fig.1-5-5	30			µs
2	Falling time	t_f		30			

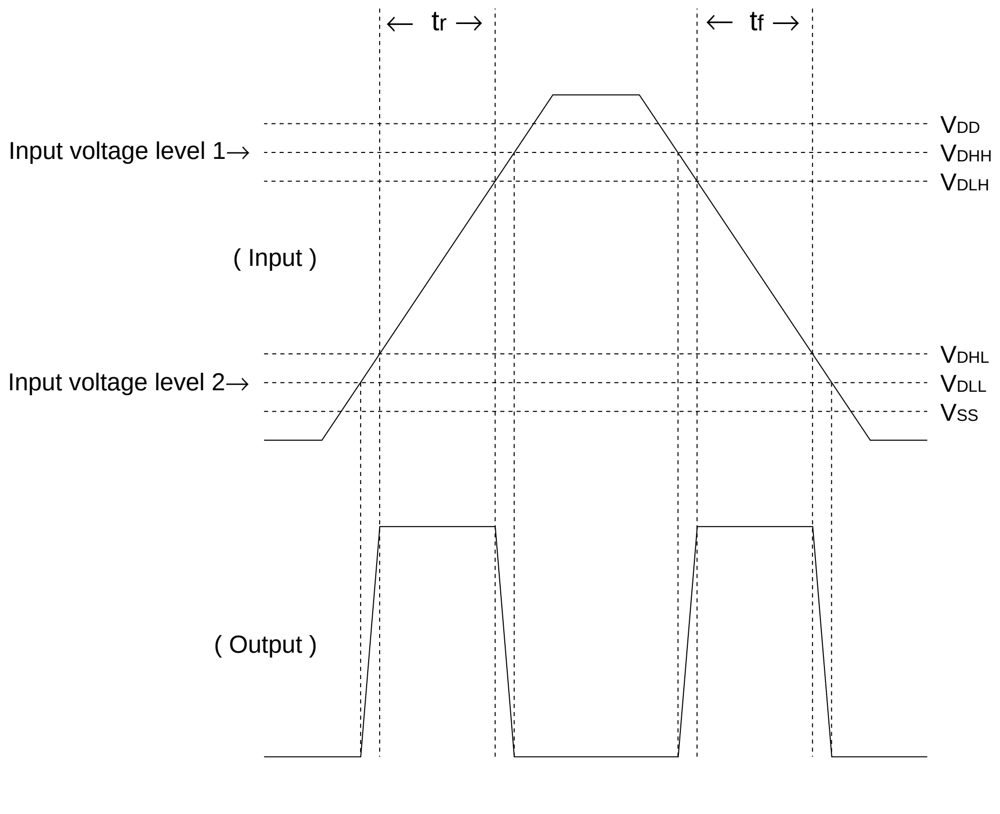


Figure 1-5-5 AC Zero-cross Detector

1-5-5 A/D Converter Characteristics

*8

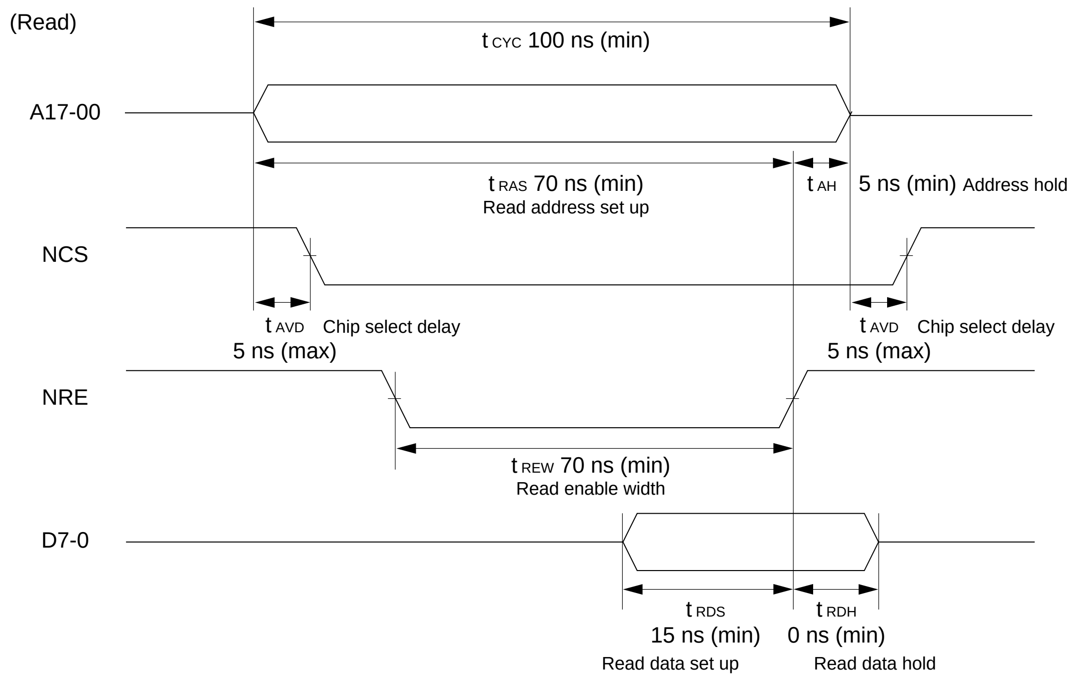
Ta = 25°C V_{DD} = 5.0 V V_{SS} = 0 V
EPROM vers. is in ( ).

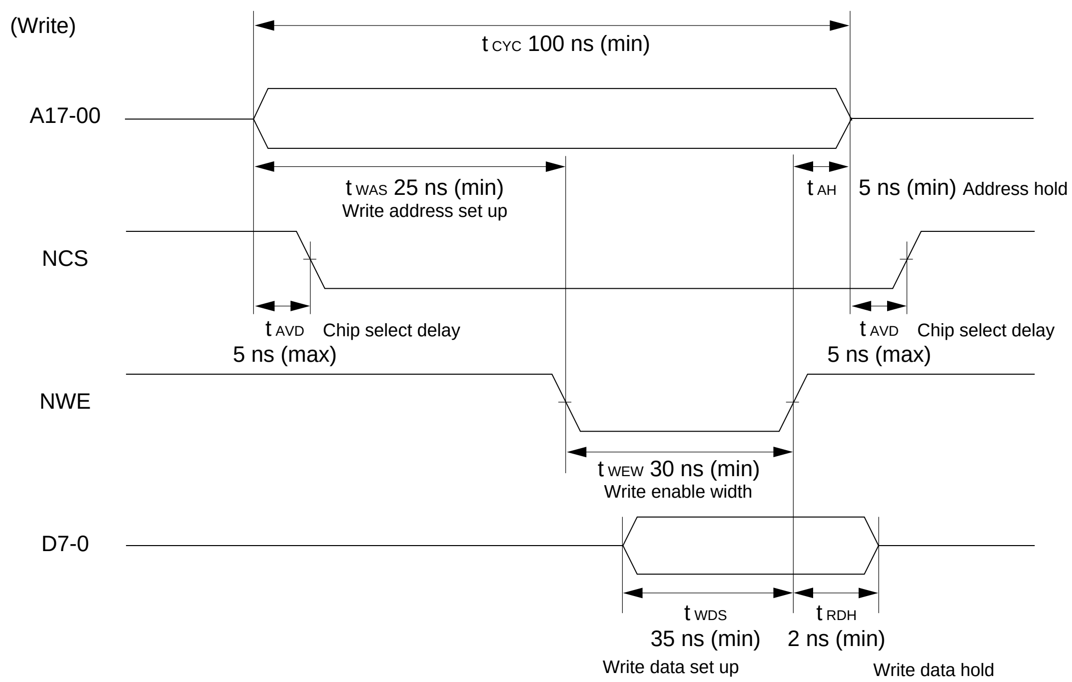
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	Non-linearity error 1		V_{DD} = 5.0 V V_{SS} = 0 V V_{REF+} = 5.0 V V_{REF-} = 0 V T_{AD} = 1.00 µs			± 3	LSB
3	Differential non-linearity error 1					± 3	
4	Non-linearity error 2		V_{DD} = 5.0 V V_{SS} = 0 V V_{REF+} = 5.0 V V_{REF-} = 0 V f_{OSC} = 32.768 kHz			± 5	
5	Differential non-linearity error 2					± 5	
6	Zero transition voltage		V_{DD} = 5.0 V V_{SS} = 0 V V_{REF+} = 5.0 V V_{REF-} = 0 V T_{AD} = 1.00 µs		30	100	mV
7	Full-scale transition voltage			4900	4970		
8	A/D conversion time		fosc = 8 MHz T_{AD} = 1.00 µs	12		28	µs
9			fosc = 4 MHz T_{AD} = 1.00 µs	12		28	
10			fx = 32.768 kHz T_{AD} = 15.2 µs	183.12		427.28	
11	Sampling time		f_{OSC} = 8 MHz T_{AD} = 1.00 µs	2.0		18.0	
12			fosc = 4 MHz T_{AD} = 1.00 µs	2.0		18.0	
13			fx = 32.768 kHz T_{AD} = 15.2 µs	30.52		274.68	
14	Reference voltage	V_{REF+}	*9	2.0		V_{DD}	V
15		V_{REF-}	*9	V_{SS}		3.0	
16	Analog input voltage			V_{REF-}		V_{REF+}	
17	Analog input leakage current		V_{ADIN} = 0 V to 5.0 V unselected channel			± 2	µA
18	Reference voltage pin input leakage current		Ladder resistor OFF $V_{REF-} \leq V_{REF+} \leq V_{DD}$			± 10	
19	Ladder resistance	R_{ladd}		20	50	80	kΩ

*8 T_{AD} means A/D conversion clock cycle.
The value of 2, 3, 6 and 7 are guaranteed on the condition that V_{DD} = V_{REF+} = 5 V, V_{SS} = V_{REF-} = 0 V.

*9 There should be more than 2 V between V_{REF+} and V_{REF-}.

1-5-6 Bus Timing (0 wait states) during Memory Expansion





> **!** To prevent the through current, add the pull-up / pull-down resistor or the level holding circuit to the expansion bus line (address + data) to fix the level of the expansion bus line. (Especially for stand-by mode.)

1-6 Option

1-6-1 ROM Option

MN101C38 series has ROM option address to specify the operating mode after reset and the watchdog timer frequency.

■ROM Option Bits

7	6	5	4	3	2	1	0
-	-	WDMD	-	-	WDSEL2	WDSEL1	NSSTRT

NSSTRT	Operating mode after reset
0	SLOW mode
1	NORMAL mode

WDSEL2	WDSEL1	Watchdog timer frequency
0	0	$fs/2^{16}$
	1	$fs/2^{18}$
1	X	$fs/2^{20}$

WDMD	Set always to "1".

Figure 1-6-1 ROM Option Bits

ROM option address differs depending on the model.

Table 1-6-1 ROM Option Address

Model	ROM option address
MN101C38A	x'0FFFF'
MN101C38C	x'0FFFF'
MN101CP38C	x'0FFFF'

Even if SLOW mode is selected after reset, connect oscillator pins to the high speed oscillation input.

The WDMD (bp5) should be always set to "1". If it is set to "0", that operation cannot be stopped after the watchdog timer is started.

1-6-2 Option Check List

Date:

SE No.

Model Name	MN101C

Customer		Countersign	

1. Operating mode after reset

NORMAL mode	SLOW mode

2. Watchdog timer period

fs/2^{16}	
fs/2^{18}	
fs/2^{20}	

3. Supply voltage operating range

CPU Operation	Used	Unused	Supply Voltage during Operation
At High Speed OSC1 Operation			V to V
At Low Speed XI Operation			V to V
At HALT0			V to V
At HALT1			V to V
At STOP			V to V

4. Type and frequency of oscillation input

Type	System Clock OSC1 Input	Timer Clock XI Input
External Clock		
Crystal		
Ceramic		
Frequency	MHz	kHz
Unused		

5. System operation clock

OSC1 only	
OSC1 and XI	

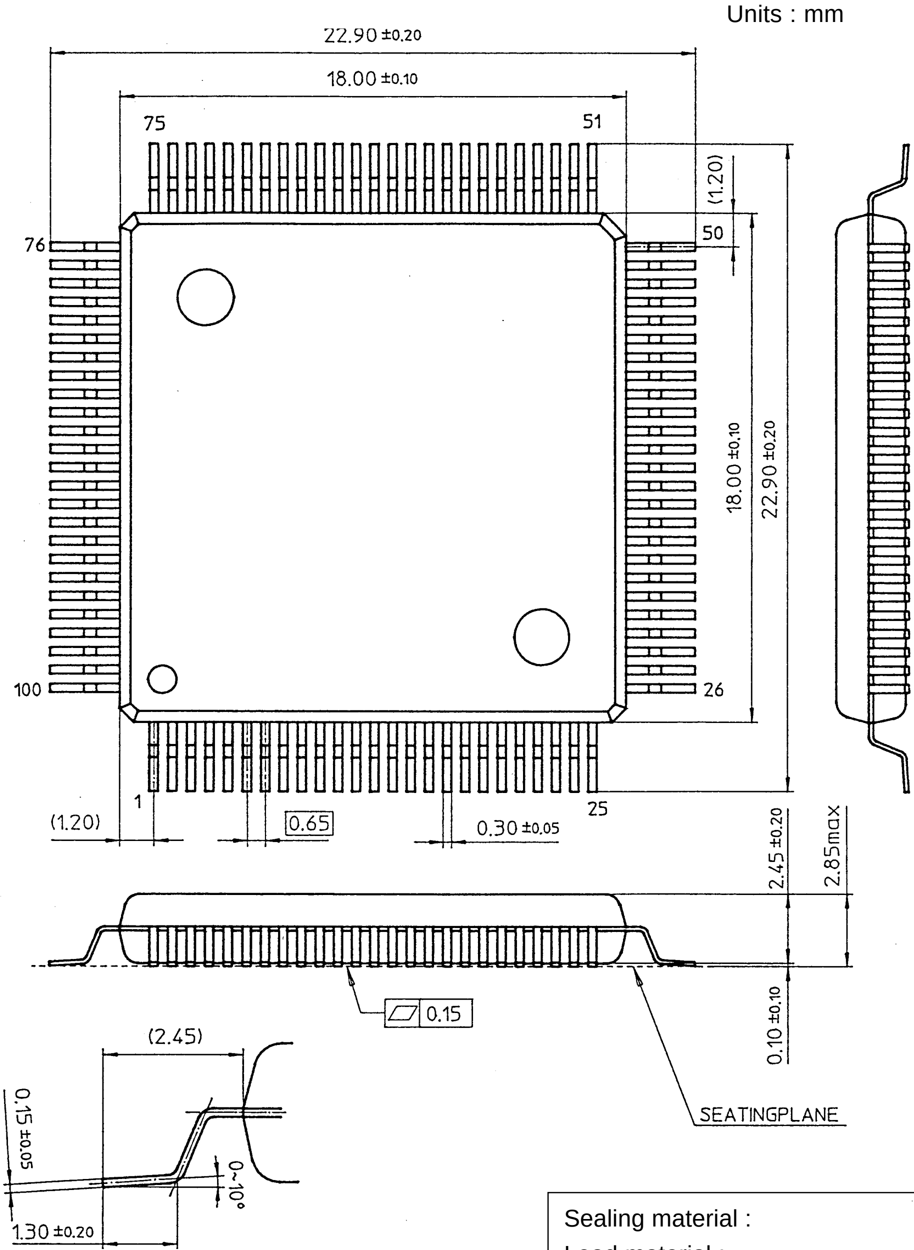
This check list is subjected to change. Please request the most recent check list from the sales office when doing ROM release.

Option of this product is used a part of the built-in ROM.
Please set data on the address of the option when doing ROM release.

1-7 Package Dimension

Package Code : *QFP100-P-1818B

Units : mm



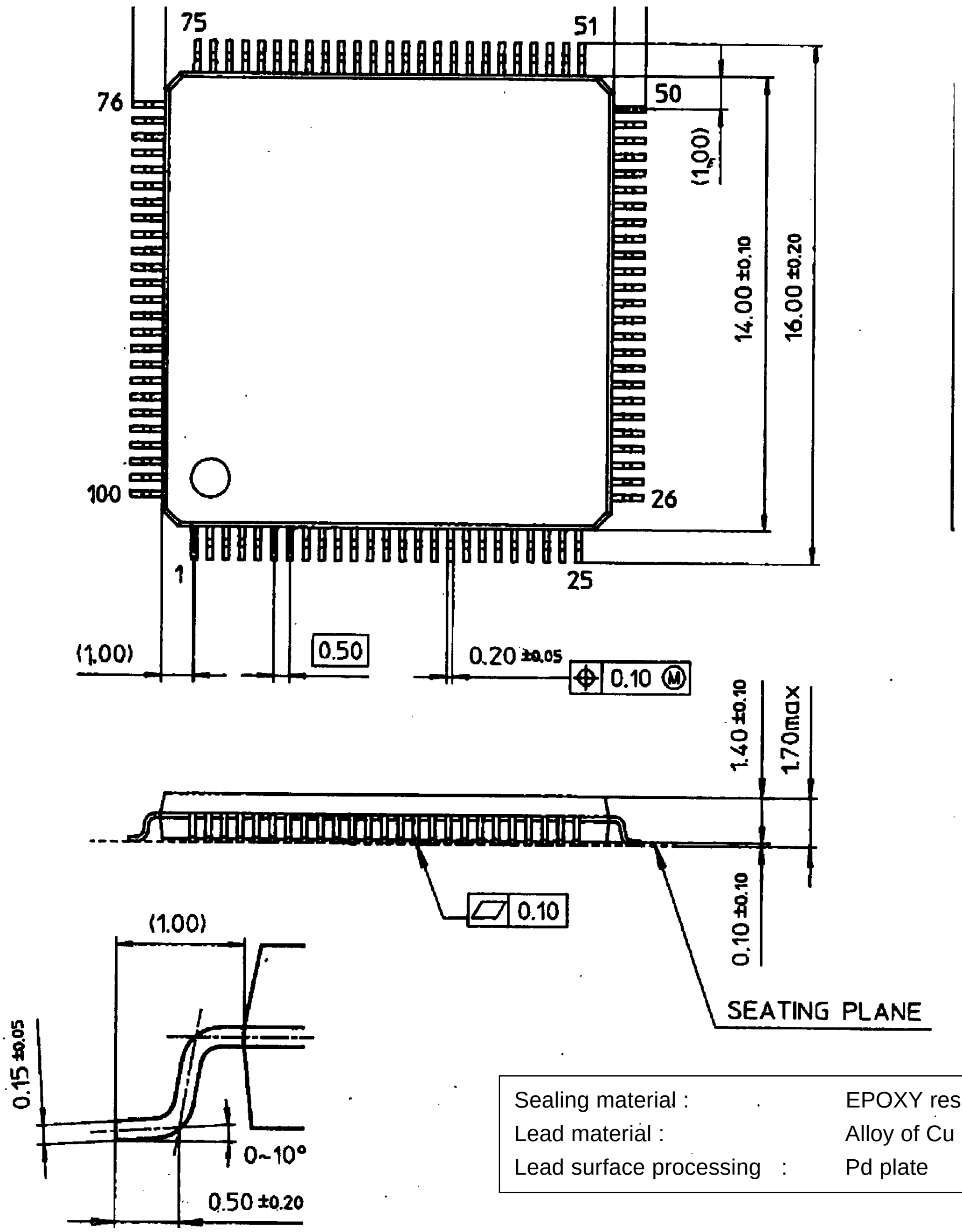
Sealing material :	EPOXY resin
Lead material :	Alloy of Cu
Lead surface processing :	Pd plate

Figure 1-7-1 100-Pin QFP

> ! The package dimension is subjected to change. Before using this product, please obtain product specifications from the sales office.

Package Code : LQFP100-P-1414

Units : mm



Sealing material :		EPOXY resin
Lead material :		Alloy of Cu
Lead surface processing	:	Pd plate

Figure 1-7-2 100-Pin LQFP

The package dimension is subjected to change. Before using this product, please obtain product specifications from the sales office.

1-8 Precautions

1-8-1 General Usage

■Connection of V_{DD} pin, and V_{SS} pin

All V_{DD} pins should be connected directly to the power supply and all V_{SS} pins should be connected to ground in the external. Please consider the LSI chip orientation before mounting it on to the printed circuit board. Incorrect connection may lead a fusion and break a micro controller.

■Cautions for Operation

(1) If you install the product close to high-field emissions (under the cathode ray tube, etc), shield the package surface to ensure normal performance.

(2) Each model has different operating condition,
- Operation temperature should be well considered. For example, if temperature is over the operating condition, its operation may be executed wrongly.
- Operation voltage should be also well considered. If the operation voltage is over the operation range, it can be shortened the length of its life. If the operation voltage is below the operating range, it operation may be wrong.

1-8-2 Unused Pins

■Unused Pins (for output and LCD output)
Set unused pins (for output and LCD output) open.

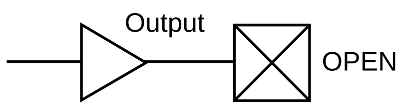


Figure 1-8-1 Unused Pins (for output and LCD output)

■Unused Pins (only for input)
Insert 10 kΩ to 100 kΩ resistor to unused pins (only for input) for pull-up or pull-down. If the input is unstable, Pch transistor and Nch transistor of input inverter are on, and through current goes to the input circuit. That increases current consumption and causes power supply noise.

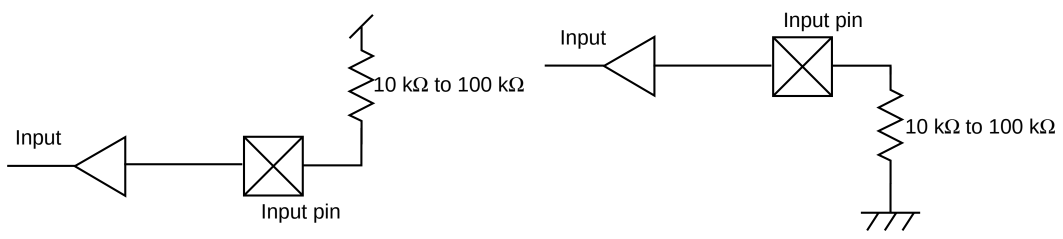


Figure 1-8-2 Unused Pins (only for input)

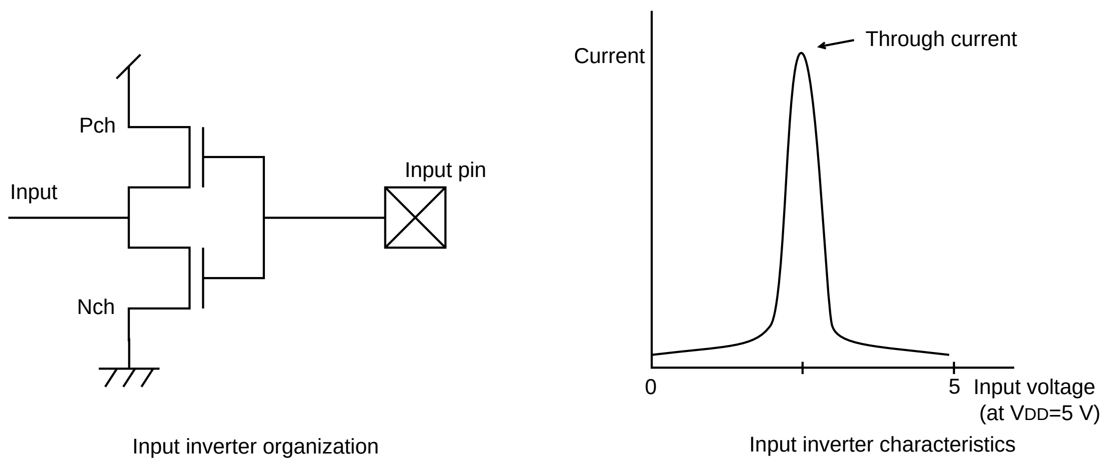


Figure 1-8-3 Input Inverter Organization and Characteristics

■Unused pins (for I/O)

Unused I/O pins should be set according to pins' condition at reset. If the output is high impedance (Pch / Nch transistor : output off) at reset, to stabilize input, set 10 kΩ to 100 kΩ resistor to be pull-up or pull-down. If the output is on at reset, set them open.

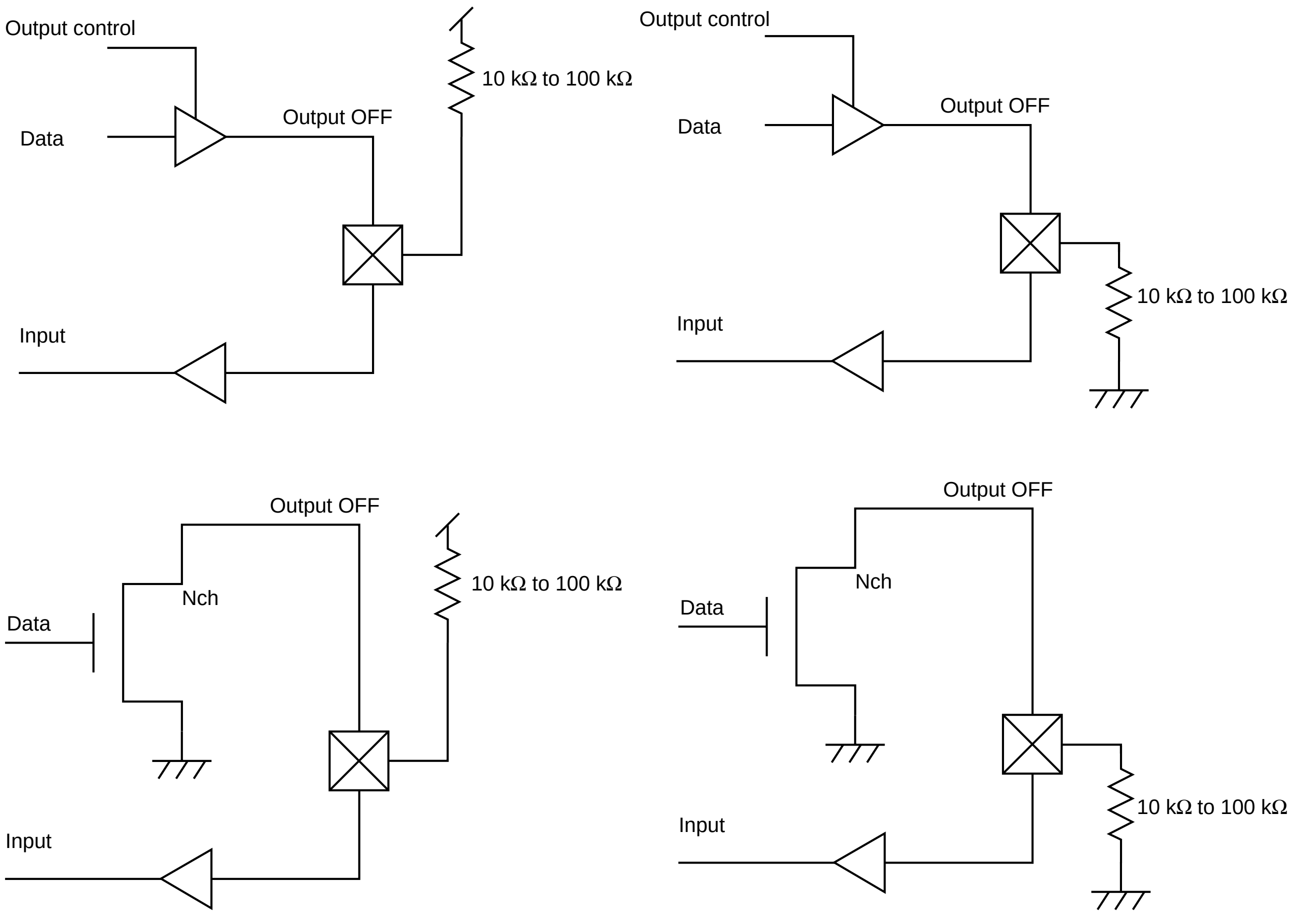


Figure 1-8-4 Unused I/O pins (high impedance output at reset)

1-8-3 Power Supply

■The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If the input pin voltage is applied before power supply is on, a latch up occurs and causes the destruction of micro controller by a large current flow.

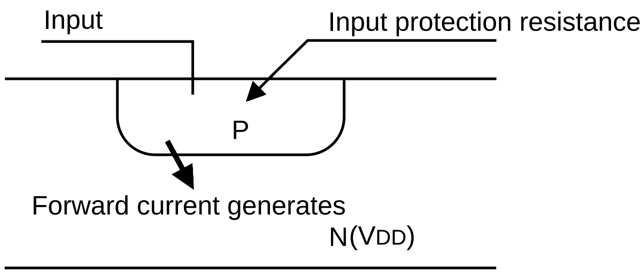
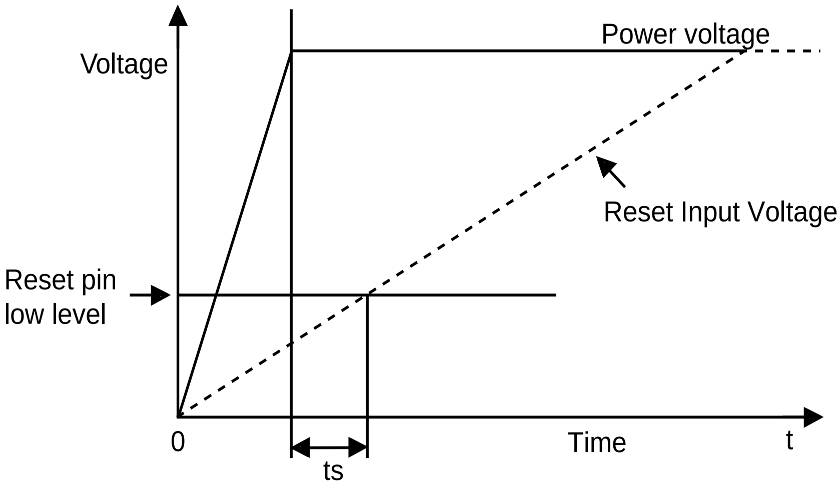


Figure 1-8-5 Power Supply and Input Pin Voltage

■The Relation between Power Supply and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time, ts, before rising, in order to be recognized as a reset signal.



[☞ Chapter 2. 2-5-1 Reset Operation]

Figure 1-8-6 Power Supply and Reset Input Voltage

1-8-4 Power Supply Circuit

■Cautions for Setting Circuits with V_{DD}

The CMOS logic microcontroller is high speed and high density. So, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver. Figure 1-8-6 shows an example for emitter follower type power supply circuit.

■An Example for Emitter Follower Type Power Supply Circuit

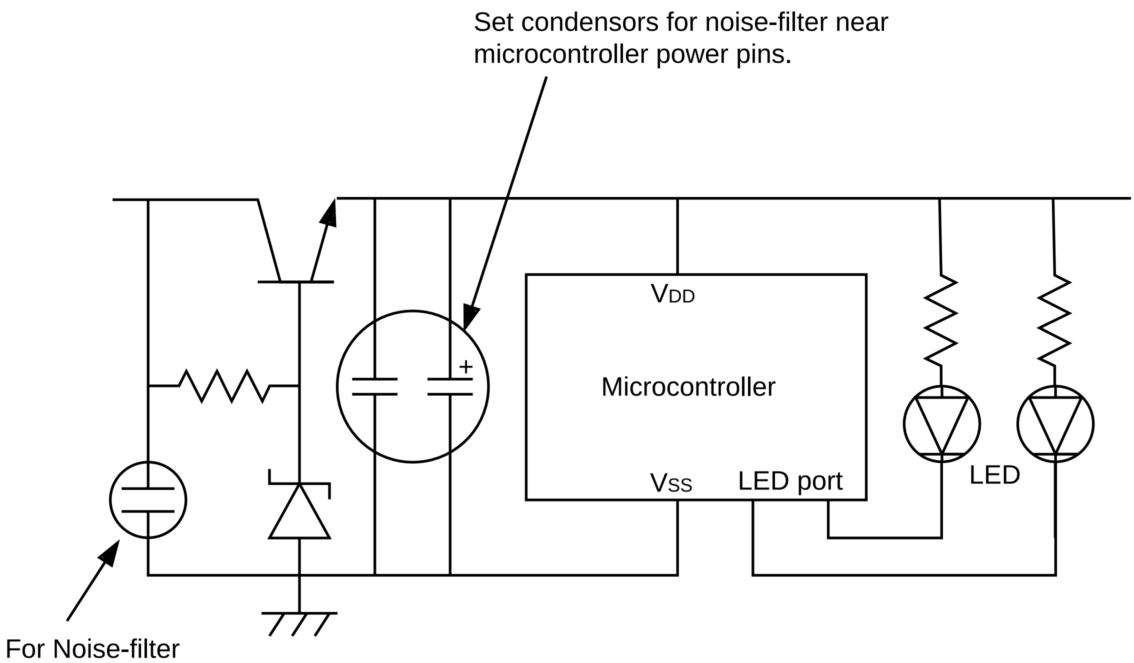


Figure 1-8-6 An Example for Emitter Follower Type Power Supply Circuit

1-8-5 Usage of Resonator

Ceramic resonator or crystal resonator can be used for oscillator clock of this LSI.

■Recommended resonator

Basic configuration with ceramic resonator is shown by the fallowing figure, and recommended resonator and its circuit constant are by the following table.

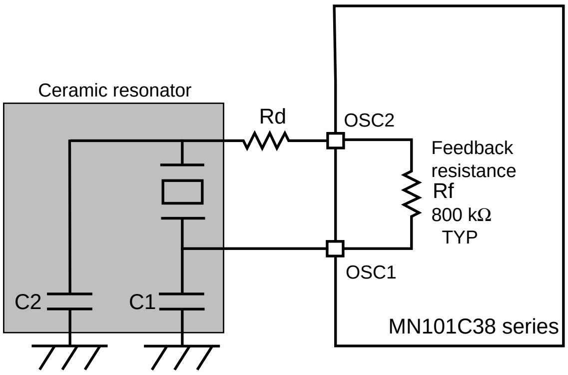


Figure 1-8-7 Basic configuration of Ceramic Resonator Connection

Table 1-8-1 Recommended Ceramic Resonator and Its Circuit Constant

Oscillation frequency	Ceramic resonator product number	Recommended circuit constant	
		Load capacity C1=C2	Dumping resistance Rd
20 MHz	EFOB2005B5 (Chip type)	33 pF ± 5 pF(built-in)	-
	EFOEX2005B4 (Discrete type)	33 pF ± 5 pF(built-in)	-
16 MHz	EFOB1605B5 (Chip type)	33 pF ± 5 pF(built-in)	-
	EFOEX1605E4 (Discrete type)	33 pF ± 5 pF(built-in)	-
8 MHz	EFOS8004B5 (Chip type)	33 pF ± 5 pF(built-in)	-
	EFOMC8004A4 (Discrete type)	33 pF ± 5 pF(built-in)	-
4 MHz	EFOS4004B5 (Chip type)	33 pF ± 5 pF(built-in)	-
	EFOMC4004A (Discrete type)	33 pF ± 5 pF(built-in)	-
2 MHz	EFOS2004B5 (Chip type)	33 pF ± 5 pF(built-in)	-
	EFOMC2004A4 (Discrete type)	33 pF ± 5 pF(built-in)	-

Inquiry : Matsushita Electronic Components Co., Ltd.
URL : http://www.maco.panasonic.co.jp/htm-binl/maco/index.html

Recommended value above is the consequence of the oscillation estimate by this LSI alone.
Insert dumping resistance if needed after the oscillation estimate on the application system substrate.

As for crystal resonator, an oscillation estimate is not held by this LSI. Apply the recommended value by an resonator maker to circuit constant.

> Circuit constant of crystal resonator or ceramic resonator which are connected to OSC1/OSC2 and XI/XO varies depending on stray capacitance of resonator or populated circuit. Consult an resonator maker to decide it without fail.

Chapter 2 CPU Basics

2-1 Overview

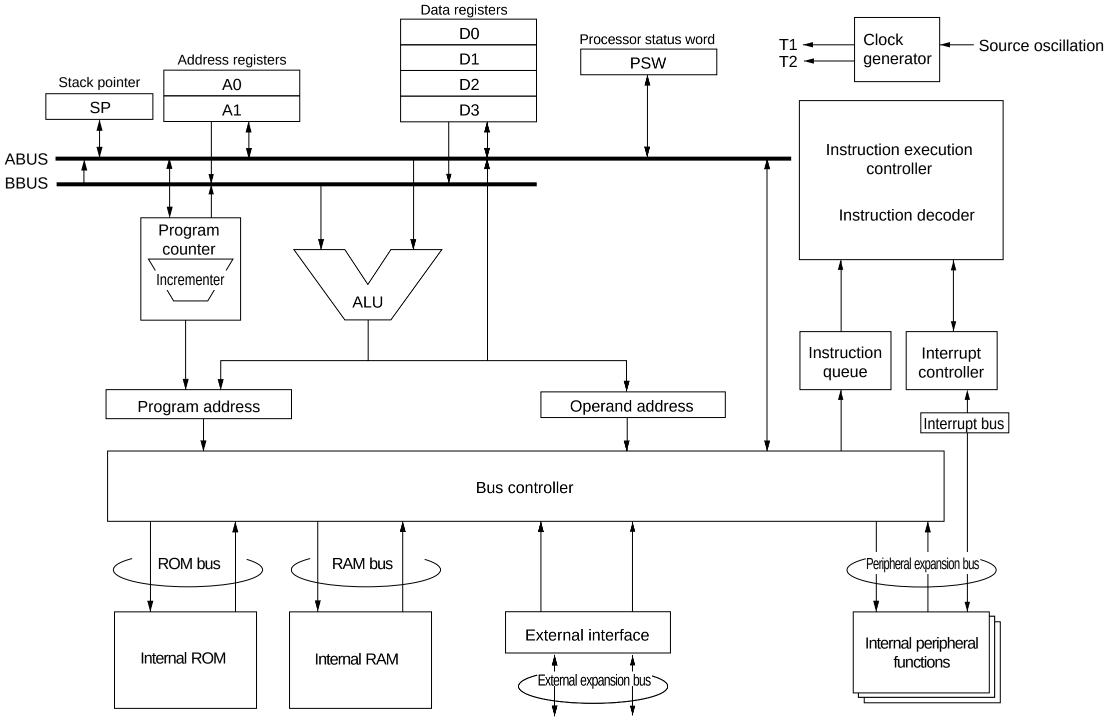
The MN101C CPU has a flexible optimized hardware configuration. It is a high speed CPU with a simple and efficient instruction set. Specific features are as follows:

1. Minimized code sizes with instruction lengths based on 4-bit increments
   The series keeps code sizes down by adopting a minimum instruction length of one byte and variable instruction lengths based on 4-bit increments.
2. Minimum instruction execution time is one system clock cycle.
3. Minimized register set that simplifies the architecture and supports C language
   The instruction set has been determined, depending on the size and capacity of hardware, after an analysis of embedded application programing code and creation code by C language compiler. Therefore, the set is simple instruction using the minimal register set required for C language compiler. ["MN101C LSI User's Manual" (Architecture Instructions)]

Table 2-1-1 Basic Specifications

Structure	Load / store architecture	
	Six registers	Data : 8-bit × 4 Address : 16-bit × 2
	Other	PC : 19-bit PSW : 8-bit SP : 16-bit
Instructions	Number of instructions	37
	Addressing modes	9
	Instruction length	Basic portion : 1 byte (min.) Extended portion : 0.5-byte × n (0 ≤ n ≤ 9)
Basic performance	Internal operating frequency (max.)	10 MHz
	Instruction execution	Min. 1 cycle
	Inter-register operation	Min. 2 cycles
	Load / store	Min. 2 cycles
	Conditional branch	2 to 3 cycles
Pipeline	3-stage (instruction fetch, decode, execution)	
Address space	256 KB (max. 64 KB for data) [2-2 Memory space]	
External bus	Address	18-bit (max.)
	Data	8-bit
	Minimum bus cycle	1 system clock cycle
Interrupt	Vector interrupt	3 interrupt levels
Low-power dissipation mode	STOP mode	
	HALT mode	

2-1-1 Block Diagram



Clock generator	Uses a clock oscillator circuit driven by an external crystal or ceramic resonator to supply clock signals to CPU blocks.
Program counter	Generates addresses for the instructions to be inserted into the instruction queue. Normally incremented by sequencer indication, but may be set to branch destination address or ALU operation result when branch instructions or interrupts occur.
Instruction queue	Stores up to 2 bytes of pre-fetched instructions.
Instruction decoder	Decodes the instruction queue, sequentially generates the control signals needed for instruction execution, and executes the instruction by controlling the blocks within the chip.
Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
ALU	Executes arithmetic operations, logic operations, shift operations, and calculates operand addresses for register relative indirect addressing mode.
Internal ROM, RAM	Assigned to the execution program, data and stack region.
Address register	Stores the addresses specifying memory for data transfer. Stores the base address for register relative indirect addressing mode.
Data register	Holds data for operations. Two 8-bit registers can be connected to form a 16-bit register.
Interrupt controller	Detects interrupt requests from peripheral functions and requests CPU shift to interrupt processing.
Bus controller	Controls connection of CPU internal bus and CPU external bus.
Internal peripheral functions	Includes peripheral functions (timer, serial interface, A/D converter, etc.). Peripheral functions vary with model.

Figure 2-1-1 Block Diagram and Function

2-1-2 CPU Control Registers

This LSI locates the peripheral circuit registers in memory space (x'03F00' to x'03FFF') with memory-mapped I/O. CPU control registers are also located in this memory space.

Table 2-1-2 CPU Control Registers

Registers	Address	R/W	Function	Pages
CPUM	x'03F00'	R/W *1	CPU mode control register	II - 24
MEMCTR	x'03F01'	R/W	Memory control register	II - 17
Reserved	x'03FE0'	-	For debugger	-
NMICR	x'03FE1'	R/W	Non-maskable interrupt control register	III - 16
xxxICR	x'03FE2' | x'03FFE'	R/W	Maskable interrupt control register	III - 17 to 29
Reserved	x'03FFF'	-	Reserved (For reading interrupt vector data on interrupt process)	-

*1 Part of the register is only readable

2-1-3 Instruction Execution Controller

The instruction execution controller consists of four blocks: memory, instruction queue, instruction registers, and instruction decoder.

Instructions are fetched in 1-byte units, and temporarily stored in the 2-byte instruction queue. Transfer is made in 1-byte or half-byte units from the instruction queue to the instruction register to be decoded by the instruction decoder.

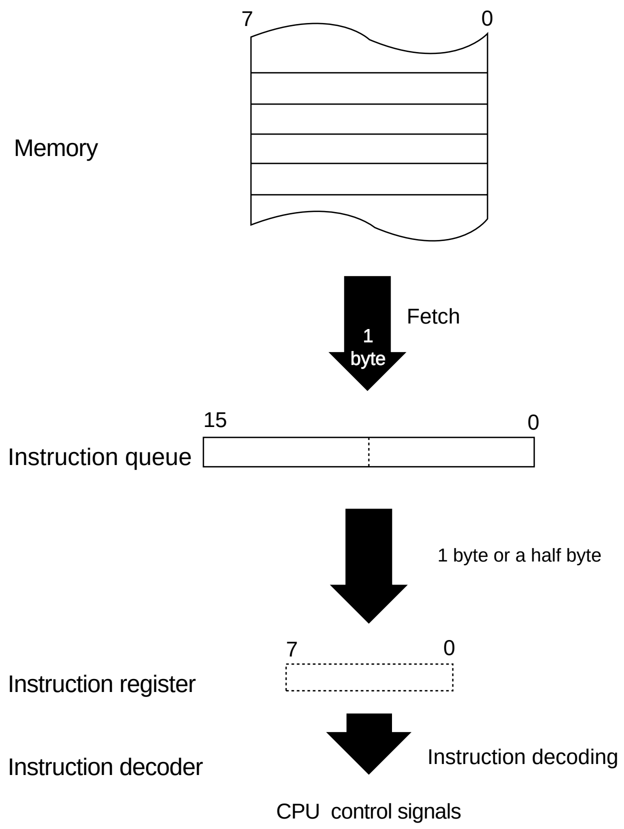


Figure 2-1-2 Instruction Execution Controller Configuration

2-1-4 Pipeline Process

Pipeline process means that reading and decoding are executed at the same time on different instructions, then instructions are executed without stopping. Pipeline process makes instruction execution continual and speedy. This process is executed with instruction queue and instruction decoder.

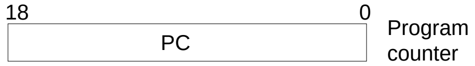
Instruction queue is buffer that fetches the second instruction in advance. That is controlled to fetch the next instruction when instruction queue is empty at each cycle on execution. At the last cycle of instruction execution, the first word (operation code) of executed instruction is stored to instruction register. At that time, the next operand or operation code is fetched to instruction queue, so that the next instruction can be executed immediately, even if register direct (da) or immediate (imm) is needed at the first cycle of the next instruction execution. But on some other instruction such as branch instruction, instruction queue becomes empty on the time that the next operation code to be executed is stored to instruction register at the last cycle. Therefore, only when instruction queue is empty, and direct address (da) or immediate data (imm) are needed, instruction queue keeps waiting for a cycle.

Instruction queue is controlled automatically by hardware so that there is no need to be controlled by software. But when instruction execution time is estimated, operation of instruction queue should be into consideration. Instruction decoder generates control signal at each cycle of instruction execution by micro program control. Instruction decoder uses pipeline process to decode instruction queue at one cycle before control signal is needed.

2-1-5 Registers for Address

Registers for address include program counter (PC), address registers (A0, A1), and stack pointer (SP).

■Program Counter (PC)
This register gives the address of the currently executing instruction. It is 19 bits wide to provide access to a 256 KB address space in half byte (4-bit increments). The LSB of the program counter is used to indicate half byte instruction. The program counter after reset is stored from the value of vector table at the address of 4000.



■Address Registers (A0, A1)

These registers are used as address pointers specifying data locations in memory. They support the operations involved in address calculations (i.e. addition, subtraction and comparison). Those pointers are 2 bytes data. Transfers between these registers and memory are always in 16-bit units. Either odd or even address can be transferred. At reset, the value of address register is undefined.

	15 0
Address Registers	A0
	A1

■Stack Pointer (SP)

This register gives the address of the byte at the top of the stack. It is decremented during push operations and incremented during pop operations. At reset, the value of SP is undefined.

	15 0
Stack Pointer	SP

2-1-6 Registers for Data

Registers for data include four data registers (D0, D1, D2, D3).

■Data Registers (D0, D1, D2, D3)

Data registers D0 to D3 are 8-bit general-purpose registers that support all arithmetic, logical and shift operations. All registers can be used for data transfers with memory.

The four data registers may be paired to form the 16-bit data registers DW0 (D0+D1) and DW1 (D2+D3). At reset, the value of Dn is undefined.

	15 8	7 0	
Data registers	D1	D0	DW0
	D3	D2	DW1

2-1-7   Processor Status Word

Processor status word (PSW) is an 8-bit register that stores flags for operation results, interrupt mask level, and maskable interrupt enable. PSW is automatically pushed onto the stack when an interrupt occurs and is automatically popped when return from the interrupt service routine.

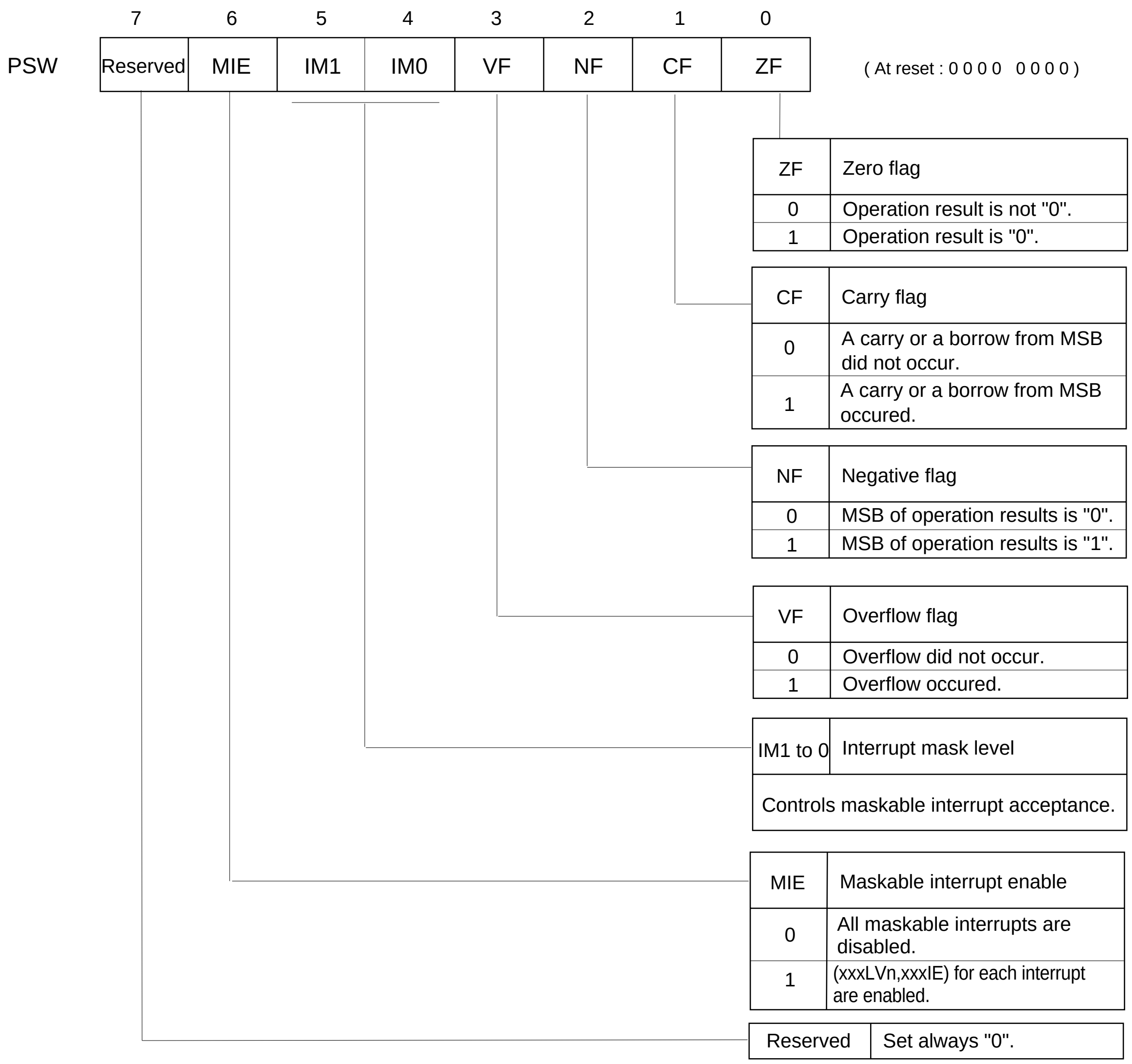


Figure 2-1-3   Processor Status Word (PSW)

■Zero Flag (ZF)
Zero flag (ZF) is set to "1", when all bits are '0' in the operation result. Otherwise, zero flag is cleared to "0".

■Carry Flag (CF)
Carry flag (CF) is set to "1", when a carry from or a borrow to the MSB occurs. Carry flag is cleared to "0", when no carry or borrow occurs.

■Negative Flag (NF)
Negative flag (NF) is set to "1" when MSB is '1' and reset to "0" when MSB is '0'. Negative flag is used to handle a signed value.

■Overflow Flag (VF)
Overflow flag (VF) is set to "1", when the arithmetic operation results overflow as a signed value. Otherwise, overflow flag is cleared to "0".
Overflow flag is used to handle a signed value.

■Interrupt Mask Level (IM1 and IM0)
Interrupt mask level (IM1 and IM0) controls the maskable interrupt acceptance in accordance with the interrupt factor interrupt priority for the interrupt control circuit in the CPU. The 2-bit control flag defines levels '0' to '3'. Level 0 is the highest mask level. The interrupt request will be accepted only when the level set in the interrupt level flag (xxxLVn) of the interrupt control register (xxxICR) is higher than the interrupt mask level. When the interrupt is accepted, the level is reset to IM1-IM0, and interrupts whose mask levels are the same or lower are rejected during the accepted interrupt processing.

Table 2-1-3　Interrupt Mask Level and Interrupt Acceptance

	Interrupt mask level		Priority	Acceptable interrupt levels
	IM1	IM0		
Mask level 0	0	0	High	Non-maskable interrupt (NMI) only
Mask level 1	0	1	.	NMI, Level 0
Mask level 2	1	0	.	NMI, Level 0 to 1
Mask level 3	1	1	Low	NMI, Level 0 to 2

■Maskable Interrupt Enable (MIE)
Maskable interrupt enable flag (MIE) enables/disables acceptance of maskable interrupts by the CPU's internal interrupt acceptance circuit. A '1' enables maskable interrupts; a '0' disables all maskable interrupts regardless of the interrupt mask level (IM1-IM0) setting in PSW.
This flag is not changed by interrupts.

2-1-8 Addressing Modes

The MN101C38 series supports the nine addressing modes.

Each instruction uses a combination of the following addressing modes.

1) Register direct
2) Immediate
3) Register indirect
4) Register relative indirect
5) Stack relative indirect
6) Absolute
7) RAM short
8) I/O short
9) Handy

These addressing modes are well-suited for C language compilers. All of the addressing modes can be used for data transfer instructions. In modes that allow half-byte addressing, the relative value can be specified in half-byte (4-bit) increments, so that instruction length can be shorter. Handy addressing reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combining handy addressing with absolute addressing reduces code size. For transfer data between memory, 7 addressing modes ; register indirect, register relative indirect, stack relative indirect, absolute, RAM short, I/O short, handy can be used. For operation instruction, register direct and immediate can be used. Refer to instruction's manual for the MN101C series.

This LSI is designed for 8-bit data access. It is possible to transfer data in 16-bit increments with odd or even addresses.

Table 2-1-4 Addressing Modes

Addressing mode		Effective address	Explanation
Register direct	Dn/DWn An/SP PSW	-	Directly specifies the register. Only internal registers can be specified.
Immediate	imm4/imm8 imm16	-	Directly specifies the operand or mask value appended to the instruction code.
Register indirect	(An)	15 … 0: An	Specifies the address using an address register.
Register relative indirect	(d8, An)	15 … 0: An+d8	Specifies the address using an address register with 8-bit displacement.
	(d16, An)	15 … 0: An+d16	Specifies the address using an address register with 16-bit displacement.
	(d4, PC) (branch instructions only)	17 … 0 H: PC+d4 * 1	Specifies the address using the program counter with 4-bit displacement and H bit.
	(d7, PC) (branch instructions only)	17 … 0 H: PC+d7 * 1	Specifies the address using the program counter with 7-bit displacement and H bit.
	(d11, PC) (branch instructions only)	17 … 0 H: PC+d11 * 1	Specifies the address using the program counter with 11-bit displacement and H bit.
	(d12, PC) (branch instructions only)	17 … 0 H: PC+d12 * 1	Specifies the address using the program counter with 12-bit displacement and H bit.
	(d16, PC) (branch instructions only)	17 … 0 H: PC+d16 * 1	Specifies the address using the program counter with 16-bit displacement and H bit.
Stack relative indirect	(d4, SP)	15 … 0: SP+d4	Specifies the address using the stack pointer with 4-bit displacement.
	(d8, SP)	15 … 0: SP+d8	Specifies the address using the stack pointer with 8-bit displacement.
	(d16, SP)	15 … 0: SP+d16	Specifies the address using the stack pointer with 16-bit displacement.
Absolute	(abs8)	7 … 0: abs8	Specifies the address using the operand value appended to the instruction code. Optimum operand length can be used to specify the address.
	(abs12)	11 … 0: abs12	
	(abs16)	15 … 0: abs16	
	(abs18) (branch instructions only)	17 … 0 H: abs18 * 1	
RAM short	(abs8)	7 … 0: abs8	Specifies an 8-bit offset from the address x'00000'.
I/O short	(io8)	15 … 0: IOTOP+io8	Specifies an 8-bit offset from the top address (x'03F00') of the special function register area.
Handy	(HA)	-	Reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combined use with absolute addressing reduces code size.

* 1 H: half-byte bit

2-2 Memory Space

2-2-1 Memory Mode

ROM is the read only area and RAM is the memory area which contains readable/writable data. In addition to these, peripheral resources such as memory-mapped special registers are allocated. The MN101C series supports three memory modes (single chip mode, memory expansion mode, processor mode) in its memory model. Setting of each mode is different.

In single chip mode, the system consists of only internal memory. In memory expansion mode, and processor mode, ROM, RAM and external device for operation can be connected.

Settings for each modes are as follows ;

Table 2-2-1 Memory Mode Setup

Memory mode	MMOD pin	EXMEM flag in (MEMCTR register)	EXADV3 to 1 flag in (EXADV register)
Single chip mode	L	0	-
Memory expansion mode	L	1	0/1

MMOD pin should be fixed to "L" level.
Do not change the setup of MMOD pin after reset.

2-2-2 Single-chip Mode

In single-chip mode, the system consists of only internal memory. This is the optimized memory mode and allows construction of systems with the highest performance.

The single-chip mode uses only internal ROM and internal RAM. The MN101C series devices offer up to 12 KB of RAM and up to 240 KB of ROM. MN101C38C devices offer 2048 bytes of RAM and 48 KB of ROM.

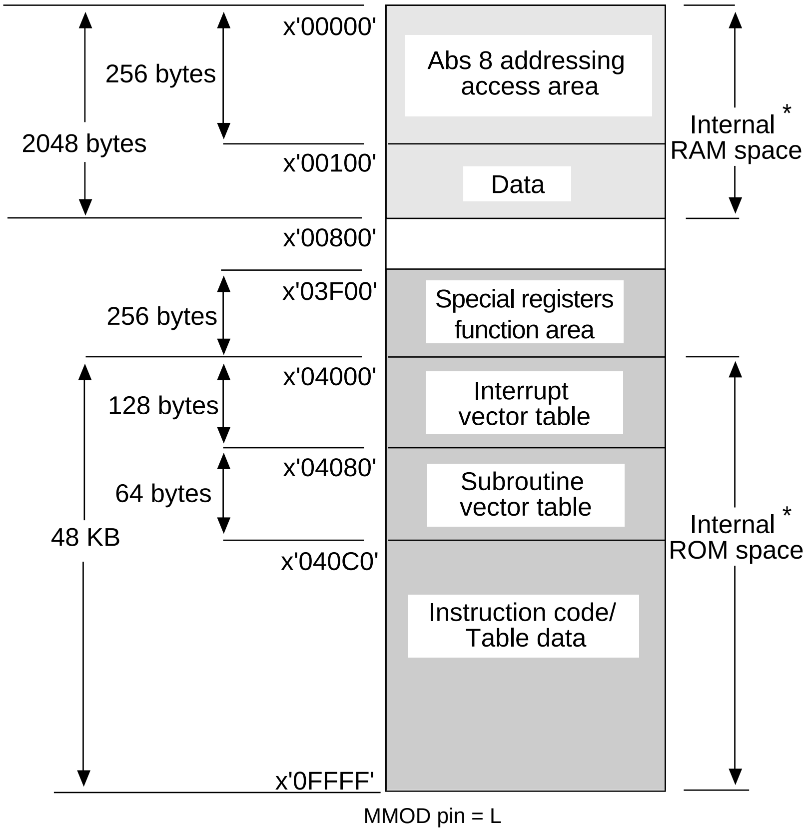


Figure 2-2-1 Single-chip Mode

* Differs depending on the model.

[☞ Table 2-2-2. Internal ROM / Internal RAM]

Table 2-2-2 Internal ROM / Internal RAM

Model	Internal RAM		Internal ROM	
	Address	bytes	Address	bytes
MN101C38A	X'00000'to X'005FF'	1536	X'04000' to X'0BFFF'	32 K
MN101C38C	X'00000' to X'007FF'	2048	X'04000' to X'0FFFF'	48 K

* x'0FFFF' can not be used for MN101C38A/38C because of ROM option.

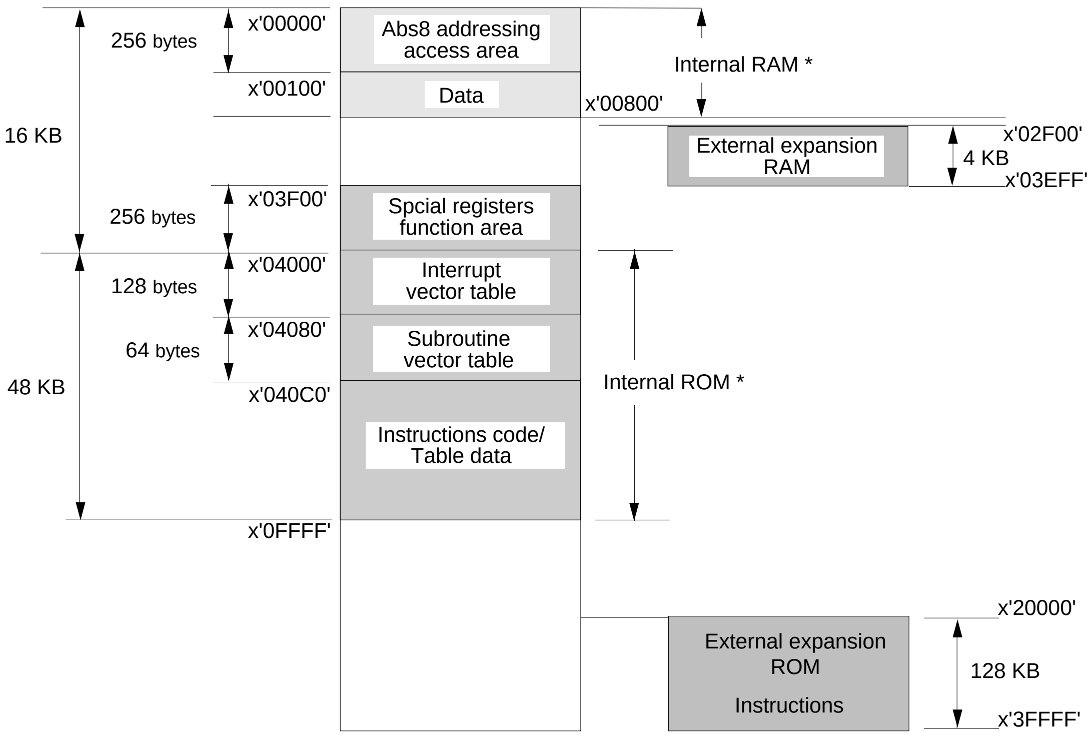
> The value of internal RAM is uncertain when power is applied to it.
> It needs to be initialized before it is used.

2-2-3 Memory Expansion Mode

The MN101C series can connect external ROM, RAM and external devices for operation in memory expansion mode. This is the mode to expand to external memory while using internal ROM and RAM.

The memory expansion mode is set by assigning EXMEM flag (bp4) of the memory control register (MEMCTR), on single chip mode. The pins A8 to A 17 of the address expansion control register (EXADV) control the address output to pins by setting the bit 7 to bit 5 of the EXADV.
Memory areas can be externally expanded as follows :

ROM: x'20000'-x'3FFFF' (128 KB)
RAM: x'02F00'-x'03EFF' (4 KB)



MMOD pin=L
EXMEM flag=1

Figure 2-2-2 Memory Expansion Mode

* Differs depending on the model.
[☞ Table 2-2-2. Internal ROM / Internal RAM]

The value of internal RAM is uncertain when power is applied to it. It needs to be initialized before it is used.

2-2-4 Special Function Registers

The MN101C series locates the special function registers (I/O spaces) at the addresses x'03F00' to x'03FFF' in memory space. The special function registers of this LSI are located as shown below.

Table 2-2-3 Register Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
03F0X	CPUM	MEMCTR	WDCTR	DLYCTR											EXADV		CPU mode, memory control
03F1X	P0OUT	P1OUT	P2OUT	P3OUT		P5OUT	P6OUT	P7OUT	P8OUT							SYSMD	I/O Ports: Port output
03F2X	P0IN	P1IN	P2IN	P3IN		P5IN	P6IN	P7IN	P8IN		PAIN						I/O Ports: Port input
03F3X	P0DIR	P1DIR		P3DIR		P5DIR	P6DIR	P7DIR	P8DIR	P10MD	PAIMD		P4IMD				I/O Ports: I/O mode control
03F4X	P0PLU	P1PLU	P2PLU	P3PLU		P5PLU	P6PLU	P7PLU	P8PLU		PAPLUD	FLOAT1	FLOAT2				I/O Ports: Resistor control
03F5X	SC0MD0	SC0MD1	SC0MD2	SC0MD3	SC0CTR	SC0TBR	SC0RXB	SC1MD0	SC1MD1	SC1TRB							Serial I/F control
03F6X			TM2BC	TM3BC	TM4BCL	TM4BCH	TM4ICL	TM4ICH	TM5BC								Timer control
03F7X			TM2OC	TM3OC	TM4OCL	TM4OCH			TM5OC								Timer control
03F8X			TM2MD	TM3MD	TM4MD				TM5MD	RMCTR	NFCTR						Timer control
03F9X	ANCTR0	ANCTR1	ANBUF0	ANBUF1													A/D control
03FAX																	Reserved
03FBX	LC00BUF	LC01BUF	LC02BUF	LC03BUF	LC04BUF	LC05BUF	LC06BUF	LC07BUF	LC08BUF	LC09BUF	LC0ABUF	LC0BBUF	LC0CBUF	LC0DBUF	LC0EBUF	LC0FBUF	LCD control
03FCX	LC10BUF	LC11BUF	LC12BUF	LC13BUF	LC14BUF	LC15BUF	LC16BUF	LC17BUF	LC18BUF	LC19BUF			LCCTR	LCMD			LCD control
03FDX																	LCD control
03FEX		NMICR	IRQ0ICR	IRQ1ICR			TM2ICR	TBICR	SC0ICR		ADICR	IRQ2ICR	IRQ3ICR	IRQ4ICR	TM3ICR	TM4ICR	Interrupt control
03FFX	TM5ICR	SC1ICR															Interrupt control

2-3 Bus Interface

2-3-1 Bus Controller

The MN101C series provides separate buses to the internal memory and internal peripheral circuits to reduce bus line loads. Therefore, this series realizes faster operation.

There are four such buses: ROM bus, RAM bus, peripheral expansion bus (I/O bus), and external expansion bus. They connect to the internal ROM, internal RAM, internal peripheral circuits, and external interfaces respectively. The bus control block controls the parallel operation of instruction read and data access, the access speed adjustment for low-speed external devices. A functional block diagram of the bus controller is given below.

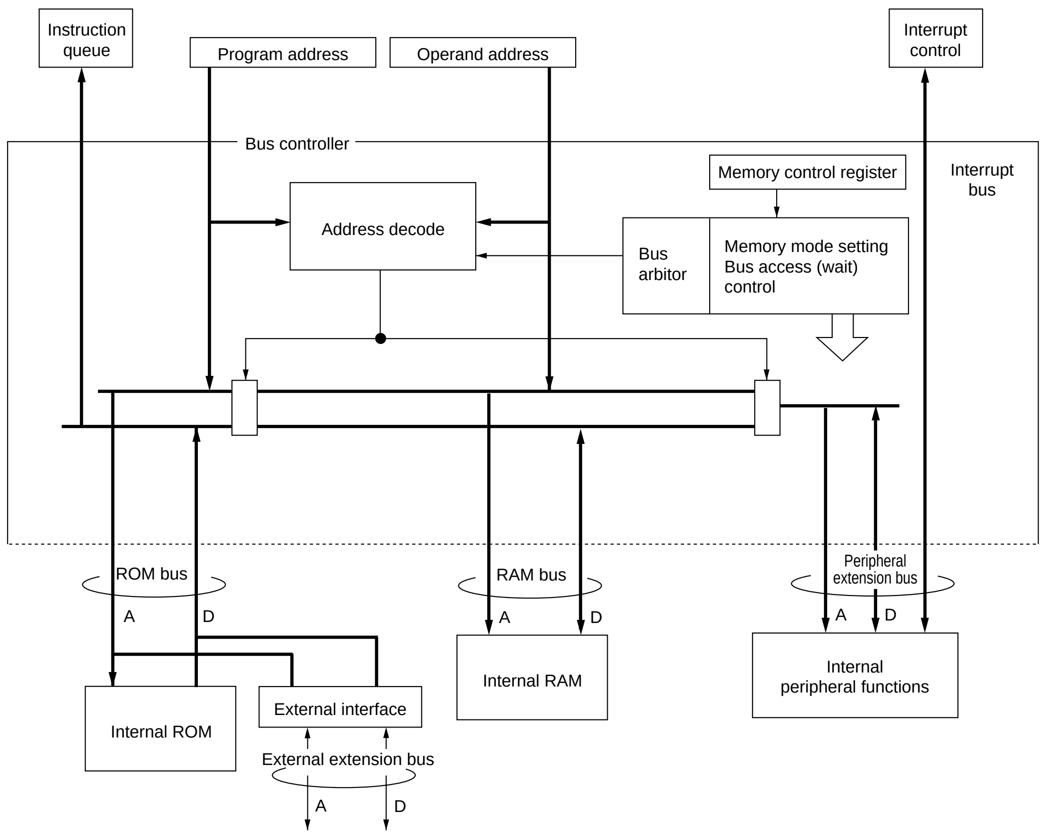


Figure 2-3-1 Functional Block Diagram of the Bus Controller

In memory expansion mode or processor mode, the external expansion bus can access external device. Memory control register (MEMCTR) can be used to select the access mode, fixed wait cycle mode or handshake mode. Wait cycle setting to peripheral expansion bus, connected to internal peripheral circuits is available.

2-3-2 Control Registers

Bus interface is controlled by 2 registers : the memory control register (MEMCTR) and the expansion address control register (EXADV).

■Memory Control Register (MEMCTR)

	7	6	5	4	3	2	1	0	
MEMCTR	IOW1	IOW0	IVBA	EXMEM	EXWH	IRWE	EXW1	EXW0	(At reset : 1 1 0 0 1 0 1 1)

EXW1 to 0	Fixed wait cycles	Bus cycle at 20 MHz oscillation
0 0	No wait cycles	100 ns
0 1	1 wait cycle	150 ns
1 0	2 wait cycles	200 ns
1 1	3 wait cycles	250 ns

IRWE	Software write enable flag for interrupt request
0	Software write disable Even if data is written to each interrupt control register (xxxICR), the state of the interrupt request flag (xxxIR) will not change.
1	Software write enable

EXWH	Fixed wait cycle mode or handshake mode
0	Handshake mode
1	Fixed wait cycle mode

EXMEM	Memory expansion mode
0	Do not expand external memory
1	Expand external memory

IVBA	Base address setting for interrupt vector table
0	Interrupt vector base = x'04000'
1	Interrupt vector base = x'00100'

IOW1 to 0	Wait cycles when accessing special register area	Bus cycle at 20 MHz oscillation
0 0	No wait cycles	100 ns
0 1	1 wait cycle	150 ns
1 0	2 wait cycles	200 ns
1 1	3 wait cycles	250 ns

Figure 2-3-2 Memory Control Register (MEMCTR: x'3F01' R/W)

The EXW1-EXW0 wait settings affect accesses to external devices in the memory expansion mode. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles.

The IOW1-IOW0 wait settings affect accesses to the special registers located at the addresses x'3F00'-x'3FFF'. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles. Wait setting of IOW is a function, which CPU supports for special use, for example, when special function register or I/O is expanded to external. For this LSI, wait cycle setting is not always necessary. Select "no-wait cycle" for high performance system construction.

■Expansion Address Control Register (EXADV)

	7	6	5	4	3	2	1	0
EXADV	EXADV3	EXADV2	EXADV1	-	-	-	-	-

(At reset : 0 0 0 - - - - -)

EXADV1	P73 - P70 "A11 - A8" address output during memory expansion mode.
0	General port
1	"A11 to A8" address output

EXADV2	P77 - P74 "A15 - A12" address output during memory expansion mode.
0	General port
1	"A15 to A12" address output

EXADV3	P54, P53 "A17, 16" address output during memory expansion mode.
0	General port
1	"A17, 16" address output

Figure 2-3-3 Expansion Address Control Register (EXADV : x'03F0E', R/W)

In memory expansion mode, unused address pins can be used as general ports.

2-3-3 Fixed Wait Cycle Mode

This mode accesses ROM, RAM, or other low-speed devices connected to the external expansion bus by inserting the number of wait cycles specified in the external fixed wait counter (EXW) field of the memory control register (MEMCTR).

Fixed wait cycle mode is used to automatically insert the number of wait cycles specified by the fixed wait counter (EXWn) in the MEMCTR. After reset, MEMCTR specifies the fixed wait cycle to three wait cycles. To change to handshake mode or to use a different number, modify the appropriate bits in MEMCTR.

2-3-4 Handshake Mode

Handshake mode uses the interlock control method in the data transfer sequence , with a transfer enable signals (NRE, NWE) and a data acknowledge signal (NDK).

Handshake mode adjusts the wait cycle for each external device that has a different access speed when the DK generation circuit is provided for each device. CPU of this LSI keeps waiting until the reception of data acknowledge signal to ensure sufficient wait time so that external device can receive data with no error. ["MN101C LSI User's Manual" (Architecture Instructions)]

On handshake mode, watchdog timer can be used to detect NDK not received error.
The reception of NDK is waited until the non-maskable interrupt is generated by the overflow of watchdog timer.

■Access Timing with No Wait Cycles

The NRE or NWE timing is determined based on OSC2. However, since the delay from OSC2 to RE or WE varies depending upon the product, use NRE or NWE as the reference when synchronizing with other devices. Operation timing is same as the timing at NORMAL mode (OSC high oscillation selection).

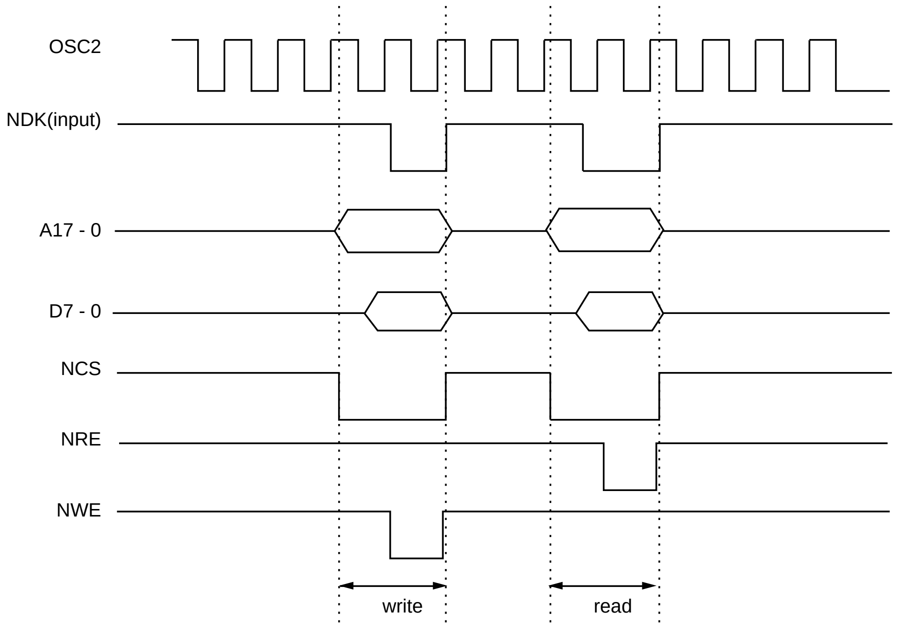


Figure 2-3-4 ROM and RAM Access Timing with No Wait Cycles

■Access Timing with 1 Wait Cycle

Access timing with 2 or 3 wait cycles follows the same pattern. The latter part of the cycle is extended and the timing is the same.

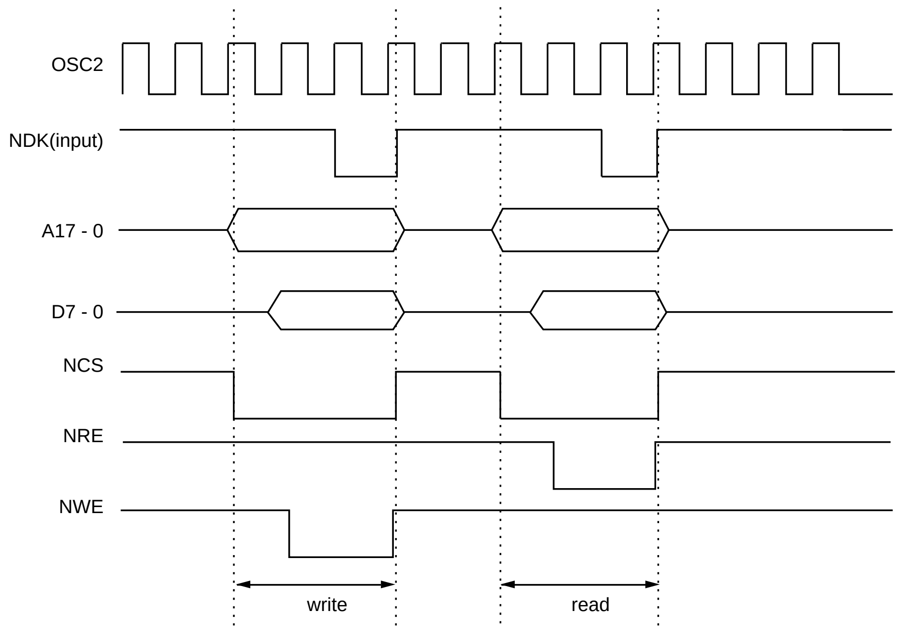


Figure 2-3-5 ROM and RAM Access Timing with 1 Wait Cycle

2-3-5 External Memory Connection Example

■SRAM Connection Example
This example shows connection to SRAM.
The external expansion RAM area is x'02F00' to x'03EFF'.

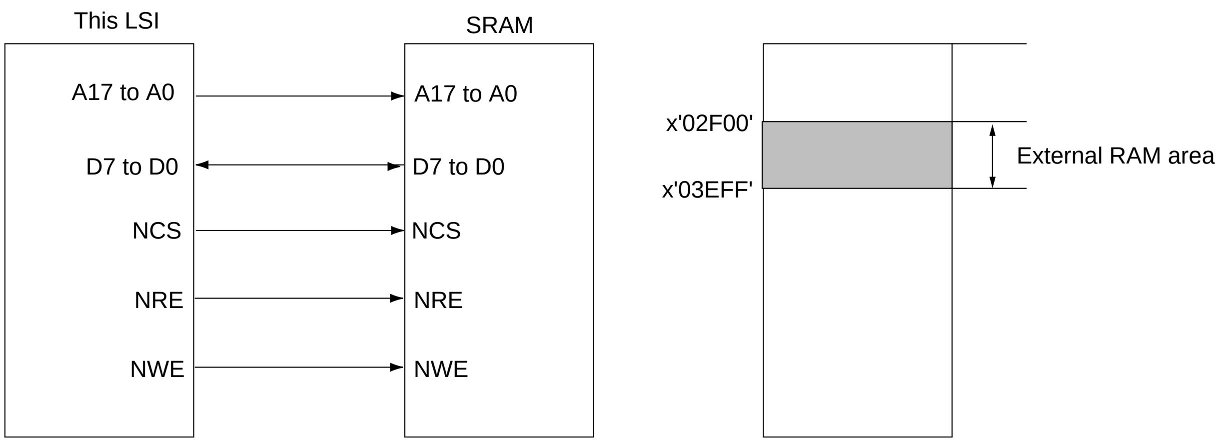


Figure 2-3-7 SRAM Connection Example

2-4 Standby Function

2-4-1 Overview

The MN101C38 series has two sets of system clock oscillator (high speed oscillation, low speed oscillation) for two CPU operating modes (NORMAL and SLOW), each with two standby modes (HALT and STOP). Power consumption can be decreased with using those modes.

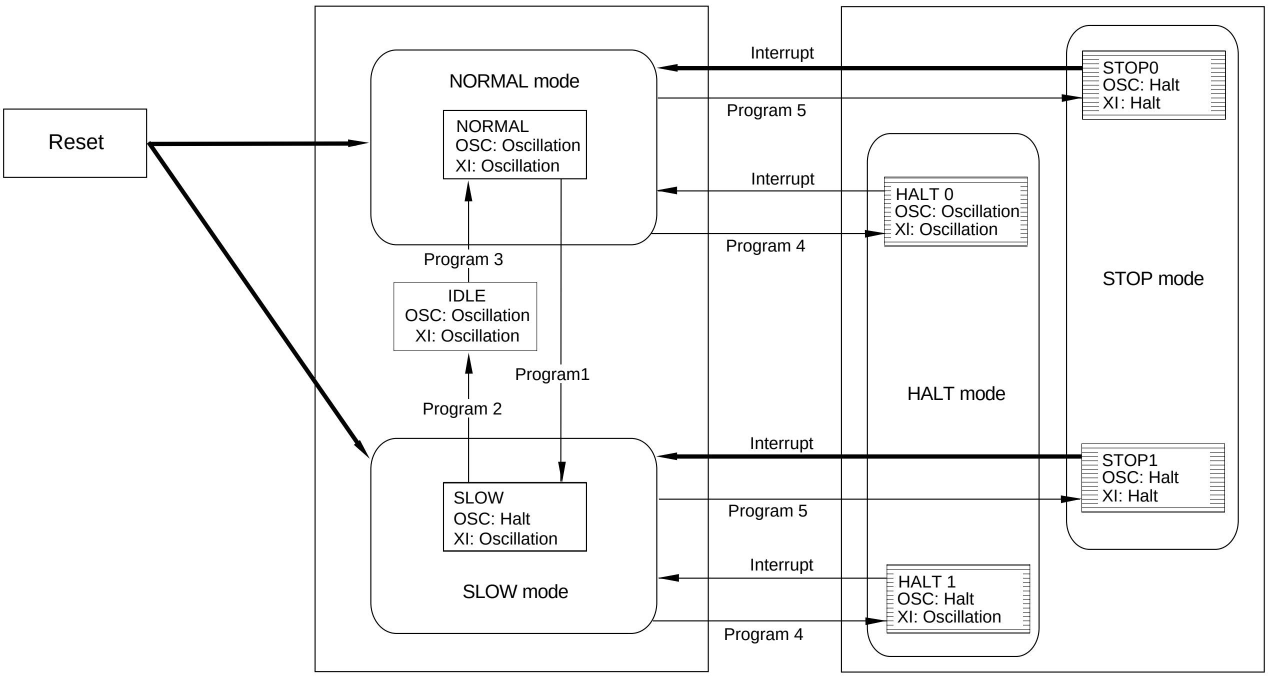


Figure 2-4-1 Transition Between Operation Modes

■HALT Modes (HALT0, HALT1)

– The CPU stops operating. But both of the oscillators remain operational in HALT0 and only the high-frequency oscillator stops operating in HALT1.
– An interrupt returns the CPU to the previous CPU operating mode - that is, to NORMAL from HALT0 or to SLOW from HALT1.

■STOP Modes (STOP0, STOP1)

– The CPU and both of the oscillators stop operating.
– An interrupt restarts the oscillators and, after allowing time for them to stabilize, returns the CPU to the previous CPU operating mode - that is, to NORMAL from STOP0 or to SLOW from STOP1.

■SLOW Mode

– This mode executes the software using the low-frequency clock. Since the high-frequency oscillator is turned off, the device consumes less power while executing the software.

■IDLE Mode

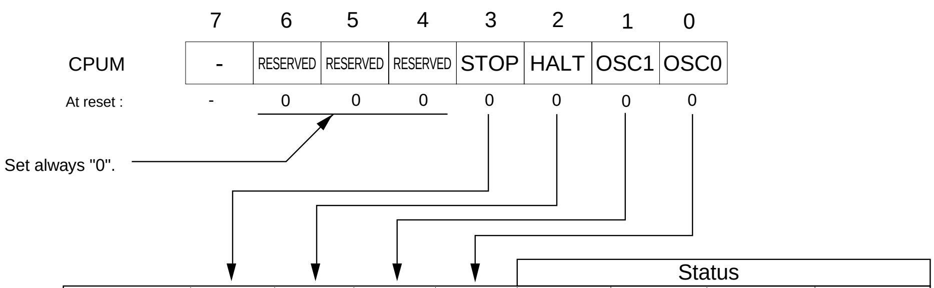
– This mode allows time for the high-frequency oscillator to stabilize when the software is changing from SLOW to NORMAL mode.

To reduce power dissipation in STOP and HALT modes, it is necessary to check the stability of both the output current from pins and port level of input pins. For output pins, the output level should match the external level or direction control should be changed to input mode. For input pins, the external level should be fixed.
The MN101C38 series has two system clock oscillation circuits. OSC is for high-frequency operation (NORMAL mode) and XI is for low-frequency operation (SLOW mode). Transition between NORMAL and SLOW modes or to standby mode is controlled by the CPU mode control register (CPUM). Reset and interrupts are the return factors from standby mode. A wait period is inserted for oscillation stabilization at reset and when returning from STOP mode, but not when returning from HALT mode. High/low-frequency oscillation mode is automatically returned to the same state as existed before entering standby mode.

> ! To stabilize the synchronization at the moment of switching clock speed between high speed oscillation (fosc) and low speed oscillation (fx), fosc should be set to 2.5 times or higher frequency than fx.

2-4-2 CPU Mode Control Register

Transition from one mode to another mode is controlled by the CPU mode control register (CPUM).



Operation mode	STOP	HALT	OSC1	OSC0	Status: OSC1 /OSC2	XI/XO	System clock (fs)	CPU
NORMAL	0	0	0	0	Oscillation	Oscillation	fosc/2	Operating
IDLE	0	0	0	1	Oscillation	Oscillation	fx/4	Operating
SLOW	0	0	1	1	Halt	Oscillation	fx/4	Operating
HALT0	0	1	0	0	Oscillation	Oscillation	fosc/2	Halt
HALT1	0	1	1	1	Halt	Oscillation	fx/4	Halt
STOP0	1	0	0	0	Halt	Halt	Halt	Halt
STOP1	1	0	1	1	Halt	Halt	Halt	Halt

Figure 2-4-2 Operating Mode and Clock Oscillation (CPUM : x'3F00', R/W)

The procedure for transition from NORMAL to HALT or STOP mode is given below.

(1) If the return factor is a maskable interrupt, set the MIE flag in the PSW to "1" and set the interrupt mask (IM) to a level permitting acceptance of the interrupt.

(2) Clear the interrupt request flag (xxxIR) in the maskable interrupt control register (xxxICR) , set the interrupt enable flag (xxxIE) for the return factor, and set the IE flag in the PSW.

(3) Set CPUM to HALT or STOP mode.

> Set the IRWE flag of the memory control register (MEMCTR) to clear interrupt request flag by software.

> The system clock (fs) is fosc/2 at NORMAL mode, and fx/4 at SLOW mode.

2-4-3 Transition between SLOW and NORMAL

The MN101C38 series has two CPU operating modes, NORMAL and SLOW. Transition from SLOW to NORMAL requires passing through IDLE mode.

A sample program for transition from NORMAL to SLOW mode is given below.

```
Program 1
        MOV   x'3', D0            ; Set SLOW mode.
        MOV   D0, (CPUM)
```

Transition from NORMAL to SLOW mode, when the low-frequency clock has fully stabilized, can be done by writing to the CPU mode control register. In this case, transition through IDLE is not needed.

For transition from SLOW to NORMAL mode, the program must maintain the IDLE mode until high-frequency clock oscillation is fully stable. In IDLE mode, the CPU operates on the low-frequency clock.

> **!** For transition from SLOW to NORMAL, oscillation stabilization waiting time is required same as that after reset. Software must count that time.
> We recommend selecting the oscillation stabilization time after consulting with oscillator manufacturers.

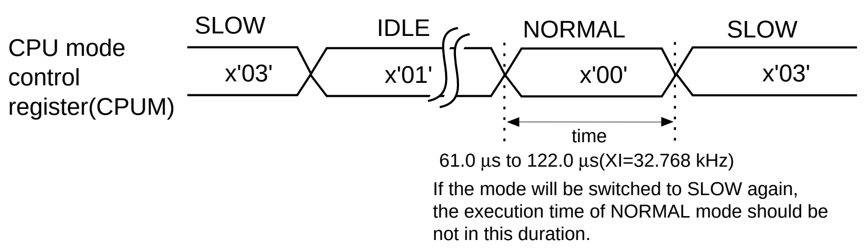
Sample program for transition from SLOW to NORMAL mode is given below.

```
Program 2
              MOV          x'01', D0          ; Set IDLE mode.
              MOV          D0, (CPUM)
```

```
Program 3
        MOV   x'0B', D0      ; A loop to keep approx. 6.7 ms with low-frequency clock (32 kHz)
LOOP    ADD   -1, D0         ; operation when changed to high-frequency clock (20 MHz).
        BNE   LOOP           ;
        SUB   D0, D0         ;
        MOV   D0, (CPUM)     ;  Set NORMAL mode.
```

Refer the following cautions to initiate the program on the transition to SLOW mode in case where the execution time at NORMAL mode is too short.

After the transition to NORMAL mode from SLOW mode, if the mode is returned to SLOW again during 2 to 4 cycles of the low speed oscillation clock, the short pulse can be generated in the system of the clock causing errors.



The following (1) or (2) should be executed on the program by the software.

(1) When the execution time at NORMAL is above that duration.

The following program should be inserted to make the waiting time for more than 4 cycles of low speed oscillation clock, before the transition from NORMAL to SLOW.

Program for waiting time

```
        MOV   WAIT_CONST, D0
LOOP    NOP
        NOP
        NOP
        ADD   -1, D0
        BNE   LOOP
```

High speed oscillation clock [MHz]	Setting value of WAIT_CONST (decimal)
17	195
18	206
19	218
20	229

low speed oscillation clock = 32.768 kHz

(2) When the execution time at NORMAL is above that duration, also its possibility will be cleared at IDLE.

Set the program for switching to SLOW mode, not to NORMAL mode from IDLE.

2-4-4 Transition to STANDBY Modes

The program initiates transitions from a CPU operating mode to the corresponding STANDBY (HALT/STOP) modes by specifying the new mode in the CPU mode control register (CPUM). Interrupts initiate the return to the former CPU operating mode.

Before initiating a transition to a STANDBY mode, however, the program must
(1) Set the maskable interrupt enable flag (MIE) in the processor status word (PSW) to '0' to disable all maskable interrupts temporarily.
(2) Set the interrupt enable flags (xxxIE) in the interrupt control registers (xxxICR) to '1' or '0' to specify which interrupts do and do not initiate the return from the STANDBY mode. Set MIE '1' to enable those maskable interrupts.

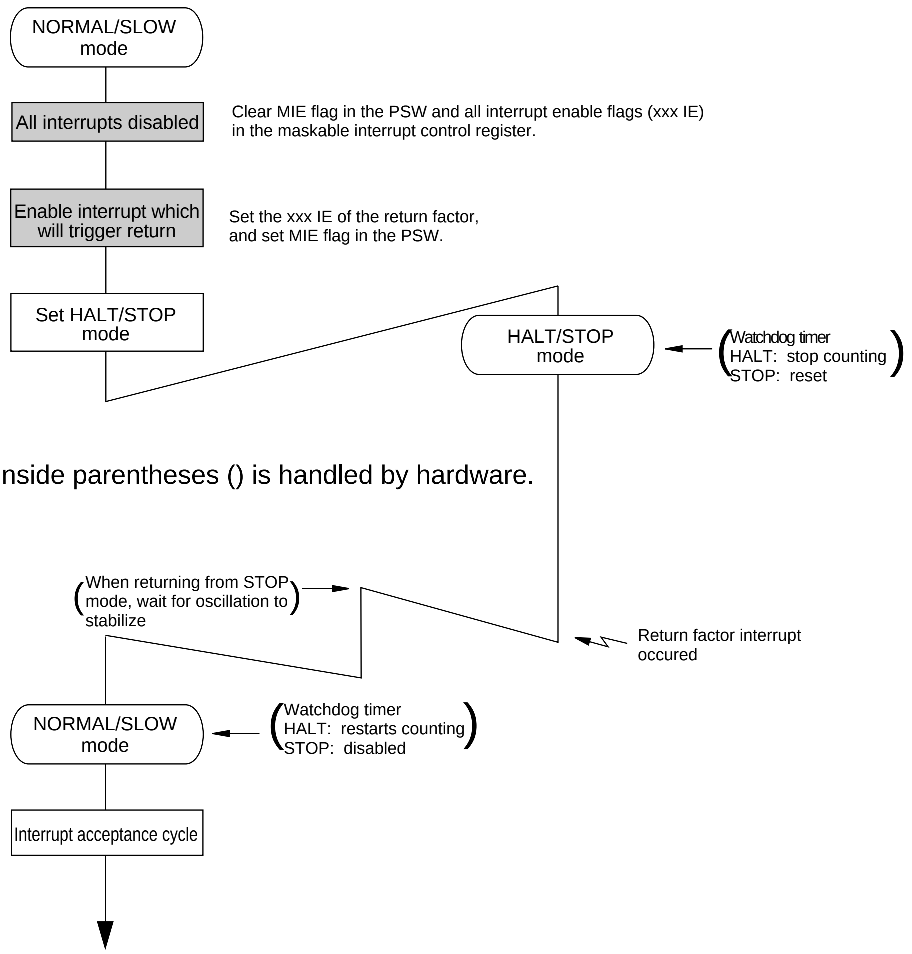


Figure 2-4-3 Transition to/from STANDBY Mode

> If the interrupt is enabled but interrupt priority level of the interrupt to be used is not equal to or higher than the mask level in PSW before transition to HALT or STOP mode, it is impossible to return to CPU operation mode by maskable interrupt.

■Transition to HALT modes

The system transfers from NORMAL mode to HALT0 mode, and from SLOW mode to HALT1 mode. The CPU stops operating, but the oscillators remain operational. There are two ways to leave a HALT mode: a reset or an interrupt. A reset produces a normal reset; an interrupt, an immediate return to the CPU state prior to the transition to the HALT mode. The watchdog timer, if enabled, resumes counting.

Program 4

```
        MOV     x'4',  D0       ; Set HALT mode.
        MOV     D0,  (CPUM)
        NOP                     ; After written in CPUM, some NOP
        NOP                     ; instructions (three or less) are
        NOP                     ; executed.
```

■Transition to STOP mode

The system transfers from NORMAL mode to STOP0 mode, and from SLOW mode to STOP1 mode. In both cases, oscillation and the CPU are both halted. There are two ways to leave a STOP mode: a reset or an interrupt.

Program 5

```
        MOV     x'8',  D0       ; Set STOP mode
        MOV     D0,  (CPUM)
        NOP                     ; After written in CPUM, some NOP
        NOP                     ; instructions (three or less) are
        NOP                     ; executed.
```

Right after the instruction of the transition to HALT, STOP mode, NOP instruction should be inserted 3 times.

2-5 Reset

2-5-1 Reset Operation

The CPU contents are reset and registers are initialized when the NRST pin (P27) is pulled to low.

■Initiating a Reset

There are two methods to initiate a reset.

(1) Drive the NRST pin low.
NRST pin should be held "low" for more than OSC 4 clock cycles (200 ns at a 20 MHz).

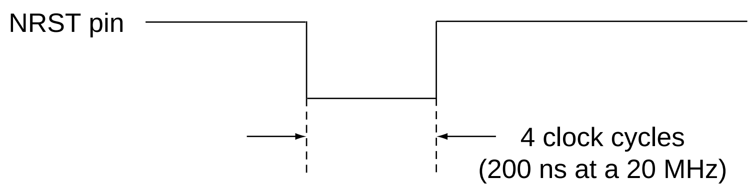


Figure 2-5-1 Minimum Reset Pulse Width

(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transferring to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.

[Chapter 4. 4-4-2 Registers]

> When NRST pin is connected to low power voltage, circuit that gives pulse for enough low level time at sudden unconnected. And reset can be generated even if NRST pin is held "low" for less than OSC 4 clock cycles, take notice of noise.

■Sequence at Reset

(1) When reset pin comes to high level from low level, the internal 14-bit counter (It can be used as watchdog timer, too.) starts its operation by system clock. The period from starting its count from its overflow is called oscillation stabilization wait time.

(2) During reset, internal register and special function register are initiated.

(3) After oscillation stabilization wait time, internal reset is released and program is started from the address written at address x'04000' at interrupt vector table.

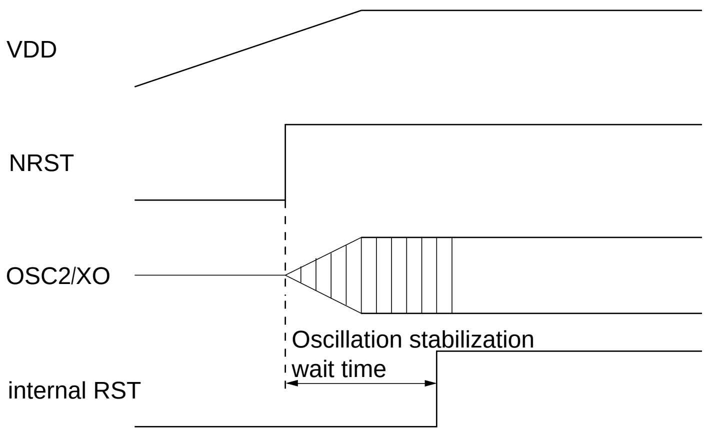


Figure 2-5-2   Reset Released Sequence

> On MN101C38 series, the oscillation is stopped during the NRST pin (p27) is low level.

2-5-2　　Oscillation Stabilization Wait Time

Oscillation stabilization wait time is the period from the stop of oscillation circuit to the stabilization for oscillation. Oscillation stabilization wait time is automatically inserted at releasing from reset and at recovering from STOP mode. At recovering from STOP mode the oscillation stabilization wait time control register (DLYCTR) is set to select the oscillation stabilization wait time. At releasing from reset, oscillation stabilization wait time is fixed.

The timer that counts oscillation stabilization wait time is also used as a watchdog timer at anytime except at releasing from reset and at recovering from STOP mode. Watchdog timer is initiated at reset and at STOP mode and starts counting from the initialize value (x'0000') when system clock (fs) is as clock source. After oscillation stabilization wait time, it continues counting as a watchdog timer.

[☞ Chapter 8　Watchdog timer]

■Block Diagram of Oscillation Stabilization Wait Time (watchdog timer)

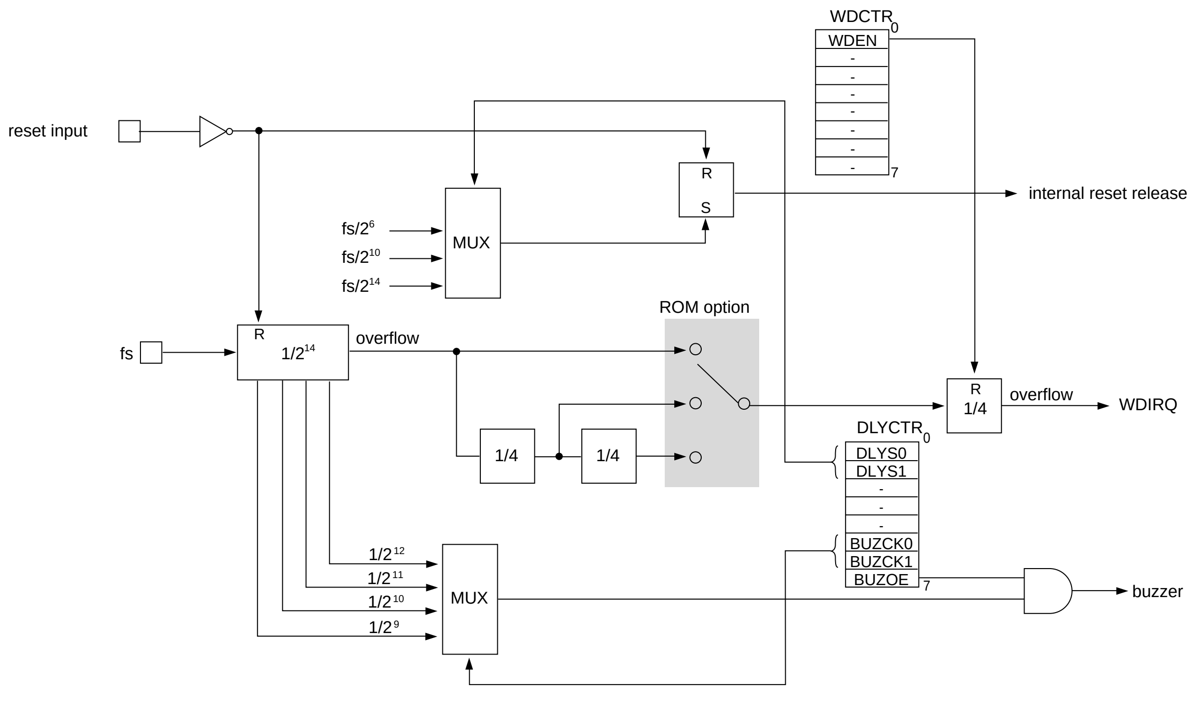


Figure 2-5-3　Block Diagram of Oscillation Stabilization Wait Time (watchdog timer)

■Oscillation Stabilization Wait Time Control Register

	7	6	5	4	3	2	1	0
DLYCTR	BUZOE	BUZCK1	BUZCK0	-	-	-	DLYS1	DLYS0

(At reset : 0 x x - - - 0 0)

DLYS1	DLYS0	Oscillation stabilization wait period selection
0	0	fs/2^{14}
	1	fs/2^{10}
1	0	fs/2^{6}
	1	Do not set.

Note : After reset is released, the oscillation stabilization wait period is fixed at fs/2^{14}.

BUZCK1	BUZCK0	Buzzer output frequency selection
0	0	fs/2^{12}
	1	fs/2^{11}
1	0	fs/2^{10}
	1	fs/2^{9}

BUZOE	P06 output selection
0	P06 port data output
1	P06 buzzer output

Figure 2-5-4 Oscillation Stabilization Wait Time Control Register (DLYCTR : x'03F03', R/W)

■Control the Oscillation Stabilization Wait Time

At recovering from STOP mode, the bit 1-0 (DLYS1, DLYS0) of the oscillation stabilization wait time control register can be set to select the oscillation stabilization wait time from 2^{14}, 2^{10}, 2^{6} $\times$ system clock. The DLYCTR register is also used for controlling of buzzer functions.

[☞ Chapter 9 Buzzer]

At releasing from reset, the oscillation stabilization wait time is fixed to "2^{14} $\times$ system clock". System clock is determined by the CPU mode control register (CPUM).

Table 2-5-1 Oscillation Stabilization Wait Time

DLYS1	DLYS0	period	Oscillation stabilization wait time (at fosc = 20 MHz)
0	0	2^{14} $\times$ Systemclock	1.6384 ms
0	1	2^{10} $\times$ Systemclock	102.4 µs
1	0	2^{6} $\times$ Systemclock	6.4 µs
1	1	Do not set.	

Chapter 3 Interrupts

3-1 Overview

This LSI speeds up interrupt response with circuitry that automatically loads the branch address to the corresponding interrupt service routine from an interrupt vector table : reset, non-maskable interrupts (NMI), 8 maskable peripheral interrupts, and 5 external interrupts.

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. After the interrupt is accepted, the program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack. And an interrupts handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted. Maximum 12 machine cycles before execution, and maximum 11 machine cycles after execution.

Each interrupt has an interrupt control register, which controls the interrupts. Interrupt control register consists of the interrupt level field (LV1-0), interrupt enable flag (IE), and interrupt request flag (IR).

Interrupt request flag (IR) is set to "1" by an interrupt request, and cleared to "0" by the interrupt acceptance. This flag is managed by hardware, but can be rewritten by software.

Interrupt enable flag (IE) is the flag that enables interrupts in the group. There is no interrupt enable flag in non-maskable interrupt (NMI). Once this interrupt request flag is set, it is accepted without any conditions. Interrupt enable flag is set in maskable interrupt. Interrupt enable flag (IE) of each maskable interrupt is valid when the maskable interrupt enable flag (MIE flag) of PSW is "1".

Maskable interrupts have had vector numbers by hardware, but their priority can be changed by setting interrupts level field. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. Maskable interrupts are accepted when its level is higher than the interrupt mask level (IM1-0) of PSW. Non-maskable interrupts are always accepted, regardless of the interrupt mask level.

3-1-1 Functions

Table 3-1-1 Interrupt Functions

Interrupt type	Reset (interrupt)	Non-maskable interrupt	Maskable interrupt
Vector number	0	1	2 to 20
Table address	x'04000'	x'04004'	x'04008' to x'04050'
Starting address	Address specified by vector address		
Interrupt level	-	-	Level 0 to 2 (Set by software)
Interrupt factor	External RST pin input	Errors detection, PI interrupt	External pin input Internal peripheral function
Generated operation	Direct input to CPU core	Input to CPU core from non-maskable interrupt control register (NMICR)	Input interrupt request level set in interrupt level flag (xxxLVn) of maskable interrupt control register (xxxICR) to CPU core.
Accept operation	Always accepts	Always accepts	Acceptance only by the interrupt control of the register (xxxICR) and the interrupt mask level in PSW.
Machine cycles until acceptance	12	12	12
PSW status after acceptance	All flags are cleared to "0".	The interrupt mask level flag in PSW is cleared to "00".	Values of the interrupt level flag (xxxLVn) are set to the interrupt mask level (masking all interrupt requests with the same or the lower priority).

3-1-2 Block Diagram

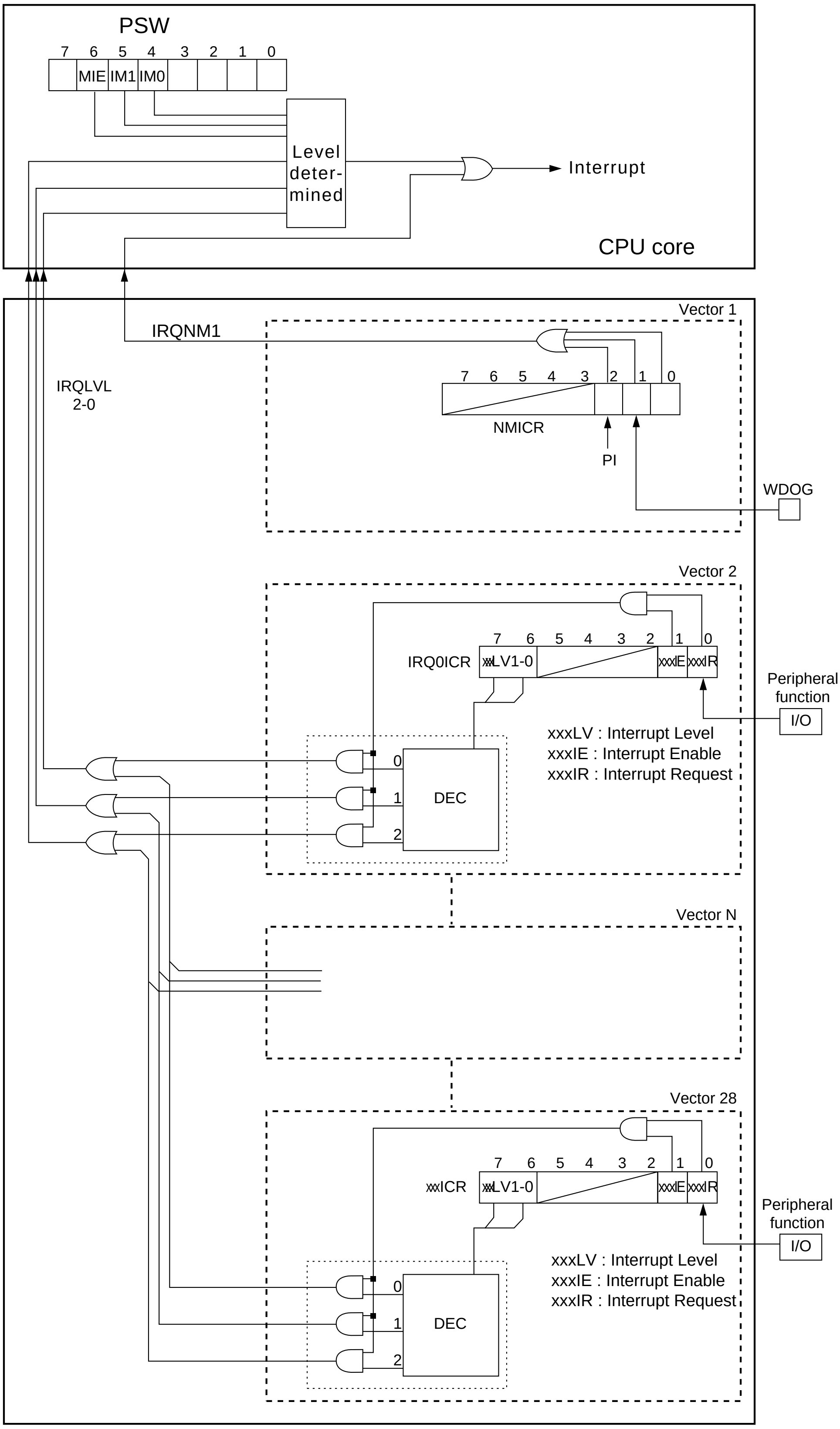


Figure 3-1-1 Interrupt Block Diagram

3-1-3 Operation

■Interrupt Processing Sequence

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. The program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack, and execution branches to the address specified by the corresponding interrupt vector.

An interrupt handler ends by restoring the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

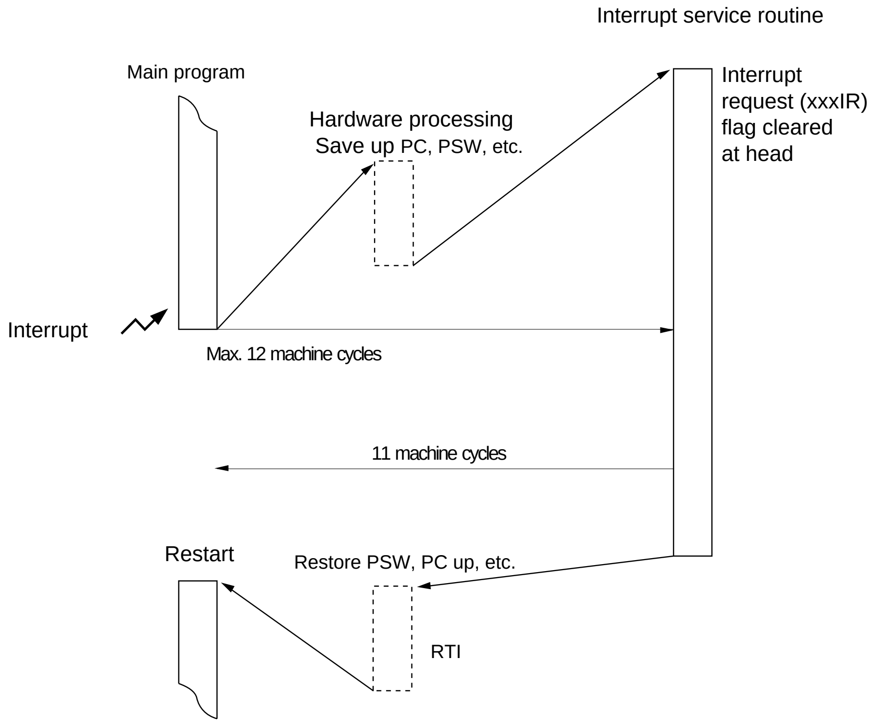


Figure 3-1-2 Interrupt Processing Sequence (maskable interrupts)

Non-maskable interrupts have priority over maskable ones.

■Interrupt Sources and Vector Addresses

Here is the list of interrupt vector address and interrupt group.

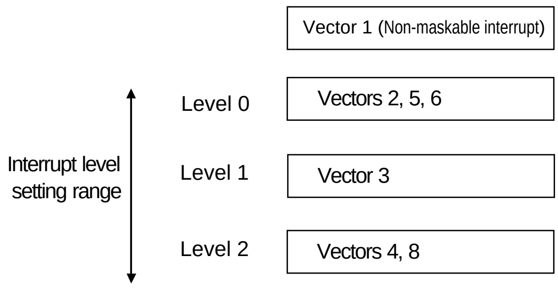
Table 3-1-2 Interrupt Vector Address and Interrupt Group

Vector Number	Vector Address	Interrupt group (Interrupt source)		Control Register (address)	
0	x'04000'	Reset	-	-	-
1	x'04004'	Non-maskable interrupt	NMI	NMICR	x'03FE1'
2	x'04008'	External interrupt 0	IRQ0	IRQ0ICR	x'03FE2'
3	x'0400C'	External interrupt 1	IRQ1	IRQ1ICR	x'03FE3'
4	x'04010'	Reserved	-	-	x'03FE4'
5	x'04014'	Reserved	-	-	x'03FE5'
6	x'04018'	Timer 2 interrupt	TM2IRQ	TM2ICR	x'03FE6'
7	x'0401C'	Time base period	TBIRQ	TBICR	x'03FE7'
8	x'04020'	Serial interface 0 interrupt	SC0IRQ	SC0ICR	x'03FE8'
9	x'04024'	Reserved	-	-	x'03FE9'
10	x'04028'	AD converter interrupt	ADIRQ	ADICR	x'03FEA'
11	x'0402C'	External interrupt 2	IRQ2	IRQ2ICR	x'03FEB'
12	x'04030'	External interrupt 3	IRQ3	IRQ3ICR	x'03FEC'
13	x'04034'	External interrupt 4	IRQ4	IRQ4ICR	x'03FED'
14	x'04038'	Timer 3 interrupt	TM3IRQ	TM3ICR	x'03FEE'
15	x'0403C'	Timer 4 interrupt	TM4IRQ	TM4ICR	x'03FEF'
16	x'04040'	Timer 5 interrupt	TM5IRQ	TM5ICR	x'03FF0'
17	x'04044'	Serial interface 1 interrupt	SC1IRQ	SC1ICR	x'03FF1'
18	x'04048'	Reserved	-	-	x'03FF2'
19	x'0404C'	Reserved	-	-	x'03FF3'
20	x'04050'	Reserved	-	-	x'03FF4'

For unused interrupts and reserved interrupts, set the address the RTI instruction is described on to the corresponded address.

■Interrupt Level and Priority

This LSI allocated vector numbers and interrupt control registers (except reset interrupt) to each interrupt. The interrupt level (except reset interrupt, non-maskable interrupt) can be set by software, per each interrupt group. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. For example, if a vector 3 set to level 1 and a vector 4 set to level 2 request interrupts simultaneously, vector 3 will be accepted.



Priority	Interrupt vector No.
1	Vector 1
2	Vector 2
3	Vector 5
4	Vector 6
5	Vector 3
6	Vector 4
7	Vector 8

Figure 3-1-3 Interrupt Priority Outline

■Determination of Interrupt Acceptance

The following is the procedure from interrupt request input to acceptance.

(1) The interrupt request flag (xxxIR) in the corresponding external interrupt control register (IRQnICR) or internal interrupt control register (xxxICR) is set to '1'.

(2) An interrupt request is input to the CPU, If the interrupt enable flag (xxxIE) in the same register is '1'.

(3) The interrupt level (IL) is set for each interrupt. The interrupt level (IL) is input to the CPU.

(4) The interrupt request is accepted, If IL has higher priority than IM and MIE is '1'.

(5) After the interrupt is accepted, the hardware resets the interrupt request flag (xxxIR) in the interrupt control register (xxxICR) to '0'.

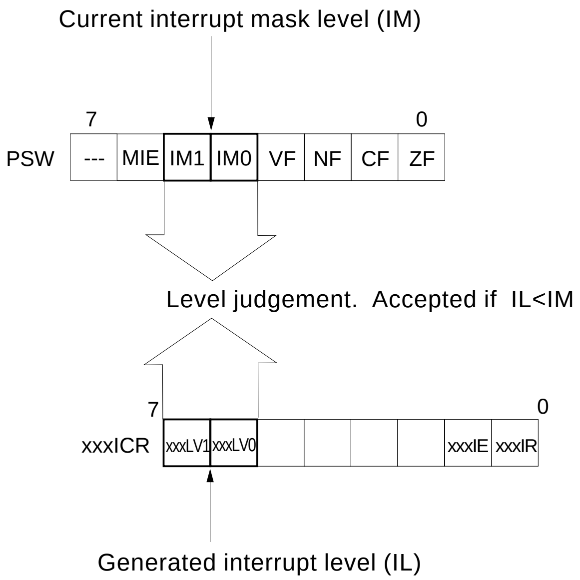


Figure 3-1-4 Determination of Interrupt Acceptance

The corresponding interrupt enable flag (xxxIE) is not cleared to "0", even if the interrupt is accepted.

When the setting is xxxLV1=1, xxxLV0=1, the interrupt is disabled regardless of the value of xxxIE, xxxIR.

MIE='0' and interrupts are disabled when:

- MIE in the PSW is reset to '0' by a program
- Reset is detected

MIE='1' and interrupts are enabled when:

- MIE in the PSW is set to '1' by a program

The interrupt mask level (IM=IM1 - IM0) in the processor status word (PSW) changes when:

- The program alters it directly,
- A reset initializes it to 0 (00b),
- The hardware accepts and thus switches to the interrupt level (IL) for a maskable interrupt.
- Execution of the RTI instruction at the end of an interrupt service routine restores the processor status word (PSW) and thus the previous interrupt mask level.

> The maskable interrupt enable (MIE) flag in the processor status word (PSW) is not cleared to "0" when an interrupt is accepted.

> Non-maskable interrupts have priority over maskable ones.

■Interrupt Acceptance Operation

When accepting an interrupt, the MN101C38 series hardware saves the handy address register, the return address from the program counter, and the processor status word (PSW) to the stack and branches to the interrupt handler using the starting address in the vector table.

The following is the hardware processing sequence after interrupt acceptance.

1. The stack pointer (SP) is updated.
   (SP-6 → SP)
2. The contents of the handy address register (HA) are saved to the stack.
   Upper half of HA → (SP+5)
   Lower half of HA → (SP+4)
3. The contents of the program counter (PC), the return address, are saved to the stack.
   PC bits 18, 17, and 0 → (SP+3)
   PC bits 16-9 → (SP+2)
   PC bits 8-1 → (SP+1)
4. The contents of the PSW are saved to the stack.
   PSW → (SP)
5. The interrupt level (xxxLVn) for the interrupt is copied to the interrupt mask (IMn) in the PSW.
   Interrupt level (xxxLVn) → IMn
6. The hardware branches to the address in the vector table.

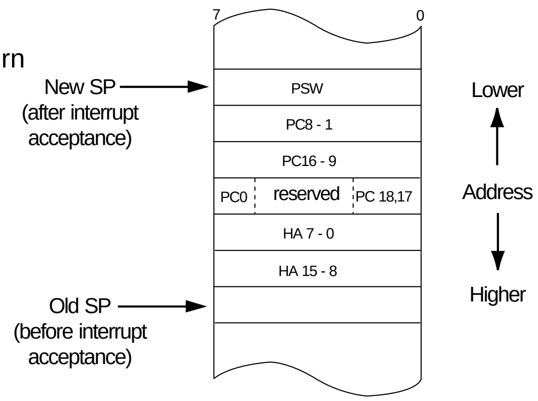


Figure 3-1-5 Stack Operation during interrupt acceptance

■Interrupt Return Operation

An interrupt handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

The following is the processing sequence after the RTI instruction.

1. The contents of the PSW are restored from the stack. (SP)
2. The contents of the program counter (PC), the return address, are restored from the stack. (SP+1 to SP+3)
3. The contents of the handy address register (HA) are restored from the stack. (SP+4, SP+5)
4. The stack pointer is updated. (SP+6 → SP)
5. Execution branches to the address in the program counter.

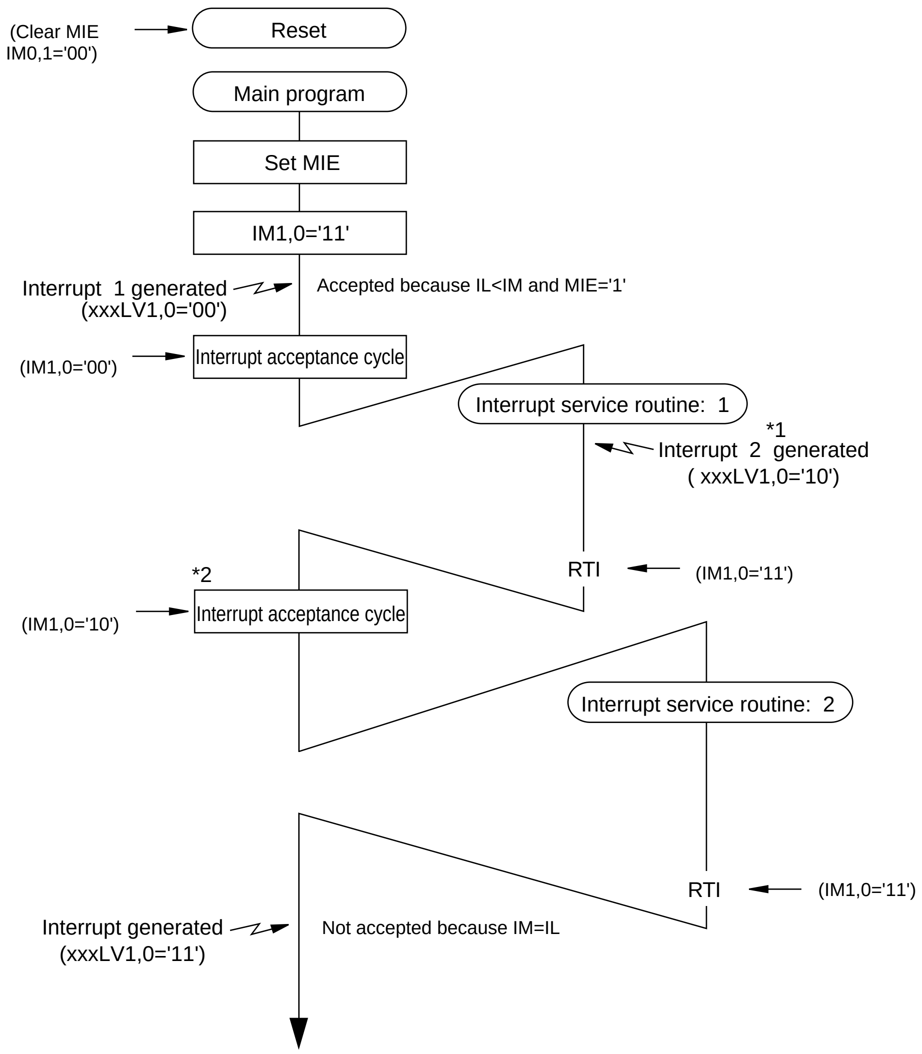
The handy address register is an internal register used by the handy addressing function. The hardware saves its contents to the stack to prevent the interrupt from interfering with operation of the function.

> Registers such as data register, or address register are not saved, so that PUSH instruction should be used to save data register or address register onto the stack, if necessary.

> The address bp6 to bp2, when program counter (PC) are saved to the stack, are reserved. Do not change by program.

■Maskable Interrupt

Figure 3-1-6 shows the processing flow when a second interrupt with a lower priority level (xxxLV1-xxxLV0='10') arrives during the processing of one with a higher priority level (xxxLV1-xxxLV0='00').



Parentheses ( ) indicate hardware processing.

*1 If during the processing of the first interrupt, an interrupt request with an interrupt level (IL) numerically lower than the interrupt mask (IM) arrives, it is accepted as a nested interrupt. If IL ≥ IM, however, the interrupt is not accepted.

*2 The second interrupt, postponed because its interrupt level (IL) was numerically greater than the interrupt mask (IM) for the first interrupt service routine, is accepted when the first interrupt handler returns.

Figure 3-1-6 Processing Sequence for Maskable Interrupts

■Multiplex Interrupt

When an MN101C38 series device accepts an interrupt, it automatically disables acceptance of subsequent interrupts with the same or lower priority level. When the hardware accepts an interrupt, it copies the interrupt level (xxxLVn) for the interrupt to the interrupt mask (IM) in the PSW. As a result, subsequent interrupts with the same or lower priority levels are automatically masked. Only interrupts with higher priority levels are accepted. The net result is that interrupts are normally processed in decreasing order of priority. It is, however, possible to alter this arrangement.

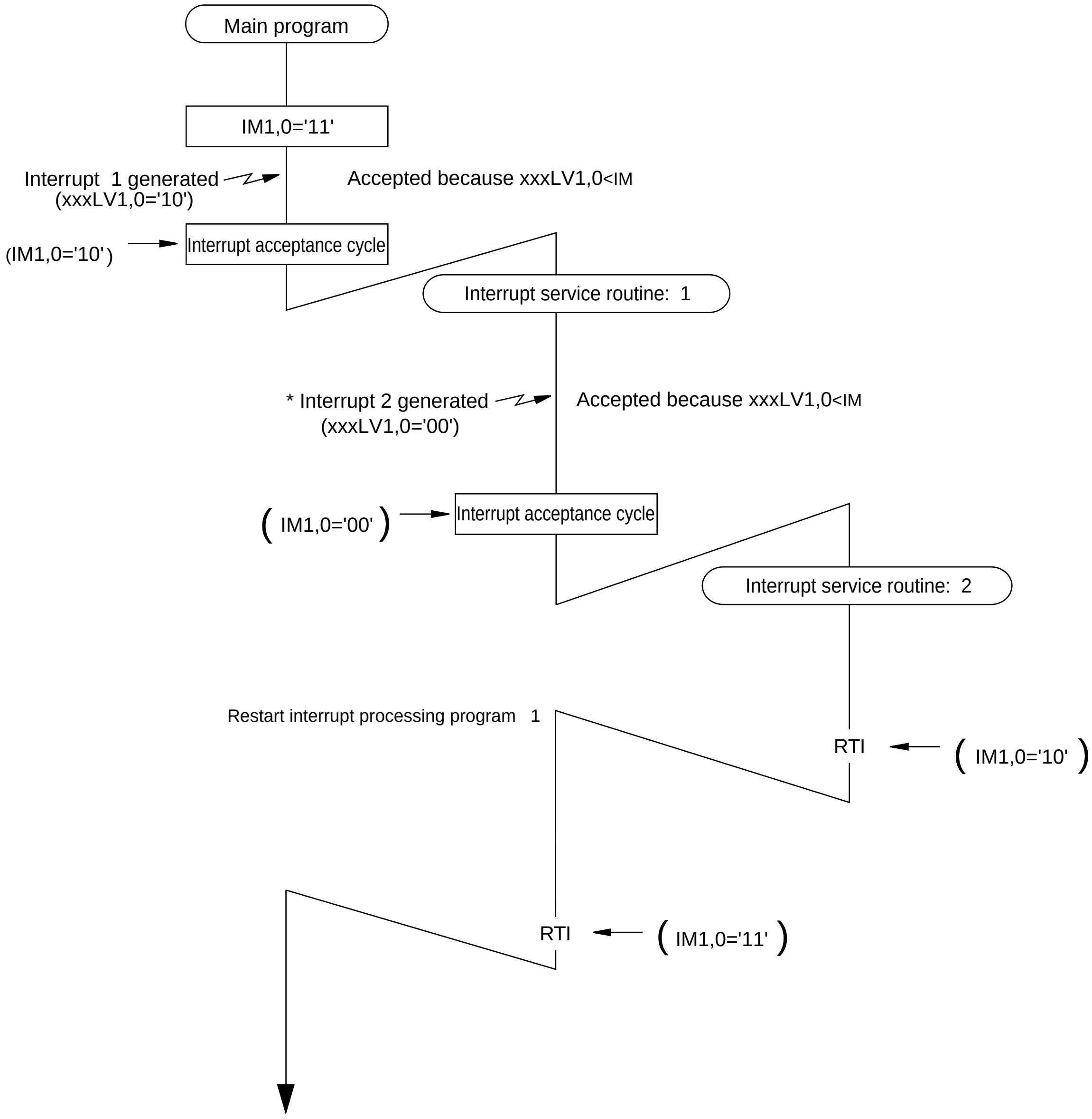
1. To disable interrupt nesting
   - Reset the MIE bit in the PSW to "0."
   - Raise the priority level of the interrupt mask (IM) in the PSW.
2. To enable interrupts with lower priority than the currently accepted interrupt
   - Lower the priority level of the interrupt mask (IM) in the PSW.

Multiplex interrupts are only enabled for interrupts with levels higher than the PSW interrupt mask level (IM).

It is possible to forcibly rewrite IM to accept an interrupt with a priority lower than the interrupt being processed, but be careful of stack overflow.

Do not operate the maskable interrupt control register (xxxICR) when multiple interrupts are enabled. If operation is necessary, first clear the PSW MIE flag to disable interrupts.

Figure 3-1-7 shows the processing flow for multiple interrupts (interrupt 1: xxxLV1-xxxLV0='10', and interrupt 2: xxxLV1-xxxLV0='00').



Parentheses ( ) indicate hardware processing

Figure 3-1-7 Processing Sequence with Multiple Interrupts Enabled

3-1-4 Interrupt Flag Setup

■ Interrupt request flag (IR) setup by the software

The interrupt request flag is operated by the hardware. That is set to "1" when any interrupt factor is generated, and cleared to "0" when the interrupt is accepted. If you want to operate it by the software, the IRWE flag of MEMCTR should be set to "1".

■ Interrupt flag setup procedure

A setup procedure of the interrupt request flag set by the hardware and the software shows as follows ;

Setup Procedure	Description
(1) Disable all maskable interrupts. PSW bp6 : MIE = 0	(1) Clear the MIE flag of PSW to disable all maskable interrupts. This is necessary, especially when the interrupt control register is changed.
(2) Select the interrupt factor.	(2) Select the interrupt factor such as interrupt edge selection, or timer interrupt cycle change.
(3) Enable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 1	(3) Set the IRWE flag of MEMCTR to enable the interrupt request flag to be rewritten. This is necessary only when the interrupt request flag is changed by the software.
(4) Rewrite the interrupt request flag. xxxICR bp0 : xxxIR	(4) Rewrite the interrupt request flag (xxxIR) of the interrupt control register (xxxICR).
(5) Disable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 0	(5) Clear the IRWE flag so that interrupt request flag can not be rewritten by the software.
(6) Set the interrupt level. xxxICR bp7-6 : xxxLV1-0 PSW bp5-4 : IM1-0	(6) Set the interrupt level by the xxxLV1-0 flag of the interrupt control register (xxxICR). Set the IM1-0 flag of PSW when the interrupt acceptance level of CPU should be changed.
(7) Enable the interrupt. xxxICR bp1 : xxxIE = 1	(7) Set the xxxIE flag of the interrupt control register (xxxICR) to enable the interrupt.
(8) Enable all maskable interrupts. PSW bp6 : MIE = 1	(8) Set the MIE flag of PSW to enable maskable interrupts.

3-2 Control Registers

3-2-1 Registers List

Table 3-2-1 Interrupt Control Registers

Register	Address	R/W	Functions	Page
NMICR	x'03FE1'	R/W	Non-maskable interrupt control register	III - 16
IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	III - 17
IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	III - 18
IRQ2ICR	x'03FEB'	R/W	External interrupt 2 control register	III - 19
IRQ3ICR	x'03FEC'	R/W	External interrupt 3 control register	III - 20
IRQ4ICR	x'03FED'	R/W	External interrupt 4 control register	III - 21
TM2ICR	x'03FE6'	R/W	Timer 2 interrupt control register (Timer 2 interrupt)	III - 22
TM3ICR	x'03FEE'	R/W	Timer 3 interrupt control register (Timer 3 interrupt)	III - 23
TM4ICR	x'03FEF'	R/W	Timer 4 interrupt control register (Timer 4 interrupt)	III - 24
TM5ICR	x'03FF0'	R/W	Timer 5 interrupt control register (Timer 5 interrupt)	III - 25
TBICR	x'03FE7'	R/W	Time base interrupt control register (Time base period)	III - 26
SC0ICR	x'03FE8'	R/W	Serial interface 0 interrupt control register (Serial interface 0 interrupt)	III - 27
SC1ICR	x'03FF1'	R/W	Serial interface 1 interrupt control register (Serial interface 1 interrupt)	III - 28
ADICR	x'03FEA'	R/W	A/D converter interrupt control register (A/D converter interrupt)	III - 29

R/W : Readable / Writable.

Writing to the interrupt control register should be done after that all maskable interrupts are set to be disabled by the MIE flag of the PSW register.

If the interrupt level flag (xxxLVn) is set to "level 3", its vector is disabled, regardless of interrupt enable flag and interrupt request flag.

3-2-2 Interrupt Control Registers

The interrupt control registers include the non-maskable interrupt control register (NMICR), the external interrupt control register (IRQnICR) and the internal interrupt control register (xxxICR).

■Non-maskable Interrupt Control Register (NMICR address: x'03FE1')
The non-maskable interrupt control register (NMICR) stores the non-maskable interrupt request. When the non-maskable interrupt request is generated, the interrupt is accepted regardless of the interrupt mask level (IMn) of PSW. The hardware then branches to the address stored at location x'04004' in the interrupt vector table. The watchdog timer overflow interrupt request flag (WDIR) is set to "1" when the watchdog timer overflows. The program interrupt request flag (PIR) is set to "1" when the undefined instruction is executed.

	7	6	5	4	3	2	1	0	
NMICR	-	-	-	-	-	PIR	WDIR	Reserved	(At reset : -----000)

Reserved	Always set to "0".

WDIR	Watchdog interrupt request flag
0	No interrupt request
1	Interrupt request generated

PIR	Program interrupt request flag
0	No interrupt request
1	Interrupt request generated

Figure 3-2-1 Non-maskable Interrupt Control Register (NMICR:x'03FE1', R/W)

On this LSI, when undefined instruction is decoded, the program interrupt request flag (PIR) is set to "1", and the non-maskable interrupt is generated.
If the PIR flag setup is confirmed by the non-maskable interrupt service routine, the reset via the software is recommended. When software reset, the reset pin (P27) outputs "0".

Once the WDIR becomes "1" by generating of non-maskable interrupt, only the program can clear it to "0".

■External Interrupt 0 Control Register (IRQ0ICR)

The external interrupt 0 control register (IRQ0ICR) controls interrupt level of the external interrupt 0, active edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag for external interrupt is set to level 3 (IRQ0LV1=IRQ0LV0="1"), the interrupt of its vector is disabled regardless of the external interrupt request flag and the external interrupt enable flag.

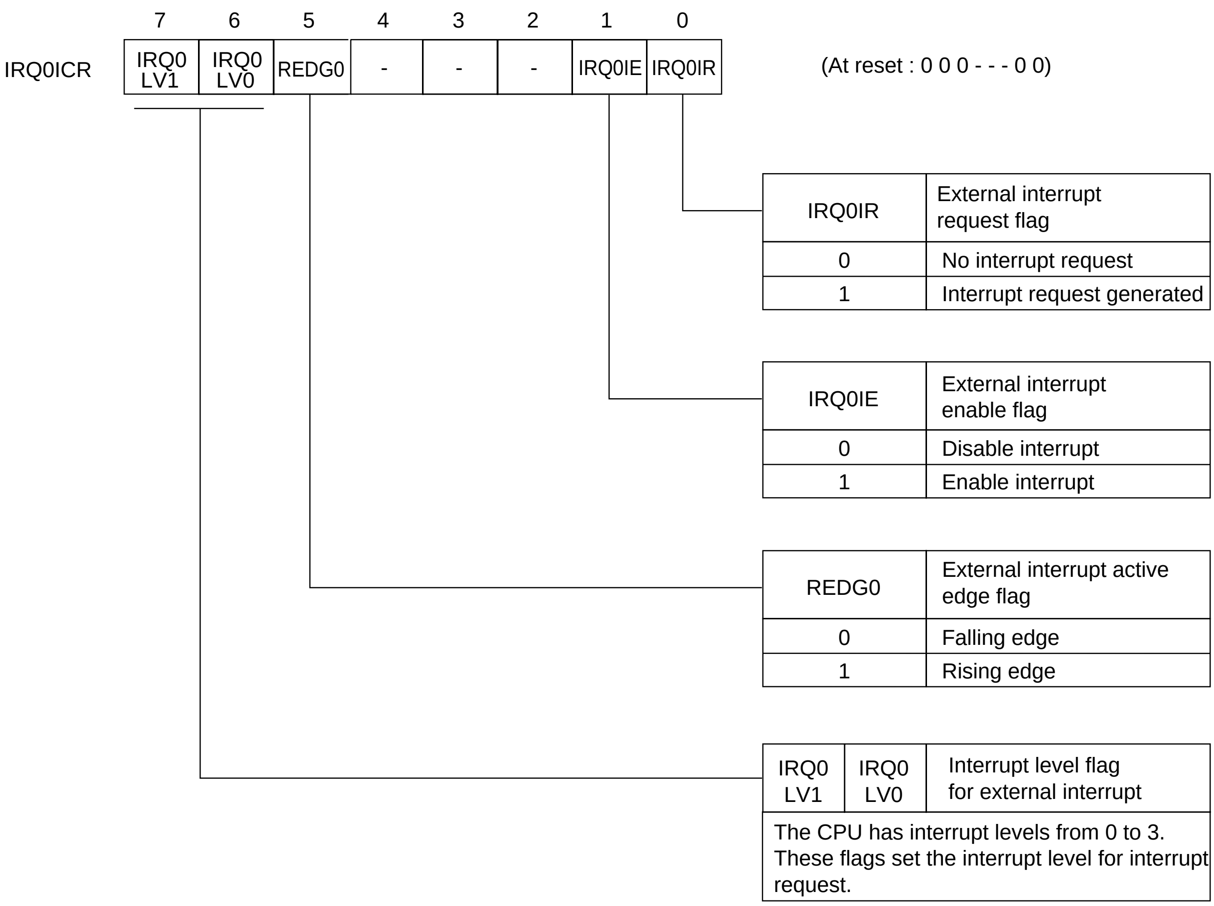


Figure 3-2-2 External Interrupt 0 Control Register (IRQ0ICR : x'03FE2', R/W)

■External Interrupt 1 Control Register (IRQ1ICR)

The external interrupt 1 control register (IRQ1ICR) controls interrupt level of external interrupt 1, active edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag for external interrupt is set to level 3 (IRQ1LV1=IRQ1LV0="1"), the interrupt of its vector is disabled regardless of the external interrupt request flag and the external interrupt enable flag.

	7	6	5	4	3	2	1	0
IRQ1ICR	IRQ1 LV1	IRQ1 LV0	REDG1	-	-	-	IRQ1IE	IRQ1IR

(At reset : 0 0 0 - - - 0 0)

IRQ1IR	External interrupt request flag
0	No interrupt request
1	Interrupt request generated

IRQ1IE	External interrupt enable flag
0	Disable interrupt
1	Enable interrupt

REDG1	External interrupt active edge flag
0	Falling edge
1	Rising edge

IRQ1 LV1	IRQ1 LV0	Interrupt level flag for external interrupt
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-3 External Interrupt 1 Control Register (IRQ1ICR : x'03FE3', R/W)

■External Interrupt 2 Control Register (IRQ2ICR)

The external interrupt 2 control register (IRQ2ICR) controls interrupt level of external interrupt 2, active edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag for external interrupt is set to level 3 (IRQ2LV0=IRQ2LV1="1"), the interrupt of its vector is disabled regardless of the external interrupt request flag and the external interrupt enable flag.

	7	6	5	4	3	2	1	0
IRQ2ICR	IRQ2 LV1	IRQ2 LV0	REDG2	-	-	-	IRQ2IE	IRQ2IR

(At reset : 0 0 0 - - - 0 0)

IRQ2IR	External interrupt request flag
0	No interrupt request
1	Interrupt request generated

IRQ2IE	External interrupt enable flag
0	Disable interrupt
1	Enable interrupt

REDG2	External interrupt active edge flag
0	Falling edge
1	Rising edge

IRQ2 LV1	IRQ2 LV0	Interrupt level flag for external interrupt
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-4 External Interrupt 2 Control Register (IRQ2ICR : x'03FEB', R/W)

■External Interrupt 3 Control Register (IRQ3ICR)

The external interrupt 3 control register (IRQ3ICR) controls interrupt level of external interrupt 3, active edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag for external interrupt is set to level 3 (IRQ3LV1=IRQ3LV0="1"), the interrupt of its vector is disabled regardless of the external interrupt request flag and the external interrupt enable flag.

	7	6	5	4	3	2	1	0
IRQ3ICR	IRQ3 LV1	IRQ3 LV0	REDG3	-	-	-	IRQ3IE	IRQ3IR

(At reset : 0 0 0 - - - 0 0)

IRQ3IR	External interrupt request flag
0	No interrupt request
1	Interrupt request generated

IRQ3IE	External interrupt enable flag
0	Disable interrupt
1	Enable interrupt

REDG3	External interrupt active edge flag
0	Falling edge
1	Rising edge

IRQ3 LV1	IRQ3 LV0	Interrupt level flag for external interrupt
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-5 External Interrupt 3 Control Register (IRQ3ICR : x'03FEC', R/W)

■External Interrupt 4 Control Register (IRQ4ICR)

The external interrupt 4 control register (IRQ4ICR) controls interrupt level of external interrupt 4, active edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag for external interrupt is set to level 3 (IRQ4LV1=IRQ4LV0="1"), the interrupt of its vector is disabled regardless of the external interrupt request flag and the external interrupt enable flag.

	7	6	5	4	3	2	1	0
IRQ4ICR	IRQ4 LV1	IRQ4 LV0	REDG4	-	-	-	IRQ4IE	IRQ4IR

(At reset : 0 0 0 - - - 0 0)

IRQ4IR	External interrupt request flag
0	No interrupt request
1	Interrupt request generated

IRQ4IE	External interrupt enable flag
0	Disable interrupt
1	Enable interrupt

REDG4	External interrupt active edge flag
0	Falling edge
1	Rising edge

IRQ4 LV1	IRQ4 LV0	Interrupt level flag for external interrupt
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-6 External Interrupt 4 Control Register (IRQ4ICR : x'03FED', R/W)

■Timer 2 Interrupt Control Register (TM2ICR)

The timer 2 interrupt control register (TM2ICR) controls interrupt level of timer 2 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (TM2LV1=TM2LV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

	7	6	5	4	3	2	1	0
TM2ICR	TM2 LV1	TM2 LV0	-	-	-	-	TM2IE	TM2IR

(At reset : 0 0 - - - - 0 0)

TM2IR	Interrupt request flag
0	No interrupt request
1	Interrupt request generated

TM2IE	Interrupt enable flag
0	Disable interrupt
1	Enable interrupt

TM2 LV1	TM2 LV0	Interrupt level flag
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-7 Timer 2 Interrupt Control Register (TM2ICR : x'03FE6', R/W)

■Timer 3 Interrupt Control Register (TM3ICR)

The timer 3 interrupt control register (TM3ICR) controls interrupt level of timer 3 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (TM3LV1=TM3LV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

	7	6	5	4	3	2	1	0
TM3ICR	TM3 LV1	TM3 LV0	-	-	-	-	TM3IE	TM3IR

(At reset : 0 0 - - - - 0 0)

TM3IR	Interrupt request flag
0	No interrupt request
1	Interrupt request generated

TM3IE	Interrupt enable flag
0	Disable interrupt
1	Enable interrupt

TM3 LV1	TM3 LV0	Interrupt level flag
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-8 Timer 3 Interrupt Control Register (TM3ICR : x'03FEE', R/W)

■Timer 4 Interrupt Control Register (TM4ICR)

The timer 4 interrupt control register (TM4ICR) controls interrupt level of timer 4 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (TM4LV1=TM4LV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

	7	6	5	4	3	2	1	0
TM4ICR	TM4 LV1	TM4 LV0	-	-	-	-	TM4IE	TM4IR

(At reset : 0 0 - - - - 0 0)

TM4IR	Interrupt request flag
0	No interrupt request
1	Interrupt request generated

TM4IE	Interrupt enable flag
0	Disable interrupt
1	Enable interrupt

TM4 LV1	TM4 LV0	Interrupt level flag
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-9 Timer 4 Interrupt Control Register (TM4ICR : x'03FEF', R/W)

■Timer 5 Interrupt Control Register (TM5ICR)

The timer 5 interrupt control register (TM5ICR) controls interrupt level of timer 5 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (TM5LV1=TM5LV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

	7	6	5	4	3	2	1	0
TM5ICR	TM5 LV1	TM5 LV0	-	-	-	-	TM5IE	TM5IR

(At reset : 0 0 - - - - 0 0)

TM5IR	Interrupt request flag
0	No interrupt request
1	Interrupt request generated

TM5IE	Interrupt enable flag
0	Disable interrupt
1	Enable interrupt

TM5 LV1	TM5 LV0	Interrupt level flag
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-10 Timer 5 Interrupt Control Register (TM5ICR : x'03FF0', R/W)

■Time Base Interrupt Control Register (TBICR)

The time base interrupt control register (TBICR) controls interrupt level of time base interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (TBLV1=TBLV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

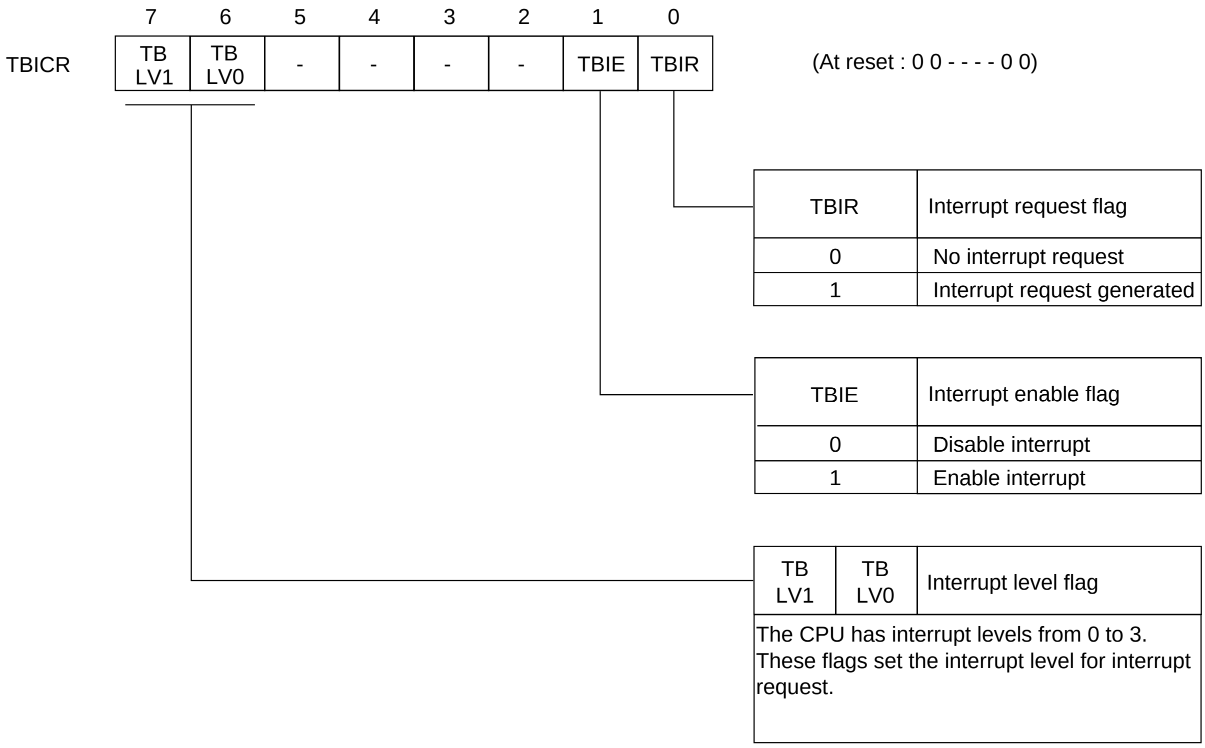


Figure 3-2-11 Time Base Interrupt Control Register (TBICR : x'03FE7', R/W)

■Serial interface 0 Interrupt Control Register (SC0ICR)

The serial interface 0 interrupt control register (SC0ICR) controls interrupt level of serial interface 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (SC0LV1=SC0LV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

	7	6	5	4	3	2	1	0
SC0ICR	SC0 LV1	SC0 LV0	-	-	-	-	SC0IE	SC0IR

(at reset : 0 0 - - - - 0 0)

SC0IR	Interrupt request flag
0	No interrupt request flag
1	Interrupt request generated

SC0IE	Interrupt enable flag
0	Disable interrupt
1	Enable interrupt

SC0 LV1	SC0 LV0	Interrupt level flag
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-12 Serial interface 0 Interrupt Control Register (SC0ICR : x'03FE8', R/W)

■Serial interface 1 Interrupt Control Register (SC1ICR)

The serial interface 1 interrupt control register (SC1ICR) controls interrupt level of serial interface 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (SC1LV1=SC1LV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

	7	6	5	4	3	2	1	0
SC1ICR	SC1 LV1	SC1 LV0	-	-	-	-	SC1IE	SC1IR

(At reset : 0 0 - - - - 0 0)

SC1IR	Interrupt request flag
0	No interrupt request
1	Interrupt request generated

SC1IE	Interrupt enable flag
0	Disable interrupt
1	Enable interrupt

SC1 LV1	SC1 LV0	Interrupt level flag
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-13 Serial interface 1 Interrupt Control Register (SC1ICR : x'03FF1', R/W)

■A/D Conversion Interrupt Control Register (ADICR)

The A/D conversion interrupt control register (ADICR) controls interrupt level of A/D conversion interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0". When the interrupt level flag is set to level 3 (ADLV1=ADLV0="1"), the interrupt of its vector is disabled regardless of the interrupt request flag and the interrupt enable flag.

	7	6	5	4	3	2	1	0
ADICR	AD LV1	AD LV0	-	-	-	-	ADIE	ADIR

(At reset : 0 0 - - - - 0 0)

ADIR	Interrupt request flag
0	No interrupt request
1	Interrupt request generated

ADIE	Interrupt enable flag
0	Disable interrupt
1	Enable interrupt

AD LV1	AD LV0	Interrupt level flag
The CPU has interrupt levels from 0 to 3. These flags set the interrupt level for interrupt request.		

Figure 3-2-14 A/D Conversion Interrupt Control Register (ADICR : x'03FEA', R/W)

3-3 External Interrupts

There are 5 external interrupts in this LSI. The circuit (external interrupt interface) for the external interrupt input signal, is built-in between the external interrupt input pin and the interrupt controller block. This external interrupt interface can manage to do with any kind of external interrupts.

3-3-1 Overview

Table 3-3-1 shows the list for functions which external interrupts 0 to 4 can be used.

Table 3-3-1 External Interrupt Functions

	External interrupt 0 (IRQ0)	External interrupt 1 (IRQ1)	External interrupt 2 (IRQ2)	External interrupt 3 (IRQ3)	External interrupt 4 (IRQ4)
External interrupt input pin	P20	P21	P22	P23	P24, PA0 - PA7
Programmable active edge interrupt	√	√	√	√	√ (P24)
Key input interrupt	-	-	-	-	√ (PA0 - PA7)
Noise filter built-in	√	√	-	-	-
AC zero-cross detection	-	√	-	-	-
Capture trigger for timer 4	√	√	√	-	-
Port 7 synchronous output event	-	-	√	-	-

3-3-2 Block Diagram

■External Interrupt 0 Interface, External Interrupt 1 Interface, Block Diagram

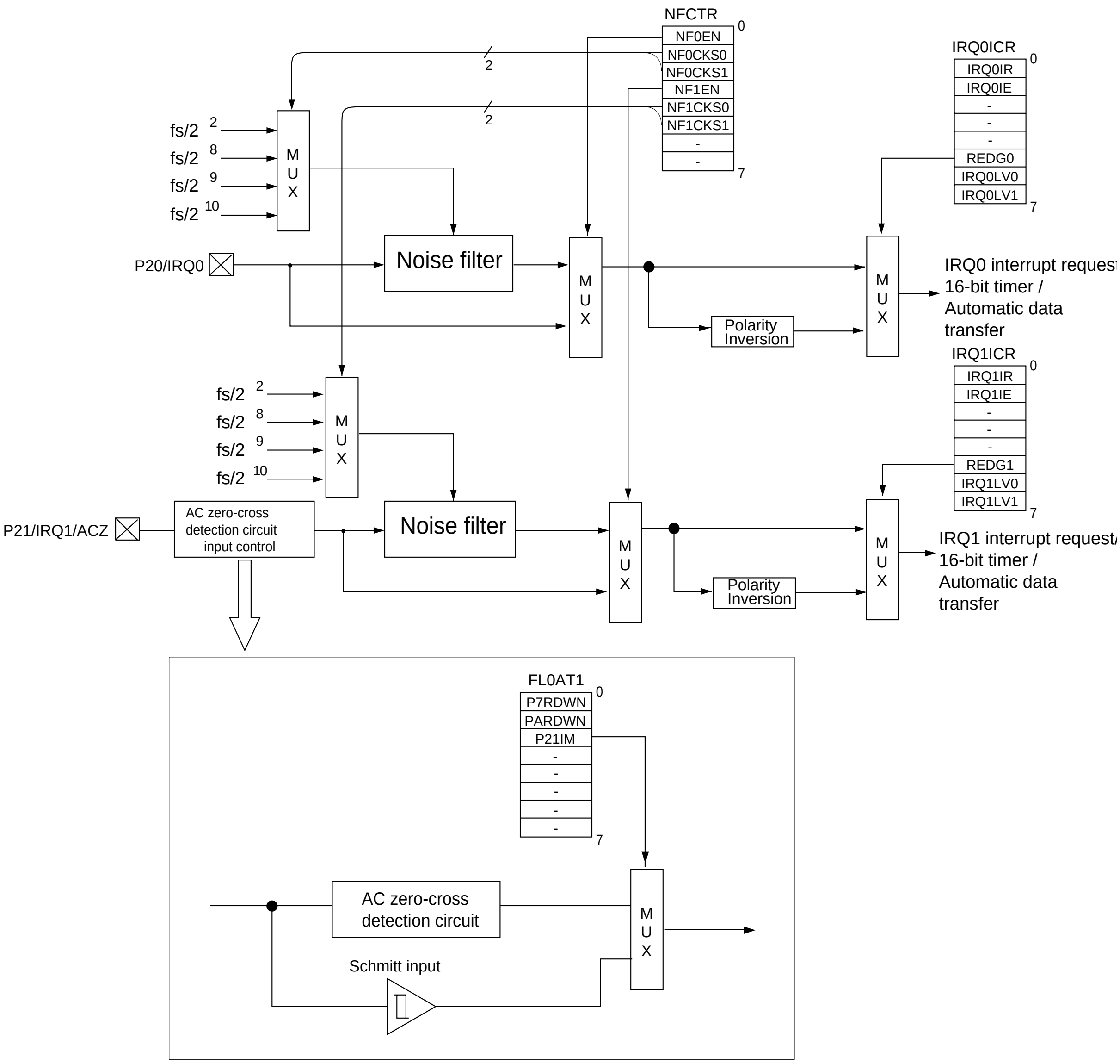


Figure 3-3-1 External Interrupt 0 Interface and External Interrupt 1 Interface Block Diagram

■External Interrupt 2 Interface and External Interrupt 3 Interface Block Diagram

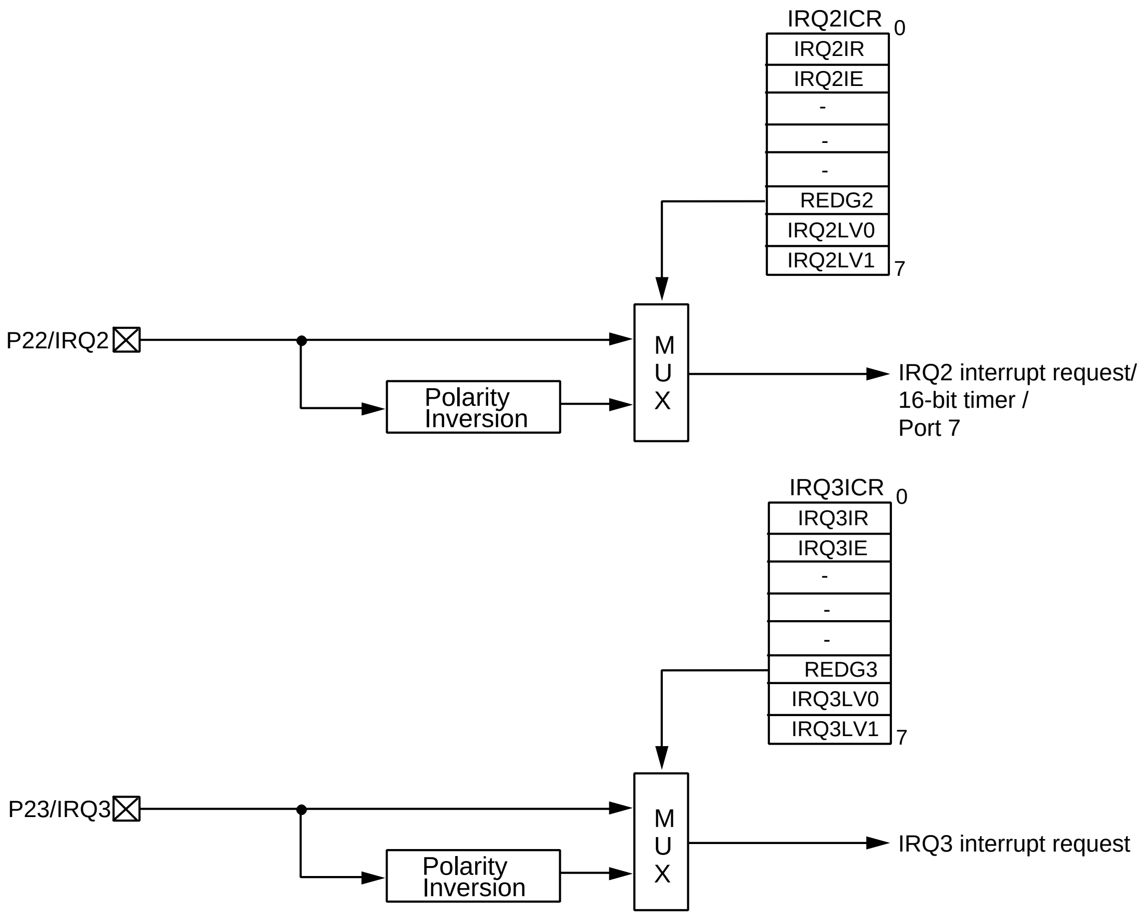


Figure 3-3-2 External Interrupt 2 Interface, External Interrupt 3 Interface

■External Interrupt 4 Interface Block Diagram

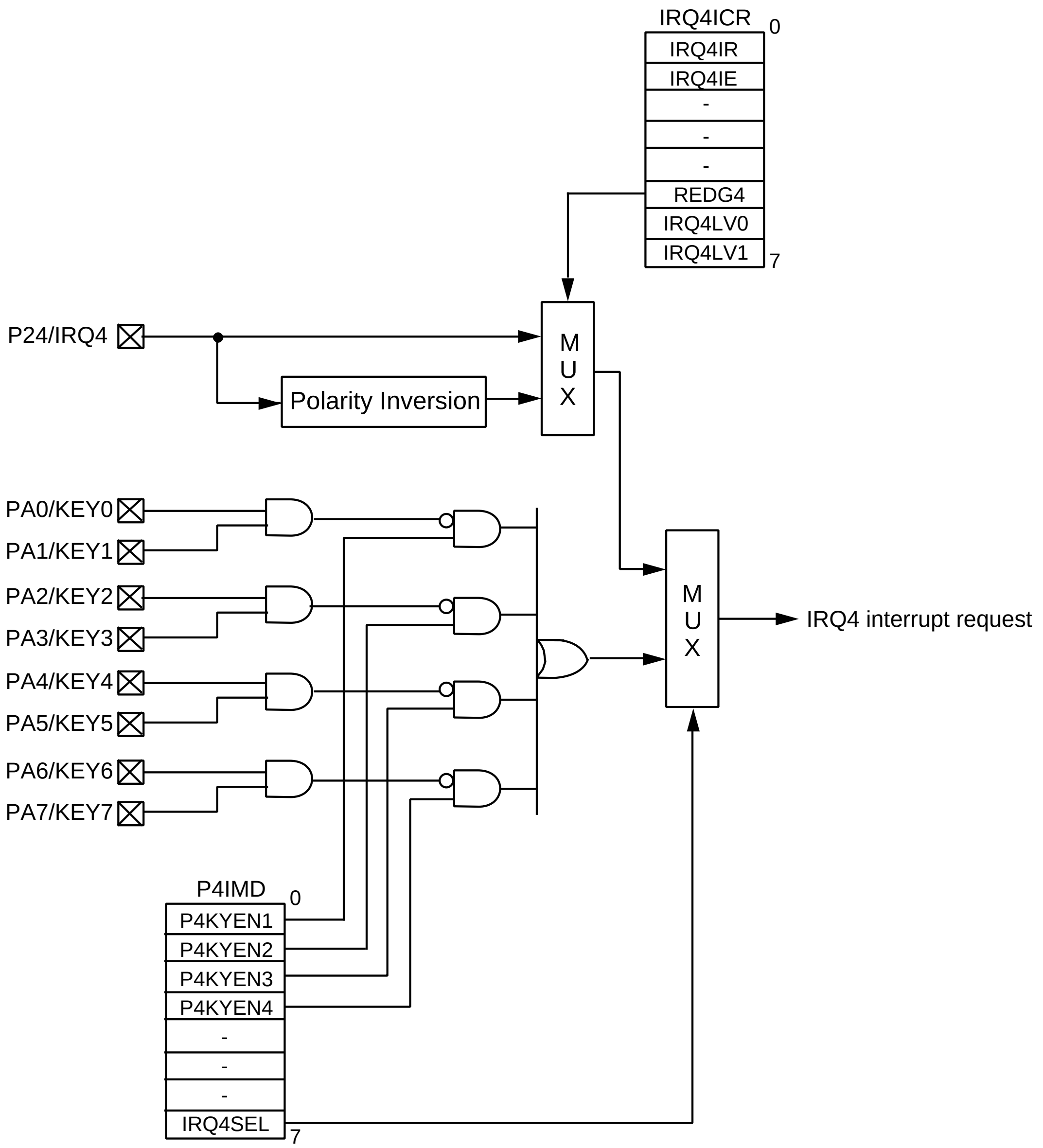


Figure 3-3-3 External Interrupt 4 Interface Block Diagram

3-3-3 Control Registers

The external interrupt input signals, which operated in each external interrupt 0 to 4 interface generate interrupt requests.

External interrupt 0 to 4 interface are controlled by the external interrupt control register (IRQnICR). And external interrupt interface 0 to 1 are controlled by the noise filter control register (NFCTR), and external interrupt interface 4 is controlled by the port 4 key interrupt control register (P4IMD). When the external interrupt 1 is used for AC zero-cross detection, it is controlled by the pin control register 1 (FLOAT1).

Table 3-3-2 shows the list of registers, control external interrupt 0 to 4.

Table 3-3-2 External Interrupt Control Register

External Interrupt	Register	Address	R/W	Function	Page
External interrupt 0	IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	III - 17
	NFCTR	x'03F8A'	R/W	Noise filter control register	III - 35
External interrupt 1	IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	III - 18
	NFCTR	x'03F8A'	R/W	Noise filter control register	III - 35
	FLOAT1	x'03F4B'	R/W	Pin control register 1	III - 36
External interrupt 2	IRQ2ICR	x'03FEB'	R/W	External interrupt 2 control register	III - 19
External interrupt 3	IRQ3ICR	x'03FEC'	R/W	External interrupt 3 control register	III - 20
External interrupt 4	IRQ4ICR	x'03FED'	R/W	External interrupt 4 control register	III - 21
	P4IMD	x'03F3C'	R/W	Port 4 key interrupt control register	III - 37

R/W : Readable / Writable.

■Noise Filter Control Register (NFCTR)

The noise filter control register (NFCTR) sets the noise remove function to IRQ0 and IRQ1 and also selects the sampling cycle of noise remove function.

	7	6	5	4	3	2	1	0
NFCTR	-	-	NF1SCK1	NF1SCK0	NF1EN	NF0SCK1	NF0SCK0	NF0EN

(at reset : - - 0 0 0 0 0 0)

NF0EN	IRQ0/ noise filter setup
0	Noise filter OFF
1	Noise filter ON

NF0CKS1	NF0CKS0	IRQ0 noise filter sampling period
0	0	$fs/2^{2}$
	1	$fs/2^{8}$
1	0	$fs/2^{9}$
	1	$fs/2^{10}$

NF1EN	IRQ1 noise filter sampling setup
0	Noise filter OFF
1	Noise filter ON

NF1CKS1	NF1CKS0	IRQ1/ noise sampling period
0	0	$fs/2^{2}$
	1	$fs/2^{8}$
1	0	$fs/2^{9}$
	1	$fs/2^{10}$

Figure 3-3-4 Noise Filter Control Register (NFCTR : x'03F8A', R/W)

■Pin Control Register 1 (FLOAT 1)

	7	6	5	4	3	2	1	0
FLOAT1	—	—	—	—	—	P21IM	PARDWN	P7RDWN

(at reset : - - - - - 0 0 0)

P7RDWN	Port 7 pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

PARDWN	Port A pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

P21IM	P21 input mode selection
0	Schmitt trigger input
1	ACZ input

Figure 3-3-5 Pin Control Register 1 (FLOAT1 : x'03F4B', R/W)

■Port 4 Key Interrupt Control Register (P4IMD)

The port 4 key interrupt control register (P4IMD) selects if key interrupt is approved, and if external interrupt IRQ4 is approved. Also, this register selects, by 2 bits, which pin on port 4 approved key interrupt.

	7	6	5	4	3	2	1	0
P4IMD	IRQ4SEL	-	-	-	P4KYEN4	P4KYEN3	P4KYEN2	P4KYEN1

(At reset : 0 - - - 0 0 0 0)

P4KYEN1	P41, P40 key interrupt selection
0	disable
1	enable

P4KYEN2	P43, P42 key interrupt selection
0	disable
1	enable

P4KYEN3	P45, P44 key interrupt selection
0	disable
1	enable

P4KYEN4	P47, P46 key interrupt selection
0	disable
1	enable

IRQ4SEL	IRQ4 interrupt source selection
0	external interrupt IRQ4
1	Port 4 key interrupt

Figure 3-3-6 Port 4 Key Interrupt Control Register (P4IMD : x'03F3C', R/W)

3-3-4 Programmable Active Edge Interrupt

■Programmable Active Edge Interrupts (External interrupts 0 to 4)

Through register settings, external interrupts 0 to 4 can generate interrupt at the selected edge either rising or falling edge.

■Programmable Active Edge Interrupt Setup Example (External interrupts 0 to 4)

External interrupt 3 (IRQ3) is generated at the rising edge of the input signal from P23.

The table below provides a setup example for IRQ3.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ3ICR (x'3FEC') bp5 : REDG3 = 1	(1) Set the REDG3 flag of the external interrupt 3 control register (IRQ3ICR) to "1" to specify the rising edge as the active edge for interrupts.
(2) Set the interrupt level. IRQ3ICR (x'3FEC') bp7-6 : IRQ3LV1-0= 10	(2) Set the interrupt priority level in the IRQ3LV1-0 flag of the IRQ3ICR register. If any interrupt request flag had already been set, clear it. [☞ Chapter 3. 3-1-4 Interrupt flag setup]
(3) Enable the interrupt. IRQ3ICR (x'3FEC') bp1 : IRQ3IE = 1	(3) Set the IRQ3IE flag of the IRQ3ICR register to "1" to enable the interrupt.

External interrupt 3 is generated at the rising edge of the input signal from P23.

> The Interrupt request flag may be set to "1" at switching the interrupt edge, so specify the interrupt active edge before the interrupt permission.

> If the interrupt request flag is set to "1" at the switching of the interrupt edge, an interrupt is generated by setting the interrupt enable flag. Therefore, you had better clear the interrupt request flag after the switching of the interrupt edge.
> [☞ Chapter 3. 3-1-4 Interrupt flag setup]

> The external interrupt pin is recommended to be pull-up in advance.

3-3-5 Key Input Interrupt

■Key Input Interrupt (External interrupt 4)
This LSI can set port 4 pin (PA0 - PA7) by 2 bits to key input pin. Key input interrupt can generate an interrupt at the falling edge, if at least 1 key input pin outputs low level.

Key input pin should be pull-up in advance.

Set each bit of the port A input control register (PAIMD) associated with the key input pins to "0" in advance.

When key input interrupt is used, set the IRQ4SEL flag of the key interrupt control register (P4IMD) to "1".

When port 4 key input interrupt is used, set the REDG4 flag of the external interrupt 4 control register (IRQ4ICR) to "0" (falling edge).

■Key Input Interrupt Setup Example (External interrupt 4)

After PA0 to PA3 of port A are set to key input pins and key is input (low level), the external interrupt 4 (IRQ4) is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the key input pin to input. PAIMD (x'3F3A') bp3-0 : PAIMD3-0 = 0000	(1) Set the PADIR3-0 flag of the port A direction control register (PADIR) to "0000" to set PA0 to PA3 pins to input pins.
(2) Set the pull-up resistance. PAPLUD (x'3F4A') bp3-0 : PAPLUD3-0 = 1111	(2) Set the PAPLUD 3-0 flag of the port A pull-up/down resistor control register (PAPLUD) to "1111" to add the pull-up resistance to PA0 to PA3 pins.
(3) Select the key input interrupt. P4IMD (x'3F3C') bp7 : IRQ4SEL = 1	(3) Set the IRQ4SEL flag of the port A key interrupt control register (PAIMD) to "1" to select the external interrupt A source to the port A key interrupt.
(4) Select the key input pin. P4IMD (x'3F3C') bp1-0 : PAKYEN2-1= 11	(4) Set the PAKYEN 2-1 flag of the port A key interrupt control register (P4IMD) to "11" to set PA0 to PA3 pins to key input pins.
(5) Specify the interrupt active edge IRQ4ICR (x'3FED') bp5 : REDG4 = 0	(5) Specify the falling edge to the interrupt active edge by setting "0" to the REDG4 flag of the external interrupt 4 control register (IRQ4ICR).
(6) Set the interrupt level. IRQ4ICR (x'3FED') bp7-6 : IRQ4LV1-0= 10	(6) Set the interrupt level by the IRQ4LV1-0 flag of the IRQ4ICR register. If the interrupt request flag has been already set, clear it. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(7) Enable the interrupt. IRQ4ICR (x'3FED') bp1 : IRQ4IE = 1	(7) Set the IRQ4IE flag of the IRQ4ICR register to "1" to enable the interrupt.

Note : The above (3) and (4), and (5) and (6) can be set at the same time.

If there is at least one input signal, from the PA0 to PA3 pins, shows low level, the external interrupt 4 is generated at the falling edge.

The setup of the key input should be done before the interrupt is enabled.

3-3-6 Noise Filter

■Noise Filter (External interrupts 0 to1)
Noise filter reduces noise by sampling the input waveform from the external interrupt pins (IRQ0, IRQ1). Its sampling cycle can be selected from 4 types (fs/2^2, fs/2^8, fs/2^9, fs/2^{10}).

■Noise Remove Selection (External interrupts 0 to 1)
Noise remove function can be used by setting the NFnEN flag of the noise filter control register (NFCTR) to "1".

Table 3-3-3 Noise Remove Function

NFnEN	IRQ0 input (P20)	IRQ1 input (P21)
0	IRQ0 Noise filter OFF	IRQ1 Noise filter OFF
1	IRQ0 Noise filter ON	IRQ1 Noise filter ON

■Sampling Cycle Setup (External interrupts 0 and 1)
The sampling cycle of noise remove function can be set by the NFnCKS 1- 0 flag of the NFCTR register.

Table 3-3-4 Sampling Cycle / Time of Noise Remove Function

NFnCKS1	NFnCKS0	Sampling cycle	High-frequency oscillation			
			at fosc=20 MHz		at fosc=8 MHz	
0	0	fs/2^2	2.5 MHz	400 ns	1 MHz	1 µs
	1	fs/2^8	39.06 kHz	25.60 µs	15.62 kHz	64 µs
1	0	fs/2^9	19.53 kHz	51.20 µs	7.81 kHz	128 µs
	1	fs/2^{10}	9.77 kHz	102.40 µs	3.91 kHz	256 µs

■Noise Remove Function Operation (External interrupts 0 to 1)
After sampling the input signal to the external interrupt pins (IRQ0, IRQ1) by the set sampling time, if the same level comes continuously three times, that level is sent to the inside of LSI. If the same level does not come continuously three times, the previous level is sent. It means that only the signal with the width of more than " Sampling time × 3 sampling clocks " can pass through the noise filter, and other much narrower signals are removed, because those are regarded as noise.

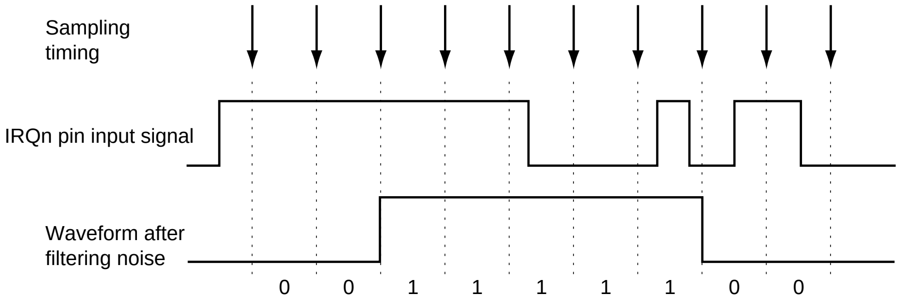


Figure 3-3-7 Noise Remove Function Operation

Noise filter can not be used at STOP mode and HALT mode.

■Noise Filter Setup Example (External interrupt 0 and 1)

Noise remove function is added to the input signal from P20 pin to generate the external interrupt 0 (IRQ0) at the rising edge. The sampling clock is set to $fs/2^2$, and the operation state is fosc = 20 MHz. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(1) Set the REDG 0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to specify the interrupt active edge to the rising edge.
(2) Select the sampling clock. NFCTR (x'3F8A') bp2-1 : NF0CKS1-0 = 00	(2) Select the sampling clock to $fs/2^2$ by the NF0CKS1-0 flag of the noise filter control register (NFCTR).
(3) Set the noise filter operation. NFCTR (x'3F8A') bp0 : NF0EN = 1	(3) Set the NF0EN flag of the NFCTR register to "1" to add the noise filter operation.
(4) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(4) Set the interrupt level by the IRQ0LV 1- 0 flag of the IRQ0ICR register. If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(5) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(5) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.

Note : The above (2) and (3) are set at the same time.

The input signal from the P20 pin generates the external interrupt 0 at the rising edge of the signal, after passing through the noise filter.

> ! The setup of the noise filter should be done before the interrupt is enabled.

> The external interrupt pins are recommended to be pull-up in advance.

3-3-7 AC Zero-cross Detector

This LSI has AC zero-cross detector circuit. The P21/SENS pin is the input pin of AC zero-cross detector circuit. AC zero-cross detector circuit output the high level when the input level is at the middle, and outputs the low level at other level.

■AC Zero-cross Detector (External interrupt 1)
AC zero-cross detector sets the IRQ1 pin to the high level when the input signal (P21/SENS pin) is at intermediate range. At the other level, IRQ1 pin is set to the low level. AC zero-cross can be detected by setting the P21IM flag of the pin control register (FLOAT1) to "1".

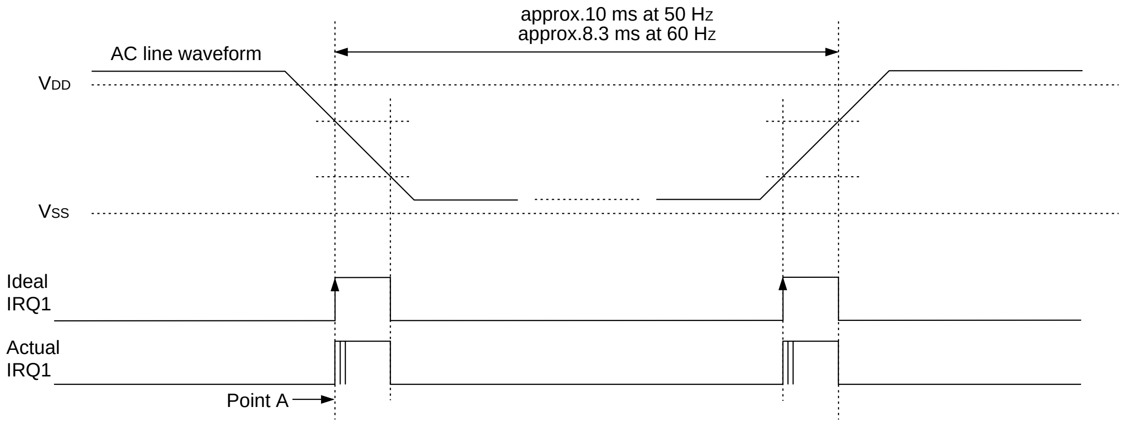


Figure 3-3-8 AC Line Waveform and IRQ1 Generation Timing

Actual IRQ1 interrupt request is generated several times at crossing the 1/2 VDD of AC line waveform. So, the filtering operation by the program is necessary.

If you select the noise filter, the judgement of this program can be easier. But it can not be used for the recover when OSC is stopped at the back up mode.

■AC Zero-cross Detector Setup Example (External interrupt 1)
AC zero-cross detector generates the external interrupt 1 (IRQ1) by using P21/SENS pin.
The sampling clock is set to fs/2^2, and the noise filter is used.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the interrupt edge. IRQ1ICR (x'3FE3') bp5 : REDG1 = 1	(1) Set the REDG1 flag of the external interrupt 1 control register (IRQ1ICR) to "1" to specify the active edge of the external interrupt to "rising".
(2) Select the noise filter and its sampling clock. NFCTR (x'3F8A') bp3 : NF1EN = 1 bp5-4 : NF1CKS1-0 = 00	(2) Select the noise filter by the NF1EN, NFCKS1-0 flag of the noise filter control register (NFCTR). And select fs/2^2 for its sampling cycle.
(3) Select the AC zero-cross detector signal. FLOAT1 (x'3F4B') bp2 : P21IM = 1	(3) Set the P21IM flag of the pin control register 1 (FLOAT1) to "1" to select the AC zero-cross detector signal as the external interrupt 1 generation factor.
(4) Set the interrupt level. IRQ1ICR (x'3FE3') bp7-6 : IRQ1LV1-0= 10	(4) Set the interrupt level by the IRQ1LV 1-0 flag of the IRQ1ICR register. If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(5) Enable the interrupt. IRQ1ICR (x'3FE3') bp1 : IRQ1IE = 1	(5) Set the IRQ1IE flag of the IRQ1ICR register to "1" to enable the interrupt.

When the input signal level from P21/SENS pin crosses 1/2 V_{DD}, the external interrupt 1 is generated.

Chapter 4 I/O Ports

4-1 Overview

4-1-1 I/O Port Diagram

A total of 71 pins on this LSI, including those shared with special function pins, are allocated for the 9 I/O ports of ports 0 to 3, ports 5 to 8 and port A. Each I/O port is assigned to its corresponding special function register area in memory. I/O ports are operated in byte or bit units in the same way as RAM.

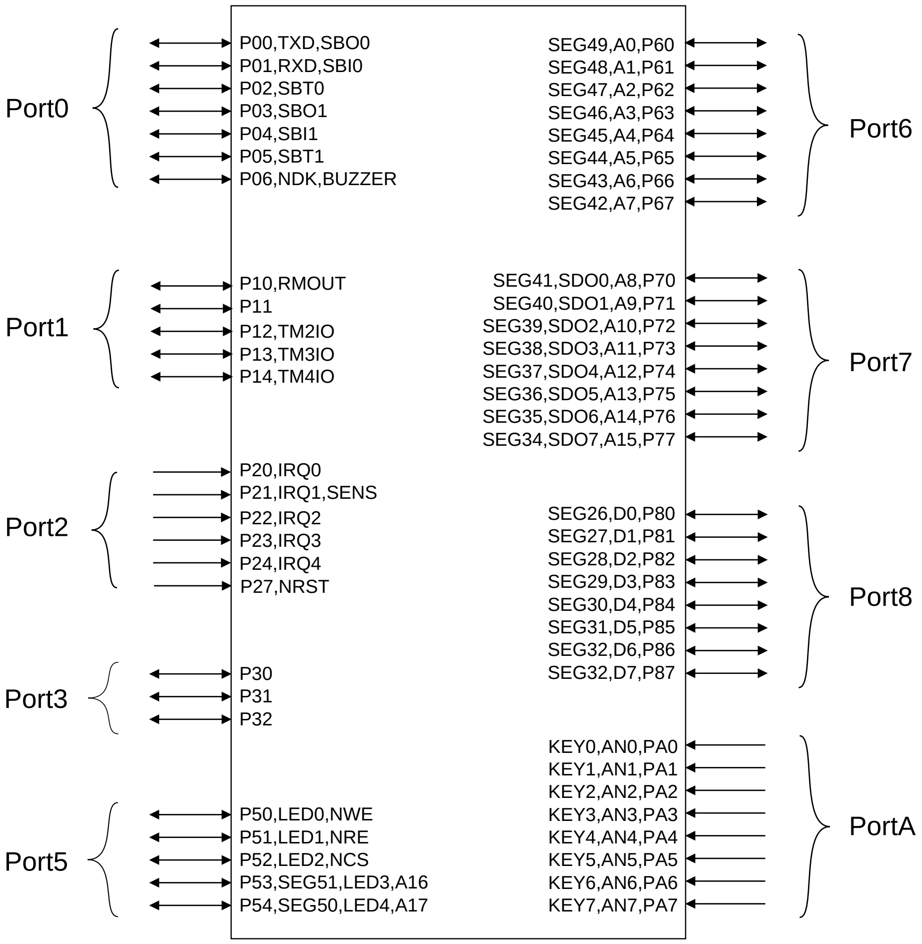


Figure 4-1-1 I/O Port Functions

4-1-2 I/O Port Status at Reset

Table 4-1-1 I/O Port Status at Reset (Single chip mode)

Port Name	I/O mode	Pull-up / Pull-down resistor	I/O port, special functions
Port 0	Input mode	No pull-up resistor	I/O port
Port 1	Input mode	No pull-up resistor	I/O port
Port 2	Input mode	No pull-up resistor	I/O port
Port3	Input mode	No pull-up resistor	I/O port
Port 5	Input mode	No pull-up resistor	I/O port
Port 6	Input mode	No pull-up resistor	I/O port
Port 7	Input mode	No pull-up / pull-down resistor	I/O port
Port 8	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up / pull-down resistor	I/O port

Calculate the resistor of pull-up and pull-down, based on the electrical characteristics of LSI User's Manual of each model as shown below:

Pull-up resistor

For example: When pins maintain the low level guaranteed performance by the prescription of the electrical characteristics. (Notes: It is not 0 V.)

When V_{DD} = 5 V V_{IN} = 1.5 V
Input current : Min = - 30 µA, Typ = - 100 µA, Max = - 300 µA.
(- means that the current runs from microcontroller.)
Convert this to resistor value: Typ = 35 kΩ
However, this value changes widely by temperature. If it changes between - 40 °C and 85 °C, it may be Min = 11.7 kΩ to Max = 117 kΩ.

Pull-down resistor

For example: When pins maintain the high level guaranteed performance by the prescription of the electrical characteristics. (Notes: It is not V_{DD}.)

When V_{DD} = 5 V V_{IN} = 3.5 V
Input current : Min = - 30 µA, Typ = - 100 µA, Max = - 300 µA.
Convert this to resistor value: Typ = 35 kΩ
However, this value changes widely by temperature. If it changes between - 40 °C and 85 °C, it may be Min = 11.7 kΩ to Max = 117 kΩ.

4-1-3 Control Registers

Ports 0 to 3, 5 to 8 and A are controlled by the data output register (PnOUT), the data input register (PnIN), the I/O direction control register (PnDIR), the pull-up resistor control register (PnPLU) and the pull-up / pull-down resistor control resister (PnPLUD) and registers (SYSMD, P1OMD, PAIMD, P4IMD, EXADV, FLOAT1, FLOAT2, LCCTR) that control special function pin.

This I/O control is valid at selection of the special function, as well.

Table 4-1-3 shows the registers to control ports 0 to 3, 5 to 8 and A ;

Table 4-1-2 I/O Port Control Registers List (1/2)

	Register	Address	R/W	Function	Page
Port 0	P0OUT	x'03F10'	R/W	Port 0 output register	IV-7
	P0IN	x'03F20'	R	Port 0 input register	IV-7
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV-7
	P0PLU	x'03F40'	R/W	Port 0 pull-up resistor control register	IV-7
Port 1	P1OUT	x'03F11'	R/W	Port 1 output register	IV-13
	P1IN	x'03F21'	R	Port 1 input register	IV-13
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-13
	P1PLU	x'03F41'	R/W	Port 1 pull-up resistor control register	IV-13
	P1OMD	x'03F39'	R/W	Port 1 output mode register	IV-14
Port 2	P2OUT	x'03F12'	R/W	Port 2 output register	IV-18
	P2IN	x'03F22'	R	Port 2 input register	IV-18
	P2PLU	x'03F42'	R/W	Port 2 pull-up resistor control register	IV-18
Port 3	P3OUT	x'03F13'	R/W	Port 3 output register	IV-21
	P3IN	x'03F23'	R	Port 3 input register	IV-21
	P3DIR	x'03F33'	R/W	Port 3 direction control register	IV-21
	P3PLU	x'03F43'	R/W	Port 3 pull-up resistor control register	IV-21

Table 4-1-3 I/O Port Control Registers List (2/2)

	Register	Address	R/W	Function	Page
Port 5	P5OUT	x'03F15'	R/W	Port 5 output register	IV-24
	P5IN	x'03F25'	R	Port 5 input register	IV-24
	P5DIR	x'03F35'	R/W	Port 5 direction control register	IV-24
	P5PLU	x'03F45'	R/W	Port 5 pull-up resistor control register	IV-24
	LCCTR	'x03FCC'	R/W	Segment output control register	IV-26,31,38,42
Port 6	P6OUT	x'03F16'	R/W	Port 6 output register	IV-30
	P6IN	x'03F26'	R	Port 6 input register	IV-30
	P6DIR	x'03F36'	R/W	Port 6 direction control register	IV-30
	P6PLU	x'03F46'	R/W	Port 6 pull-up resistor control register	IV-30
	LCCTR	x'03FCC'	R/W	Segment output control register	IV-26,31,38,42
Port 7	P7OUT	x'03F17'	R/W	Port 7 output register	IV-35
	P7IN	x'03F27'	R	Port 7 input register	IV-35
	P7DIR	x'03F37'	R/W	Port 7 direction control register	IV-35
	P7PLUD	x'03F47'	R/W	Port 7 pull-up / pull-down resistor control register	IV-35
	LCCTR	x'03FCC'	R/W	Segment output control register	IV-26,31,38,42
Port 8	P8OUT	x'03F18'	R/W	Port 8 output register	IV-41
	P8IN	x'03F28'	R	Port 8 input register	IV-41
	P8DIR	x'03F38'	R/W	Port 8 direction control register	IV-41
	P8PLU	x'03F48'	R/W	Port 8 pull-up resistor control register	IV-41
	LCCTR	x'03FCC'	R/W	Segment output control register	IV-26,31,38,42
Port A	PAIN	x'03F2A'	R	Port A input register	IV-45
	PAIMD	x'03F3A'	R/W	Port A input mode register	IV-45
	PAPLUD	x'03F4A'	R/W	Port A pull-up / pull-down resistor control register	IV-45
	P4IMD	x'03F3C'	R/W	Key interrupt control register	IV-47
Pin control	EXADV	x'03F0E'	R/W	Expansion address output control register	IV-25,36
	SYSMD	x'03F1F'	R/W	Synchronous output control register	IV-37
	FLOAT1	x'03F4B'	R/W	Pin control register 1	IV-37,46
	FLOAT2	x'03F4C'	R/W	Pin control register 2	IV-37
	LCCTR	x'03FCC'	R/W	Segment output control register	IV-26,31,38,42

R/W : Readable/Writable
R : Readable only

4-2 Port 0

4-2-1 Description

■General Port Setup

Each bit of the port 0 control I/O direction register (P0DIR) can be set individually to set pins as input or output. The control flag of the port 0 direction control register (P0DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 0 direction control register (P0DIR) to "0" and read the value of the port 0 input register (P0IN).

To output data to pin, set the control flag of the port 0 direction control register (P0DIR) to "1" and write the value of the port 0 output register (P0OUT).

Each pin can be set individually if pull-up resistor is added or not, by the port 0 pull-up resistor control register (P0PLU). Set the control flag of the port 0 pull-up resistor control register (P0PLU) to "1" to add pull-up resistor.
At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

■Special Function Pin Setup

P00 to P02 are used as I/O pin for serial interface 0, as well. P00 is output pin of the serial interface 0 transmission data, and UART transmission data. When the SC0SBOS flag of the serial interface 0 mode register 3 (SC0MD3) is "1", P00 is serial data output pin. P01 is the input pin of the serial interface 0 reception data, and UART reception data. When the SC0SBIS flag of the serial interface 0 mode register 3 (SC0MD3) is "1", P01 is serial data input pin. P02 is I/O pin of the serial interface 0 clock. When the SC0SBTS flag of serial interface 0 mode register 3 (SC0MD3) is "1", P02 is serial interface clock output pin.
P00 and P02 can be selected as either an push-pull output or Nch open-drain output by the SC0SBOM and the SC0SBTM of the serial interface 0 mode register 3 (SC0MD3).

[☞ Chapter 10 10-2. Control registers]

P03 to P05 are used as I/O pin for serial interface 1, as well. P03 is output pin of the serial interface 1 transmission data. When the SC1SBOS flag of the serial interface 1 mode register 1 (SC1MD1) is "1", P03 is serial data output pin. P04 is the serial interface 1 reception data input pin. When the SC1SBIS flag of the serial interface 1 mode register 1 (SC1MD1) is "1", P04 is serial data input pin. P05 is I/O pin of the serial interface 1 clock. When the SC1SBTS flag of serial interface 1 mode register 1 (SC1MD1) is "1", P05 is serial interface clock output pin.
P03 and P05 can be selected as either an push-pull output or Nch open-drain output by the SC1SBOM and the SC1SBTM of the serial interface 1 mode register 1 (SC1MD1).

[☞ Chapter 11 11-2. Control registers]

P06 is used as a buzzer output pin, as well. When the bp7 of the oscillation stabilization control register (DLYCTR) is "1", buzzer output is enabled. In memory expansion mode, data acknowledge mode input pin (NDK) is selected. In those mode, input mode is always selected.

4-2-2 Registers

	7	6	5	4	3	2	1	0	
P0OUT	-	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0	(At reset : - 0 0 0 0 0 0 0)

P0OUT	Output data
0	L(VSS level)
1	H(VDD level)

Port 0 output register (P0OUT : x'03F10', R/W)

	7	6	5	4	3	2	1	0	
P0IN	-	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0	(At reset : - X X X X X X X)

P0IN	Input data
0	Pin is low(VSS level).
1	Pin is high(VDD level).

Port 0 input register (P0IN : x'03F20', R)

	7	6	5	4	3	2	1	0	
P0DIR	-	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0	(At reset : - 0 0 0 0 0 0 0)

P0DIR	I/O mode selection
0	Input mode
1	Output mode

Port 0 direction control register (P0DIR : x'03F30', R/W)

	7	6	5	4	3	2	1	0	
P0PLU	-	P0PLU6	P0PLU5	P0PLU4	P0PLU3	P0PLU2	P0PLU1	P0PLU0	(At reset : - 0 0 0 0 0 0 0)

P0PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 0 pull-up resistor control register (P0PLU : x'03F40', R/W)

Figure 4-2-1 Port 0 Registers

4-2-3　Block Diagram

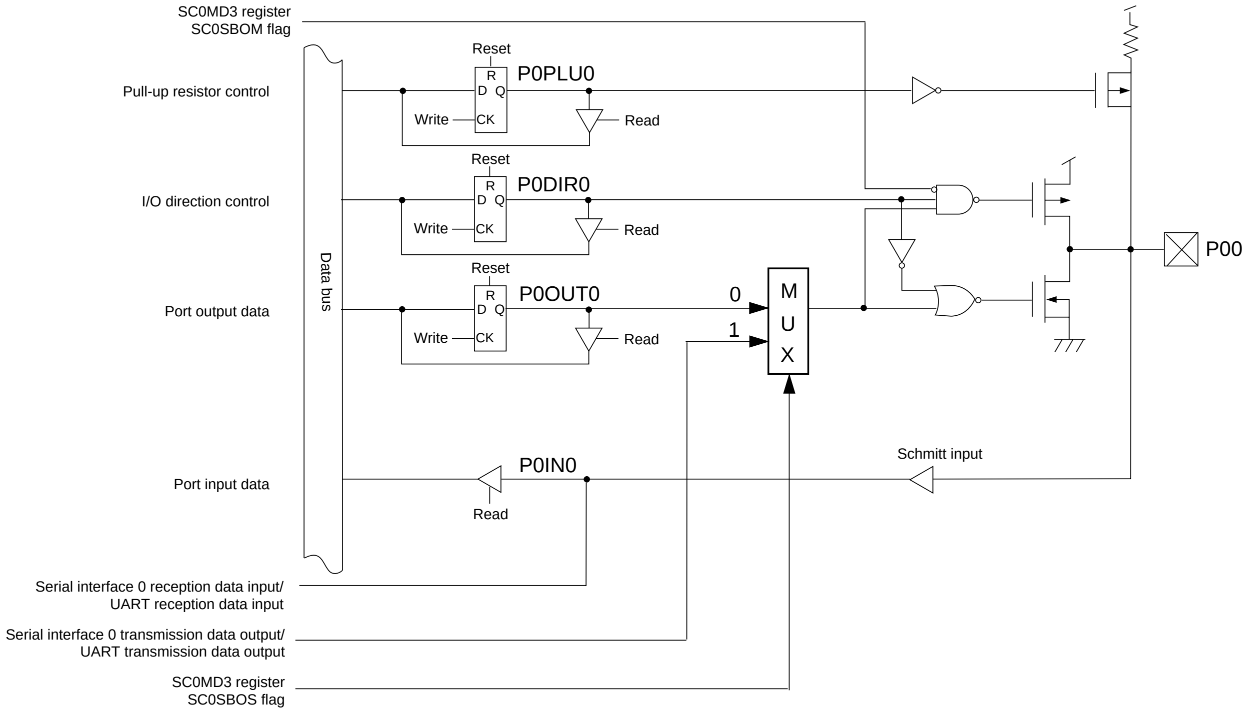


Figure 4-2-2　Block diagram (P00)

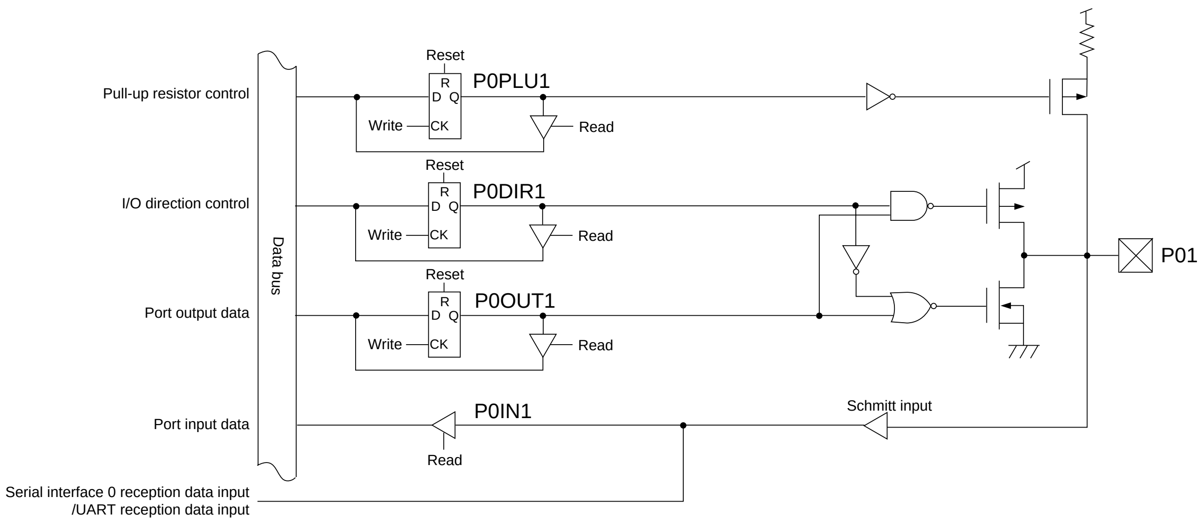


Figure 4-2-3　Block diagram (P01)

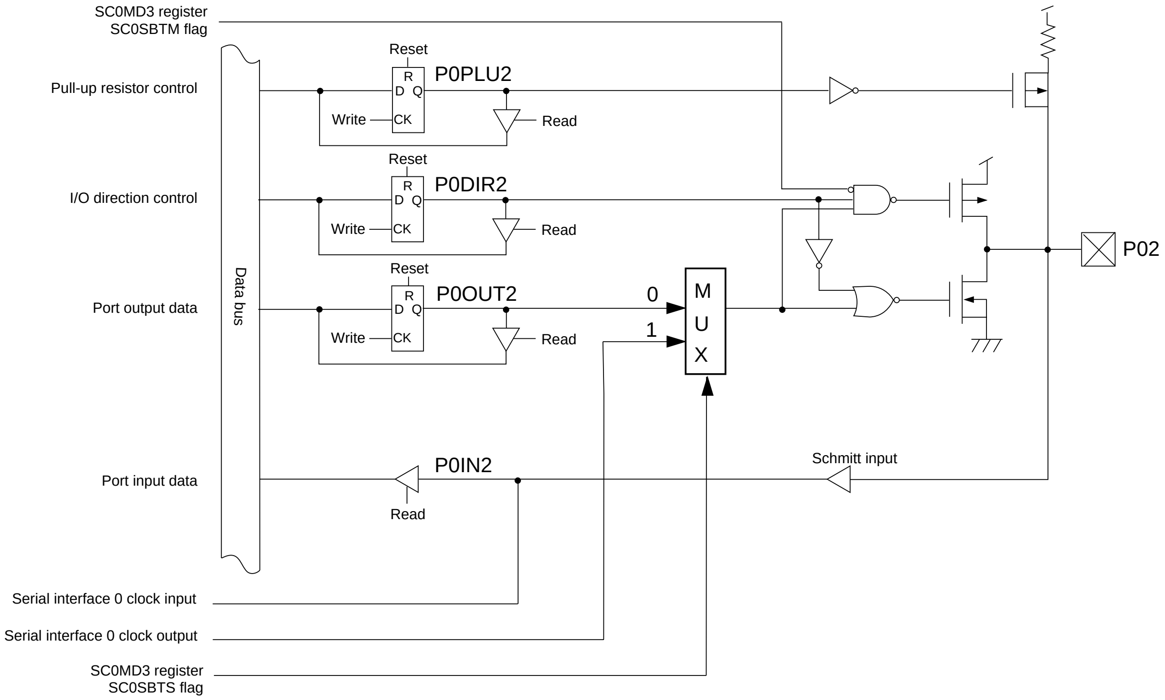


Figure 4-2-4 Block diagram (P02)

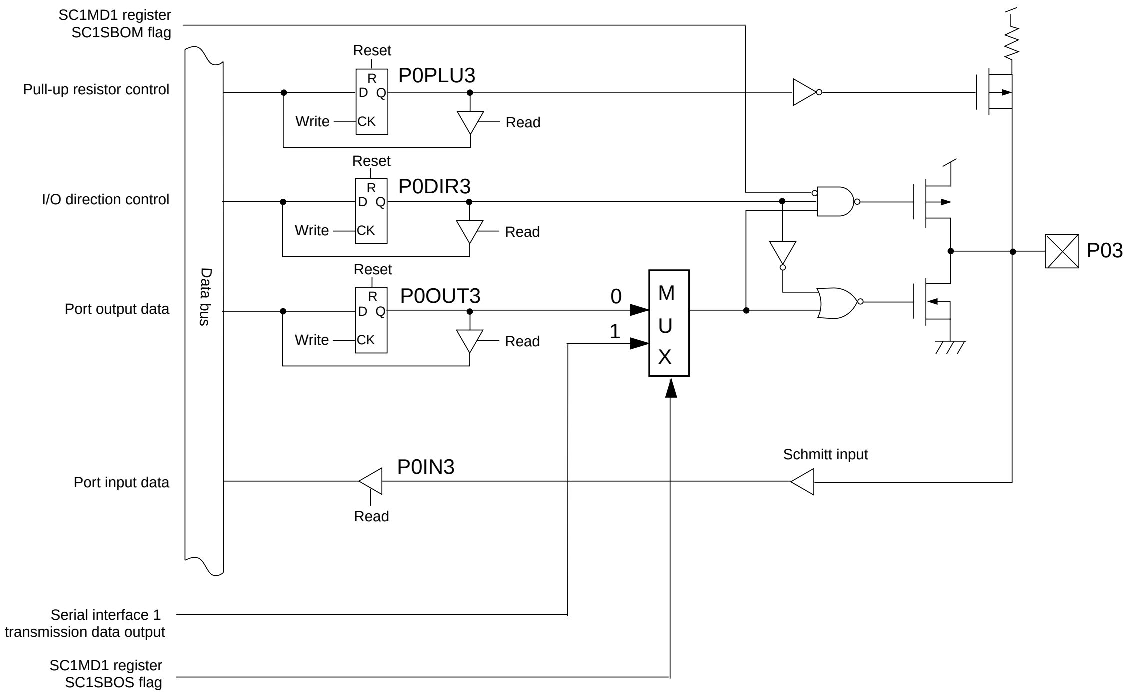


Figure 4-2-5 Block diagram (P03)

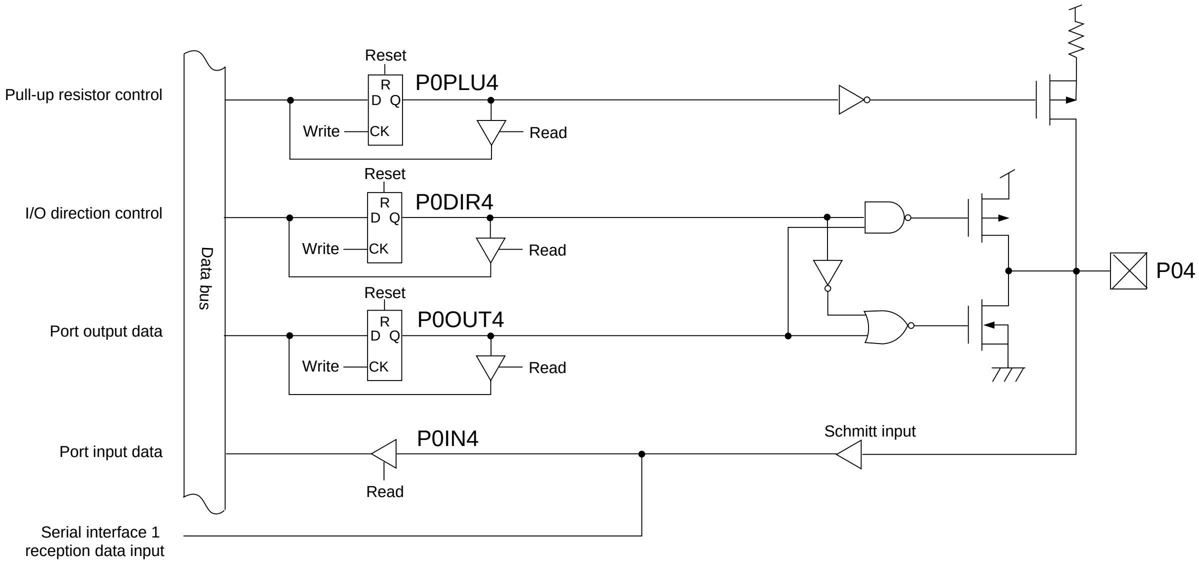


Figure 4-2-6 Block Diagram (P04)

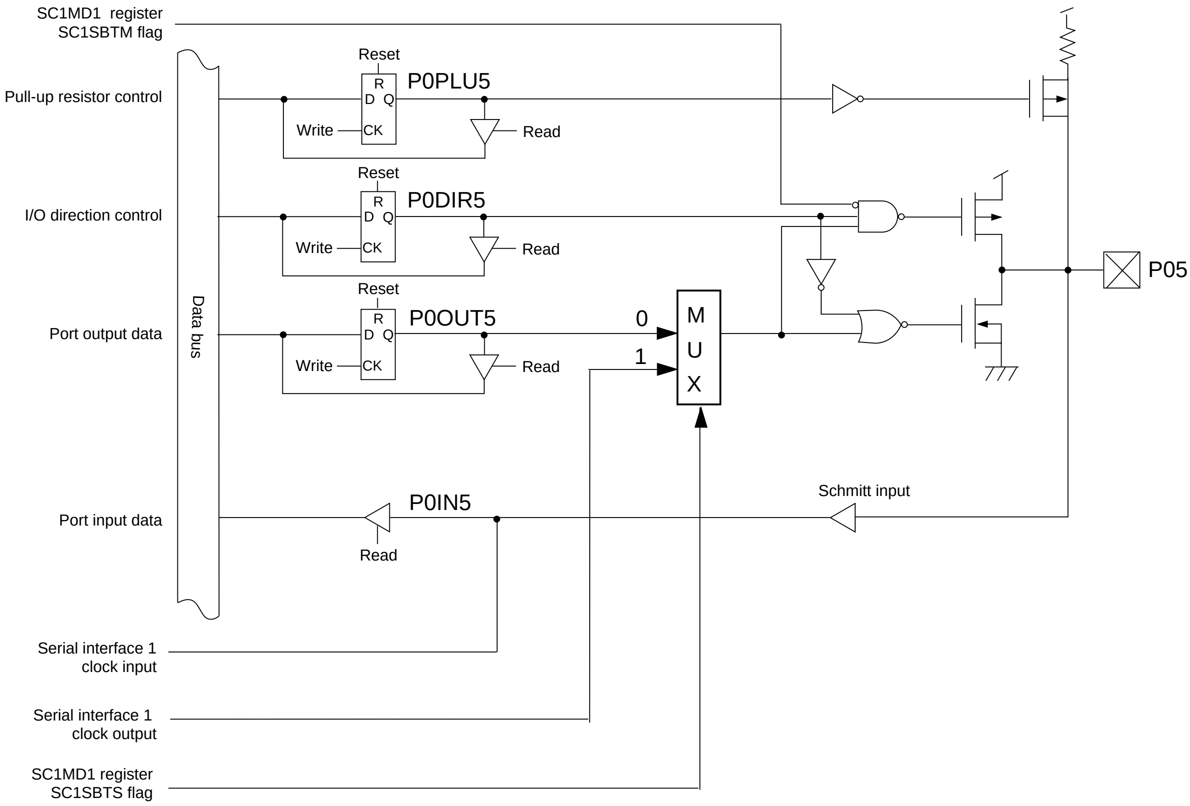


Figure 4-2-7 Block Diagram (P05)

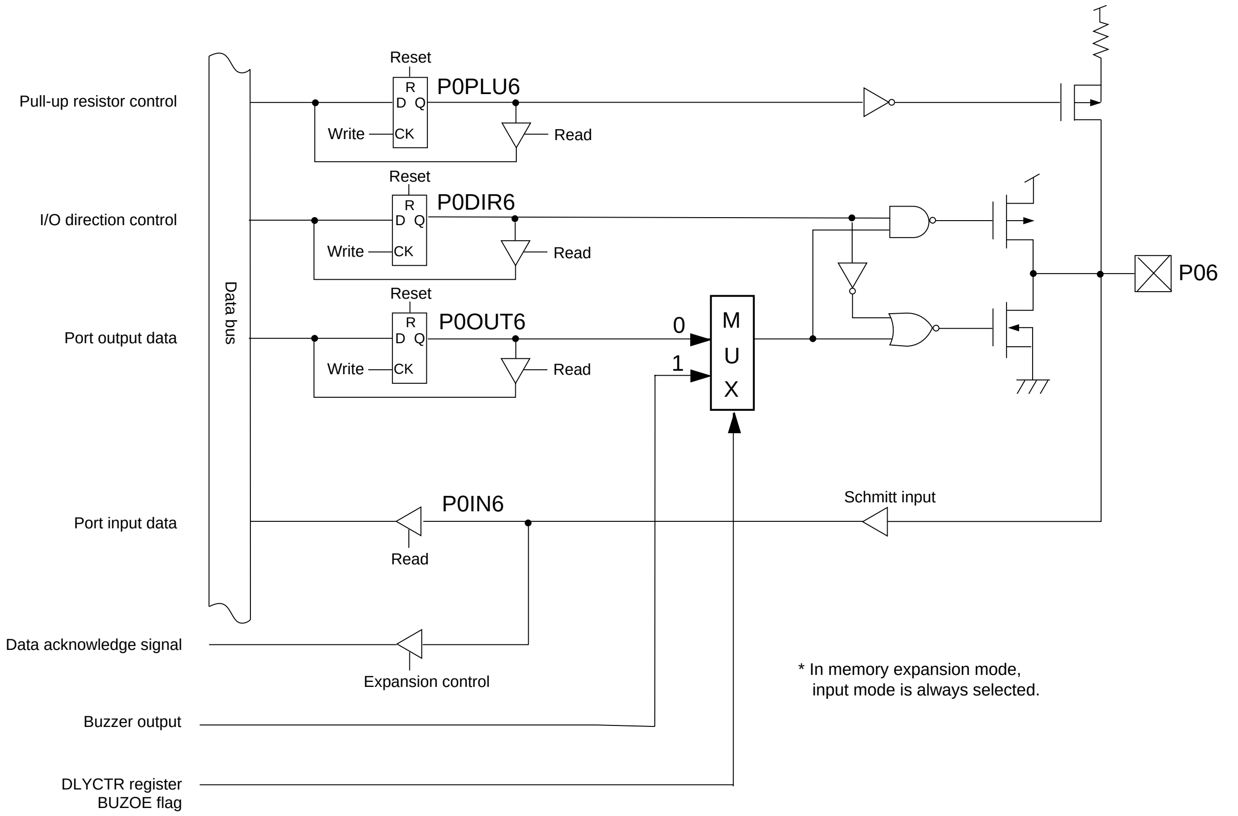


Figure 4-2-8 Block Diagram (P06)

In memory expansion mode, P06 pin is used for NDK pin even if the handshake mode is not used. So P06 cannot be used for general input pin or buzzer output.

4-3 Port 1

4-3-1 Description

■General Port Setup
Each bit of the port 1 control I/O direction register (P1DIR) can be set individually to set pins as input or output. The control flag of the port 1 direction control register (P1DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 1 direction control register (P1DIR) to "0" and read the value of the port 1 input register (P1IN).

To output data to pin, set the control flag of the port 1 direction control register (P1DIR) to "1" and write the value of the port 1 output register (P1OUT).

Each pin can be set individually if pull-up resistor is added or not, by the port 1 pull-up resistor control register (P1PLU). Set the control flag of the port 1 pull-up resistor control register (P1PLU) to "1" to add pull-up resistor.

At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

■Special Function Pin Setup
P12 to P14 are used as timer I/O pin, as well. P10 is used as remote control carrier output pin, as well. The port 1 output mode register (P1OMD) can select P10 and P12 to P14 output mode by each bit. When the port 1 output mode register (P1OMD) is "1", special function data is output, and when it is "0", they are used as general port.

4-3-2 Registers

	7	6	5	4	3	2	1	0	
P1OUT	-	-	-	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	(At reset : - - - 0 0 0 0 0)

P1OUT	Output data
0	Low (V_{SS} level)
1	High (V_{DD} level)

Port 1 output register (P1OUT : x'03F11', R/W)

	7	6	5	4	3	2	1	0	
P1IN	-	-	-	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	(At reset : - - - X X X X X)

P1IN	Input data
0	Pin is low(V_{SS} level).
1	Pin is high(V_{DD} level).

Port 1 input register (P1IN : x'03F21', R)

	7	6	5	4	3	2	1	0	
P1DIR	-	-	-	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	(At reset : - - - 0 0 0 0 0)

P1DIR	I/O mode selection
0	Input mode
1	Output mode

Port 1 direction control register (P1DIR : x'03F31', R/W)

	7	6	5	4	3	2	1	0	
P1PLU	-	-	-	P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0	(At reset : - - - 0 0 0 0 0)

P1PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 1 pull-up resistor control register (P1PLU : x'03F41', R/W)

Figure 4-3-1 Port 1 Registers (1/2)

	7	6	5	4	3	2	1	0	
P1OMD	—	—	—	P14TCO	P13TCO	P12TCO	—	P10TCO	(At reset : - - - 0 0 0 - 0)

P10TCO	I/O port, timer 0 output selection
0	I/O port
1	Timer 0 output

P12TCO	I/O port, timer 2 output selection
0	I/O port
1	Timer 2 output

P13TCO	I/O port, timer 3 output selection
0	I/O port
1	Timer 3 output

P14TCO	I/O port, timer 4 output selection
0	I/O port
1	Timer 4 output

Port 1 output mode register (P1OMD : x'03F39', R/W)

Figure 4-3-2   Port 1 Registers (2/2)

4-3-3 Block Diagram

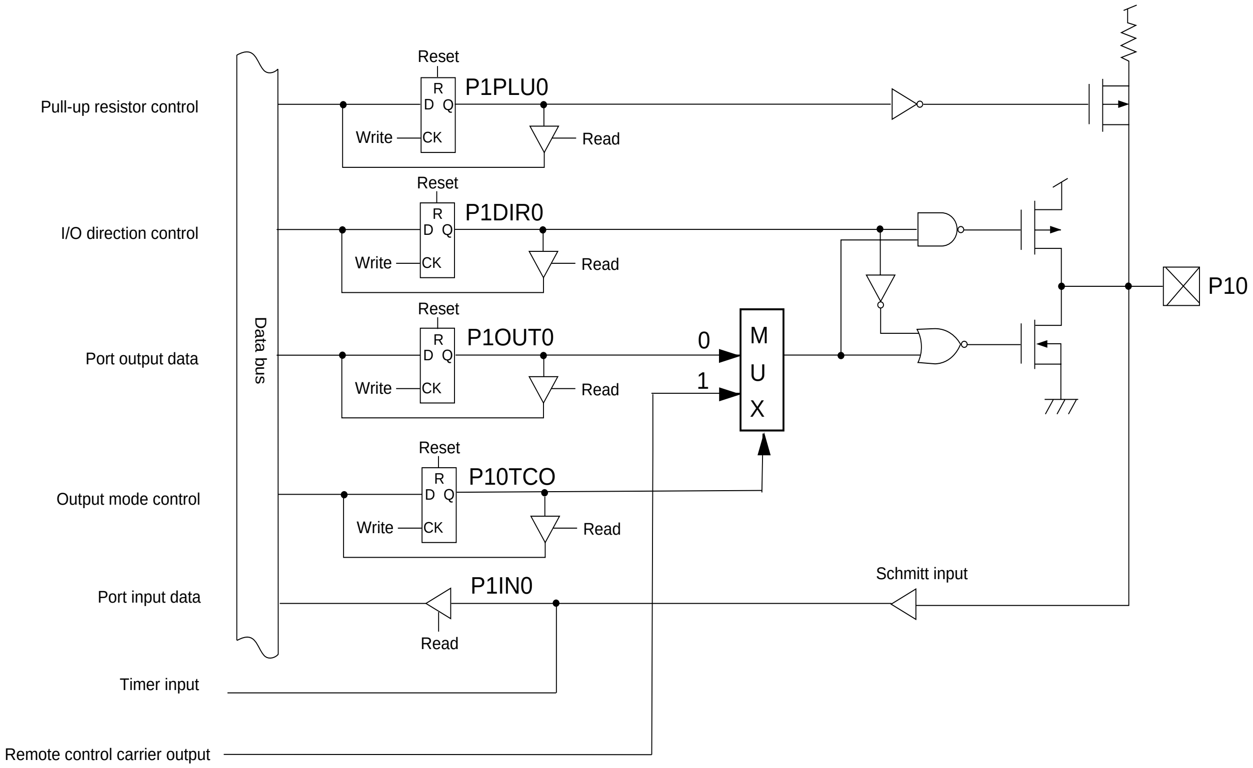


Figure 4-3-3 Block Diagram (P10)

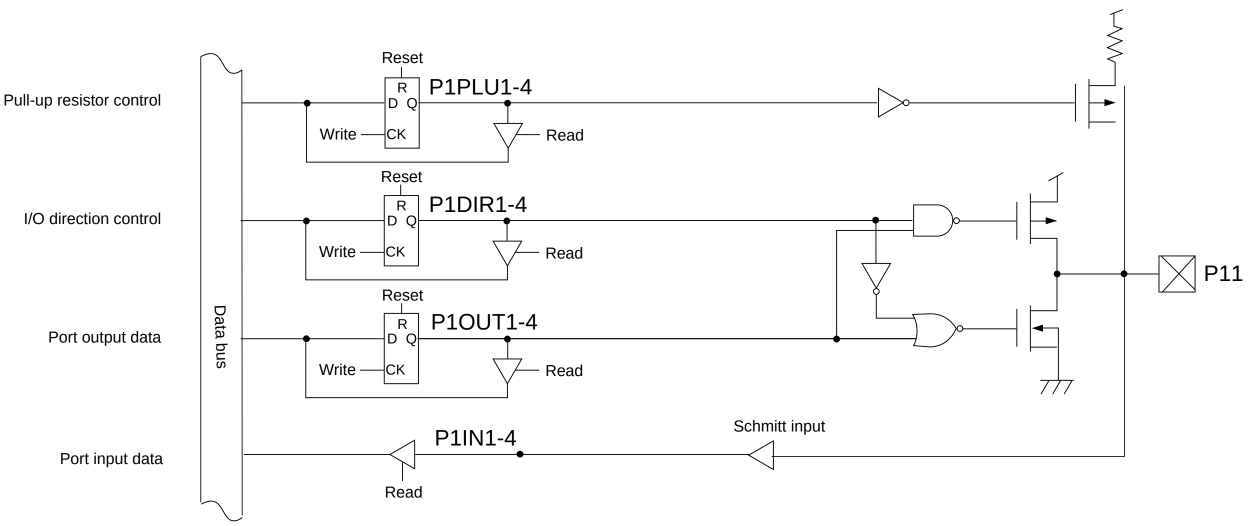


Figure 4-3-4 Block Diagram (P11)

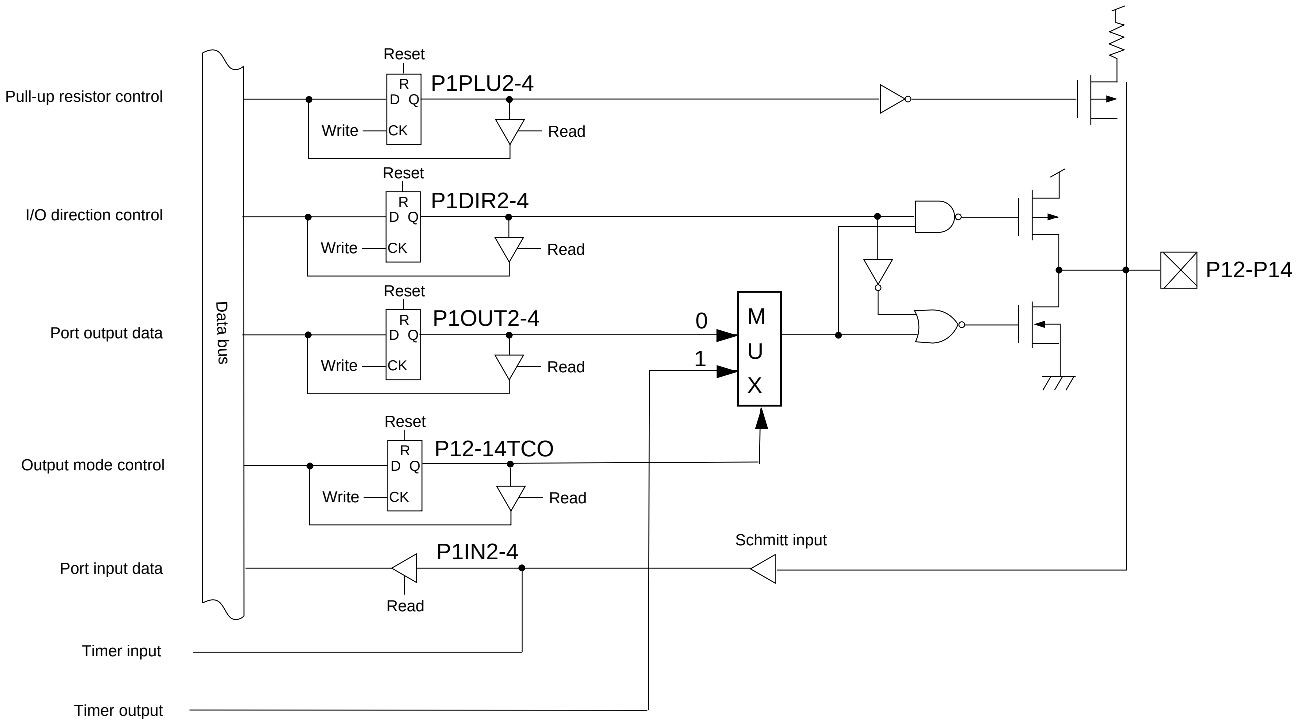


Figure 4-3-5   Block Diagram (P12 to P14)

4-4 Port 2

4-4-1 Description

■General Port Setup
Port 2 is input port, except P27. To read input data of pin, read out the value of the port 2 input register (P2IN).

P27 is reset pin. When the software is reset, write the bp7 of the port 2 output register (P2OUT) to "0".

The port 2 pull-up resistor control register (P2PLU) can select if port 2 is added pull-up resistor or not, by each bit. When the control flag of the port 2 pull-up resistor control register (P2PLU) is set to "1", pull-up resistor is added. P27 is always added pull-up resistor.

■Special Function Pin Setup
P20 to P24 are used as external interrupt pins, as well.

P21 is used as an input pin for external interrupt and AC zero-cross. To read data of AC zero-cross, set the bp2 of the pin control register (FLOAT1) to "1" and read the value of the port 2 input register (P2IN).

4-4-2 Registers

	7	6	5	4	3	2	1	0
P2OUT	P2OUT7	—	—	—	—	—	—	—

(At reset : 1 - - - - - - -)

P2OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 2 output register(P2OUT : x'03F12', R/W)

	7	6	5	4	3	2	1	0
P2IN	—	—	—	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0

(At reset : - - - X X X X X)

P2IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 2 input register (P2IN : x'03F22', R)

	7	6	5	4	3	2	1	0
P2PLU	—	—	—	P2PLU4	P2PLU3	P2PLU2	P2PLU1	P2PLU0

(At reset : - - - 0 0 0 0 0)

P2PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 2 pull-up resistor control register(P2PLU : x'03F42', R/W)

Figure 4-4-1 Port 2 Registers

4-4-3 Block Diagram

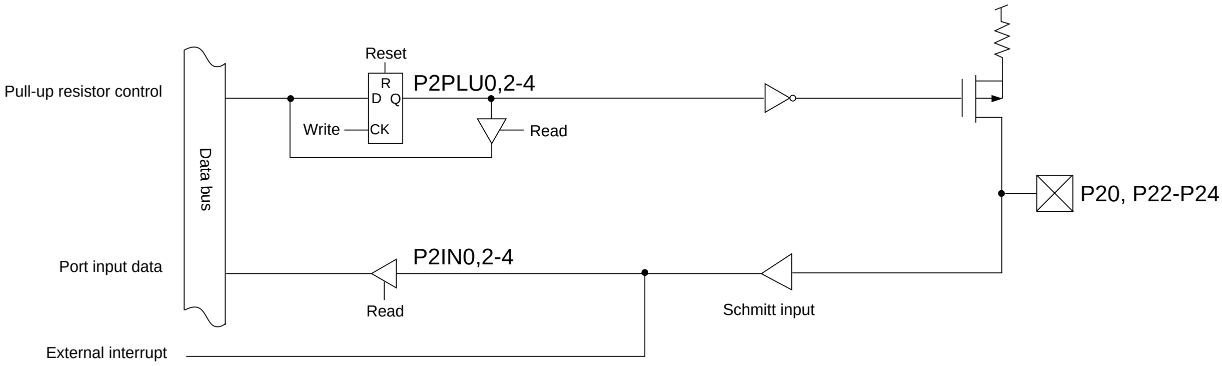


Figure 4-4-2 Block Diagram (P20, P22 to P24)

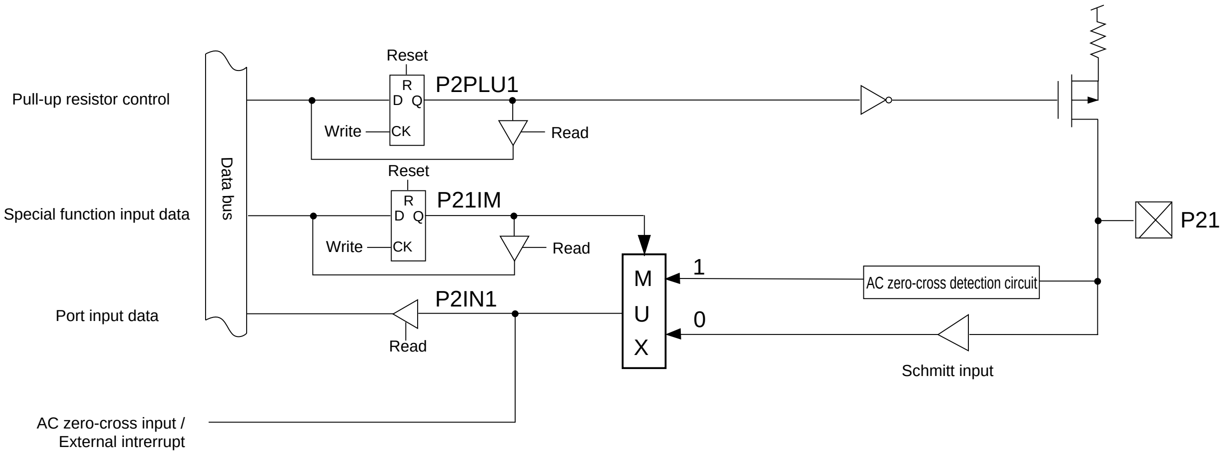


Figure 4-4-3 Block Diagram (P21)

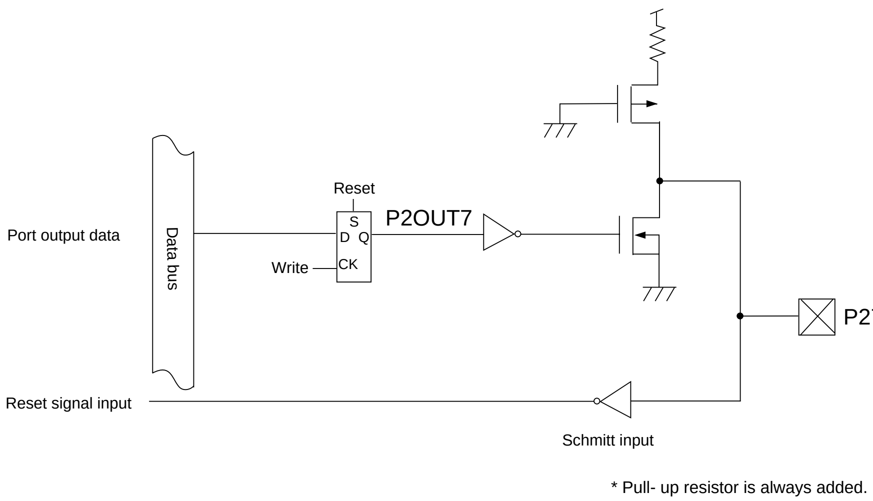


Figure 4-4-4 Block Diagram (P27)

4-5 Port 3

4-5-1 Description

■General Port Setup
Each bit of the port 3 control I/O direction register (P3DIR) can be set individually to set pins as input or output. The control flag of the port 3 direction control register (P3DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 3 direction control register (P3DIR) to "0" and read the value of the port 3 input register (P3IN).

To output data to pin, set the control flag of the port 3 direction control register (P3DIR) to "1" and write the value of the port 3 output register (P3OUT).

Each pin can be set individually if pull-up resistor is added or not, by the port 3 pull-up resistor control register (P3PLU). Set the control flag of the port 3 pull-up resistor control register (P3PLU) to "1" to add pull-up resistor.
At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

4-5-2 Registers

	7	6	5	4	3	2	1	0
P3OUT	—	—	—	—	—	P3OUT2	P3OUT1	P3OUT0

(At reset : - - - - - 0 0 0)

P3OUT	Output data
0	L(V_{SS} level)
1	H(V_{DD} level)

Port 3 output register (P3OUT : x'03F13', R/W)

	7	6	5	4	3	2	1	0
P3IN	—	—	—	—	—	P3IN2	P3IN1	P3IN0

(At reset : - - - - - X X X)

P3IN	Input data
0	Pin is low(V_{SS} level).
1	Pin is high(V_{DD} level).

Port 3 input register (P3IN : x'03F23', R)

	7	6	5	4	3	2	1	0
P3DIR	—	—	—	—	—	P3DIR2	P3DIR1	P3DIR0

(At reset : - - - - - 0 0 0)

P3DIR	I/O mode selection
0	Input mode
1	Output mode

Port 3 direction control register (P3DIR : x'03F33', R/W)

	7	6	5	4	3	2	1	0
P3PLU	—	—	—	—	—	P3PLU2	P3PLU1	P3PLU0

(At reset : - - - - - 0 0 0)

P3PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 3 pull-up resistor control register (P3PLU : x'03F43', R/W)

Figure 4-5-1 Port 3 Registers

4-5-3 Block Diagram

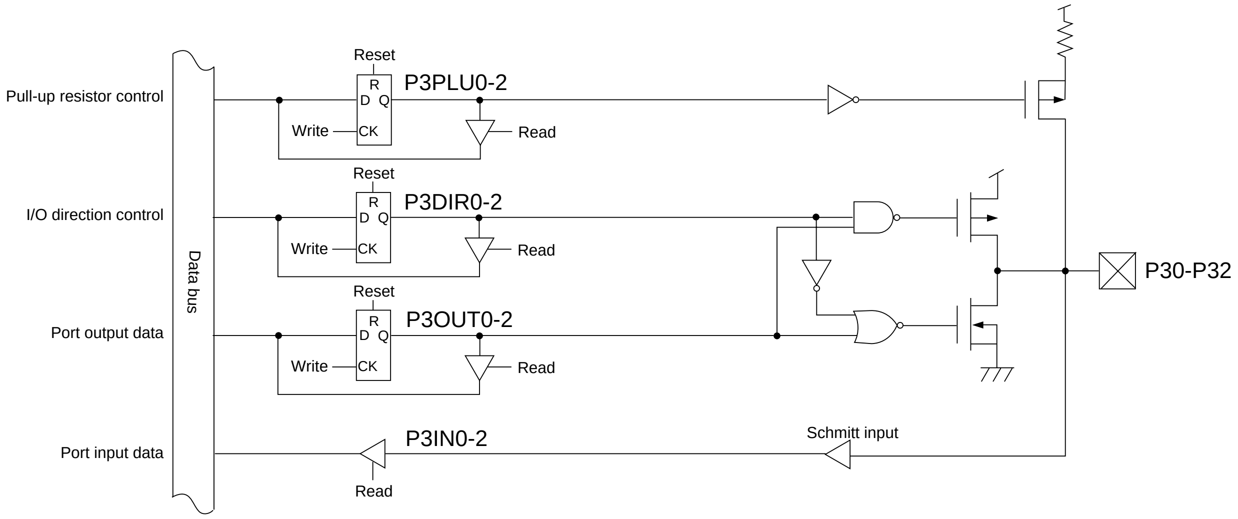


Figure 4-5-2 Block diagram (P30, P31, P32)

4-6 Port 5

4-6-1 Description

■General Port Setup
Each bit of the port 5 control I/O direction register (P5DIR) can be set individually to set pins as input or output. The control flag of the port 5 direction control register (P5DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 5 direction control register (P5DIR) to "0" and read the value of the port 5 input register (P5IN).

To output data to pin, set the control flag of the port 5 direction control register (P5DIR) to "1" and write the value of the port 5 output register (P5OUT).

Each pin can be set individually if pull-up resistor is added or not, by the port 5 pull-up resistor control register (P5PLU). Set the control flag of the port 5 pull-up resistor control register (P5PLU) to "1" to add pull-up resistor.

At reset, the P50 to P54 input mode is selected and pull-up resistors are disabled (high impedance output).

■Special Function Pin Setup
P50 to P54 are used as LED driving pins, as well.

P53 and P54 are used as LCD driving pins (segment output), as well. The bp0 of the segment output control register (LCCTR) set if they are used as segment output pins or general I/O pins.

In memory expansion mode, P50 to P52 are output pins for control signal to the expansion memory. In this mode, output mode is always selected.

In memory expansion mode, P53 and P54 are output pins for address to the expansion memory. But the bp7 of the address output control register (EXADV) set if they are used as address output pins or general I/O pins.

Table 4-6-1 Expansion Pins (P50 to P54)

Pins	In memory expansion mode *
P50	NWE
P51	NRE
P52	NCS
P53	A16 (External memory address bp16)
P54	A17 (External memory address bp17)

* In memory expansion mode, the bp7 of the EXADV register should be set to "1" for P53, 54 output address.

4-6-2 Registers

	7	6	5	4	3	2	1	0	
P5OUT	—	—	—	P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0	(At reset : - - - 0 0 0 0 0)

P5OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 5 output register (P5OUT : x'03F15', R/W)

	7	6	5	4	3	2	1	0	
P5IN	—	—	—	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0	(At reset : - - - X X X X X)

P5IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 5 input register (P5IN : x'03F25', R)

	7	6	5	4	3	2	1	0	
P5DIR	—	—	—	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0	(At reset : - - - 0 0 0 0 0)

P5DIR	I/O mode selection
0	Input mode
1	Output mode

Port 5 direction control register (P5DIR : x'03F35', R/W)

	7	6	5	4	3	2	1	0	
P5PLU	—	—	—	P5PLU4	P5PLU3	P5PLU2	P5PLU1	P5PLU0	(At reset : - - - 0 0 0 0 0)

P5PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 5 pull-up resistor control register (P5PLU : x'03F45', R/W)

Figure 4-6-1 Port 5 Registers (1/3)

	7	6	5	4	3	2	1	0
EXADV	EXADV3	EXADV2	EXADV1	-	-	-	-	-

(At reset : 0 0 0 - - - - -)

EXADV1	P73 - P70 "A11 - A8" address output during memory expansion mode.
0	General port
1	"A11 to A8" address output

EXADV2	P77 - P74 "A15 - A12" address output during memory expansion mode.
0	General port
1	"A15 to A12" address output

EXADV3	P54, P53 "A17, 16" address output during memory expansion mode.
0	General port
1	"A17, 16" address output

Expansion address output control register (EXADV: x'03F0E', R/W)

Figure 4-6-2 Port 5 Registers (2/3)

In memory expansion mode, unused address pin can be used as general port.

	7	6	5	4	3	2	1	0	
LCCTR	—	SEGSEL6	SEGSEL5	SEGSEL4	SEGSEL3	SEGSEL2	SEGSEL1	SEGSEL0	(At reset : - 0 0 0 0 0 0 0)

SEGSEL0	SEG51 to 50 Port (P53 to P54) selection
0	Port (P53 to P54)
1	SEG51 to 50

SEGSEL1	SEG49 to 46 Port (P60 to P63) selection
0	Port (P60 to P63)
1	SEG49 to 46

SEGSEL2	SEG45 to 42 Port (P64 to P67) selection
0	Port (P64 to P67)
1	SEG45 to 42

SEGSEL3	SEG41 to 38 Port (P70 to P73) selection
0	Port (P70 to P73)
1	SEG41 to 38

SEGSEL4	SEG37 to 34 Port (P74 to P77) selection
0	Port (P74 to P77)
1	SEG37 to 34

SEGSEL5	SEG30 to 33 Port (P84 to P87) selection
0	Port (P84 to P67)
1	SEG30 to 33

SEGSEL6	SEG26 to 29 Port (P80 to P83) selection
0	Port (P80 to P83)
1	SEG26 to 29

Segment output control register (LCCTR : x'03FCC', R/W)

Figure 4-6-3 Port 5 Registers (3/3)

4-6-3 Block Diagram

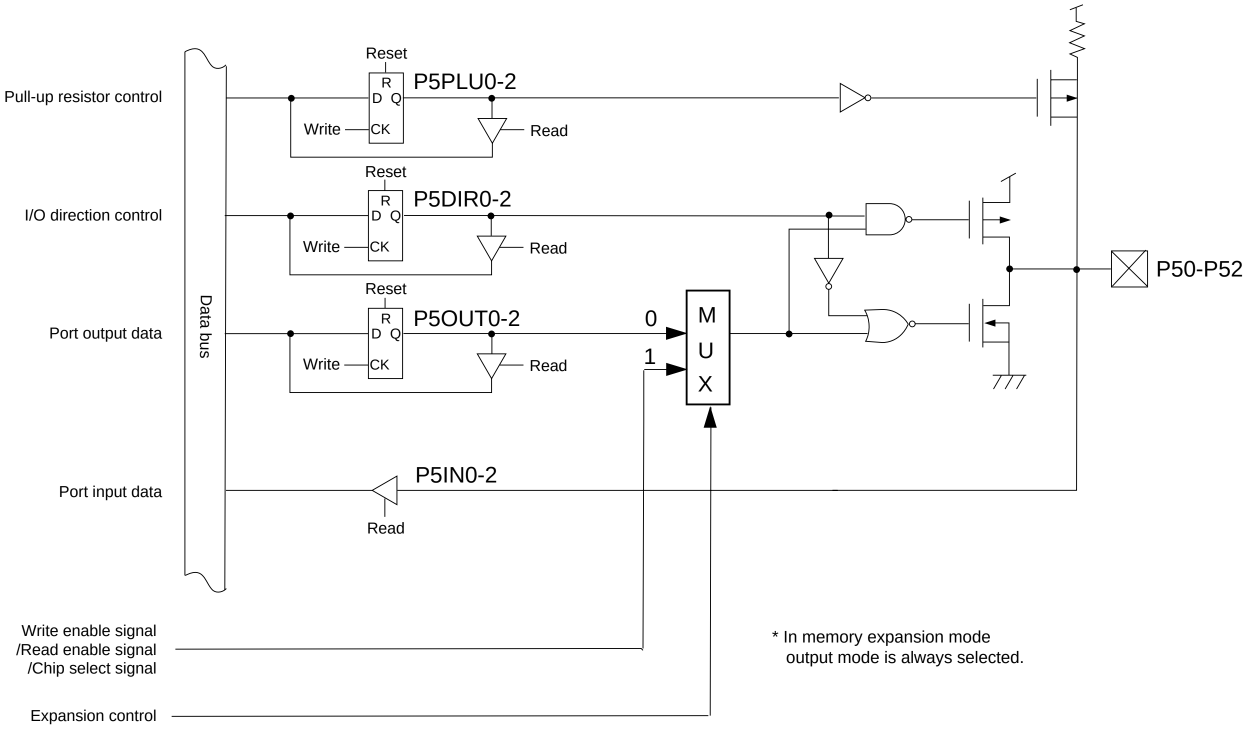
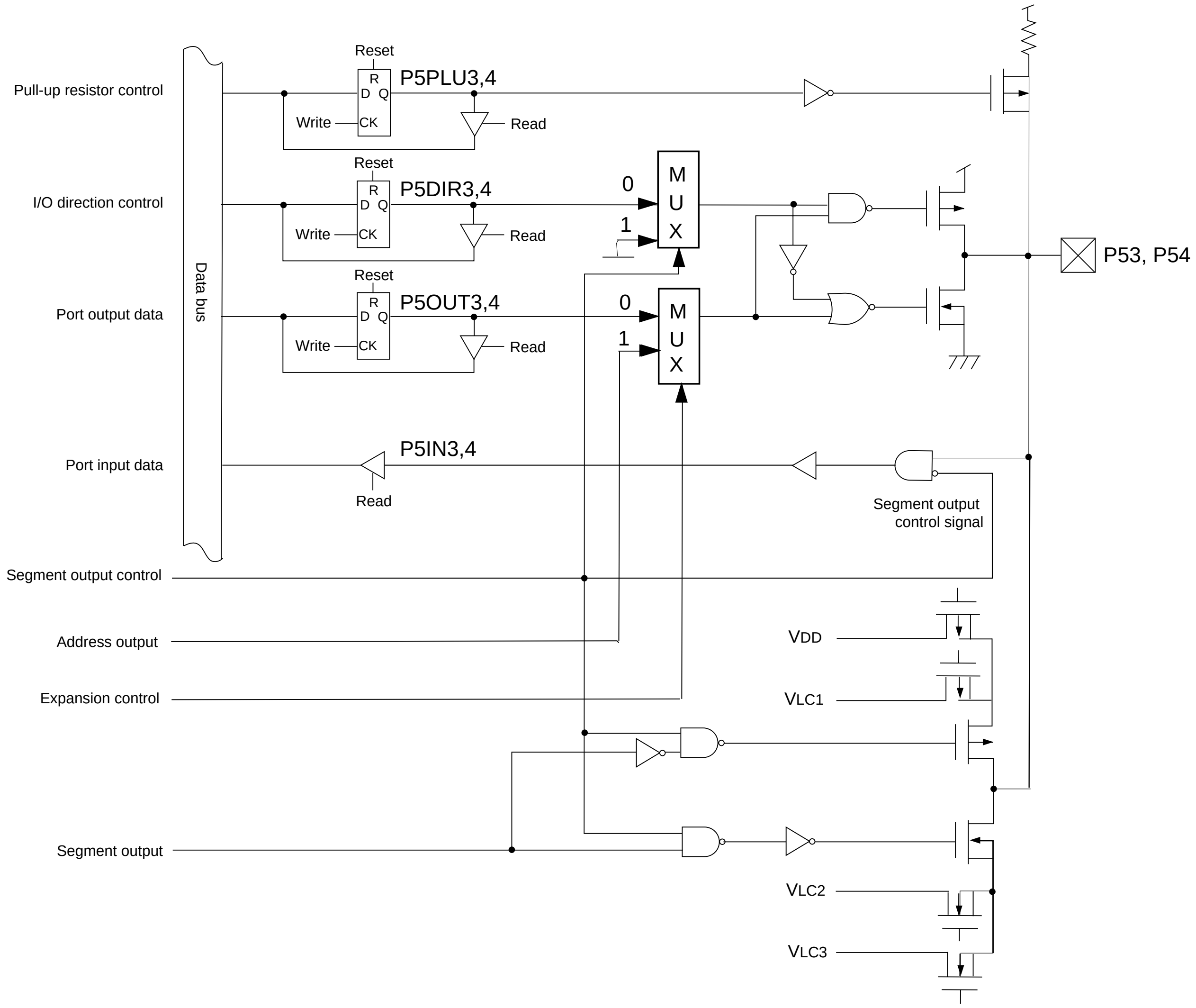


Figure 4-6-4 Block Diagram (P50 to P52)



* When segment output is selected, segment output control automatically sets port I/O direction control to input mode, and segment output control is set to "without pull-up resistors".

* In memory expansion mode, set the bp7 of the EXADV register to be used as general I/O pin, or as address output pin.

Figure 4-6-5 Block Diagram (P53, P54)

4-7 Port 6

4-7-1 Description

■General port Setup
Each bit of the port 6 control I/O direction register (P6DIR) can be set individually to set pins as input or output. The control flag of the port 6 direction control register (P6DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 6 direction control register (P6DIR) to "0" and read the value of the port 6 input register (P6IN).

To output data to pin, set the control flag of the port 6 direction control register (P6DIR) to "1" and write the value of the port 6 output register (P6OUT).

Each pin can be set individually if pull-up resistor is added or not, by the port 6 pull-up resistor control register (P6PLU). Set the control flag of the port 6 pull-up resistor control register (P6PLU) to "1" to add pull-up resistor.

At reset, the P60 to P67 input mode is selected and pull-up resistors are disabled (high impedance output).

■Special Function Pin Setup
P60 to P67 are used as LCD driving pins (segment output), as well. The bp1 and 2 of the segment output control register (LCCTR) set if they are used as segment output pins or general I/O pins.

In memory expansion mode, P60 to P67 are output pins to the expansion memory. In this mode, any register cannot control input or output. Only at access to the expansion memory, address is output, and during other period (at NCS = "H") it is high impedance state (input mode).

Table 4-7-1 Expansion Pins (P60 to P67)

Pins	In memory expansion mode
P60	A0 (External memory address bp0)
P61	A1 (External memory address bp1)
P62	A2 (External memory address bp2)
P63	A3 (External memory address bp3)
P64	A4 (External memory address bp4)
P65	A5 (External memory address bp5)
P66	A6 (External memory address bp6)
P67	A7 (External memory address bp7)

4-7-2 Registers

	7	6	5	4	3	2	1	0	
P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	(At reset : 0 0 0 0 0 0 0 0)

P6OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 6 output register (P6OUT : x'03F16', R/W)

	7	6	5	4	3	2	1	0	
P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	(At reset : X X X X X X X X)

P6IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 6 intput register (P6IN : x'03F26', R)

	7	6	5	4	3	2	1	0	
P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	(At reset : 0 0 0 0 0 0 0 0)

P6DIR	I/O mode selection
0	Input mode
1	Output mode

Port 6 direction control register (P6DIR : x'03F36', R/W)

	7	6	5	4	3	2	1	0	
P6PLU	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0	(At reset : 0 0 0 0 0 0 0 0)

P6PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 6 pull-up resistor control register (P6PLU : x'03F46', R/W)

Figure 4-7-1 Port 6 Registers (1/2)

	7	6	5	4	3	2	1	0	
LCCTR	—	SEGSEL6	SEGSEL5	SEGSEL4	SEGSEL3	SEGSEL2	SEGSEL1	SEGSEL0	(At reset : - 0 0 0 0 0 0 0)

SEGSEL0	SEG51 to 50 Port (P53 to P54) selection
0	Port (P53 to P54)
1	SEG51 to 50

SEGSEL1	SEG49 to 46 Port (P60 to P63) selection
0	Port (P60 to P63)
1	SEG49 to 46

SEGSEL2	SEG45 to 42 Port (P64 to P67) selection
0	Port (P64 to P67)
1	SEG45 to 42

SEGSEL3	SEG41 to 38 Port (P70 to P73) selection
0	Port (P70 to P73)
1	SEG41 to 38

SEGSEL4	SEG37 to 34 Port (P74 to P77) selection
0	Port (P74 to P77)
1	SEG37 to 34

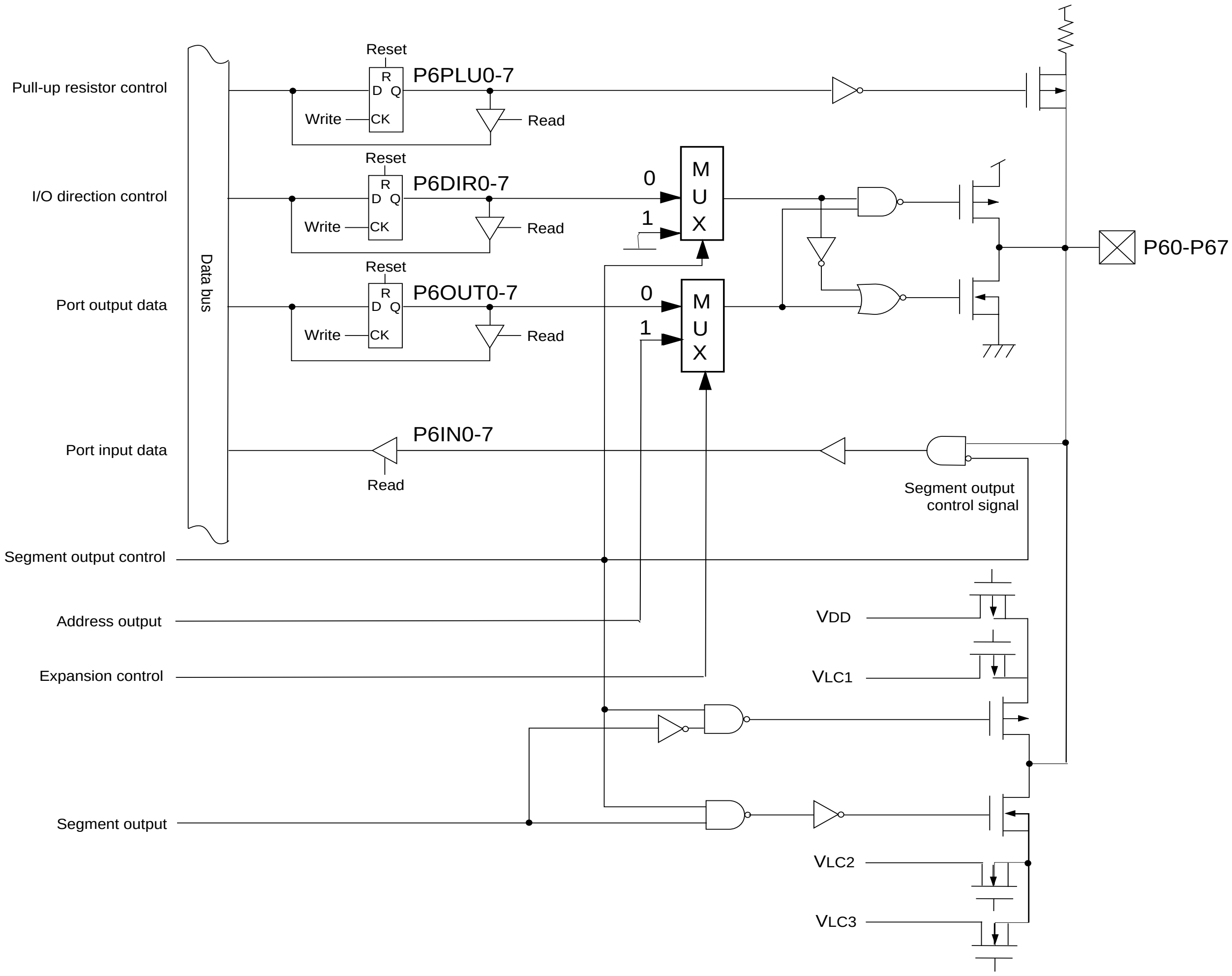
SEGSEL5	SEG30 to 33 Port (P84 to P87) selection
0	Port (P84 to P67)
1	SEG30 to 33

SEGSEL6	SEG26 to 29 Port (P80 to P83) selection
0	Port (P80 to P83)
1	SEG26 to 29

Segment output control register (LCCTR : x'03FCC', R/W)

Figure 4-7-2 Port 6 Registers (2/2)

4-7-3 Block Diagram



* When segment output is selected, segment output control automatically sets port I/O direction control to input mode, and segment output control is set to "without pull-up resistors".

* In memory expansion mode, output mode is always selected.

Figure 4-7-3 Block Diagram (P60 to P67)

4-8 Port 7

4-8-1 Description

■General Port Setup

Each bit of the port 7 control I/O direction register (P7DIR) can be set individually to set pins as input or output. The control flag of the port 7 direction control register (P7DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 7 direction control register (P7DIR) to "0" and read the value of the port 7 input register (P7IN).

To output data to pin, set the control flag of the port 7 direction control register (P7DIR) to "1" and write the value of the port 7 output register (P7OUT).

Each pin can be set individually if pull-up / pull-down resistor is added or not, by the port 7 pull-up / pull-down resistor control register (P7PLUD). But pull-up / pull-down cannot be mixed. Set the control flag of the port 7 pull-up / pull-down resistor control register (P7PLUD) to "1" to add pull-up or pull-down resistor. The pin control register 1 (FLOAT1) select if pull-up resistor or pull-down resistor is added. The bp0 of the pin control register 1 (FLOAT1) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

At reset, the P70 to P77 input mode is selected and pull-up resistors are disabled (high impedance output).

■Special Function Pin Setup

The synchronous output control register (SYSMD) selects the synchronous output pin of the port 7, in each bit. When the SYSMD is "1", it can be used for synchronous output, and when it is "0", it can be used for general port. The synchronous output event is selected by the pin control register 2 (FLOAT2). When the bp1, bp0 of the FLOAT2 are "00", the external interrupt 2 (IRQ2) is selected, and "01" for the timer 4 interrupt, and "10" for the timer 2 interrupt.

[☞ Chapter 4 4-11. Synchronous output p.IV-49]

P70 to P77 are used as LCD driving pins (segment output), as well. The bp3 and 4 of the segment output control register (LCCTR) set if they are used as segment output pins or general I/O pins.

In memory expansion mode, P70 to P77 are output pins to the expansion memory. But in memory expansion mode, the bp5 or bp6 of the address output control register (EXADV) set if they are used as address output pins or general I/O pins.

Table 4-8-1 Expansion Pins (P70 to P77)

Pins	In memory expansion mode *
P70	A8 (External memory address bp8)
P71	A9 (External memory address bp9)
P72	A10 (External memory address bp10)
P73	A11 (External memory address bp11)
P74	A12 (External memory address bp12)
P75	A13 (External memory address bp13)
P76	A14 (External memory address bp14)
P77	A15 (External memory address bp15)

* In memory expansion mode, the bp5, 6 of the EXADV register should be set to "1" for P70 to P77 output address.

4-8-2 Registers

	7	6	5	4	3	2	1	0
P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0

(At reset : 0 0 0 0 0 0 0 0)

P7OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 7 output register (P7OUT : x'03F17', R/W)

	7	6	5	4	3	2	1	0
P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0

(At reset : X X X X X X X X)

P7IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 7 input register (P7IN : x'03F27', R)

	7	6	5	4	3	2	1	0
P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0

(At reset : 0 0 0 0 0 0 0 0)

P7DIR	I/O mode selection
0	Input mode
1	Output mode

Port 7 direction control register (P7DIR : x'03F37', R/W)

	7	6	5	4	3	2	1	0
P7PLUD	P7PLUD7	P7PLUD6	P7PLUD5	P7PLUD4	P7PLUD3	P7PLUD2	P7PLUD1	P7PLUD0

(At reset : 0 0 0 0 0 0 0 0)

P7PLUD	Pull-up (or Pull-down) resistor selection
0	No pull-up (or pull-down) resistor
1	Pull-up (or Pull-down) resistor

Port 7 pull-up / pull-down resistor control register (P7PLUD : x'03F47', R/W)

Figure 4-8-1 Port 7 Registers (1/4)

	7	6	5	4	3	2	1	0
EXADV	EXADV3	EXADV2	EXADV1	-	-	-	-	-

(At reset : 0 0 0 - - - - -)

EXADV1	P73 - P70 "A11 - A8" address output during memory expansion mode.
0	General port
1	"A11 to A8" address output

EXADV2	P77 - P74 "A15 - A12" address output during memory expansion mode.
0	General port
1	"A15 to A12" address output

EXADV3	P54, P53 "A17, 16" address output during memory expansion mode.
0	General port
1	"A17, 16" address output

Expansion address output control register (EXADV: x'03F0E', R/W)

Figure 4-8-2 Port 7 Registers (2/4)

In memory expansion mode, unused address pin can be used as general port.

	7	6	5	4	3	2	1	0	
FLOAT1	—	—	—	—	—	P21IM	PARDWN	P7RDWN	(At reset : - - - - - 0 0 0)

P7RDWN	Port 7 pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

PARDWN	Port A pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

P21IM	P21 input mode selection
0	Schmitt trigger input
1	ACZ input

Pin control register 1 (FLOAT1 : X'03F4B', R/W)

	7	6	5	4	3	2	1	0	
FLOAT2	—	—	—	—	—	—	P7SYEVS1	P7SYEVS0	(At reset : - - - - - - 0 0)

P7SYEVS1	P7SYEVS0	Port 7 synchronous output event selection
0	0	External interrupt 2 (IRQ2)
0	1	Timer 4 interrupt
1	0	Timer 2 interrupt
1	1	Timer 1 interrupt

Pin control register 2 (FLOAT2 : x'03F4C', R/W)

	7	6	5	4	3	2	1	0	
SYSMD	SYSMD7	SYSMD6	SYSMD5	SYSMD4	SYSMD3	SYSMD2	SYSMD1	SYSMD0	(At reset : 0 0 0 0 0 0 0 0)

SYSMD	Synchronous output control selection
0	Use as I/O pin
1	Use as synchronous output pin

Synchronous output control register (SYSMD : X'03F1F', R/W)

Figure 4-8-3 Port 7 Registers (3/4)

! Set the bp1-0of the pin control register 2 (FLOAT2) to the value except "11".

	7	6	5	4	3	2	1	0	
LCCTR	—	SEGSEL6	SEGSEL5	SEGSEL4	SEGSEL3	SEGSEL2	SEGSEL1	SEGSEL0	(At reset : - 0 0 0 0 0 0 0)

SEGSEL0	SEG51 to 50 Port (P53 to P54) selection
0	Port (P53 to P54)
1	SEG51 to 50

SEGSEL1	SEG49 to 46 Port (P60 to P63) selection
0	Port (P60 to P63)
1	SEG49 to 46

SEGSEL2	SEG45 to 42 Port (P64 to P67) selection
0	Port (P64 to P67)
1	SEG45 to 42

SEGSEL3	SEG41 to 38 Port (P70 to P73) selection
0	Port (P70 to P73)
1	SEG41 to 38

SEGSEL4	SEG37 to 34 Port (P74 to P77) selection
0	Port (P74 to P77)
1	SEG37 to 34

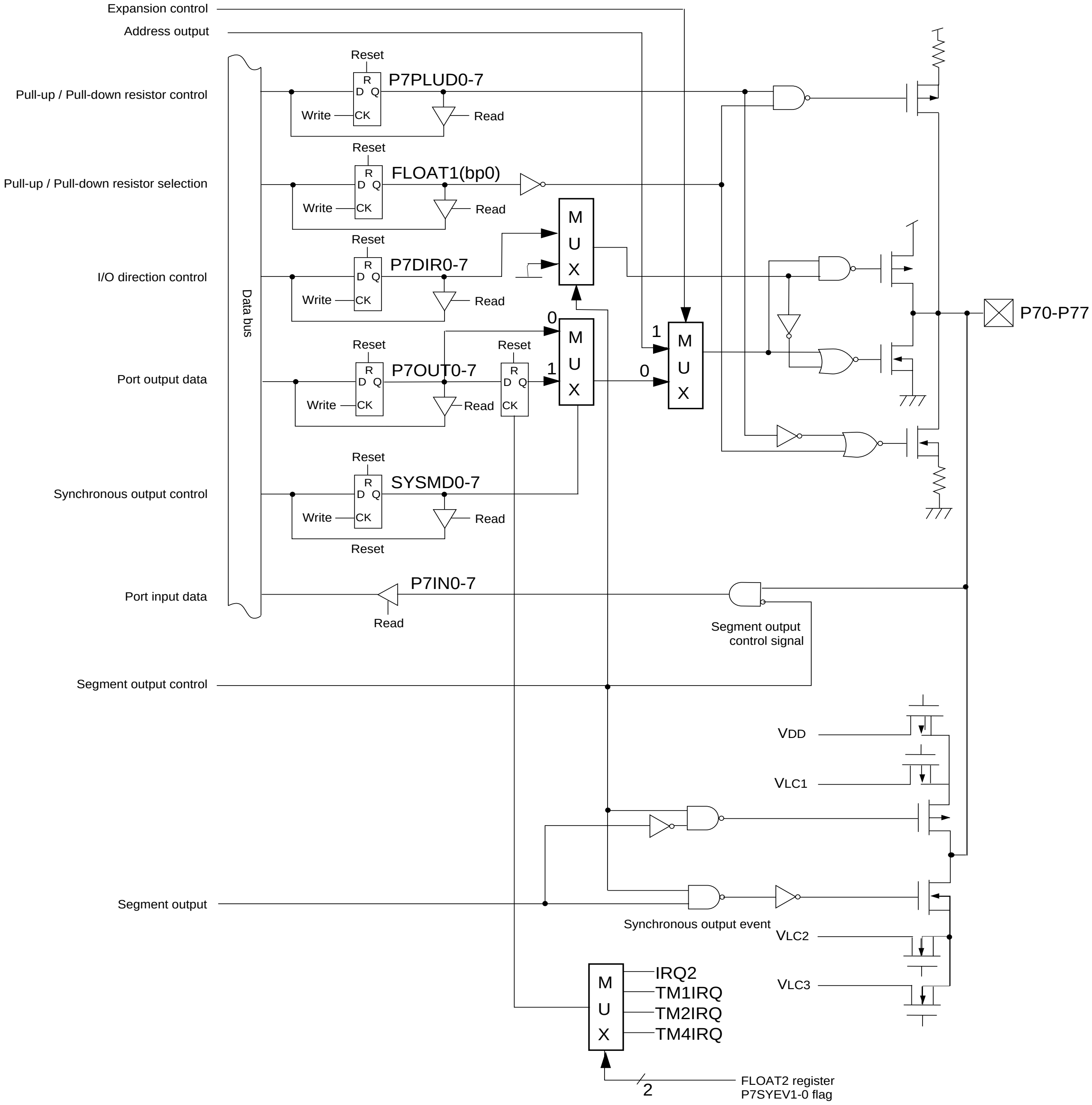
SEGSEL5	SEG30 to 33 Port (P84 to P87) selection
0	Port (P84 to P67)
1	SEG30 to 33

SEGSEL6	SEG26 to 29 Port (P80 to P83) selection
0	Port (P80 to P83)
1	SEG26 to 29

Segment output control register (LCCTR : x'03FCC', R/W)

Figure 4-8-4 Port 7 Registers (4/4)

4-8-3 Block Diagram



* When segment output is selected, segment output control automatically sets port I/O direction control to input mode, and segment output control is set to "without pull-up resistors".

* In memory expansion mode, set the bp5, 6 of the EXADV register to be used as general I/O pin, or as address output pin.

Figure 4-8-5 Block Diagram (P70 to P77)

4-9 Port 8

4-9-1 Description

■General Port Setup

Each bit of the port 8 control I/O direction register (P8DIR) can be set individually to set pins as input or output. The control flag of the port 8 direction control register (P8DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 8 direction control register (P8DIR) to "0" and read the value of the port 8 input register (P8IN).

To output data to pin, set the control flag of the port 8 direction control register (P8DIR) to "1" and write the value of the port 8 output register (P8OUT).

Each pin can be set individually if pull-up resistor is added or not, by the port 8 pull-up resistor control register (P8PLU). Set the control flag of the port 8 pull-up resistor control register (P8PLU) to "1" to add pull-up resistor.

At reset, the P80 to P87 input mode is selected and pull-up resistors are disabled (high impedance output).

■ Special Function Pin Setup

P80 to P87 are used as LCD driving pins (segment output), as well. The bp5 and 6 of the segment output control register (LCCTR) set if they are used as segment output pins or general I/O pins.

In memory expansion mode, P80 to P87 are I/O pins to the expansion memory. In this mode, any register cannot control input or output.

Table 4-9-1 Expansion Pins (P80 to P87)

Pins	In memory expansion mode
P80	D0 (External memory data bp0)
P81	D1 (External memory data bp1)
P82	D2 (External memory data bp2)
P83	D3 (External memory data bp3)
P84	D4 (External memory data bp4)
P85	D5 (External memory data bp5)
P86	D6 (External memory data bp6)
P87	D7 (External memory data bp7)

4-9-2 Registers

P8OUT (At reset : 0 0 0 0 0 0 0 0)

7	6	5	4	3	2	1	0
P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0

P8OUT	Output data
0	Low (V_{SS} level)
1	High (V_{DD} level)

Port 8 output register (P8OUT : x'03F18', R/W)

P8IN (At reset : X X X X X X X X)

7	6	5	4	3	2	1	0
P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0

P8IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 8 input register (P8IN : x'03F28', R)

P8DIR (At reset : 0 0 0 0 0 0 0 0)

7	6	5	4	3	2	1	0
P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0

P8DIR	I/O mode selection
0	Input mode
1	Output mode

Port 8 direction control register (P8DIR : x'03F38', R/W)

P8PLU (At reset : 0 0 0 0 0 0 0 0)

7	6	5	4	3	2	1	0
P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0

P8PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 8 pull-up resistor control register (P8PLU : x'03F48', R/W)

Figure 4-9-1 Port 8 Registers (1/2)

	7	6	5	4	3	2	1	0	
LCCTR	—	SEGSEL6	SEGSEL5	SEGSEL4	SEGSEL3	SEGSEL2	SEGSEL1	SEGSEL0	(At reset : - 0 0 0 0 0 0 0)

SEGSEL0	SEG51 to 50 Port (P53 to P54) selection
0	Port (P53 to P54)
1	SEG51 to 50

SEGSEL1	SEG49 to 46 Port (P60 to P63) selection
0	Port (P60 to P63)
1	SEG49 to 46

SEGSEL2	SEG45 to 42 Port (P64 to P67) selection
0	Port (P64 to P67)
1	SEG45 to 42

SEGSEL3	SEG41 to 38 Port (P70 to P73) selection
0	Port (P70 to P73)
1	SEG41 to 38

SEGSEL4	SEG37 to 34 Port (P74 to P77) selection
0	Port (P74 to P77)
1	SEG37 to 34

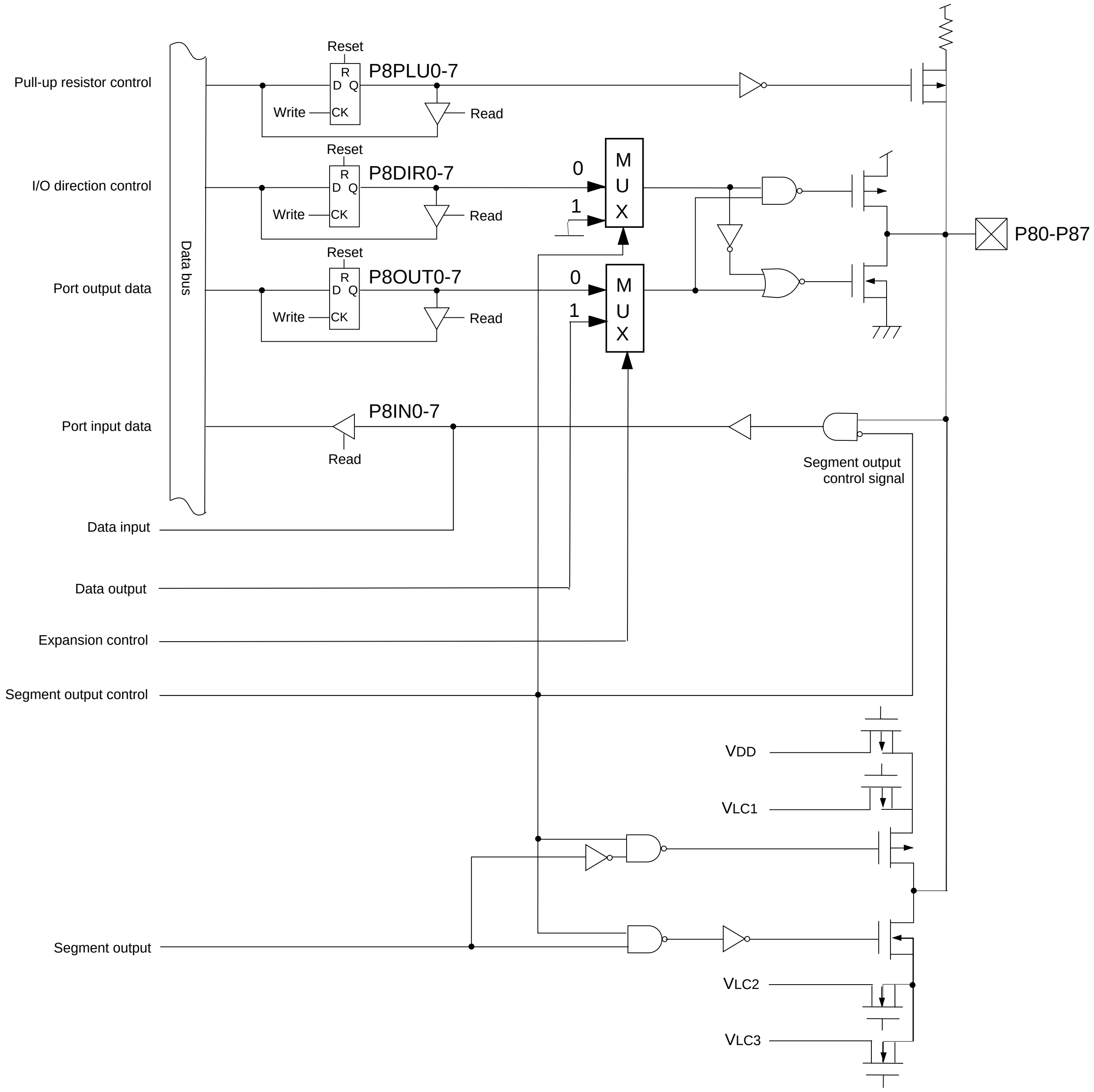
SEGSEL5	SEG30 to 33 Port (P84 to P87) selection
0	Port (P84 to P67)
1	SEG30 to 33

SEGSEL6	SEG26 to 29 Port (P80 to P83) selection
0	Port (P80 to P83)
1	SEG26 to 29

Segment output control register (LCCTR : x'03FCC', R/W)

Figure 4-9-2 Port 8 Registers (2/2)

4-9-3 Block Diagram



* In memory expansion mode, output mode is always selected.

* When segment output is selected, segment output control automatically sets port I/O direction control to input mode, and segment output control is set to "without pull-up resistors".

Figure 4-9-3 Block Diagram (P80 to P87)

4-10 Port A

4-10-1 Description

■General Port Setup

Port A is input port. To read input data of pin, read the value of the port A input register (PAIN).

Each pin can be set individually if pull-up / pull-down resistor is added or not, by the port A pull-up / pull-down resistor control register (PAPLUD). But pull-up / pull-down cannot be mixed. Set the control flag of the port A pull-up / pull-down resistor control register (PAPLUD) to "1" to add pull-up or pull-down resistor. The pin control register 1 (FLOAT1) select if pull-up resistor or pull-down resistor is added. The bp1 of the FLOAT1 is set to "1" for pull-down resistor, and set to "0" for pull-up resistor.

At reset, the PA0 to PA7 input mode is selected and pull-up resistors are disabled.

■Special Function Pin Setup

PA0 to PA7 are used as input pins for analog. Each bit can be set individually as an input by the port A input mode register (PAIMD). When they are used as analog input pins, set the port A input mode register (PAIMD) to "1". Then, the value of the port A input register (PAIN) is "1".

> By setting the control flag of the PAIMD register to "1", the through current is not occurred when input voltage is at intermediate level.

PA0 to PA7 are used as input pins for KEY interrupt as well.

> Key input pin should be pull-up pin in advance.

> When key input interrupt is used, set the REDG4 flag of the external input 4 control register (IRQ4ICR) to "0" (falling edge).

4-10-2 Registers

PAIN

7	6	5	4	3	2	1	0
PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0

(At reset : X X X X X X X X)

PAIN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port A input register (PAIN : x'03F2A', R)

PAIMD

7	6	5	4	3	2	1	0
PAIMD7	PAIMD6	PAIMD5	PAIMD4	PAIMD3	PAIMD2	PAIMD1	PAIMD0

(At reset : 0 0 0 0 0 0 0 0)

PAIMD	I/O port, analog n input pin selection
0	I/O port
1	Analog n input pin

Port A input control register (PAIMD : x'03F3A', R/W)

PAPLUD

7	6	5	4	3	2	1	0
PAPLUD7	PAPLUD6	PAPLUD5	PAPLUD4	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0

(At reset : 0 0 0 0 0 0 0 0)

PAPLUD	Pull-up (or Pull-down) resistor selection
0	No pull-up (or pull-down) resistor
1	Pull-up (or Pull-down) resistor

Port A pull-up / pull-down resistor control register (PAPLUD : x'03F4A', R/W)

Figure 4-10-1 Port A Registers (1/3)

	7	6	5	4	3	2	1	0	
FLOAT1	—	—	—	—	—	P21IM	PARDWN	P7RDWN	(At reset : - - - - - 0 0 0)

P7RDWN	Port 7 pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

PARDWN	Port A pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

P21IM	P21 input mode selection
0	Schmitt trigger input
1	ACZ input

Pin control register 1 (FLOAT1 : X'03F4B', R/W)

Figure 4-10-2 Port A Registers (2/3)

	7	6	5	4	3	2	1	0
P4IMD	IRQ4SEL	-	-	-	P4KYEN4	P4KYEN3	P4KYEN2	P4KYEN1

(At reset : 0 - - - 0 0 0 0)

P4KYEN1	PA0, PA1 key interrupt selection
0	disable
1	enable

P4KYEN2	PA2, PA3 key interrupt selection
0	disable
1	enable

P4KYEN3	PA4, PA5 key interrupt selection
0	disable
1	enable

P4KYEN4	PA6, PA7 key interrupt selection
0	disable
1	enable

IRQ4SEL	IRQ4 interrupt source selection
0	external interrupt IRQ4
1	PA key interrupt

Key interrupt control register (P4IMD : x'03F3C', R/W)

Figure 4-10-3 Port A Registers (3/3)

4-10-3 Block Diagram

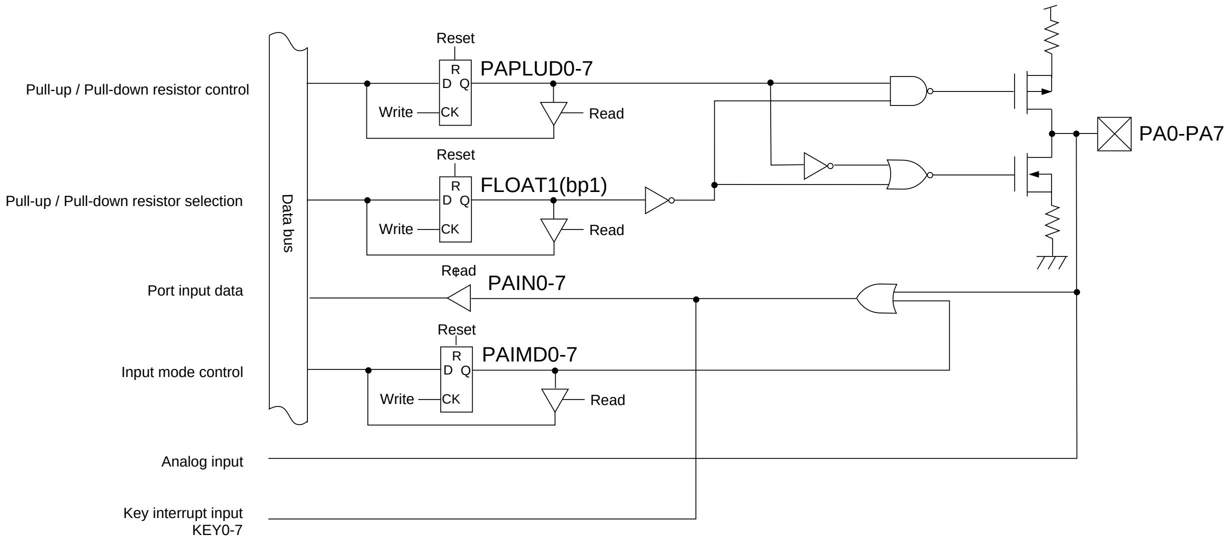


Figure 4-10-4 Block Diagram (PA0 to PA7)

4-11 Synchronous Output (Port 7)

Port 7 has the synchronous output function that outputs the any set data to pins, in synchronization with the generation of the specified event. Synchronous event is selected from the external interrupt 2 (P22/ IRQ2), timer 2 interrupt or timer 4 interrupt signal.

4-11-1 Block Diagram

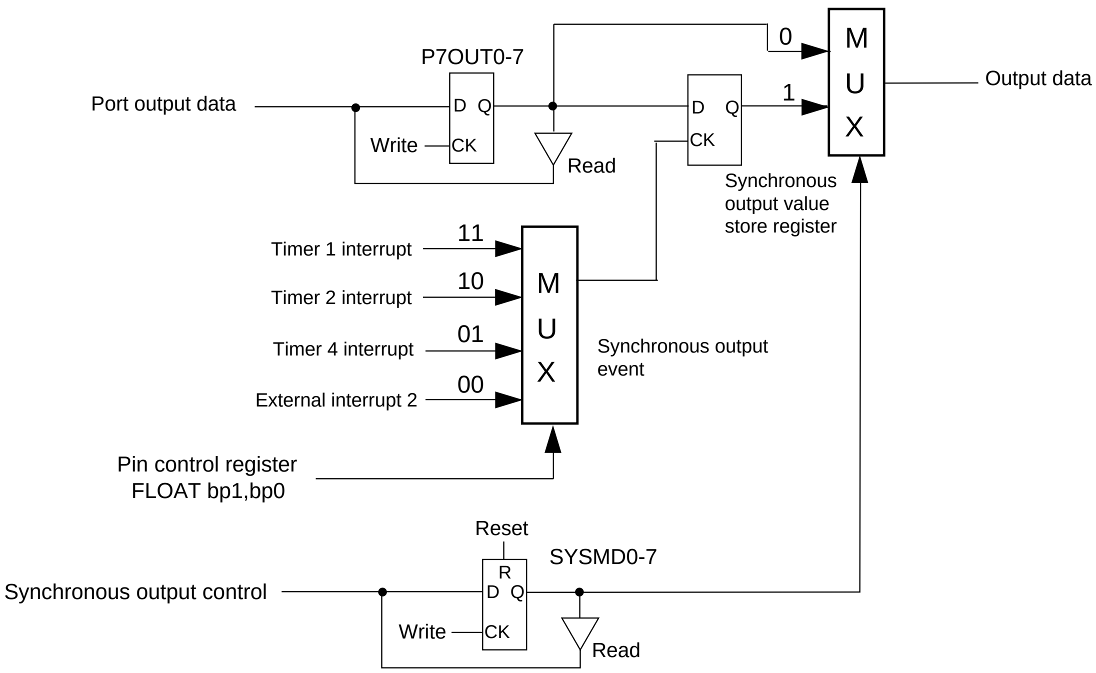


Figure 4-11-1 Synchronous Output Control Block Diagram

Set the bp1-0of the pin control register 2 (FLOAT2) to the value except "11".

4-11-2 Registers

Table 4-11-1 shows the synchronous output control registers of port 7.

Table 4-11-1 Synchronous Output Control Registers

	Register	Address	R/W	Function	Page
Port 7	FLOAT2	x'03F4C'	R/W	Pin control register 2	Ⅳ - 37
	SYSMD	x'03F1F'	R/W	Synchronous output control register	Ⅳ - 37
	P7DIR	x'03F37'	R/W	Port 7 direction control register	Ⅳ - 35
	P7PLUD	x'03F47'	R/W	Port 7 Pull-up / Pull-down control register	Ⅳ - 35
	P7OUT	x'03F17'	R/W	Port 7 output register	Ⅳ - 35

R/W : Readable/Writable

4-11-3 Operation

■Synchronous Output Setup

The synchronous output control register (SYSMD) selects the synchronous output pin of the port 7, in each bit.

The synchronous output event is selected by the pin control register 2 (FLOAT2).

Table 4-11-2 Synchronous Output Event

		Page
Synchronous output port	Port 7	Ⅳ - 33
Output event	External interrupt 2 (IRQ2)	Ⅲ - 19
	Timer 2	V - 25
	Timer 4	VI - 24

When the external interrupt 2 (IRQ2) is selected, the interrupt edge should be specified. The interrupt edge can be specified by the external interrupt 2 control register (IRQ2ICR). The synchronous output recognizes the generation of the specified edge as an event.

■Synchronous Output Operation

When the synchronous output control register (SYSMD) is set to disable the synchronous output (I/O port), the port 7 is functioned as a general port. [☞ Figure 4-11-1. Block Diagram]

After the output mode is selected by the port 7 direction control register (P7DIR), if the synchronous output is enabled by the synchronous output control register (SYSMD), the value of the synchronous output value stored register is output from pins. If the synchronous output event that is set by the pin control register 2 (FLOAT2) is never generated, the synchronous output value stored register holds the same value when the synchronous output event is enabled.

Store the value that should be output from pin after the synchronous output event is generated, to the port 7 output register (P7OUT). Once the synchronous output event that is set by the pin control register 2 (FLOAT2) is generated, the data of the synchronous output value stored register is switched to the data of the port 7 output register (P7OUT), and the output value from pin is changed.

> When the port 7 synchronous output is disabled, the value of the synchronous output value stored register is not always same to the value of the port 7 output register (P7OUT).
> This is because, the pin output may be changed at switching from general output to synchronous output.

■Port 7 Synchronous Output (External interrupt 2 IRQ2)

The synchronous output timing when the synchronous output event is set at the falling edge of the external interrupt 2, is shown below. The latched data on port 7 is output in synchronization with the falling edge of the IRQ2.

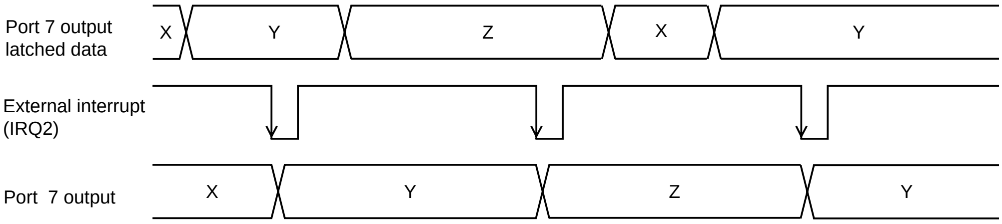


Figure 4-11-2 Synchronous Output Timing by Event Generation (IRQ2)

■Port 7 Synchronous Output (Timers 2 and 4)

The timer interrupt flag TMnIRQ is generated when binary counter and compare register are matched. The latched data on port 7 is output from the port 7 in synchronization with the rising edge of the TMnIRQ. About the setting of each timer operation. [☞ Chapter 5. 8-bit timers, Chapter 6. 16-bit timers]

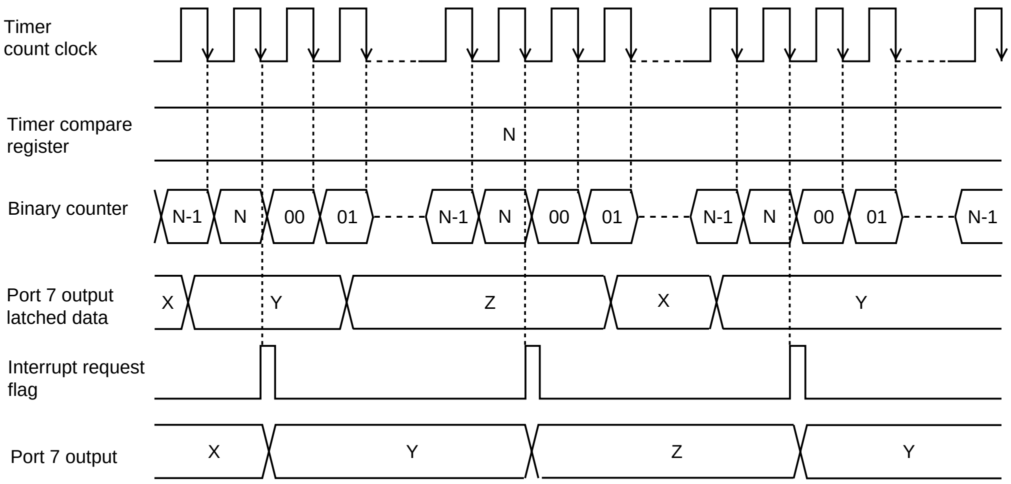


Figure 4-11-3 Synchronous Output Timing by Event Generation (Timers 2 and 4)

4-11-4 Setup Example

A setup example of the port 7 synchronous output by the external interrupt 2 (IRQ2) is shown as follows. As it is operated, the initial output data of port 7 is "55", the synchronous output data is "AA", and the rising edge of the IRQ2 is selected at the synchronous event.

An example setup procedure, with description of each step is shown below.

Setup Procedure	Description
(1) Select the synchronous output event. FLOAT2 (x'3F4C') bp1-0 :P7SYEVS1-0 = 00	(1) Set the P7SYEVS1-0 flag of the FLOAT2 register to "00" to set the synchronous output event to the IRQ2.
(2) Specify the interrupt edge. IRQ2ICR(x'3FEB') bp5 : REDG2 = 1	(2) Set the REDG2 flag of the IRQ2ICR register to "1" to set the active edge of the IRQ2 at the rising edge.
(3) Set the initial output data. P7OUT(x'3F17') bp7-0 : P7OUT7-0 = x'55' P7DIR(x'3F37') bp7-0 : P7DIR7-0 = x'FF'	(3) Set the initial output data "55" to the P7OUT register. Select output mode after the P7DIR7-0 flag of the P7DIR register is set to "FF". Port 7 outputs "55".
(4) Set the synchronous output pin. SYSMD(x'3F1F') bp7-0 : SYSMD7-0 = x'FF'	(4) Port 7 is set to synchronous output pin by setting the SYSMD7-0 flag of the SYSMD register to "FF".
(5) Set the synchronous output data. P7OUT(x'3F17') bp7-0 : PDOUT7-0 = x'AA'	(5) Set the synchronous output data "AA" to the P7OUT register.
(6) Event is generated. Rising edge is generated at P22.	(6) Port 7 outputs "AA" at the rising edge of IRQ2.

Chapter 5 8-bit Timers

5-1 Overview

This LSI contains 1 general purpose 8-bit timer (Timers 2) and 1 8-bit timer (Timers 3) that can be also used as baud rate timer. Timers timers 2 and 3 can be used as 16-bit timers with cascade connection.

5-1-1 Functions

Table 5-1-1 shows functions of each timer.

Table 5-1-1 Timer Functions

	Timer 2 (8 bit)	Timer 3 (8 bit)	Timer 5 * (8 bit)
Interrupt source	TM2IRQ	TM3IRQ	TM5IRQ
Timer operation	√	√	√
Event count	√	√	-
Timer pulse output	√	√	-
PWM output	√	-	-
Synchronous output	√	-	-
Serial transfer clock output	-	√ (SIF0,1)	-
Cascade connection	√		-
Remote control carrier output	-	√	-
Clock source	fs fs/4 fx TM2IO input	fosc fs/4 fs/16 TM3IO input	fosc fs/4 fx $fosc/2^{13}$ $fx/2^{13}$
fosc : Machine clock (High speed oscillation) fx : Machine clock (Low speed oscillation) fs : System clock (at NORMAL mode : fs=fosc/2, at SLOW mode : fs=fx/4) - When timer 3 is used as a baud rate timer for serial interface function, it is not used as a general timer.			

* Description of timer 5 is shown in Chapter 7.

5-1-2 Block Diagram

■Timers 2 and 3 Block Diagram

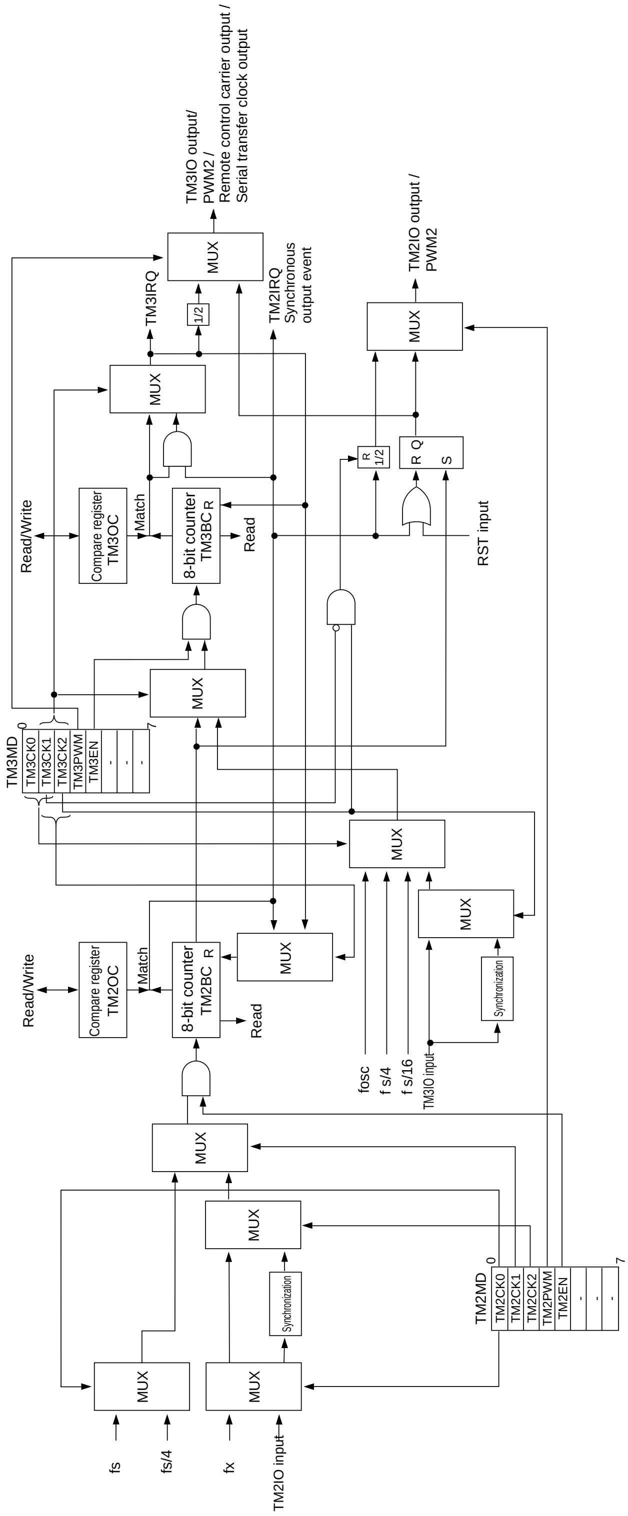


Figure 5-1-1 Timers 2 and 3 Block Diagram

■Remote Control Carrier Output Block Diagram

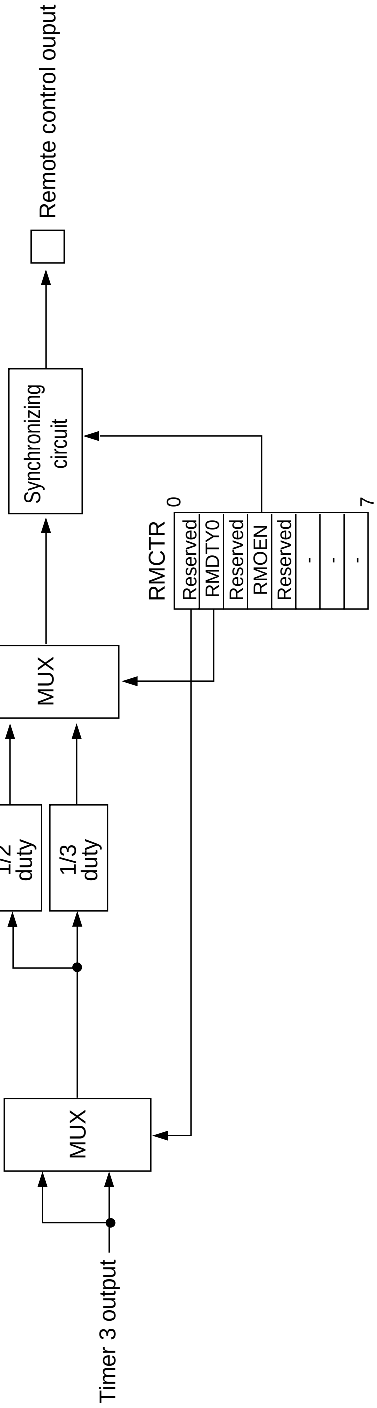


Figure 5-1-2 Remote Control Carrier Output Block Diagram

5-2 Control Registers

Timers 2 and 3 consist of the binary counter (TMnBC) and the compare register (TMnOC). And they are controlled by the mode register (TMnMD). Remote control carrier output is controlled by the remote control carrier output control register (RMCTR).

5-2-1 Registers

Table 5-2-1 shows registers that control timers 2 and 3 and remote control carrier output.

Table 5-2-1 8-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 2	TM2BC	x'03F62'	R	Timer 2 binary counter	V - 6
	TM2OC	x'03F72'	R/W	Timer 2 compare register	V - 6
	TM2MD	x'03F82'	R/W	Timer 2 mode register	V - 7
	TM2ICR	x'03FE6'	R/W	Timer 2 interrupt control register	Ⅲ - 22
	P1OMD	x'03F39'	R/W	Port 1 output mode register	Ⅳ - 14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	Ⅳ - 13
Timer 3	TM3BC	x'03F63'	R	Timer 3 binary counter	V - 6
	TM3OC	x'03F73'	R/W	Timer 3 compare register	V - 6
	TM3MD	x'03F83'	R/W	Timer 3 mode register	V - 8
	TM3ICR	x'03FEE'	R/W	Timer 3 interrupt control register	Ⅲ - 23
	P1OMD	x'03F39'	R/W	Port 1 output mode register	Ⅳ - 14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	Ⅳ - 13
Remote control carrier output	RMCTR	x'03F89'	R/W	Remote control carrier output control register	V - 9

R/W : Readable / Writable
R : Readable only

5-2-2　Programmable Timer Registers

Each of timers 2 and 3 has 8-bit programmable timer registers. Programmable timer register consists of compare register and binary counter.

Compare register is 8-bit register which stores the value to be compared to binary counter.

■Timer 2 Compare Register (TM2OC)

	7	6	5	4	3	2	1	0	
TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	(At reset : X X X X X X X X)

Figure 5-2-1　Timer 2 Compare Register (TM2OC : x'03F72', R/W)

■Timer 3 Compare Register (TM3OC)

	7	6	5	4	3	2	1	0	
TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	(At reset : X X X X X X X X)

Figure 5-2-2　Timer 3 Compare Register (TM3OC : x'03F73', R/W)

Binary counter is 8-bit up counter. If any data is written to compare register during counting is stopped, binary counter is cleared to x'00'.

■Timer 2 Binary Counter (TM2BC)

	7	6	5	4	3	2	1	0	
TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	(At reset : 0 0 0 0 0 0 0 0)

Figure 5-2-3　Timer 2 Binary Counter (TM2BC : x'03F62', R)

■Timer 3 Binary Counter (TM3BC)

	7	6	5	4	3	2	1	0	
TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	(At reset : 0 0 0 0 0 0 0 0)

Figure 5-2-4　Timer 3 Binary Counter (TM3BC : x'03F63', R)

5-2-3 Timer Mode Registers

Timer mode register is readable/writable register that controls timers 2 and 3.

■Timer 2 Mode Register (TM2MD)

	7	6	5	4	3	2	1	0
TM2MD	-	-	-	TM2EN	TM2PWM	TM2CK2	TM2CK1	TM2CK0

(At reset : - - - 0 0 X X X)

TM2CK2	TM2CK1	TM2CK0	Clock source
-	0	0	fs
		1	fs/4
0	1	0	fx
		1	TM2IO input
1		0	Synchronous fx
		1	Synchronous TM2IOinput

TM2PWM	Timer 2 operation mode selection
0	Normal timer operation
1	PWM operation

TM2EN	Timer 2 count control
0	Disable the count
1	Enable the count

Figure 5-2-5 Timer 2 Mode Register (TM2MD : x'03F82', R/W)

■Timer 3 Mode Register (TM3MD)

	7	6	5	4	3	2	1	0
TM3MD	-	-	-	TM3EN	TM3PWM	TM3CK2	TM3CK1	TM3CK0

(At reset : - - - 0 0 X X X)

TM3CK2	TM3CK1	TM3CK0	Clock source
0	0	0	fosc
		1	fs/4
	1	0	fs/16
		1	TM3IO input
1	0	-	Timer 2 and Timer 3 cascade connection
	1	1	Synchronous TM3IO input

TM3PWM	P13 output selection at TM2PWM operation
0	Timer 3 output
1	Timer 2 PWM output

TM3EN	Timer 3 count control
0	Disable the count
1	Enable the count

Figure 5-2-6 Timer 3 Mode Register (TM3MD : x'03F83', R/W)

■Remote Control Carrier Output Control Register (RMCTR)

	7	6	5	4	3	2	1	0
RMCTR	-	-	-	Reserved	RMOEN	Reserved	RMDTY0	Reserved

(At reset : - - - 0 0 X X 0)

Reserved	Set always "0".

RMDTY0	Remote control carrier output duty
0	1/2 duty
1	1/3 duty

Reserved	Set always "0".

RMOEN	Enable remote control carrier output
0	Output low level
1	Output remote control carrier

Reserved	Set always "0".

Figure 5-2-7 Remote Control Carrier Output Control Register (RMCTR : x'03F89', R/W)

5-3 8-bit Timer Count

5-3-1 Operation

The timer operation can constantly generate interrupts.

■8-bit Timer Operation (Timers 2 and 3)
The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TMnOC), in advance. If the binary counter (TMnBC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then binary counter is cleared and counting is restarted from x'00'.
Table 5-3-1 shows clock source that can be selected.

Table 5-3-1 Clock Source (Timers 2 and 3) at Timer Operation

Clock source	1 count time	Timer 2 (8 Bit)	Timer 3 (8 Bit)
fosc	50 ns	-	√
fs	100 ns	√	-
fs/4	400 ns	√	√
fs/16	1.6 µs	-	√
fx	30.5 µs	√	-
Notes : as fosc = 20 MHz fx = 32.768 kHz fs = fosc/2 = 10 MHz			

■Count Timing of Timer Operation (Timers 2 and 3)

Binary counter counts up with selected clock source as a count clock.

The basic operation of the whole function of 8-bit timer is as follows ;

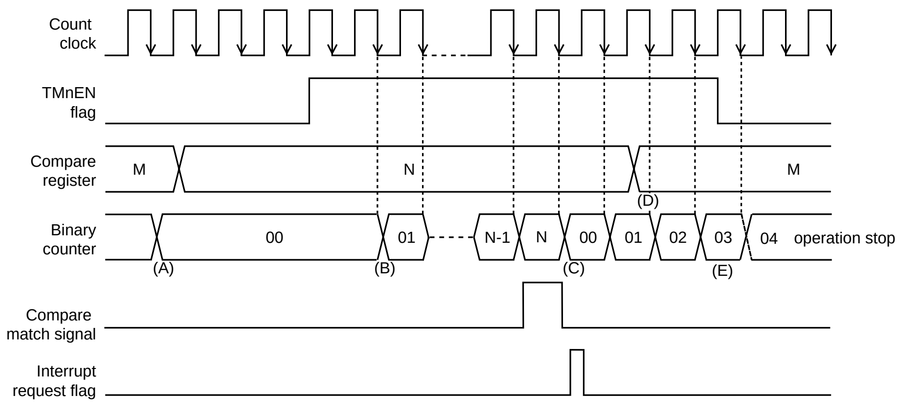


Figure 5-3-1 Count Timing of Timer Operation (Timers 2 and 3)

(A) If the value is written to the compare register during the TMnEN flag is "0", the binary counter is cleared to x'00', at the writing cycle.

(B) If the TMnEN flag is "1", the binary counter is started to count.
The counter starts to count up at the falling edge of the count clock.
But the binary counter doesn't count up at the first falling of the count edge.

(C) If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared to x'00' and the counting is restarted.

(D) Even if the compare register is rewritten during the TMnEN flag is "1", the binary counter is not changed.

(E) If the TMnEN flag is "0", the binary counter is stopped after 1 count up.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So, set the compare register as :

Compare register setting = (count till the interrupt request - 1)

If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.

If the interrupt is enabled, the timer interrupt request flag should be cleared before timer operation is started.

Even if the TMnEN flag of the timer is cleared during operation, it does not stop until the next count clock. Therefore, during max. 1 count clock after the TMnEM is cleared, the binary counter cannot be initialized.

5-3-2 Setup Example

■Timer Operation Setup Example (Timers 2 and 3)

Timer function can be set by using timer 2 that generates the constant interrupt. By selecting fs/4 (at fosc = 20 MHz) as a clock source, interrupt is generated every 250 clock cycles (100 µs) .

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'3F82') bp4 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the counting of timer 2.
(2) Select the normal timer operation. TM2MD (x'3F82') bp3 :TM2PWM = 0	(2) Set the TM2PWM flag of the TM2MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM2MD (x'3F82') bp2-0 :TM2CK2-0 = 001	(3) Select fs/4 to the clock source by the TM2CK2-0 flag of the TM2MD register.
(4) Set the cycle of the interrupt generation. TM2OC (x'3F72') = x'F9'	(4) Set the value of the interrupt generation cycle to the timer 2 compare register (TM2OC). The cycle is 250, so that the setting value is set to 249 (x'F9'). At that time, the timer 2 binary counter (TM2BC) is initialized to x'00'.
(5) Set the interrupt level. TM2ICR (x'3FE6') bp7-6 :TM2LV1-0 = 10	(5) Set the interrupt level by the TM2LV1-0 flag of the timer 2 interrupt control register (TM2ICR). If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt flag setting]
(6) Enable the interrupt. TM2ICR (x'3FE6') bp1 :TM2IE = 1	(6) Set the TM2IE flag of the TM2ICR register to "1" to enable the interrupt.

Setup Procedure	Description
(7) Start the timer operation. TM2MD (x'3F82') bp4 :TM2EN = 1	(7) Set the TM2EN flag of the TM2MD register to "1" to start the timer 2.

The TM2BC starts to count up from 'x00'. When the TM2BC reaches the setting value of the TM2OC register, the timer 2 interrupt request flag is set at the next count clock, then the value of the TM2BC becomes x'00' and restart to count up.

When the TMnEN flag of the TMnMD register is changed at the same time to other bit, binary counter may count up by the switching operation.

The initial value of the TM3CK2-0 in the TM3MD register is indefinite.
When timer 2 / timer 3 is used independently, set any mode except cascade connection.

If fx is selected as the count clock source in timer 2, when the binary counter is read at operation, uncertain value on counting up may be read. To prevent this, select the synchronous fx as the count clock source. In this case, the timer 2 counter counts up in synchronization with system clock, therefore the correct value is always read.
But, if the synchronous fx is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

5-4 8-bit Event Count

5-4-1 Operation

Event count operation has 2 types ; TMnIO input and synchronous TMnIO input can be selected as the count clock.

■8-bit Event Count Operation
Event count means that the binary counter (TMnBC) counts the input signal from external to the TMnIO pin. If the value of the binary counter reaches the setting value of the compare register (TMnOC), interrupts can be generated at the next count clock.

Table 5-4-1 Event Count Input Clock

	Timer 2	Timer 3
Event input	TM2IO input (P12)	TM3IO input (P13)
	Synchronous TM2IO input	Synchronous TM3IO input

■Count Timing of TMnIO Input (Timers 2 and 3)
When TMnIO input is selected, TMnIO input signal is directly input to the count clock of the timer n. The binary counter counts up at the falling edge of the TMnIO input signal.

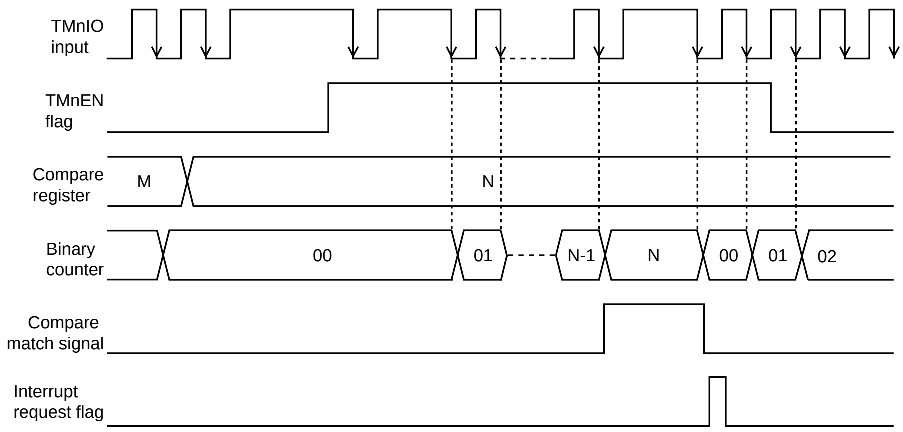


Figure 5-4-1 Count Timing of TMnIO Input (Timers 2 and 3)

When the TMnIO input is selected for count clock source and the value of the timer n binary counter is read during operation, incorrect value at count up may be read. To prevent this, use the event count by synchronous TMnIO input, as the following page.

■Count Timing of Synchronous TMnIO Input (Timers 2 and 3)

If the synchronous TMnIO input is selected, the synchronizing circuit output signal is input to the timer n count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TMnIO input signal is changed.

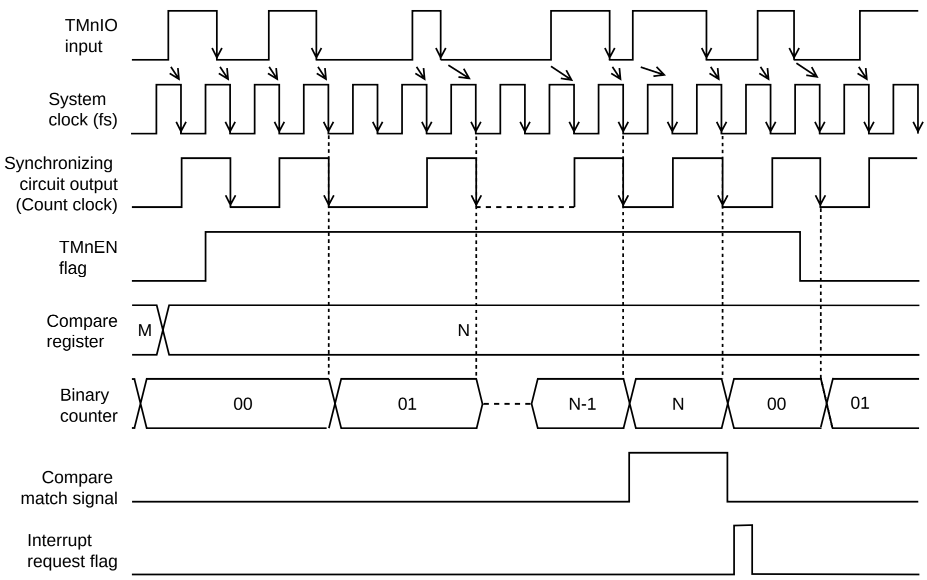


Figure 5-4-2 Count Timing of Synchronous TMnIO Input (Timers 2 and 3)

When the synchronous TMnIO input is selected as the count clock source, the timer n counter counts up in synchronization with system clock, therefore the correct value is always read.

But, if the synchronous TMnIO is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

5-4-2 Setup Example

■Event Count Setup Example (Timers 2 and 3)
If the falling edge of the TM2IO input pin signal is detected 5 times with using timer 2, an interrupt is generated.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'3F82') bp4 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop timer 2 counting.
(2) Set the special function pin to input. P1DIR (x'3F31') bp2 :P1DIR2 = 0	(2) Set the P1DIR2 flag of the port 1 direction control register (P1DIR) to "0" to set P12 pin to input mode. If it needs, pull up resistor should be added. [☞ Chapter 4. I/O Port Function]
(3) Select the normal timer operation. TM2MD (x'3F82') bp3 :TM2PWM = 0	(3) Set the TM2PWM flag of the TM2MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM2MD (x'3F82') bp2-0 :TM2CK2-0 = 011	(4) Select the clock source to TM2IO input by the TM2CK2-0 flag of the TM2MD register.
(5) Set the interrupt generation cycle. TM2OC (x'3F72') = x'04'	(5) Set the timer 2 compare register (TM2OC) the interrupt generation cycle. Counting is 5, so the setting value should be 4. At that time, the timer 2 binary counter (TM2BC) is initialized to x'00'.
(6) Set the interrupt level. TM2ICR (x'3FE6') bp7-6 :TM2LV1-0 = 10	(6) Set the interrupt level by the TM2LV1-0 flag of the timer 2 interrupt control register (TM2ICR). If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]

Setup Procedure	Description
(7) Enable the interrupt. TM2ICR (x'3FE6') bp1 :TM2IE = 1	(7) Set the TM2IE flag of the TM2ICR register to "1" to enable the interrupt.
(8) Start the event counting. TM2MD (x'3F82') bp4 :TM2EN = 1	(8) Set the TM2EN flag of the TM2MD register to start timer 2.

Every time TM2BC detects the falling edge of TM2IO input, TM2BC counts up from 'x00'. When TM2BC reaches the setting value of theTM2OC register, the timer 2 interrupt request flag is set at the next count clock, then the value of TM2BC becomes x'00' and counting up is restarted.

5-5 8-bit Timer Pulse Output

5-5-1 Operation

The TMnIO pin can output a pulse signal with any cycle.

■Operation of Timer Pulse Output (Timers 2 and 3)
The timers can output 2 × cycle signal, compared to the setting value in the compare register (TMnOC).
Output pins are as follows ;

Table 5-5-1 Timer Pulse Output Pins

	Timer 2	Timer 3
Pulse output pin	TM2IO output (P12)	TM3IO output (P13)

■Count Timing of Timer Pulse Output (Timers 2 and 3)

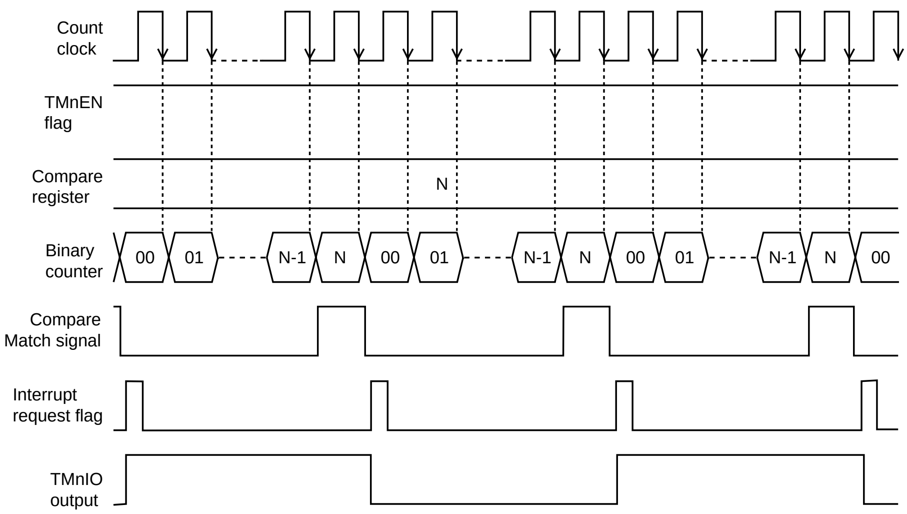


Figure 5-5-1 Count Timing of Timer Pulse Output (Timers 2 and 3)

The TMnIO pin outputs 2 × cycle, compared to the value in the compare register. If the binary counter reaches the compare register, and the binary counter is cleared to x'00', TMnIO output is inverted.

5-5-2 Setup Example

■Timer Pulse Output Setup Example (Timers 2 and 3)
TM3IO pin outputs 50 kHz pulse by using timer 3. For this, select fosc as clock source, and set a 1/2 cycle (100 kHz) for the timer 3 compare register (at fosc=20 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM3MD (x'3F83') bp4 :TM3EN = 0	(1) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop timer 3 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F39') bp3 :P13TCO = 1 P1DIR (x'3F31') bp3 :P1DIR3 = 1	(2) Set the P13TCO flag of the port 1 output mode register (P1OMD) to "1" to set P13 the special function pin. Set the P1DIR3 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. If it needs, pull-up resister should be added. [☞ Chapter 4. I/O Ports]
(3) Select the normal timer operation. TM3MD (x'3F83') bp3 :TM3PWM = 0	(3) Set the TM3PWM flag of the TM3MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM3MD (x'3F83') bp2-0 :TM3CK2-0 = 000	(4) Select fosc for the clock source by the TM3CK2-0 flag of the TM3MD register.
(5) Set the timer pulse output cycle. TM3OC (x'3F73') = x'C7'	(5) Set the timer 3 compare register (TM3OC) to the 1/2 of the timer pulse output cycle. The setting value should be 200-1=199(x'C7'), because 100 kHz is divided by 20 MHz. At that time, the timer 3 binary counter (TM3BC) is initialized to x'00'.
(6) Start the timer operation. TM3MD (x'3F83') bp4 :TM3EN = 1	(6) Set the TM3EN flag of the TM3MD register to "1" to start timer 3.

TM3BC counts up from x'00'. If TM3BC reaches the setting value of the TM3OC register, then TM3BC is cleared to x'00', TM3IO output signal is inverted and TM3BC restarts to count up from x'00'.

When port 1 is used as pulse output pin, the settings of the port 1 direction control register (P1DIR) and the port 1 pull-up register (P1PLU) are need to set to "1".

Set the compare register value as follows,

$$\text{The compare register value} = \frac{\text{The timer pulse output cycle}}{\text{The count clock cycle} \times 2} - 1$$

The initial value of timer output and the initialization (low level)

	Initial value (after reset release)	To initialize (Set to low level)	Program example
Timer 2	Low level	After timers 2 and 3 are set to cascade connection, the setting should be the original.	mov x'04', (TM3MD) bclr (TM3MD), 2
Timer 3	indefinite	After P13 output selection is set to the timer 2 PWM output (TM2PWM flag = 1), the setting should be back to the timer 3 output.	mov x'08', (TM3MD) bclr (TM3MD), 3

5-6 8-bit PWM Output

The TMnIO pin outputs the PWM waveform, which is determined by the match timing for the compare register and the overflow timing of the binary counter.

5-6-1 Operation

■Operation of 8-bit PWM Output (Timer 2)
The PWM waveform with any duty cycle is generated by setting the duty cycle of PWM "H" period to the compare register (TMnOC). The cycle is the period from the full count to the overflow of the 8-bit timer.
Table 5-6-1 shows PWM output pins ;

Table 5-6-1 Output Pins of PWM Output

	Timer 2
PWM output pin	TM2IO output pin (P12) TM3IO output pin (P13)

■Count Timing of PWM Output (at normal) (Timer 2)

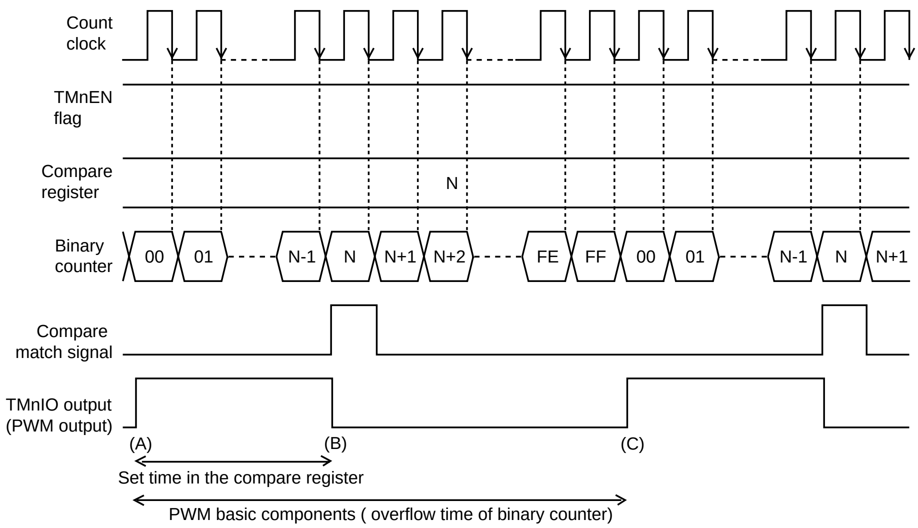


Figure 5-6-1 Count Timing of PWM Output (at Normal)

PWM source waveform,

(A) is "H" while counting up from x'00' to the value stored in the compare register.

(B) is "L" after the match to the value in the compare register, then the binary counter continues counting up till the overflow.

(C) is "H" again, if the binary counter overflows.

■Count Timing of PWM Output (when the compare register is x'00') (Timer 2)
Here is the count timing when the compare register is set to x'00' ;

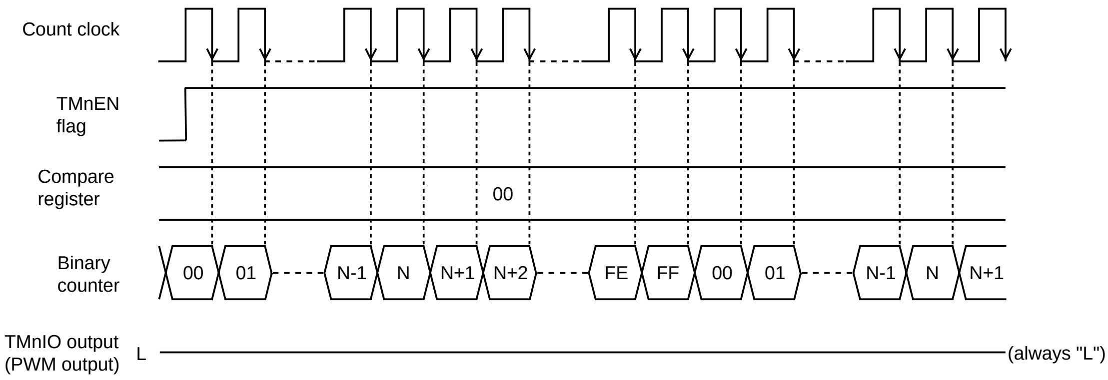


Figure 5-6-2 Count Timing of PWM Output (when compare register is x'00')

■Count Timing of PWM Output (when the compare register is x'FF') (Timer 2)
Here is the count timing when the compare register is set to x'FF' ;

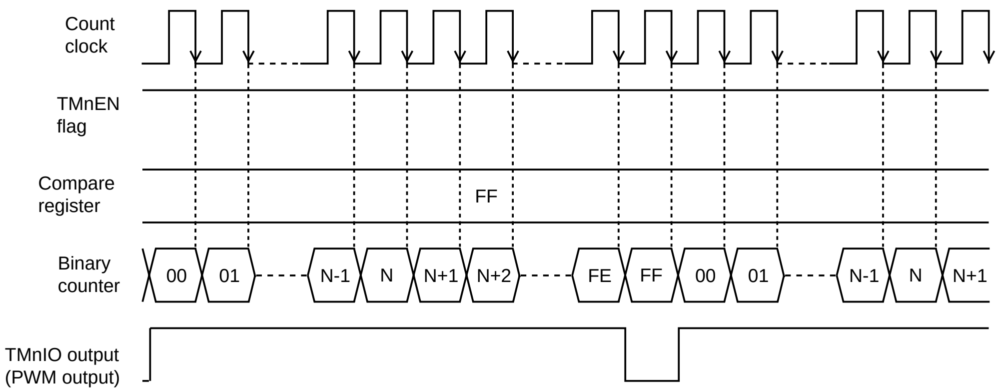


Figure 5-6-3 Count Timing of PWM Output (when compare register is x'FF')

5-6-2 Setup Example

■PWM Output Setup Example (Timer 2)

The 1/4 duty cycle PWM output waveform is output from the TM2IO output pin at 2 kHz by using timer 2 (at fosc=4.19 MHz). Cycle period of PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the setting value of the compare register. An example setup procedure, with a description of each step is shown below.

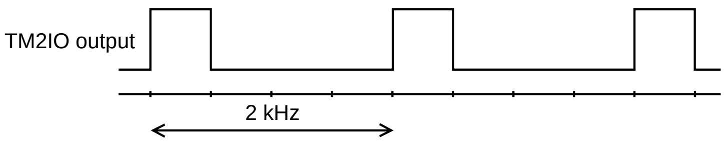


Figure 5-6-4 Output Waveform of TM0IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'3F82') bp4 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the timer 2 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F39') bp2 :P12TCO = 1 P1DIR (x'3F31') bp2 :P1DIR2 = 1	(2) Set the P12TCO flag of the port 1 output mode register (P1OMD) to "1" to set P12 pin to the special function pin. Set the P1DIR2 flag of the port 1 direction control register (P1DIR) to "1" for the output mode. If it needs, pull up resistor should be added. [☞ Chapter 4. I/O Ports]
(3) Select the PWM operation. TM2MD (x'3F82') bp3 :TM2PWM = 1	(3) Set the TM2PWM flag of the TM2MD register to "1" to select the PWM operation.
(4) Select the count clock source. TM2MD (x'3F82') bp2-0 :TM2CK2-0 = 001	(4) Select "fs/4" for the clock source by the TM2CK2-0 flag of the TM2MD register.

Setup Procedure	Description
(5) Set the period of PWM "H" output. TM2OC (x'3F72') = x'40'	(5) Set the "H" period of PWM output to the timer 2 compare register (TM2OC). The setting value is set to 256 / 4 = 64 (x'40'), because it should be the 1/4 duty of the full count (256). At that time, the timer 2 binary counter (TM2BC) is initialized to x'00'.
(6) Start the timer operation. TM2MD (x'3F82') bp4 :TM2EN = 1	(6) Set the TM2EN flag of the TM2MD register to "1" to operate timer 2.

TM2BC counts up from x'00'. PWM source waveform outputs "H" till TM2BC reaches the setting value of the TM2OC register, and outputs "L" after that. Then, TM2BC continues counting up, and PWM source waveform outputs "H" again, once overflow happens, and TM2BC restarts counting up from x'00'.

If the timer 2 PWM output is selected by setting the TM3PWM flag of the TM3MD register to "1", the TM3IO pin outputs the timer 2 PWM output, too.

When port 1 is used as PWM output pin, the settings of the P1DIR register and the P1PLU register are need to set to "1".

5-7 8-bit Timer Synchronous Output

5-7-1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latched data is output from port 7 at the next count clock.

■Synchronous Output Operation by 8-bit timer (Timer 2)
The port 7 latched data is output from the output pin at the interrupt request generation by the match of the binary counter and the compare register.
Only port 7 can perform synchronous output operation, and individual pins can be set. 8-bit timers that have synchronous output operation are timer 2.

Table 5-7-1 Synchronous Output Port (Timer 2)

	Timer 2
Synchronous output port	Port 7

■Count Timing of Synchronous Output (Timer 2)

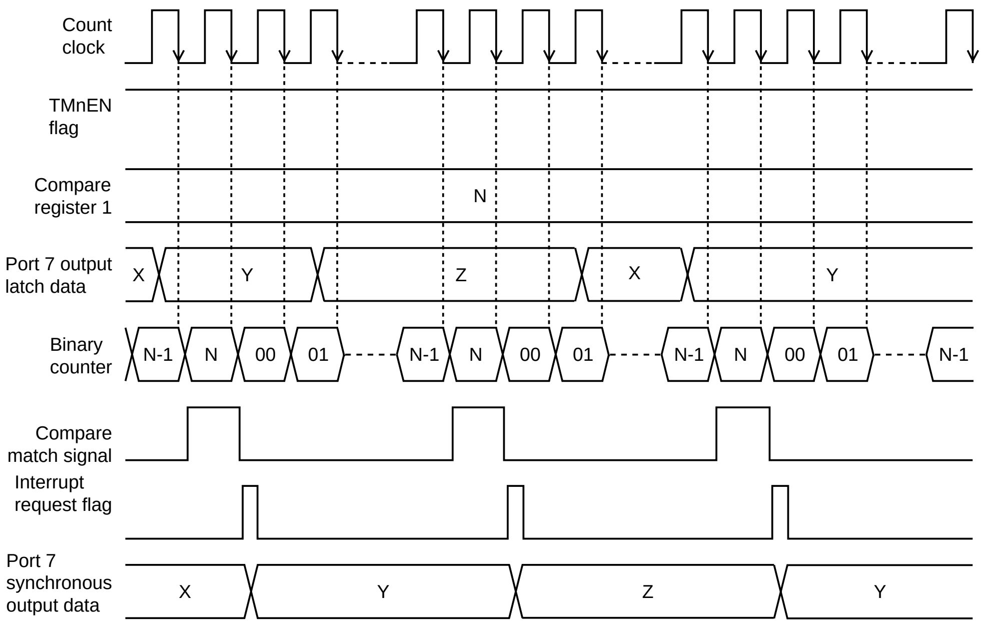


Figure 5-7-1 Count Timing of Synchronous Output (Timer 2)

The port 7 latched data is output from the output pin in synchronization with the interrupt request generation by the match of binary counter and compare register.

5-7-2 Setup Example

■Synchronous Output Setup Example (Timer 2)

Setup example that latched data of port 7 is output constantly (100 µs) by using timer 2 from the synchronous output pin is shown below. The clock source of timer 2 is selected fs/4 (at fosc=8 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Start the counter. TM2MD (x'3F82') bp4 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the timer 2 counting.
(2) Select the synchronous output event. FLOAT2 (x'3F4C') bp1-0 :P7SYEVS2-1 = 10	(2) Set the P7SYEVS2-1 flag of the pin control register 2 (FLOAT2) to "10" to set the synchronous output event to timer 2 interrupt.
(3) Set the synchronous output pin. SYSMD (x'3F1F') = x'FF' P7DIR (x'3F37') = x'FF'	(3) Set the synchronous output control register (SYSMD) to x'FF' to set the synchronous output pin. (P77 to P70 are synchronous output pin.) Set the port 7 direction control register (P7DIR) to x'FF' to set port 7 to output mode. If it needs, pull up resistor should be added. [☞ Chapter 4. I/O Ports]
(4) Select the normal timer operation. TM2MD (x'3F82') bp3 :TM2PWM = 0	(4) Set the TM2PWM flag of the TM2MD register to "0" to select the normal timer operation.
(5) Select the count clock source. TM2MD (x'3F82') bp2-0 :TM2CK2-0 = 001	(5) Select fs/4 for clock source by TM2CK2-0 flag of the TM2MD register.

Setup Procedure	Description
(6) Set the synchronous output event generation cycle. TM2OC (x'3F72') = x'63'	(6) Set the synchronous output generation cycle to the timer 2 compare register (TM2OC). The setting value is set to 100 - 1 = 99 (x'63'), because 1 MHz is divided by 10 kHz. At that time, the timer 2 binary counter (TM2BC) is initialized to x'00'.
(7) Start the timer operation. TM2MD (x'3F82') bp4 :TM2EN = 1	(7) Set the TM2EN flag of the TM2MD register to "1" to start timer 2.

TM2BC counts up from x'00'. If any data is written to the port 7 output register (P7OUT), the data of port 7 is output from the synchronous output pin in every time an interrupt request is generated by the match of TM2BC and the set value of the TM2OC register.

> When the port 7 synchronous output is disabled, the value of the synchronous output value storage register is not always same to the value of the port 7 output register (P7OUT). Therefore, the pin output may be changed at the switching from the general output to the synchronous output.

5-8 Serial Interface Transfer Clock Output

5-8-1 Operation

Serial interface transfer clock can be created by using the timer output signal.

■Serial Interface Transfer Clock Operation by 8-bit Timer (Timer 3)
Timer 3 output can be used as a transfer clock source for serial interface 0 and serial interface 1.

Table 5-8-1 Timer for Serial Interface Transfer Clock

Serial transfer clock	Timer 3
Serial interface 0	√
Serial interface 1	√

■Timing of Serial Interface Transfer Clock (Timer 3)

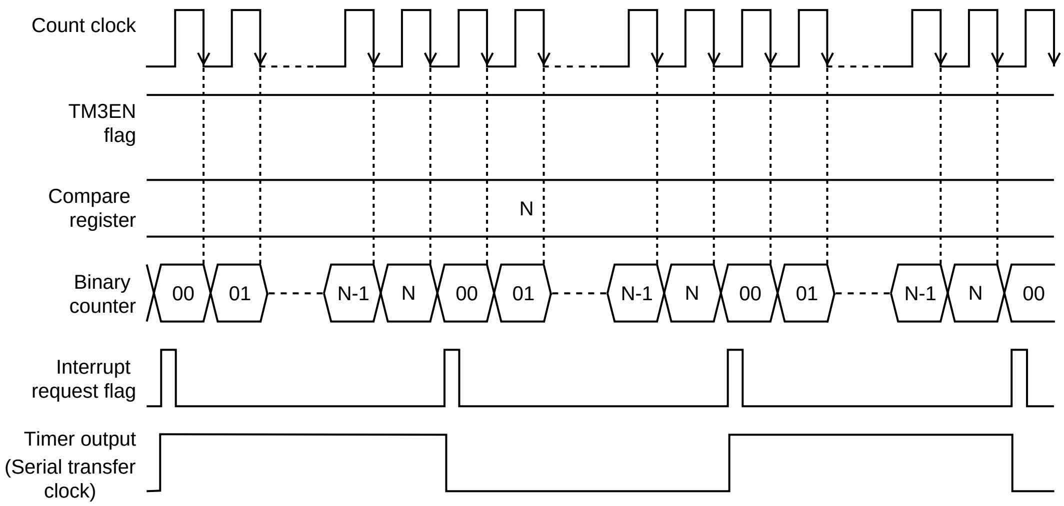


Figure 5-8-1 Timing of Serial Interface Transfer Clock (Timer 3)

The timer pulse output is used as the clock source of the serial interface. And its frequency is 1/2 of the set frequency in the timer compare register.
The count timing is same to the timing of timer operation. For the baud rate calculation and the serial interface setup, [☞ Chapter 10. Serial Interface 0]

5-8-2 Setup Example

■Serial Interface Transfer Clock Setup Example (Timer 0 and Timer 3)
How to create a transfer clock for half duplex UART (serial interface 0) using with timer 3 is shown below. The baud rate is selected to be 300 bps, the source clock of timer 3 is selected to be fs/4 (at fosc=8 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM3MD (x'3F83') bp4 :TM3EN = 0	(1) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop timer 3 counting.
(2) Select the normal timer operation. TM3MD (x'3F83') bp3 :TM3PWM = 0	(2) Set the TM3PWM flag of the TM3MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM3MD (x'3F83') bp2-0 :TM3CK2-0 = 001	(3) Select the clock source to fs/4 by the TM3CK2-0 flag of the TM3MD register.
(4) Set the baud rate. TM3OC (x'3F73') = x'CF'	(4) Set the timer 3 compare register (TM3OC) to the value that baud rate comes to 300 bps. [☞ Chapter 10. Table 10-3-18] At that time, the timer 3 binary counter (TM3BC) is initialized to x'00'.
(5) Start the timer operation TM3MD (x'3F83') bp4 :TM3EN = 1	(5) Set the TM3EN flag of the TM3MD register to "1" to start timer 3.

TM3BC counts up from x'00'. Timer 3 output is the clock of the serial interface 0 at transmission and reception.

For the compare register setup value and the serial interface operation setup, [☞ Chapter 10. Serial Interface 0]

5-9 Cascade Connection

5-9-1 Operation

Cascading timer 2 and 3 form a 16-bit timer.

■8-bit Timer Cascade Connection Operation (Timer 2 + Timer 3)
Timer 2 and timer 3 are combined to be a 16-bit timer. Cascading timer is operated at clock source of timer 2 which are lower 8 bits.

Table 5-9-1 Timer Functions at Cascade Connection

	Timer 2 + Timer 3 (16 Bit)
Interrupt source	TM3IRQ
Timer operation	√
Event count	√ (TM2IO input)
Timer pulse output	√ (TM3IO output)
PWM output	-
Synchronous output	-
Serial interface transfer clock output	√ (TM3IO output)
Remote control carrier output	√
Clock source	fs fs/4 fx TM2IO input
fosc : Machine clock (High speed oscillation) fx : Machine clock (Low speed oscillation) fs : System clock (at NORMAL mode : fs=fosc/2, at SLOW mode : fs=fx/4)	

At cascade connection, the binary counter and the compare register are operated as a 16 bit register. At operation, set the TMnEN flag of the upper and lower 8-bit timers to "1" to be operated.
Also, the clock source is the one which is selected in the lower 8-bit timer.
Other setup and count timing is the same to the 8-bit timer at independently operation.

When timer 2 and timer 3 are used in cascade connection, timer 3 interrupt request flag is used. Disable the timer 2 interrupt. Timer pulse output of timer 2 is "L" fixed output.

At the cascade connection, if the binary counter should be cleared by rewriting the compare register, the TMnEN flags of the lower and upper 8 bits timers mode registers should be set to "0" to stop the counting, then rewrite the compare register.
Also, set the (TM3OC + TM2OC) register by the 16-bit access instruction.

5-9-2 Setup Example

■Cascade Connection Timer Setup Example (Timer 2 + Timer 3)
Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 2 and timer 3, as a 16-bit timer is shown. An interrupt is generated in every 2500 cycles (1 ms) by selecting source clock to fs/4 (fosc=20 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM2MD (x'3F82') bp4 :TM2EN = 0 TM3MD (x'3F83') bp4 :TM3EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0", the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop timer 2 and timer 3 counting.
(2) Select the normal operation of lower timer . TM2MD (x'3F82') bp3 :TM2PWM = 0	(2) Set both of the TM2PWM flag of the TM2MD register to "0" to select the normal operation of timer 2.
(3) Set the cascade connection. TM3MD (x'3F83') bp2-0 :TM3CK2-0 = 100	(3) Connect timer 2 and timer 3 in cascade connection by the TM3CK2-0 flag of the TM3MD register.
(4) Select the count clock source. TM2MD (x'3F82') bp2-0 :TM2CK2-0 = 001	(4) Set the clock source to fs/4 by the TM2CK2-0 flag of the TM2MD register.
(5) Set the interrupt generation cycle TMnOC(x'3F73', x'3F72')=x'09C3'	(5) Set the timer 3 compare register + timer 2 compare register (TM3OC + TM2OC) to the interrupt generation cycle (x'09C3' : 2500 cycles - 1). At that time, timer 3 binary counter + timer 2 binary counter (TM3BC + TM2BC) are initialized to x'0000'.
(6) Disable the lower timer interrupt. TM2ICR (x'3FE4') bp1 :TM2IE = 0	(6) Set the TM2IE flag of the timer 2 interrupt control register (TM2ICR) to "0" to disable the interrupt.

Setup Procedure	Description
(7) Set the level of the upper timer interrupt. TM3ICR (x'3FEE') bp7-6 :TM3LV1-0 = 10	(7) Set the interrupt level by the TM3LV1-0 flag of the timer 3 interrupt control register (TM3ICR). If any interrupt request flag had already been set, clear it.
(8) Enable the upper timer interrupt. TM3ICR (x'3FEE') bp1 :TM3IE = 1	(8) Set the TM3IE flag of the TM3ICR register to "1" to enable the interrupt. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Start the upper timer operation. TM3MD (x'3F83') bp4 :TM3EN = 1	(9) Set the TM3EN flag of the TM3MD register to "1" to start timer 3.
(10) Start the lower timer operation. TM2MD (x'3F82') bp4 :TM2EN = 1	(10) Set the TM2EN flag of the TM2MD register to "1" to start timer 2.

TM3BC + TM2BC counts up from x'0000' as a 16-bit timer. When TM3BC + TM2BC reaches the set value of TM3OC + TM2OC register, the timer 3 interrupt request flag is set to "1" at the next count clock, and the value of TM3BC + TM2BC becomes x'0000' and counting up is restarted.

Use a 16-bit access instruction to set the (TM3OC + TM2OC) register.

If the lower timer starts to operate before the upper timer does, the first overflow signal of the lower timer may be invalid. To prevent this, start the upper timer operation before the lower timer operation.

5-10 Remote Control Carrier Output

5-10-1 Operation

Carrier pulse for remote control can be generated.

■Operation of Remote Control Carrier Output (Timer 3)
Remote control carrier pulse is based on output signal of timer 3. Duty cycle is selected from 1/2, 1/3. RMOUT (P10) outputs remote control carrier output signal.

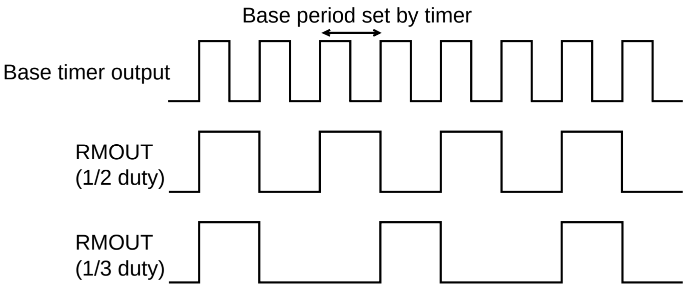


Figure 5-10-1 Duty Cycle of Remote Control Carrier Output Signal

■Count Timing of Remote Control Carrier Output (Timer 3)

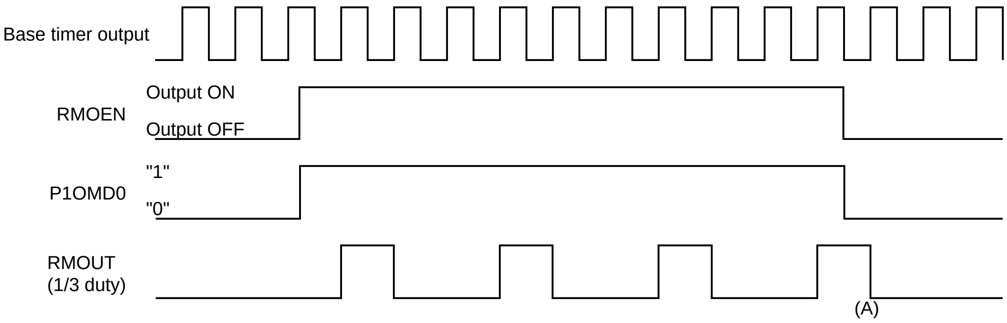


Figure 5-10-2 Count Timing of Remote Control Carrier Output Function (Timer 3)

(A) Even if the RMOEN flag is off when the carrier output is high, the carrier waveform is held by the synchronizing circuit.

> When the RMOEN flag is switched to on, set the P10TCO flag of the P1OMD register to "1". When it is switched to off, set it to "0".

> When the RMOEN flag is changed, do not change the base cycle and its duty at the same time. If they are changed at the same time, the carrier wave form is not output properly.

5-10-2 Setup Example

■Remote Control Carrier Output Setup Example (Timer 3)
Here is the setting example that the RMOUT pin outputs the 1/3 duty carrier pulse signal with "H" period of 36.7 kHz, by using timer 3. The source clock of timer 3 is set to fosc (at 8 MHz).
An example setup procedure, with a description of each step is shown below.

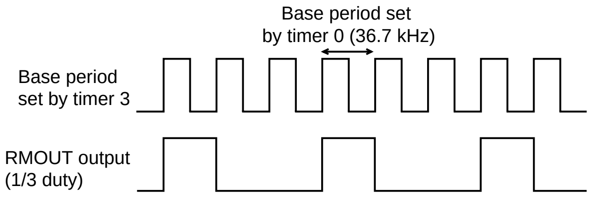


Figure 5-10-3 Output Wave Form of RMOUT Output Pin

Setup Procedure	Description
(1) Disable the remote control carrier output. RMCTR (x'3F89') bp3 : RMOEN = 0	(1) Set the RMOEN flag of the remote control carrier output control register (RMCTR) to "0" to disable the remote control carrier output.
(2) Select the carrier output duty. RMCTR (x'3F89') bp1 : RMDTY0 = 1	(2) Set the RMDTY0 flag of the RMCTR register to "1" to select 1/3 duty.
(3) Stop the counter. TM3MD (x'3F83') bp4 : TM3EN = 0	(3) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop the timer 3 counting.
(4) Set the remote control carrier output of the special function pin. P1OUT (x'3F11') bp0 : P1OUT0 = 0 P1OMD (x'3F39') bp0 : P1OTC0 = 1 P1DIR (x'3F31') bp0 : P1DIR0 = 1	(4) Set the P1OUT0 flag of the port 1 output register (P1OUT) to "0" to set the output data of P10 pin to "0. Set the P1OTC0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin as a special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" for output mode.
(5) Select the normal timer operation. TM3MD (x'3F83') bp3 : TM3PWM = 0	(5) Set the TM3PWM flag of the TM3MD register to "0" to select normal timer operation.

Setup Procedure	Description
(6) Select the count clock source. TM3MD (x'3F83') bp2-0 : TM3CK2-0 = 000	(6) Select fosc to clock source by the TM3CK2-0 flag of the TM3MD register.
(7) Set the base cycle of remote control carrier. TM3OC (x'3F73') = x'6C'	(7) Set the base cycle of remote control carrier by writing x'6C' to the timer 3 compare register (TM3OC). The set value should be (8 MHz/ 73.4 kHz) - 1 = 108(x'6C') 8 MHz is divided to be 73.4 kHz, 2 times 36.7 kHz.
(8) Start the timer operation. TM3MD (x'3F83') bp4 : TM3EN = 1	(8) Set the TM3EN flag of the TM3MD register to "1" to stop the timer 3 counting.
(9) Enable the remote control carrier output. RMCTR (x'3F89') bp3 : RMOEN = 1	(9) Set the RMOEN flag of the RMCTR register to "1" to enable the remote control carrier output.

TM3BC counts up from x'00'. Timer 3 outputs the base cycle pulse set in TM3OC. Then, the 1/3 duty remote control carrier pulse signal is output. If the RMOEN flag of the RMCTR register is set to "0", the remote control carrier pulse signal output is stopped.

Chapter 6 16-bit Timer

6-1 Overview

This LSI contains a general-purpose 16-bit timer (Timer 4).

6-1-1 Functions

Table 6-1-1 shows the functions of timer 4 can use.

Table 6-1-1 16-bit Timer Functions

	Timer 4 (16-bit timer)
Interrupt source	TM4IRQ
Timer operation	√
Event count	√
Timer pulse output	√
PWM output (Added Pulse Type)	√
Synchronous output	√
Capture function	√
Clock source	fosc fs/4 fs/16 TM4IO input
fosc : Machine clock (High speed oscillation) fs : System clock (at NORMAL mode : fs=fosc/2, at SLOW mode : fs=fx/4)	

6-1-2 Block Diagram

■Timer 4 Block Diagram

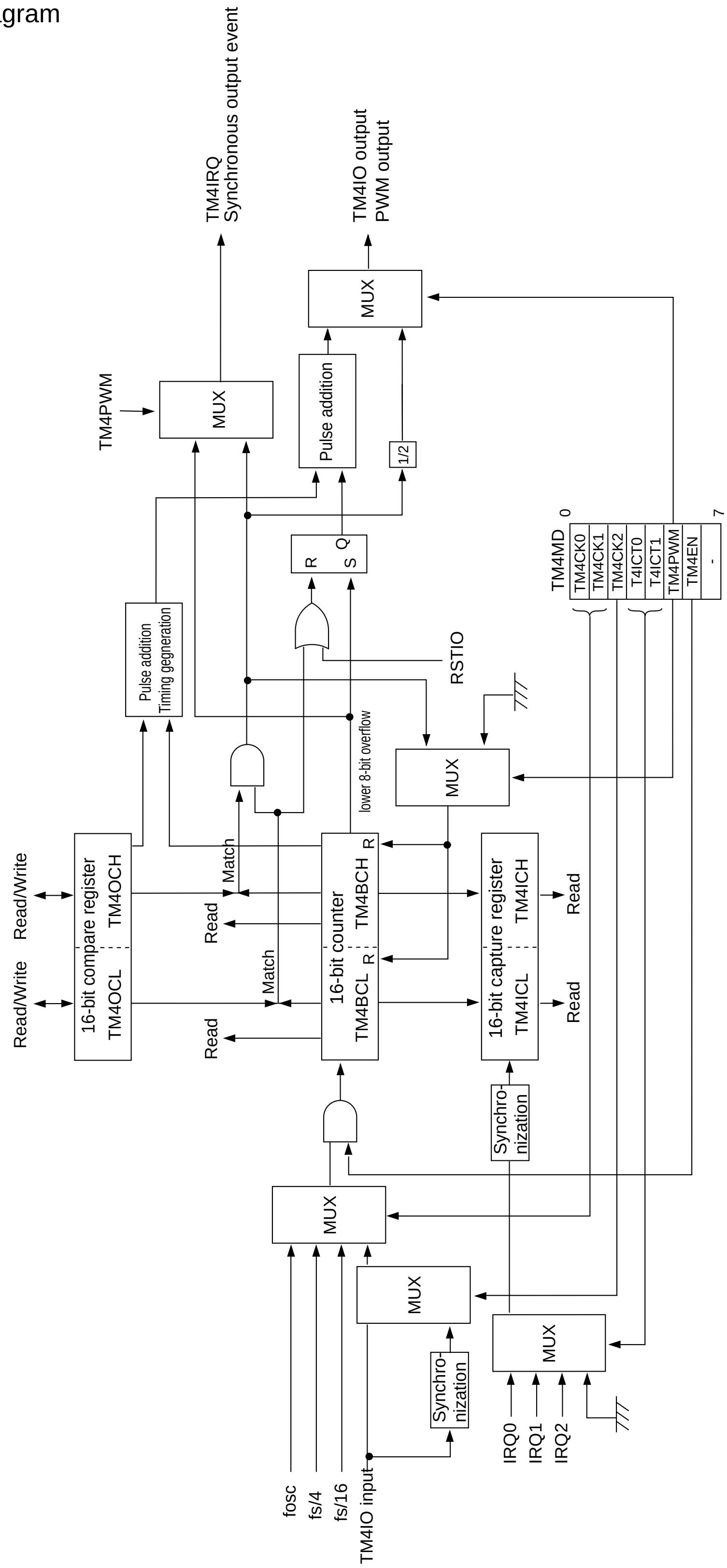


Figure 6-1-1 Timer 4 Block Diagram

6-2 Control Registers

Timer 4 contains the binary counter (TM4BCL/TM4BCH), the compare register (TM4OCL/TM4OCH) and input capture register (TM4ICL/TM4ICH). The timer 4 mode register (TM4MD) controls timer 4.

6-2-1 Registers

Table 6-2-1 shows the registers that control timer 4.

Table 6-2-1 16-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 4	TM4BCL	x'03F64'	R	Timer 4 binary counter (lower 8 bits)	VI - 5
	TM4BCH	x'03F65'	R	Timer 4 binary counter (upper 8 bits)	VI - 5
	TM4OCL	x'03F74'	R/W	Timer 4 compare register (lower 8 bits)	VI - 5
	TM4OCH	x'03F75'	R/W	Timer 4 compare register (upper 8 bits)	VI - 5
	TM4ICL	x'03F66'	R	Timer 4 input capture regsiter (lower 8 bits)	VI - 6
	TM4ICH	x'03F67'	R	Timer 4 input capture register (upper 8 bits)	VI - 6
	TM4MD	x'03F84'	R/W	Timer 4 mode register	VI - 7
	TM4ICR	x'03FEF'	R/W	Timer 4 interrupt register (timer 4 compare match)	III - 24
	P1OMD	x'03F39'	R/W	Port 1 output mode register	IV - 14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 13

R/W : Readable/Writable
R : Readable only

6-2-2 Programmable Timer Registers

Timer 4 has a 16-bit programmable timer register. It contains a compare register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate by 16-bit access.

Compare register is a 16-bit register stores the value that compared to binary counter.

■Timer 4 Compare Register (TM4OC)

	7	6	5	4	3	2	1	0	
TM4OCL	TM4OCL7	TM4OCL6	TM4OCL5	TM4OCL4	TM4OCL3	TM4OCL2	TM4OCL1	TM4OCL0	(At reset : X X X X X X X X)

Figure 6-2-1 Timer 4 Compare Register Lower 8 bits (TM4OCL : x'03F74', R/W)

	7	6	5	4	3	2	1	0	
TM4OCH	TM4OCH7	TM4OCH6	TM4OCH5	TM4OCH4	TM4OCH3	TM4OCH2	TM4OCH1	TM4OCH0	(At reset : X X X X X X X X)

Figure 6-2-2 Timer 4 Compare Register Upper 8 bits (TM4OCH : x'03F75', R/W)

Binary counter is a 16-bit up counter. If any data is written to a compare register during counting is stopped, the binary counter is cleared to x'0000'.

■Timer 4 Binary Counter (TM4BC)

	7	6	5	4	3	2	1	0	
TM4BCL	TM4BCL7	TM4BCL6	TM4BCL5	TM4BCL4	TM4BCL3	TM4BCL2	TM4BCL1	TM4BCL0	(at reset : 0 0 0 0 0 0 0 0)

Figure 6-2-3 Timer 4 Binary Counter Lower 8 bits (TM4BCL : x'03F64', R)

	7	6	5	4	3	2	1	0	
TM4BCH	TM4BCH7	TM4BCH6	TM4BCH5	TM4BCH4	TM4BCH3	TM4BCH2	TM4BCH1	TM4BCH0	(at reset : 0 0 0 0 0 0 0 0)

Figure 6-2-4 Timer 4 Binary Counter Upper 8 bits (TM4BCH : x'03F65', R)

Input capture register is a register that holds the value loaded from a binary counter by capture trigger. Capture trigger is generated by an input signal from an external interrupt pin (Directly writing to the register by program is disable.).

■Timer 4 Input Capture Register (TM4IC)

	7	6	5	4	3	2	1	0	
TM4ICL	TM4ICL7	TM4ICL6	TM4ICL5	TM4ICL4	TM4ICL3	TM4ICL2	TM4ICL1	TM4ICL0	(At reset : X X X X X X X X)

Figure 6-2-5   Timer 4 Input Capture Register Lower 8 bits (TM4ICL : x'03F66', R)

	7	6	5	4	3	2	1	0	
TM4ICH	TM4ICH7	TM4ICH6	TM4ICH5	TM4ICH4	TM4ICH3	TM4ICH2	TM4ICH1	TM4ICH0	(At reset : X X X X X X X X)

Figure 6-2-6   Timer 4 Input Capture Register Upper 8 bits (TM4ICH : x'03F67', R)

6-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 4.

■Timer 4 Mode Register (TM4MD)

	7	6	5	4	3	2	1	0
TM4MD	-	TM4EN	TM4PWM	TM4ICTS1	TM4ICTS0	TM4CK2	TM4CK1	TM4CK0

(at reset : - 0 0 0 0 X X X)

TM4CK2	TM4CK1	TM4CK0	Clock source
0	0	0	fosc
		1	fs/4
	1	0	fs/16
		1	TM4IO input
1			Synchronous TM4IO input

TM4ICTS1	TM4ICTS0	Capture trigger for timer 4
0	0	Disable input capture
	1	IRQ0
1	0	IRQ1
	1	IRQ2

TM4PWM	Timer 4 operation mode
0	16-bit timer normal operation
1	PWM operation

TM4EN	Timer 4 count control
0	Disable the count
1	Enable the count

Figure 6-2-7 Timer 4 Mode Register (TM4MD : x'03F84', R/W)

6-3 16-bit Timer Count

6-3-1 Operation

Timer operation can constantly generate interrupt.

■16-bit Timer Operation (Timer 4)

The generation cycle of an timer interrupt is set by the clock source selection and the set value of the compare register (TM4OC), in advance. When the binary counter (TM4BC) reaches the set value of the compare register, the timer 4 interrupt request flag is set to "1" at the next count clock, the binary counter (TM4BC) is cleared to x'0000' and the counting up is restarted from x'0000'.

!	When the CPU reads the 16-bit binary counter (TM4BC), the read data is treated as 8-bits unit data, even if it is a 16-bit MOVW instruction. As a result, the CPU will read the data incorrectly if a carry from the lower 8 bits to the upper 8 bits occurs during counting.

Table 6-3-1 shows the clock source that can be selected.

Table 6-3-1 Clock Source at Timer Operation (Timer 4)

Clock source	1 count time
fosc	50 ns
fs/4	400 ns
fs/16	1.6 µs
as fosc = 20 MHz, fs = fosc/2 = 10 MHz	

■Count Timing of Timer Operation (Timer 4)

The binary counter counts up with the selected clock source as the count clock.

The basic operation of the whole function of 16-bit timer is as follows ;

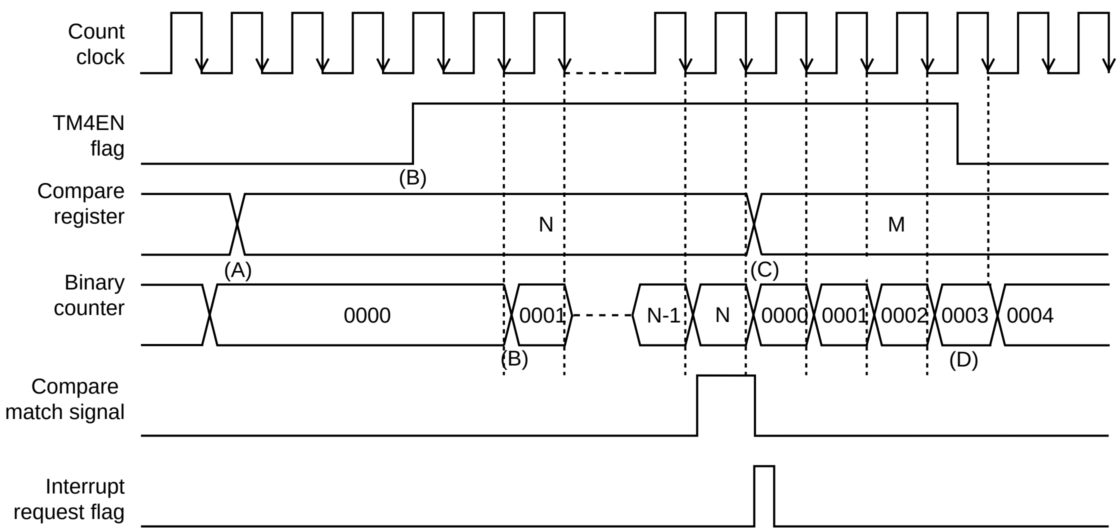


Figure 6-3-1 Count Timing of Timer Operation (Timer 4)

(A) Set the value to the timer 4 compare register (TM4OC).

(B) If the TM4EN flag is "1", the binary counter starts counting from x'0000'.
The counting is happened at the falling edge of the count clock.
But the binary counter doesn't count up at the first falling edge of the count clock.

(C) If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, and the binary counter is cleared to x'0000' to restart counting up.

(D) If the TM4EN flag is "0", the binary counter is stopped after 1 counting up.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So, set the compare register as :

Compare register setting = (count till the interrupt request - 1)

If the interrupt is enabled, the timer interrupt request flag should be cleared before timer operation is started.

If the set value of the compare register (TM4OC) is smaller than that of the binary counter (TM4BC) during the count operation, the binary counter counts up to the overflow, at first.

Even if the TM4EN flag of the timer 4 is cleared during operation, it does not stop until the next count clock. Therefore, during max. 1 count clock after the TM4EN is cleared, the binary counter cannot be initialized.

6-3-2 Setup Example

■Timer Operation Setup Example (Timer 4)

Timer 4 generates an interrupt constantly for timer function. Fosc (fosc=20 MHz at operation) is selected as a clock source to generate an interrupt every 1000 cycles (50 µs).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM4MD (x'3F84') bp6 : TM4EN = 0	(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop timer 4 counting.
(2) Select the normal timer operation. TM4MD (x'3F84') bp5 : TM4PWM = 0	(2) Set the TM4PWM flag of the TM4MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM4MD (x'3F84') bp2-0 : TM4CK2-0 = 000	(3) Select fosc as a clock source by the TM4CK2-0 flag of the TM4MD register.
(4) Set the interrupt generation cycle. TM4OC (x'3F75', x'3F74')=x'03E7'	(4) Set the interrupt generation cycle to the timer 4 compare register (TM4OC). The cycle is 1000. The set value should be 1000 - 1 = 999 (x'03E7').
(5) Set the interrupt level. TM4ICR (x'3FEF') bp7-6 : TM4LV1-0 = 10	(5) Set the interrupt level by the TM4LV1-0 flag of the timer 4 interrupt control register (TM4ICR). If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM4ICR (x'3FEF') bp1 : TM4IE = 1	(6) Set the TM4IE flag of the TM4ICR register to "1" to enable the interrupt.
(7) Start the timer operation. TM4MD (x'3F84') bp6 : TM4EN = 1	(7) Set the TM4EN flag of the TM4MD register to "1" to start timer 4.

TM4BC counts up from x'0000'. When TM4BC reaches the set value of the TM4OC register, the timer 4 interrupt request flag is set to "1" at the next count clock and the TM4BC becomes x'0000' and counts up, again.

When the TM4EN flag of the TM4MD register is changed at the same time to other bit, binary counter may count up by the switching operation.

If the value of the TM4OCH and TM4OCL register are rewritten when the timer 4 is stopped, the timer 4 binary counter becomes x'0000'.
But, even if the TM4EN flag of the operating timer is cleared to "0", it doesn't stop until the count edge of the next clock. Therefore, during max. 1 count clock after the TM4EN is cleared, the binary counter cannot be initialized.

6-4 16-bit Event Count

6-4-1 Operation

Event count operation has 2 types ; TM4IO input and synchronous TM4IO input can be selected as the count clock.

■16-bit Event Count Operation (Timer 4)

Event count means that the binary counter (TM4BC) counts the input signal from external to the TM4IO pin. If the value of the binary counter reaches the setting value of the compare register (TM4OC), interrupts can be generated at the next count clock.

Table 6-4-1 Event Count Input Clock Source

	Timer 4
Event input	TM4IO input (P14)
	Synchronous TM4IO input

■Count Timing of TM4IO Input (Timer 4)

When TM4IO input is selected, TM4IO input signal is directly input to the count clock of the timer 4. The binary counter counts up at the falling edge of the TM4IO input signal.

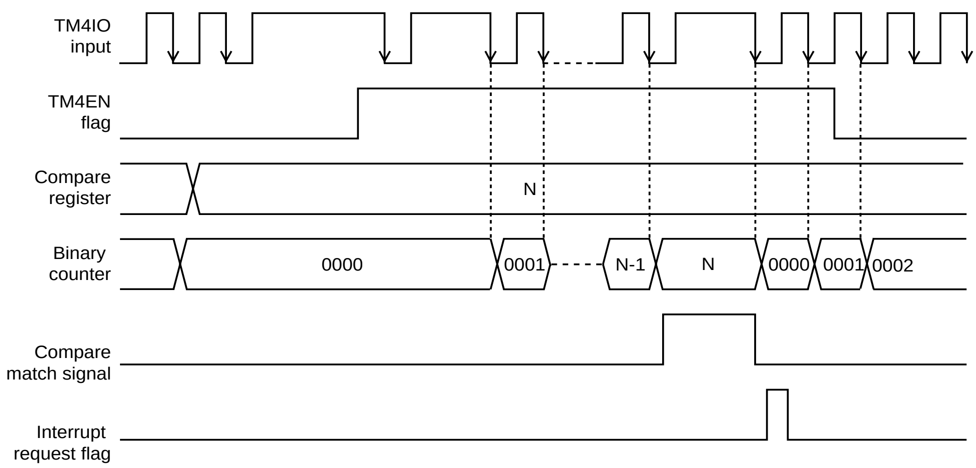


Figure 6-4-1 Count Timing TM4IO Input (Timer 4)

If the binary counter is read at operation, incorrect data at counting up may be read. To prevent this, use the event count by the synchronous TM4IO input as the following page.

■Count Timing of Synchronous TM4IO Input (Timer 4)

If the synchronous TM4IO input is selected, the synchronizing circuit output signal is input to the count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TM4IO input signal is changed. The binary counter counts up at the falling edge of the synchronizing circuit output signal or the synchronizing circuit output signal that passed through the divide-by circuit.

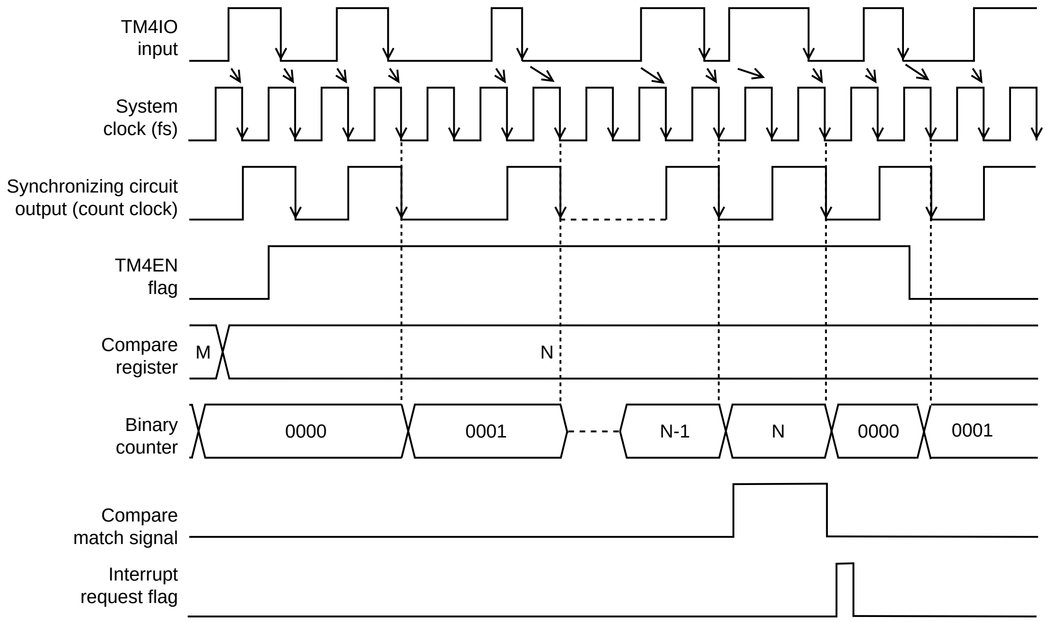


Figure 6-4-2 Count Timing of Synchronous TM4IO Input (Timer 4)

When the synchronous TM4IO input is selected as the count clock source, the timer 4 counter counts up in synchronization with system clock, therefore the correct value is always read.
But, if the synchronous TM4IO is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

6-4-2 Setup Example

■Event Count Setup Example (Timer 4)

If the falling edge of the TM4IO input pin signal is detected 5 times using timer 4, an interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM4MD (x'3F84') bp6 : TM4EN = 0	(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop timer 4 counting.
(2) Select the normal timer operation. TM4MD (x'3F84') bp5 : TM4PWM = 0	(2) Set the TM4PWM flag of the TM4MD register to "0" to select the normal timer operation.
(3) Set the special function pin to input mode. P1DIR (x'3F31') bp4 : P1DIR4 = 0	(3) Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "0" to set P14 pin to input mode. If it needs, pull up resistor should be added. [☞ Chapter 4 I/O Ports]
(4) Select the count clock source. TM4MD (x'3F84') bp2-0 : TM4CK2-0 = 011	(4) Select the TM4IO input as a clock source by the TM4CK2-0 flag of the TM4MD register.
(5) Set the interrupt generation cycle. TM4OC (x'3F75', x'3F74')=x'0004'	(5) Set the interrupt generation cycle to the timer 4 compare register (TM4OC). The set value should be 4, because the counting is 5 times.
(6) Set the interrupt level. TM4ICR (x'3FEF') bp7-6 :TM4LV1-0 = 10	(6) Set the interrupt level by the TM4LV1-0 flag of the timer 4 interrupt control register (TM4ICR). If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]

Setup Procedure	Description
(7) Enable the interrupt. TM4ICR (x'3FEF') bp1 : TM4IE = 1	(7) Set the TM4IE flag of the TM4ICR register to "1" to enable interrupt.
(8) Start the event count. TM4MD (x'3F84') bp6 : TM4EN = 1	(8) Set the TM4EN flag of the TM4MD register to "1" to start timer 4.

Every time TM4BC detects the falling edge of TM4IO input, TM4BC counts up from 'x0000'. When TM4BC reaches the setting value of theTM4OC register, the timer 4 interrupt request flag is set at the next count clock, then the value of TM4BC becomes x'0000' and counting up is restarted.

6-5 16-bit Timer Pulse Output

6-5-1 Operation

TM4IO pin can output a pulse signal with any frequency.

■Operation of 16-bit Timer Pulse Output (Timer 4)
The timers can output 2 × cycle signal, compared to the setting value in the compare register (TM4OC).
Output pins are as follows ;

Table 6-5-1 Timer Pulse Output Pin

	Timer 4
Pulse output pin	TM4IO output (P14)

■Count Timing of Timer Pulse Output (Timer 4)

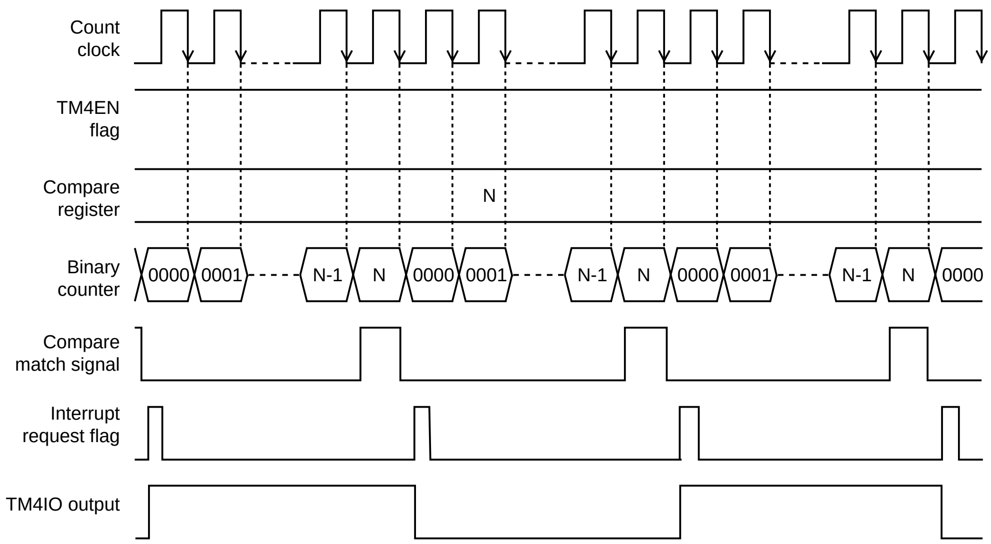


Figure 6-5-1 Count Timing of Timer Pulse Output (Timer 4)

The TM4IO pin outputs 2 × cycle, compared to the value in the compare register. If the binary counter reaches the compare register, and the binary counter is cleared to x'0000', TM4IO output (timer output) is inverted. The inversion of the timer output is changed at the rising edge of the count clock. This is happened to form the waveform inside to correct the output cycle.

In the initial state after releasing reset, the timer pulse output is low output.

6-5-2 Setup Example

■Timer Pulse Output Setup Example (Timer 4)

TM4IO pin outputs 50 kHz pulse by using timer 4. For this, select fosc as clock source, and set a 1/2 cycle (100 kHz) for the timer 4 compare register (at fosc=20 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM4MD (x'3F84') bp6 : TM4EN = 0	(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop timer 4 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F39') bp4 : P14TCO = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P14TCO flag of the port 1 output mode register (P1OMD) to "1" to set P14 pin as the special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. If it needs, pull-up resister should be added. [☞ Chapter 4 I/O Ports]
(3) Select the normal timer operation. TM4MD (x'3F84') bp5 : TM4PWM = 0	(3) Set the TM4PWM flag of the timer 4 mode register (TM4MD) to "0" to select the normal timer operation.
(4) Select the count clock source. TM4MD (x'3F84') bp2-0 : TM4CK2-0 = 000	(4) Select fosc as a clock source by the TM4CK1-0 flag of the TM4MD register.
(5) Set the timer pulse output cycle. TM4OC (x'3F75', x'3F74')=x'00C7'	(5) Set the 1/2 frequency of the timer pulse output cycle to the timer 4 compare register (TM4OC). To be 100 kHz by a divided 20 MHz, set as follows ; 200 - 1 = 199 (x'C7')
(6) Start the timer operation. TM4MD (x'3F84') bp6 : TM4EN = 1	(6) Set the TM4EN flag of the TM4MD register to "1" to start timer 4.

TM4BC counts up from x'0000'. If TM4BC reaches the set value of the TM4OC register and TM4BC is cleared to x'0000', the signal of the TM4IO output is inverted and TM4BC counts up from x'0000', again.

Set the compare register value as follows,

$$\text{The compare register value} = \frac{\text{The timer pulse output cycle}}{\text{The count clock cycle} \times 2} - 1$$

6-6 Added Pulse Type 16-bit PWM Output

6-6-1 Operation

In the added pulse method 16-bit PWM output, a 1-bit output is appended to the basic component of the 8-bit PWM output, and the output is from TM4IO. Precise 16-bit control is possible based on the number of PWM repetitions (256 times) to which this bit is appended.

■Added Pulse Type 16-bit PWM Output (Timer 4)
The lower 8 bits of the compare register (TM4OCL) set the duty ("H" period) of the basic PWM waveform and the upper 8 bits of the compare register (TC4OCH) set the added pulse position. The cycle of the basic PWM waveform is the period of the full count overflow in the lower 8 bits of the binary counter (TM4BCL). Table 6-6-1 shows the PWM output pin.

Table 6-6-1 PWM Output Pin

	Timer 4
PWM output pin	TM4IO output pin (P14)

■Added Pulse Type PWM Output (Timer 4)

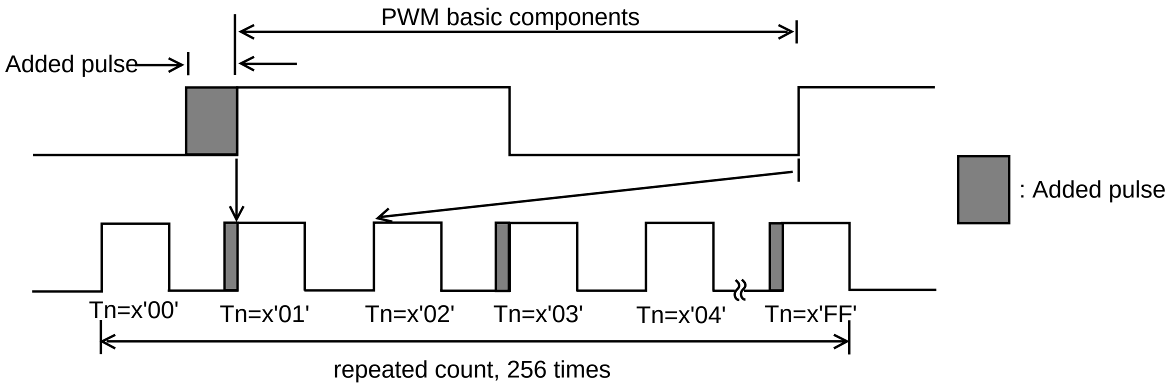


Figure 6-6-1 Added Pulse Type PWM Output

Set the P1DIR register and the P1PLU register, when the P14 pin is used as a PWM output pin.

For PWM operation, x'FF' in TM4OCL produces the same result as x'00' : constant low level output at the PWM4 pin, not constant high. Do not set x'FF' in TM4OCL.

■Setting the Added Pulse Position

The upper 8 bits of timer 4 compare register (TM4OCH) set the position of the added pulse. If the TM4OCH register is set to x'00', an additional bit is not appended to the basic PWM component. If the TM4OCH register is set to x'FF', an additional bit is repeatedly appended to the 255 basic PWM components during the cycle. The relation between the value set in the TM4OCH register and the position of the added pulse is shown in the table below.

In the TM4OCH register, the position of the added pulse (the value of Tn) depends which bit has "1". And the number of the setting value in TM4OCH is the number of bits to be added. For example, if x'03' is set in the TM4OCH register (set "1" in bp0 and bp1), bits are appended to pulse positions for x'01' (Tn=x'80") and x'02' (Tn=x'40', x'C0'), shown in the below table.

The setting value of TM4OCH	Position of the added pulse (the value of Tn)
0 0 0 0 0 0 0 0 (x'00')	none
0 0 0 0 0 0 0 1 (x'01')	x'80'
0 0 0 0 0 0 1 0 (x'02')	x'40',x'C0'
0 0 0 0 0 1 0 0 (x'04')	x'20',x'60',x'A0',x'C0'
0 0 0 0 1 0 0 0 (x'08')	x'10',x'30',x'50',x'70',x'90',x'B0',x'D0',x'F0'
0 0 0 1 0 0 0 0 (x'10')	x'08',x'18',x'28',x'38',x'48',x'58',- - - - - ,x'E8',x'F8'
0 0 1 0 0 0 0 0 (x'20')	x'04',x'0C',x'14',x'1C',x'24',x'2C,- - - - - ,x'F4',x'FC'
0 1 0 0 0 0 0 0 (x'40')	x'02',x'06',x'0A',x'0E',x'12',x'16,- - - - - ,x'FA',x'FE'
1 0 0 0 0 0 0 0 (x'80')	x'01',x'03',x'05',x'07',x'09',x'0B,- - - - - ,x'FD',x'FF'
(bp7) (bp0)	

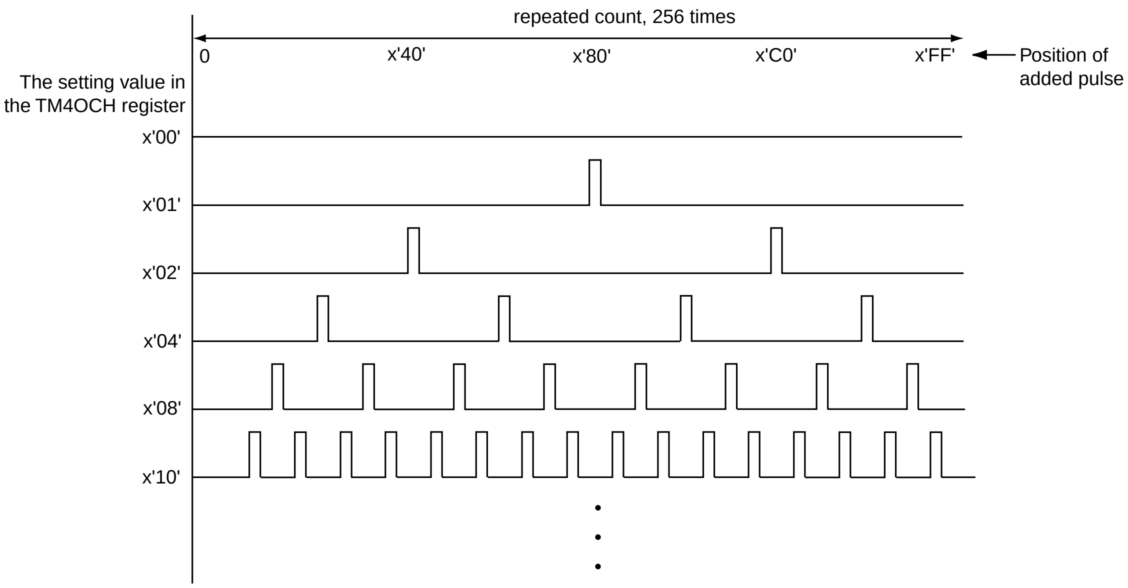


Figure 6-6-2 The Setting Value in The TM4OCH Register and The Position of The Added Pulse

6-6-2 Setup Example

■Added Pulse Type 16-bit PWM Output Setup Example (Timer 4)
The TM4IO output pin outputs the 1/4 duty (64 :192) PWM output waveform at 78.125 kHz with timer 4. In the PWM output repetitions (256 times), the added pulse is appended 7 times and the duty becomes 65 : 191. The high frequency oscillation (fosc) is set to be operated at 20 MHz.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM4MD (x'3F84') bp6 : TM4EN = 0	(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop timer 4 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F39') bp4 : P14TCO = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P14TCO flag of the port 1 output mode register (P1OMD) to "1" to set the P14 pin as a special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. If it needs, pull-up resister should be added. [☞ Chapter 4 I/O Ports]
(3) Select the count clock source. TM4MD (x'3F84') bp2-0 : TM4CK2-0 = 000	(3) Select fosc as a clock source by the TM4CK2-0 flag of the TM4MD register.
(4) Set the PWM operation. TM4MD (x'3F84') bp5 : TM4PWM = 1	(4) Set the TM4PWM flag of the timer 4 mode register (TM4MD) to "1" to select the PWM operation.
(5) Set the PWM output "H" period and the location of the added pulse. TM4OC(x'3F75', x'3F74') = x'0740'	(5) Set the "H" period of the PWM output in the lower 8 bits of the timer 4 compare register (TM4OCL). To be 1/4 duty of the full count 256 of the lower 8 bits in the timer 4 binary counter (TM4BCL), the setting value should be 256 / 4 = 64 (x'40'). Also set the location of the added pulse in the upper 8 bits of the compare register. If it is set to x'07', the added pulse is appended 7 times in 256 repetitions.

Setup Procedure	Description
(6) Start the timer operation. TM4MD (x'3F84') bp6 : TM4EN = 1	(6) Set the TM4EN flag of the TM4MD register to "1" to start timer 4.

TM4BCL counts up from x'00'. The PWM source waveform outputs "H" until TM4BCL reaches the set value of the TM4OCL register, then, after the match it outputs "L". After that, TM4BCL continues to count up, once a overflow happens, the PWM source waveform outputs "H" again, and TM4BCL counts up from x'00', again.

From the above setting, the basic PWM waveform becomes 64 : 192. And the TM4OCH is set to x'07', in the PWM output repetitions (256 times), the added pulse is appended 7 times and the duty becomes 65 : 191.

For PWM operation, x'FF' in TM4OCL produces the same result as x'00' : constant low level output at the PWM4 pin, not constant high. Do not set x'FF' in TM4OCL.

Use a 16-bit access instruction to set the TM4OCH, TM4OCL register.

6-7 16-bit Timer Synchronous Output

6-7-1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latched data is output from port 7 at the next count clock.

■Synchronous Output Operation by 16-bit timer (Timer 4)
The port 7 latched data is output from the output pin at the interrupt request generation by the match of the binary counter (TM4OC) and the compare register.
Only port 7 can perform synchronous output operation, and individual pins can be set.

■Count Timing of Synchronous Output (Timer 4)

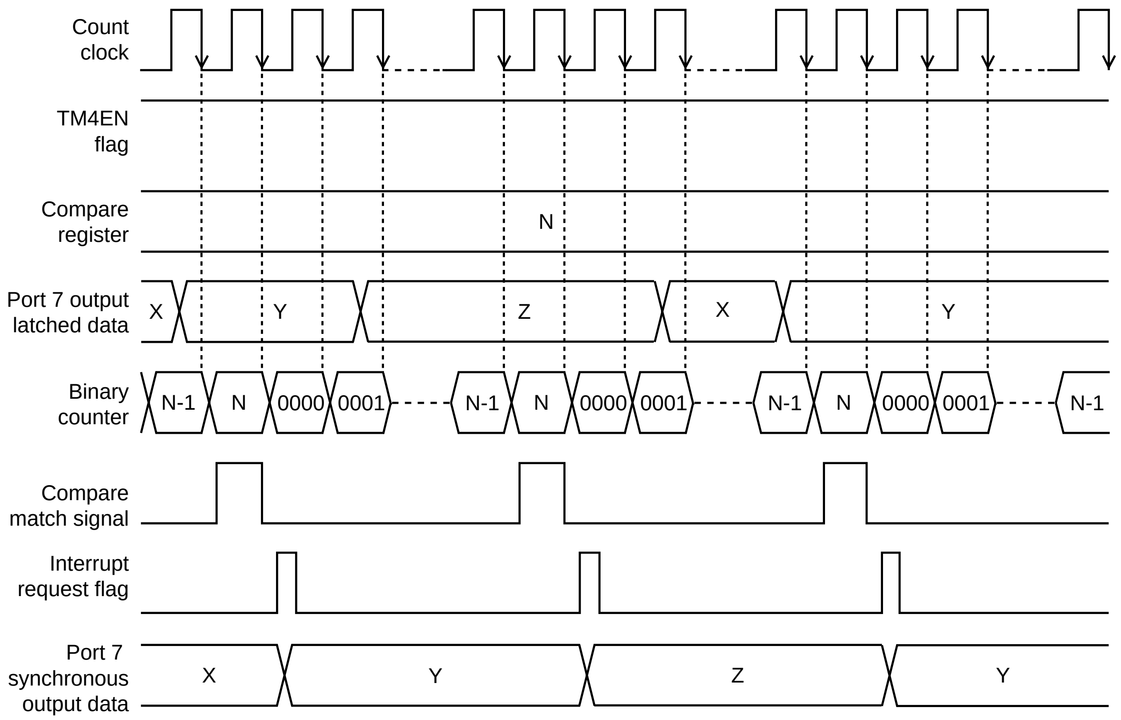


Figure 6-7-1 Count Timing of Synchronous Output (Timer 4)

The port 7 latched data is output from the output pin in synchronization with the interrupt request generation by the match of binary counter and compare register.

Even if the port 7 is used as a synchronous output pin, the setting of the P7DIR register is necessary.

6-7-2 Setup Example

■Synchronous Output Setup Example (Timer 4)
Setup example that latched data of port 7 is output constantly (100 μs) by using timer 4 from the synchronous output pin is shown below. The clock source of timer 4 is selected fs/4 (at fosc=8 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM4MD (x'3F84') bp6 : TM4EN = 0	(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop timer 4 counting.
(2) Select the synchronous output event. FLOAT2 (x'3F4C') bp1-0 : P7SYEVS2-1 = 01	(2) Set the P7SYEVS2-1 flag of the pin control register 2 (FLOAT2) to "01" to set the synchronous output event to the timer 4 interrupt.
(3) Set the synchronous output pin. SYSMD (x'3F1F') = x'FF' P7DIR (x'3F37') = x'FF'	(3) Set the synchronous output control register (SYSMD) to x'FF' to set the synchronous output pin. (P77 to P70 : Synchronous output pin) Set the port 7 direction control register (P7DIR) to x'FF' to set port 7 to output pin. If it needs, pull up resistor should be added. [☞ Chapter 4 I/O Ports]
(4) Select the count clock source. TM4MD (x'3F84') bp2-0 : TM4CK2-0 = 001	(4) Select fs/4 as a clock source by the TM4CK2-0 flag of the TM4MD register.
(5) Select the normal timer operation. TM4MD (x'3F84') bp5 : TM4PWM = 0	(5) Set the TM4PWM flag of the TM4MD register to "0" to select the normal timer operation.
(6) Set the synchronous output event generation cycle. TM4OC (x'3F75',x'3F74')=x'0063'	(6) Set the synchronous output event generation cycle to the timer 4 compare register (TM4OC). To be 10 kHz by dividing 1 MHz, set as follows ; 100 - 1 = 99 (x'0063')
(7) Start the timer operation. TM4MD (x'3F84') bp6 : TM4EN = 1	(7) Set the TM4EN flag of the TM4MD register to "1" to start timer 4.

TM4BC counts up from x'0000'. If any data is written to the port 7 output register (P7OUT), TM4BC reaches the set value of TM4OC register and the synchronous output pin outputs data of port 7 in every time an interrupt request is generated.

When the port 7 synchronous output is disabled, the value of the synchronous output value storage register is not always same to the value of the port 7 output register (P7OUT). Therefore, the pin output may be changed at the switching from the general output to the synchronous output.

6-8 16-bit Timer Capture

6-8-1 Operation

The value of a binary counter is stored to register at the timing of the external interrupt input signal.

■Capture Operation with External Interrupt Signal as a Trigger (Timer 4)
Capture trigger of input capture function is generated at the external interrupt signal that passed through the external interrupt interface block. The capture trigger is selected by the timer 4 mode register (TM4MD) and the external interrupt control register (IRQ0ICR, IRQ1ICR, IRQ2ICR).
Here are the capture trigger to be selected and the interrupt flag setup.

Table 6-8-1 Capture Trigger

Capture trigger source	Timer 4 mode register	External interrupt n control register (IRQnICR)	Interrupt starting edge of external interrupt n
	T4ICTS1-0	REDGn (bp5)	
Disable input capture	00	-	-
IRQ0 falling edge	01(IRQ0)	0	IRQ0 falling edge
IRQ0 rising edge	01(IRQ0)	1	IRQ0 rising edge
IRQ1 falling edge	10(IRQ1)	0	IRQ1 falling edge
IRQ1 rising edge	10(IRQ1)	1	IRQ1 rising edge
IRQ2 falling edge	11(IRQ2)	0	IRQ2 falling edge
IRQ2 rising edge	11(IRQ2)	1	IRQ2 rising edge

An interrupt request and a capture trigger are generated at switching the active edge of an external interrupt by program, when the setup is as follows ;

(1) at switching the active edge from the falling to the rising, when the interrupt pin is "H" level.

(2) at switching the active edge from the rising to the falling, when the interrupt pin is "L" level.

Operate the interrupt flag with regard to the noise influence on the program.
[☞ Chapter 3 3-3-4. Programmable Active Edge Interrupt]

■Capture Count Timing at Falling Edges of External Interrupt Signal is selected as a Trigger (Timer 4)

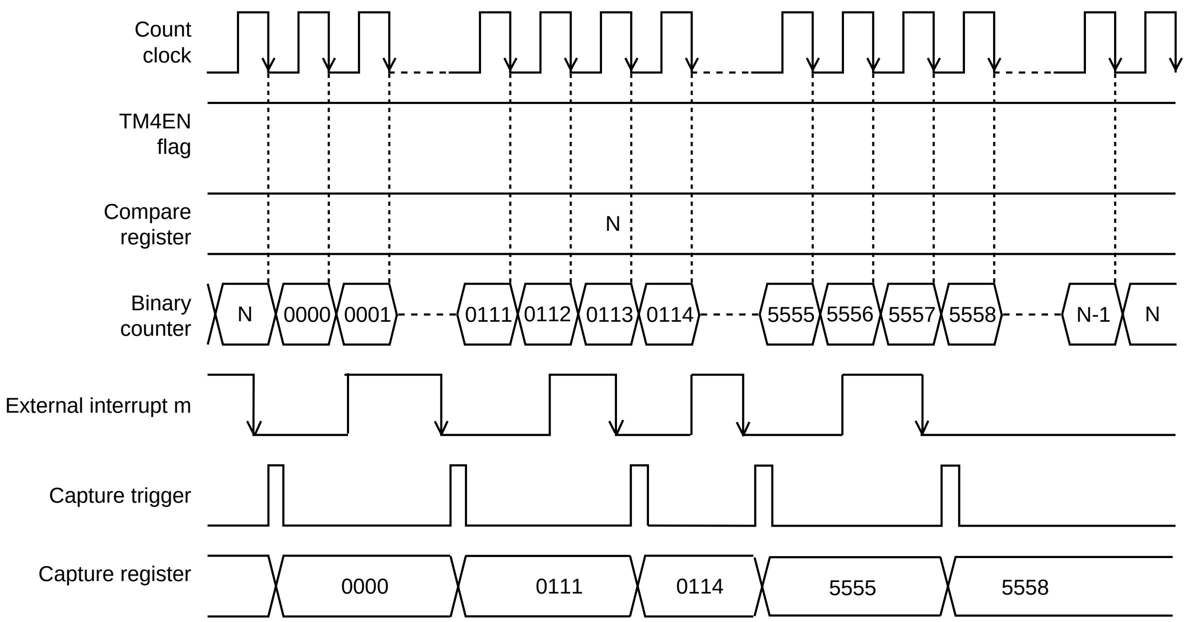


Figure 6-8-1 Capture Count Timing at an External Interrupt Signal is selected as a Trigger (Timer 4)

A capture trigger is generated at the falling edges of the external interrupt m input signal. At the same timing, the value of a binary counter is stored to the input capture register. A capture trigger is generated only at the edge that is specified as a capture trigger source. The other count timing is same to the count timing of the timer operation.

> When the binary counter is used as a free counter that counts x'0000' to x'FFFF', set the compare register to x'FFFF'.

> If a capture trigger is generated before the value of the input capture register is read, the value of the input capture register can be rewritten.

6-8-2 Setup Example

■Capture Function Setup Example (Timer 4)

Pulse width measurement is enabled by storing the value of the binary counter to the capture register at the interrupt generation edge of the external interrupt 0 input signal with timer 4. The interrupt generation edge is specified to be the rising edge.

An example setup procedure, with a description of each step is shown below.

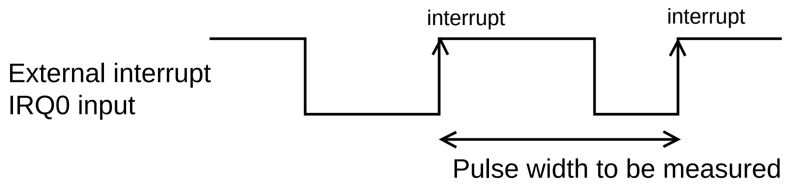


Figure 6-8-2 Pulse Width Measurement of External Interrupt 0

Setup Procedure	Description
(1) Stop the counter. TM4MD (x'3F84') bp6 : TM4EN = 0	(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop timer 4 counting.
(2) Select the count clock source. TM4MD (x'3F84') bp2-0 : TM4CK2-0 = 000	(2) Select fosc as clock source by the TM4CK2-0 flag of the TM4MD register.
(3) Select the capture trigger generation interrupt source. TM4MD (x'3F84') bp4-3 : T4ICTS1-0 = 01	(3) Select the external interrupt 0 (IRQ0) input as a generation source of capture trigger by the T4ICTS1-0 flag of the TM4MD register.
(4) Select the interrupt generation active edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(4) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as the interrupt generation active edge.
(5) Select the normal timer operation. TM4MD (x'3F84') bp5 : TM4PWM = 0	(5) Set the TM4PWM flag of the timer 4 mode register (TM4MD) to "0" to select the normal timer operation.
(6) Set the compare register. TM4OC(x'3F75',x'3F74') = x'FFFF'	(6) Set the timer 4 compare register (TM4OCH, TM4OCL) to x'FFFF'. At that time, the timer 4 binary counter (TM4BC) is initialized to x'0000'.

Setup Procedure	Description
(7) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(7) Set the interrupt level by the IRQ0LV1-0 flag of the IRQ0ICR register. If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(8) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(8) Enable the interrupt by setting the IRQ0IE flag of the IRQ0ICR register to "1".
(9) Start the timer operation. TM4MD (x'3F84') bp6 : TM4EN = 1	(9) Set the TM4EN flag of the TM4MD register to "1" to start timer 4.

TM4BC counts up from x'0000'. At the timing of the rising edge of the external interrupt 0 input signal, the value of TM4BC is stored to the TM4IC register.
At the above (7), (8), the IRQ0 interrupt is enabled, but input capture is available even if an interrupt is disabled. However, if an interrupt is enabled, the pulse width between rising edges of the external interrupt input signal can be measured by reading the value of TM4IC register by the interrupt service routine, and by calculating the margin of the capture values (the values of the TM4IC register).

Chapter 7 Time Base Timer / 8-bit Free-running Timer

7-1 Overview

This LSI has a time base timer and a 8-bit free-running timer (timer 5).
Time base timer is a 13-bit timer counter. These timers stop the timer counting only at standby mode (STOP mode).

7-1-1 Functions

Table 7-1-1 shows the clock sources and the interrupt generation cycles that timer 5 and time base timer can select.

Table 7-1-1 Clock Source and Generation Cycle

	Time base timer	Timer 5 (8-Bit free-running timer)
Timer operation	√	√
Interrupt source	TBIRQ	TM5IRQ
Clock source	fosc fx	fosc fs/4 fx fosc $\times$ $1/2^{13}$ (*1) fx $\times$ $1/2^{13}$ (*2)
Interrupt generation cycle	fosc $\times$ $1/2^{7}$ (*1) fosc $\times$ $1/2^{8}$ (*1) fosc $\times$ $1/2^{9}$ (*1) fosc $\times$ $1/2^{10}$ (*1) fosc $\times$ $1/2^{13}$ (*1) fx $\times$ $1/2^{7}$ (*2) fx $\times$ $1/2^{8}$ (*2) fx $\times$ $1/2^{9}$ (*2) fx $\times$ $1/2^{10}$ (*2) fx $\times$ $1/2^{13}$ (*2)	The interrupt generation cycle is decided by the any value written to TM5OC.

fosc : Machine clock (High speed oscillation)
fx : Machine clock (Low speed oscillation)
fs : System clock (at NORMAL mode : fs = fosc / 2, at SLOW mode : fs = fx / 4)
- *1 can be used as a clock source of time base timer is selected to 'fosc'.
- *2 can be used as a clock source of time base timer is selected to 'fx'.
- Time base timer and timer 5 cannot stop timer counting.

7-1-2 Block Diagram

■Timer 5, Time Base Timer Block Diagram

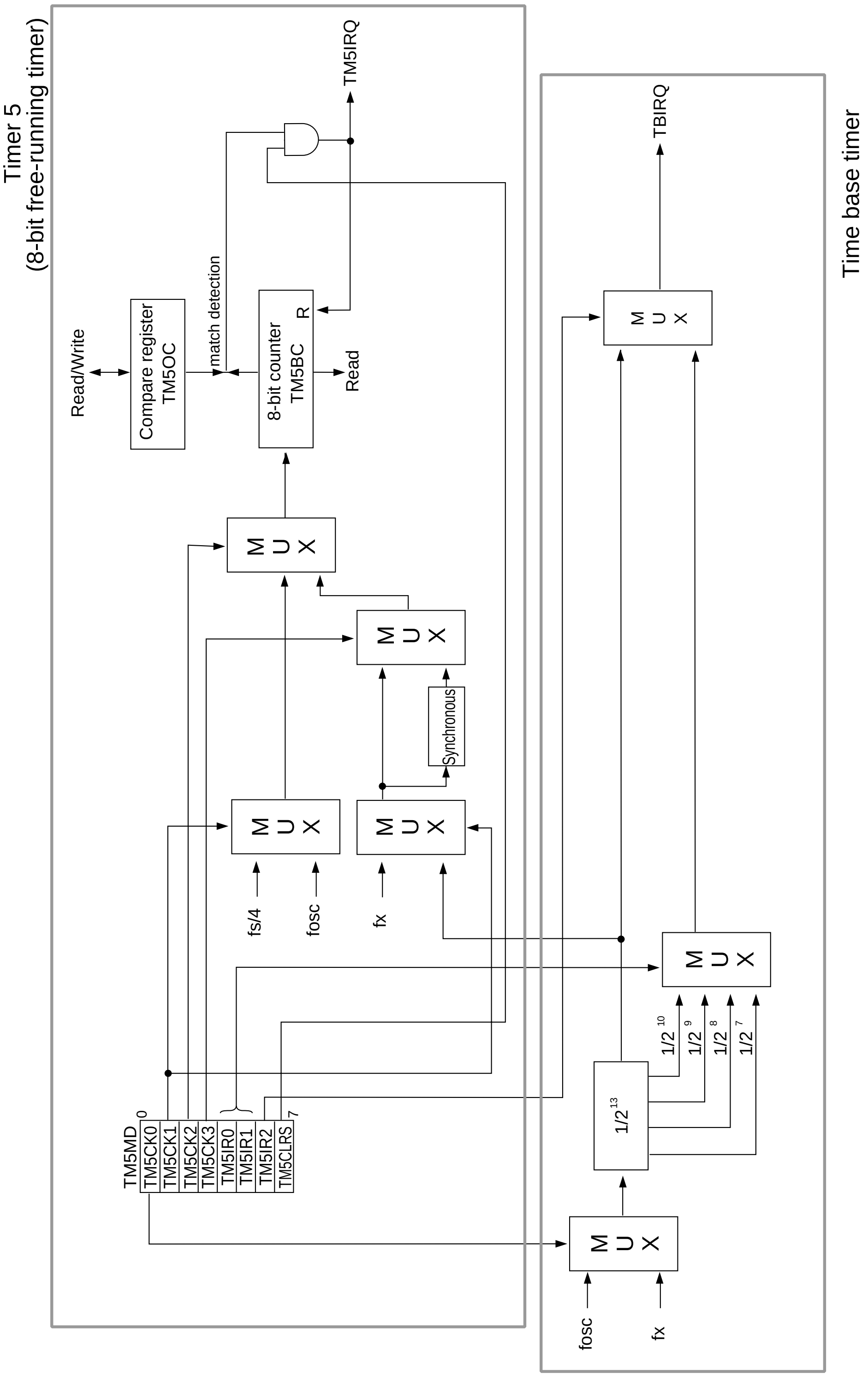


Figure 7-1-1 Block Diagram (Timer 5, Time Base Timer)

7-2 Control Registers

Timer 5 consists of binary counter (TM5BC), compare register (TM5OC), and is controlled by mode register (TM5MD). Time base timer is controlled by mode register (TM5MD), too.

7-2-1 Control Registers

Table 7-2-1 shows the registers that control timer 5, time base timer.

Table 7-2-1 Control Registers

	Register	Address	R/W	Function	Page
Timer 5	TM5BC	x'03F68'	R	Timer 5 binary counter	VII - 5
	TM5OC	x'03F78'	R/W	Timer 5 compare register	VII - 5
	TM5MD	x'03F88'	R/W	Timer 5 mode register	VII - 6
	TM5ICR	x'03FF0'	R/W	Timer 5 interrupt control register	III - 25
Timer base timer	TM5MD	x'03F88'	R/W	Timer 5 mode register	VII - 6
	TBICR	x'03FE7'	R/W	Time base interrupt control register	III - 26

R/W : Readable / Writable
R : Readable only

7-2-2 Programmable Timer Registers

Timer 5 is a 8-bit programmable counter.
Programmable counter consists of compare register (TM5OC) and binary counter (TM5BC).

Binary counter is a 8-bit up counter. When the TM5CLRS flag of the timer 5 mode register (TM5MD) is "0" and the interrupt cycle data is written to the compare register (TM5OC), the timer 5 binary counter (TM5BC) is cleared to x'00'.

■Timer 5 Binary Counter (TM5BC)

	7	6	5	4	3	2	1	0	
TM5BC	TM5BC7	TM5BC6	TM5BC5	TM5BC4	TM5BC3	TM5BC2	TM5BC1	TM5BC0	(at reset : 0 0 0 0 0 0 0 0)

Figure 7-2-1 Timer 5 Binary Counter (TM5BC : x'03F68', R)

■Timer 5 Compare Register (TM5OC)

	7	6	5	4	3	2	1	0	
TM5OC	TM5OC7	TM5OC6	TM5OC5	TM5OC4	TM5OC3	TM5OC2	TM5OC1	TM5OC0	(at reset : X X X X X X X X)

Figure 7-2-2 Timer 5 Compare Register (TM5OC : x'03F78', R/W)

7-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 5 and time base timer.

■Timer 5 Mode Register (TM5MD)

	7	6	5	4	3	2	1	0
TM5MD	TM5CLRS	TM5IR2	TM5IR1	TM5IR0	TM5CK3	TM5CK2	TM5CK1	TM5CK0

(At reset : 0 X X X X X X 0)

TM5CKS0	Time base timer clock source
0	fosc
1	fx

TM5CK3	TM5CK2	TM5CK1	Timer 5 clock source
-	0	0	fosc
		1	fs/4
0	1	0	fx
		1	Output of time base timer
1		0	Synchronous fx
		1	Synchronous output of time base timer

TM5IR2	TM5IR1	TM5IR0	Time base timer interrupt cycle selection
0	0	0	Time base selection clock × $1/2^7$
		1	Time base selection clock × $1/2^8$
	1	0	Time base selection clock × $1/2^9$
		1	Time base selection clock × $1/2^{10}$
1	X	X	Time base selection clock × $1/2^{13}$

TM5CLRS	Timer 5 binary counter clear selection
0	Enable the initialization of TM5BC as TM5OC is written
1	Disable the initialization of TM5BC as TM5OC is written

* TM5IRQ is disabled as TM5CLRS = 0,
TM5IRQ is enabled as TM5CLRS = 1.

Figure 7-2-3 Timer 5 Mode Register (TM5MD : x'03F88', R/W)

7-3 8-bit Free-running Timer

7-3-1 Operation

■8-bit Free-running Timer (Timer 5)

The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TM5OC), in advance. If the binary counter (TM5BC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then binary counter is cleared and counting is restarted from x'00'.

Table 7-3-1 shows clock source that can be selected.

Table 7-3-1 Clock Source at Timer Operation (Timer 5)

Clock source	One count time
fosc	50 ns
fs/4	400 ns
fx	30.5 µs
fosc × $1/2^{13}$	409.6 µs
fx × $1/2^{13}$	250 ms
fosc = 20(MHz) fx = 32.768(kHz) calculated as fs = fosc/2 = 10 MHz	

Timer 5 cannot stop its timer counting except at standby mode (STOP mode).

■8-bit Free-running Timer as a 1 minute-timer, a 1 second-timer

Table 7-3-2 shows the clock source selection and the TM5OC register setup, when a 8-bit free-running timer is used as a 1 minute-timer, a 1 second-timer.

Table 7-3-2 1 minute-timer, 1 second-timer Setup (Timer 5)

Interrupt Generation Cycle	Clock Source	TM5OC Register
1 min	$fx \times 1/2^{13}$	x'EF'
1 s	$fx \times 1/2^{10}$	x'1F'
	$fx \times 1/2^{13}$	x'03'
fx = 32.768 (kHz)		

When the 1 minute-timer (1 min.) is set on Table 7-3-2, the bp1 waveform frequency (cycle) of the TM5BC register is 1 Hz (1 s). So, that can be used for adjusting the seconds.

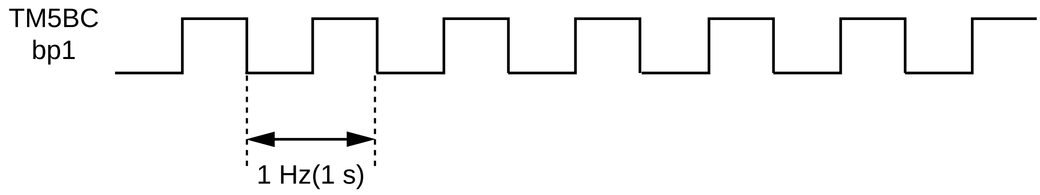


Figure 7-3-1 Waveform of TM5BC Register bp1 (Timer 5)

■Count Timing of Timer Operation (Timer 5)

Binary counter counts up with the selected clock source as a count clock.

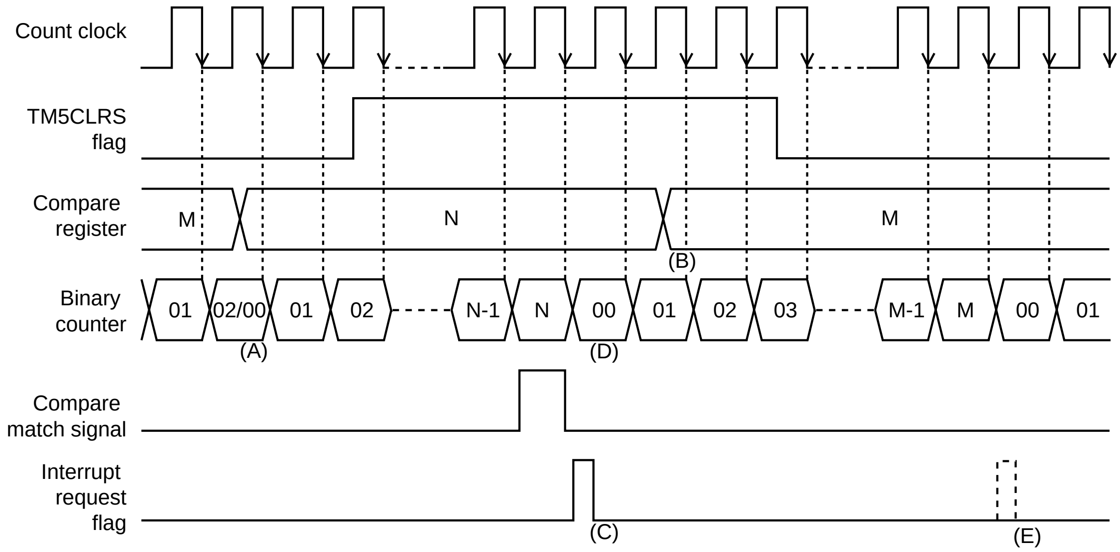


Figure 7-3-2   Count Timing of Timer Operation (Timer 5)

(A) When any data is written to the compare register as the TM5CLRS flag is "0", the binary counter is cleared to x'00'.

(B) Even if any data is written to the compare register as the TM5CLRS flag is "1", the binary counter is not changed.

(C) When the binary counter reaches the value of the compare register as the TM5CLRS flag is "1", an interrupt request flag is set at the next count clock.

(D) When an interrupt request flag is set, the binary counter is cleared to x'00' and restarts the counting.

(E) Even if the binary counter reaches the value of the compare register as the TM5CLRS flag is "0", no interrupt request flag is set.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So, set the compare register as :   Compare register setting = (count till the interrupt request - 1)

If fx is selected as the count clock source in timer 5, when the binary counter is read at operation, uncertain value on counting up may be read. To prevent this, select the synchronous fx as the count clock source.
But, if the synchronous fx is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

If the compare register is set smaller value than the binary counter's during the count operation, the binary counter counts up to the overflow, at first.

7-3-2 Setup Example

■Timer Operation Setup (Timer 5)

Timer 5 generates an interrupt constantly for timer function. fs/4 (fosc=20 MHz) is selected as a clock source to generate an interrupt every 250 dividing (100 µs).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Enable the binary counter initialization. TM5MD (x'3F88') bp7 : TM5CLRS = 0	(1) Set the TM5LRS flag of the timer 5 mode register (TM5MD) to "0". At that time, the initialization of the timer 5 binary counter (TM5BC) is enabled.
(2) Select the clock source. TM5MD (x'3F88') bp3-1 : TM5CK3-1 = 001	(2) Clock source can be selected by the TM5CK3-1 flag of the TM5MD register. Actually, fs/4 is selected.
(3) Set the interrupt generation cycle. TM5OC (x'3F78') = x'F9'	(3) Set the interrupt generation cycle to the timer 5 compare register (TM5OC). At that timer, TM5BC is initialized to x'00'.
(4) Enable the interrupt request generation. TM5MD (x'3F88') bp7 : TM5CLRS = 1	(4) Set the TM5CLRS flag of the TM5MD register to "1" to enable the interrupt request generation.
(5) Set the interrupt level. TM5ICR (x'3FF0') bp7-6 : TM5LV1-0 = 01	(5) Set the interrupt level by the TM5LV1-0 flag of the timer 5 interrupt control register (TM5ICR). If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM5ICR (x'3FF0') bp1 : TM5IE = 1	(6) Set the TM5IE flag of the TM5ICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

As TM5OC is set, TM5BC is initialized to x'00' to count up.

When TM5BC matches TM5OC, the timer 5 interrupt request flag is set at the next count clock and TM5BC is cleared to x'00' to restart counting.

If the interrupt is enabled, the timer 5 interrupt request flag should be cleared before timer 5 operation is started.

If the TM5CLRS flag of the TM5MD register is set to "0", TM5BC can be initialized in every rewriting of TM5OC register, but in that state the timer 5 interrupt is disabled. If the timer 5 interrupt should be enabled, set the TM5CLRS flag to "1" after rewriting the TM5OC register.

On the timer 5 clock source selection, either the time base timer output or the time base timer synchronous output is selected, the clock setup of time base timer is necessary.

7-4 Time Base Timer

7-4-1 Operation

■Time Base Timer (Time Base Timer)

The Interrupt is constantly generated.

Table 7-4-1 shows the interrupt generation cycle in combination with the clock source ;

Table 7-4-1 Time Base Timer Interrupt Generation Cycle

Selected clock source	Interrupt generation cycle	
fosc (= 20 MHz)	fosc $\times$ 1/2^7	6.4 µs
	fosc $\times$ 1/2^8	12.8 µs
	fosc $\times$ 1/2^9	25.6 µs
	fosc $\times$ 1/2^{10}	51.2 µs
	fosc $\times$ 1/2^{13}	409.6 µs
fosc (= 8.39 MHz)	fosc $\times$ 1/2^7	15.2 µs
	fosc $\times$ 1/2^8	30.5 µs
	fosc $\times$ 1/2^9	61.0 µs
	fosc $\times$ 1/2^{10}	122.0 µs
	fosc $\times$ 1/2^{13}	976.4 µs
fx (= 32.768 kHz)	fx $\times$ 1/2^7	3.9 ms
	fx $\times$ 1/2^8	7.8 ms
	fx $\times$ 1/2^9	15.6 ms
	fx $\times$ 1/2^{10}	31.2 ms
	fx $\times$ 1/2^{13}	250 ms

■Count Timing of Timer Operation (Time Base Timer)

The counter counts up with the selected clock source as a count clock.

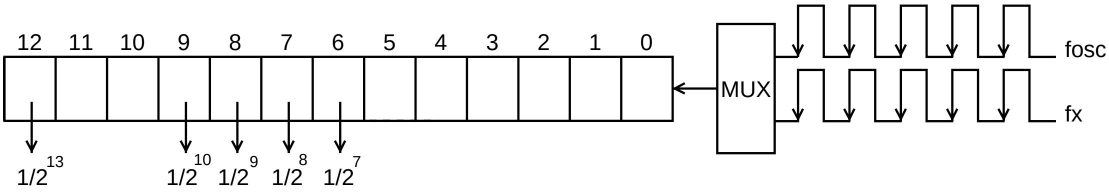


Figure 7-4-1   Count Timing of Timer Operation (Time Base Timer)

When the selected interrupt cycle has passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

An interrupt may be generated at switching of the clock source. Enable interrupt after switching the clock source.

Time base timer cannot stop the operation.

13-bit counter of time base timer can be initialized only at reset.

This LSI has built-in time base timer for digital clock. For example, if fx (= 32.768 kHz) is selected as clock source, interrupt request flag is set by 13-bit counter par 250 ms. However, the 13-bit counter can be initialized only at reset. Therefore, the first interrupt request flag is not always set after 250 ms.
Depending on counting condition, the first interrupt request flag is generated after 0 ms (minimum) to 250 ms (maximum). So, digital clock may gain 250 ms (maximum).

How to keep a error to a minimum, on setting for digital clock.
When fx (= 32.768 kHz) is set as clock source, and the time base timer is used as digital clock ;

- Select fosc as clock source.

    ↓

- Generate interrupt.

    ↓

- During interrupt service routine, change clock source to fx, and initialize a digital clock.

7-4-2   Setup Example

■Timer Operation Setup (Time Base Timer)

Time base timer generates an interrupt constantly in the selected interrupt cycle. The interrupt generation cycle is as fosc × $1/2^{13}$ (as 0.976 ms : fosc = 8.39 MHz) for generation interrupts.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the clock source. TM5MD (x'3F88') bp0 : TM5CK0 = 0	(1) Select fosc as a clock source by the TM5CK0 flag of the timer 5 mode register (TM5MD).
(2) Select the interrupt generation cycle. TM5MD (x'3F88') bp6-4 : TM5IR2-0 = 100	(2) Select the selected clock × $1/2^{13}$ as an interrupt generation cycle by the TM5IR2-0 flag of the TM5MD register.
(3) Set the interrupt level. TBICR (x'3FE7') bp7-6 : TBLV1-0 = 01	(3) Set the interrupt level by the TBLV1-0 flag of the time base interrupt control register (TBICR). If any interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(4) Enable the interrupt. TBICR (x'3FE7') bp1 : TBIE = 1	(4) Set the TBIE flag of the TBICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

When the selected interrupt generation cycle has passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

Chapter 8 Watchdog Timer

8-1 Overview

This LSI has a watchdog timer. This timer is used to detect software processing errors. It is controlled by the watchdog timer control register (WDCTR). And, once an overflow of watchdog timer is generated, a watchdog interrupt (WDIRQ) is generated. If the watchdog interrupt is generated twice, consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware (Reset pin outputs low level.).

8-1-1 Block Diagram

■Watchdog Timer Block Diagram

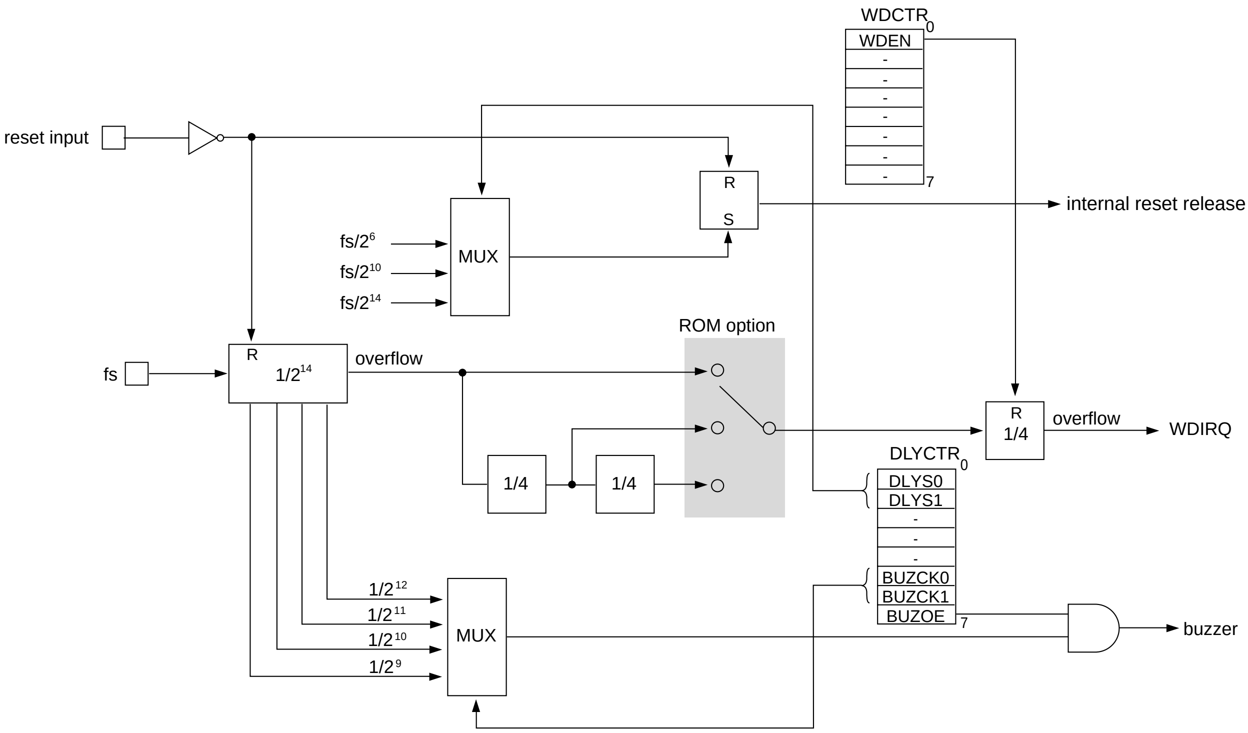


Figure 8-1-1 Block Diagram (Watchdog Timer)

The watchdog timer is also used as a timer to count the oscillation stabilization wait time. This is used as a watchdog timer except at recovering from STOP mode and at reset releasing.
The watchdog timer is initialized at reset or at STOP mode, and counts system clock (fs) as a clock source from the initial value (x'0000'). The oscillation stabilization wait time is set by the oscillation stabilization control register (DLYCTR). After the oscillation stabilization wait, counting is continued as a watchdog timer. [☞ Chapter 2 2-5. Reset]

8-2 Control Registers

The watchdog timer is controlled by the watchdog timer control register (WDCTR). And the cycle of the watchdog timer period is set in ROM option.

[☞ Chapter 1 1-6-1. Rom option]

■Watchdog Timer Control Register (WDCTR)

	7	6	5	4	3	2	1	0	
WDCTR	-	-	-	-	-	-	-	WDEN	(at reset : - - - - - - - 0)

WDEN	Watchdog timer
0	Watchdog timer is cleared/disabled.
1	Watchdog timer is enabled.

Figure 8-2-1 Watchdog Timer Control Register (WDCTR : x'03F02', R/W)

8-3 Operation

8-3-1 Operation

The watchdog timer counts system clock (fs) as a clock source. If the watchdog timer overflows, the watchdog interrupt (WDIRQ) is generated as an non-maskable interrupt (NMI). At reset, the watchdog timer is stopped. The watchdog timer control register (WDCTR) sets if the watchdog timer is enabled or disabled.

If the watchdog interrupt (WDIRQ) is generated twice consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware (Reset pin outputs low level.) .

■Usage of Watchdog Timer

When the watchdog timer is used, constant clear in program is necessary to prevent an overflow of the watchdog timer. As a result of the software failure, the software cannot execute in the intended sequence, thus the watchdog timer overflows and error is detected. After error is detected, the watchdog timer interrupt (WDIRQ) is generated as non-maskable interrupt (NMI).

> Programming of the watchdog timer is generally done in the last step of its programming.

■How to Clear Watchdog Timer

The upper 2 bits of the watchdog timer can be cleared by setting the WDEN flag of the watchdog timer control register (WDCTR) to "0".

> The upper 2 bits of the watchdog timer are cleared when the WDEN flag of the watchdog timer control register (WDCTR) is set to "0". Therefore, depending on the clear timing the watchdog timer may be reset at 1/4 × (watchdog timer frequency). If the WDEN flag is to be repeatedly cleared and set at regular intervals, those operations should be performed within 1/4 of the watchdog timer frequency.

■Watchdog Timer Period

The watchdog timer period is decided by the system clock (fs) and ROM option.

[☞ Chapter 1 1-6-1. Rom option]

If the watchdog timer is not cleared till the set period of watchdog timer, that is regarded as an error and the watchdog interrupt (WDIRQ) of the non-maskable interrupt (NMI) is generated.

Table 8-3-1 Watchdog Timer Period

WDSEL2	WDSEL1	Watchdog timer period
0	0	$2^{16} \times$ system clock
0	1	$2^{18} \times$ system clock
1	X	$2^{20} \times$ system clock

System clock is decided by the CPU mode control register (CPUM).

The watchdog timer period is generally decided from the execution time for main routine of program. That should be set the longer period than the value of the execution time for main routine divided by natural number (1, 2, , ,). And insert the instruction of the watchdog timer clear to the main routine as that value makes the same cycle.

> If the watchdog timer interrupt service routine does not respond to a watchdog timer interrupt for resetting the chip, the hardware responds to the next one by pulling the RESET pin low to reset the chip.

■Watchdog Timer and CPU Mode

The relation between this watchdog timer and CPU mode features are as follows ;

(1) In NORMAL, IDLE, SLOW mode, the system clock is counted.
(2) The counting is continued regardless of switching at NORMAL, IDLE, SLOW mode.
(3) In HALT mode, the watchdog timer is not stopped.
(4) In STOP mode, the watchdog timer is cleared automatically by hardware.
(5) In STOP mode, the watchdog interrupt cannot be generated.
(6) After releasing reset or recovering from STOP, the counting is executed for the duration of the oscillation stabilization wait time.

> On HALT mode, the watchdog timer count won't stop. If it should be stopped, set the WDEN flag of the watchdog timer control register (WDCTR) to "0" to stop the watchdog timer operation, before transition to HALT mode.

> When CPU mode is switched to STOP mode during the watchdog timer operation, the operation does not stop after it operates as a counter for oscillation stabilization waiting at recover. If the watchdog timer is not necessary to detect errors, set the WDEN flag of the watchdog timer control register (WDCTR) to "0" to stop the watchdog timer, before CPU mode is switched to STOP mode.

8-3-2 Setup Example

The watchdog timer detects errors. On the following example, the watchdog timer period is set to $2^{18} \times$ system clock in ROM option.
An example setup procedure, with a description of each step is shown below.

■Initial Setup Program (Watchdog Timer Initial Setup Example)

Setup Procedure	Description
(1) Start the watchdog timer operation. WDCTR (x'03F02') bp0 : WDEN = 1	(1) Set the WDEN flag of the WDCTR register to start the watchdog timer operation.

■Main Routine Program (Watchdog Timer Constant Clear Setup Example)

Setup Procedure	Description
(1) Set the constant watchdog timer clear. BCLR (WDCTR) WDEN (bp0 : WDEN = 0) BSET (WDCTR) WDEN (bp0 : WDEN = 1)	(1) Clear the watchdog timer under the 1/4 cycle of $2^{18} \times$ system clock. The watchdog timer clear should be inserted in the main routine, with the same cycle, and to be the set cycle. Operate the watchdog timer again, after it is stopped (Upper 2 bits of the counter are cleared).

The upper 2 bits of the watchdog timer are cleared when the WDEN flag of the watchdog timer control register (WDCTR) is set to "0". Therefore, depending on the clear timing the watchdog timer may be reset at 1/4 $\times$ (watchdog timer frequency). If the WDEN flag is to be repeatedly cleared and set at regular intervals, those operations should be performed within 1/4 of the watchdog timer frequency.

■Interrupt Service Routine Setup

Setup Procedure	Description
(1) Set the watchdog interrupt service routine. NMICR (x'03FE1') TBNZ (NMICR) WDIR, WDPRO	(1) If the watchdog timer overflows, the non maskable interrupt is generated. Confirm that the WDIR flag of the non maskable interrupt control register (NMICR) is "1" on the interrupt service routine and manage the suitable execution.

Proper operation, right before the WDOG interrupt is not guaranteed. Therefore, if the WDOG interrupt is generated, initialize the system.

Chapter 9 Buzzer

9-1 Overview

This LSI has a buzzer. It can output the square wave having a frequency $1/2^9$ to $1/2^{12}$ of the system clock (fs) from P06/BUZZER pin.

9-1-1 Block Diagram

■Buzzer Block Diagram

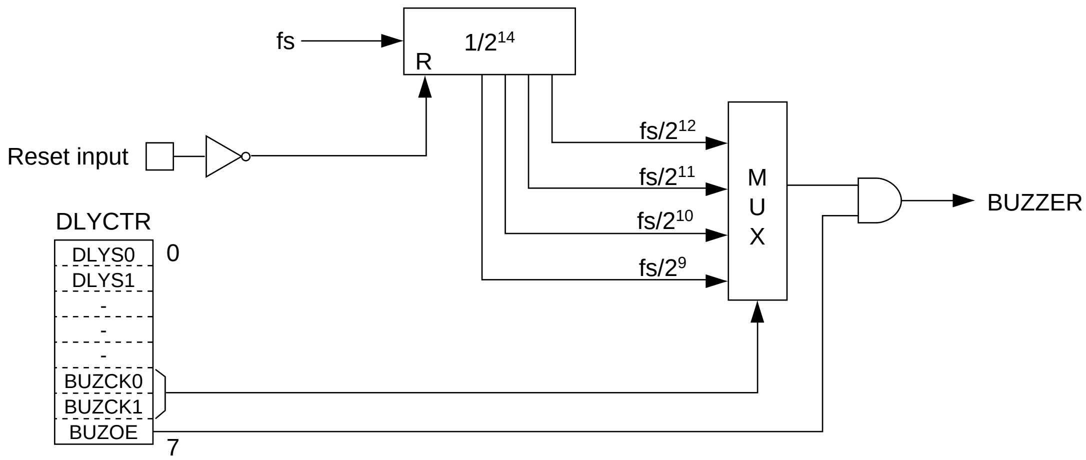


Figure 9-1-1 Block Diagram (Buzzer)

9-2 Control Register

■Oscillation Stabilization Wait Time Control Register

	7	6	5	4	3	2	1	0
DLYCTR	BUZOE	BUZCK1	BUZCK0	-	-	-	DLYS1	DLYS0

(At reset : 0 x x - - - 0 0)

DLYS1	DLYS0	Oscillation stabilization wait period selection
0	0	$fs/2^{14}$
	1	$fs/2^{10}$
1	0	$fs/2^{6}$
	1	Do not set.

Note : After reset is released, the oscillation stabilization wait period is fixed at $fs/2^{14}$.

BUZCK1	BUZCK0	Buzzer output frequency selection
0	0	$fs/2^{12}$
	1	$fs/2^{11}$
1	0	$fs/2^{10}$
	1	$fs/2^{9}$

BUZOE	P06 output selection
0	P06 port data output
1	P06 buzzer output

Figure 9-2-1 Oscillation Stabilization Wait Timer Control Register (DLYCTR : x'03F03', R/W)

9-3　Operation

9-3-1　Operation

■Buzzer

Buzzer outputs the square wave having a frequency $1/2^9$ to $1/2^{12}$ of the system clock (fs). The BUZCK 1, 0 flag of the oscillation stabilization wait control register (DLYCTR) set the frequency of buzzer output. The BUZOE flag of the oscillation stabilization wait control register (DLYCTR) sets buzzer output ON / OFF.

■Buzzer Output Frequency

The frequency of buzzer output is decided by the frequency of the system clock (fs) and the bit 6, 5 (BUZCK1, BUZCK0) of the oscillation stabilization wait control register (DLYCTR). Table 9-3-1 shows the buzzer output frequency.

Table 9-3-1　Buzzer Output Frequency

fosc	fs	BUZCK1	BUZCK0	Buzzer output frequency
20 MHz	10 MHz	0	0	2.44 kHz
		0	1	4.88 kHz
8.39 MHz	4.19 MHz	0	1	2.05 kHz
		1	0	4.10 kHz
2 MHz	1 MHz	1	1	1.95 kHz

9-3-2 Setup Example

Buzzer outputs 2-kHz square wave from P06 pin. It is used 8.39 MHz as the high oscillation clock (fosc). An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the buzzer frequency. DLYCTR (x'3F03') bp6-5 : BUZCK1-0 = 01	(1) Set the BUZCK1-0 flag of the oscillation stabilization wait control register (DLYCTR) to "01" to select $fs/2^{11}$ to the buzzer frequency. When the high oscillation clock fosc is 8.39 MHz, the buzzer output frequency is 2 kHz.
(2) Set P06 pin. P0OUT (x'3F10') bp6 : P0OUT6 = 0 P0DIR (x'3F30') bp6 : P0DIR6 = 1	(2) Set the output data P0OUT6 of P06 pin to "0", and set the direction control P0DIR6 of P06 pin to "1" to select output mode. P06 pin outputs low level.
(3) Buzzer output ON. DLYCTR (x'3F03') bp7 : BUZOE = 1	(3) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "1" to output the square wave of the buzzer output frequency set by P06 pin.
(4) Buzzer output OFF. DLYCTR (x'3F03') bp7 : BUZOE = 0	(4) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "0" to clear, and P06 pin outputs low level.

Chapter 10 Serial Interface 0

10-1 Overview

This LSI contains a serial interface 0 that can be used for both communication types of clock synchronous and UART (Half-duplex).

10-1-1 Functions

Table 10-1-1 shows functions of serial interface 0.

Table 10-1-1 Serial Interface 0 Functions

Communication style	clock synchronous	UART (half-duplex)
Interrupt	SC0IRQ	SC0IRQ
Used pins	SBO0,SBI0,SBT0	TXD,RXD
3 channels type	√	-
2 channels type	√ (SBO0,SBT0)	√
1 channel type	-	√ (TXD)
Specification of transfer bit count / Frame selection	1 to 8 bits	7 bits + 1 stop 7 bits + 2 stops 8 bits + 1 stop 8 bits + 2 stops
Selection of parity bit	-	√
Parity bit control	-	0 parity 1 parity odd parity even parity
Selection of start condition	√	no selection Start bit is always added.
Specification of the first transfer bit	√	√
Specification of input edge / output edge	√	-
Internal clock 1/8 dividing	√	only 1/8 dividing is available
Clock source	fs/2 fs/4 fs/16 Timer 3 output External clock	fs/2 fs/4 fs/16 Timer 3 output
Maximum transfer rate	5.0 MHz	625 kbps
fosc : Machine clock (High speed oscillation) fs : System clock (at NORMAL mode : fs=fosc/2, at SLOW mode : fs=fx/4) When the transmission and reception are operated at the same time at master communication of the clock synchronous, select "no start condition".-		

Set fs/2 as maximum frequency for external clock.

10-1-2 Block Diagram

■Serial Interface 0 Block Diagram

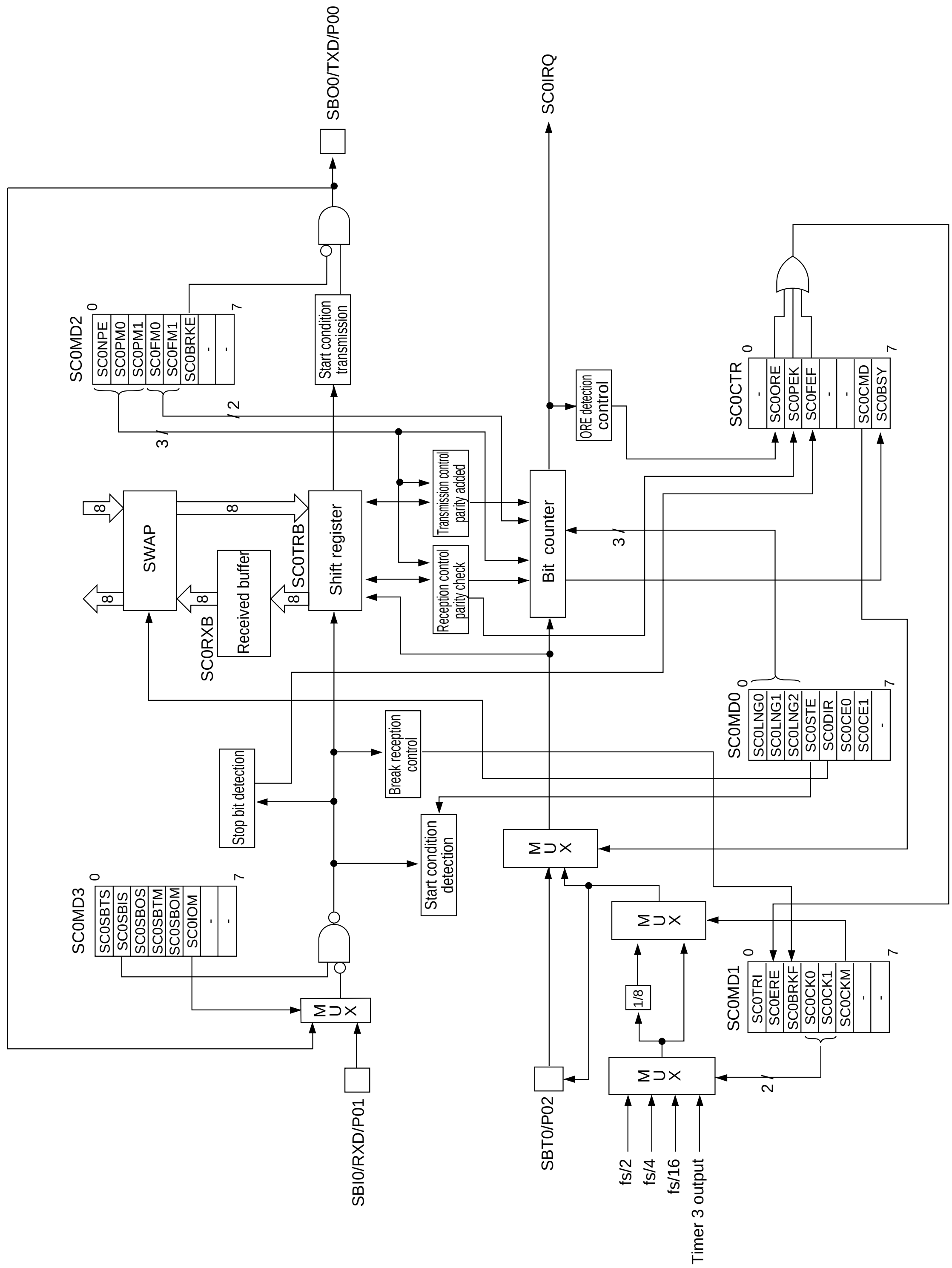


Figure 10-1-1 Serial Interface 0 Block Diagram

10-2 Control Registers

10-2-1 Registers

Table 10-2-1 shows registers to control serial interface 0.

Table 10-2-1 Serial Interface 0 Control Registers

	Register	Address	R/W	Function	Page
Serial interface 0	SC0MD0	x'03F50'	R/W	Serial interface 0 mode register 0	X - 6
	SC0MD1	x'03F51'	R/W	Serial interface 0 mode register 1	X - 7
	SC0MD2	x'03F52'	R/W	Serial interface 0 mode register 2	X - 8
	SC0MD3	x'03F53'	R/W	Serial interface 0 mode register 3	X - 9
	SC0CTR	x'03F54'	R/W	Serial interface 0 control register	X - 10
	SC0TRB	x'03F55'	R/W	Serial interface 0 transmission / reception shift register	X - 5
	SC0RXB	x'03F56'	R	Serial interface 0 reception data buffer	X - 5

R/W : Readable / Writable
R : Readable only

10-2-2 Data Buffer Registers

Serial Interface 0 has a 8-bit shift register to shift the transmission and reception data and a 8-bit data buffer register for reception.

■Serial Interface 0 Transmission/Reception Shift Register (SC0TRB)

	7	6	5	4	3	2	1	0	
SC0TRB	SC0TRB7	SC0TRB6	SC0TRB5	SC0TRB4	SC0TRB3	SC0TRB2	SC0TRB1	SC0TRB0	(at reset : X X X X X X X X)

Figure 10-2-1 Serial Interface 0 Transmission/Reception Shift Register (SC0TRB : x'03F55', R/W)

■Serial Interface 0 Received Data Buffer (SC0RXB)

	7	6	5	4	3	2	1	0	
SC0RXB	SC0RXB7	SC0RXB6	SC0RXB5	SC0RXB4	SC0RXB3	SC0RXB2	SC0RXB1	SC0RXB0	(at reset : X X X X X X X X)

Figure 10-2-2 Serial Interface 0 Reception Data Buffer (SC0RXB : x'03F56', R)

10-2-3 Mode Registers / Control Registers

■Serial Interface 0 Mode Register 0 (SC0MD0)

	7	6	5	4	3	2	1	0
SC0MD0	-	SC0CE0	SC0CE1	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0

(at reset : - 0 0 X X 0 0 0)

SC0LNG2	SC0LNG1	SC0LNG0	Synchronous serial transfer bit count
0	0	0	8 bits
		1	7 bits
	1	0	6 bits
		1	5 bits
1	0	0	4 bits
		1	3 bits
	1	0	2 bits
		1	1 bit

SC0STE	Synchronous serial data transfer start condition selection
0	Disable start condition
1	Enable start condition

SC0DIR	First bit to be transferred
0	MSB first
1	LSB first

SC0CE0	SC0CE1	Reception data input edge	Transmission data output edge
0	0	Rising	Falling
	1	Falling	Rising
1	0	Falling	Falling
	1	Rising	Rising

Figure 10-2-3 Serial Interface 0 Mode Register 0 (SC0MD0 : x'03F50', R/W)

■Serial Interface 0 Mode Register 1 (SC0MD1)

The SC0TRI, SC0ERE, and SC0BRKF flags are only readable.

	7	6	5	4	3	2	1	0
SC0MD1	-	-	SC0CKM	SC0CK1	SC0CK0	SC0BRKF	SC0ERE	SC0TRI

(at reset : - - X 0 0 0 0 0)

SC0TRI	Transmission / Reception interrupt request flag
0	Transmission interrupt request
1	Reception interrupt request

SC0ERE	Error monitor
0	No error
1	Error

SC0BRKF	Break status receive monitor
0	Data
1	Break

SC0CK1	SC0CK0	Clcok source
0	0	fs/2
	1	fs/4
1	0	fs/16
	1	Timer 3 output

SC0CKM	1/8 dividing of transfer clock selection
0	Do not divide by 8
1	Divide by 8

Clock source can be selected as an external clock by setting the SBT0 pin to input mode. At UART mode (SC0CMD=1),the SC0CKM is fixed to "1".

Figure 10-2-4 Serial Interface 0 Mode Register 1 (SC0MD1 : x'03F51', R/W)

■Serial Interface 0 Mode Register 2 (SC0MD2)

	7	6	5	4	3	2	1	0
SC0MD2	-	-	SC0BRKE	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE

(at reset : - - 0 0 0 X X X)

SC0NPE	Parity enable
0	Enable parity bit
1	Disable parity bit

SC0PM1	SC0PM0	Added bit specification	
		Transmission	Reception
0	0	Add "0"	Check for "0"
	1	Add "1"	Check for "1"
1	0	Add odd parity	Check for odd parity
	1	Add even parity	Check for even parity

SC0FM1	SC0FMO	Frame mode specification
0	0	7 data bits + 1 stop bit
	1	7 data bits + 2 stop bits
1	0	8 data bits + 1 stop bit
	1	8 data bits + 2 stop bits

SC0BRKE	Break status transmit control
0	Data transmit
1	Break transmit

Figure 10-2-5　Serial Interface 0 Mode Register 2 (SC0MD2 : x'03F52', R/W)

■Serial Interface 0 Mode Register 3 (SC0MD3)

	7	6	5	4	3	2	1	0
SC0MD3	-	-	SC0IOM	SC0SBOM	SC0SBTM	SC0SBOS	SC0SBIS	SC0SBTS

(at reset : - - 0 0 0 0 0 0)

SC0SBTS	SBT0 pin function selection
0	Port
1	Serial interface clock pin

SC0SBIS	SBI0 input control (reception enable flag)
0	"1" input
1	Serial data input

SC0SBOS	SBO0 pin function selection (transmission enable flag)
0	Port
1	Serial data communication

SC0SBTM	SBT0 pin configuration
0	Push - pull output
1	N ch open drain output

SC0SBOM	SBO0 pin configuration
0	Push - pull output
1	N ch open drain output

SC0IOM	Reception port
0	SBI0 : Reception port SBO0 : Transmission port
1	SBI0 : General port SBO0 : Transmission / Reception port

Figure 10-2-6 Serial Interface 0 Mode Register 3 (SC0MD3 : x'03F53', R/W)

■Serial Interface 0 Control Register (SC0CTR)

The SC0ORE, SC0PEK, SC0FEF,and SC0BSY flags are only readable .

	7	6	5	4	3	2	1	0
SC0CTR	SC0BSY	SC0CMD	-	-	SC0FEF	SC0PEK	SC0ORE	-

(At reset : 0 0 - - 0 0 0 -)

SC0ORE	Overrun error detection
0	No error
1	Error

SC0PEK	Parity error detection
0	No error
1	Error

SC0FEF	Framing error detection
0	No error
1	Error

SC0CMD	Clock synchronous / UART selection
0	Clock synchronous
1	UART

SC0BSY	Serial bus status
0	Other use
1	Serial transmission in progress

Figure 10-2-7 Serial Interface 0 Control Register (SC0CTR : x'03F54', R/W)

10-3 Operation

Serial Interface 0 can be used for both clock synchronous and half-duplex UART.

10-3-1 Clock Synchronous Serial Interface

■Selection of Clock Synchronous Serial Interface
When the serial interface 0 is used as clock synchronous serial interface, set the SC0CMD flag of the serial interface control register (SC0CTR) to "0".

■Activation Factor for Communication
Table 10-3-1 shows activation factors for communication. At master, the transfer clock is generated by setting data to the transmission / reception shift register SC0TRB, or by receiving a start condition. At slave, input an external clock, or input an external clock after a start condition is input.

Table 10-3-1 Synchronous Serial Interface Activation Factor

Operation mode			Activation factor	Sequence communication
Transmission	at master	Enable start condition	Writing data to serial buffer	√
		Disable start condition	Writing data to serial buffer	√
	at slave	Enable start condition	Clock reception *	√
		Disable start condition	Clock reception	√
Reception	at master	Enable start condition	Start condition reception	√
		Disable start condition	Writing data to serial buffer	–
	at slave	Enable start condition	Start condition reception	√
		Disable start condition	Clock reception	√

* Start condition is output by writing the transmission data to the transmission / reception shift register SC0TRB when the SC0SBOS flag of the serial interface 0 mode register 3 (SC0MD3) is set to "1". Then, the transmission is started by the slave clock.

When synchronous serial interface is used for master clock reception, it is necessary to write dummy data to the transmission / reception shift register (SC0TRB) for starting master clock. Automatic sequence reception with automatic data transfer can not be used, because it is necessary to write dummy data to serial interface buffer and to read reception data per a frame reception.

Cautions for master clock reception by the synchronous serial interface 0

On the product with serial interface 1 or serial interface 2, master clock reception by synchronous serial interface 1, 2 is started by setting the SCxSBTS of the serial interface mode register (SCxMDx) to "1", then, setting the SCxSBIS to "1" and writing dummy data to the transmission / reception shift register (SCxTRB).

But, by the above setting, this serial interface 0 cannot output the master clock, so that the reception is not started.
Therefore, the following setup by the software is necessary.

<By software>
When synchronous serial interface 0 is used for master clock reception, it is necessary to set the SC0SBTS flag of the serial interface 0 mode register 3 (SC0MD3) to "1", then, set the SC0SBIS flag to "1" and set the SC0SBOS flag to "1".
At last, the master clock is output by the writing dummy data to the transmission / reception shift register (SC0TRB), then, the reception is started.

Program example for master clock reception by the synchronous serial interface 0

SC0SBTS	← 1	
SC0SBIS, SC0SBOS	← 1, 1	
SC0TRB	← x'XX'	(dummy data is written, reception is started)

The SBO0 pin cannot be used as general output port by setting the SC0SBOS flag to "1". But it can be used as general input port by setting the bp0 of the port 0 direction control register (P0DIR) to "0".

Serial data communication of serial interface 0 can be available by setting the SC0SBIS flag or the SC0SBOS flag of the SC0MD3 register to "1". The SC0SBIS flag or the SC0SBOS flag should be set to "1" after all conditions are set.

On the master communication of the clock synchronous, set the SC0SBTS flag to "1" before the SC0SBOS flag or the SC0SBIS flag of the SC0MD3 register is set to "1". But, at the slave communication, the SC0SBTS flag needs not to be set to "1".

■Transfer Bit Count

The transfer bit count is selected from 1 bit to 8 bits. Set it by the SC0LNG2 to 0 flag of the SC0MD0 register (at reset : 000).

The SC0LNG2 to 0 flags change at the opposite edge of the transmission data output edge.

After the transfer has completed, the transfer bit count in the SC0LNG2 to 0 flags of the SC0MD0 register is changed. Except in an 8-bit transfer, reset the transfer bit count at the time of the next transmission.

When the SC0SBOS flag or the SC0SBIS flag of the SC0MD3 register is "1" and the SC0CE1 to 0 flags of the SC0MD0 register are changed, the transfer bit count in the SC0LNG2 to 0 flags of the SC0MD0 register may be incremented.

■Start Condition

The SC0STE flag of the SC0MD0 register sets if a start condition is enabled or not. If a start condition is enabled and input, a bit counter is cleared to start the communication. The start condition, if the SC0CE1 flag of the SC0MD0 register is set to "0", is regarded when a data line (SBI0 pin (with 3 channels) or SBO0 pin (with 2 channels) is changed from "H" to "L" as a clock line (SBT0 pin) is "H". Also, the start condition, if the SC0CE1 flag is set to "1", is regarded when a data line (SBI0 pin (with 3 channels) or SBO0 pin (with 2 channels) is changed from "H" to "L" as a clock line (SBT0 pin) is "L".

When the reception and the transmission should be operated at the same time, disable start condition for proper operation.

Enabling the start condition drives the SBO0 pin high level for a fixed time interval (1/2 the clock source cycle) after the transmission has completed. If the start condition is disabled, the SBO0 pin will remain at the level of the last data bit.

If the start condition is enabled, the SC0LNG2 to 0 flags of the SC0MD0 register will be cleared when the start condition is received. In this case, the receive bit count is fixed at 8 bits.

On the master communication of the clock synchronous, if start condition is enabled, the reception and the transmission should not be operated at the same time. The clock may be continued to output after the communication has completed.

■First Transfer Bit

The SC0DIR flag of the SC0MD0 register can set the first transfer bit. MSB first or LSB first can be selected.

■Transmission Data

Set the transmission data to the transmission / reception shift register (SC0TRB).

When switching from transmission to reception, set the SC0SBOS flag of the SC0MD0 register to "0" and then set the SC0SBIS flag to "1". Do not change both of these flags at the same time.

When switching from reception to transmission, set the SC0SBIS flag of the SC0MD0 register to "0" and then set the SC0SBOS flag to "1". Do not change both of these flags at the same time.

■Tranfer Bit Count and First Transfer Bit

On transmission, when the transfer bit is 1 bit to 7 bits, the data storing method to the transmission / reception shift register SC0TRB is different, depending on the first transfer bit selection. At MSB first, use the upper bits of SC0TRB. When there are 6 bits to be transferred, as shown on figure 10-3-1-1, if data "A" to "F" are stored to bp2 to bp7 of SC0TRB, the transmission is started from "F" to "A". At LSB first, use the lower bits on the program. When there are 6 bits to be transferred, as shown on figure 10-3-1-2, if data "A" to "F" are stored to bp0 to bp5 on the program, the transmission is started from "A" to "F", because their order is changed in the SWAP circuit.

	7	6	5	4	3	2	1	0
SC0TRB	F	E	D	C	B	A		

Figure 10-3-1-1 Transfer Bit Count and First Transfer Bit (starting with MSB)

	7	6	5	4	3	2	1	0
Setting on program			F	E	D	C	B	A

	7	6	5	4	3	2	1	0
SC0TRB	A	B	C	D	E	F		

Figure 10-3-1-2 Transfer Bit Count and First Transfer Bit (starting with LSB)

■Received Data Buffer

The received data buffer SC0RXB is the sub-buffer that pushed the received data in the internal shift register. After the communication complete interrupt SC0IRQ is generated, data stored in the transmission / reception shift register is stored to the received data buffer SC0RXB automatically. SC0RXB can store data up to 1 byte. SC0RXB is rewritten in every communication complete, so read data of SC0RXB till the next receive complete. And before the next data reception is started, the same data to the SC0RXB can be read, even if the SC0TRB is reading.

When the SC0SBIS flag of the SC0MD3 register is set to "serial interface input", the SC0TRI flag of the SC0MD1 register is set to "1" at the same time SC0IRQ is generated. SC0TRI is cleared to "0" when the next reception has completed.

■Receive Bit Count and First Transfer Bit

On reception, when the transfer bit count is 1 bit to 7 bits, the data reading method from the received data buffer SC0RXB is different depending on the first transfer bit selection. At MSB first, data are read from the lower bits of SC0RXB. When there are 6 bits to be transferred, as shown on figure 10-3-2-1, if data "F" to "A" are stored to bp0 to bp5 of SC0RXB. Also, data are read as the same way. At LSB first, data are read from the upper bits of SC0RXB. When there are 6 bits to be transferred, as shown on figure 10-3-2-2, if data "A" to "F" are stored to bp0 to bp5 of SC0RXB. But their order is changed in the SWAP circuit, and reading is started from the upper bits.

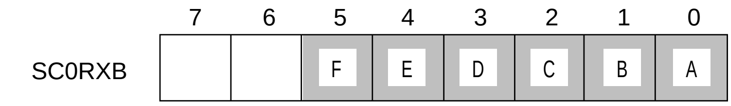


Figure 10-3-2-1 Receive Bit Count and Transfer First Bit (starting with MSB bit)

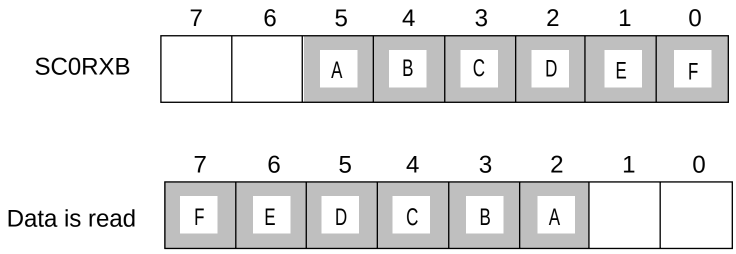
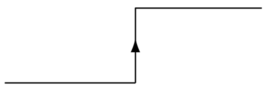
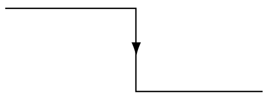
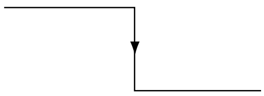
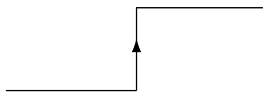
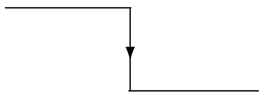
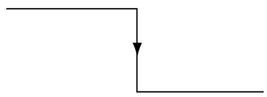
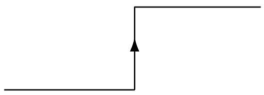
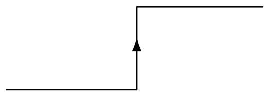


Figure 10-3-2-2 Receive Bit Count and Transfer First Bit (starting with LSB bit)

■Input Edge / Output Edge Setup

The SC0CE1 to 0 flag of the SC0MD0 register set an output edge of the transmission data, an input edge of the reception data. As the SC0CE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SC0CE0 = "0", the reception data is stored at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table 10-3-2 Input Edge and Output Edge of Transmission Reception Data

SC0CE0	SC0CE1	Reception data input edge	Transmission data output edge
0	0		
0	1		
1	0		
1	1		

■Clock Setup

The clock source can be selected from the internal clock or the external clock. Here is the internal clock source that can be set by the SC0CK1 to 0 register of the SC0MD1 register. Also, the internal clock can be divided by 8, by setting the SC0CKM flag of the SC0MD1 register to "1".

Table 10-3-3 Synchronous Serial Interface Internal Clock Source

	Serial interface 0
Clock source (internal clock)	fs/2
	fs/4
	fs/16
	Timer 3 output

■Data Input Pin Setup

3 channels type (clock pin (SBT0 pin), data output pin (SBO0 pin), data input pin (SBI0 pin)) or 2 channels type (clock pin (SBT0 pin), data I/O pin (SBO0 pin)) can be selected as the communication. SBI0 pin can be used for only serial data input. SBO0 pin can be used for serial data input or output. The SC0IOM flag of the SC0MD3 register can select if the serial data is input from SBI0 pin or SBO0 pin. When "data input from SBO0 pin" is selected to set the 2 channels type, the P0DIR0 flag of the P0DIR register controls direction of SBO0 pin to switch transmission / reception. At that time, SBI0 pin is free to be used as a general port.

At reception, if SC0IOM of the SC0MD3 register is set to "1" and "serial data input from SBO0" is selected, SBI0 pin is used as a general port.

■BUSY Flag

When the activation factor is generated, shown in Table 10-3-1, and the serial interface communication is started, the BUSY flag SC0BSY of the SC0CTR register is set to "1". That is cleared to "0" when the communication complete interrupt SC0IRQ is generated.

■Other Control Flag Setup

Table 10-3-4 shows flags that are not used at clock synchronous communication. So, they need not to be set or monitored.

Table 10-3-4 Other Control Flag

Register	Flag	Detail
SC0MD1	SC0BRKF	Brake status reception monitor
	SC0ERE	Error monitor
SC0MD2	SC0NPE	Parity is enabled
	SC0PM1 to 0	Added bit specification
	SC0FM1 to 0	Frame mode specification
	SC0BRKE	Brake status transmission control
SC0CTR	SC0ORE	Overrun error detection
	SC0PEK	Parity error detection
	SC0FEF	Frame error detection

■Transmission Timing

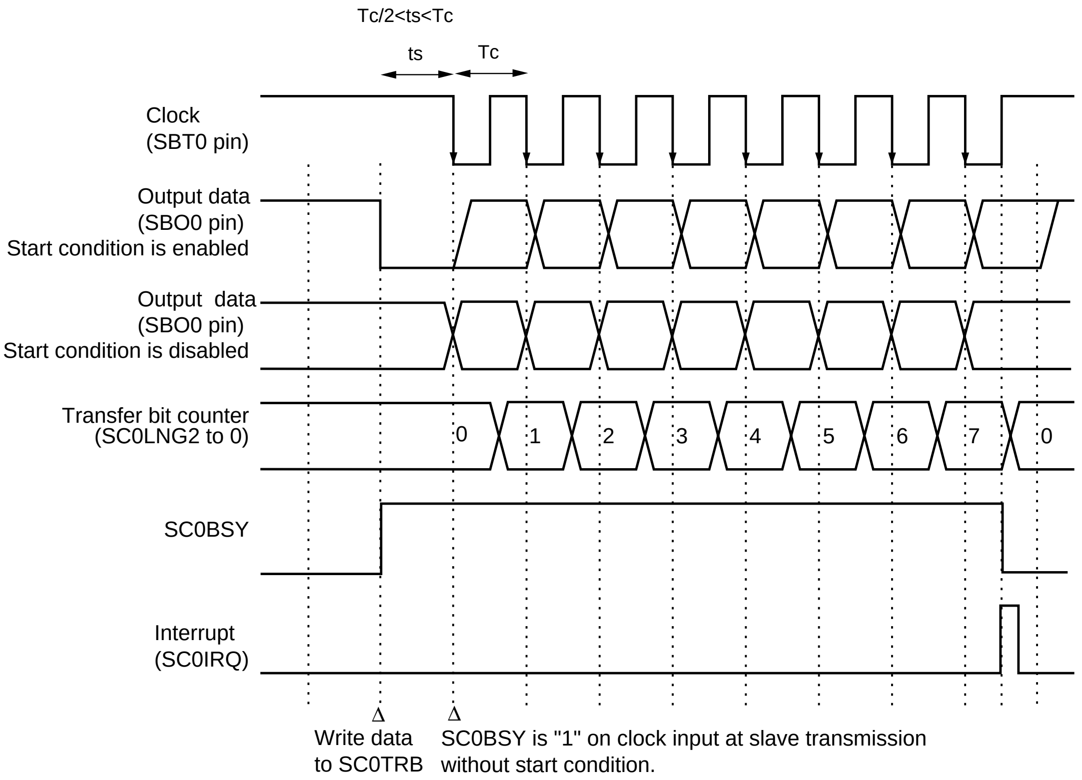


Figure 10-3-3 Transmission Timing (falling edge)

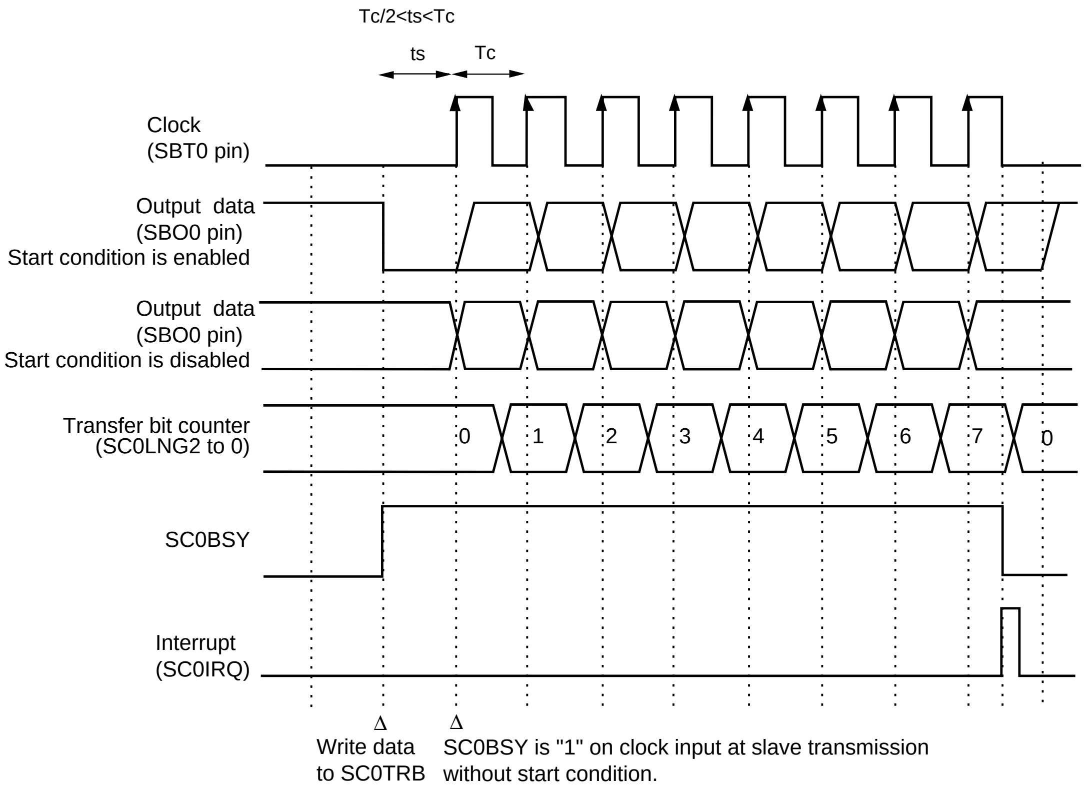


Figure 10-3-4 Transmission Timing (rising edge)

■Reception Timing

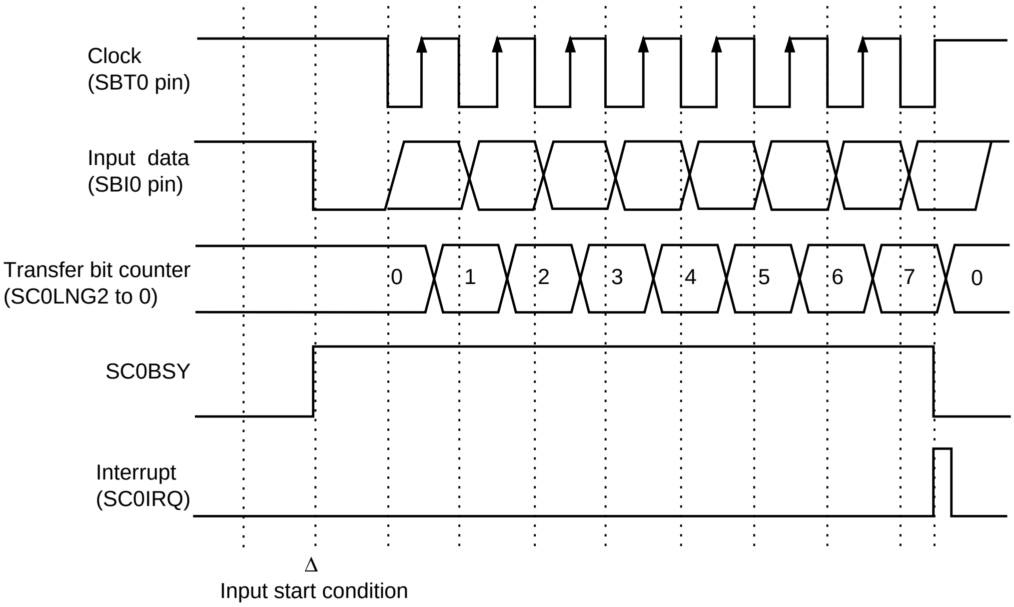


Figure 10-3-5　Reception Timing (rising edge, start condition is enabled)

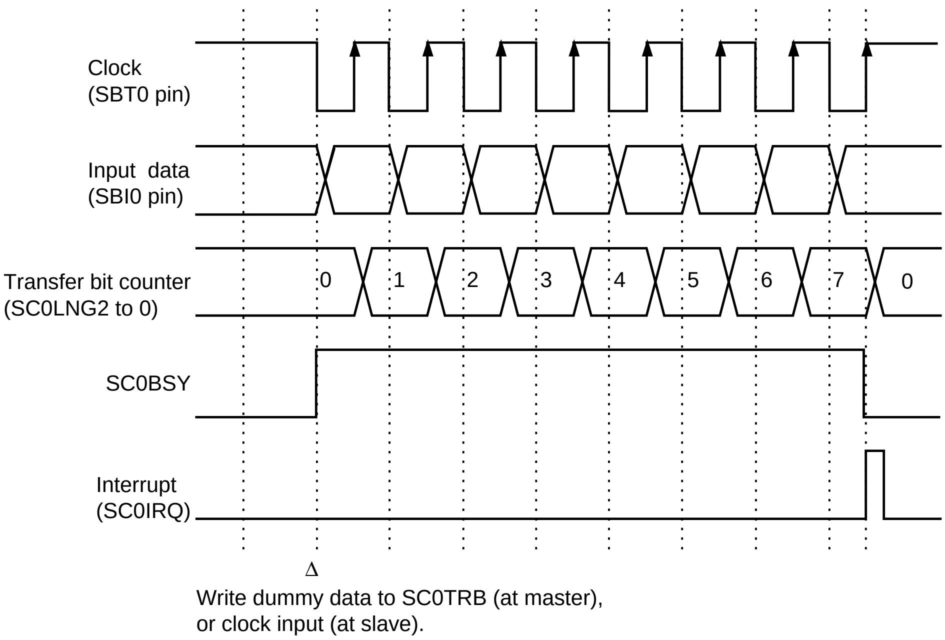


Figure 10-3-6　Reception Timing (rising edge, start condition is disabled)

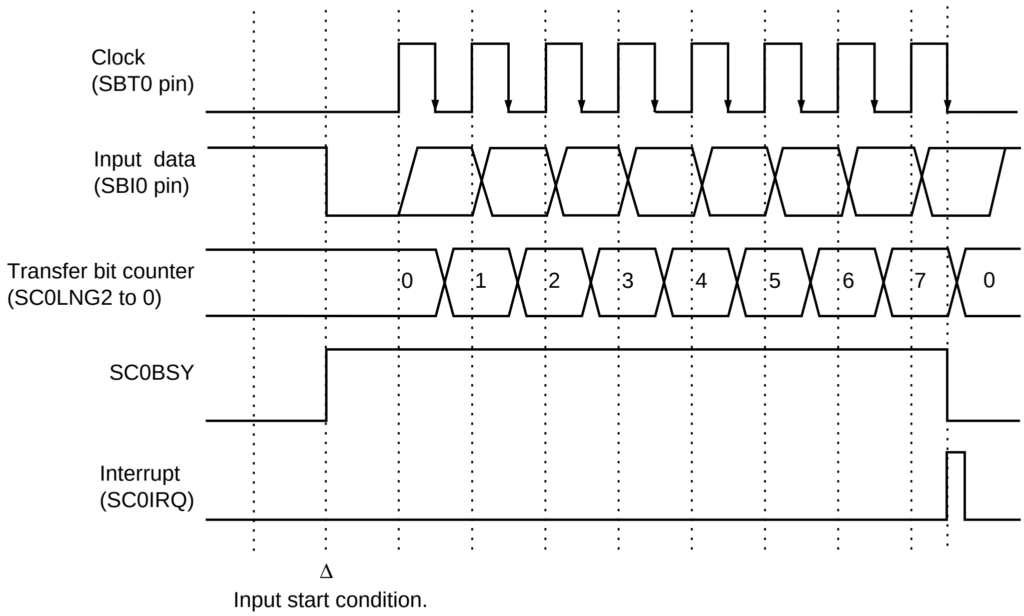


Figure 10-3-7 Reception Timing (falling edge, start condition is enabled)

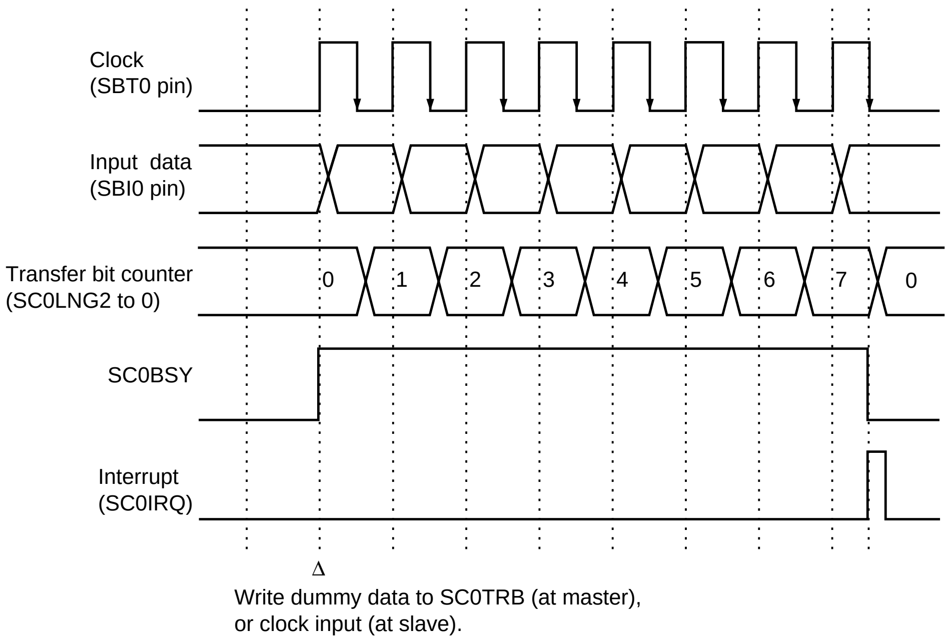


Figure 10-3-8 Reception Timing (falling edge, start condition is disabled)

■Transmission / Reception Simultaneous Timing

When transmission and reception are operated at the same time, set the SC0CE0 to 1 flag of the SC0MD0 register to "00" or "01". Data is received at the opposite edge of the transmission clock, so that the reception clock should be the opposite edge of the transmission clock from the other side.

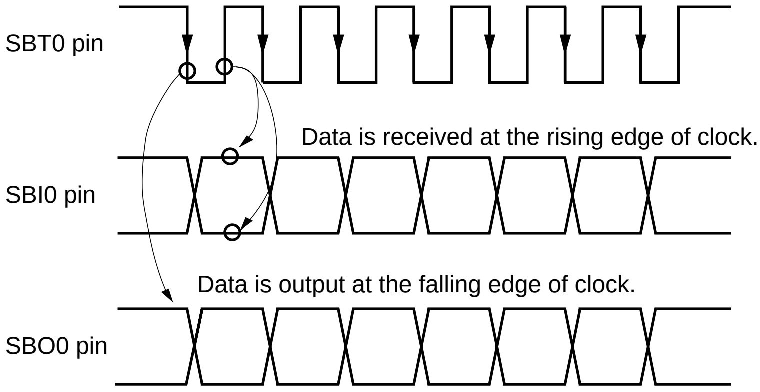


Figure 10-3-9 Transmission / Reception Timing
(Reception : rising edge, Transmission : falling edge)
(SC0CE0 = 0, SC0CE1 = 0)

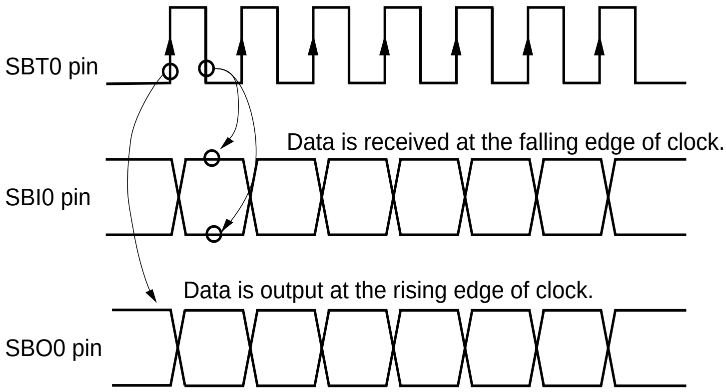


Figure 10-3-10 Transmission / Reception Timing
(Reception : falling edge, Transmission : rising edge)
(SC0CE0 = 0, SC0CE1 = 1)

■Pins Setup (3 channels, at transmission)

Table 10-3-5 shows the setup for synchronous serial interface pin with 3 channels (SBO0 pin, SBI0 pin, SBT0 pin) at transmission.

Table 10-3-5 Setup for Synchronous Serial Interface Pin (3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0 pin	SBI0 pin	SBT0 pin	
			Internal clock (master communication)	External clock (slave communication)
Pin	P00	P01	P02	
SBI0 / SBO0 pin	SBI0 / SBO0 independent		-	
	SC0MD3(SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Port
	SC0MD3(SC0SBOS)	SC0MD3(SC0SBIS)	SC0MD3(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0OMD3(SC0SBOM)		SC0MD3(SC0SBTM)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	P0PLU(P0PLU0)		P0PLU(P0PLU2)	

■Pins Setup (3 channels, at reception)

Table 10-3-6 shows the setup for synchronous serial interface pin with 3 channels (SBO0 pin, SBI0 pin, SBT0 pin at reception).

Table 10-3-6 Setup for Synchronous Serial Interface Pin (3 channels, at reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0 pin	SBI0 pin	SBT0 pin	
			Internal clock (master communication)	External clock (slave communication)
Pin	P00	P01	P02	
SBI0 / SBO0 pin	SBI0 / SBO0 independent		-	
	SC0MD3(SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Port
	SC0MD3(SC0SBOS)	SC0MD3(SC0SBIS)	SC0MD3(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0MD3(SC0SBTM)	
I/O	-	Input mode	Output mode	Input mode
		P0DIR(P0DIR1)	P0DIR(P0DIR2)	
Pull-up	-	Added / Not added	Added / Not added	Added / Not added
		P0PLU(P0PLU1)	P0PLU(P0PLU2)	

■Pins Setup (3 channels, at transmission / reception)

Table 10-3-7 shows the setup for synchronous serial interface pin with 3 lines (SBO0 pin, SBI0 pin, SBT0 pin) at transmission / reception.

Table 10-3-7 Setup for Synchronous Serial Interface Pin (3 channels, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0 pin	SBI0 pin	SBT0 pin	
			Internal clock (master communication)	External clock (slave communication)
Pin	P00	P01	P02	
SBI0 / SBO0 pin	SBI0 / SBO0 independent		-	
	SC0MD3(SC0IOM)			
Function	Serial data output	Serial data input	Serial clock I/O	Port
	SC0MD3(SC0SBOS)	SC0MD3(SC0SBIS)	SC0MD3(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0MD3(SC0SBOM)		SC0MD3(SC0SBTM)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR(P0DIR0)	P0DIR(P0DIR1)	P0DIR(P0DIR2)	
Pull-up	Added / Not added	Added / Not added	Added / Not added	Added / Not added
	P0PLU(P0PLU0)	P0PLU(P0PLU1)	P0PLU(P0PLU2)	

■Pins Setup (2 channels, at transmission)

Table 10-3-8 shows the setup for synchronous serial interface pin with 2 channels (SBO0 pin, SBT0 pin) at transmission. SBI0 pin can be used as a general port.

Table 10-3-8 Setup for Synchronous Serial Interface Pin (2 channels, at transmission)

Setup item	Data I/O pin	Serial unused pin	Clock I/O pin	
	SBO0 pin	SBI0 pin	SBT1 pin	
			Internal clock (master communication)	External clock (slave communication)
Pin	P00	P01	P02	
SBI0 / SBO0 pin	SBI0 / SBO0 connected		-	
	SC0MD3(SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Port
	SC0MD3(SC0SBOS)	SC0MD3(SC0SBIS)	SC0MD3(SC0SBTS)	
Stype	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0MD3(SC0SBOM)		SC0MD3(SC0SBTM)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	P0PLU(P0PLU0)		P0PLU(P0PLU2)	

■Pins Setup (2 channels, at reception)

Table 10-3-9 shows the setup for synchronous serial interface pin with 2 channels (SBO0 pin, SBT0 pin) at reception. SBI0 pin can be used as a general port.

Table 10-3-9 Setup for Synchronous Serial Interface Pin (2 channels, at reception)

Setup item	Data I/O pin	Serial unused pin	Clock I/O pin	
	SBO0 pin	SBI0 pin	SBT0 pin	
			Internal clock (master communication)	External clock (slave communication)
Pin	P00	P01	P02	
SBI0 / SBO0 pin	SBI0 / SBO0 connected		-	
	SC0MD3(SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Port
	SC0MD3 (SC0SBOS)	SC0MD3 (SC0SBIS)	SC0MD3(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0MD3(SC0SBTM)	
I/O	Input mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	P0PLU(P0PLU0)		P0PLU(P0PLU2)	

10-3-2 Setup Example

■Transmission / Reception Setup Example

The setup example for clock synchronous serial interface communication with serial interface 0 is shown. Table 10-3-10 shows the conditions at transmission / reception.

Table 10-3-10 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	set to		Setup item	set to
SBI0 / SBO0 pin	Independent (with 3 channels)		Clock source	fs/2
Transfer bit count	8 bits		Clock source 1/8 dividing	not divided by 8
Start condition	none		SBT0 / SBO0 pin style	N-ch open-drain
First transfer bit	MSB		SBT0 pin pull-up resistor	Not added
Input clock edge	falling edge		SBO0 pin pull-up resistor	Not added
			SBI0 pin pull-up resistor	Added
Output clock edge	rising edge		Serial 0 communication complete interrupt	Enable
Clock	Internal clock (master communication)			

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the clock synchronous serial interface. SC0CTR (x'3F54') bp6 : SC0CMD = 0	(1) Set the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "0" to select the clock synchronous serial interface.
(2) Set the SC0MD0 register. Select the transfer bit count SC0MD0 (x'3F50') bp2-0 : SC0LNG2-0 = 000	(2) Set the SC0LNG2-0 flag of the serial interface 0 mode register 0 (SC0MD0) to "000" to set the transfer bit to 8 bits.
Select the start condition. SC0MD0 (x'3F50') bp3 : SC0STE = 0	Set the SC0STE flag of the SC0MD0 register to "0" to disable start condition.
Select the first bit to be transferred. SC0MD0 (x'3F50') bp4 : SC0DIR = 0	Set the SC0DIR flag of the SC0MD0 register to "0" to set MSB as a transfer first bit.
Select the transfer edge. SC0MD0 (x'3F50') bp6 : SC0CE0 = 0 bp5 : SC0CE1 = 1	Set the SC0CE0, 1 flag of the SC0MD0 register to "0, 1" to set the transmission data output edge "rising" and the received data input edge "falling".

Setup Procedure	Description
(3) Select the clock source. SC0MD1 (x'3F51') bp4-3 : SC0CK1-0 = 00 bp5 : SC0CKM = 0	(3) Set the SC0CK1-0 flag of the SC0MD1 register to "00" to select the clock source "fs/2". Set the SC0CKM flag to "0" to select not to divide the clock source by 1/8.
(4) Select the transfer clock. SC0MD3 (x'3F53') bp0 : SC0BTS = 1	(4) Set the SC0SBTS flag of the SC0MD3 register to "1" to set the SBT0 pin to serial interface clock I/O pin. The communication is used with the internal clock (master communication).
(5) Control the pin type. SC0MD3 (x'3F53') bp4-3 : SC0SBOM, SC0SBTM = 11 bp5 : SC0IOM = 0 P0PLU (x'3F40') bp2-0 : P0PLU2-0 = 010	(5) Set the SC0SBOM, SC0SBTM flag of the SC0MD3 register to "11" to select the SBO0/ SBT0 pin to "N-ch open-drain". Set the SC0IOM flag to "0" to set "input serial data from the SBI0 pin". Set the POPLU2-0 flag of the POPLU register to "010" to select "add pull-up resistor only to the SBI0 pin.
(6) Control the pin direction. P0DIR (x'3F30') bp2-0 : P0DIR2-0 = 101	(6) Set the P0DIR2-0 flag of the port 0 pin direction control register (P0DIR) to "101" to set P00 and P02 to output mode and to set P01 to input mode.
(7) Control the pin function. SC0MD3 (x'3F53') bp2 : SC0SBOS = 1 bp1 : SC0SBIS = 1	(7) Set the SC0SBOS, SC0SBIS flag of the SC0MD3 register to "1" to set SBO0 pin "serial data output", SBI0 pin "serial data input".
(8) Set the interrupt level. SC0ICR (x'3FF8') bp7-6 : SC0LV1-0 = 10	(8) Set the interrupt level by the SC0LV1-0 flag of the serial interface 0 interrupt control register (SC0ICR).
(9) Enable the interrupt. SC0ICR (x'3FF8') bp1 : SC0IE = 1	(9) Set the SC0IE flag of the SC0ICR register to "1" to enable interrupts. If the interrupt request flag (SC0IR of the SC0ICR register) had already been set, clear SC0IR before an interrupt is enabled. [Chapter 3 3-1-4. Interrupt Flag Setup]

Setup Procedure	Description
(10) Start serial interface transmission. Transmission data→SC0TRB (x'3F55') Reception data→input to SBI0 pin.	(10) Set the transmission data to the serial interface 0 transmission / reception shift register (SC0TRB). Then, an internal clock is generated to start transmission / reception. After the transmission has finished, serial interface 0 interrupt SC0IRQ is generated.

Note : In (2), each settings can be set at once.

When only reception with 3 channels is operated, set SC0SBOS of the SC0MD3 register to "0" and select a port. The SBO0 pin can be used as a general port.

When SBO0 / SBI0 pin are connected for communication with 2 lines, the SBO0 pin inputs / outputs serial data. The port direction control register P0DIR switches input / output. At reception, set SC0SBIS of the SC0MD3 register to "1", always, to select "serial data input". The SBI0 pin can be used as a general port.

If the SC0IOM flag of the SC0MD3 register is set to "1", the SBI0 pin can be used as port. When the SBO0 pin is input mode, reception is operated, and when it is output mode, transmission is operated.

When the register except the SC0TRB is written or rewritten, set the SC0SBOS, SC0SBIS flag to "0".

When the internal clock is used as clock source, write dummy data to the SC0TRB register after setting the SC0SBIS flag and the SC0SBOS flag of the SC0MD3 register to "1". Even if the reception is operated again, write dummy data to the SC0TRB register.

10-3-3 Half-duplex UART Serial Interface

Serial interface 0 can be used for half-duplex UART communication. Table 10-3-11 shows UART serial interface functions.

Table 10-3-11 UART Serial Interface Functions

Communication style	UART(Half-duplex)
Interrupt	SC0IRQ(transmission, reception)
Used pins	TXD(output, input) RXD(input)
First transfer bit	MSB/LSB
Parity bit selection	√
Parity bit control	0 parity 1 parity odd parity even parity
Frame selection	7 bits + 1 stop 7 bits + 2 stops 8 bits + 1 stop 8 bits + 2 stops
Maximum transfer rate	625 kbps

■Selection of Half-duplex UART Serial Interface

When the serial interface 0 is used as half-duplex UART serial interface, set the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "1".

■Activation Factor for Communication

At transmission, if any data is written to the transmission / reception shift register SC0TRB, a start bit (Data is changed from "H" to "L") is generated to start transfer. At reception, if a start bit (Data is changed from "H" to "L") is received, communication is started. At reception, if the data length of "L" is longer than 0.5 bit, that can be regarded as a start bit.

■Transmission

Data transfer is automatically started by writing data to the transmission / reception shift register SC0TRB after setting the SC0SBOS flag of the SC0MD3 register to "1". During transmission, reception and start bit input are disabled.

■Reception

When the SC0SBIS flag of the SC0MD3 register is set to "1" and a start bit is received, reception is started after the transfer bit counter is set as frame mode is specified. During reception, transmission is disabled.

■Transfer Bit Count Setup

The transfer bit count is automatically set after the frame mode is specified by the SC0FM1 to 0 flag of the SC0MD2 register. If the SC0CMD flag of the SC0CTR register is set to "1", and UART communication is selected, the synchronous serial data transfer bit count selection flag SC0LNG2 to 0 of the SC0MD0 register is automatically set.

■Input Edge / Output Edge Setup

The SC0CE 1-0 flag of the SC0MD0 register set an output edge of the transmission data, an input edge of the received data. At UART communication, the transfer clock is not necessary, but the SC0CE1-0 flag should be set to decide the timing of the data transmission / reception in this serial interface. At UART communication, generally, set the SC0CE1-0 flag to "00", the transmission data output edge to "falling", and the reception data input edge to "rising". Refer to Table 10-3-2 (X-16) for Input Edge / Output Edge Setup detail.

■Data Input Pin Setup

The communication mode can be selected from with 2 channels (data output pin (TXD pin), data input pin (RXD pin)), or with 1 channel (data I/O pin TXD pin). The RXD pin can be used only for serial data input. The TXD pin can be used for serial data input or output. The SC0IOM flag of the SC0MD3 register can specify which pin, RXD or TXD to input the serial data. "Data input from TXD pin" is selected to be with 1 channel communication. At switching transmission / reception, TXD pin's direction should be controlled by the P0DIR0 flag of the P0DIR register. At that time, the RXD pin is not used, so that it can be used as a general port.

■Frame Mode and Parity Check Setup

Figure 10-3-11 shows the data format at UART communication.

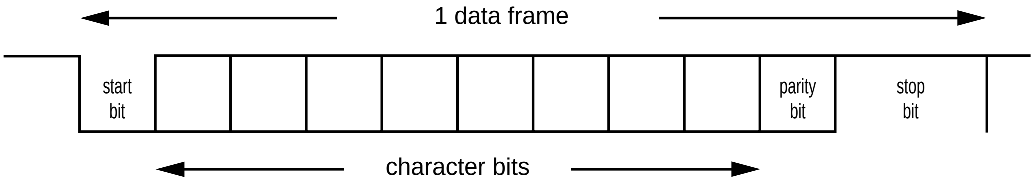


Figure 10-3-11 UART Serial Interface Transmission / Reception Data Format

The transmission / reception data consists of start bit, character bit, parity bit and stop bit.
Table 10-3-12 shows its kinds to be set.

Table 10-3-12 UART Serial Interface Transmission / Reception Data

Start bit	1 bit (must be 'L')
Character bit	7, 8 bits
Parity bit	fixed to 0, fixed to 1, even, odd, none
Stop bit	1, 2 bits (noramally 'H')

The SC0FM1 to 0 flag of the SC0MD2 register sets the frame mode. Table 10-3-13 is shown the UART serial interface frame mode setting. If the SC0CMD flag of the SC0CTR register is set to "1", and UART communication is selected, the SC0LNG2 to 0 flag of the SC0MD0 register is automatically set.

Table 10-3-13 UART Serial Interface Frame Mode

SC0MD2 register		Frame mode
SC0FM1	SC0FM0	
0	0	Character bit 7 bits + Stop bit 1 bit
0	1	Character bit 7 bits + Stop bit 2 bits
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

Parity bit is to detect wrong bits with transmission / reception data.
Table 10-3-14 shows kinds of parity bit. The SC0NPE, SC0PM1 to 0 flag of the SC0MD2 register set parity bit.

Table 10-3-14 Parity Bit of UART Serial Interface

SC0MD2 register			Parity bit	Setup
SC0NPE	SC0PM1	SC0PM0		
0	0	0	fixed to 0	Set parity bit to "0".
0	0	1	fixed to 1	Set parity bit to "1".
0	1	0	odd parity	Control the total number of "1" of parity bit and character bit should be odd.
0	1	1	even parity	Control the total number of "1" of parity bit and character bit should be even.
1	-	-	none	Do not add parity bit.

■Break Status Transmission Control Setup
The SC0BRKE flag of the SC0MD2 register generates the break status. If SC0BRKE is set to "1" to select the break transmission, all bits from start bits to stop bits transfer "0".

■Reception Error
At reception , there are 3 types of error ; overrun error, parity error and framing error. Reception error can be determined by the SC0ORE, SC0PEK and SC0FEF flag of the SC0CTR register. Even one of those errors is detected, the SC0ERE flag of the SC0MD1 register is set to "1". The reception error flag is renewed at generation of the reception complete interrupt SC0IRQ. The judgement of the received error flag should be operated until the next communication has finished. The communication operation does not have any effect on those error flags. Table 10-3-15 shows the list of reception error source.

Table 10-3-15 Reception Error Source of UART Serial Interface

Flag	Error	Error source	
SC0ORE	Overrun error	Next data is received before reading the receive buffer.	
SC0PEK	Parity error	at fixed to 0	when parity bit is "1"
		at fixed to 1	when parity bit is "0"
		odd parity	The total of "1" of parity bit and character bit is even.
		even parity	The total of "1" of parity bit and character bit is odd.
SC0FEF	Framing error	Stop bit ('H') is not detected.	

■Judgement of Break Status Reception

Reception at break status can be judged. If all received data from start bit to stop bit is "0", the SC0BRKF flag of the SC0MD1 register is set and regard the break status. The SC0BRKF flag is set at generation of the reception complete interrupt SC0IRQ.

■Selection of Start Condition

The SC0STE flag of the SC0MD0 register is originally to select start condition of the synchronous serial data communication. When serial interface 0 is used as half-duplex UART serial interface, set the SC0STE flag always to "0" to prevent the following errors.

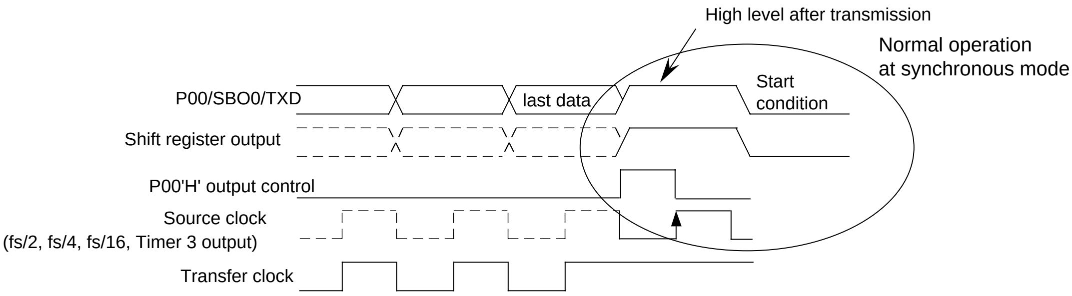
< Caution >

At UART communication, set the SC0STE flag of the SC0MD register to "0".

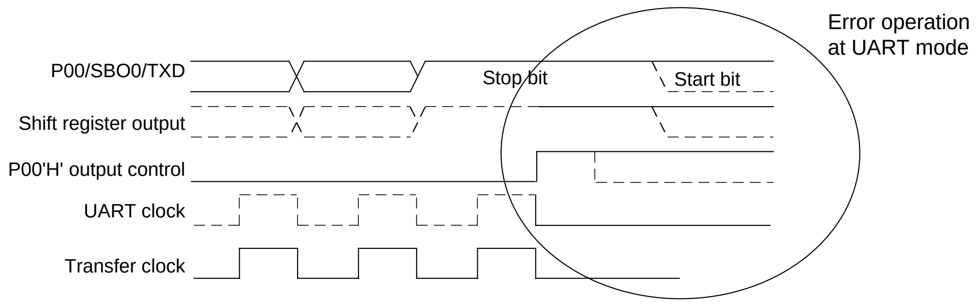
< Error >

At UART transmission, when the SC0STE flag is "1", start bit becomes "H" at the 2nd transmission and after.

[At synchronous serial data transmission (as the SC0STE flag = 1)]



[At UART transmission (as the SC0STE flag = 1)]



■Other Control Flags
The following flags need not to be set at UART communication.

Table 10-3-16 Other Control Flags

Register	Flag	Detail
SC0MD0	SC0LNG2 to 0	Selection ot the transfer bit count (automatically set)
SC0MD1	SC0CKM	Selection of the 1/8 division (automatically set)
SC0MD3	SC0SBTS	Selection of the SBT pin's function
	SC0SBTM	Selection of the SBT pin's style

The following items are the same to clock synchronous serial interface.
Reference as follows ;

■First Transfer Bit Setup
Refer to : X-13

■Transfer Bit Count and First Transfer Bit
Refer to : X-15

■Received Data Buffer
Refer to : X-15

■Receive Bit Count and First Transfer Bit
Refer to : X-15

■BUSY Flag Operation
Refer to : X-18

■Transmission Timing

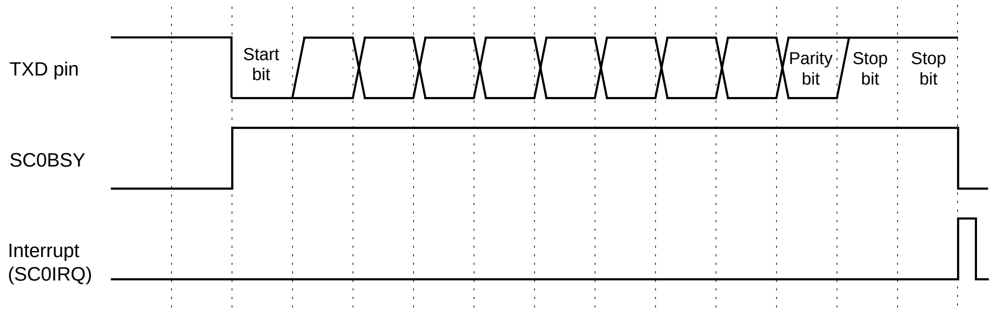


Figure 10-3-12 Transmission Timing (parity bit is enabled)

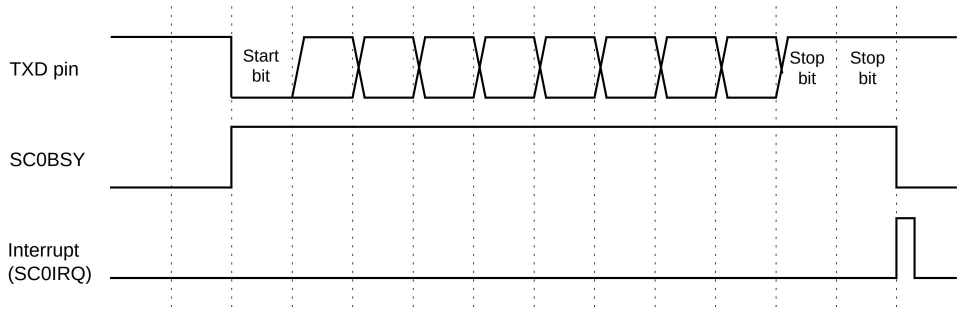


Figure 10-3-13 Transmission Timing (parity bit is disabled)

■Reception Timing

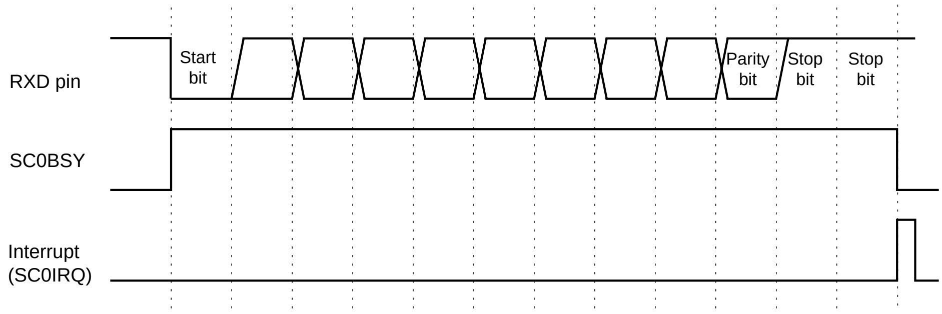


Figure 10-3-14 Reception Timing (parity bit is enabled)

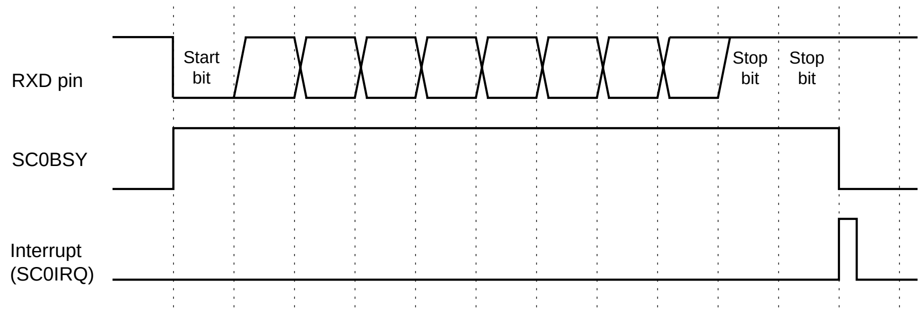
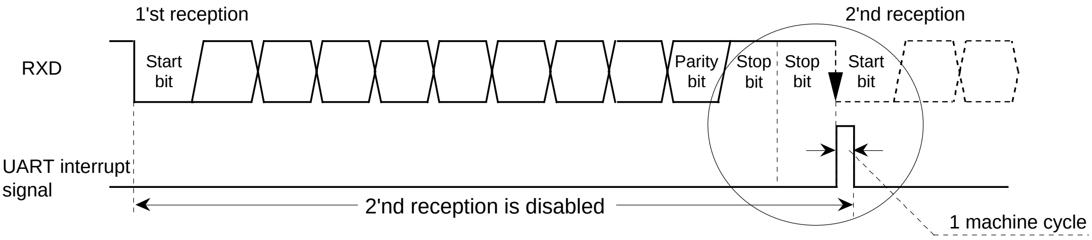


Figure 10-3-15 Reception Timing (parity bit is disabled)

■Sequence Communication



On the above sequence communication, this UART cannot regard start bit when the "H" period of the interrupt signal generated inside at reception complete and the falling edge of start bit input from the RXD pin are happened at the same time (1 machine cycle). Therefore, from the 2nd reception, the operation cannot be properly executed.

To prevent this, the reception interrupt signal and the falling edge of the start bit should not be happened at the same time.
There are 2 ways to solve it.

Method 1 (by stop bit)
Set the stop bit at the transmission side to "2 bits", and set the stop bit at the reception side to "1 bit".
(For parity bit, set the same to both sides of the reception and transmission.)

Method 2 (by parity bit)
Set the transmission parity bit to "always 1", and set the reception parity bit to "none".
(For stop bit, set the same to both sides of the reception and transmission. At the reception, parity bit is regarded as one of stop bit.)

This error can be prevented if one of the above methods can be enabled.
Both methods do not depend on the combination of the oscillation frequency and the baud rate timer setup.

■Transfer Rate

Baud rate timer (timer 3) can set any transfer rate.

Table 10-3-17 shows the setup example of the transfer rate. For detail of the baud rate timer setup, [☞ Chapter 5. 5-8 serial interface transfer clock output operation]

Table 10-3-17 UART Serial Interface Transfer Rate Setup Register

Setup	Register	Page
Serial 0 clock source (timer 3 output)	SC0MD1	X - 7
Timer 3 clock source	TM3MD	V - 8
Timer 3 compare register	TM3OC	V - 6

Timer 3 compare register is set as follows ;

overflow cycle = (set value of compare register + 1) $\times$ timer clock cycle

baud rate = 1 / (overflow cycle $\times$ 2 $\times$ 8) ("8" means that clock source is divided by 8)

Therefore,

set value of compare register = timer clock frequency / (baud rate $\times$ 2 $\times$ 8) - 1

For example, if baud rate should be 300 bps at timer 3 clock source fs/4 (fosc = 8 MHz, fs = fosc/2), set value should be as follows ;

Set value of compare register = $(8 \times 10^6 / 2 / 4) / (300 \times 2 \times 8) - 1$

= 207

= x'CF'

Timer 3 clock source and the set values of timer 3 compare register at the standard transfer rate are shown on the following page.

> ! At UART communication, "clock source is divided by 8" is selected, regardless of the setup for the SC0CKM flag of the SC0MD1 register.

Table 10-3-18 UART Serial Interface Transfer Rate and Timer 3 Compare Register (decimal)

fosc (MHz)	Clock Source (timer 3)	Transfer Rate (bps)											
		300		1200		2400		4800		9600		19200	
		Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value
4.00	fosc	-	-	207	1202	103	2403	51	4807	25	9615	12	19230
	fs/4	103	300	-	-	-	-	-	-	-	-	-	-
	fs/16	-	-	-	-	-	-	-	-	-	-	-	-
4.19	fosc	-	-	217	1201	108	2402	54	4762	15	9699	-	-
	fs/4	108	300	-	-	-	-	-	-	-	-	-	-
	fs/16	-	-	-	-	-	-	-	-	-	-	-	-
8.00	fosc	-	-	-	-	207	2404	103	4807	51	9615	25	19230
	fs/4	207	300	51	1201	-	-	-	-	-	-	-	-
	fs/16	-	-	-	-	-	-	-	-	-	-	-	-
8.38	fosc	-	-	-	-	217	2403	108	4805	54	9523	26	19398
	fs/4	217	300	54	1190	-	-	-	-	-	-	-	-
	fs/16	-	-	-	-	-	-	-	-	-	-	-	-
12.00	fosc	-	-	-	-	-	-	155	1808	77	9615	38	19230
	fs/4	-	-	77	1202	38	2403	-	-	-	-	-	-
	fs/16	77	300	-	-	-	-	-	-	-	-	-	-
16.00	fosc	-	-	-	-	-	-	207	4808	103	9615	51	19230
	fs/4	-	-	103	1202	51	2404	-	-	-	-	-	-
	fs/16	103	300	-	-	-	-	-	-	-	-	-	-
16.76	fosc	-	-	-	-	-	-	217	4805	108	9610	54	19045
	fs/4	-	-	108	1201	54	2381	-	-	-	-	-	-
	fs/16	108	300	-	-	-	-	-	-	-	-	-	-
20.00	fosc	-	-	-	-	-	-	-	-	129	9615	64	19231
	fs/4	-	-	129	1202	64	2404	32	4735	-	-	-	-
	fs/16	129	300	-	-	-	-	-	-	-	-	-	-

■Pin Setup (1, 2 channels, at transmission)

Table 10-3-19 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXD pin, RXD pin, regardless of those pins are independent / connected. The RXD pin can be used as general port (P01).

Table 10-3-19 UART Serial Interface Pin Setup (1, 2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXD pin	RXD pin
Pin	P00	P01
TXD / RXD pins	TXD / RXD pins connected or independe	
	SC0MD3(SC0IOM)	
Function	Serial data output	"1" input
	SC0MD3(SC0SBOS)	SC0MD3(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0MD3(SC0SBOM)	
I/O	Output mode	-
	P0DIR(P0DIR0)	
Pul-up	Added / Not added	-
	P0PLU(P0PLU0)	

■Pin Setup (2 channels, at reception)

Table 10-3-20 shows the pins setup at UART serial interface reception with 2 channels (TXD pin, RXD pin). The TXD pin can be used as general port (P00).

Table 10-3-20 UART Serial Interface Pin Setup (2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXD pin	RXD pin
Pin	P00	P01
TXD / RXD pin	TXD / RXD pins independent	
	SC0MD3(SC0IOM)	
Function	port	serial data input
	SC0MD3(SC0SBOS)	SC0MD3(SC0SBIS)
Style	-	-
I/O	-	input mode
	-	P0DIR(P0DIR1)
Pull-up	-	added / not added
		P0PLU(P0PLU1)

■Pin Setup (1 channel, at reception)

Table 10-3-21 shows the pin setup at UART serial interface reception with 1 channel (TXD pin). The RXD pin can be used as general port (P01).

Table 10-3-21 UART Serial Interface Pin Setup (1 channel, at reception)

<table>
<tr><td rowspan="2">Setup item</td><td>Data output pin</td><td>Serial unused pin</td></tr>
<tr><td>TXD pin</td><td>RXD pin</td></tr>
<tr><td>Pin</td><td>P00</td><td>P01</td></tr>
<tr><td rowspan="2">TXD / RXD pin</td><td colspan="2">TXD / RXD pins connected</td></tr>
<tr><td colspan="2">SC0MD3(SC0IOM)</td></tr>
<tr><td rowspan="2">Function</td><td>Port</td><td>Serial data input</td></tr>
<tr><td>SC0MD3(SC0SBOS)</td><td>SC0MD3(SC0SBIS)</td></tr>
<tr><td>Style</td><td>-</td><td>-</td></tr>
<tr><td rowspan="2">I/O</td><td>Input mode</td><td>-</td></tr>
<tr><td>P0DIR(P0DIR0)</td><td>-</td></tr>
<tr><td rowspan="2">Pull-up</td><td>added / not added</td><td rowspan="2">-</td></tr>
<tr><td>P0PLU(P0PLU0)</td></tr>
</table>

10-3-4 Setup Example

■Transmission Setup

The setup example at UART transmission with serial interface 0 is shown.

Table 10-3-22 shows the conditions at transmission.

Table 10-3-22 UART Interface Transmission Setup

Setup item	set to
TXD / RXD pin	connected (with 1 channel)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	timer 3 output
TXD pin type	Nch open-drain
Pull-up resistor of TXD pin	not added
Parity bit add / check	"0"add / check
Serial interface 0 interrupt	Enable.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the UART communication. SC0CTR (x'3F54') bp6 : SC0CMD = 1	(1) Set the SC0CMD flag of the SC0CTR register to "1" to select the UART communication.
(2) Select the first bit to be transferred. SC0MD0 (x'3F50') bp4 : SC0DIR = 0	(2) Select MSB as first transfer bit by the SC0DIR flag of the SC0MD0 register.
(3) Select the start condition. SC0MD0 (x'3F50') bp3 : SC0STE = 0	(3) Set the SC0STE flag of the SC0MD0 register to disable start condition. [☞ X-33 ■Selection of Start Condition]
(4) Select the clock source. SC0MD1 (x'3F51') bp4-3 : SC0CK1-0 = 11	(4) Set the SC0CK1-0 flag to select timer 3 output as a clock source.
(5) Select the parity bit. SC0MD2 (x'3F52') bp0 : SC0NPE = 0 bp2-1 : SC0PM1-0 = 00	(5) Set the SC0NPE flag of the SC0MD2 register to select "parity is enabled", and set the SC0PM1-0 flag to select "0 added".

Setup Procedure	Description
(6) Specify the flame mode. SC0MD2 (x'3F52') bp4-3 : SC0FM1-0 = 11	(6) Set the SC0FM1-0 flag of the SC0MD2 register to "11" to select 8 bits data + 2 stop bits at the frame mode.
(7) Control the output data. SC0MD2 (x'3F52') bp5 : SC0BRKE = 0	(7) Set the SC0BRKE flag of the SC0MD2 register to "0" to select serial data transmission.
(8) Control the pin type. SC0MD3 (x'3F53') bp4 : SC0SBOM = 1 P0PLU (x'3F40') bp0 : P0PLU0 = 0	(8) Set the SC0SBOM flag of the SC0MD3 register to "1" to select N-ch open drain for the TXD pin. Set the P0PLU0 flag of the P0PLU register to "0" not to add pull-up resistor.
(9) Select the reception mode. SC0MD3 (x'3F53') bp5 : SC0IOM = 1	(9) Set the SC0IOM flag of the SC0MD3 register to "1" to set the SBO0 to transmission / reception port.
(10) Control the pin direction. P0DIR (x'3F30') bp0 : P0DIR0 = 1	(10) Set the P0DIR0 flag of the P0DIR register to "1" to set P00 to output mode.
(11) Select the interrupt level. SC0ICR (x'03FE8') bp7-6 : SC0LV1-0 = 10	(11) Select the interrupt level by the SC0LV1-0 flag of the serial interface 0 interrupt control register (SC0ICR).
(12) Enable the interrupt. SC0ICR (x'3FE8') bp1 : SC0IE = 1	(12) Set the SC0IE flag of the SC0ICR register to "1" to enable the interrupt request. If any interrupt request flag had already been set, clear it. [Chapter 3. 3-1-4 Interrupt Flag Setup]
(13) Set the baud rate timer.	(13) Set the baud rate timer by the TM3MD register, TM3OC register. And set the TM3EN flag to "1" to operate timer 3. [Chapter 5. 5-8 Serial interface transfer clock output]
(14) Set the serial interface communication. SC0MD3 (x'3F53') bp2 : SC0SBOS = 1	(14) Set the SC0SBOS flag of the SC0MD3 register to "1" to set the serial interface communication.
(15) Start the serial interface communication. SC0TRB (x'3F55')	(15) Set the transfer data to the SC0TRB register. And the serial interface communication is started.

Only timer 3 can be used as a baud rate timer.
For baud rate setup, [☞ Chapter 5. 5-8 Serial Interface Transfer Clock Output]

Serial interface 0 is operated by setting the SC0SBOS flag or the SC0SBIS flag of the SC0MD3 register to "1".
The SC0SBOS flag or the SC0SBIS flag should be set after all conditions are set.
After that, at transmission, the communication is started by writing data to the SC0TRB.

When a register except the SC0TRB is written / rewritten, set the SC0SBOS, the SC0SBIS flag to "0", in advance.

When the TXD / RXD pin are connected for communication with 1 channel, the TXD pin inputs / outputs serial data. The port direction control register P0DIR should be set, for switching input / output. The RXD pin can be used as a general port.

When the serial interface port is enabled, if the SC0CE1-0 flag of the SC0MD0 register is switched, the transfer bit count may be changed. If it is used as half-duplex UART serial interface, setting the SC0CE1-0 flag fixed to "00" is recommended.

After transmission has completed, the TXD pin is "H" level.

If the frame mode is set by the SC0FM flag of the SC0MD2 register, the SC0LNG2-0 flag of the SC0MD0 register is automatically set.

After the transfer has completed, the transfer bit count in the SC0LNG2-0 flag of the SC0MD0 register is automatically set.

At UART transmission, set the SC0SBOS flag of the SC0MD3 register to "1", and set the SC0SBIS flag to "0". Setting both of flags to "1" is disabled.

■Reception Setup

The setup example at UART reception with serial interface 0 is shown.

Table 10-3-23 shows the conditions at reception.

Table 10-3-23 UART Interface Transmission Reception Setup

Setup item	set to
TXD / RXD pin	connected (with 1 channel)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	timer 3
TXD pin type	Nch open-drain
Pull-up resistor of TXD pin	added
Parity bit add / check	"0"add / check
Serial 0 interface interrupt	Enable.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the UART communication. SC0CTR (x'3F54') bp6 : SC0CMD = 1	(1) Set the SC0CMD flag of the SC0CTR register to "1" to select the UART communication.
(2) Select the first bit to be transferred. SC0MD0 (x'3F50') bp4 : SC0DIR = 0	(2) Select MSB as first transfer bit by the SC0DIR flag of the SC0MD0 register.
(3) Select the start condition. SC0MD0 (x'3F50') bp3 : SC0STE = 0	(3) Set the SC0STE flag of the SC0MD0 register to disable start condition. [☞ X-33 ■Selection of Start Condition]
(4) Select the clock source. SC0MD1 (x'3F51') bp4-3 : SC0CK1-0 = 11	(4) Set the SC0CK1-0 flag of the SC0MD1 register to select timer 3 output as a clock source.
(5) Select the parity bit. SC0MD2 (x'3F52') bp0 : SC0NPE = 0 bp2-1 : SC0PM1-0 = 00	(5) Set the SC0NPE flag of the SC0MD2 register to select "parity is enabled", and set the SC0PM1-0 flag to select "0 checked".
(6) Specify the frame mode. SC0MD2 (x'3F52') bp4-3 : SC0FM1-0 = 11	(6) Set the SC0FM1-0 flag of the SC0MD2 register to "11" to select 8 bits data + 2 stop bits at the frame mode.
(7) Select the reception mode. SC0MD3 (x'3F53') bp5 : SC0IOM = 1	(7) Set the SC0IOM flag of the SC0MD3 register to "1" to set the SBO0 to transmission / reception port.

Setup Procedure	Description
(8) Control the pin direction. P0DIR (x'3F30') bp0 : P0DIR0 = 0	(8) Set the P0DIR0 flag of the P0DIR register to "0" to set the TXD pin to input mode.
(9) Add pull-up resistor to the TXD pin. P0PLU (x'3F40') bp0 : P0PLU0 = 1	(9) Set the P0PLU0 flag of the P0PLU register to add pull-up resistor to the TXD pin.
(10) Select the interrupt level. SC0ICR (x'03FE8') bp7-6 : SC0LV1-0 = 10	(10) Select the interrupt level by the SC0LV1-0 flag of the serial interface 0 interrupt control register (SC0ICR).
(11) Enable the interrupt. SC0ICR (x'3FE8') bp1 : SC0IE = 1	(11) Set the SC0IE flag of the SC0ICR register to "1" to enable the interrupt request. If any interrupt request flag had already been set, clear it. [Chapter 3. 3-1-4 Interrupt Flag Setup]
(12) Set the baud rate timer.	(12) Set the baud rate timer by the TM3MD register, TM3OC register. And set the TM3EN flag to "1" to operate timer 3.
(13) Set the serial interface communication. SC0MD3 (x'3F53') bp1 : SC0SBIS = 1	(13) Set the SC0SBIS flag of the SC0MD3 register to "1" to set the serial interface communication.
(14) Start the serial interface reception. Received data → Input to TXD	(14) After start bit is received by inputting serial interface data from the TXD pin, the received data is stored to the serial interface transmission / reception shift register (SC0TRB). When the reception has completed, the serial interface 0 interrupt (SC0IRQ) is generated, then, the received data is stored to the received buffer (SC0RXB).

When the TXD / RXD pin are connected for communication with 1 channel, the TXD pin inputs / outputs serial data. The port direction control register P0DIR should be set, for switching input / output. At reception, the SC0SBIS flag of the SC0MD3 register should be set to "1" and select "serial interface data input". The RXD pin can be used as a general port.

Only timer 3 can be used as a baud rate timer.
For baud rate setup, [Chapter 5. 5-8 Serial Interface Transfer Clock Output]

Serial interface 0 is operated by setting the SC0SBOS flag or the SC0SBIS flag of the SC0MD3 register to "1".
The SC0SBOS flag or the SC0SBIS flag should be set after all conditions are set.
After that, at reception, the communication is started by receiving start bit.

When a register except the SC0TRB is written / rewritten, set the SC0SBOS, the SC0SBIS flag of the SC0MD3 register to "0", in advance.

When the TXD / RXD pin are connected for communication with 1 channel, the TXD pin inputs / outputs serial data. The port direction control register P0DIR should be set, for switching input / output. The RXD pin can be used as a general port.

When the serial interface port is enabled, if the SC0CE1-0 flag of the SC0MD0 register is switched, the transfer bit count may be changed. If it is used as half-duplex UART serial interface, setting the SC0CE1-0 flag fixed to "00" is recommended.

After reception has completed, the TXD pin is "H" level.

If the frame mode is set by the SC0FM flag of the SC0MD2 register, the SC0LNG2-0 flag of the SC0MD0 register is automatically set.

After the transfer has completed, the transfer bit count in the SC0LNG2-0 flag of the SC0MD0 register is automatically set.

At UART reception, set the SC0SBIS flag of the SC0MD3 register to "1", and set the SC0SBOS flag to "0". Setting both of flags to "1" is disabled.

Chapter 11 Serial Interface 1

11-1 Overview

This LSI contains a serial interface 1 can be used for clock synchronous serial interface communication.

11-1-1 Functions

Table 11-1-1 shows functions of serial interface 1.

Table 11-1-1 Serial Interface 1 Functions

Communication style	clock synchronous
Interrupt	SC1IRQ
Used pins	SBO1,SBI1,SBT1
3 channels type	√
2 channels type	-
Selection of start condition	√
Specification of transfer bit count	1 to 8 bits
Specify of the first transfer bit	√
Specify of input edge / output edge	√
Clock source	fs/2 fs/8 fs/64 timer 3 output external clock
Maximum transfer rate	5.0 MHz
fosc : Machine clock (High speed oscillation) fs : System clock (at NORMAL mode : fs=fosc/2 at SLOW mode : fs=fx/4)	

Set fs/2 as maximum frequency for external clock.

11-1-2 Block Diagram

■Serial Interface 1 Block Diagram

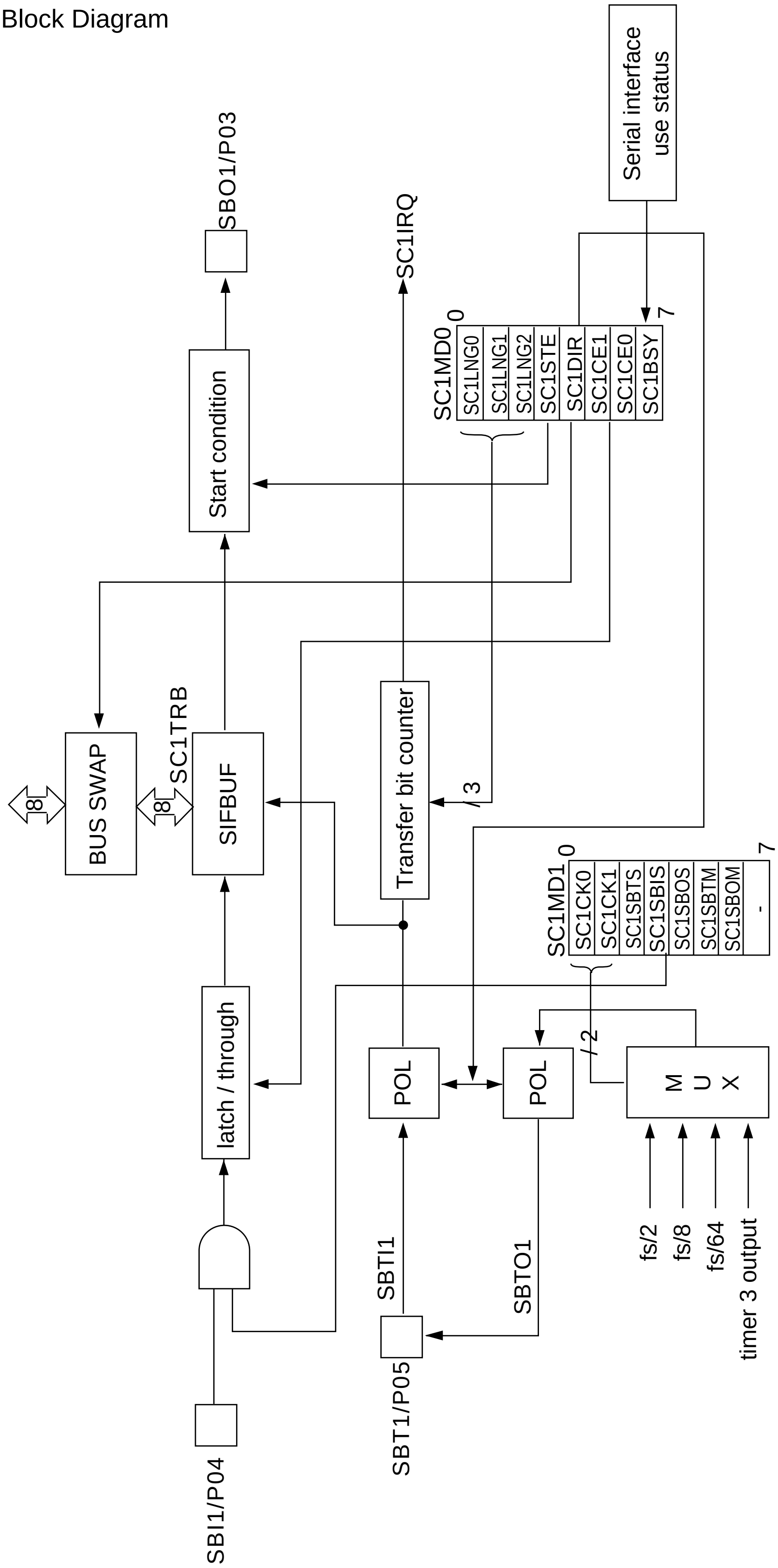


Figure 11-1-1 Serial Interface 1 Block Diagram

11-2 Control Registers

11-2-1 Registers

Table 11-2-1 shows registers to control serial interface 1.

Table 11-2-1 Serial Interface 1 Control Registers

	Register	Address	R/W	Function	Page
Serial 1	SC1MD0	x'03F57'	R/W	Serial interface 1 mode register 0	XI - 6
	SC1MD1	x'03F58'	R/W	Serial interface 1 mode register 1	XI - 7
	SC1TRB	x'03F59'	R/W	Serial interface 1 transmission / reception shift register	XI - 5

R/W : Readable / Writable

11-2-2 Data Register

Serial Interface 1 has a 8-bit data shift register to shift the transmission and reception data.

■Serial Interface 1 Transmission / Reception Shift Register (SC1TRB)

	7	6	5	4	3	2	1	0	
SC1TRB	SC1TRB7	SC1TRB6	SC1TRB5	SC1TRB4	SC1TRB3	SC1TRB2	SC1TRB1	SC1TRB0	(at reset : X X X X X X X X)

Figure 11-2-1 Serial Interface 1 Transmission / Reception Shift Register (SC1TRB : x'03F59', R/W)

11-2-3　Mode Registers

■Serial Interface 1 Mode Register 0 (SC1MD0)

SC1BSY flag is only for reading.

	7	6	5	4	3	2	1	0
SC1MD0	SC1BSY	SC1CE0	SC1CE1	SC1DIR	SC1STE	SC1LNG2	SC1LNG1	SC1LNG0

(At reset : 0 0 0 X X 0 0 0)

SC1LNG2	SC1LNG1	SC1LNG0	Transfer bit count
0	0	0	8 bits
		1	7 bits
	1	0	6 bits
		1	5 bits
1	0	0	4 bits
		1	3 bits
	1	0	2 bits
		1	1 bit

SC1STE	Synchronous serial transfer start condition selection
0	Disable start condition
1	Enable start condition

SC1DIR	First bit to be transfered
0	MSB first
1	LSB first

SC1CE0	SC1CE1	Reception data input edge	Transmission data output edge
0	0	Rising	Falling
0	1	Falling	Rising
1	0	Falling	Falling
1	1	Rising	Rising

SC1BSY	Serial but status
0	Other use
1	Serial transmission inprogress

Figure 11-2-2　Serial Interface 1 Mode Register 0 (SC1MD0 : x'03F57', R/W)

■Serial Interface 1 Mode Register 1 (SC1MD1)

	7	6	5	4	3	2	1	0
SC1MD1	-	SC1SBOM	SC1SBTM	SC1SBOS	SC1SBIS	SC1SBTS	SC1CK1	SC1CK0

(At reset : - 0 0 0 0 0 0 0)

SC1CK1	SC1CK0	Clock source
0	0	fs/2
	1	fs/8
1	0	fs/64
	1	Timer 3 output

SC1SBTS	SBT1 pin function selection
0	Port
1	Serial interface clock pin

SC1SBIS	SBI1 input control (reception enable flag)
0	"0" input
1	Serial interface input

SC1SBOS	SBO1 pin function selection (transmission enable flag)
0	Port
1	Serial interface communication

SC1SBTM	SBT1 pin configuration
0	Push pull output
1	N-ch open drain output

SC1SBOM	SBT1 pin configuration
0	Push pull output
1	N-ch open drain output

Clock source can be set as external clock by setting the SBT1 pin to input mode.

Figure 11-2-3 Serial Interface 1 Mode Register 1 (SC1MD1 : x'03F58', R/W)

11-3 Operation

Serial Interface 1 can be used for clock synchronous serial interface.

11-3-1 Clock Synchronous Serial Interface

■Activation Factor for Communication

Table 11-3-1 shows activation factors for communication. At master, the transfer clock is generated by setting data to the transmission / reception shift register SC1TRB, or by receiving a start condition. At slave, input an external clock, or input an external clock after a start condition is input.

Table 11-3-1 Synchronous Serial Interface Activation Factor

Operation mode			Activation Factor	Sequence communication
Transmission	Master communication	Start condition is enabled	Writing data to serial buffer	√
		Start condition is disabled	Writing data to serial buffer	√
	Slave communication	Start condition is enabled	Clock reception *	√
		Start condition is disabled	Clock reception	√
Reception	Master communication	Start condition is enabled	Start condition is received	√
		Start condition is disabled	Writing data to serial buffer	–
	Slave communication	Start condition is enabled	Start condition is received	√
		Start condition is disabled	Clock reception	√

* When the SC1SBOS flag of the serial interface 1 mode register 1 (SC1MD1) is "1", start condition is output by writing the transmission data to the transmission / reception shift register SC1TRB, then the transmission is started by the slave clock.

When synchronous serial interface is used for master clock reception, it is necessary to write dummy data to the transmission / reception shift register (SC1TRB) for starting master clock. Automatic sequence reception with automatic data transfer can not be used, because it is necessary to write dummy data to serial interface buffer and to read reception data per a frame reception.

Serial data communication of serial interface 1 can be available by setting the SC1SBOS flag or the SC1SBIS flag of the SC1MD1 register to "1". The SC1SBOS flag or the SC1SBIS flag should be set to "1" after all conditions are set.

On the master communication of the clock synchronous, set the SC1SBTS flag to "1" before the SC1SBIS flag or the SC1SBOS flag of the SC1MD1 register is set to "1". But, at the slave communication, the SC1SBTS flag need not to be set to "1".

■Transfer Bit Count

The transfer bit count is selected from 1 bit to 8 bits. Set it by the SC1LNG 2 to 0 flag of the SC1MD0 register (at reset : 000).

The SC1LNG2 to 0 flags change at the opposite edge of the transmission data output edge.

After the transfer has completed, the transfer bit count in the SC1LNG2 to 0 flags of the SC1MD0 register is changed. Except in an 8-bit transfer, reset the transfer bit count at the time of the next transmission.

When the SC1SBOS flag or the SC1SBIS flag of the SC1MD1 register to "1" and the SC1CE1 to 0 flags of the SC1MD0 register are changed, the transfer bit count in the SC1LNG2 to 0 flags of the SC1MD0 register may be incremented.

■Start Condition Setup

Wether or not the start condition is set is controlled by the SC1STE flag of the SC1MD0 register. If a start condition is enabled, and it is being set, a bit counter is cleared to start the communication. After the SC1CE1 flag of the SC1MD0 register is cleared to "0", the start condition is received when a data line (SBI1 pin) is changed from "H" to "L" as a clock line (SBT1 pin) is "H". Also, the SC1CE1 flag is set to "1", that is received when a data line (SBI1 pin) is changed from "H" to "L" as a clock line (SBT1 pin) is "L".

Enabling the start condition drives the SBO1 pin high level for a fixed time interval (1/2 the clock source cycle) after the transmission has completed. If the start condition is disabled, the SBO1 pin will remain at the level of the last data bit.

If the start condition is enabled, the SC1LNG2 to 0 flags of the SC1MD0 register will be cleared when the start condition is received. In this case, the receive bit count is fixed at 8 bits.

■First Transfer Bit Setup

Either MSB or LSB can be selected as a first transfer bit by the SC1DIR flag of the SC1MD0 register.

■Transmission / Reception Data Buffer

The transmission reception shift register, SC1TRB is used as the data register for transmission and reception. Data to be transferred should be set to the SC1TRB. The data is output in sync with the transfer clock and is stored to the SC1TRB bit by bit.

> When switching from transmission to reception, set the SC1SBOS flag of the SC1MD1 register to "0" and then set the SC1SBIS flag to "1". Do not change both of these flags at the same time.

> When switching from reception to transmission, set the SC1SBIS flag of the SC1MD1 register to "0" and then set the SC1SBOS flag to "1". Do not change both of these flags at the same time.

■Tranfer Bit Count and First Transfer Bit

On transmission, when the transfer bit is 1 bit to 7 bits, the data storing method to the transmission / reception shift register SC1TRB is different, depending on the first transfer bit selection. At MSB first, use the upper bits of SC1TRB. When there are 6 bits to be transferred, as shown on figure 11-3-1-1, if data "A" to "F" are stored to bp2 to bp7 of SC1TRB, the transmission is started from "F" to "A". At LSB first, use the lower bits on the program. When there are 6 bits to be transferred, as shown on figure 11-3-1-2, if data "A" to "F" are stored to bp0 to bp5 on the program, the transmission is started from "A" to "F", because their order is changed in the SWAP circuit.

	7	6	5	4	3	2	1	0
SC1TRB	F	E	D	C	B	A		

Figure 11-3-1-1   Transfer Bit Count and First Transfer Bit (starting with MSB)

	7	6	5	4	3	2	1	0
Setting on program			F	E	D	C	B	A

	7	6	5	4	3	2	1	0
SC1TRB	A	B	C	D	E	F		

Figure 11-3-1-2   Transfer Bit Count and First Transfer Bit (starting with LSB)

■Receive Bit Count and First Transfer Bit

On reception, when the transfer bit count is 1 bit to 7 bits, the data reading method from the transmission / reception shift register SC1TRB is different depending on the first transfer bit selection. At MSB first, data are read from the lower bits of SC1TRB. When there are 6 bits to be transferred, as shown on figure 11-3-2-1, if data "F" to "A" are stored to bp0 to bp5 of SC1TRB. Also, data are read as the same way. At LSB first, data are read from the upper bits of SC1TRB. When there are 6 bits to be transferred, as shown on figure 11-3-2-2, if data "A" to "F" are stored to bp0 to bp5 of SC1TRB. But their order is changed in the SWAP circuit, and reading is started from the upper bits.

	7	6	5	4	3	2	1	0
SC1TRB			F	E	D	C	B	A

Figure 11-3-2-1   Receive Bit Count and Transfer First Bit (starting with MSB bit)

	7	6	5	4	3	2	1	0
SC1TRB			A	B	C	D	E	F

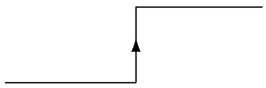
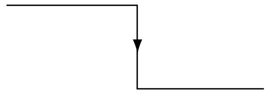
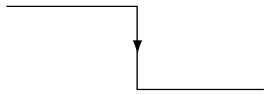
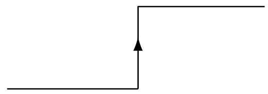
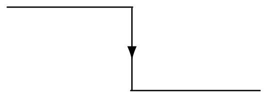
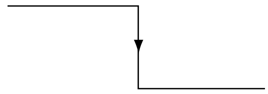
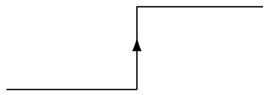
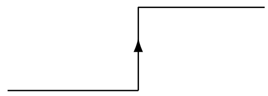
	7	6	5	4	3	2	1	0
Data is read	F	E	D	C	B	A		

Figure 11-3-2-2   Receive Bit Count and Transfer First Bit (starting with LSB bit)

■Input Edge / Output Edge Setup

The SC1CE1 to 0 flag of the SC1MD0 register set an output edge of the transmission data, an input edge of the reception data. As the SC1CE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SC1CE0="0", the reception data is stored at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table 11-3-2　Transmission Data Output Edge and Received Data Input Edge

SC1CE0	SC1CE1	Received data input edge	Transmission data output edge
0	0		
0	1		
1	0		
1	1		

■Clock Setup

The internal clock or the external clock can be selected as clock source. Table 11-3-3 shows internal clock source that the SC1CK1 to 0 register of the SC1MD1 register can set.

Table 11-3-3　Synchronous Serial Interface Internal Clock Source

	Serial interface 1
Clock source (internal clock)	fs/2
	fs/8
	fs/64
	Timer 3 output

■Data Input Pin Setup

Only 3 channels type (clock pin (SBT1 pin), data output pin (SBO1 pin), data input pin (SBI1 pin)) can be selected as the communication mode. SBI1 pin can be used for serial data input. SBO1 pin can be used for serial data output. If only transmission is operated, the SBI1 pin can be used as general I/O pin. And if only reception is operated, the SBO1 pin can be used as general I/O pin.

■BUSY Flag

When the activation factor is generated, shown in table 11-3-1, and the serial interface communication is started, the BUSY flag SC1BSY of the SC1MD0 register is set to "1". That is cleared to "0" when the communication complete interrupt SC1IRQ is generated.

■Trasnmission Timing

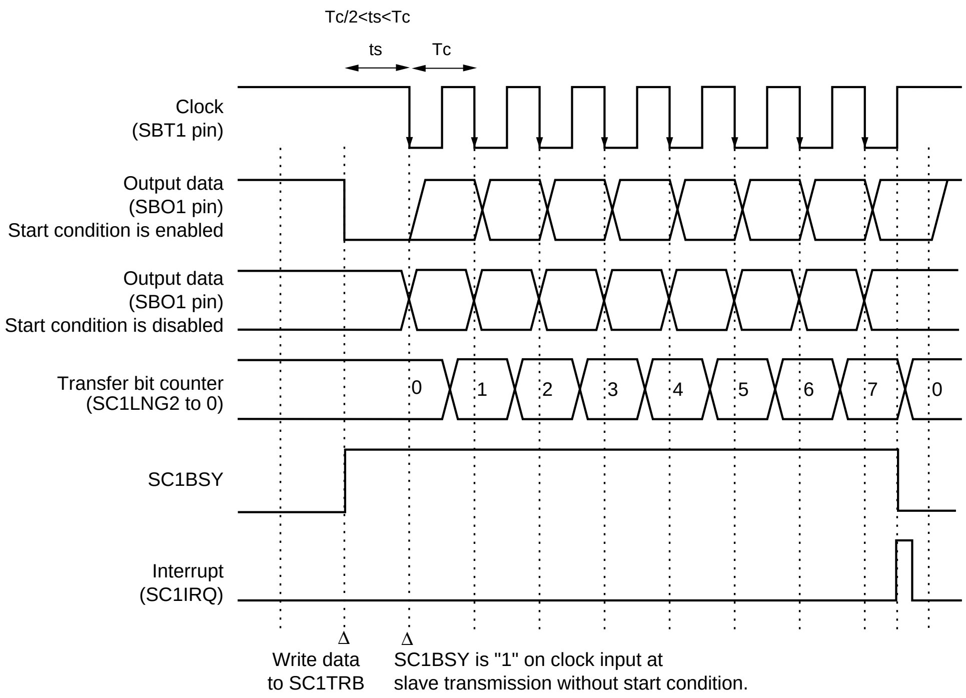


Figure 11-3-3 Transmission Timing (at falling edge)

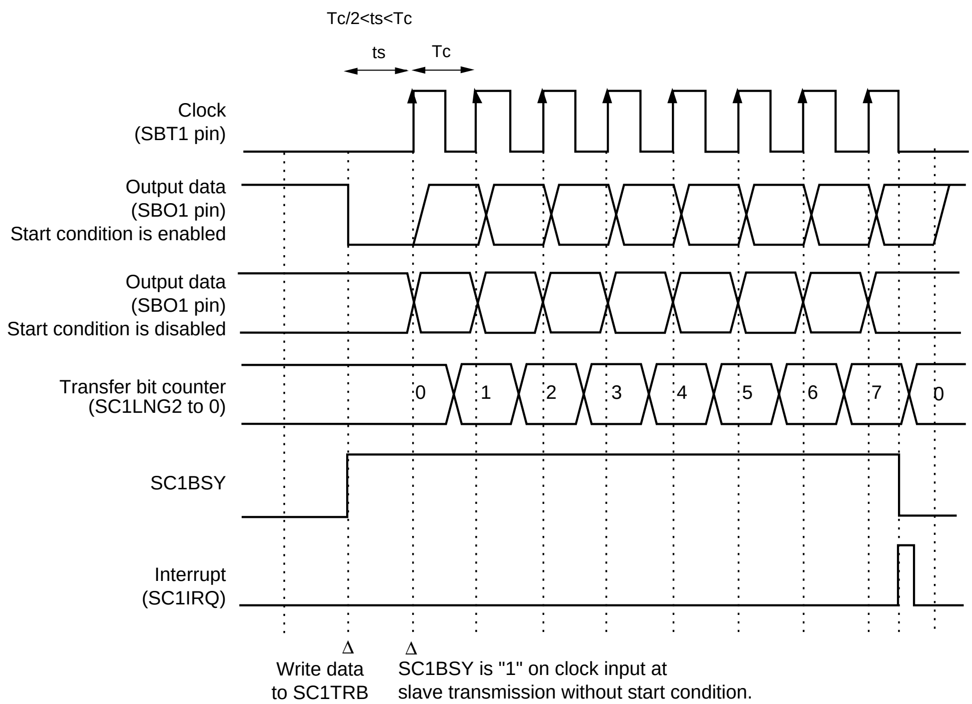


Figure 11-3-4 Transmission Timing (at rising edge)

■Reception Timing

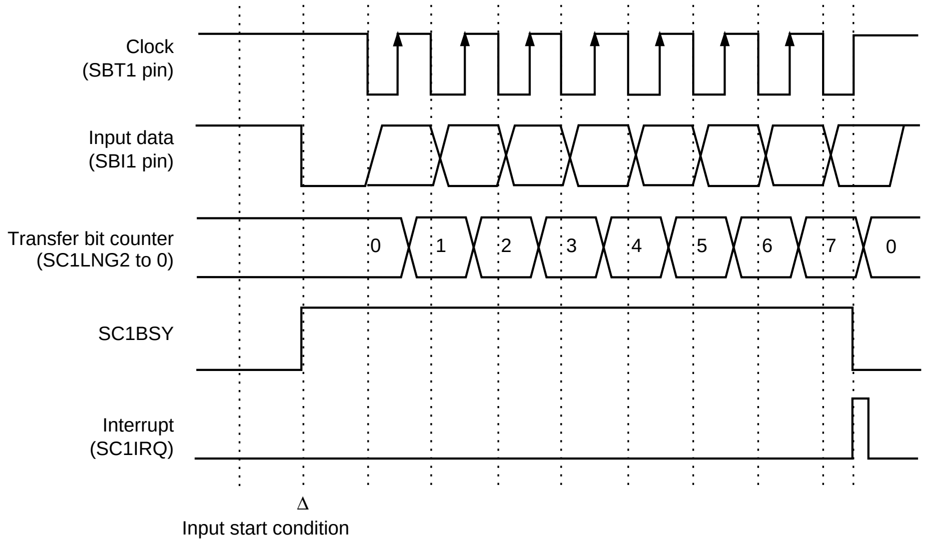


Figure 11-3-5 Reception Timing (at rising edge, start condition is enabled)

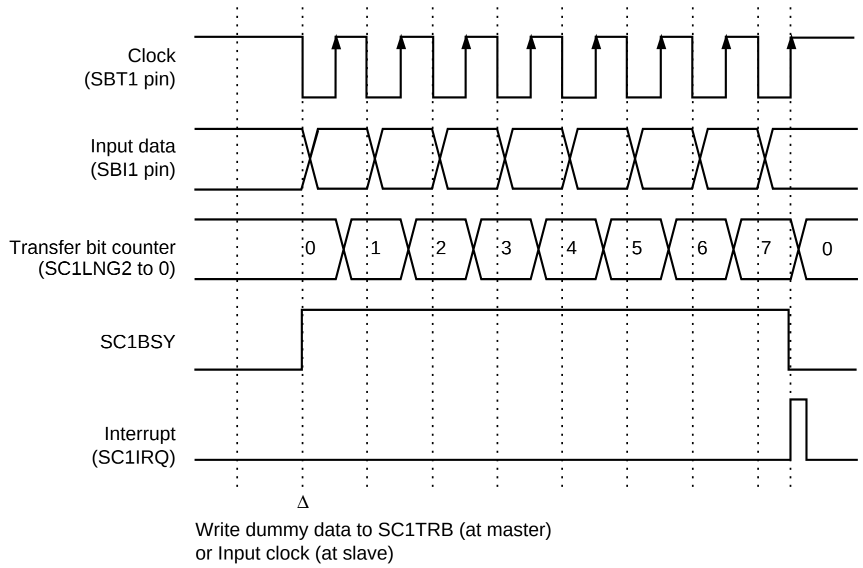


Figure 11-3-6 Reception Timing (at rising edge, start condition is disabled)

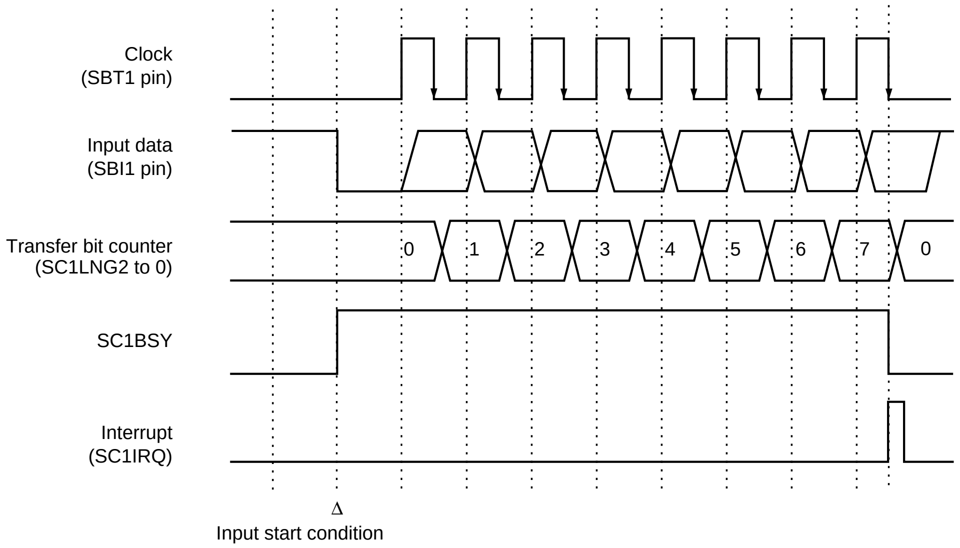


Figure 11-3-7 Reception Timing (at falling edge, start condition is enabled)

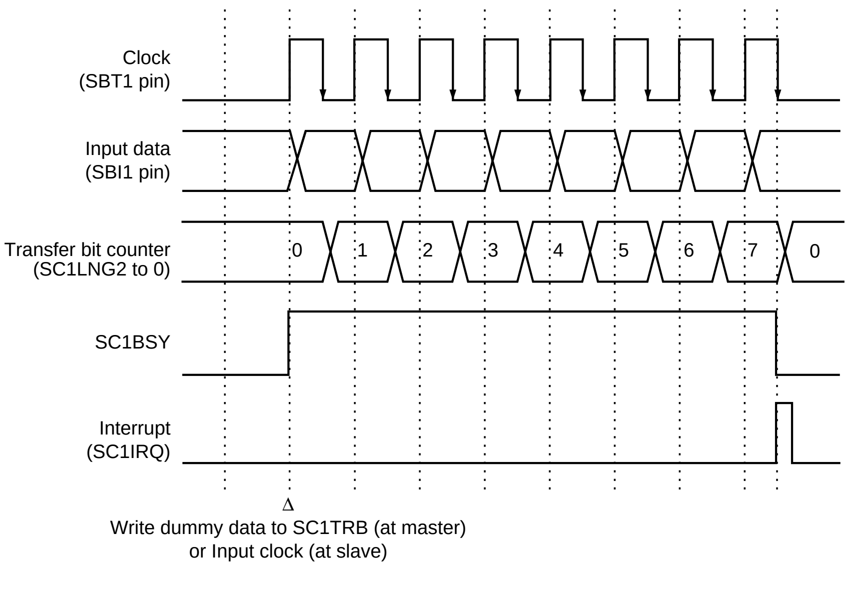


Figure 11-3-8 Reception Timing (at falling edge, start condition is disabled)

■Transmission / Reception Simultaneous Timing

When transmission and reception are operated at the same time, set the SC1CE0 to 1 flag of the SC1MD0 register to "00" or "01". Data is received at the opposite edge of the transmission clock, so that the reception clock should be the opposite edge of the transmission clock from the other side.

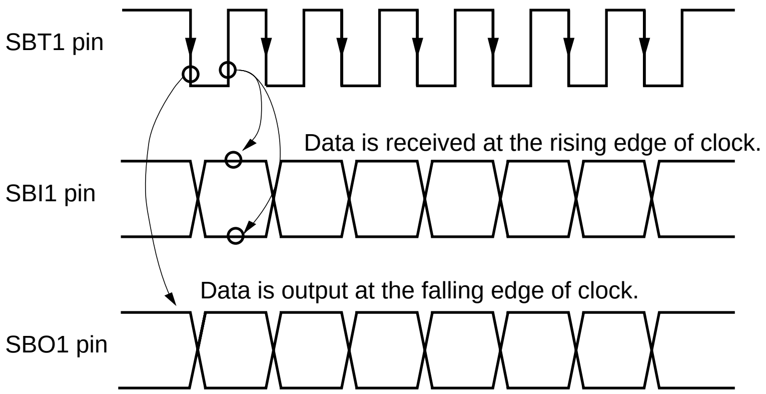


Figure 11-3-9 Transmission / Reception Timing
(Reception : at rising edge, Transmission : at falling edge)
(SC1CE0=0, SC1CE1=0)

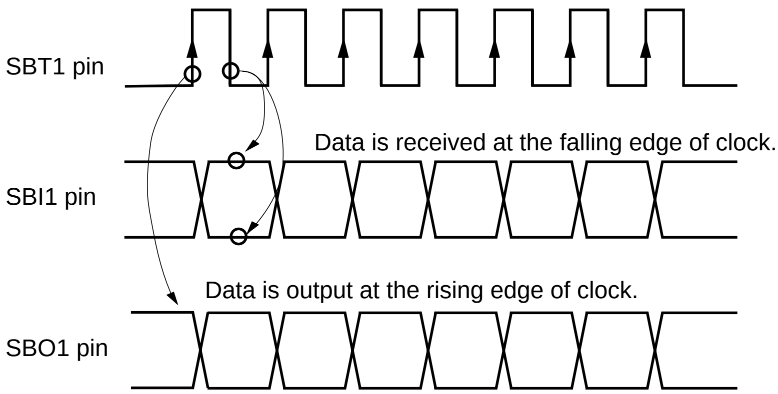


Figure 11-3-10 Transmission / Reception Timing
(Reception : at falling edge, Transmission : at rising edge)
(SC1CE0=0, SC1CE1=1)

■Pins Setup (3 channels type, at transmission)

Table 11-3-4 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at transmission.

Table 11-3-4 Setup for Synchronous Serial Interface Pin (3 channels type, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Internal clock	External clock
Pin	P03	P04	P05	
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC1MD1 (SC1SBOS)	SC1MD1(SC1SBIS)	SC1MD1(SC1SBTS)	
Style	Push pull / Nch open-drain	-	Push pull / Nch open-drain	Push pull / Nch open-drain
	SC1MD1 (SC1SBOM)		SC1MD1(SC1SBTM)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR3)		P0DIR(P0DIR5)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	P0PLU(P0PLU3)		P0PLU(P0PLU5)	

■Pins Setup (3 channels type, at reception)

Table 11-3-5 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at reception.

Table 11-3-5 Setup for Synchronous Serial Interface Pin (3 channels type, at reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Internal clock	External clock
Pin	P03	P04	P05	
Function	Port	Serial data input	Serial clock I/O	Port
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)	SC1MD1(SC1SBTS)	
Style	-	-	Push pull / Nch open-drain	Push pull / Nch open-drain
			SC1MD1(SC1SBTM)	
I/O	-	Input mode	Output mode	Input mode
		P0DIR(P0DIR4)	P0DIR(P0DIR5)	
Pull-up	-	Added / Not added	Added / Not added	Added / Not added
		P0PLU(P0PLU4)	P0PLU(P0PLU5)	

■Pins Setup (3 channels type, at transmission / reception)

Table 11-3-6 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at transmission / reception.

Table 11-3-6 Setup for Synchronous Serial Interface Pin (3 channels type, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Internal clock	External clock
Pin	P03	P04	P05	
Function	Serial data output	"1" input	Serial clock I/O	Port
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)	SC1MD1(SC1SBTS)	
Style	Push pull / Nch open-drain	-	Push pull / Nch open-drain	Push pull / Nch open-drain
	SC1MD1(SC1SBOM)		SC1MD1(SC1SBTM)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR(P0DIR3)	P0DIR(P0DIR4)	P0DIR(P0DIR5)	
Pull-up	Added / Not added	Added / Not added	Added / Not added	Added / Not added
	P0PLU(P0PLU3)	P0PLU(P0PLU4)	P0PLU(P0PLU5)	

11-3-2 Setup Example

■Transmission / Reception Setup Example

The setup example for clock synchronous serial interface communication with serial interface 1 is shown. Table 11-3-7 shows the conditions at transmission / reception.

Table 11-3-7 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	set to	Setup item	set to
Transfer bit count	8 bits	Clock source	fs/2
Start condition	none	SBT1/SBO1 pin style	N-ch open-drain
First transfer bit	MSB	SBT1 pin pull-up resistor	Not added
Input data edge	falling edge	SBO1 pin pull-up resistor	Not added
		SBI1 pin pull-up resistor	Added
Output data edge	rising edge	Serial interface 1 interrupt	Enable
Clock	Internal clock (master communication)		

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the SC1MD0 register. Select the transfer bit count. SC1MD0 (x'3F57') bp2-0 : SC1LNG2-0 = 000	(1) Set the SC1LNG2-0 flag of the serial interface 1 mode register 0 (SC1MD0) to "000" to set the transfer bit count "8 bits".
Select the start condition. SC1MD0 (x'3F57') bp3 : SC1STE = 0	Set the SC1STE flag of the SC1MD0 register to "0" to disable start condition.
Select the first bit to be transferred. SC1MD0 (x'3F57') bp4 : SC1DIR = 0	Set the SC1DIR flag of the SC1MD0 register to "0" to set MSB as a first transfer bit.
Select the transfer edge. SC1MD0 (x'3F57') bp6 : SC1CE0 = 0 bp5 : SC1CE1 = 1	Set the SC1CE0, 1 flag of the SC1MD0 register to "0, 1" to set the transmission data output edge to "rising" and the received data input edge to "falling".

Setup Procedure	Description
(2) Select the clock source. SC1MD1 (x'3F58') bp1-0 : SC1CK1-0 = 00	(2) Set the SC1CK1-0 flag of the SC1MD1 register to "00" to select "fs/2" as a clock source.
(3) Select the transfer clock. SC1MD1 (x'3F58') bp2 : SC1SBTS = 1	(3) Set the SC1SBTS flag of the SC1MD1 register to "1" to set the SBT1 pin to serial interface clock I/O pin. The communication is with internal clock (master communication).
(4) Control the pin type. SC1MD1 (x'3F58') bp6-5 : SC1SBOM, SC1SBTM = 11 P0PLU (x'3F40') bp5-3 : P0PLU5-3 = 010	(4) Set the SC1SBOM, SC1SBTM flag of the SC1MD1 register to "11" to select "N-ch open drain" to the SBO1/SBT1 pin. Set the P0PLU5-3 flag of the P0PLU register to "010" to add pull-up resistor only to the SBI1 pin.
(5) Control the pin direction. P0DIR (x'3F30') bp5-3 : P0DIR5-3 = 101	(5) Set the P0DIR5-3 flag of the port 0 pin's direction control register (P0DIR) to "101" to set P03, P05 "output mode", and to set P04 "input mode".
(6) Control the pin function. SC1MD1 (x'3F58') bp4 : SC1SBOS = 1 bp3 : SC1SBIS = 1	(6) Set the SC1SBOS, SC1SBIS flag of the SC1MD1 register to "1" to set the SBO1 pin to "serial interface data output", the SBI1 pin to "serial interface data input".
(7) Set the interrupt level. SC1ICR (x'03FF1') bp7-6 : SC1LV1-0 = 10	(7) Set the interrupt level by the SC1LV1-0 flag of the serial interface 1 interrupt control register (SC1ICR).
(8) Enable the interrupt. SC1ICR (x'3FF1') bp1 : SC1IE = 1	(8) Set the SC1IE flag of the SC1ICR register to "1" to enable interrupts. If the interrupt request flag (SC1IR of the SC1ICR register) had already been set, clear SC1IR before an interrupt is enabled. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Start serial interface transmission. Transmission data→SC1TRB (x'3F55') Reception data→input to SBI1 pin.	(9) Set the transmission data to the serial interface 1 transmission / reception shift register (SC1TRB). Then, an internal clock is generated to start transmission / reception. After transmission has finished, serial interface 1 interrupt SC1IRQ is generated.

When only reception with 3 channels is operated, set SC1SBOS of the SC1MD1 register to "0" and select a port. The SBO1 pin can be used as a general port.

When the register except the SC1TRB is written or rewritten, set the SC1SBOS, SC1SBIS flag to "0".

When the internal clock is used as clock source, write dummy data to the SC1TRB register after setting the SC1SBIS flag and the SC1SBOS flag of the SC1MD1 register to "1". Even if the reception is operated again, write dummy data to the SC1TRB register.

Chapter 12 LCD Functions

12

12-1 Overview

This LSI contains an internal LCD driver circuit with 52 segment pins and 4 common pins. The LCD driver consists of a segment output latch, a prescaler, a timing control circuit, segment drivers, common drivers and a LCD voltage control circuit.

12-1-1 Functions

Functions of the LCD driver circuits are shown below.

Table 12-1-1 Functions of the LCD

	LCD
Duty	Static 1/2 Duty 1/3 Duty 1/4 Duty
Segment Output Pins	SEG0 to SEG51
Common Output Pins	COM0 to COM3
LCD Power Supply	V_{LC1} to V_{LC3}
Clock Source (LCDCLK)	$fosc/2^{11}$ $fosc/2^{12}$ $fosc/2^{13}$ $fosc/2^{14}$ $fosc/2^{15}$ $fosc/2^{16}$ $fosc/2^{17}$ $fosc/2^{18}$ $fx/2^{6}$ $fx/2^{7}$ $fx/2^{8}$ $fx/2^{9}$
fosc: Machine clock (High speed oscillation) fx: Machine clock (Low speed oscillation) LCDCLK: LCD clock source (which is selected in LCDCK0 to LCDCK3)	

12-1-2 LCD Operation at Standby Mode

At standby mode, LCD driver operation may be restricted.
Table 12-1-2 shows the relation of the standby mode and the LCD operation.

Table 12-1-2 LCD Operation at Standby Mode

CPU Mode		LCD Clock	
		fosc	fx
Operation Mode	NORMAL	O	O
	SLOW	×	O
Standby Mode	HALT0	Δ	Δ
	HALT1	×	Δ
	STOP	×	×

O : LCD Operation is enabled.
Δ : Keeping Display is enabled.
× : LCD Operation is disabled.

Before getting into the CPU mode which the LCD operation is disabled, switch the LCD off and switch the segment output to port.

12-1-3 Maximum Number of Pixels

Table 12-1-3 shows the maximum number of pixels that can be displayed.

Table 12-1-3 Maximum Number of Pixels that can be Displayed

Duty	Maximum Number of Pixels (Segment × Common)	8-segment LCD Panel	Common Pins	Segment Output Latch Bits
Static	52(52 × 1)	6 rows	COM0	bit0, bit4
1/2	104(52 × 2)	13 rows	COM0 to COM1	bit0 to bit1, bit4 to bit5
1/3	156(52 × 3)	17 rows	COM0 to COM2	bit0 to bit2, bit4 to bit6
1/4	208(52 × 4)	26 rows	COM0 to COM3	bit0 to bit3, bit4 to bit7

12-1-4 LCD Driver Circuit Block Diagram

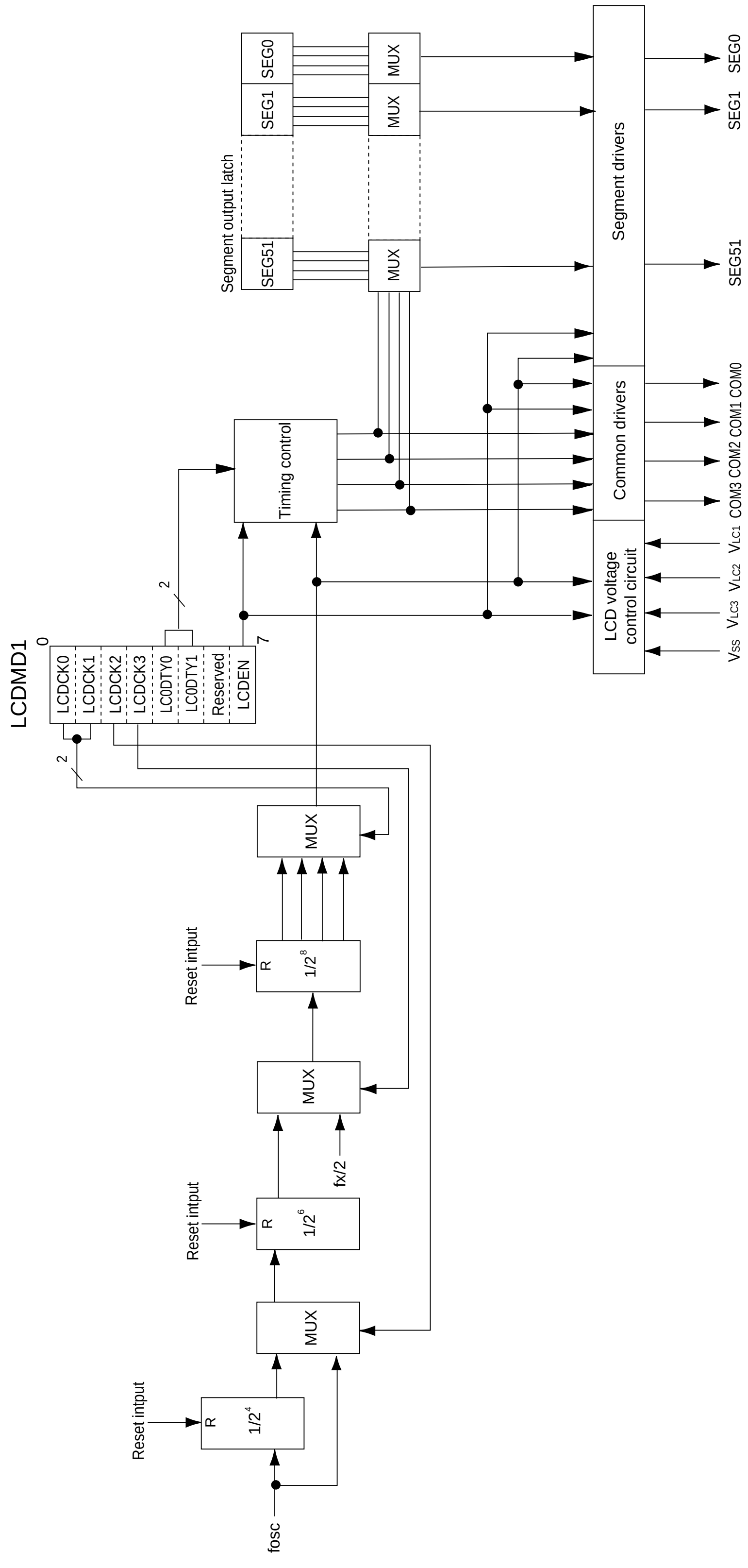


Figure 12-1-1 LCD Driver Circuit Block Diagram

12-2 LCD Control Registers

The LCD is controlled by LCD mode control register (LCMD) and segment output control register (LCCTR). The LCD display data is stored in the segment output latch.

12-2-1 LCD Control Registers List

LCD control registers are listed below.

Tabel 12-2-1 LCD Control Registers List

Register abbreviation	Address	R/W	Register Name	Page
LCMD	x'03FCD'	R/W	LCD mode control register	XII - 6
LCCTR	x'03FCC'	R/W	Segment output control register	XII - 8

R/W: Readable/Writable

* Segment output latch is located at addresses x’03FB0’ to x’03FC9’ : SEG0 to SEG51.

[☞ Chapter 12 12-2-4 Segment Output Latch]

12-2-2 LCD Mode Control Register (LCMD)

The LCD mode control register (LCMD) is readable/writable register that specifies LCD display ON/OFF, the display duty and the LCD clock (LCDCLK).

■LCD Mode Control Register (LCMD)

	7	6	5	4	3	2	1	0	
LCMD	LCDEN	Reserved	LC0DTY1	LC0DTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0	(at reset: 00000000)

LCDCK3	LCDCK2	LCDCK1	LCDCK0	LCD clock source selection
0	0	0	0	fosc/2^{11}
			1	fosc/2^{12}
		1	0	fosc/2^{13}
			1	fosc/2^{14}
	1	0	0	fosc/2^{15}
			1	fosc/2^{16}
		1	0	fosc/2^{17}
			1	fosc/2^{18}
1	X	0	0	fx/2^{6}
			1	fx/2^{7}
		1	0	fx/2^{8}
			1	fx/2^{9}

LC0DTY1	LC0DTY0	LCD display duty selection
0	0	1/4 duty
	1	1/3 duty
1	0	1/2 duty
	1	Static

Reserved	Always set to "0".

LCDEN	Enable / disable LCD driver circuit
0	Stop (turn off LCD)
1	Start (illuminate LCD)

Figure 12-2-1 LCD Mode Control Register (LCMD: x’3FCD’, R/W)

■Setup of the LCD frame cycle

The LCD clock is supplied by the fosc or fx clock, divided by the prescaler. Bits 0 to 3 of the LCMD register sets the LCD clock, and LC0DTY0 to 1 sets the LCD frame cycle. Representative input frequencies corresponding to the LCD clock and the LCD frame cycle are shown below.

Table 12-3-4 Input Frequency and the LCD Clock

		Input Frequency									
Input Clock	Duty	20 MHz		16 MHz		8 MHz		4 MHz		32.768 kHz	
LCDCK3 to 0	LCDTY1 to 0	LCD Clock	Frame	LCD Clock	Frame	LCD Clock	Frame	LCD Clock	Frame	LCD Clock	Frame
0000 (OSC1/2^{11})	00 (1/4 duty)	9766 Hz	2441 Hz	7813 Hz	1953 Hz	3906 Hz	977 Hz	1953 Hz	488 Hz		
	01 (1/3 duty)		3255 Hz		2604 Hz		1302 Hz		651 Hz		
	10 (1/2 duty)		4883 Hz		3906 Hz		1953 Hz		977 Hz		
	11 (static)		9766 Hz		7813 Hz		3906 Hz		1953 Hz		
0001 (OSC1/2^{12})	00 (1/4 duty)	4883 Hz	1221 Hz	3906 Hz	977 Hz	1953 Hz	488 Hz	977 Hz	244 Hz		
	01 (1/3 duty)		1628 Hz		1302 Hz		651 Hz		326 Hz		
	10 (1/2 duty)		2441 Hz		1953 Hz		977 Hz		488 Hz		
	11 (static)		4883 Hz		3906 Hz		1953 Hz		977 Hz		
0010 (OSC1/2^{13})	00 (1/4 duty)	2441 Hz	610 Hz	1953 Hz	488 Hz	977 Hz	244 Hz	488 Hz	122 Hz		
	01 (1/3 duty)		814 Hz		651 Hz		326 Hz		163 Hz		
	10 (1/2 duty)		1221 Hz		977 Hz		488 Hz		244 Hz		
	11 (static)		2441 Hz		1953 Hz		977 Hz		488 Hz		
0011 (OSC1/2^{14})	00 (1/4 duty)	1221 Hz	305 Hz	977 Hz	244 Hz	488 Hz	122 Hz	244 Hz	61 Hz		
	01 (1/3 duty)		407 Hz		326 Hz		163 Hz		81 Hz		
	10 (1/2 duty)		610 Hz		488 Hz		244 Hz		122 Hz		
	11 (static)		1221 Hz		977 Hz		488 Hz		244 Hz		
0100 (OSC1/2^{15})	00 (1/4 duty)	610 Hz	153 Hz	488 Hz	122 Hz	244 Hz	61 Hz	122 Hz	31 Hz		
	01 (1/3 duty)		203 Hz		163 Hz		81 Hz		41 Hz		
	10 (1/2 duty)		305 Hz		244 Hz		122 Hz		61 Hz		
	11 (static)		610 Hz		488 Hz		244 Hz		122 Hz		
0101 (OSC1/2^{16})	00 (1/4 duty)	305 Hz	76 Hz	244 Hz	61 Hz	122 Hz	31 Hz	61 Hz	15 Hz		
	01 (1/3 duty)		102 Hz		81 Hz		41 Hz		20 Hz		
	10 (1/2 duty)		153 Hz		122 Hz		61 Hz		31 Hz		
	11 (static)		305 Hz		244 Hz		122 Hz		61 Hz		
0110 (OSC1/2^{17})	00 (1/4 duty)	153 Hz	38 Hz	122 Hz	31 Hz	61 Hz	15 Hz	31 Hz	8 Hz		
	01 (1/3 duty)		51 Hz		41 Hz		20 Hz		10 Hz		
	10 (1/2 duty)		76 Hz		61 Hz		31 Hz		15 Hz		
	11 (static)		153 Hz		122Hz		61 Hz		31 Hz		
0111 (OSC1/2^{18})	00 (1/4 duty)	76 Hz	19 Hz	61 Hz	15 Hz	31 Hz	8 Hz	15 Hz	4 Hz		
	01 (1/3 duty)		25 Hz		20 Hz		10 Hz		5 Hz		
	10 (1/2 duty)		38 Hz		31 Hz		15 Hz		8 Hz		
	11 (static)		76 Hz		61 Hz		31 Hz		15 Hz		
1x00 (XI/2^6)	00 (1/4 duty)									512 Hz	128 Hz
	01 (1/3 duty)										171 Hz
	10 (1/2 duty)										256 Hz
	11 (static)										512 Hz
1x01 (XI/2^7)	00 (1/4 duty)									256 Hz	64 Hz
	01 (1/3 duty)										85 Hz
	10 (1/2 duty)										128 Hz
	11 (static)										256 Hz
1x10 (XI/2^8)	00 (1/4 duty)									128 Hz	32 Hz
	01 (1/3 duty)										43 Hz
	10 (1/2 duty)										64 Hz
	11 (static)										128 Hz
1x11 (XI/2^9)	00 (1/4 duty)									64 Hz	16 Hz
	01 (1/3 duty)										21 Hz
	10 (1/2 duty)										32 Hz
	11 (static)										64 Hz

12-2-3 Segment Output Control Register (LCCTR)

The segment output control register (LCCTR) is readable/writable register that controls the selection between port output (P5,P6,P7,P8) and segment output (SEG26 to SEG51). At reset, LCCTR is set to the input port values.
If SEGSEL0 to SEGSEL7 of LCCTR is set “1”, appropriate pins are all invalid. At this time, the data of the appropriate port is read, it returns “0”.
Because SEG0 to SEG25 is segment output only, it does not need output control.

■Segment Output Control Register (LCCTR)

	7	6	5	4	3	2	1	0	
LCCTR	-	SEGSEL6	SEGSEL5	SEGSEL4	SEGSEL3	SEGSEL2	SEGSEL1	SEGSEL0	(at reset: 00000000)

SEGSEL0	SEG51 to 50 / Port 53 to 54 select
0	Port 53 to 54
1	SEG51 to 50

SEGSEL1	SEG49 to 46 / Port 60 to 63 select
0	Port 60 to 63
1	SEG49 to 46

SEGSEL2	SEG45 to 42 / Port 64 to 67 select
0	Port 64 to 67
1	SEG45 to 42

SEGSEL3	SEG41 to 38 / Port 70 to 73 select
0	Port 70 to 73
1	SEG41 to 38

SEGSEL4	SEG37 to 34 / Port 74 to 77 select
0	Port 74 to 77
1	SEG37 to 34

SEGSEL5	SEG30 to 33 / Port 84 to 87 select
0	Port 84 to 87
1	SEG30 to 33

SEGSEL6	SEG26 to 29 / Port 80 to 83 select
0	Port 80 to 83
1	SEG26 to 29

Figure 12-2-2 LCD Output Control Register (LCCTR: x’3FCC’, R/W)

12-2-4 Segment Output Latch

The segment output latch stores the LCD display data. A 4-bit latch is assigned to every single segment. Bit0 and bit4 are read in synchronization with the timing of COM0, bit1 and bit5 with COM1, bit2 and bit6 with COM2, and bit3 and bit7 with COM3. If the content is “1”, the segment pin outputs the “selective voltage”. If “0”, “non-selective voltage” is output.

Addresses are assigned within the range of x’3FB0' to x’3FC9'. Data read and write operations can be performed in the same way as for RAM access. At reset, the value of the segment output latch is undefined. The correspondence between the segment output latch and the segment/common pins is shown in Figure 12-2-3.

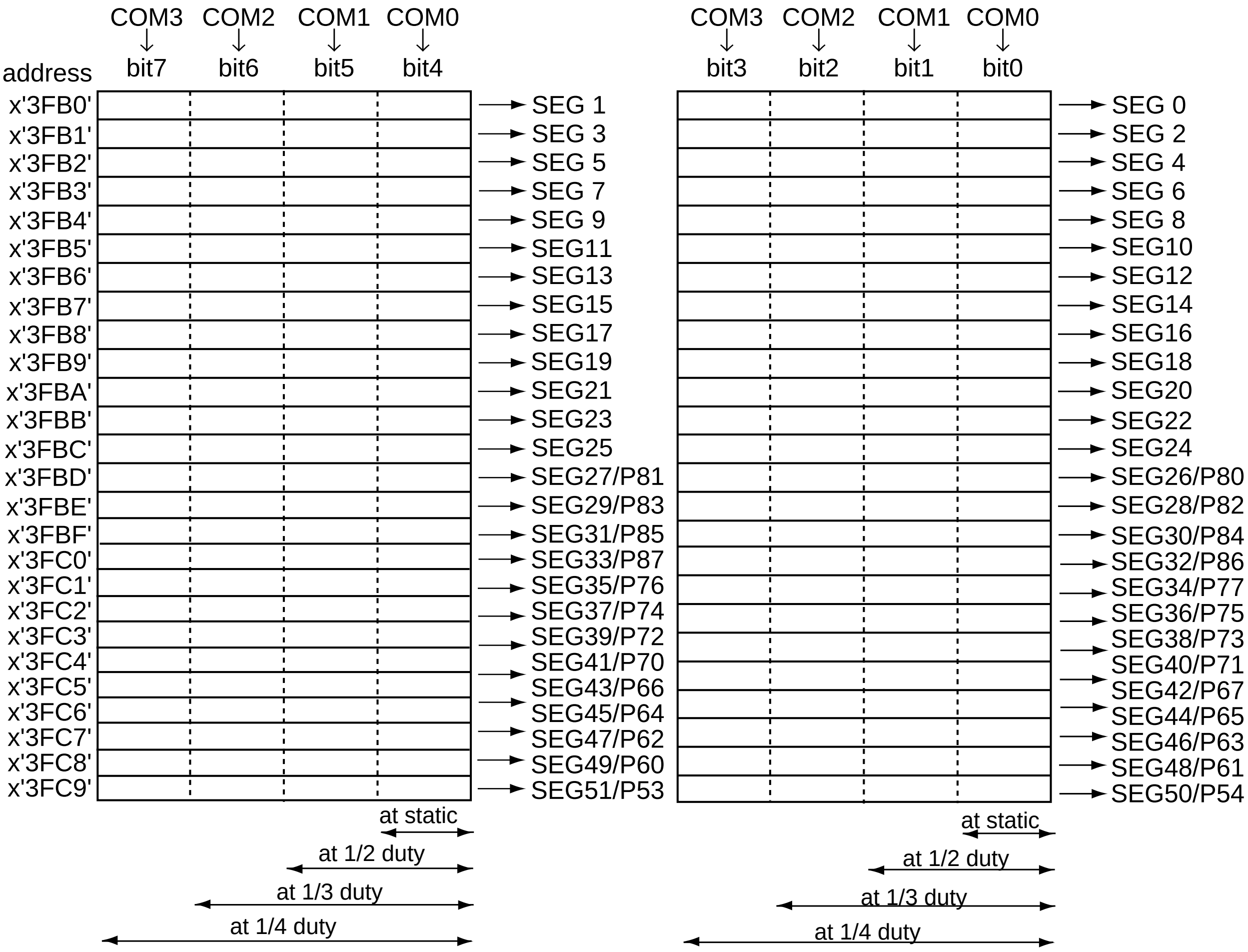


Figure 12-2-3 Correspondance between the Segment Output Latch and the Segment/Common Pins

> When a duty ratio other than 1/4 is used, the LCD display will be affected if a “1” is written to bits not used for the segment output latch. Therefore, write “0” to bits 7 and 3 when using a 1/3 duty ratio, to bits 7, 6, 3 and 2 when using a 1/2 duty ratio, and to bits 7, 6, 5, 3, 2 and 1 when the display mode is static.

12-2-5 Operation

The LCD driver is capable of static display and dynamic display (1/2 duty 1/2 bias, 1/3 duty 1/3bias, 1/4 duty 1/3 bias) through the segment output pins (SEG0 to SEG24) and the common output pins (COM0 to COM3).

■The LCD driver circuit operation
The LCD driver circuit generates the timing siginals, which are necessary for controling 1/2 duty, 1/3 duty, 1/4 duty and static, at the timing control circuit, based on the LCD clock divided by the prescaler, and supplies them to the common driver and the multiplexer.

The common driver outputs the common signals which are necessary for the LCD display, based on the voltage from the LCD power supply. At reset, or when the LCD is OFF, V_{DD} is output. When the LCD is OFF, V_{DD} is output and the potential difference between the LCD electrodes becomes 0 V.

The multiplexer selects the segment output latched data in response to the signal from the timing control circuit and supplies it to the segment driver. The segment driver converts the content of the segment output latch into the signals, which is capable of driving the LCD, based on the voltage supplied to LCD power supply, then outputs the segment signal.
When the LCD is OFF V_{SS} is output and the potential difference between the LCD electrodes becomes 0 V.

> ! When the LCD is OFF, V_{DD} is output and the potential difference between the LCD electrodes becomes 0 V.
> At reset, because the segments are also used as PORT pins, they are set PORT input pins and become Hi-z. Therefore there could be some adverse effects such as blinks of the LCD display. After reset, set the segment output control register (LCCTR) again.

> ! If the clock stops while LCD is displayed, the LCD may be crushed by the pressure of DC voltage to LCD electrodes.

12-3 LCD Voltage Control Circuit

Supply the voltage listed in Table 12-3-1 to the LCD power supply pins, so that the LCD driver voltage will be supllied to the segment and common signals. Examples of LCD power supply connections are shown in Figure 12-3-1.

Table 12-3-1 LCD Power Supply

Bias Method / LCD Power Supply	Static	1/2	1/3
V_{LC1}	V_{DD}	V_{DD} - 1/2 V_{LCD}	V_{DD} - 1/3 V_{LCD}
V_{LC2}	V_{DD} - V_{LCD}		V_{DD} - 2/3 V_{LCD}
V_{LC3}		V_{DD} - V_{LCD}	V_{DD} - V_{LCD}

V_{LCD}: LCD panel driver voltage (the maximum supply voltage to the LCD panel)

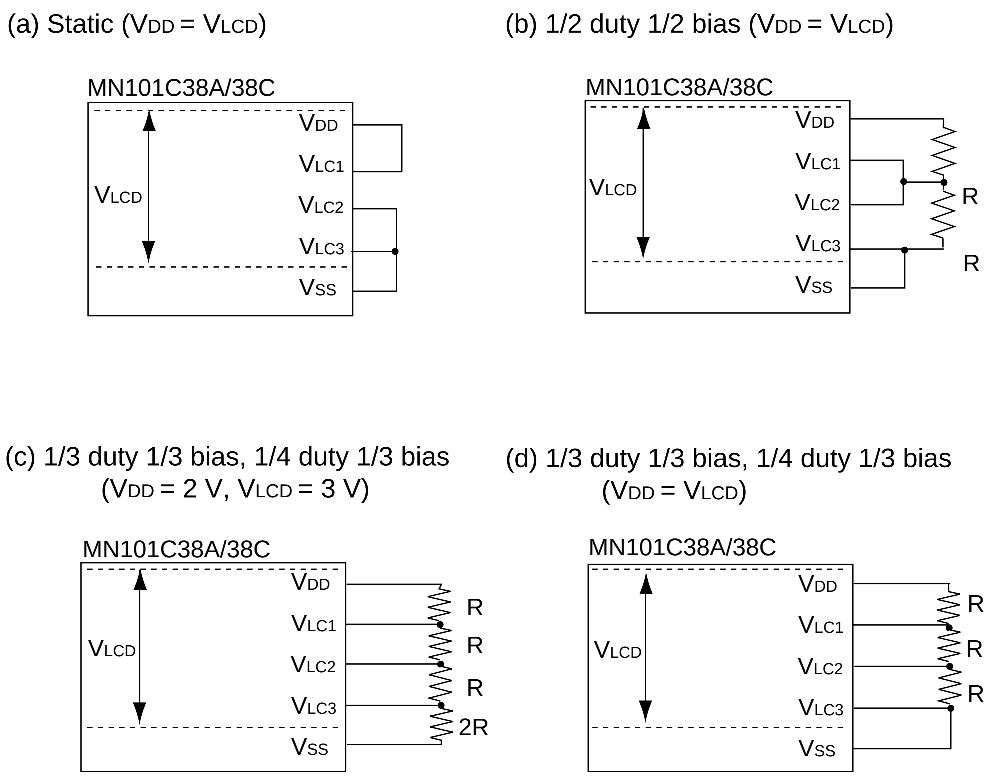


Figure 12-3-1 Examples of the LCD Power Supply Connection

1. In Figure 12-3-1, current always flows through the voltage divider resistors.
   The following connection can be used to cut off the current flow through these dividing resistors.

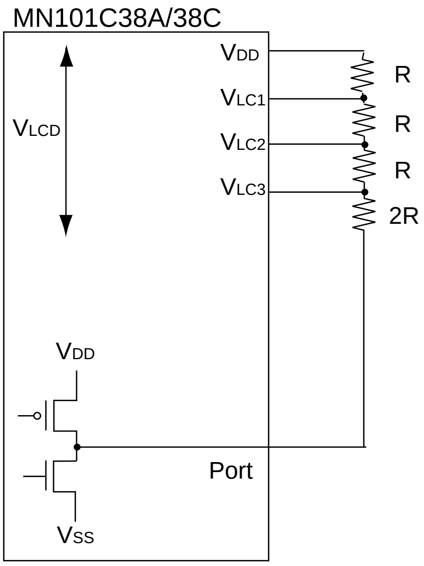


Figure 12-3-2 Voltage Dividing Resistors with Current Cutoff

2. The LCD power supply $V_{LC1\ to\ 3}$ is applied as shown below. The specific V_{LCD} value varies depending on the type of LCD used. Refer to the LCD specifications to determine the correct value.

   $V_{LC1} = V_{DD} - 1/3\ V_{LCD}$

   $V_{LC2} = V_{DD} - 2/3\ V_{LCD}$

   $V_{LC3} = V_{DD} - V_{LCD}$

   V_{DD} are normally divided by resistors and supplied to the LCD. Commonly used resistor values range between several tens to several hundreds kΩ. When $V_{LCD} = V_{DD}$, R' is no need. In Figure 12-3-3, C is a bias capacitor in the range of 0.01 µF to 0.1 µF, which is used to reduce the impedance of the power supply.

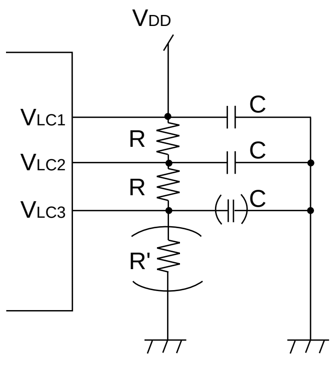


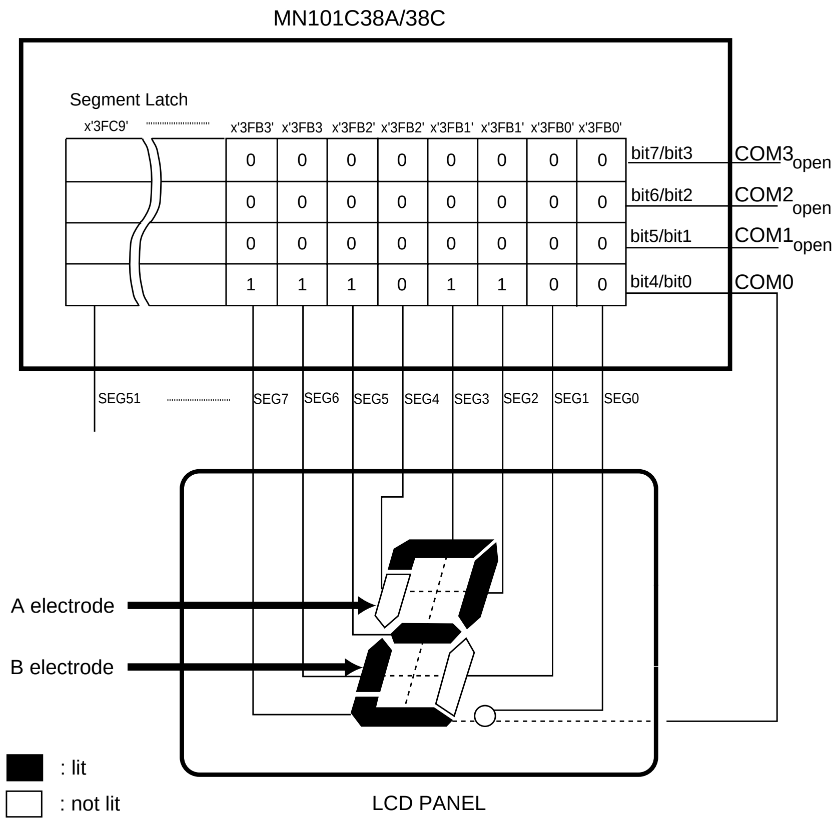
Figure 12-3-3 Supply to V_{LC1} to V_{LC3}

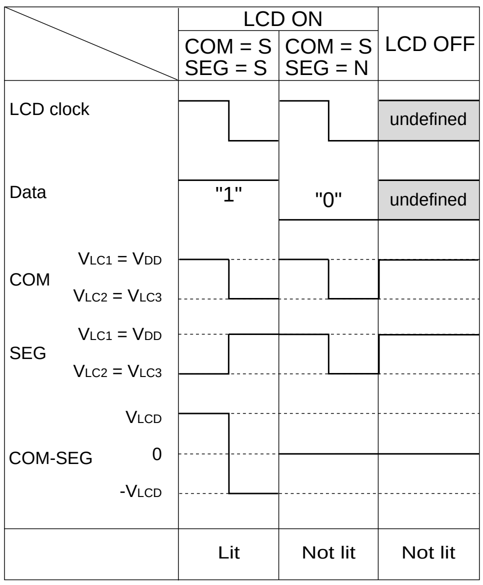
12-4 LCD Function Operation

Examples of the LCD panels' connections, displays and driving waveforms for static, 1/2 duty, 1/3 duty and 1/4 duty at each operation are shown below.

12-4-1 LCD Display Examples (Static)

■Static





S: selective voltage N: non-selective voltage VLCD: LCD driver voltage

In case of static, COM(COM0) always outputs selective voltage.

■**Static Driving Waveform**

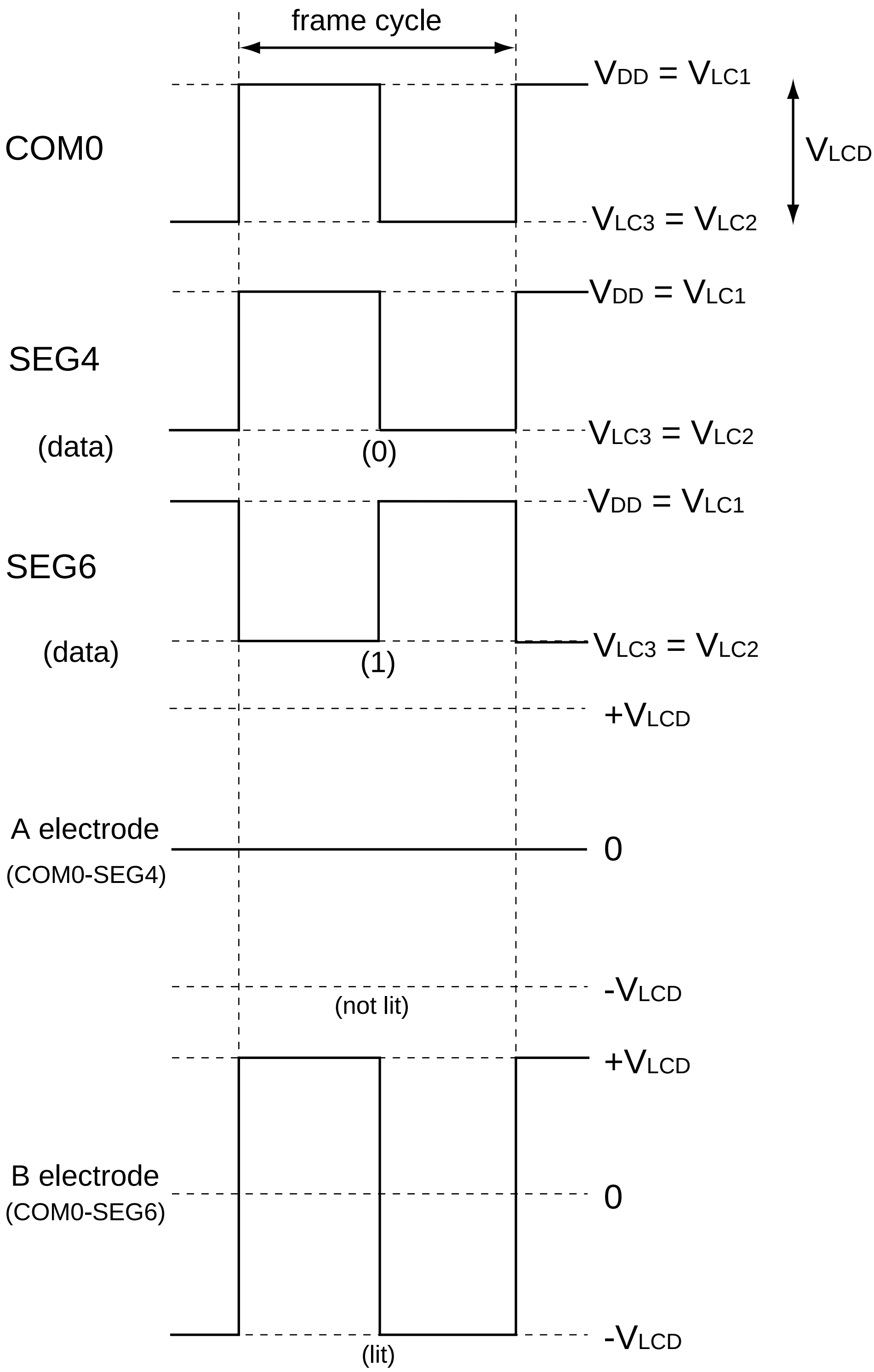


Figure 12-4-1 LCD Display Example of Static

12-4-2 Setup Example (Static)

■Setup Example of the LCD Function Operation (Static)

Segment signal (SEG0 to SEG7) and common signal (COM0) make the 8-segment LCD panel display "2". [☞ Chapter 12 12-4-1. LCD Display Examples (Static)]

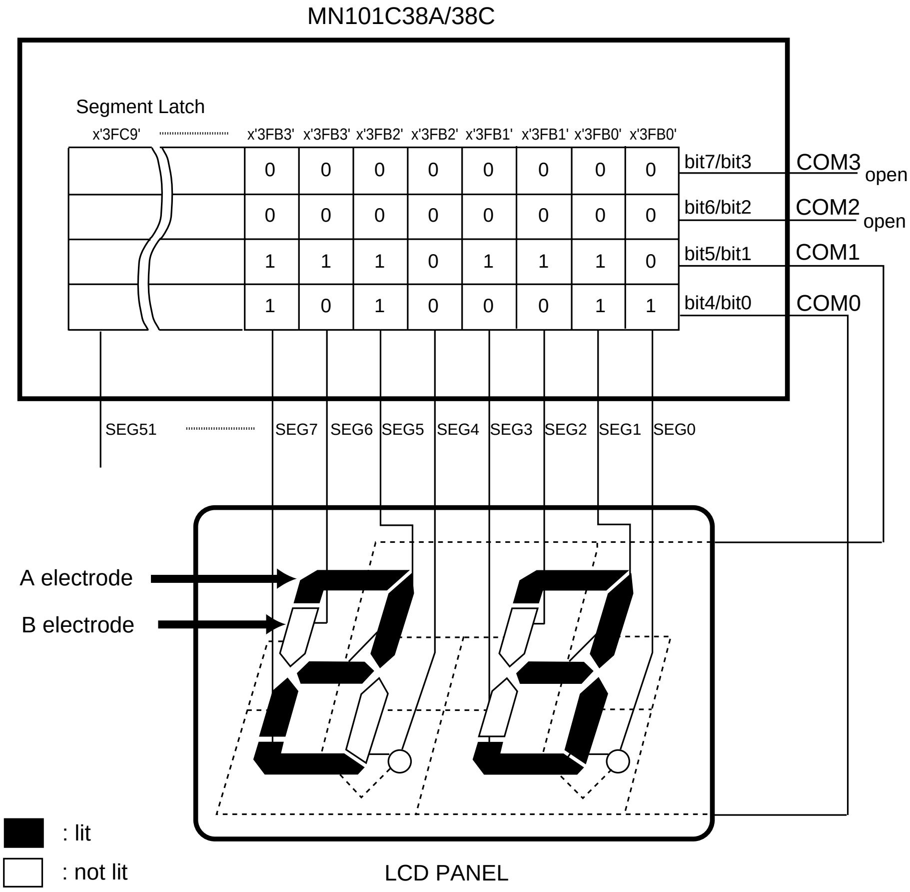
It is used 4 MHz as the high oscillation clock (fosc), 122Hz as fosc/2^{15} for LCD clock, and 122 Hz as frame frequency.

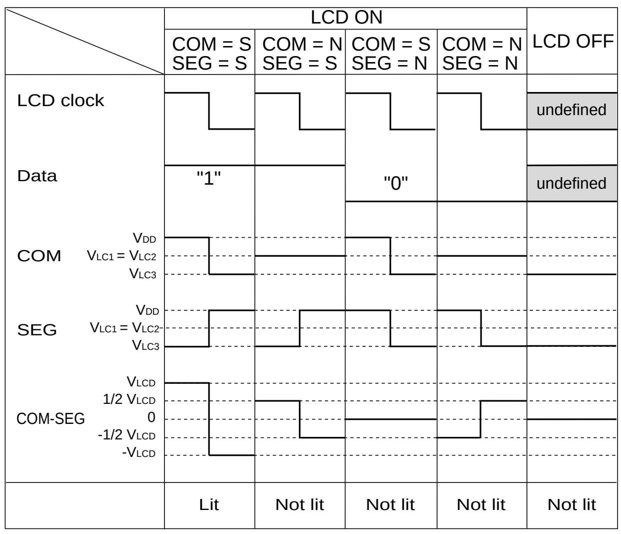
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the LCD operation LCMD(x'3FCD') bp7 : LCDEN = 0	(1) Set the LCDEN flag of the LCD mode control register (LCMD) to "0" to stop the LCD operation.
(2) Setup of the LCD display duty LCMD (x'3FCD') bp5-4 : LCDDTY1-0 = 11	(2) Set LC1SEL flags of the LCD mode control register (LCMD) to "0" to switch into the static driver mode.
(3) Setup of the LCD clock LCMD (x'3FCD') bp3-0 : LCDCK3-0 = 0100	(3) Set fosc/2^{15} as the LCD clock source by LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Setup of the display data Segment output latch SEG1-0 (x'3FB0') = x'00' Segment output latch SEG3-2 (x'3FB1') = x'11' Segment output latch SEG5-4 (x'3FB2') = x'10' Segment output latch SEG7-6 (x'3FB3') = x'11'	(4) Set display data "2" by the segment output latch SEG0 to 7 (x'3FB0' to x'3FB3'). [☞ Chapter 12 12-4-1. LCD Display Examples (Static)]
(5) Start the LCD operation LCMD (x'3FCD') bp7 : LCDEN = 1	(5) Set the LCDEN flag of the LCD mode control register (LCMD) to "1" to start the LCD operation.

12-4-3 LCD Display Examples (1/2 Duty)

■1/2 Duty





S: selective voltage N: non-selective voltage VLCD: LCD driver voltage

■1/2 Duty Driving Waveform

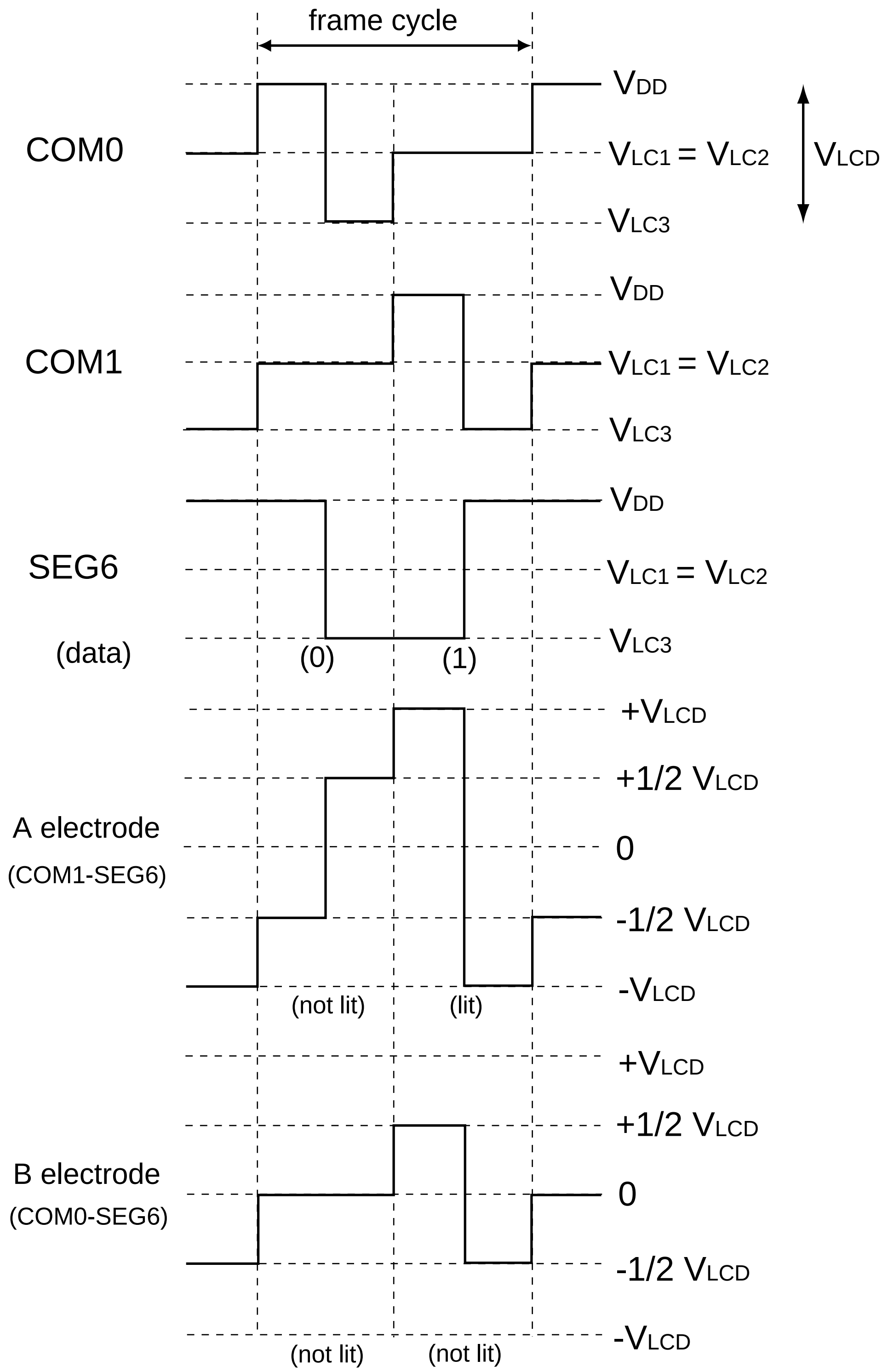


Figure 12-4-2 LCD Display Example of 1/2 Duty

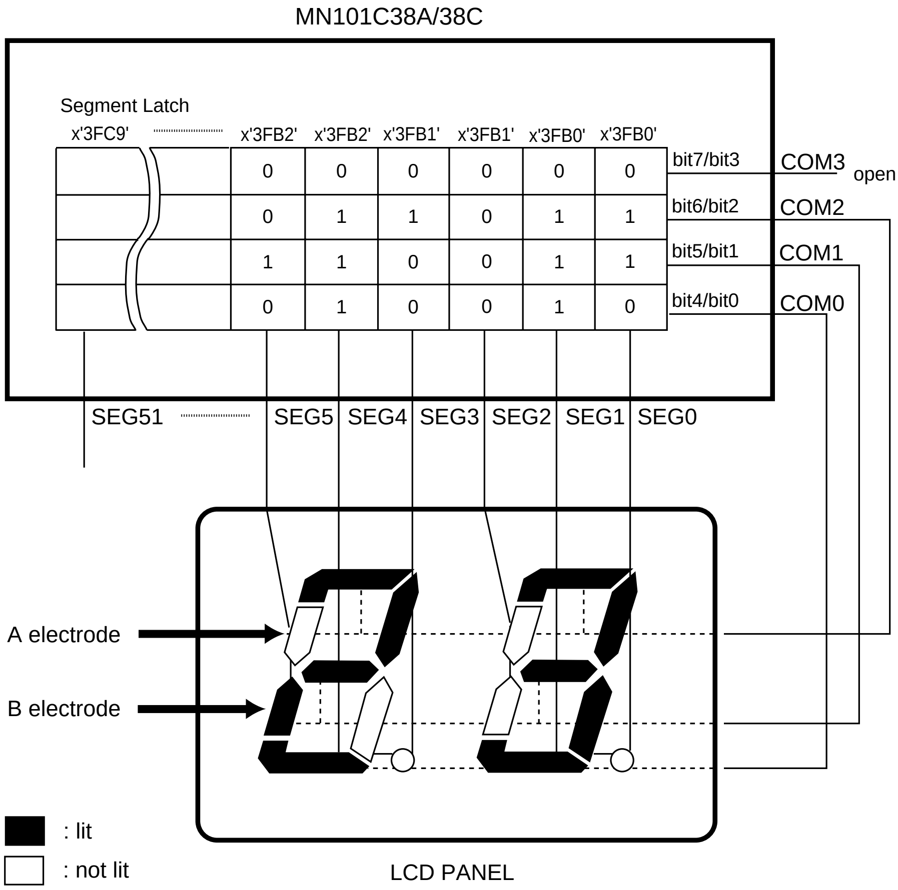
12-4-4 Setup Example (1/2 Duty)

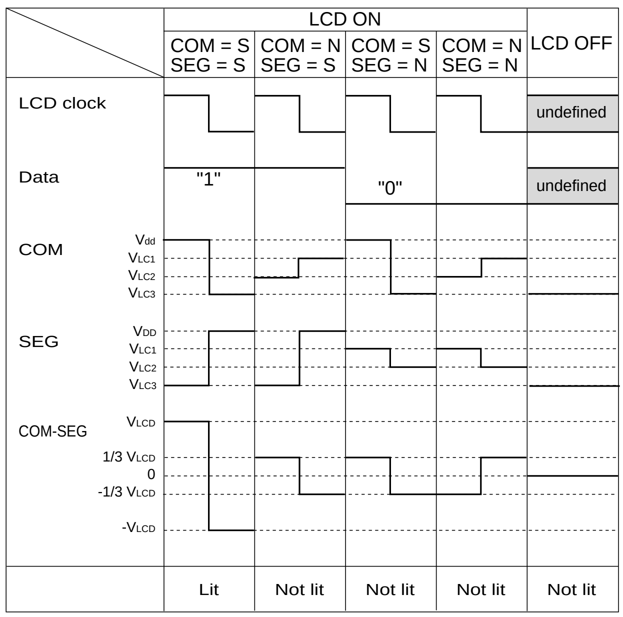
■Setup Example of the LCD Function Operation (1/2 Duty)
Segment signal (SEG0 to SEG7) and common signal (COM0 to COM1) at the display mode of 1/2 duty 1/2 bias make the double-digit 8-segment LCD panel display “23”. [☞ Chapter 12 12-4-3. LCD Display Examples (1/2 Duty)]
It is used 4 MHz as the high oscillation clock (fosc), 122Hz as fosc/2^{15} for LCD clock, and 61 Hz as frame frequency.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the LCD operation LCMD(x’3FCD’) bp7 : LCDEN = 0	(1) Set the LCDEN flag of the LCD mode control register (LCMD) to “0” to stop the LCD operation.
(2) Setup of the LCD display duty LCMD (x’3FCD’) bp5-4 : LCDDTY1-0 = 10	(2) Set 1/2 as the display duty by LC0DTY1-0 flags of the LCD mode control register (LCMD).
(3) Setup of the LCD clock LCMD (x’3FCD’) bp3-0 : LCDCK3-0 = 0100	(3) Set fosc/2^{15} as the LCD clock source by LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Setup of the display data Segment output latch SEG1-0 (x’3FB0’) = x’31’ Segment output latch SEG3-2 (x’3FB1’) = x’22’ Segment output latch SEG5-4 (x’3FB2’) = x’30’ Segment output latch SEG7-6 (x’3FB3’) = x’32’	(4) Set “23” as the display data by the segment output latch SEG0 to 7 (x’3FB0’ to x’3FB3’). [☞ Chapter 12 12-4-3. LCD Display Examples (1/2 Duty)]
(5) Start the LCD operation LCMD (x’3FCD’) bp7 : LCDEN = 1	(5) Set the LCDEN flag of the LCD mode control register (LCMD) to “1” to start the LCD operation.

12-4-5 LCD Display Examples (1/3 Duty)

■1/3 Duty





S: selective voltage N: non-selective voltage VLCD: LCD driver voltage

■1/3 Duty Driving Waveform

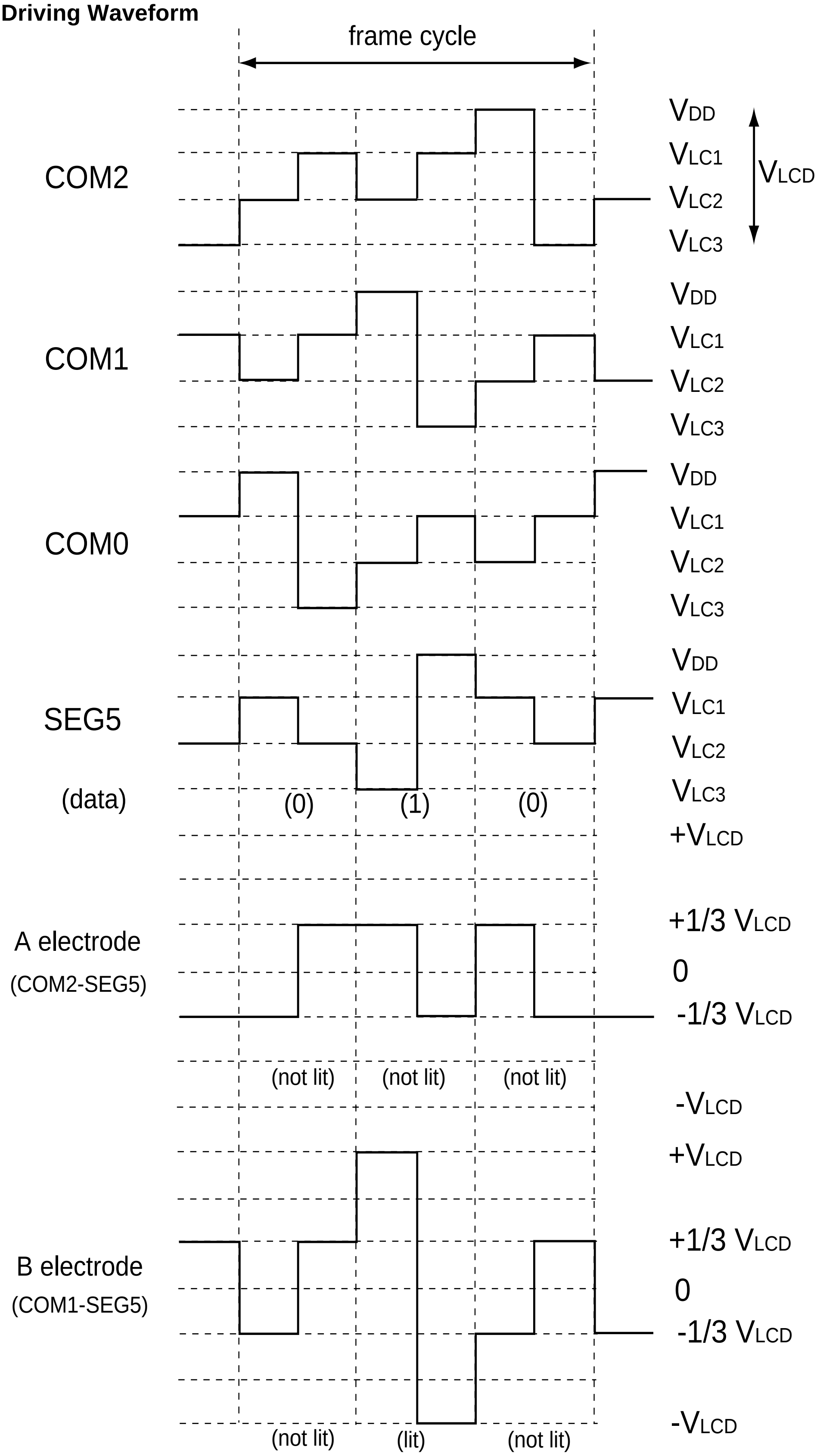


Figure 12-4-3 LCD Display Example of 1/3 Duty

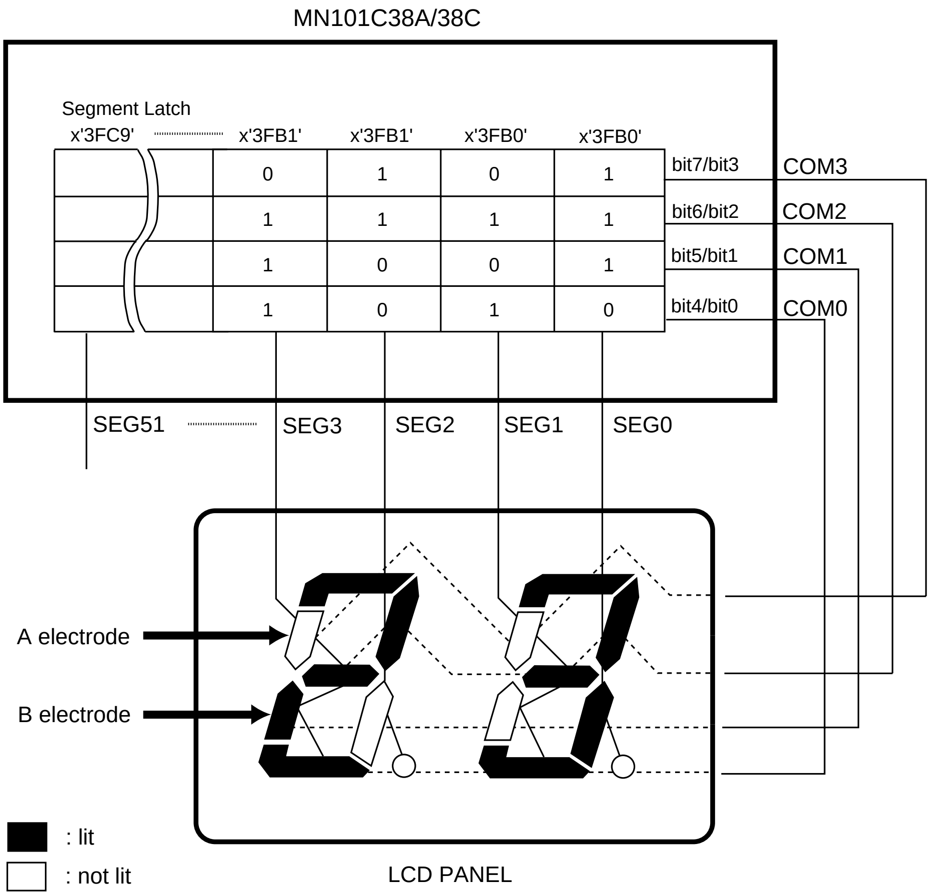
12-4-6 Setup Example (1/3 Duty)

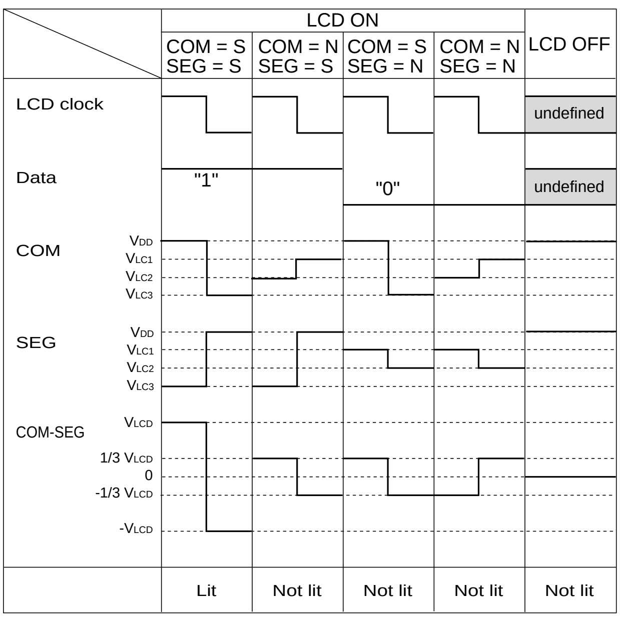
■Setup Example of the LCD Function Operation (1/3 Duty)
Segment signal (SEG0 to SEG5) and common signal (COM0 to COM2) at the display mode of 1/3 duty 1/3 bias make the double-digit 8-segment LCD panel display “23”. [☞ Chapter 12 12-4-5. LCD Display Examples (1/3 Duty)]
It is used 4 MHz as the high oscillation clock (fosc), 122Hz as fosc/2^{15} for LCD clock, and 41 Hz as frame frequency.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the LCD operation LCMD(x’3FCD’) bp7 : LCDEN = 0	(1) Set the LCDEN flag of the LCD mode control register (LCMD) to “0” to stop the LCD operation.
(2) Setup of the LCD display duty LCMD (x’3FCD’) bp5-4 : LCDDTY1-0 = 01	(2) Set 1/3 as the display duty by LC0DTY1-0 flags of the LCD mode control register (LCMD).
(3) Setup of the LCD clock LCMD (x’3FCD’) bp3-0 : LCDCK3-0 = 0100	(3) Set fosc/2^{15} as the LCD clock source by LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Setup of the display data Segment output latch SEG1-0 (x’3FB0’) = x’76’ Segment output latch SEG3-2 (x’3FB1’) = x’40’ Segment output latch SEG5-4 (x’3FB2’) = x’27’	(4) Set “23” as the display data by the segment output latch SEG0 to 5 (x’3FB0’ to x’3FB2’). [☞ Chapter 12 12-4-5. LCD Display Examples (1/3 Duty)]
(5) Start the LCD operation LCMD (x’3FCD’) bp7 : LCDEN = 1	(5) Set the LCDEN flag of the LCD mode control register (LCMD) to “1” to start the LCD operation.

12-4-7 LCD Display Examples (1/4Duty)

■1/4 Duty





S: selective voltage N: non-selective voltage V_{LCD}: LCD driver voltage

■1/4 Duty Driving Waveform

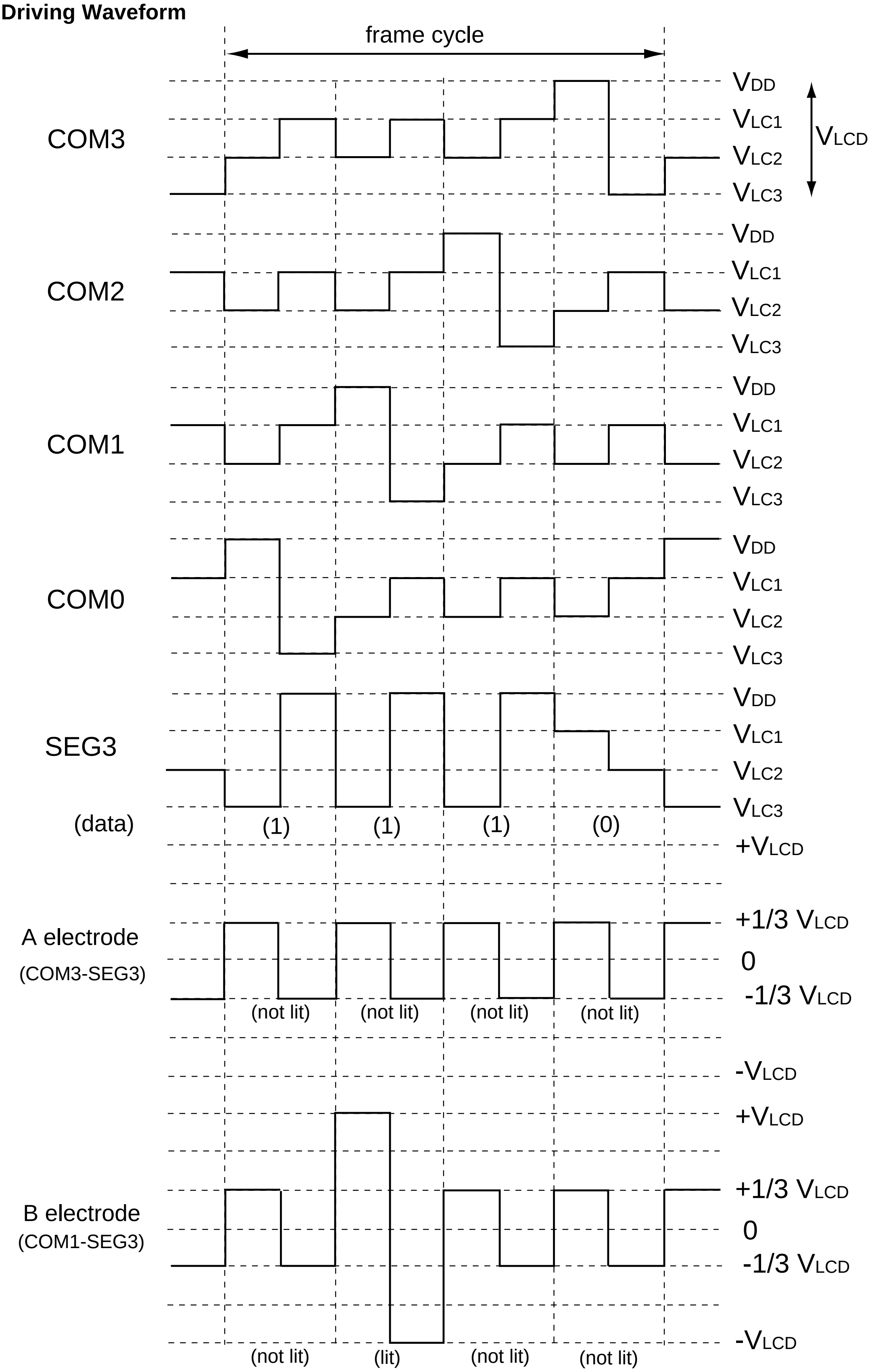


Figure 12-4-4 LCD Display Example of 1/4 Duty

12-4-8 Setup Example (1/4 Duty)

■Setup Example of the LCD Function Operation (1/4 Duty)

Segment signal (SEG0 to SEG29) and common signal (COM0 to COM3) at the display mode of 1/4 duty 1/3 bias make the fifteen-digit 8-segment LCD panel display “323232323232323”. [☞ Chapter 12 12-4-7. LCD Display Examples (1/4 Duty)]

It is used 4 MHz as the high oscillation clock (fosc), 122Hz as fosc/2^{15} for LCD clock, and 31 Hz as frame frequency.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the LCD operation LCMD(x’3FCD’) bp7 : LCDEN = 0	(1) Set the LCDEN flag of the LCD mode control register (LCMD) to “0” to stop the LCD operation.
(2) Setup of the segment output segment/port pins LCCTR (x’3FCC’) bp6-0 : SEGSEL6-0 = x’40’	(2) Select SEG29-26 by SEGSEL6 to 0 flags of the output control register (LCCTR).
(3) Setup of the LCD display duty LCMD (x’3FCD’) bp5-4 : LCDDTY1-0 = 00	(3) Set 1/4 as the display duty by LC0DTY1-0 flags of the LCD mode control register (LCMD).
(4) Setup of the LCD clock LCMD (x’3FCD’) bp3-0 : LCDCK3-0 = 0100	(4) Set fosc/2^{15} as the LCD clock source by LCDCK3-0 flags of the LCD mode control register (LCMD).
(5) Setup of the display data Segment output latch SEG1-0 (x’3FB0’) = x’5E’ Segment output latch SEG3-2 (x’3FB1’) = x’7C’ Segment output latch SEG5-4 (x’3FB2’) = x’5E’ Segment output latch SEG7-6 (x’3FB3’) = x’7C’ Segment output latch SEG9-8 (x’3FB4’) = x’5E’ Segment output latch SEG11-10 (x’3FB5’) = x’7C’ Segment output latch SEG13-12 (x’3FB6’) = x’5E’	(5) Set “323232323232323” as the display data by the segment output latch SEG0-29 (x’3FB0’ to x’3FBE’). [☞ Chapter 12 12-4-7. LCD Display Examples (1/4 Duty)]

Setup Procedure	Description
Segment output latch SEG15-14 (x'3FB7') = x'7C' Segment output latch SEG17-16 (x'3FB8') = x'5E' Segment output latch SEG19-18 (x'3FB9') = x'7C' Segment output latch SEG21-20 (x'3FBA') = x'5E' Segment output latch SEG23-22 (x'3FBB') = x'7C' Segment output latch SEG25-24 (x'3FBC') = x'5E' Segment output latch SEG27-26 (x'3FBD') = x'7C' Segment output latch SEG29-28 (x'3FBE') = x'5E'	
(5) Start the LCD operation LCMD (x'3FCD') bp7 : LCDEN = 1	(5) Set the LCDEN flag of the LCD mode control register (LCMD) to "1" to start the LCD operation.

Chapter 13 A/D Conversion Functions

13-1 Overview

This LSI has an A/D converter with 10 bits resolution. That has a built-in sample hold circuit, and the analog input can be switched channel 0 to 7 (AN0 to AN7). As A/D converter is stopped, the power consumption can be reduced by a built-in ladder resistance.

13-1-1 Functions

Table 13-1-1 shows the A/D converter functions.

Table 13-1-1   A/D Converter Functions

A/D input pins	8 pins
Pins	AN7 to AN0
Interrupt	ADIRQ
Resolution	10 bits
Conversion time (min.)	9.6 µs (as T_{AD} =800 ns)
Input range	V_{REF-} to V_{REF+}
Power consumption	Built-in ladder resistance (ON/OFF)

Keep reference voltage between V_{REF+} and V_{REF-} above 2 V.

13-1-2 Block Diagram

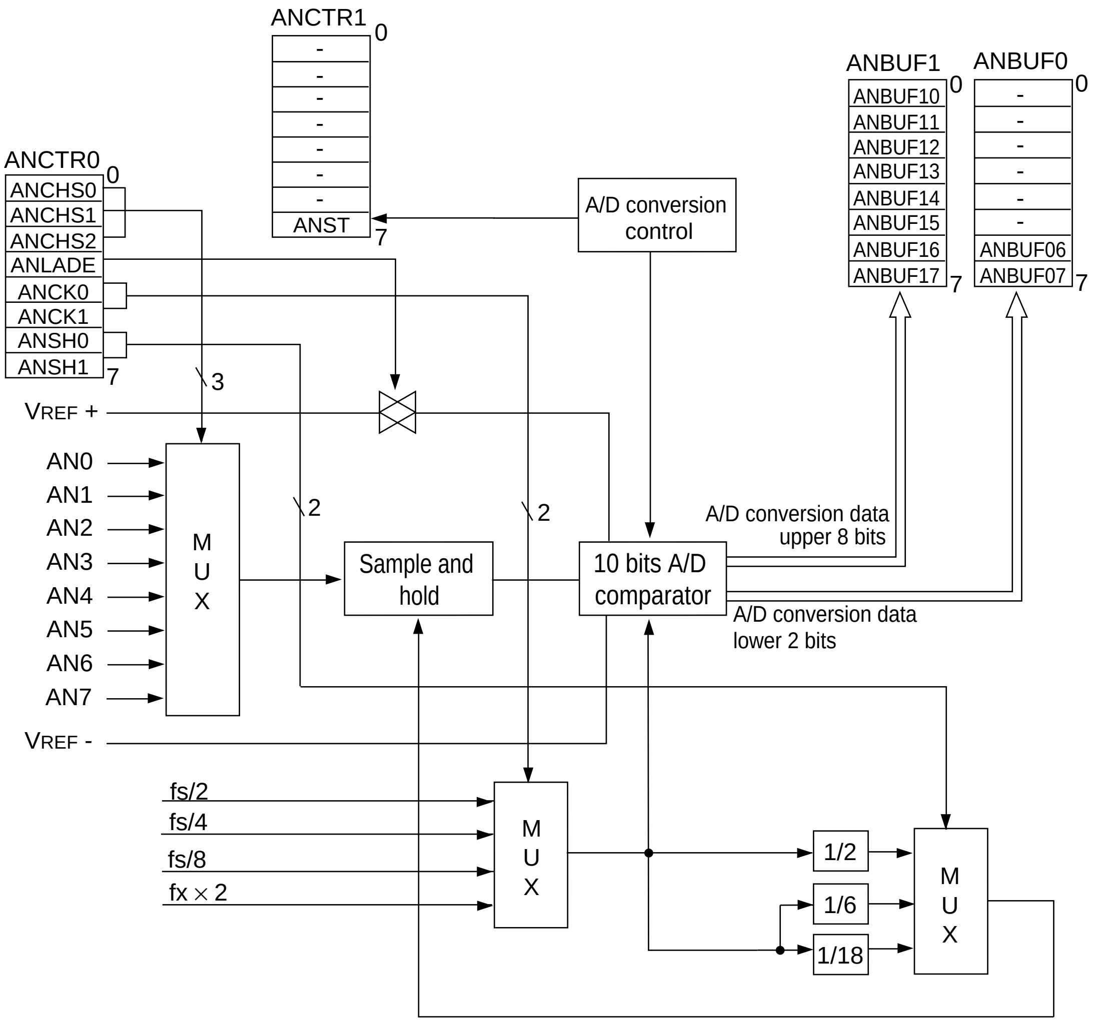


Figure 13-1-1 A/D Converter Block Diagram

13-2 Control Registers

A/D converter consists of the control register (ANCTRn) and the data storage buffer (ANBUFn).

13-2-1 Registers

Table 13-2-1 shows the registers used to control A/D converter.

Table 13-2-1 A/D Converter Control Registers

Register	Address	R/W	Function	Page
ANCTR0	x'03F90'	R/W	A/D converter control register 0	XIII - 5
ANCTR1	x'03F91'	R/W	A/D converter control register 1	XIII - 6
ANBUF0	x'03F92'	R	A/D buffer 0	XIII - 7
ANBUF1	x'03F93'	R	A/D buffer 1	XIII - 7
ADICR	x'03FEA'	R/W	A/D converter interrupt control register	III - 29
PAIMD	x'03F3A'	R/W	Port A input mode register	IV - 45
PAPLUD	x'03F4A'	R/W	Port A pull-up/pull-down resistance control register	IV - 45

R/W : Readable/Writable
R : Readable only

13-2-2 Control Registers

■A/D Converter Control Register 0 (ANCTR0)

	7	6	5	4	3	2	1	0
ANCTR0	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	ANCHS2	ANCHS1	ANCHS0

(At reset : X X X X 0 X X X)

ANCHS2	ANCHS1	ANCHS0	Analog input selection
0	0	0	AN0
		1	AN1
	1	0	AN2
		1	AN3
1	0	0	AN4
		1	AN5
	1	0	AN6
		1	AN7

ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF
1	A/D ladder resistance ON

ANCK1	ANCK0	A/D conversion clock (ftad = 1/T_{AD})
0	0	fs/2
	1	fs/4
1	0	fs/8
	1	fx × 2

* as 800 ns < T_{AD} ≤ 15.26 µs

ANSH1	ANSH0	Sample and hold time
0	0	T_{AD} × 2
	1	T_{AD} × 6
1	0	T_{AD} × 18
	1	Not to use

* Sampling and holding time is decided by the input impedance at analog input.
T_{AD} means the cycle for A/D conversion clock.

Figure 13-2-1 A/D Converter Control Register 0 (ANCTR0 : x'03F90', R/W)

■A/D Converter Control Register 1 (ANCTR1)

ANCTR1 (At reset : 0 - - - - - - -)

	7	6	5	4	3	2	1	0
ANCTR1	ANST	-	-	-	-	-	-	-

ANST	A/D conversion status
0	A/D conversion is completed, stopped.
1	A/D conversion is started, in progress.

Figure 13-2-2 A/D Converter Control Register 1 (ANCTR1 : x'03F91', R/W)

13-2-3　A/D Buffers

They are reading only registers that stores result of A/D conversion.

■A/D Buffer 0 (ANBUF0)

The lower 2 bits from the result of A/D conversion are stored to this register.

	7	6	5	4	3	2	1	0	
ANBUF0	ANBUF07	ANBUF06	-	-	-	-	-	-	(at reset : X X - - - - - -)

Figure 13-2-3　A/D Buffer 0 (ANBUF0 : x'03F92', R)

■A/D Buffer 1 (ANBUF1)

The upper 8 bits from the result of A/D conversion are stored to this register.

	7	6	5	4	3	2	1	0	
ANBUF1	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10	(at reset : X X X X X X X X)

Figure 13-2-4　A/D Buffer 1 (ANBUF1 : x'03F93', R)

13-3 Operation

Here is a description of A/D converter circuit setup procedure.

(1) Set the analog pins.
Set the analog input pin, set in (2), to "special function pin" by the port A input mode register (PAIMD).
*** Setup for the port A input mode register should be done before analog voltage is put to pins.**

(2) Select the analog input pin.
Select the analog input pin from AN7 to AN0 (PA7 to PA0) by the ANCHS2 to ANCHS0 flag of the A/D converter control register 0 (ANCTR0).

(3) Select the A/D converter clock.
Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
Keep the converter clock (TAD) over 800 ns with any resonators.

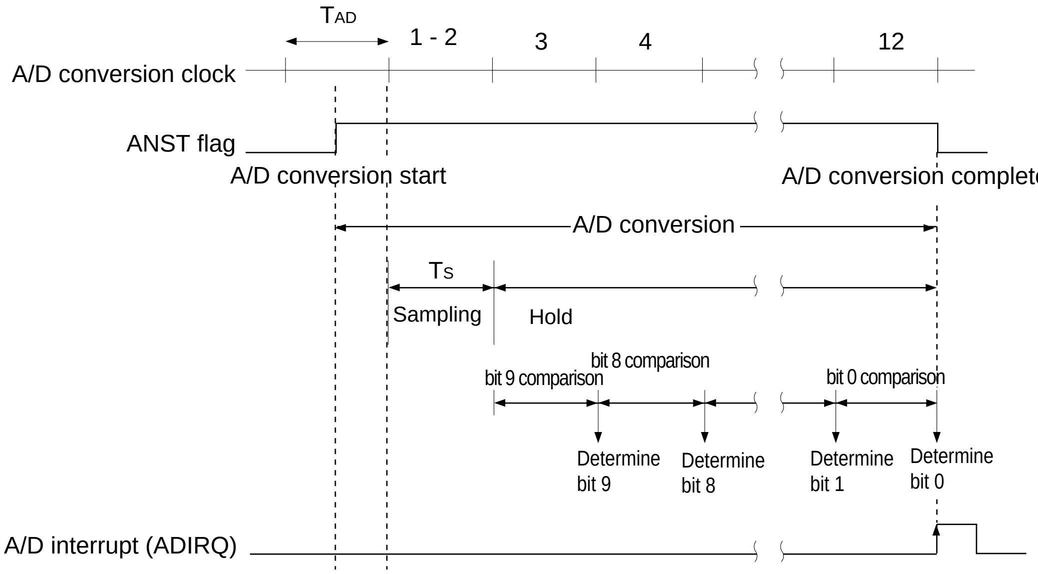
(4) Set the sample hold time.
Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0). The sample hold time should be based on analog input impedance.

(5) Set the A/D ladder resistance.
Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1", and a current flow through the ladder resistance and A/D converter goes into the waiting.
*** (2) to (5) are not in order. (3), (4) and (5) can be operated simultaneously.**

(6) Start the A/D conversion.
Set the ANST flag of the A/D converter control register 1 (ANCTR1) to "1" to start A/D converter.

(7) A/D conversion
Each bit of the A/D buffer 0, 1 is generated after sampled in the sample and hold time set in (3).
Each bit is generated in sequence from MSB to LSB.

(8) Complete the A/D conversion.
When A/D conversion has finished, the ANST flag is cleared to "0", and the result of the conversion is stored to the A/D buffer (ANBUF0, 1). At the same time, the A/D complete interrupt request (ADIRQ) is generated.



* This example is as sampling and hold time is $T_{AD} \times 2$.

Figure 13-3-1 Operation of A/D Conversion

To read the value of the A/D conversion, A/D conversion should be done several times to prevent noise error by confirming the match of level by program, or by using the average value.

13-3-1 Setup

■Input Pins of A/D Converter Setup

Input pins for A/D converter is selected by the ANCH2 to 0 flag of the ANCTR0 register.

Table 13-3-1 Input Pins of A/D Converter Setup

ANCHS2	ANCHS1	ANCHS0	A/D pin
0	0	0	AN0 pin
		1	AN1 pin
	1	0	AN2 pin
		1	AN3 pin
1	0	0	AN4 pin
		1	AN5 pin
	1	0	AN6 pin
		1	AN7 pin

■Clock of A/D Converter Setup

The A/D converter clock is set by the ANCK1 to 0 flag of the ANCTR0 register. Set the A/D converter clock (TAD) more than 800 ns and less than 15.26 µs. Table 13-3-2 shows the machine clock (fosc, fx, fs) and the A/D converter clock (TAD). (calculated as fs = fosc/2, fx/4)

Table 13-3-2 A/D Conversion Clock and A/D Conversion Cycle

ANCK1	ANCK0	A/D conversion clock	A/D conversion cycle (TAD)		
			at oscillation for high speed		at oscillation for low speed
			at fosc = 20 MHz	at fosc = 8.38 MHz	at fx = 32.768 kHz
0	0	fs/2	200.00 ns (unusable)	477.33 ns (unusable)	244.14 µs (unusable)
	1	fs/4	400.00ns (unusable)	954.65ns	488.28 µs (unusable)
1	0	fs/8	800.00 ns	1.91 µs	976.56 µs (unusable)
	1	fx × 2	15.26 µs	15.26 µs	15.26 µs

■Sampling Time (Ts) of A/D Converter Setup

The sampling time of A/D converter is set by the ANSH1 to 0 flag of the ANCTR0 register. The sampling time of A/D converter depends on external circuit, so set the right value by analog input impedance.

Table 13-3-3 Sampling Time of A/D Conversion and A/D Conversion Time

ANSH1	ANSH0	Sampling time (Ts)	A/D conversion time			
			at TAD = 800 ns	at TAD = 954.65 ns	at TAD = 1.91 µs	at TAD = 15.26 µs
0	0	TAD × 2	9.60 µs	11.46 µs	22.92 µs	183.12 µs
	1	TAD × 6	12.80 µs	15.27 µs	30.56 µs	244.16 µs
1	0	TAD × 18	22.40 µs	26.73 µs	53.48 µs	427.28 µs
	1	Reserved	-	-	-	-

■Built-in Ladder Resistor Control

The ANLADE flag of the ANCTR0 register is set to "1" to send a current to the ladder resistance for A/D conversion. As A/D converter is stopped, the ANLADE flag of the ANCTR0 register is set to "0" to save the power consumption.

Table 13-3-4 A/D Ladder Resistor Control

ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF (A/D conversion stopped)
1	A/D ladder resistance ON (A/D conversion stopped)

■A/D Conversion Starting Setup

A/D conversion starting is set by the ANST flag of the ANCTR1 register. The ANST flag of the ANCTR1 register is set to "1" to start A/D conversion. Also, the ANST flag of the ANCTR1 register is set to "1" during A/D conversion, then cleared to "0" as the A/D conversion complete interrupt is generated.

Table 13-3-5 A/D Conversion Starting

ANST	A/D conversion status
0	A/D conversion completed or stopped.
1	A/D conversion started or in progress.

13-3-2 Setup Example

■A/D Converter Setup Example by Registers

A/D conversion is started by setting registers. The analog input pins are set to AN0, the converter clock is set to fs/4, and the sampling hold time is set to TAD × 6. Then, A/D conversion complete interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD (x'3F3A') bp0 : PAIMD0 = 1 PAPLUD (x'3F4A') bp0 : PAPLUD0 = 0	(1) Set the analog input pin, set in (2), to the special function pin by the port A input mode register (PAIMD). Also, set no pull-up/pull-down resistance by the port A pull-up/pull-down resistance control register (PAPLUD).
(2) Select the analog input pin. ANCTR0 (x'3F90') bp2-0 : ANCHS2-0 = 000	(2) Set the AN0 (PA0) to the analog input pin by setting the ANCHS2-0 flag of the A/D converter control register 0 (ANCTR0) to "000".
(3) Select the A/D converter clock. ANCTR0 (x'3F90') bp5-4 : ANCK1-0 = 01	(3) Set the fs/4 to the A/D converter clock by setting the ANCK1-0 flag of the A/D converter control register 0 (ANCTR0) to "01".
(4) Set the sample and hold time. ANCTR0 (x'3F90') bp7-6 : ANSH1-0 = 01	(4) Set the TAD × 6 to the sample and hold time by setting the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0) to "01".
(5) Set the interrupt level. ADICR (x'3FEA') bp7-6 : ADLV1-0 = 00	(5) Set the interrupt level by the ADLV1-0 flag of the A/D conversion complete interrupt control register (ADICR). If any interrupt request flag had already been set, clear it. [☞ Chapter 3. 3-1-4 Interrupt Flag Setting]
(6) Enable the interrupt. ADICR (x'3FEA') bp1 : ADIE = 1	(6) Enable the interrupt by setting the ADIE flag of the ADICR register to "1".
(7) Set the A/D ladder resistance. ANCTR0 (x'3F90') bp3 : ANLADE = 1	(7) Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.

Setup Procedure	Description
(8) Start the A/D conversion. ANCTR1 (x'3F91') bp7 : ANST = 1	(8) Set the ANST flag of the A/D converter control register 1 (ANCTR1) to "1" to start the A/D conversion.
(9) Complete the A/D conversion. ANBUF0 (x'3F92') ANBUF1 (x'3F93')	(9) When the A/D conversion has finished, the A/D conversion complete interrupt is generated and the ANST flag of the A/D converter control register 1 (ANCTR1) is cleared to "0". The result of the conversion is stored to the A/D converter buffer (ANBUF0, 1).

Note : The above (2) to (4) can be set at once.

Start the A/D conversion after the current flowing through the ladder resistors stabilizes. The wait time should be decided by the calculated time from the ladder resistance (max. 80 kΩ) and the external bypass capacitor connected between V_{REF+} and V_{REF-}.

13-3-3 Cautions

Since conversion can be damaged by noise easily, antinoise measures are necessary.

■Antinoise measures
For A/D input (analog input pin), add condenser near the VSS pins of micro controller.

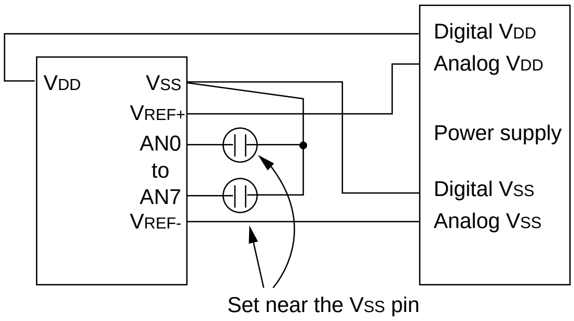


Figure 13-3-2 A/D Converter Recommended Example 1

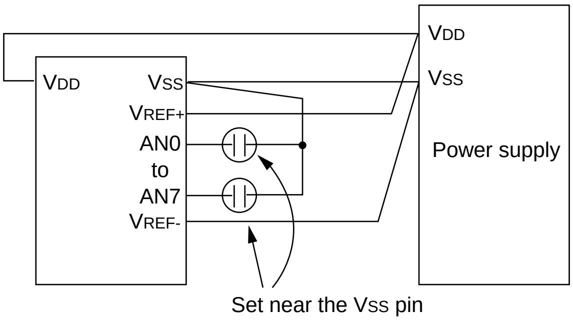
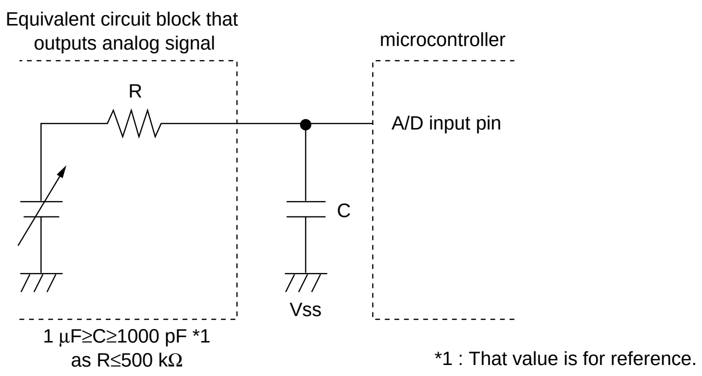


Figure 13-3-3 A/D Converter Recommended Example 2

For high precision of A/D conversion, the following cautions on A/D converter should be kept.

1. The input impedance R of A/D input pin should be under 500 kΩ[*1], and the external capacitor C (more than 1000 pF, under 1 µF)[*1].
2. The A/D conversion frequency should be set with consideration of R, C time constant.
3. At the A/D conversion, if the input level of micro controller is changed, or the peripheral added circuit is switched to ON/OFF, the A/D conversion may work wrongly, because the analog input pins and power pins does not fix. At the check of the setup, confirm the wave form of analog input pins.



Recommend Connection with A/D Converter

Chapter 14 Appendices

14-1 EPROM Version

14-1-1 Overview

EPROM version is microcomputer which was replaced the mask ROM of the MN101C38 series with an electronically programmable EPROM. There are MN101CP38CAF/HL and PX-AP101C38-AC/HC for MN101C38 series.

The MN101CP38CAF and the MN101CP38CHL are sealed in plastic. Once data is written to the internal EPROM, it cannot be erased. The PX-AP101C38-AC/HC are sealed in a ceramic package with a window. Written data can be erased by exposing the physical chip to intense ultraviolet radiation. We offer the PX-AP101C38-AC/HC for a 100-pin flat package.

Setting the EPROM version to EPROM mode, functions as a microcomputer are halted, and the internal EPROM can be programmed. For EPROM mode pin connection, refer to figure 14-1-2. Programming Adapter Connection.

The specification for writing to the internal EPROM are the same as for a general-purpose 1 M-bit EPROM (V_{PP} = 12.5 V, tpw = 0.2 ms). Therefore, by using a dedicated programming adapter (supplied by Panasonic) which can convert the 100 pin of EPROM version to 32 pin, having the same configuration as a normal EPROM, a general-purpose ROM writer can be used to perform read and write operations.

The EPROM Version is described on the following items :

- Cautions on use of the internal EPROM
- Erasing Data in Windowed Package (PX-AP101C38-AC/HC)
- Differences between mask ROM version and EPROM version
- Writing to the Microcomputer with internal EPROM
- Cautions on handling a ROM writer
- Programming Adapter Connection
- Option bit

14-1-2 Cautions on Use

EPROM Version differs from the MN101C38C/38A Mask ROM Version in some of its electrical characteristics. The user should be aware of the following cautions :

(1) To prevent data from being erased by ultraviolet light after a program is written, affix seals impermeable to UV rays to the glass sections at the top and side sections of the CPU.
(PX-AP101C38-AC, PX-AP101C38-HC)

(2) Because of device characteristics of the MN101CP38xxx, a writing test cannot be performed on all bits.Therefore, the reliability of data writing may not be 100% ensured.

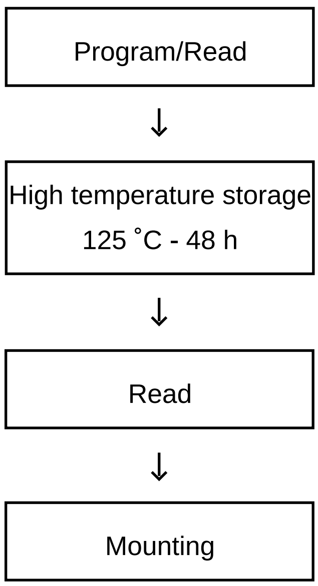
(3) When a program is being written, be sure that V_{DD} power supply (6 V) is connected before applying the V_{PP} power supply (12.5 V). Disconnect the V_{PP} supply before disconnecting the V_{DD} supply.

(4) V_{PP} should never exceed + 13.5 V including overshoot.

(5) If a device is removed while a V_{PP} of + 12.5 V is applied, device reliability may be damaged.

(6) At NCE = V_{IL}, do not change Vpp from V_{IL} to + 12.5 V or from + 12.5 V to V_{IL}.

(7) After a program is written, screening at a high temperature storage before mounting is recommended.



14-1-3 Erasing Data in Windowed Package (PX-AP101C38-AC/HC)

To erase data of an internal EPROM with windowed packaging ("0" → "1"), UV light at 253.7 nm is used to irradiate the chip through a permeable cover.

The recommended exposure is 10 W·s/cm^2. This coverage can be achieved by using a commercial UV lamp positioned 2 to 3 cm above the package for 15 - 20 minutes (when the illumination intensity of the package surface is 12000 µW/cm^2). Remove any filters attached to the lamp. With a mirrored reflector plate to the lamp, illumination intensity will increase 1.4 to 1.8 times, and decrease the erasure time.

If the window becomes dirty with oil, adhesive, etc., UV light permeability will get worse, causing the erasure time to increase. If this happens, clean with alcohol or another solvent that will not harm the package. The above recommended exposure has enough leeway, with several times as much as it takes to erase all the bits. It is based on the reliable data over all temperature and voltage. The lump and the level of illumination should be regularly checked and well controlled.

Data in internal EPROM with windowed packaging is erased by applying a light that the wavelength is shorter than 400 nm. Fluorescent lamp and sunlight are not able to erase data as much as UV light of 253.7 nm is, but those light sources are also able to erase data more or less. To expose those light sources for a long while can damage its system. To prevent this, cover the window with an opaque label.

If the wavelength is longer than 400 nm to 500 nm, data can not be erased. However, because of typical semiconductor characteristics, the circuit may malfunction if the chip is exposed to an extremely high illumination intensity. The chip will operate normally if this exposure is stopped. However, for areas where it is continuous, take necessary precautions against the light that the wavelength is longer than 400 nm.

14-1-4 Differences between Mask ROM Version and EPROM Version

The differences between the 8-bit microcontroller MN101C38 series (Mask ROM version) and MN101CP38C (internal EPROM version) are as follows ;

Table 14-1-1 Differences between Mask ROM version and internal EPROM version

	MN101C38 series (Mask ROM version)	MN101CP38C (EPROM version)
Operating voltage	2.0 V to 5.5 V(1.00 µs / at 2 MHz) 2.0 V to 5.5 V (125 µs / at 32.768 kHz)	2.3 V to 5.5 V(1.00 µs / at 2 MHz) 2.3 V to 5.5 V (125 µs / at 32.768 kHz)
Pin DC Characteristics	Output current, input current and input judge level are the same.	
Option bits (Settings for operating mode after reset and watchdog timer frequency) [☞ Chapter 1 1-6. Option]	ROM option	EPROM option
	Data for ROM option setting is used as option data.	Data for EPROM option setting is used as option data.
Oscillation characteristics	The combination of oscillator and each version should be estimated to match when EPROM version is changed to Mask ROM version for mass production.	
Noise characteristics	EMC check should be done on each version when EPROM version is changed to Mask ROM version for mass production.	

There are no other functional differences.

14-1-5 Writing to Microcomputer with Internal EPROM

The device type that set by each ROM writer should be selected the mode for writing 1 M-bit EPROM.
Set the writing voltage to 12.5 V.

■Mounting the device in the programming adapter and the position of the No.1 pin.

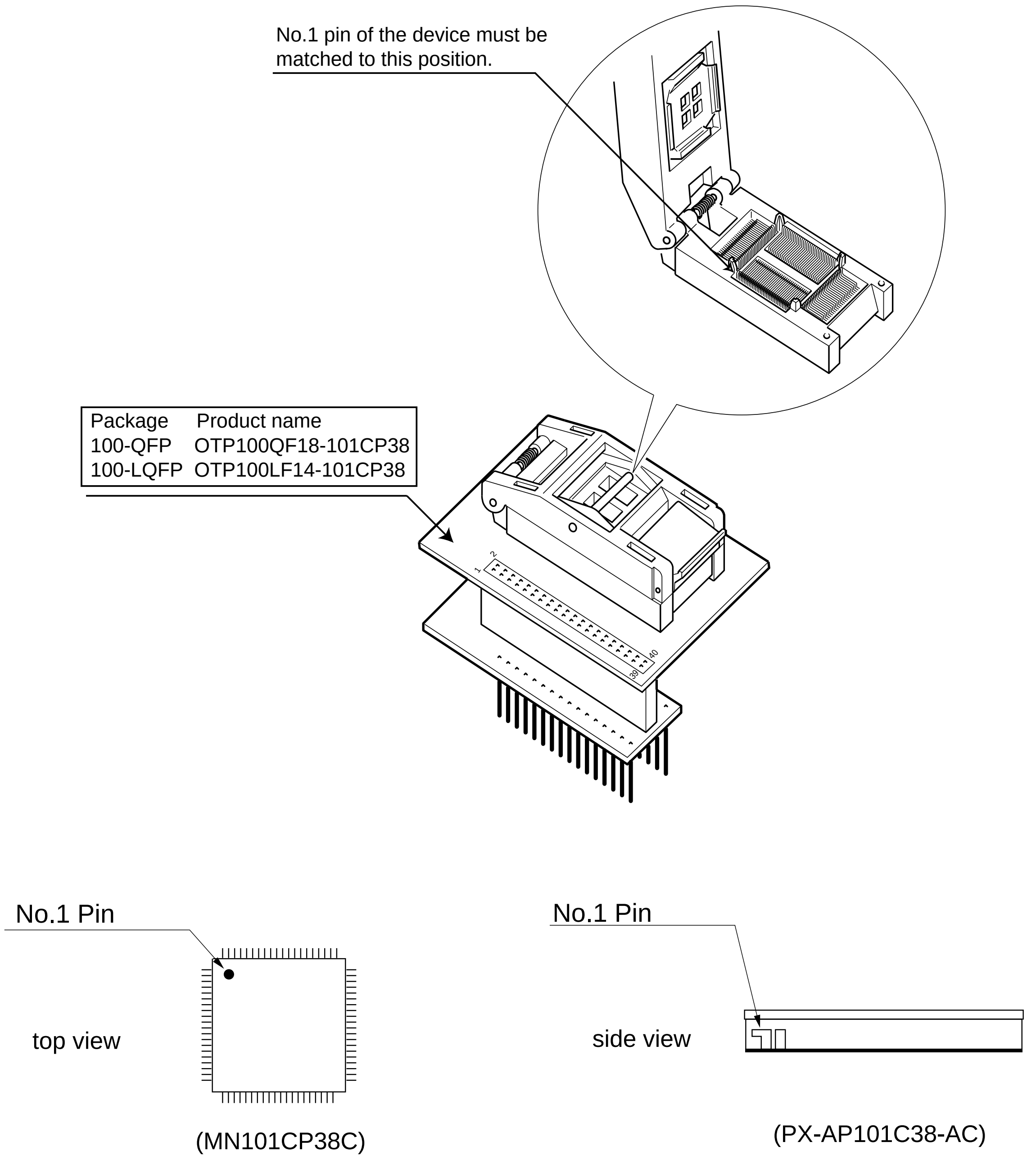


Figure 14-1-1 Mounting a Device in Programming Adapter and the Position of No.1 Pin

■ROM Writer Setup

The device types should be set up as listed below.

Table 14-1-2 Setup for Device Type

Equip. name	Vendor	Device type	Remarks
Pecker30	Aval Data	Hitachi 27C101	
		Mitsubishi 27C101	
2900	Data I/O	Hitachi 27C101	Do not run ID check.
		Mitsubishi 27C101	
ChipLab	Data I/O	Hitachi 27C101	Do not run ID check and pin connection inspection.
		Mitsubishi 27C101	

The above table is based on the standard samples.

14-1-6 Cautions on Operation of ROM Writer

■Cautions on Handling the ROM writer

(1) The V_{PP} programming voltage for the EPROM versions is 12.5 V.
Programming with a 21 V ROM writer can lead to damage. The ROM writer specifications must match those for standard 1 M-bit EPROM : V_{PP} = 12.5 V ; tpw = 0.2 ms.

(2) Make sure that the socket adapter matches the ROM writer socket and that the chip is correctly mounted in the socket adapter. Faulty connections can damage the chip.

(3) After clearing all memory of the ROM writer, load the program to the ROM writer.

(4) After confirming the device type, write the loaded program in (3) to this LSI address, from x'4000' to the final address of the internal ROM.

(5) There is the same address for ROM option setting, even on EPROM version.

[☞ Chapter 14 14-1-8. Option Bit]

> The internal ROM space of this LSI is from x'4000'.
> [☞ Chapter 2 2-2. Memory Space]

> This writer has no internal ID codes of "Silicon Signature" and "Intelligent Identifier" of the auto-device selection command of ROM writer. If the auto-device selection command is to be executed for this writer, the device is likely damaged. Therefore, never use this command.

■When the writing is disabled

When the writing is disabled, check the following points.

(1) Check that the device is mounted correctly on the socket (pin bending, connection failure).

(2) Check that the erase check result is no problem.

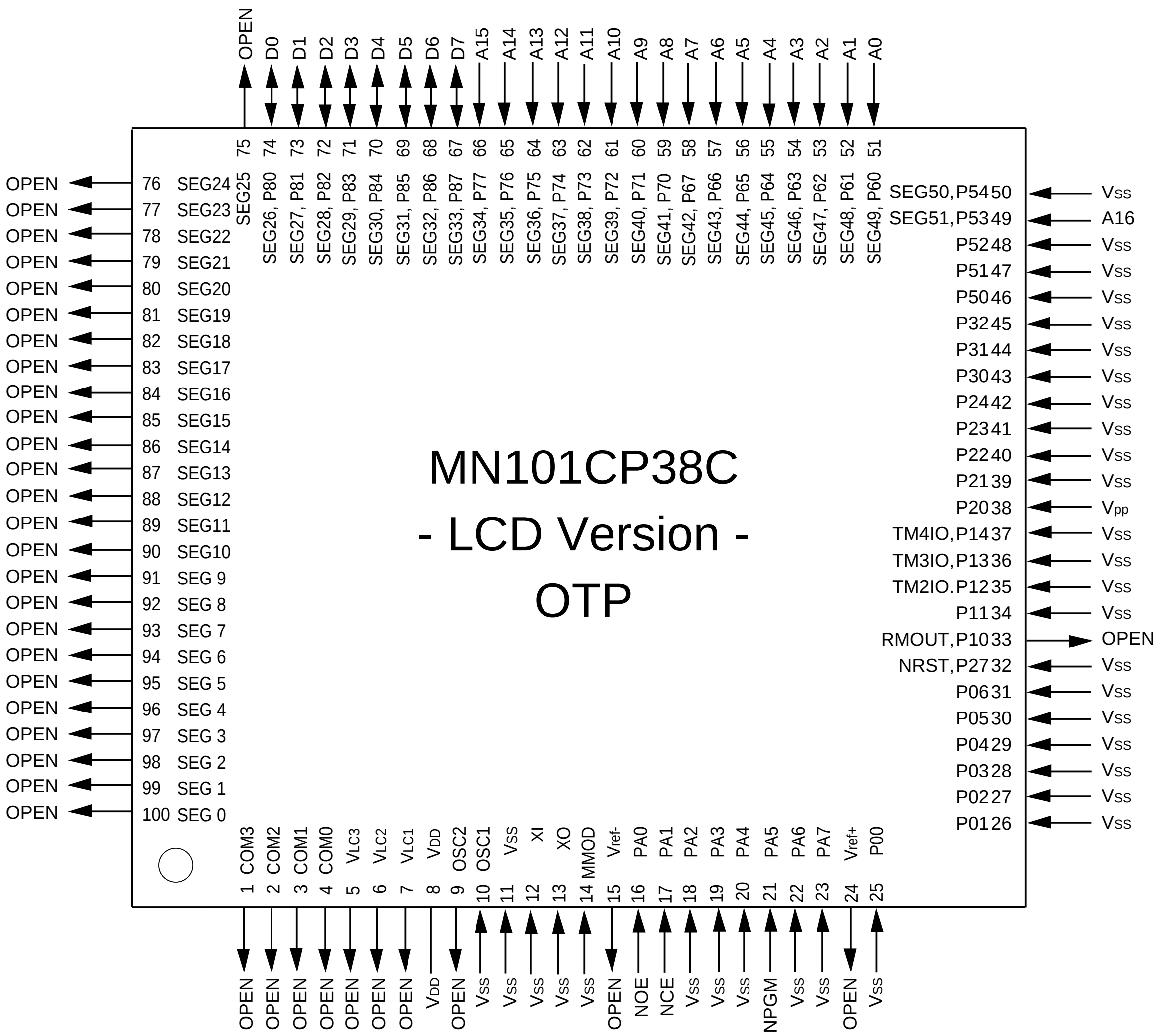
(3) Check that the adapter type is identical to the device name.

(4) Check that the writing mode is set correctly.

(5) Check that the data is correctly transferred to the ROM writer.

(6) Recheck the check points (1) to (5) provided on the above paragraph of 'Cautions on Handling the ROM writer'.

14-1-7 Programming Adapter Connection



Package : LQFP100-P-1414 *1 / QFP100-P-1818B
Pin pitch : 0.5 mm / 0.65 mm

***1 Under development**

Figure 14-1-2 MN101CP38C EPROM Programming Adapter Connection

14-1-8 Option Bit

MN101CP38C has EPROM option address to specify the operating mode after reset and the watchdog timer frequency.

■EPROM Option Bits

7	6	5	4	3	2	1	0
-	-	WDMD	-	-	WDSEL2	WDSEL1	NSSTRT

NSSTRT	Operating mode after reset
0	SLOW mode
1	NORMAL mode

WDSEL2	WDSEL1	Watchdog timer frequency
0	0	$fs/2^{16}$
	1	$fs/2^{18}$
1	X	$fs/2^{20}$

WDMD	Must be set "1".

Figure 14-1-3 EPROM Option Bits

Model	EPROM option address
MN101CP38C	x'0FFFF'

Even if SLOW mode is selected after reset, connect oscillator pins as well as to the high speed oscillation input.

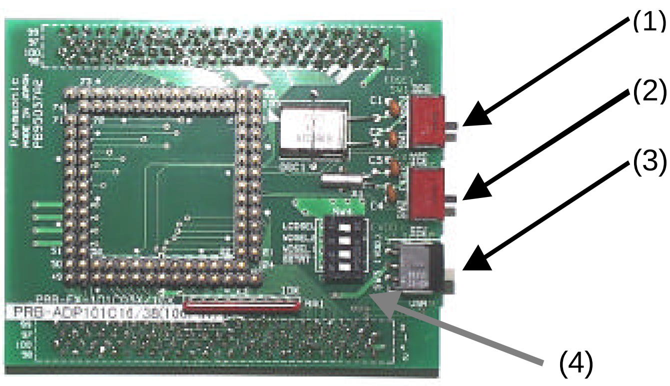
The WDMD (bp5) should be always set to "1". If it is set to "0", that operation cannot be stopped after the watchdog timer is started.

14-2 Probe Switches

14-2-1 PRB-ADP101C16/38 (100PIN) Probe Switches

Adapter boards vary depending upon the models. This adapter board must be used for only MN101C16/38(100PIN).
Use the adapter board with an EV board, PRB-EV101C15.
Improper matching may cause any damage to the ICE.
The switches that the adapter board provides for configuring the probe are described below.

Adapter Board Layout



(1) Oscillator control (SW1)

Set this switch to its USR position to drive the in-circuit emulator with the oscillator built into the target device. If there is no target device, set this switch to the ICE position to use the oscillator built into the probe.

(2) X1 control (SW2)

Set this switch to its USR position to drive the in-circuit emulator with the X1 oscillator built into the target device. If there is no target device, set this switch to the ICE position to use the oscillator built into the probe.

(3) Power supply control (SW3)

Set this switch to its USR position to use the power supply from the target device. If there is no target device, set this switch to the ICE position to use the 5-volt power supply from the in-circuit emulator.

(4) Function control DIP switches

These switch settings vary with the individual target device as described below.

LCDSEL ON: if using LCD
OFF: if using LED

Watchdog Timer Frequency (WDSEL2, WDSEL1)

Switch settings		Watchdog timer Frequency
WDSEL1	WDSEL2	
OFF	OFF	fosc/2^{17}
ON	OFF	fosc/2^{19}
Don't care	ON	fosc/2^{21}

Starting Oscillation, after a reset ($\overline{\text{SSTRT}}$)
ON: Low-speed (X1) operation
OFF: High-speed (OSC)

14-2-2 PRB-EV101C15

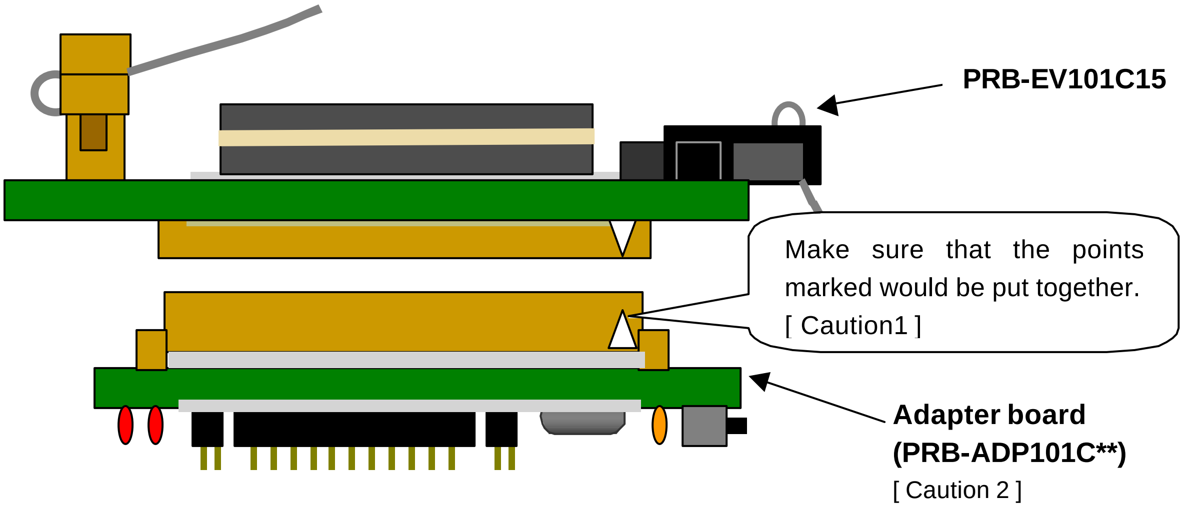
<Compatible devices>

-This board corresponds to the following devices.
(The product type is subject to change without prior notice. The latest information should be confirmed on our web site.)

- MN101C08	- MN101C16	- MN101C39
- MN101C09	- MN101C24	- MN101C42
- MN101C10	- MN101C27	- MN101C45
- MN101C11	- MN101C28	- MN101C48
- MN101C14	- MN101C30	- MN101C51
- MN101C15	- MN101C38	

< How to connect >

Figure 1. Connecting a PRB-EV101C15 to an Adapter board(PRB-ADP101C)**



[Caution1]
When connect the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

[Caution2]
Please visit our web site to check the adapter boards corresponding to your microcomputer .we update the web site periodically.

14-3 Special Function Registers List

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
x'3F00'	CPUM	-	Reserved	Reserved	Reserved	STOP	HALT	OSC1	OSC0	II - 24
		-	0	0	0	0	0	0	0	
			Set always "0"	Set always "0"	Set always "0"	STOP transition request	HALT transition request	Oscillation control		
x'3F01'	MEMCTR	IOW1	IOW0	IVBA	EXMEM	EXWH	IRWE	EXW1	EXW0	II - 17
		1	1	0	0	1	0	1	1	
		I/O wait setup		Interrupt vector address	External memory expansion mode specified	Fixes wait mode / Hand shake mode	Interrupt request flag	Wait cycle of external memory		
x'3F02'	WDCTR	-	-	-	-	-	-	-	WDEN	VIII - 3
		-	-	-	-	-	-	-	0	
									WDT activation	
x'3F03'	DLYCTR	BUZOE	BUZCK1	BUZCK0	-	-	-	DLYS1	DLYS0	II - 33 IX - 3
		0	x	x	-	-	-	0	0	
		Enable buzzer output	Buzzer output frequency setup					Oscillation stabilization wait cycle setup		
x'3F0E'	EXADV	EXADV3	EXADV2	EXADV1	-	-	-	-	-	II - 18 IV - 25, 36
		0	0	0	-	-	-	-	-	
		A17/A16 address output at memory expansion mode	A15 to A12 address output at memory expansion mode	A11 to A8 address output at memory expansion mode						
x'3F10'	P0OUT	-	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0	IV - 7
		-	0	0	0	0	0	0	0	
			Port 0 output data							
x'3F11'	P1OUT	-	-	-	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	IV - 13
		-	-	-	0	0	0	0	0	
					Port 1 output data					
x'3F12'	P2OUT	P2OUT7	-	-	-	-	-	-	-	IV - 18
		1	-	-	-	-	-	-	-	
		Port2 output data								
x'3F13'	P3OUT	-	-	-	-	-	P3OUT2	P3OUT1	P3OUT0	IV - 21
		-	-	-	-	-	0	0	0	
							Port 3 output data			
x'3F15'	P5OUT	-	-	-	P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0	IV - 24
		-	-	-	0	0	0	0	0	
					Port 5 output data					
x'3F16'	P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	IV - 30
		0	0	0	0	0	0	0	0	
		Port 6 output data								
x'3F17'	P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0	IV - 35
		0	0	0	0	0	0	0	0	
		Port 7 output data								
x'3F18'	P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	IV - 41
		0	0	0	0	0	0	0	0	
		Port 8 output data								

Note) x : Initial value is unstable - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
x'3F1F'	SYSMD	SYSMD7	SYSMD6	SYSMD5	SYSMD4	SYSMD3	SYSMD2	SYSMD1	SYSMD0	IV - 37
		0	0	0	0	0	0	0	0	
		I/O port / Synchronous output control								
x'3F20'	P0IN	-	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0	IV - 7
		-	x	x	x	x	x	x	x	
			Port 0 input data							
x'3F21'	P1IN	-	-	-	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	IV - 13
		-	-	-	x	x	x	x	x	
					Port 1 input data					
x'3F22'	P2IN	-	-	-	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0	IV - 18
		-	-	-	x	x	x	x	x	
					Port 2 input data					
x'3F23'	P3IN	-	-	-	-	-	P3IN2	P3IN1	P3IN0	IV - 21
		-	-	-	-	-	x	x	x	
							Port 3 input data			
x'3F25'	P5IN	-	-	-	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0	IV - 24
		-	-	-	x	x	x	x	x	
					Port 5 input data					
x'3F26'	P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	IV - 30
		x	x	x	x	x	x	x	x	
		Port 6 input data								
x'3F27'	P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0	IV - 35
		x	x	x	x	x	x	x	x	
		Port 7 input data								
x'3F28'	P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	IV - 41
		x	x	x	x	x	x	x	x	
		Port 8 input data								
x'3F2A'	PAIN	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0	IV - 45
		x	x	x	x	x	x	x	x	
		Port A input data								
x'3F30'	P0DIR	-	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0	IV - 7
		-	0	0	0	0	0	0	0	
			Port 0 I/O direction control							
x'3F31'	P1DIR	-	-	-	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	IV - 13
		-	-	-	0	0	0	0	0	
					Port 1 I/O direction control					
x'3F33'	P3DIR	-	-	-	-	-	P3DIR2	P3DIR1	P3DIR0	IV - 21
		-	-	-	-	-	0	0	0	
							Port 3 I/O direction control			
x'3F35'	P5DIR	-	-	-	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0	IV - 24
		-	-	-	0	0	0	0	0	
					Port 5 I/O direction control					

Note) x : Initial value is unstable - : No data

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
x'3F36'	P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	IV - 30
		0	0	0	0	0	0	0	0	
		Port 6 I/O direction control								
x'3F37'	P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0	IV - 35
		0	0	0	0	0	0	0	0	
		Port 7 I/O direction control								
x'3F38'	P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	IV - 41
		0	0	0	0	0	0	0	0	
		Port 8 I/O direction control								
x'3F39'	P1OMD	-	-	-	P14TCO	P13TCO	P12TCO	-	P10TCO	IV - 14
		-	-	-	0	0	0	-	0	
					I/O port / Special function pin control					
x'3F3A'	PAIMD	PAIMD7	PAIMD6	PAIMD5	PAIMD4	PAIMD3	PAIMD2	PAIMD1	PAIMD0	IV - 45
		0	0	0	0	0	0	0	0	
		I/O port / Special function pin control								
x'3F3C'	P4IMD	IRQ4SEL	-	-	-	P4KYEN4	P4KYEN3	P4KYEN2	P4KYEN1	III - 37 IV - 47
		0	-	-	-	0	0	0	0	
		IRQ4 interrupt source selection				PA6, PA7 key interrupt selection	PA4, PA5 key interrupt selection	PA2, PA3 key interrupt selection	PA0, PA1 key interrupt selection	
x'3F40'	P0PLU	-	P0PLU6	P0PLU5	P0PLU4	P0PLU3	P0PLU2	P0PLU1	P0PLU0	IV - 7
		-	0	0	0	0	0	0	0	
			Port 0 pull-up resistor ON / OFF							
x'3F41'	P1PLU	-	-	-	P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0	IV - 13
		-	-	-	0	0	0	0	0	
					Port 1 pull-up resistor ON / OFF					
x'3F42'	P2PLU	-	-	-	P2PLU4	P2PLU3	P2PLU2	P2PLU1	P2PLU0	IV - 18
		-	-	-	0	0	0	0	0	
					Port 2 pull-up resistor ON / OFF					
x'3F43'	P3PLU	-	-	-	-	-	P3PLU2	P3PLU1	P3PLU0	IV - 21
		-	-	-	-	-	0	0	0	
							Port 3 pull-up resistor ON / OFF			
x'3F45'	P5PLU	-	-	-	P5PLU4	P5PLU3	P5PLU2	P5PLU1	P5PLU0	IV - 24
		-	-	-	0	0	0	0	0	
					Port 5 pull-up resistor ON / OFF					
x'3F46'	P6PLU	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0	IV - 30
		0	0	0	0	0	0	0	0	
		Port 6 pull-up resistor ON / OFF								
x'3F47'	P7PLUD	P7PLUD7	P7PLUD6	P7PLUD5	P7PLUD4	P7PLUD3	P7PLUD2	P7PLUD1	P7PLUD0	IV - 35
		0	0	0	0	0	0	0	0	
		Port 7 pull-up / pull-down resistor ON / OFF								
x'3F48'	P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	IV - 41
		0	0	0	0	0	0	0	0	
		Port 8 pull-up resistor ON / OFF								

Note) x : Initial value is unstable - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
x'3F4A'	PAPLUD	PAPLUD7	PAPLUD6	PAPLUD5	PAPLUD4	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0	IV - 45
		0	0	0	0	0	0	0	0	
		Port A pull-up / pull-down resistor ON / OFF								
x'3F4B'	FLOAT1	-	-	-	-	-	P21M	PARDWN	P7RDWN	IV - 37, 46
		-	-	-	-	-	0	0	0	
							P21 input mode selection	Port A pull-up / pull-down selection	Port 7 pull-up / pull-down selection	
x'3F4C'	FLOAT2	-	-	-	-	-	-	P7SYEVS2	P7SYEVS1	IV - 37
		-	-	-	-	-	-	0	0	
								Port 7 synchronous output event selection		
x'3F50'	SC0MD0	-	SC0CE0	SC0CE1	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0	X - 6
		-	0	0	x	x	0	0	0	
			Reception data input edge / Transmission data output edge		First bit to be transferred	Synchronous serial data transfer start condition	Synchronous serial transfer bit count			
x'3F51'	SC0MD1	-	-	SC0CKM	SC0CK1	SC0CK0	SC0BRKF	SC0ERE	SC0TRI	X - 7
		-	-	x	0	0	0	0	0	
				1/8 dividing of transfer clock	Clock source		Brake status receive monitor	Error monitor	Transmission / Reception interrupt request flag	
x'3F52'	SC0MD2	-	-	SC0BRKE	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	X - 8
		-	-	0	0	0	x	x	x	
				Brake status transmit control	Frame mode specification		Added bit specification		Parity Enable	
x'3F53'	SC0MD3	-	-	SC0IOM	SC0SBOM	SC0SBTM	SC0SBOS	SC0SBIS	SC0SBTS	X - 9
		-	-	0	0	0	0	0	0	
				SBI0 / SBO0 pin connection	SBO0 pin configuration	SBT0 pin configuration	SBO0 pin function	SBI0 input control	SBT0 pin function	
x'3F54'	SC0CTR	SC0BSY	SC0CMD	-	-	SC0FEF	SC0PEK	SC0ORE	-	X - 10
		0	0	-	-	0	0	0	-	
		Serial bus status	Clock synchronous / UART			Framing error detection	Parity error detection	Overrun error detection		
x'3F55'	SC0TRB	SC0TRB7	SC0TRB6	SC0TRB5	SC0TRB4	SC0TRB3	SC0TRB2	SC0TRB1	SC0TRB0	X - 5
		x	x	x	x	x	x	x	x	
		Serial interface 0 transmission / reception shift register								
x'3F56'	SC0RXB	SC0RXB7	SC0RXB6	SC0RXB5	SC0RXB4	SC0RXB3	SC0RXB2	SC0RXB1	SC0RXB0	X - 5
		x	x	x	x	x	x	x	x	
		Serial interface 0 reception data buffer								
x'3F57'	SC1MD0	SC1BSY	SC1CE0	SC1CE1	SC1DIR	SC1STE	SC1LNG2	SC1LNG1	SC1LNG0	XI - 6
		0	0	0	x	x	0	0	0	
		Serial bus status	Reception data input edge / Transmission data output edge		First bit to be transferred	Synchronous serial interface start condition	Transfer bit count			
x'3F58'	SC1MD1	-	SC1SBOM	SC1SBTM	SC1SBOS	SC1SBIS	SC1SBTS	SC1CK1	SC1CK0	XI - 7
		-	0	0	0	0	0	0	0	
			SBO1 pin configuration	SBT1 pin configuration	SBO1 pin function	SBI1 pin function	SBT1 pin function	Clock source		
x'3F59'	SC1TRB	SC1TRB7	SC1TRB6	SC1TRB5	SC1TRB4	SC1TRB3	SC1TRB2	SC1TRB1	SC1TRB0	XI - 5
		x	x	x	x	x	x	x	x	
		Serial interface 1 transmission / reception shift register								
x'3F62'	TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	V - 6
		0	0	0	0	0	0	0	0	
		Timer 2 binary counter								

Note) x : Initial value is unstable - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
x'3F63'	TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	V - 6
		-	-	-	0	0	0	0	0	
		Timer 3 binary counter								
x'3F64'	TM4BCL	TM4BCL7	TM4BCL6	TM4BCL5	TM4BCL4	TM4BCL3	TM4BCL2	TM4BCL1	TM4BCL0	VI - 5
		0	0	0	0	0	0	0	0	
		Timer 4 binary counter (lower 8 bits)								
x'3F65'	TM4BCH	TM4BCH7	TM4BCH6	TM4BCH5	TM4BCH4	TM4BCH3	TM4BCH2	TM4BCH1	TM4BCH0	VI - 5
		0	0	0	0	0	0	0	0	
		Timer 4 binary counter (upper 8 bits)								
x'3F66'	TM4ICL	TM4ICL7	TM4ICL6	TM4ICL5	TM4ICL4	TM4ICL3	TM4ICL2	TM4ICL1	TM4ICL0	VI - 6
		0	0	0	0	0	0	0	0	
		Timer 4 input capture register (lower 8 bits)								
x'3F67'	TM4ICH	TM4ICH7	TM4ICH6	TM4ICH5	TM4ICH4	TM4ICH3	TM4ICH2	TM4ICH1	TM4ICH0	VI - 6
		x	x	x	x	x	x	x	0	
		Timer 4 input capture register (upper 8 bits)								
x'3F68'	TM5BC	TM5BC7	TM5BC6	TM5BC5	TM5BC4	TM5BC3	TM5BC2	TM5BC1	TM5BC0	VII - 5
		0	0	0	0	0	0	0	0	
		Timer 5 binary counter								
x'3F72'	TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	V - 6
		x	x	x	x	x	x	x	x	
		Timer 2 compare register								
x'3F73'	TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	V - 6
		x	x	x	x	x	x	x	x	
		Timer 3 compare register								
x'3F74'	TM4OCL	TM4OCL7	TM4OCL6	TM4OCL5	TM4OCL4	TM4OCL3	TM4OCL2	TM4OCL1	TM4OCL0	VI - 5
		x	x	x	x	x	x	x	x	
		Timer 4 compare register (lower 8 ibts)								
x'3F75'	TM4OCH	TM4OCH7	TM4OCH6	TM4OCH5	TM4OCH4	TM4OCH3	TM4OCH2	TM4OCH1	TM4OCH0	VI - 5
		x	x	x	x	x	x	x	x	
		Timer 4 compare register (upper 8 bits)								
x'3F78'	TM5OC	TM5OC7	TM5OC6	TM5OC5	TM5OC4	TM5OC3	TM5OC2	TM5OC1	TM5OC0	VII - 5
		x	x	x	x	x	x	x	x	
		Timer 5 compare register								
x'3F82'	TM2MD	-	-	-	TM2EN	TM2PWM	TM2CK2	TM2CK1	TM2CK0	V - 7
		-	-	-	0	0	x	x	x	
					Timer 2 count control	Timer 2 operation mode	Clock source			
x'3F83'	TM3MD	-	-	-	TM3EN	TM3PWM	TM3CK2	TM3CK1	TM3CK0	V - 8
		-	-	-	0	0	x	x	x	
					Timer 3 count control	P13 output at TM2PWM operation	Clock source			
x'3F84'	TM4MD	-	TM4EN	TM4PWM	T4ICTS1	T4ICTS0	TM4CK2	TM4CK1	TM4CK0	VI - 7
		-	0	0	0	0	x	x	x	
			Timer 4 count control	Timer 4 operation mode	Capture trigger for TM4		Clock source			

Note) x : Initial value is unstable - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
x'3F88'	TM5MD	TM5CLRS	TM5IR2	TM5IR1	TM5IR0	TM5CK3	TM5CK2	TM5CK1	TM5CK0	VII - 6
		0	x	x	x	x	x	x	0	
		tm5 binary counter clear	Time base timer interrupt cycle			Timer 5 clock source			Time base timer clock source	
x'3F89'	RMCTR	-	-	-	Reserved	RMOEN	Reserved	RMDTY0	RMBTMS	V - 9
		-	-	-	0	0	x	x	0	
					Set always "0"	Enable remote control carrier output	Set always "0"	Remote control carrier output duty	Remote control carrier base timer	
x'3F8A'	NFCTR	-	-	NF1CKS1	NF1CKS0	NF1EN	NF0CKS1	NF0CKS0	NF0EN	III - 35
		-	-	0	0	0	0	0	0	
				IRQ1 noise filter sampling period		IRQ1 noise filter setup	IRQ0 noise filter sampling period		IRQ0 noise filter setup	
x'3F90'	ANCTR0	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	ANCHS2	ANCHS1	ANCHS0	XIII - 5
		x	x	x	x	0	x	x	x	
		A/D sample and hpld time		A/D conversion clock		A/D ladder resistance control	Analog input selection			
x'3F91'	ANCTR1	ANST	-	-	-	-	-	-	-	XIII - 6
		0	-	-	-	-	-	-	-	
		A/D conversion status								
x'3F92'	ANBUF0	ANBUF04	ANBUF06	-	-	-	-	-	-	XIII - 7
		x	x	-	-	-	-	-	-	
		A/D buffer 0 (lower 2 bits)								
x'3F93'	ANBUF1	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10	XIII - 7
		x	x	x	x	x	x	x	x	
		A/D buffer 1 (upper 8 bits)								
x'3FB0' to x'3FC9'	LCXXBUF	Buffer for LCD display								XII - 9
x'3FCC'	LCCTR	-	SEGSEL6	SEGSEL5	SEGSEL4	SEGSEL3	SEGSEL2	SEGSEL1	SEGSEL0	IV - 26, 31, 38, 42 XII - 8
		-	0	0	0	0	0	0	0	
			SEG26 to SEG29 / Port 80 to 83 selection	SEG30 to SEG33 / Port 83 to 87 selection	SEG37 to SEG34 / Port 74 to 77 selection	SEG41 to SEG38 / Port 70 to 73 selection	SEG45 to SEG42 / Port 64 to 67 selection	SEG49 to SEG46 / Port 60 to 63 selection	SEG51 to SEG50 / Port 53 to 54 selection	
x'3FCD'	LCMD	LCDEN	Reserved	LCDDTY1	LCDDTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0	XII - 6
		0	0	0	0	0	0	0	0	
		LCD drivers enable	Set always "0"	LCD display duty		LCD clock source				
x'3FE0'	Do not set	-	-	-	-	-	-	-	-	
		-	-	-	-	-	-	-	-	
x'3FE1'	NMICR	-	-	-	-	-	PIR	WDIR	Reserved	III - 16
		-	-	-	-	-	0	0	0	
							Program interrupt request	Watchdog interrupt request	Set always "0"	
x'3FE2'	IRQ0ICR	IRQ0LV1	IRQ0LV0	REDG0	-	-	-	IRQ0IE	IRQ0IR	III - 17
		0	0	0	-	-	-	0	0	
		IRQ0 interrupt level		IRQ0 interrupt active edge				IRQ0 interrupt enable	IRQ0 interrupt request	
x'3FE3'	IRQ1ICR	IRQ1LV1	IRQ1LV0	REDG1	-	-	-	IRQ1IE	IRQ1IR	III - 18
		0	0	0	-	-	-	0	0	
		IRQ1 interrupt level		IRQ1 interrupt active edge				IRQ1 interrupt enable	IRQ1 interrupt request	

Note) x : Initial value is unstable - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
x'3FE6'	TM2ICR	TM2LV1	TM2LV0	-	-	-	-	TM2IE	TM2IR	III - 22
		0	0	-	-	-	-	0	0	
		TM2 interrupt level						TM2 interrupt enable	TM2 interrupt request	
x'3FE7'	TBICR	TBLV1	TBLV0	-	-	-	-	TBIE	TBIR	III - 26
		0	0	-	-	-	-	0	0	
		TB interrupt level						TB interrupt enable	TB interrupt request	
x'3FE8'	SC0ICR	SC0LV1	SC0LV0	-	-	-	-	SC0IE	SC0IR	III - 27
		0	0	-	-	-	-	0	0	
		SC0 interrupt level						SC0 interrupt enable	SC0 interrupt request	
x'3FEA'	ADICR	ADLV1	ADLV0	-	-	-	-	ADIE	ADIR	III - 29
		0	0	-	-	-	-	0	0	
		AD interrupt level						AD interrupt enable	AD interrupt request	
x'3FEB'	IRQ2ICR	IRQ2LV1	IRQ2LV0	REDG2	-	-	-	IRQ2IE	IRQ2IR	III - 19
		0	0	0	-	-	-	0	0	
		IRQ2 interrupt level		IRQ2 interrupt active edge				IRQ2 interrupt enable	IRQ2 interrupt request	
x'3FEC'	IRQ3ICR	IRQ3LV1	IRQ3LV0	REDG3	-	-	-	IRQ3IE	IRQ3IR	III - 20
		0	0	0	-	-	-	0	0	
		IRQ3 interrupt level		IRQ3 interrupt active edge				IRQ3 interrupt enable	IRQ3 interrupt request	
x'3FED'	IRQ4ICR	IRQ4LV1	IRQ4LV0	REDG4	-	-	-	IRQ4IE	IRQ4IR	III - 21
		0	0	0	-	-	-	0	0	
		IRQ4 interrupt level		IRQ4 interrupt active edge				IRQ4 interrupt enable	IRQ4 interrupt request	
x'3FEE'	TM3ICR	TM3LV1	TM3LV0	-	-	-	-	TM3IE	TM3IR	III - 23
		0	0	-	-	-	-	0	0	
		TM3 interrupt level						TM3 interrupt enable	TM3 interrupt request	
x'3FEF'	TM4ICR	TM4LV1	TM4LV0	-	-	-	-	TM4IE	TM4IR	III - 24
		0	0	-	-	-	-	0	0	
		TM4 interrupt level						TM4 interrupt enable	TM4 interrupt request	
x'3FF0'	TM5ICR	TM5LV1	TM5LV0	-	-	-	-	TM5IE	TM5IR	III - 25
		0	0	-	-	-	-	0	0	
		TM5 interrupt level						TM5 interrupt enable	TM5 interrupt request	
x'3FF1'	SC1ICR	SC1LV1	SC1LV0	-	-	-	-	SC1IE	SC1IR	III - 28
		0	0	-	-	-	-	0	0	
		SC1 interrupt level						SC1 interrupt enable	SC1 interrupt request	

Note) x : Initial value is unstable - : No data

14-4 Instruction Set

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Ext.	1	2	3	4	5	6	7	8	9	10	11	Notes	Page
Data Move Instructions																							
MOV	MOV Dn,Dm	Dn→Dm	--	--	--	--	2	1			1010	DnDm											25
	MOV imm8,Dm	imm8→Dm	--	--	--	--	4	2			1010	DmDm	<#8.	...>									25
	MOV Dn,PSW	Dn→PSW	●	●	●	●	3	3		0010	1001	01Dn											26
	MOV PSW,Dm	PSW→Dm	--	--	--	--	3	2		0010	0001	01Dm											26
	MOV (An),Dm	mem8(An)→Dm	--	--	--	--	2	2			0100	1ADm											27
	MOV (d8,An),Dm	mem8(d8+An)→Dm	--	--	--	--	4	2			0110	1ADm	<d8.	...>								*1	27
	MOV (d16,An),Dm	mem8(d16+An)→Dm	--	--	--	--	7	4		0010	0110	1ADm	<d16	....	....	...>							28
	MOV (d4,SP),Dm	mem8(d4+SP)→Dm	--	--	--	--	3	2			0110	01Dm	<d4>									*2	28
	MOV (d8,SP),Dm	mem8(d8+SP)→Dm	--	--	--	--	5	3		0010	0110	01Dm	<d8.	...>								*3	29
	MOV (d16,SP),Dm	mem8(d16+SP)→Dm	--	--	--	--	7	4		0010	0110	00Dm	<d16	....	....	...>							29
	MOV (io8),Dm	mem8(IOTOP+io8)→Dm	--	--	--	--	4	2			0110	00Dm	<io8	...>									30
	MOV (abs8),Dm	mem8(abs8)→Dm	--	--	--	--	4	2			0100	01Dm	<abs	8..>									30
	MOV (abs12),Dm	mem8(abs12)→Dm	--	--	--	--	5	2			0100	00Dm	<abs	12..	...>								31
	MOV (abs16),Dm	mem8(abs16)→Dm	--	--	--	--	7	4		0010	1100	00Dm	<abs	16..	....	...>							31
	MOV Dn,(Am)	Dn→mem8(Am)	--	--	--	--	2	2			0101	1aDn											32
	MOV Dn,(d8,Am)	Dn→mem8(d8+Am)	--	--	--	--	4	2			0111	1aDn	<d8.	...>								*1	32
	MOV Dn,(d16,Am)	Dn→mem8(d16+Am)	--	--	--	--	7	4		0010	0111	1aDn	<d16	....	....	...>							33
	MOV Dn,(d4,SP)	Dn→mem8(d4+SP)	--	--	--	--	3	2			0111	01Dn	<d4>									*2	33
	MOV Dn,(d8,SP)	Dn→mem8(d8+SP)	--	--	--	--	5	3		0010	0111	01Dn	<d8.	...>								*3	34
	MOV Dn,(d16,SP)	Dn→mem8(d16+SP)	--	--	--	--	7	4		0010	0111	00Dn	<d16	....	....	...>							34
	MOV Dn,(io8)	Dn→mem8(IOTOP+io8)	--	--	--	--	4	2			0111	00Dn	<io8	...>									35
	MOV Dn,(abs8)	Dn→mem8(abs8)	--	--	--	--	4	2			0101	01Dn	<abs	8..>									35
	MOV Dn,(abs12)	Dn→mem8(abs12)	--	--	--	--	5	2			0101	00Dn	<abs	12..	...>								36
	MOV Dn,(abs16)	Dn→mem8(abs16)	--	--	--	--	7	4		0010	1101	00Dn	<abs	16..	....	...>							36
	MOV imm8,(io8)	imm8→mem8(IOTOP+io8)	--	--	--	--	6	3			0000	0010	<io8	...>	<#8.	...>							37
	MOV imm8,(abs8)	imm8→mem8(abs8)	--	--	--	--	6	3			0001	0100	<abs	8..>	<#8.	...>							37
	MOV imm8,(abs12)	imm8→mem8(abs12)	--	--	--	--	7	3			0001	0101	<abs	12..	...>	<#8.	...>						38
	MOV imm8,(abs16)	imm8→mem8(abs16)	--	--	--	--	9	5		0011	1101	1001	<abs	16..	....	...>	<#8.	...>					38
	MOV Dn,(HA)	Dn→mem8(HA)	--	--	--	--	2	2			1101	00Dn											39
MOVW	MOVW (An),DWm	mem16(An)→DWm	--	--	--	--	2	3			1110	00Ad											40
	MOVW (An),Am	mem16(An)→Am	--	--	--	--	3	4		0010	1110	10Aa										*4	40
	MOVW (d4,SP),DWm	mem16(d4+SP)→DWm	--	--	--	--	3	3			1110	011d	<d4>									*2	41
	MOVW (d4,SP),Am	mem16(d4+SP)→Am	--	--	--	--	3	3			1110	010a	<d4>									*2	41
	MOVW (d8,SP),DWm	mem16(d8+SP)→DWm	--	--	--	--	5	4		0010	1110	011d	<d8.	...>								*3	42
	MOVW (d8,SP),Am	mem16(d8+SP)→Am	--	--	--	--	5	4		0010	1110	010a	<d8.	...>								*3	42
	MOVW (d16,SP),DWm	mem16(d16+SP)→DWm	--	--	--	--	7	5		0010	1110	001d	<d16	....	....	...>							43
	MOVW (d16,SP),Am	mem16(d16+SP)→Am	--	--	--	--	7	5		0010	1110	000a	<d16	....	....	...>							43
	MOVW (abs8),DWm	mem16(abs8)→DWm	--	--	--	--	4	3			1100	011d	<abs	8..>									44
	MOVW (abs8),Am	mem16(abs8)→Am	--	--	--	--	4	3			1100	010a	<abs	8..>									44
	MOVW (abs16),DWm	mem16(abs16)→DWm	--	--	--	--	7	5		0010	1100	011d	<abs	16..	....	...>							45
	MOVW (abs16),Am	mem16(abs16)→Am	--	--	--	--	7	5		0010	1100	010a	<abs	16..	....	...>							45
	MOVW DWn,(Am)	DWn→mem16(Am)	--	--	--	--	2	3			1111	00aD											46
	MOVW An,(Am)	An→mem16(Am)	--	--	--	--	3	4		0010	1111	10aA										*4	46
	MOVW DWn,(d4,SP)	DWn→mem16(d4+SP)	--	--	--	--	3	3			1111	011D	<d4>									*2	47
	MOVW An,(d4,SP)	An→mem16(d4+SP)	--	--	--	--	3	3			1111	010A	<d4>									*2	47
	MOVW DWn,(d8,SP)	DWn→mem16(d8+SP)	--	--	--	--	5	4		0010	1111	011D	<d8.	...>								*3	48
	MOVW An,(d8,SP)	An→mem16(d8+SP)	--	--	--	--	5	4		0010	1111	010A	<d8.	...>								*3	48
	MOVW DWn,(d16,SP)	DWn→mem16(d16+SP)	--	--	--	--	7	5		0010	1111	001D	<d16	....	....	...>							49
	MOVW An,(d16,SP)	An→mem16(d16+SP)	--	--	--	--	7	5		0010	1111	000A	<d16	....	....	...>							49
	MOVW DWn,(abs8)	DWn→mem16(abs8)	--	--	--	--	4	3			1101	011D	<abs	8..>									50
	MOVW An,(abs8)	An→mem16(abs8)	--	--	--	--	4	3			1101	010A	<abs	8..>									50
	MOVW DWn,(abs16)	DWn→mem16(abs16)	--	--	--	--	7	5		0010	1101	011D	<abs	16..	....	...>							51
	MOVW An,(abs16)	An→mem16(abs16)	--	--	--	--	7	5		0010	1101	010A	<abs	16..	....	...>							51
	MOVW DWn,(HA)	DWn→mem16(HA)	--	--	--	--	2	3			1001	010D											52
	MOVW An,(HA)	An→mem16(HA)	--	--	--	--	2	3			1001	011A											52
	MOVW imm8,DWm	sign(imm8)→DWm	--	--	--	--	4	2			0000	110d	<#8.	...>								*5	53
	MOVW imm8,Am	zero(imm8)→Am	--	--	--	--	4	2			0000	111a	<#8.	...>								*6	53
	MOVW imm16,DWm	imm16→DWm	--	--	--	--	6	3			1100	111d	<#16	....	....	...>							54

NOTE: Pages for the MN101C Series Instruction Manual

*1 d8 sign-extension
*2 d4 zero-extension
*3 d8 zero-extension
*4 A=An, a=Am
*5 #8 sign-extension
*6 #8 zero-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	exten-sion	Machine Code 1 2 3 4 5 6 7 8 9 10 11	Notes	Page
	MOVW imm16,Am	imm16→Am	--	--	--	--	6	3			1101 111a <#16 ....>		54
	MOVW SP,Am	SP→Am	--	--	--	--	3	3		0010	0000 100a		55
	MOVW An,SP	An→SP	--	--	--	--	3	3		0010	0000 101A		55
	MOVW DWn,DWm	DWn→DWm	--	--	--	--	3	3		0010	1000 00Dd	*1	56
	MOVW DWn,Am	DWn→Am	--	--	--	--	3	3		0010	0100 11Da		56
	MOVW An,DWm	An→DWm	--	--	--	--	3	3		0010	1100 11Ad		57
	MOVW An,Am	An→Am	--	--	--	--	3	3		0010	0000 00Aa	*2	57
PUSH	PUSH Dn	SP-1→SP,Dn→mem8(SP)	--	--	--	--	2	3			1111 10Dn		58
	PUSH An	SP-2→SP,An→mem16(SP)	--	--	--	--	2	5			0001 011A		58
POP	POP Dn	mem8(SP)→Dn,SP+1→SP	--	--	--	--	2	3			1110 10Dn		59
	POP An	mem16(SP)→An,SP+2→SP	--	--	--	--	2	4			0000 011A		59
EXT	EXT Dn,DWm	sign(Dn)→DWm	--	--	--	--	3	3		0010	1001 000d	*3	60
Arithmetic manupulation instructions													
ADD	ADD Dn,Dm	Dm+Dn→Dm	●	●	●	●	3	2		0011	0011 DnDm		61
	ADD imm4,Dm	Dm+sign(imm4)→Dm	●	●	●	●	3	2			1000 00Dm <#4>	*6	61
	ADD imm8,Dm	Dm+imm8→Dm	●	●	●	●	4	2			0000 10Dm <#8. ...>		62
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	●	●	●	●	3	2	○	0011	1011 DnDm		63
ADDW	ADDW DWn,DWm	DWm+DWn→DWm	●	●	●	●	3	3	○	0010	0101 00Dd	*1	64
	ADDW DWn,Am	Am+DWn→Am	●	●	●	●	3	3	○	0010	0101 10Da		64
	ADDW imm4,Am	Am+sign(imm4)→Am	●	●	●	●	3	2			1110 110a <#4>	*6	65
	ADDW imm8,Am	Am+sign(imm8)→Am	●	●	●	●	5	3		0010	1110 110a <#8. ...>	*7	65
	ADDW imm16,Am	Am+imm16→Am	●	●	●	●	7	4		0010	0101 011a <#16 ....>		66
	ADDW imm4,SP	SP+sign(imm4)→SP	--	--	--	--	3	2			1111 1101 <#4>	*6	66
	ADDW imm8,SP	SP+sign(imm8)→SP	--	--	--	--	4	2			1111 1100 <#8. ...>	*7	67
	ADDW imm16,SP	SP+imm16→SP	--	--	--	--	7	4		0010	1111 1100 <#16 ....>		67
	ADDW imm16,DWm	DWm+imm16→DWm	●	●	●	●	7	4		0010	0101 010d <#16 ....>		68
ADDUW	ADDUW Dn,Am	Am+zero(Dn)→Am	●	●	●	●	3	3	○	0010	1000 1aDn	*8	69
ADDSW	ADDSW Dn,Am	Am+sign(Dn)→Am	●	●	●	●	3	3	○	0010	1001 1aDn		70
SUB	SUB Dn,Dm(when Dn≠Dm)	Dm-Dn→Dm	●	●	●	●	3	2	○	0010	1010 DnDm		71
	SUB Dn,Dn	Dn-Dn→Dn	0	0	0	1	2	1			1000 01Dn		71
	SUB imm8,Dm	Dm-imm8→Dm	●	●	●	●	5	3		0010	1010 DmDm <#8. ...>		72
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	●	●	●	●	3	2	○	0010	1011 DnDm		73
SUBW	SUBW DWn,DWm	DWm-DWn→DWm	●	●	●	●	3	3		0010	0100 00Dd	*1	74
	SUBW DWn,Am	Am-DWn→Am	●	●	●	●	3	3		0010	0100 10Da		74
	SUBW imm16,DWm	DWm-imm16→DWm	●	●	●	●	7	4		0010	0100 010d <#16 ....>		75
	SUBW imm16,Am	Am-imm16→Am	●	●	●	●	7	4		0010	0100 011a <#16 ....>		75
MULU	MULU Dn,Dm	Dm*Dn→DWk	0	●	●	●	3	8		0010	1111 111D	*4	76
DIVU	DIVU Dn,DWm	DWm/Dn→DWm-l...DWm-h	●	●	●	●	3	9		0010	1110 111d	*5	77
CMP	CMP Dn,Dm	Dm-Dn...PSW	●	●	●	●	3	2		0011	0010 DnDm		78
	CMP imm8,Dm	Dm-imm8...PSW	●	●	●	●	4	2			1100 00Dm <#8. ...>		78
	CMP imm8,(abs8)	mem8(abs8)-imm8...PSW	●	●	●	●	6	3			0000 0100 <abs 8..> <#8. ...>		79
	CMP imm8,(abs12)	mem8(abs12)-imm8...PSW	●	●	●	●	7	3			0000 0101 <abs 12.. ...> <#8. ...>		79
	CMP imm8,(abs16)	mem8(abs16)-imm8...PSW	●	●	●	●	9	5		0011	1101 1000 <abs 16.. ....> <#8. ...>		80
CMPW	CMPW DWn,DWm	DWm-DWn...PSW	●	●	●	●	3	3		0010	1000 01Dd	*1	81
	CMPW DWn,Am	Am-DWn...PSW	●	●	●	●	3	3		0010	0101 11Da		81
	CMPW An,Am	Am-An...PSW	●	●	●	●	3	3		0010	0000 01Aa	*2	82
	CMPW imm16,DWm	DWm-imm16...PSW	●	●	●	●	6	3			1100 110d <#16 ....>		82
	CMPW imm16,Am	Am-imm16...PSW	●	●	●	●	6	3			1101 110a <#16 ....>		83
Logical manipulation instructions													
AND	AND Dn,Dm	Dm&Dn→Dm	0	●	0	●	3	2		0011	0111 DnDm		84
	AND imm8,Dm	Dm&imm8→Dm	0	●	0	●	4	2			0001 11Dm <#8. ...>		84
	AND imm8,PSW	PSW&imm8→PSW	●	●	●	●	5	3		0010	1001 0010 <#8. ...>		85
OR	OR Dn,Dm	DmIDn→Dm	0	●	0	●	3	2		0011	0110 DnDm		86
	OR imm8,Dm	DmIimm8→Dm	0	●	0	●	4	2			0001 10Dm <#8. ...>		86
	OR imm8,PSW	PSWIimm8→PSW	●	●	●	●	5	3		0010	1001 0011 <#8. ...>		87
XOR	XOR Dn,Dm	Dm^Dn→Dm	0	●	0	●	3	2		0011	1010 DnDm	*9	88
	XOR imm8,Dm	Dm^imm8→Dm	0	●	0	●	5	3		0011	1010 DmDm <#8. ...>		88

NOTE: Pages for MN101C Series Instruction Manual

*1 D=DWn, d=DWm
*2 A=An, a=Am
*3 d=DWm
*4 D=DWk
*5 D=DWm
*6 #4 sign-extension
*7 #8 sign-extension
*8 Dn zero extension
*9 m=n/

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	Re-peat	Exten sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes	Page
			VF	NF	CF	ZF																	
NOT	NOT Dn	¯Dn→Dn	0	●	0	●	3	2		0010	0010	10Dn											89
ASR	ASR Dn	Dn.msb→temp,Dn.lsb→CF Dn>>1→Dn,temp→Dn.msb	0	--	●	●	3	2	○	0010	0011	10Dn											90
LSR	LSR Dn	Dn.lsb→CF,Dn>>1→Dn 0→Dn.msb	0	0	●	●	3	2	○	0010	0011	11Dn											91
ROR	ROR Dn	Dn.lsb→temp,Dn>>1→Dn CF→Dn.msb,temp→CF	0	●	●	●	3	2	○	0010	0010	11Dn											92
Bit manipulation instructions																							
BSET	BSET (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 1→mem8(IOTOP+io8)bp	0	●	0	●	5	5		0011	1000	0bp.	<io8	...>									93
	BSET (abs8)bp	mem8(abs8)&bpdata...PSW 1→mem8(abs8)bp	0	●	0	●	4	4			1011	0bp.	<abs	8..>									93
	BSET (abs16)bp	mem8(abs16)&bpdata...PSW 1→mem8(abs16)bp	0	●	0	●	7	6		0011	1100	0bp.	<abs	16..	....	...>							94
BCLR	BCLR (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 0→mem8(IOTOP+io8)bp	0	●	0	●	5	5		0011	1000	1bp.	<io8	...>									95
	BCLR (abs8)bp	mem8(abs8)&bpdata...PSW 0→mem8(abs8)bp	0	●	0	●	4	4			1011	1bp.	<abs	8..>									95
	BCLR (abs16)bp	mem8(abs16)&bpdata...PSW 0→mem8(abs16)bp	0	●	0	●	7	6		0011	1100	1bp.	<abs	16..	....	...>							96
BTST	BTST imm8,Dm	Dm&imm8...PSW	0	●	0	●	5	3		0010	0000	11Dm	<#8.	...>									97
	BTST (abs16)bp	mem8(abs16)&bpdata...PSW	0	●	0	●	7	5		0011	1101	0bp.	<abs	16..	....	...>							97
Branch instructions																							
Bcc	BEQ label	if(ZF=1), PC+3+d4(label)+H→PC if(ZF=0), PC+3→PC	--	--	--	--	3	2/3			1001	000H	<d4>									*1	98
	BEQ label	if(ZF=1), PC+4+d7(label)+H→PC if(ZF=0), PC+4→PC	--	--	--	--	4	2/3			1000	1010	<d7.	...H								*2	98
	BEQ label	if(ZF=1), PC+5+d11(label)+H→PC if(ZF=0), PC+5→PC	--	--	--	--	5	2/3			1001	1010	<d11	....	...H							*3	99
	BNE label	if(ZF=0), PC+3+d4(label)+H→PC if(ZF=1), PC+3→PC	--	--	--	--	3	2/3			1001	001H	<d4>									1	100
	BNE label	if(ZF=0), PC+4+d7(label)+H→PC if(ZF=1), PC+4→PC	--	--	--	--	4	2/3			1000	1011	<d7.	...H								*2	100
	BNE label	if(ZF=0), PC+5+d11(label)+H→PC if(ZF=1), PC+5→PC	--	--	--	--	5	2/3			1001	1011	<d11	....	...H							*3	101
	BGE label	if((VF^NF)=0),PC+4+d7(label)+H→PC if((VF^NF)=1),PC+4→PC	--	--	--	--	4	2/3			1000	1000	<d7.	...H								*2	102
	BGE label	if((VF^NF)=0),PC+5+d11(label)+H→PC if((VF^NF)=1),PC+5→PC	--	--	--	--	5	2/3			1001	1000	<d11	....	...H							*3	102
	BCC label	if(CF=0),PC+4+d7(label)+H→PC if(CF=1), PC+4→PC	--	--	--	--	4	2/3			1000	1100	<d7.	...H								*2	103
	BCC label	if(CF=0), PC+5+d11(label)+H→PC if(CF=1), PC+5→PC	--	--	--	--	5	2/3			1001	1100	<d11	....	...H							*3	103
	BCS label	if(CF=1),PC+4+d7(label)+H→PC if(CF=0), PC+4→PC	--	--	--	--	4	2/3			1000	1101	<d7.	...H								*2	104
	BCS label	if(CF=1), PC+5+d11(label)+H→PC if(CF=0), PC+5→PC	--	--	--	--	5	2/3			1001	1101	<d11	....	...H							*3	104
	BLT label	if((VF^NF)=1),PC+4+d7(label)+H→PC if((VF^NF)=0),PC+4→PC	--	--	--	--	4	2/3			1000	1110	<d7.	...H								*2	105
	BLT label	if((VF^NF)=1),PC+5+d11(label)+H→PC if((VF^NF)=0),PC+5→PC	--	--	--	--	5	2/3			1001	1110	<d11	....	...H							*3	105
	BLE label	if((VF^NF)|ZF=1),PC+4+d7(label)+H→PC if((VF^NF)|ZF=0),PC+4→PC	--	--	--	--	4	2/3			1000	1111	<d7.	...H								*2	106
	BLE label	if((VF^NF)|ZF=1),PC+5+d11(label)+H→PC if((VF^NF)|ZF=0),PC+5→PC	--	--	--	--	5	2/3			1001	1111	<d11	....	...H							*3	106
	BGT label	if((VF^NF)|ZF=0),PC+5+d7(label)+H→PC if((VF^NF)|ZF=1),PC+5→PC	--	--	--	--	5	3/4		0010	0010	0001	<d7.	...H								*2	107

NOTE: Pages for MN101C Series Instruction Manual

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

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Group	Mnemonic	Operation	Flag				Code Size	Cycle	Re-peat	Exten-sion	Machine Code											Notes	Page
			VF	NF	CF	ZF					1	2	3	4	5	6	7	8	9	10	11		
Bcc	BGT label	if((VF^NF)|ZF=0),PC+6+d11(label)+H→PC if((VF^NF)|ZF=1),PC+6→PC	--	--	--	--	6	3/4		0010	0011	0001	<d11	....	...H							*3	107
	BHI label	if(CFIZF=0),PC+5+d7(label)+H→PC if(CFIZF=1), PC+5→PC	--	--	--	--	5	3/4		0010	0010	0010	<d7.	...H								*2	108
	BHI label	if(CFIZF=0),PC+6+d11(label)+H→PC if(CFIZF=1), PC+6→PC	--	--	--	--	6	3/4		0010	0011	0010	<d11	....	...H							*3	108
	BLS label	if(CFIZF=1),PC+5+d7(label)+H→PC if(CFIZF=0), PC+5→PC	--	--	--	--	5	3/4		0010	0010	0011	<d7.	...H								*2	109
	BLS label	if(CFIZF=1),PC+6+d11(label)+H→PC if(CFIZF=0), PC+6→PC	--	--	--	--	6	3/4		0010	0011	0011	<d11	....	...H							*3	109
	BNC label	if(NF=0),PC+5+d7(label)+H→PC if(NF=1),PC+5→PC	--	--	--	--	5	3/4		0010	0010	0100	<d7.	...H								*2	110
	BNC label	if(NF=0),PC+6+d11(label)+H→PC if(NF=1),PC+6→PC	--	--	--	--	6	3/4		0010	0011	0100	<d11	....	...H							*3	110
	BNS label	if(NF=1),PC+5+d7(label)+H→PC if(NF=0),PC+5→PC	--	--	--	--	5	3/4		0010	0010	0101	<d7.	...H								*2	111
	BNS label	if(NF=1),PC+6+d11(label)+H→PC if(NF=0),PC+6→PC	--	--	--	--	6	3/4		0010	0011	0101	<d11	....	...H							*3	111
	BVC label	if(VF=0),PC+5+d7(label)+H→PC if(VF=1),PC+5→PC	--	--	--	--	5	3/4		0010	0010	0110	<d7.	...H								*2	112
	BVC label	if(VF=0),PC+6+d11(label)+H→PC if(VF=1),PC+6→PC	--	--	--	--	6	3/4		0010	0011	0110	<d11	....	...H							*3	112
	BVS label	if(VF=1),PC+5+d7(label)+H→PC if(VF=0),PC+5→PC	--	--	--	--	5	3/4		0010	0010	0111	<d7.	...H								*2	113
	BVS label	if(VF=1),PC+6+d11(label)+H→PC if(VF=0),PC+6→PC	--	--	--	--	6	3/4		0010	0011	0111	<d11	....	...H							*3	113
	BRA label	PC+3+d4(label)+H→PC	--	--	--	--	3	3			1110	111H	<d4>									*1	114
	BRA label	PC+4+d7(label)+H→PC	--	--	--	--	4	3			1000	1001	<d7.	...H								*2	114
	BRA label	PC+5+d11(label)+H→PC	--	--	--	--	5	3			1001	1001	<d11	....	...H							*3	115
CBEQ	CBEQ imm8,Dm,label	if(Dm=imm8),PC+6+d7(label)+H→PC if(Dm≠imm8),PC+6→PC	●	●	●	●	6	3/4			1100	10Dm	<#8.	...>	<d7.	...H						*2	116
	CBEQ imm8,Dm,label	if(Dm=imm8),PC+8+d11(label)+H→PC if(Dm≠imm8),PC+8→PC	●	●	●	●	8	4/5		0010	1100	10Dm	<#8.	...>	<d11	....	...H					*3	116
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+9+d7(label)+H→PC if(mem8(abs8)≠imm8),PC+9→PC	●	●	●	●	9	6/7		0010	1101	1100	<abs	8..>	<#8.	...>	<d7.	...H				*2	117
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+10+d11(label)+H→PC if(mem8(abs8)≠imm8),PC+10→PC	●	●	●	●	10	6/7		0010	1101	1101	<abs	8..>	<#8.	...>	<d11	....	...H			*3	117
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+11+d7(label)+H→PC if(mem8(abs16)≠imm8),PC+11→PC	●	●	●	●	11	7/8		0011	1101	1100	<abs	16..	....	...>	<#8.	...>	<d7.	...H		*2	118
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+12+d11(label)+H→PC if(mem8(abs16)≠imm8),PC+12→PC	●	●	●	●	12	7/8		0011	1101	1101	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3	118
CBNE	CBNE imm8,Dm,label	if(Dm≠imm8),PC+6+d7(label)+H→PC if(Dm=imm8),PC+6→PC	●	●	●	●	6	3/4			1101	10Dm	<#8.	...>	<d7.	..H>						*2	119
	CBNE imm8,Dm,label	if(Dm≠imm8),PC+8+d11(label)+H→PC if(Dm=imm8),PC+8→PC	●	●	●	●	8	4/5		0010	1101	10Dm	<#8.	...>	<d11	....	...H					*3	119
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+9+d7(label)+H→PC if(mem8(abs8)=imm8),PC+9→PC	●	●	●	●	9	6/7		0010	1101	1110	<abs	8..>	<#8.	...>	<d7.	...H				*2	120
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+10+d11(label)+H→PC if(mem8(abs8)=imm8),PC+10→PC	●	●	●	●	10	6/7		0010	1101	1111	<abs	8..>	<#8.	...>	<d11	....	...H			*3	120
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+11+d7(label)+H→PC if(mem8(abs16)=imm8),PC+11→PC	●	●	●	●	11	7/8		0011	1101	1110	<abs	16..	....	...>	<#8.	...>	<d7.	...H		*2	121
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+12+d11(label)+H→PC if(mem8(abs16)=imm8),PC+12→PC	●	●	●	●	12	7/8		0011	1101	1111	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3	121
TBZ	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+7+d7(label)+H→PC if(mem8(abs8)bp=1),PC+7→PC	0	●	0	●	7	6/7		0011	0000	0bp.	<abs	8..>	<d7.	...H						*2	122
	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+8+d11(label)+H→PC if(mem8(abs8)bp=1),PC+8→PC	0	●	0	●	8	6/7		0011	0000	1bp.	<abs	8..>	<d11	....	...H					*3	122

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes	Page
TBZ	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+7+d7(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+7→PC	0	●	0	●	7	6/7		0011	0100	0bp.	<io8	...>	<d7.	...H						*1	123
	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+8+d11(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+8→PC	0	●	0	●	8	6/7		0011	0100	1bp.	<io8	...>	<d11	....	...H					*2	123
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+9+d7(label)+H→PC if(mem8(abs16)bp=1),PC+9→PC	0	●	0	●	9	7/8		0011	1110	0bp.	<abs	16..	....	...>	<d7.	...H				*1	124
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+10+d11(label)+H→PC if(mem8(abs16)bp=1),PC+10→PC	0	●	0	●	10	7/8		0011	1110	1bp.	<abs	16..	....	...>	<d11	....	...H			*2	124
TBNZ	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+7+d7(label)+H→PC if(mem8(abs8)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011	0001	0bp.	<abs	8..>	<d7.	...H						*1	125
	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+8+d11(label)+H→PC if(mem8(abs8)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011	0001	1bp.	<abs	8..>	<d11	....	...H					*2	125
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+7+d7(label)+H→PC if(mem8(io)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011	0101	0bp.	<io8	...>	<d7.	...H						*1	126
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+8+d11(label)+H→PC if(mem8(io)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011	0101	1bp.	<io8	...>	<d11	....	...H					*2	126
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+9+d7(label)+H→PC if(mem8(abs16)bp=0),PC+9→PC	0	●	0	●	9	7/8		0011	1111	0bp.	<abs	16..	....	...>	<d7.	...H				*1	127
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+10+d11(label)+H→PC if(mem8(abs16)bp=0),PC+10→PC	0	●	0	●	10	7/8		0011	1111	1bp.	<abs	16..	....	...>	<d11	....	...H			*2	127
JMP	JMP (An)	0→PC.17-16,An→PC.15-0,0→PC.H	---	---	---	---	3	4		0010	0001	00A0											128
	JMP label	abs18(label)+H→PC	---	---	---	---	7	5		0011	1001	0aaH	<abs	18.b	p15~	0..>						*5	128
JSR	JSR (An)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+3).bp17-16→mem8(SP+2).bp1-0 0→PC.bp17-16 An→PC.bp15-0,0→PC.H	---	---	---	---	3	7		0010	0001	00A1											129
	JSR label	SP-3→SP,(PC+5).bp7-0→mem8(SP) (PC+5).bp15-8→mem8(SP+1) (PC+5).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+5).bp17-16→mem8(SP+2).bp1-0 PC+5+d12(label)+H→PC	---	---	---	---	5	6			0001	000H	<d12	....	...>							*3	129
	JSR label	SP-3→SP,(PC+6).bp7-0→mem8(SP) (PC+6).bp15-8→mem8(SP+1) (PC+6).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+6).bp17-16→mem8(SP+2).bp1-0 PC+6+d16(label)+H→PC	---	---	---	---	6	7			0001	001H	<d16	....	....	...>						*4	130
	JSR label	SP-3→SP,(PC+7).bp7-0→mem8(SP) (PC+7).bp15-8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+7).bp17-16→mem8(SP+2).bp1-0 abs18(label)+H→PC	---	---	---	---	7	8		0011	1001	1aaH	<abs	18.b	p15~	0..>						*5	130
	JSRV (tbl4)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7 0→mem8(SP+2).bp6-2, (PC+3).bp17-16→mem8(SP+2).bp1-0 mem8(x'004080+tbl4<<2)→PC.bp7-0 mem8(x'004080+tbl4<<2+1)→PC.bp15-8 mem8(x'004080+tbl4<<2+2).bp7→PC.H mem8(x'004080+tbl4<<2+2).bp1-0→ PC.bp17-16	---	---	---	---	3	9			1111	1110	<t4>										131
NOP	NOP	PC+2→PC	---	---	---	---	2	1	○		0000	0000											132

NOTE: Pages for MN101C Series Instruction Manual.

*1 d7 sign-extension
*2 d11 sign-extension
*3 d12 sign-extension
*4 d16 sign-extension
*5 aa=abs18.17 - 16

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes	Page
RTS	RTS	mem8(SP)→(PC).bp7-0 mem8(SP+1)→(PC).bp15-8 mem8(SP+2).bp7→(PC).H mem8(SP+2).bp1-0→(PC).bp17-16 SP+3→SP	---	---	---	---	2	7			0000	0001											133
RTI	RTI	mem8(SP)→PSW mem8(SP+1)→(PC).bp7-0 mem8(SP+2)→(PC).bp15-8 mem8(SP+3).bp7→(PC).H mem8(SP+3).bp1-0→(PC).bp17-16 mem8(SP+4)→HA-l mem8(SP+5)→HA-h SP+6→SP	●	●	●	●	2	11			0000	0011											134
Contorl instructions																							
REP	REP imm3	imm3-1→RPC	---	---	---	---	3	2		0010	0001	1rep										*1	135

NOTE: Pages for MN101C Series Instruction Manual.

*1 no repeat whn imm3=0, (rep: imm3-1)

Other than the instruction of MN101C Series,the assembler of this Series has the following instructions as macro instructions.
The assembler will interpret the macro instructions below as the assembler instructions.

macro instructions	replaced instructions	remarks
INC Dn	ADD 1,Dn	
DEC Dn	ADD -1,Dn	
INC An	ADDW 1,An	
DEC An	ADDW -1,An	
INC2 An	ADDW 2,An	
DEC2 An	ADDW -2,An	
CLR Dn	SUB Dn,Dm	n=m
ASL D	ADD Dn,Dm	n=m
ROL Dn	ADDC Dn,Dm	n=m
NEG Dn	NOT Dn ADD 1,Dn	
NOPL	MOVW DWn,DWm	n=m
MOV (SP),Dn	MOV (0,SP),Dn	
MOV Dn,(SP)	MOV Dn,(0,SP)	
MOVW (SP),DWn	MOVW (0,SP),DWn	
MOVW DWn,(SP)	MOVW DWn,(0,SP)	
MOVW (SP),An	MOVW (0,SP),An	
MOVW An,(SP)	MOVW An,(0,SP)	

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14-5 Instruction Map

MN101C SERIES INSTRUCTION MAP

1st nibble\2nd nibble	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	RTS	MOV #8,(io8)	RTI	CMP #8,(abs8)/(abs12)		POP An		ADD #8,Dm				MOVW #8,DWm		MOVW #8,Am	
1	JSR d12(label)		JSR d16(label)		MOV #8,(abs8)/(abs12)		PUSH An		OR #8,Dm				AND #8,Dm			
2	When the exension code is b'oo10'															
3	When the extension code is b'0011'															
4	MOV (abs12),Dm				MOV (abs8),Dm				MOV (An),Dm							
5	MOV Dn,(abs12)				MOV Dn,(abs8)				MOV Dn,(Am)							
6	MOV (io8),Dm				MOV (d4,SP),Dm				MOV (d8,An),Dm							
7	MOV Dn,(io8)				MOV Dn,(d4,SP)				MOV Dn,(d8,Am)							
8	ADD #4,Dm				SUB Dn,Dn				BGE d7	BRA d7	BEQ d7	BNE d7	BCC d7	BCS d7	BLT d7	BLE d7
9	BEQ d4		BNE d4		MOVW DWn,(HA)		MOVW An,(HA)		BGE d11	BRA d11	BEQ d11	BNE d11	BCC d11	BCS d11	BLT d11	BLE d11
A	MOV Dn,Dm / MOV #8,Dm															
B	BSET (abs8)bp								BCLR (abs8)bp							
C	CMP #8,Dm				MOVW (abs8),Am		MOVW (abs8),DWm		CBEQ #8,Dm,d7				CMPW #16,DWm		MOVW #16,DWm	
D	MOV Dn,(HA)				MOVW An,(abs8)		MOVW DWn,(abs8)		CBNE #8,Dm,d7				CMPW #16,Am		MOVW #16,Am	
E	MOVW (An),DWm				MOVW (d4,SP),Am		MOVW (d4,SP),DWm		POP Dn				ADDW #4,Am		BRA d4	
F	MOVW DWn,(Am)				MOVW An,(d4,SP)		MOVW DWn,(d4,SP)		PUSH Dn				ADDW #8,SP	ADDW #4,SP	JSRV (tbl4)	

Extension code: b'0010'

2nd nible\3rd nibble	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOVW An,Am				CMPW An,Am				MOVW SP,Am		MOVW An,SP		BTST #8,Dm			
1	JMP (A0)	JSR (A0)	JMP (A1)	JSR (A1)	MOV PSW,Dm				REP #3							
2		BGT d7	BHI d7	BLS d7	BNC d7	BNS d7	BVC d7	BVS d7	NOT Dn				ROR Dn			
3		BGT d11	BHI d11	BLS d11	BNC d11	BNS d11	BVC d11	BVS d11	ASR Dn				LSR Dn			
4	SUBW DWn,DWm				SUBW #16,DWm		SUBW #16,Am		SUBW DWn,Am				MOVW DWn,Am			
5	ADDW DWn,DWm				ADDW #16,DWm		ADDW #16,Am		ADDW DWn,Am				CMPW DWn,Am			
6	MOV (d16,SP),Dm				MOV (d8,SP),Dm				MOV (d16,An),Dm							
7	MOV Dn,(d16,SP)				MOV Dn,(d8,SP)				MOV Dn,(d16,Am)							
8	MOVW DWn,DWm (NOPL @n=m)				CMPW DWn,DWm				ADDUW Dn,Am							
9	EXT Dn,DWm		AND #8,PSW	OR #8,PSW	MOV Dn,PSW				ADDSW Dn,Am							
A	SUB Dn,Dm / SUB #8,Dm															
B	SUBC Dn,Dm															
C	MOV (abs16),Dm				MOVW (abs16),Am		MOVW (abs16),DWm		CBEQ #8,Dm,d12				MOVW An,DWm			
D	MOV Dn,(abs16)				MOVW An,(abs16)		MOVW DWn,(abs16)		CBNE #8,Dm,d12				CBEQ #8,(abs8),d7/d11		CBNE #8,(abs8),d7/d11	
E	MOVW (d16,SP),Am		MOVW (d16,SP),DWm		MOVW (d8,SP),Am		MOVW (d8,SP),DWm		MOVW (An),Am				ADDW #8,Am		DIVU	
F	MOVW An,(d16,SP)		MOVW DWn,(d16,SP)		MOVW An,(d8,SP)		MOVW DWn,(d8,SP)		MOVW An,(Am)				ADDW #16,SP		MULU	

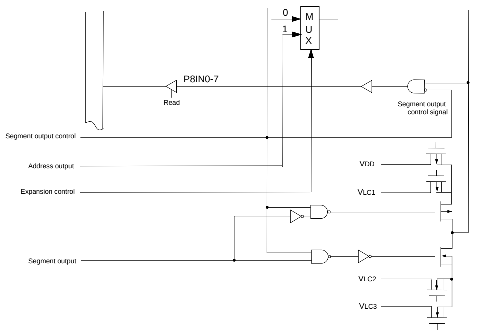
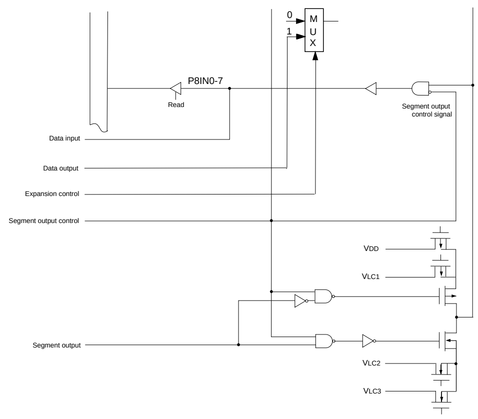
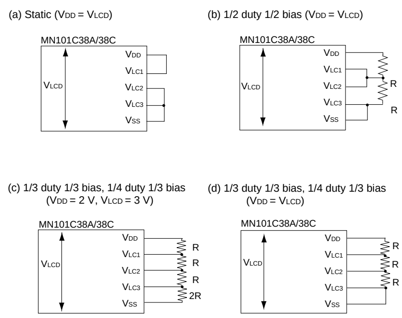
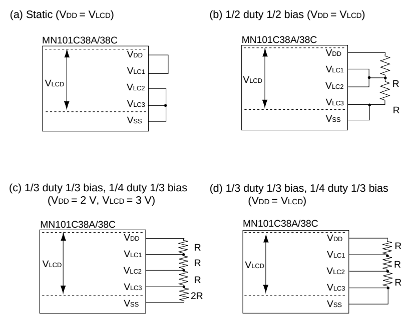
Extension code: b'0011'

<table>
<tr><th>2nd nibble\ 3rd nibble</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>F</th></tr>
<tr><td>0</td><td colspan="8">TBZ (abs8)bp,d7</td><td colspan="8">TBZ (abs8)bp,d11</td></tr>
<tr><td>1</td><td colspan="8">TBNZ (abs8)bp,d7</td><td colspan="8">TBNZ (abs8)bp,d11</td></tr>
<tr><td>2</td><td colspan="16">CMP Dn,Dm</td></tr>
<tr><td>3</td><td colspan="16">ADD Dn,Dm</td></tr>
<tr><td>4</td><td colspan="8">TBZ (io8)bp,d7</td><td colspan="8">TBZ (io8)bp,d11</td></tr>
<tr><td>5</td><td colspan="8">TBNZ (io8)bp,d7</td><td colspan="8">TBNZ (io8)bp,d11</td></tr>
<tr><td>6</td><td colspan="16">OR Dn,Dm</td></tr>
<tr><td>7</td><td colspan="16">AND Dn,Dm</td></tr>
<tr><td>8</td><td colspan="8">BSET (io8)bp</td><td colspan="8">BCLR (io8)bp</td></tr>
<tr><td>9</td><td colspan="8">JMP abs18(label)</td><td colspan="8">JSR abs18(label)</td></tr>
<tr><td>A</td><td colspan="16">XOR Dn,Dm / XOR #8,Dm</td></tr>
<tr><td>B</td><td colspan="16">ADDC Dn,Dm</td></tr>
<tr><td>C</td><td colspan="8">BSET (abs16)bp</td><td colspan="8">BCLR (abs16)bp</td></tr>
<tr><td>D</td><td colspan="8">BTST (abs16)bp</td><td>cmp #8,(abs16)</td><td>mov #8,(abs16)</td><td colspan="2"></td><td colspan="2">CBEQ #8,(abs16),d7/11</td><td colspan="2">CBNE #8,(abs16),d7/11</td></tr>
<tr><td>E</td><td colspan="8">TBZ (abs16)bp,d7</td><td colspan="8">TBZ (abs16)bp,d11</td></tr>
<tr><td>F</td><td colspan="8">TBNZ (abs16)bp,d7</td><td colspan="8">TBNZ (abs16)bp,d11</td></tr>
</table>

Ver2.1(2001.03.26)

MN101C38A/38C LSI User's Manual   Record of Changes

Diferrences between Version2.41 and 2nd Edition 5th Printing (1/2)

Page	Line	Definition	Details of Changes: Previous Edition (Ver.2.41)	Details of Changes: New Edition (Ver.2.5)
I - 11	Table 1-3-3	Change	If a capacitor is to be inserted between NRST and VDD...	If a capacitor is to be inserted between NRST and VSS...
I - 15	Table 1-3-6	Change	Discription of BUZZER	
I - 25	30	Change	Pull-up resistor ON	Pull-up resistor built-in
I - 35	2	Change	only for output	output and LCD output
	3	Change	only for output	output and LCD output
	Figure 1-8-1	Change	only for output	output and LCD output
III - 3	Table 3-1-1	Change	Vector number 2 to 18 Table address x'04008' to x'04048'	Vector number 2 to 20 Table address x'04008' to x'04050'
IV - 3	-	Add	-	Discription of calculation of resistor
IV - 43	Figure 4-9-3	Change		
IV - 49	3	Delete	timer 1 interrupt	-
		Change	timer 7 interrupt signal	timer 4 interrupt signal
V - 9	Figure 5-2-7	Change	TM0RM RMBTMS	Reserved Reserved
V - 10	Table 5-3-1	Delete	fs/64 6.4 ms - -	-
XII - 11	Table 11-3-1	Add		VLCD: LCD panel driver voltage...
	Figure 12-3-1	Change		

Diferrences between Version2.41 and 2nd Edition 5th Printing (2/2)

Page	Line	Definition	Details of Changes	
			Previous Edition (Ver.2.41)	New Edition (Ver.2.5)
XII - 23	1	Change	1/2 Duty	1/3 Duty
XII - 27	1	Change	1/2 Duty	1/4 Duty
XIV - 7	4	Delete	Please contact one of our sales offices...	-
XIV - 8	21	Delete	Please contact one of our sales offices...	-
XIV - 16	7	Change	SC0IMO	SC0IOM

Diferrences between 2nd Edition 4th Printing and Version2.41

Page	Line	Definition	Details of Changes	
			Previous Edition (Ver.2.4)	New Edition (Ver.2.41)
Cover	Pub No.	Change	21438-024E	21438-0241E
Colophon	-	Change	September, 2001 2nd Edition 4th Printing	October, 2001 Ver2.41
Sales office	-	Change		Latest version

<Note>

The list of our overseas sales offices has been updated.

Although the updated version (Ver2.41) is higher than the previous version (Ver2.4), the contents of the manual itself remains the same. The English version of the manual (Ver2.41) is the exact translation of the Japanese version of the same manual (Ver2.41).

Diferrences between 2nd Edition 3rd Printing and 2nd Edition 4th Printing

Page	Line	Definition	Details of Changes	
			Previous Edition (Ver.2.3)	New Edition (Ver.2.4)
I - 3	17	Change	64 KB	48 KB *3
	20	Change	64 KB	48 KB *3
	25	Add	-	*3 1 byte of internal ROM is reserved for ROM option. [☞ Chapter 1. 1-6-1 ROM Option]
II - 14	Figure 2-2-2	Change	96 KB	48 KB

Diferrences between 1st Edition 3rd Printing and 2nd Edition 3rd Printing

Page	Line	Definition	Details of Changes	
			Previous Edition (Ver.1.3)	New Edition (Ver.2.3)
Cover	-	Change	MN101C00	MN101C
Warning	-	Change	If you have any inquiries or questions about this book or our semiconductors, please contact one of our sales offices listed at the back of this book or Matsushita Electronics Corporation's Sales Department.	If you have any inquiries or questions about this book or our semiconductors, please contact one of our sales offices listed at the back of this book.
All Chapters	-	Change	-	Spellings and sentences.
All Chapters	-	Add	-	LSI manual of MN101C series is added. Setup examples of how to operate each functional block are also given.
I - 12	Table 1-3-4	Change	NRST pull-up resistor (Typ.50 kΩ)	pull-up resistor (Typ.35 kΩ)
Instruction Set All Pages	Title	Change	MN101C00 SERIES INDTRUCTION SET	MN101C SERIES INDTRUCTION SET
Instruction Set the 6th Page	-	Add	-	macro instructions
Instruction Map the 1st Page	Title	Change	MN101C00 SERIES INDTRUCTION MAP	MN101C SERIES INDTRUCTION MAP
Colophon	-	Delete	Matsushita Electronics Corporation	-
			© Matsushita Electronics Corporation	-

MN101C38A/38CLSI User's Manual Record of Changes (1st Edition 2nd Printing to 1st Edition 3rd Printing)

Page	Line		Details of Changes New Edition (1st Edition 3rd Printing)
-	-		Information about MN101CP38A• is deleted.

Differences between 1st Edition 1st Printing and 1st Edition 2nd Printing

<table>
<tr><th>Page</th><th>Line</th><th>1st Edition 1st Printing</th><th>1st Edition 2nd Printing</th></tr>
<tr><td>I-15</td><td></td><td><In the table of Operating conditions>
19 / Internal feedback resistor / Rating / TYP
4.0</td><td>4.5</td></tr>
<tr><td>I-24</td><td></td><td></td><td>Table 1-6-1 ROM Option Adddress<table><tr><th>Model</th><th>ROM Option Address</th></tr><tr><td>MN101C38A</td><td>X'0FFFF'</td></tr><tr><td>MN101C38C</td><td>X'0FFFF'</td></tr><tr><td>MN101CP38A</td><td>X'0FFFF'</td></tr><tr><td>MN101CP38C</td><td>X'0FFFF'</td></tr></table></td></tr>
<tr><td></td><td></td><td>After a reset, connect oscillator pins to both side, whichever an oscillator mode is.</td><td>After a reset, connect oscillator pins to the high speed oscillation input, too, even if the slow mode is selected.

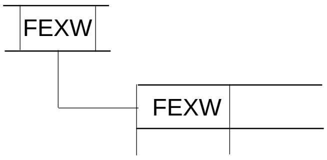
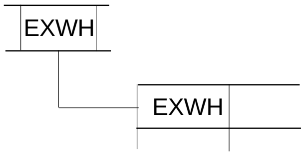
The WDMD (bp5) should be always set to "1". If it is set to "0", that operation cannot be stopped after the watchdog timer is generated.</td></tr>
<tr><td>I-25</td><td></td><td></td><td>Contents of mask option are subject to change. When placing an order for masks, please request the most recent option list from the sales office.</td></tr>
<tr><td>IX-9</td><td>2</td><td>In the MN101C38X microcomputer EPROM versions (MN101CP38A, MN101CP38C, etc.), <u>bits 2 to 0 at the highest address (See table below.)</u> in the internal EPROM specify the oscillator speed (SLOW or NORMAL)¥ ¥ ¥ ¥</td><td>In the MN101C38X microcomputer EPROM versions (MN101CP38A, MN101CP38C, etc.), <u>bits 2 to 0 at address X'0FFFF'</u> in the internal EPROM specify the oscillator speed (SLOW or NORMAL)¥ ¥ ¥ ¥</td></tr>
<tr><td></td><td></td><td>■ ROM Option Bits
Figure 9-1-2 ROM Option Bits</td><td>Figure 9-1-2 ROM Option Bits <u>(address:X'0FFFF')</u></td></tr>
<tr><td></td><td></td><td></td><td><table><tr><th>Model</th><th>EPROM Option Address</th></tr><tr><td>MN101CP38A</td><td>X'0FFFF'</td></tr><tr><td>MN101CP38C</td><td>X'0FFFF'</td></tr></table></td></tr>
<tr><td></td><td></td><td></td><td>After a reset, connect oscillator pins to the high speed oscillation input, too, even if the slow mode is selected.

The WDMD (bp5) should be always set to "1". If it is set to "0", that operation cannot be stopped after the watchdog timer is generated.</td></tr>
<tr><td>IX-11</td><td>1 to 6</td><td>9-2 PRB101C16/38-C/D Probe Switches</td><td>9-2 PRB-ADP101C16/38 Probe Switches
(The description of summary was changed.)</td></tr>
</table>

Differences between 1st Edition and 1st Edition 1st Printing (1/3)

Page	Line	1st Edition	1st Edition 1st Printing
		<Title of Chapter 2> Basic CPU	CPU Basics
I-20		Parameter / Symbol / Conditions Input pin 4 P21 (when used as SENS) 62 / Input high voltage 1 / V_{DDH}	Parameter / Symbol / Conditions Input pin 4 P21 (when used as SENS) *V_{DD}=5.0 V for P21 (SENS) 62 / Input high voltage 1 / V_{DDH}
II-2	11	2. Minimum execution time of one cycle	2. Minimum instruction execution time of one cycle
II-3		<Internal peripheral functions in the table> Includes peripheral functions (timer, serial, A/D converter, LCD control, etc.).	Includes peripheral functions (timer, serial interface, A/D converter, LCD control, etc.).
II-6	3	same time on its instruction execution, then • • • • •	same time on different instructions, then • • • • •
	31	LSB of program is bit indicates half byte.	The LSB of the program counter is used to indicate half byte instruction.
II-7	4		Those pointers are 2 bytes data.
	9	Ar reset, the value of SP is undefined.	At reset, the value of SP is undefined.
II-9	1-13	■ Zero Flag (ZF) The zero flag (ZF) is set when all the bits are '0' in the operation result. Otherwise, the zero flag is cleared. ■ Carry Flag (CF) The carry flag (CF) is set when a carry from or a borrow to the MSB occurs. The carry flag is cleared when no carry or borrow occurs. ■ Negative Flag (NF) The negative flag (NF) is set when the MSB is '1' and reset when the MSB is '0'. The negative flag is used to handle a signed value. ■ Overflow Flag (VF) The overflow flag (VF) is set when the arithmetic operation results overflow as a signed value. Otherwise, the overflow flag is cleared. The overflow flag is used to handle a signed value.	■ Zero Flag (ZF) Zero flag (ZF) is set to "1" when all bits are '0' in the operation result. Otherwise, zero flag is cleared to "0". ■ Carry Flag (CF) Carry flag (CF) is set to "1" when a carry from or a borrow to the MSB occurs. Carry flag is cleared to "0" when no carry or borrow occurs. ■ Negative Flag (NF) Negative flag (NF) is set to "1" when MSB is '1' and reset to "0" when MSB is '0'. Negative flag is used to handle a signed value. ■ Overflow Flag (VF) Overflow flag (VF) is set to "1" when the arithmetic operation results overflow as a signed value. Otherwise, overflow flag is cleared to "0". Overflow flag is used to handle a signed value.
II-10	3	Each addressing modes are uded for each instructions.	Each instruction uses a combination of the following addressing modes.
	13	Those addressing modes are well used for • • • •	These addressing modes are well used for • • • •
	16-17	Handy addressing is that reuses the last memory address accessed and is only available with the MOV and MOVW instructions.	Handy addressing reuses the last memory address accessed and is only available with MOV and MOVW instructions.

Differences between 1st Edition and 1st Edition 1st Printing (2/3)

Page	Line	1st Edition	1st Edition 1st Printing
II-16	8	peripheral circuits, and external interfaces respectively.	peripheral circuits and external interfaces respectively.
	13-16	Setting the external expansion bus to its memory expansion mode accesses external memory and other devices. The memory control register (MEMCTR) offers a choice of two access sequences: fixed wait cycle or handshake mode. Wait setting to peripheral expansion bus, connected to internal peripheral circuits is available.	In memory expansion mode, the external expansion bus can access external device. Memory control register (MEMCTR) can be used to select the access mode, fixed wait cycle mode or handshake mode. Wait cycle setting to peripheral expansion bus, connected to internal peripheral circuits is available.
II-17	1	Controll Registers	Control Registers
		<In fig. 2-3-2> 	 (Expressions of other words and sentences changed.)
II-18	5-11	After a reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles. Wait setting of IOW is the function, which CPU supports for special use, for example, when special function register or I/O is expanded to external. On this LSI, wait setting is not necessary, always. No-wait cycle should be selected with high quality system construction.	After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles. Wait setting of IOW is a function, which CPU supports for special use, for example, when special function register or I/O is expanded to external. For this LSI, wait cycle setting is not always necessary. Select "no-wait cycle" for high performance system construction.
			■ Expansion Address Control Register (EXADV)
			In memory expansion mode, unused address pins can be used as general ports.
II-19	5	field in the memory control register (MEMCTR).	field of the memory control register (MEMCTR).
	7	After a reset,	After reset,
	17-19	CPU of this LSI keeps waiting until receipt of deta acknowledge signals to ensure the time that external device can receive data with no error.	CPU of this LSI keeps waiting until the receiption of data acknowledge signal to ensure sufficient wait time so that external device can receive data with no error.
II-20	2	The RE or WE timing is determined based on OSC2.	The $\overline{RE}$ or $\overline{WE}$ timing is determined based on OSC2.
	5	Operation timing is same to the timing when a frequency rate is 2 • • • • •	Operation timing is same as the timing when the frequency rate is 2 • • • • •
	8	Access timing with 2 and 3 wait cycles • • • • •	Access timing with 2 or 3 wait cycles • • • • •
II-25		This stabilization interval is the same as that required after a reset, • • • • •	This stabilization time is the same as that required after a reset, • • • • •
II-27			After the instruction of the transition to HALT, STOP mode, NOP instruction should be executed 3 times.

Differences between 1st Edition and 1st Edition 1st Printing (3/3)

Page	Line	1st Edition	1st Edition 1st Printing
V-6	16	that the interrupt is generated after the transfer is complete.	that the interrupt is generated after the transmission is complete.
V-8	the last line	that the interrupt is generated after the transfer is complete.	that the interrupt is generated after the reception is complete.
V-14	4	that the interrupt by completing transfer is generated.	that the interrupt by completing transmission is generated.
V-16	26	that the interrupt by completing transfer is generated.	that the interrupt by completing reception is generated.

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Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

Nagaokakyo, Kyoto 617-8520, Japan
Tel: (075) 951-8151
http://www.panasonic.co.jp/semicon/

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