

## 1-1 Product Overview

### 1-1-1 Overview

The MN101C00 series of 8-bit single-chip microcomputers incorporate several types of peripheral functions. This chip series is well suited for VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, remote control, fax machine, musical instrument, and other applications.

The MN101C01D has an internal 64 KB of ROM and 2,048 bytes of RAM. Peripheral functions include six sets of timers, three sets of serial interfaces, an A/D converter, and remote control output. The configuration of this microcomputer is well suited for applications as a system controller in a VCR selection timer, CD player, MD, or portable terminal.

With two oscillation systems (max. 20 MHz/32 kHz) contained on the chip, the system clock can be switched between high and low speed. An automatic data transfer function (ATC) that is activated by interrupts, allows highly efficient interrupt processing.

When the oscillation source (fosc) is 8 MHz, a machine cycle lasts for 250 ns. When fosc is 20 MHz, a machine cycle is 100 ns. The package is a 80-pin QFS.

### 1-1-2 Product Summary

This manual describes the following models of the MN101C01 series. These products have identical functions.

Table 1-1-1 Product Summary

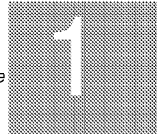
| Model      | ROM Size | RAM Size    | Classification   |
|------------|----------|-------------|------------------|
| MN101C01A* | 32 KB    | 1,536 bytes | Mask ROM version |
| MN101C01C  | 48 KB    | 2,048 bytes | Mask ROM version |
| MN101C01D  | 64 KB    | 2,048 bytes | Mask ROM version |
| MN101CP01D | 64 KB    | 2,048 bytes | EPROM version    |

\* Under development

## 1-2 Hardware Functions

|                 |   |
|-----------------|---|
| ROM/RAM Size:   | <p>&lt;Single chip mode&gt;</p> <p>Internal ROM*2 65,536×8-bit</p> <p>Internal RAM*2 2,048×8-bit</p> <p>&lt;Memory expansion mode&gt;</p> <p>Internal ROM*2 65,536×8-bit</p> <p>Internal RAM*2 2,048×8-bit</p> <p>External ROM 128K×8-bit</p> <p>External RAM 4K×8-bit</p> <p>&lt;Processor mode&gt;</p> <p>Internal ROM Unused</p> <p>Internal RAM*2 2,048×8-bit</p> <p>External ROM 240K×8-bit</p> <p>External RAM 4K×8-bit</p>   |
| Machine Cycles: | <p>High speed mode 0.10μs/20MHz (4.5V~5.5V)</p> <p>0.25μs/8MHz(2.7V~5.5V)</p> <p>1.00μs/2MHz(2.0V~5.5V)</p> <p>Low speed mode 125μs/32KHz(2.0V~5.5V)</p>  |
| Interrupts:     | <p>17 interrupts</p> <p>&lt;External interrupts&gt;</p> <p>The active edge can be selected for all external interrupts</p> <p>IRQ0 External interrupt (can be connected to noise filter)</p> <p>IRQ1 External interrupt (can determine zero crossings, can be connected to noise filter)</p> <p>IRQ2 External interrupt (synchronous output event)</p> <p>IRQ3 External interrupt</p> <p>IRQ4 External interrupt (dual function for key interrupts)</p> <p>&lt;Timer interrupts&gt;</p> <p>TM0IRQ Timer 0 (8-bit timer)</p> <p>TM1IRQ Timer 1 (8-bit timer)</p> <p>TM2IRQ Timer 2 (8-bit timer)</p> <p>TM3IRQ Timer 3 (8-bit timer)</p> <p>TM4IRQ Timer 4 (16-bit timer)</p> <p>TM5IRQ Timer 5 (8-bit timer)</p> <p>TBIRQ Clock timer interrupts</p> <p>&lt;Serial communication interrupt&gt;</p> <p>SC0IRQ Serial 0 (synchronous + simple UART)</p> <p>SC1IRQ Serial 1 (synchronous)</p> <p>SC2IRQ Serial 2 (synchronous + simple IIC)</p> <p>&lt;Automatic transfer complete interrupt&gt;</p> <p>ATCIRQ-Automatic transfer complete</p> |

\*2 Differs depending upon the model.  
[ref: 1-1-2 "Product Summary"]



<A/D conversion complete interrupt>

ADIRQ A/D conversion complete

<Runaway interrupt>

NMI Overflow of watchdog timer

Automatic transfer: Activated by each type of interrupt

Dedicated 1 word transfers between memory and peripheral function block

Variable data length up to 256 bytes

|                                |   |
|--------------------------------|---|
| Timer/Counters:                | seven timers, all can generate interrupts   |
|                                | <p>Timer 0      8-bit timer</p> <p>Square wave output and 8-bit PWM output are possible.</p> <p>Clock source: <math>f_{osc}</math>, <math>f_s</math>, <math>f_s/4</math>, TM0IO pin input</p> <p>Can generate remote control carrier</p> <p>Timer 1      8-bit timer</p> <p>Square wave output and synchronous output event</p> <p>Clock source: <math>f_s/16</math>, <math>f_s/64</math>, <math>f_x</math>, TM1IO pin input</p> <p>Timers 0 and 1 may be cascaded.</p> <p>Timer 2      8-bit timer</p> <p>Square wave output, 8-bit PWM output are possible, and synchronous output event.</p> <p>Clock source: <math>f_s</math>, <math>f_s/4</math>, <math>f_x</math>, TM2IO pin input</p> <p>Timer 3      8-bit timer</p> <p>Square wave output, synchronous serial/UART baud rate timer</p> <p>Clock source: <math>f_{osc}</math>, <math>f_s/4</math>, <math>f_s/16</math>, TM3IO pin input</p> <p>Can generate remote control carrier</p> <p>Timers 2 and 3 can be cascaded.</p> <p>Timer 4      16-bit timer</p> <p>Square wave output, 16-bit PWM output are possible, and synchronous output event.</p> <p>Clock source: <math>f_{osc}</math>, <math>f_s/4</math>, <math>f_s/16</math>, TM4IO pin input</p> <p>Input capture function</p> <p>Time base timer</p> <p>Clock source: <math>f_{osc}</math>, <math>f_s/4</math>, <math>f_x</math>, <math>f_x/2^{13}</math> or <math>f_{osc}/2^{13}</math></p> <p>XIO      at 32kHz, can be set to measure one minute intervals</p> <p>Can operate independently as timer 5 (8-bit timer).</p> <p>Watchdog timer</p> <p>Selected by the mask option as <math>f_{osc}/2^{17}</math>, <math>f_{osc}/2^{19}</math>, or <math>f_{osc}/2^{21}</math></p> |
| Synchronous output function:   | The set value in output from port 7 in synchronization with the overflow of timer 1, timer 2, or timer 4, or at the edge of transition of IRQ2.   |
| Remote control carrier output: | Based on the timer output, a remote control carrier with duty ratio of 1/2, 1/3 can be output.  |
| Buzzer output:                 | Output frequency can be selected from $f_s/2^9$ , $f_s/2^{10}$ , $f_s/2^{11}$ , or $f_s/2^{12}$   |

Serial interface: 3 channels

- CH0 Synchronous/ Simple UART (half-duplex)
  - Transfer clock:  $fs/2$ ,  $fs/4$ ,  $fs/16$ ,  $1/2$  of timer 3 output
  - When using timer 3, the transfer rates for a 12MHz oscillation are 19200/9600/4800/2400/1200/300 bps.
  - MSB or LSB can be selected as the first bit for transfer. An arbitrary transfer size of 1~8 bits can be selected.
- CH1 Synchronous
  - Transfer clock:  $fs/2$ ,  $fs/8$ ,  $fs/64$ ,  $1/2$  of timer 3 output
  - MSB or LSB can be selected as the first bit for transfer. An arbitrary transfer size of 1~8 bits can be selected.
- CH2 Synchronous
  - Transfer clock:  $fs$ ,  $fs/2$ ,  $fs/4$ ,  $1/2$  of timer 0 output
  - MSB or LSB can be selected as the first bit for transfer. An arbitrary transfer size of 1~8 bits can be selected.
  - Simple IIC communication is possible (with a single master)

A/D converter: 10 bits  $\times$  8 channels

LED driver function: 8 pins

Ports:

- I/O ports 57 ports (57 have dual functions)
  - LED (large current) driver ports: 8 ports (push-pull configuration)
  - Number of pins with dual function for external expansion mode: 30
- Input ports 13 ports (all have dual functions)
  - Number of pins with dual function for external interrupts: 5 (One of which can also be used for zero-cross input.)
  - Number of pins with dual function for A/D input: 8
  - Analog reference voltage input pins: 2
  - Operation mode input pin: 1
  - Reset input pin: 1

Operation modes: NORMAL mode  
 SLOW mode  
 HALT mode  
 STOP mode  
 and switches operating clock

Package: 80-pin QFS

# 1-3 Pins

## 1-3-1 Pin Diagram

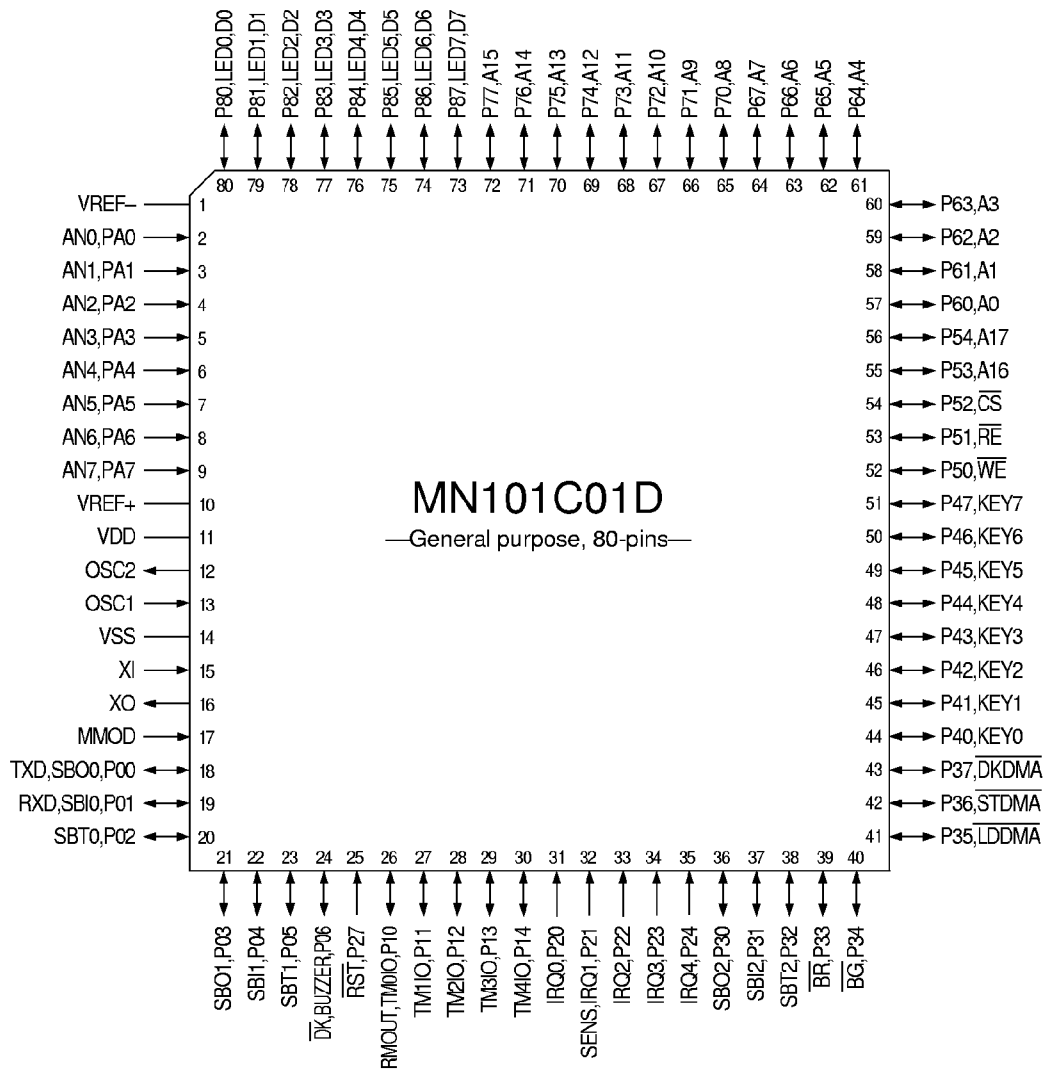


Figure 1-3-1 Pin Diagram (80QFS: top view)

## 1-3-2 Pin Function Summary

Table 1-3-1 Pin Function Summary (1/5)

| Pin No.  | Name         | Type            | Dual Function  | Function                            | Description   |
|----------|--------------|-----------------|--|-------------------------------------|---|
| 14<br>11 | VSS<br>VDD   | –               |  | Power supply pins                   | Apply 2.0V~5.5V to VDD and 0V to VSS.   |
| 13<br>12 | OSC1<br>OSC2 | Input<br>Output |  | Clock input pin<br>Clock output pin | Connect these oscillation pins to ceramic or crystal oscillators for high-speed clock operation.<br>If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.   |
| 15<br>16 | XI<br>XO     | Input<br>Output |  | Clock input pin<br>Clock output pin | Connect these oscillation pins to ceramic or crystal oscillators for low-speed clock operation.<br>If the clock is an external input, connect it to XI and leave XO open. The chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to VSS and leave XO open.   |
| 25       | RST          | I/O             | P27  | Reset pin                           | This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ).<br>Setting this pin low initializes, the internal state of the device. Thereafter, setting the input to an "H" level, releases the reset. The hardware waits for the system clock to stabilize, and then processes the reset interrupt.<br>Also, if "0" is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between $\overline{\text{RST}}$ and VDD, it is recommended that a discharge diode be placed between $\overline{\text{RST}}$ and VDD. |
| 18~24    | P00~P06      | I/O             | SBO0(TXD),<br>SB10(RXD),<br>SBT0,SBO1,<br>SB11,SBT1,<br>$\overline{\text{DK}}$<br>(BUZZER) | I/O port 0                          | 7-bit CMOS tri-state I/O port.<br>Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register.<br>At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).  |

Table 1-3-1 Pin Function Summary (2/5)

| Pin No. | Name    | Type  | Dual Function  | Function     | Description  |
|---------|---------|-------|--|--------------|--|
| 26~30   | P10~P14 | I/O   | TM0IO (RMOUT), TM1IO~TM4IO   | I/O port 1   | 5-bit CMOS tri-state I/O port.<br>Each bit can be set individually as either an input or output by the P1DIR register. A pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).  |
| 31~35   | P20~P24 | Input | IRQ0, IRQ1(SENS), IRQ2~4   | Input port 2 | 5-bit input port. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).   |
| 25      | P27     | Input | $\overline{RST}$   | Input port 2 | Port P27 has an n-channel open-drain configuration. When "0" is written and the reset is initiated by software, a low level will be output.  |
| 36~43   | P30~P37 | I/O   | SBO2<br>SB12<br>SBT2<br>$\overline{BR}$<br>$\overline{BG}$<br>$\overline{LDDMA}$<br>$\overline{STDMA}$<br>$\overline{DKDMA}$ | I/O port 3   | 8-bit CMOS tri-state I/O port.<br>Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).  |
| 44~51   | P40~P47 | I/O   | KEY0~7   | I/O port 4   | 8-bit CMOS tri-state I/O port.<br>Each bit can be set individually as either an input or output by the P4DIR register. A pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).  |
| 52~56   | P50~P54 | I/O   | $\overline{WE}$ , $\overline{RE}$ , $\overline{CS}$ , A16, A17   | I/O port 5   | 5-bit CMOS tri-state I/O port.<br>Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, when single chip mode is selected, the input mode is selected and pull-up resistors for P50~P54 are disabled (high impedance output). During processor mode, $\overline{WE}$ , $\overline{RE}$ , $\overline{CS}$ , A16, and A17 are selected. |
| 57~64   | P60~P67 | I/O   | A0~A7  | I/O port 6   | 8-bit CMOS tri-state I/O port.<br>Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, when single chip mode is selected, the input mode is selected and pull-up resistors for P60~P67 are disabled (high impedance output). During processor mode, output mode is selected for A0~A7.   |



Table 1-3-1 Pin Function Summary (3/5)

| Pin No.  | Name       | Type            | Dual Function          | Function   | Description   |
|----------|------------|-----------------|------------------------|--|---|
| 65~72    | P70~P77    | I/O             | A8~A15                 | I/O port 7   | <p>8-bit CMOS tri-state I/O port.</p> <p>Each individual bit can be switched to an input or output by the P7DIR register. A pull-up or pull-down resistor for each bit can be selected individually by the P7PLUD register.</p> <p>However, pull-up and pull-down resistors cannot be mixed. This port contains a synchronous output function.</p> <p>At reset, when single chip mode is selected, the input mode is selected and pull-up resistors for P70~P77 are disabled (high impedance output). During processor mode, A8~A15 (address signals) are set to output mode.</p> |
| 73~80    | P80~P87    | I/O             | LED0~7<br>(D0~D7)      | I/O port 8   | <p>8-bit CMOS tri-state I/O port.</p> <p>Each individual bit can be switched to an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. When configured as outputs, these pins can drive segments.</p> <p>At reset, when single-chip mode is selected, the input mode is selected and pull-up resistors for P80~P87 are disabled (high impedance output). During processor mode, D0~D7 (data signals) are set to input mode (high-impedance output).</p>  |
| 2~9      | PA0~PA7    | Input           | AN0~AN7                | Input port A   | <p>8-bit input port.</p> <p>A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD register. However, pull-up and pull-down resistors cannot be mixed.</p> <p>At reset, the PA0~PA7 input mode is selected and pull-up resistors are disabled.</p>   |
| 18<br>19 | TXD<br>RXD | Output<br>Input | SBO0(P00)<br>SBI0(P01) | UART transmit data output pin<br>UART receive data input pin | <p>In the serial interface in UART mode, these pins are configured as the receive data input pin and transmit data output pin.</p> <p>A push-pull or n-channel open-drain configuration can be selected for TXD by the SCOMDI register.</p> <p>Pull-up resistors can be selected by the P0PLU register. The TXD and RXD pins are also allocated as P00 and P01 respectively. When not used as serial/UART pins, these can be used as normal I/O pins.</p>   |

Table 1-3-1 Pin Function Summary(4/5)

| Pin No.        | Name                 | Type   | Dual Function          | Function                                   | Description  |
|----------------|----------------------|--------|------------------------|--|--|
| 18<br>21<br>36 | SBO0<br>SBO1<br>SBO2 | Output | TXD(P00)<br>P03<br>P30 | Serial interface transmit data output pins | Transmit data output pins for serial interfaces 0~2. The output configuration, either CMOS push-pull or n-channel open-drain, and pull-up resistors can be selected by the software. Set these pins to the output mode by the P0DIR,P3DIR register.<br>SBO0~2 are allocated as P00, P03, and P30. These may be used as normal I/O pins when the serial interface is not used.  |
| 19<br>22<br>37 | SB10<br>SB11<br>SB12 | Input  | RXD(P01)<br>P04<br>P31 | Serial interface receive data input pins   | Receive data input pins for serial interfaces 0~2. Pull-up resistors can be selected by the P0PLU and P3PLU register.<br>Set these pins to the input mode by the P0DIR and P3DIR register.<br>SB10~2 are allocated as P01, P04, and P31. These can be used as normal I/O pins when the serial interface is not used.   |
| 20<br>23<br>38 | SBT0<br>SBT1<br>SBT2 | I/O    | P02<br>P05<br>P32      | Serial interface clock I/O pins            | Clock input pins for serial interfaces 0~2. The output configuration, either CMOS push-pull or n-channel open-drain output, can be selected by the software. From the P0DIR register, set SBT0 to the output mode and SBT1 to the input mode. The direction of SBT0~2 is selected by the P0DIR and P3DIR register in accordance with the communication mode. Pull-up resistors can be selected by the P0PLU and P3PLU register. SBT0~2 are allocated as P02, P05, and P32. These can be used as normal I/O pins when the serial interface is not used. |
| 26             | RMOUT                | I/O    | P10,TM0IO              | Remote control transmit signal output pin  | Output pin for remote control transmit signal with a carrier signal. Can be used as a normal I/O pin when remote control is not used.  |
| 26~30          | TM0IO~<br>TM4IO      | I/O    | RMOUT<br>(P10~P14)     | Timer I/O pins                             | Event counter clock input pins, overflow pulse output pins timer 0~4 and PWM signal output pins.<br>To use these pins as event clock inputs, configure them as inputs by the P1DIR register. For overflow pulse and PWM output, configure these pins as outputs by the P1DIR register. When the pins are used as inputs, pull-up resistors can be specified by the P1PLU register. When not used for timer I/O, these can be used as normal I/O pins.  |
| 24             | BUZZER               | Output | $\overline{DK}$ (P06)  | Buzzer output                              | Piezoelectric buzzer driver pin. The driving frequency can be selected in the range of $f_s/2^2 \sim f_s/2^{12}$ by the DLYCTR register. Select output mode by the P0DIR register and select buzzer output by the DLYCTR register. When not used for buzzer output, this pin can be used as a normal I/O pin.  |

Table 1-3-1 Pin Function Summary (5/5)

| Pin No.                                | Name                                    | Type   | Dual Function  | Function  | Description   |
|--|---|--|--|---|---|
| 10<br>1                                | VREF+<br>VREF                           | –  |  | +power supply for A/D converter<br>–power supply for A/D converter  | Reference power supply pins for the A/D converter. Normally, the values of VDD=VREF+ and VSS=VREF are used.   |
| 17                                     | MMOD                                    | Input  |  | Memory mode switch input pin  | This pin sets the memory expansion mode. If used with the processor mode, set the input high. If used with the single chip mode or memory expansion mode, set the input low.  |
| 31~35                                  | IRQ0~<br>IRQ4                           | Input  | P20,<br>P21(SENS),<br>P22~P24  | External interrupt input pins   | The valid edge for these external interrupt input pins can be selected with the IRQnICR registers.<br>IRQ1 is an external interrupt pin that is able to determine AC zero crossings. It can also be used as a normal external interrupt.<br>When IRQ0~4 are not used for interrupts, these can be used as normal I/O pins.  |
| 2~9                                    | AN0~AN7                                 | Input  | PA0~PA7  | Analog input pins   | Analog input pins for an 8-channel, 10-bit A/D converter.<br>When not used for analog input, these pins can be used as normal I/O pins.   |
| 44~51                                  | KEY0~<br>KEY7                           | I/O  | P40~P47  | Key interrupt input pins  | Input pins for interrupt based on ORed result of KEY0~7 pin inputs. When not used for KEY input, these pins can be used as normal I/O pins.   |
| 32                                     | SENS                                    | Input  | IRQ1(P21)  | AC zero-cross detection input pin   | SENS is an input pin for an AC zero-cross detection circuit. The AC zero-cross circuit outputs a high level when the input is at an intermediate level. It outputs a low level at all other times. SENS is connected to the P21 input circuit and the IRQ1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as a normal P21 input. The P21IM flag of the FLOAT1 register sets which input is selected.   |
| 39<br>40<br>41<br>42<br>43             | BR<br>BG<br>LDDMA<br>STDMA<br>DKDMA     | Input<br>Output<br>Input<br>Input<br>Output          | P33~P37  | Bus release request input pin<br>Bus use authorization output pin<br>Load cycle input pin<br>Store cycle input pin<br>Memory access complete output pin | Control signals for direct memory access (DMA) of an external memory.<br>BR is the bus release request signal from the external DMA. The BG signal authorizes use of the bus. LDDMA and STDMA are load and store request signals from the external DMA.<br>The DKDMA signal indicates that memory access for the external DMA transfer is complete.   |
| 52<br>53<br>54<br>24<br>55~72<br>73~80 | WE<br>RE<br>CS<br>DK<br>A0~A17<br>D0~D7 | Output<br>Output<br>Output<br>Input<br>Output<br>I/O | P50<br>P51<br>P52<br>P6(BUZZER)<br>P60~P67<br>P70~P77<br>P53~P54<br>P80~P87<br>(LED0~LED7) | Write enable pin<br>Read enable pin<br>Chip select pin<br>Data acknowledge pin<br>Address pins<br>Data pins   | Memory control signals for an expanded memory space external to the MN101CXX.<br>WE is a strobe signal that is output for writing to external memory. RE is a strobe signal that is output for reading from external memory.<br>CS is an chip select signal that is output when external memory is accessed.<br>DK indicates that the external memory access is complete.<br>A0~A17 are address signals output to external memory.<br>D0~D7 are data signals that input data to and output data from external memory. |

## 1-4 Overview of Functions

### 1-4-1 Block Diagram

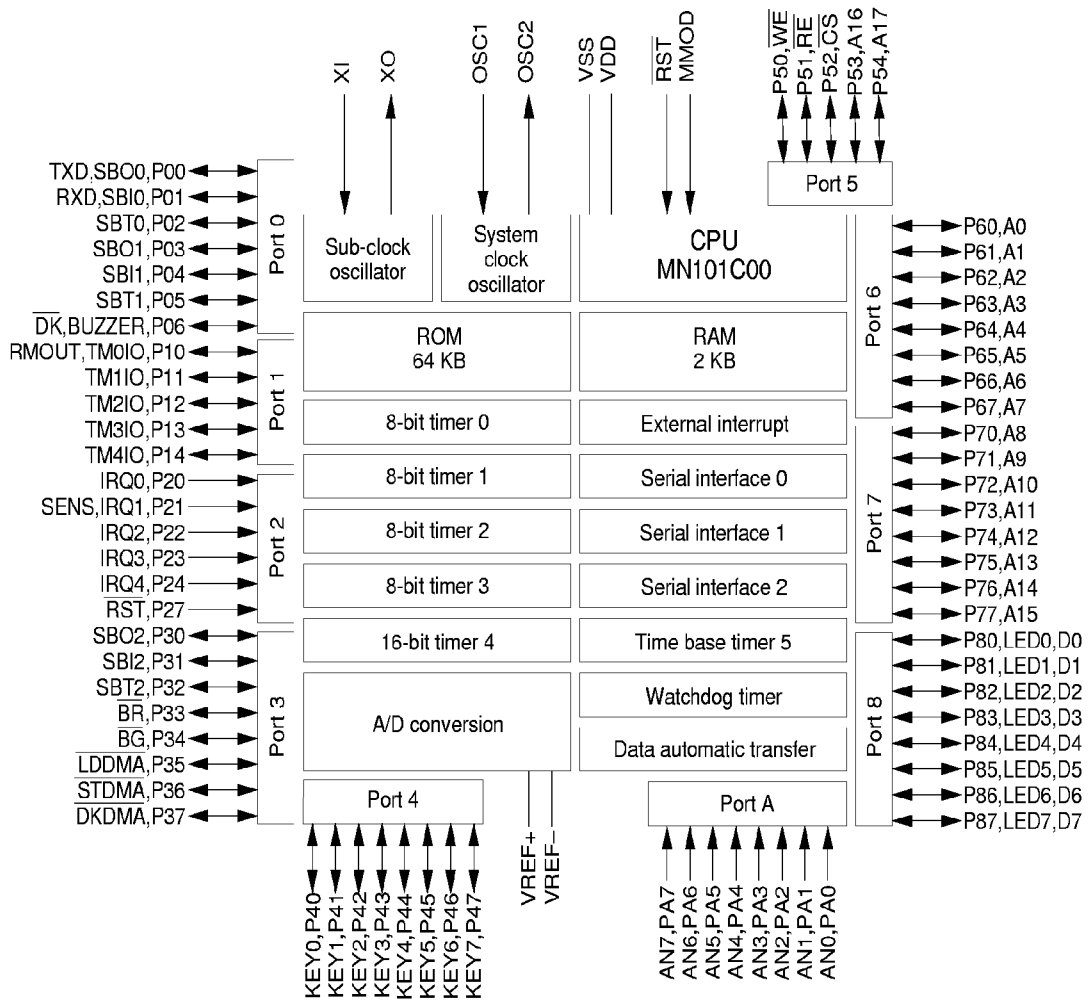


Figure 1-4-1 Block Diagram of Functions

## 1-5 Electrical Characteristics



*This LSI manual describes standard specifications. Before using the LSI, please obtain product specifications from the sales office.*

|                |  |           |
|----------------|--|-----------|
| Contents       | Model                                  | MN101C01D |
| Classification | CMOS integrated circuit                |           |
| Use            | General purpose                        |           |
| Function       | CMOS, 8-bit, single-chip microcomputer |           |

### 1-5-1 Absolute Maximum Ratings

| Parameter |                                      | Symbol        | Rating              | Unit    |    |
|-----------|--------------------------------------|---------------|---------------------|---------|----|
| 1         | Supply voltage                       | $V_{DD}$      | -0.3~+7.0           | V       |    |
| 2         | Input clamp current (SENS)           | IC            | -400~400            | $\mu$ A |    |
| 3         | Input pin voltage                    | $V_I$         | -0.3~ $V_{DD}$ +0.3 | V       |    |
| 4         | Output pin voltage                   | $V_O$         | -0.3~ $V_{DD}$ +0.3 | V       |    |
| 5         | I/O pin voltage                      | $V_{IO1}$     | -0.3~ $V_{DD}$ +0.3 | V       |    |
| 6         | Peak output current                  | P8            | $I_{OL1}$ (peak)    | 30      | mA |
| 7         |                                      | Except P8     | $I_{OL2}$ (peak)    | 20      |    |
| 8         |                                      | All pins      | $I_{OH}$ (peak)     | -10     |    |
| 9         |                                      | P8            | $I_{OL1}$ (avg)     | 20      |    |
| 10        |                                      | Other than P8 | $I_{OL2}$ (avg)     | 15      |    |
| 11        |                                      | All pins      | $I_{OH}$ (avg)      | -5      |    |
| 12        | Average output current <sup>*1</sup> |               |                     |         |    |
| 12        | Tolerable loss                       | PT            | 400                 | mW      |    |
| 13        | Ambient operating temperature        | $T_{opr}$     | -40~85              | °C      |    |
| 14        | Storage temperature                  | $T_{stg}$     | -55~+125            | °C      |    |

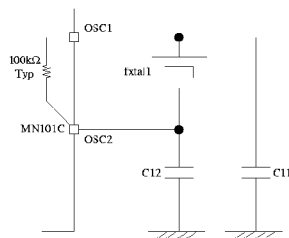
Note: <sup>\*1</sup> Applicable even for an interval of 100ms.

## 1-5-2 Operating Conditions

$$T_a = -40 \sim +85^\circ\text{C} \quad V_{DD} = 2.0 \sim 5.5\text{V} \quad V_{SS} = 0\text{V}$$

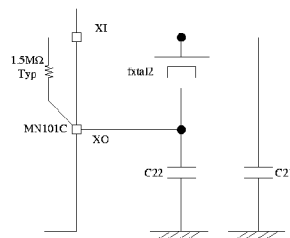
| Parameter                              | Symbol                          | Conditions   | Rating                          |       |        | Unit          |
|--|---------------------------------|--------------|---------------------------------|-------|--------|---------------|
|  |                                 |              | MIN                             | TYP   | MAX    |               |
| <b>Supply voltage</b>                  |                                 |              |                                 |       |        |               |
| 1                                      | Supply voltage during operation | $V_{DD1}$    | $f_{osc} \leq 20.0\text{MHz}$   | 4.5   | 5.5    | V             |
| 2                                      |                                 | $V_{DD2}$    | $f_{osc} \leq 8.39\text{MHz}$   | 2.7   | 5.5    |               |
| 3                                      |                                 | $V_{DD3}$    | $f_{osc} \leq 2.00\text{MHz}$   | 2.0   | 5.5    |               |
| 4                                      |                                 | $V_{DD4}$    | $f_x = 32.768\text{kHz}$        | 2.0   | 5.5    |               |
| 5                                      | Voltage to maintain RAM data    | $V_{DD5}$    | During STOP mode                | 1.8   | 5.5    |               |
| <b>Operating speed *1</b>              |                                 |              |                                 |       |        |               |
| 6                                      | Instruction execution time      | $t_{c1}$     | $V_{DD} = 4.5 \sim 5.5\text{V}$ | 0.100 |        | $\mu\text{s}$ |
| 7                                      |                                 | $t_{c2}$     | $V_{DD} = 2.7 \sim 5.5\text{V}$ | 0.238 |        |               |
| 8                                      |                                 | $t_{c3}$     | $V_{DD} = 2.0 \sim 5.5\text{V}$ | 1.00  |        |               |
| 9                                      |                                 | $t_{c4}$     | $V_{DD} = 2.0 \sim 5.5\text{V}$ |       | 125    |               |
| <b>Crystal oscillator 1 Fig. 1-5-1</b> |                                 |              |                                 |       |        |               |
| 10                                     | Crystal frequency               | $f_{xtal 1}$ | $V_{DD} = 4.5 \sim 5.5\text{V}$ | 1.0   | 20.0   | MHz           |
| 11                                     | External capacitors             | $C_{11}$     |                                 |       | 20     | pF            |
| 12                                     |                                 | $C_{12}$     |                                 |       | 20     |               |
| 13                                     | Internal feedback resistor      | RF10         |                                 |       | 100    | k $\Omega$    |
| <b>Crystal oscillator 2 Fig. 1-5-2</b> |                                 |              |                                 |       |        |               |
| 14                                     | Crystal frequency               | $f_{xtal 2}$ |                                 |       | 32.768 | kHz           |
| 15                                     | External capacitors             | $C_{21}$     |                                 |       | 20     | pF            |
| 16                                     |                                 | $C_{22}$     |                                 |       | 20     |               |
| 17                                     | Internal feedback resistor      | RF20         |                                 |       | 1.5    | M $\Omega$    |

Note: \*1  $t_{c1}, t_{c2}, t_{c3}$ : where OSC1 is the CPU clock  
 $t_{c4}$ : where XI is the CPU clock



The instruction cycle is twice the clock cycle.  
 The feedback resistor is built-in.

Figure 1-5-1 Crystal Oscillator 1



The instruction cycle is four times the clock cycle.  
 The feedback resistor is built-in.

Figure 1-5-2 Crystal Oscillator 2

| Parameter   | Symbol                  | Conditions   | Rating |     |      | Unit    |
|---|-------------------------|--------------|--------|-----|------|---------|
|   |                         |              | MIN    | TYP | MAX  |         |
| External clock input 1 OSC1 (OSC2 is unconnected) |                         |              |        |     |      |         |
| 18  | Clock frequency         | $f_{osc\ 1}$ | 1.0    |     | 20.0 | MHz     |
| 19  | High level pulse width* | $t_{wh\ 1}$  | 20.0   |     | 30.0 | ns      |
| 20  | Low level pulse width*  | $t_{wl\ 1}$  |        |     |      |         |
| 21  | Rise time               | $t_{wr\ 1}$  |        |     | 5.0  | ns      |
| 22  | Fall time               | $t_{wf\ 1}$  |        |     |      |         |
| External clock input 2 XI (XO is unconnected)     |                         |              |        |     |      |         |
| 23  | Clock frequency         | $f_{osc\ 2}$ | 32.768 |     | 100  | kHz     |
| 24  | High level pulse width* | $t_{wh\ 2}$  | 3.5    |     |      | $\mu$ s |
| 25  | Low level pulse width*  | $t_{wl\ 2}$  |        |     |      |         |
| 26  | Rise time               | $t_{wr\ 2}$  |        |     | 20   | ns      |
| 27  | Fall time               | $t_{wf\ 2}$  |        |     |      |         |

\*1 Set the clock duty ratio to 45~55%.

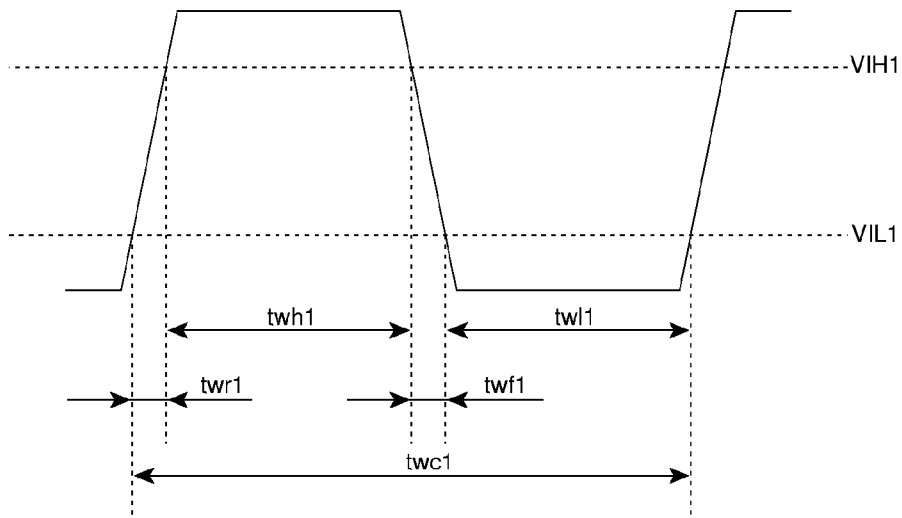


Figure 1-5-3 OSC1 Timing Chart

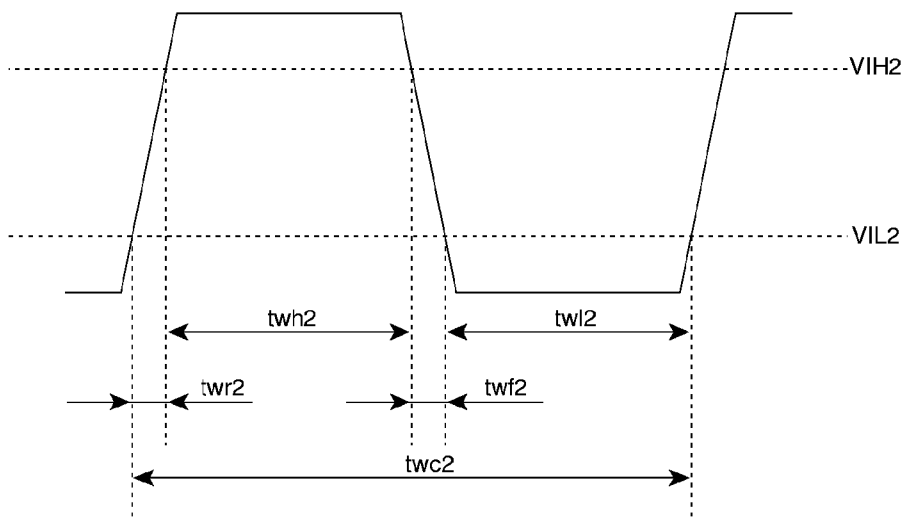


Figure 1-5-4 XI Timing Chart



### 1-5-3 DC Characteristics

$$T_a = -40 \sim +85^\circ\text{C} \quad V_{DD} = 2.0 \sim 5.5\text{V} \quad V_{SS} = 0\text{V}$$

| Parameter                            | Symbol                          | Conditions | Rating                            |     |         | Unit                            |               |
|--------------------------------------|---------------------------------|------------|-----------------------------------|-----|---------|---------------------------------|---------------|
|                                      |                                 |            | MIN                               | TYP | MAX     |                                 |               |
| Supply current (no load at output)*1 |                                 |            |                                   |     |         |                                 |               |
| 1                                    | Supply current during operation | $I_{DD1}$  | fosc=20.0MHz, $V_{DD}=5\text{V}$  |     | 25      | 60                              | mA            |
| 2                                    |                                 | $I_{DD2}$  | fosc=8.39MHz, $V_{DD}=5\text{V}$  |     | 10      | 25                              |               |
| 3                                    |                                 | $I_{DD3}$  | fx =32.768kHz, $V_{DD}=3\text{V}$ |     | t. b. f | t. b. f<br>(120 $\mu\text{A}$ ) | $\mu\text{A}$ |
| 4                                    | Supply current during HALT mode | $I_{DD4}$  | fx =32.768kHz, $V_{DD}=3\text{V}$ |     | 4       | 8                               |               |
| 5                                    | Supply current during STOP mode | $I_{DD5}$  | $V_{DD}=5\text{V}$                |     | 0       | 2                               |               |

Notes: \*1 Measured under conditions of  $T_a=25^\circ\text{C}$  and no load.

The supply current during operation,  $I_{DD1}$  ( $I_{DD2}$ ), is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is fixed at  $V_{SS}$ , the input pins are fixed at  $V_{DD}$ , and a 20MHz (8.39MHz) square wave of amplitude  $V_{DD}$ ,  $V_{SS}$  is input to the OSC1 pin.

The supply current during operation,  $I_{DD3}$ , is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is fixed at  $V_{SS}$ , the input pins are fixed at  $V_{DD}$ , and a 32.768kHz square wave of amplitude  $V_{DD}$ ,  $V_{SS}$  is input to the XI pin.

The supply current during HALT mode,  $I_{DD4}$ , is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <HALT mode>, the MMOD pin is fixed at  $V_{SS}$ , the input pins are fixed at  $V_{DD}$ , and an 32.768kHz square wave of amplitude  $V_{DD}$ ,  $V_{SS}$  is input to the OSC1 pin.

The supply current during STOP mode is measured under the following conditions: After the oscillation mode is set to <STOP mode>, the MMOD pin is fixed at  $V_{SS}$ , the input pins are fixed at  $V_{DD}$ , and the OSC1 and XI pins are unconnected.

$$T_a = -40 \sim +85^\circ\text{C} \quad V_{DD} = 2.0 \sim 5.5\text{V} \quad V_{SS} = 0\text{V}$$

| Parameter  | Symbol                | Conditions | Rating  |             |      | Unit        |               |
|--|-----------------------|------------|---|-------------|------|-------------|---------------|
|  |                       |            | MIN   | TYP         | MAX  |             |               |
| Input pin 1 MMOD                                 |                       |            |   |             |      |             |               |
| 6  | Input high voltage 1  | $V_{IH1}$  |   | $0.8V_{DD}$ |      | $V_{DD}$    | V             |
| 7  | Input high voltage 2  | $V_{IH2}$  | $V_{DD} = 4.5 \sim 5.5\text{V}$                                   | $0.7V_{DD}$ |      | $V_{DD}$    | V             |
| 8  | Input low voltage 1   | $V_{IL1}$  |   | 0           |      | $0.2V_{DD}$ | V             |
| 9  | Input low voltage 2   | $V_{IL2}$  | $V_{DD} = 4.5 \sim 5.5\text{V}$                                   | 0           |      | $0.3V_{DD}$ | V             |
| 10   | Input leakage current | $I_{LK1}$  | $V_{IN} = 0 \sim V_{DD}$  |             |      | $\pm 10$    | $\mu\text{A}$ |
| Input pin 2 P20, P22~P24 (Schmitt trigger input) |                       |            |   |             |      |             |               |
| 11   | Input high voltage    | $V_{IH3}$  |   | $0.8V_{DD}$ |      | $V_{DD}$    | V             |
| 12   | Input low voltage     | $V_{IL3}$  | $V_{DD} = 5\text{V}, V_{IN} = 1.5\text{V}$<br>Pull-up resistor ON | 0           |      | $0.2V_{DD}$ | V             |
| 13   | Input leakage current | $I_{LK3}$  | $V_{IN} = 0 \sim V_{DD}$  |             |      | $\pm 10$    | $\mu\text{A}$ |
| 14   | Input high current    | $I_{IH3}$  |   | -30         | -100 | -300        | $\mu\text{A}$ |
| Input pin 3—1 P21 (Schmitt trigger input)        |                       |            |   |             |      |             |               |
| 15   | Input high voltage    | $V_{IH4}$  |   | $0.8V_{DD}$ |      | $V_{DD}$    | V             |
| 16   | Input low voltage     | $V_{IL4}$  |   | 0           |      | $0.2V_{DD}$ | V             |
| 17   | Input leakage current | $I_{LK4}$  | $V_{IN} = 0 \sim V_{DD}$  |             |      | $\pm 10$    | $\mu\text{A}$ |
| 18   | Input high current    | $I_{IH4}$  | $V_{DD} = 5\text{V}, V_{IN} = 1.5\text{V}$<br>Pull-up resistor ON | -30         | -100 | -300        | $\mu\text{A}$ |
| Input pin 3—2 P21 (when used as SENS)            |                       |            |   |             |      |             |               |
| 19   | Input high voltage 1  | $V_{DHH}$  |   | 4.5         |      | $V_{DD}$    | V             |
| 20   | Input low voltage 1   | $V_{DLH}$  | Fig. 1-5-5  | $V_{SS}$    |      | 3.5         |               |
| 21   | Input high voltage 2  | $V_{DHL}$  |   |             | 1.5  |             | $V_{DD}$      |
| 22   | Input low voltage 2   | $V_{DLL}$  |   | $V_{SS}$    |      | 0.5         |               |
| 23   | Input leakage current | $I_{LK10}$ | $V_{IN} = 0\text{V} \sim V_{DD}$                                  |             |      | $\pm 10$    | $\mu\text{A}$ |
| 24   | Input clamp current   | $I_{C10}$  | $V_{IN} > V_{DD}, V_{IN} < 0\text{V}$                             |             |      | $\pm 400$   |               |

SENS pin

|    |           |                 |            |    |  |    |
|----|-----------|-----------------|------------|----|--|----|
| 25 | Rise time | tr <sub>s</sub> | Fig. 1-5-5 | 30 |  | μs |
| 26 | Fall time | tf <sub>s</sub> |            | 30 |  |    |

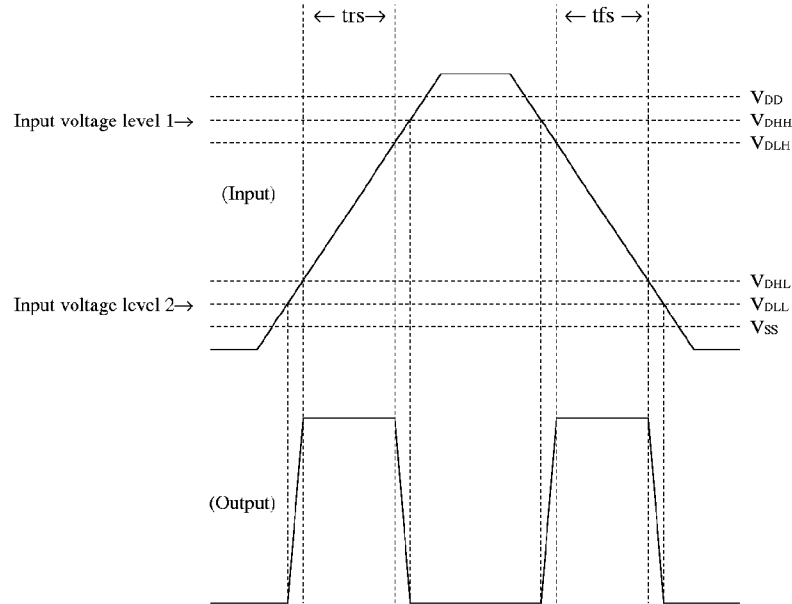


Figure 1-5-5 Operation of AC Zero-Cross Detection Circuit

$T_a = -40 \sim +85^\circ\text{C}$   $V_{DD} = 2.0 \sim 5.5\text{V}$   $V_{SS} = 0\text{V}$

| Parameter           | Symbol                | Conditions | Rating   |             |             | Unit |    |
|---------------------|-----------------------|------------|--|-------------|-------------|------|----|
|                     |                       |            | MIN  | TYP         | MAX         |      |    |
| Input pin 4 PA0~PA7 |                       |            |  |             |             |      |    |
| 27                  | Input high voltage 1  | $V_{IH5}$  | $0.8V_{DD}$  |             | $V_{DD}$    | V    |    |
| 28                  | Input high voltage 2  | $V_{IH6}$  | $V_{DD} = 4.5 \sim 5.5\text{V}$  | $0.7V_{DD}$ | $V_{DD}$    | V    |    |
| 29                  | Input low voltage 1   | $V_{IL5}$  | 0  |             | $0.2V_{DD}$ | V    |    |
| 30                  | Input low voltage 2   | $V_{IL6}$  | $V_{DD} = 4.5 \sim 5.5\text{V}$  | 0           | $0.3V_{DD}$ | V    |    |
| 31                  | Input leakage current | $I_{LK5}$  | $V_{IN} = 0 \sim V_{DD}$   |             | $\pm 2$     | μA   |    |
| 32                  | Input high current    | $I_{IH5}$  | $V_{DD} = 5\text{V}$ , $V_{IN} = 1.5\text{V}$<br>Full up resistor ON   | 30          | 100         | 300  | μA |
| 33                  | Input low current     | $I_{IL5}$  | $V_{DD} = 5\text{V}$ , $V_{IN} = 3.5\text{V}$<br>Pull-down resistor ON | 30          | 100         | 300  | μA |

$$T_a = -40 \sim +85^\circ\text{C} \quad V_{DD} = 2.0 \sim 5.5\text{V} \quad V_{SS} = 0\text{V}$$

| Parameter  | Symbol                | Conditions | Rating  |             |             | Unit          |               |
|--|-----------------------|------------|---|-------------|-------------|---------------|---------------|
|  |                       |            | MIN   | TYP         | MAX         |               |               |
| I/O pin 5 P27 (RST)  |                       |            |   |             |             |               |               |
| 34   | Input high voltage    | $V_{IH7}$  | $0.9V_{DD}$   |             | $V_{DD}$    | V             |               |
| 35   | Input low voltage     | $V_{IL7}$  | 0   |             | $0.2V_{DD}$ | V             |               |
| 36   | Input leakage current | $I_{LK7}$  | $V_{IN} = 0 \sim V_{DD}$  |             | $\pm 10$    | $\mu\text{A}$ |               |
| 37   | Input high current    | $I_{IH7}$  | $V_{DD} = 5\text{V}, V_{IN} = 1.5\text{V}$<br>Internal pull-up resistor | -30         | -100        | -300          | $\mu\text{A}$ |
| 38   | Output low voltage    | $V_{OL7}$  | $V_{DD} = 5\text{V}, I_{OL} = 1.0\text{mA}$                             |             | 0.5         | V             |               |
| I/O pin 6 P00~P06, P10~P14, P30~P37, P40~P47 (Schmitt trigger input) |                       |            |   |             |             |               |               |
| 39   | Input high voltage    | $V_{IH8}$  | $0.8V_{DD}$   |             | $V_{DD}$    | V             |               |
| 40   | Input low voltage     | $V_{IL8}$  | 0   |             | $0.2V_{DD}$ | V             |               |
| 41   | Input leakage current | $I_{LK8}$  | $V_{IN} = 0 \sim V_{DD}$  |             | $\pm 10$    | $\mu\text{A}$ |               |
| 42   | Input high current    | $I_{IH8}$  | $V_{DD} = 5\text{V}, V_{IN} = 1.5\text{V}$<br>Pull-up resistor ON       | -30         | -100        | -300          | $\mu\text{A}$ |
| 43   | Output high voltage   | $V_{OH8}$  | $V_{DD} = 5\text{V}, I_{OH} = 0.5\text{mA}$                             | 4.5         |             | V             |               |
| 44   | Output low voltage    | $V_{OL8}$  | $V_{DD} = 5\text{V}, I_{OL} = 1.0\text{mA}$                             |             | 0.5         | V             |               |
| I/O pin 7 P50~P54, P60~P67   |                       |            |   |             |             |               |               |
| 45   | Input high voltage 1  | $V_{IH9}$  | $0.8V_{DD}$   |             | $V_{DD}$    | V             |               |
| 46   | Input high voltage 2  | $V_{IH10}$ | $V_{DD} = 4.5 \sim 5.5\text{V}$   | $0.7V_{DD}$ |             | $V_{DD}$      | V             |
| 47   | Input low voltage 1   | $V_{IL9}$  |   | 0           |             | $0.2V_{DD}$   | V             |
| 48   | Input low voltage 2   | $V_{IL10}$ | $V_{DD} = 4.5 \sim 5.5\text{V}$   | 0           |             | $0.3V_{DD}$   | V             |
| 49   | Input leakage current | $I_{LK9}$  | $V_{IN} = 0 \sim V_{DD}$  |             | $\pm 10$    | $\mu\text{A}$ |               |
| 50   | Input high current    | $I_{IH9}$  | $V_{DD} = 5\text{V}, V_{IN} = 1.5\text{V}$<br>Pull-up resistor ON       | -30         | -100        | -300          | $\mu\text{A}$ |
| 51   | Output high voltage   | $V_{OH9}$  | $V_{DD} = 5\text{V}, I_{OH} = -0.5\text{mA}$                            | 4.5         |             | V             |               |
| 52   | Output low voltage    | $V_{OL9}$  | $V_{DD} = 5\text{V}, I_{OL} = 1.0\text{mA}$                             |             | 0.5         | V             |               |
| I/O pin 8 P70~P77  |                       |            |   |             |             |               |               |
| 53   | Input high voltage 1  | $V_{IH11}$ | $0.8V_{DD}$   |             | $V_{DD}$    | V             |               |
| 54   | Input high voltage 2  | $V_{IH12}$ | $V_{DD} = 4.5 \sim 5.5\text{V}$   | $0.7V_{DD}$ |             | $V_{DD}$      | V             |
| 55   | Input low voltage 1   | $V_{IL11}$ |   | 0           |             | $0.2V_{DD}$   | V             |
| 56   | Input low voltage 2   | $V_{IL12}$ | $V_{DD} = 4.5 \sim 5.5\text{V}$   | 0           |             | $0.3V_{DD}$   | V             |
| 57   | Input leakage current | $I_{LK8}$  | $V_{IN} = 0 \sim V_{DD}$  |             | $\pm 10$    | $\mu\text{A}$ |               |
| 58   | Input high current    | $I_{IH8}$  | $V_{DD} = 5\text{V}, V_{IN} = 1.5\text{V}$<br>Pull-up resistor ON       | -30         | -100        | -300          | $\mu\text{A}$ |
| 59   | Input low current     | $I_{IL8}$  | $V_{DD} = 5\text{V}, V_{IN} = 3.5\text{V}$<br>Pull-down resistor ON     | 30          | 100         | 300           | $\mu\text{A}$ |
| 60   | Output high voltage   | $V_{OH8}$  | $V_{DD} = 5\text{V}, I_{OH} = -0.5\text{mA}$                            | 4.5         |             | V             |               |
| 61   | Output low voltage    | $V_{OL8}$  | $V_{DD} = 5\text{V}, I_{OL} = 1.0\text{mA}$                             |             | 0.5         | V             |               |

$T_a = -40 \sim +85^\circ\text{C}$   $V_{DD} = 2.0 \sim 5.5\text{V}$   $V_{SS} = 0\text{V}$ 

| Parameter         | Symbol                | Conditions | Rating   |             |             | Unit          |               |
|-------------------|-----------------------|------------|--|-------------|-------------|---------------|---------------|
|                   |                       |            | MIN  | TYP         | MAX         |               |               |
| I/O pin 9 P80~P87 |                       |            |  |             |             |               |               |
| 62                | Input high voltage 1  | $V_{IH13}$ | $0.8V_{DD}$  |             | $V_{DD}$    | V             |               |
| 63                | Input high voltage 2  | $V_{IH14}$ | $V_{DD} = 4.5 \sim 5.5\text{V}$                                      | $0.7V_{DD}$ | $V_{DD}$    | V             |               |
| 64                | Input low voltage 1   | $V_{IL13}$ | 0  |             | $0.2V_{DD}$ | V             |               |
| 65                | Input low voltage 2   | $V_{IL14}$ | $V_{DD} = 4.5 \sim 5.5\text{V}$                                      | 0           | $0.3V_{DD}$ | V             |               |
| 66                | Input leakage current | $I_{LK13}$ | $V_{IN} = 0 \sim V_{DD}$   |             | $\pm 10$    | $\mu\text{A}$ |               |
| 67                | Input high current    | $I_{IH13}$ | $V_{DD} = 5\text{V}$ , $V_{IN} = 1.5\text{V}$<br>Pull up resistor ON | -30         | -100        | -300          | $\mu\text{A}$ |
| 68                | Output high voltage   | $V_{OH13}$ | $V_{DD} = 5\text{V}$ , $I_{OH} = -0.5\text{mA}$                      | 4.5         |             |               | V             |
| 69                | Output low voltage    | $V_{OL13}$ | $V_{DD} = 5\text{V}$ , $I_{OL} = 15\text{mA}$                        |             | 1.0         |               | V             |

### 1-5-4 A/D Converter Characteristics

 $T_a = -40 \sim +85^\circ\text{C}$   $V_{DD} = 2.0 \sim 5.5\text{V}$   $V_{SS} = 0\text{V}$ 

| Parameter | Symbol                                      | Conditions   | Rating     |      |            | Unit          |
|-----------|---|--|------------|------|------------|---------------|
|           |   |  | MIN        | TYP  | MAX        |               |
| 1         | Resolution                                  |  |            |      | 10         | Bits          |
| 2         | Nonlinear error 1                           | $V_{DD} = 5.0\text{V}$ , $V_{SS} = 0\text{V}$<br>$V_{REF+} = 5.0\text{V}$ , $V_{REF-} = 0\text{V}$<br>$T_{AD} = 800\text{ns}$      |            |      | $\pm 3$    | LSB           |
| 3         | Differential linear error 1                 |  |            |      | $\pm 3$    | LSB           |
| 4         | Nonlinear error 2                           | $V_{DD} = 5.0\text{V}$ , $V_{SS} = 0\text{V}$<br>$V_{REF+} = 5.0\text{V}$ , $V_{REF-} = 0\text{V}$<br>$f_{OSC} = 32.768\text{kHz}$ |            |      | $\pm 5$    | LSB           |
| 5         | Differential linear error 2                 |  |            |      | $\pm 5$    | LSB           |
| 6         | Zero traction voltage                       | $V_{DD} = 5.0\text{V}$ , $V_{SS} = 0\text{V}$<br>$V_{REF+} = 5.0\text{V}$ , $V_{REF-} = 0\text{V}$<br>$T_{AD} = 800\text{ns}$      |            | 30   | 100        | mV            |
| 7         | Full-scale transition voltage               |  | 4900       | 4970 |            | mV            |
| 8         | A/D conversion time                         | $T_{AD} = 800\text{ns}$  | 9.6        |      |            | $\mu\text{s}$ |
| 9         |   | $f_{OSC} = 32.768\text{kHz}$   |            |      | 183        | $\mu\text{s}$ |
| 10        |   | $f_{OSC} = 8\text{MHz}$  | 1.0        |      | 36         | $\mu\text{s}$ |
| 11        | Sampling time                               | $f_{OSC} = 32.768\text{kHz}$   |            | 30.5 |            | $\mu\text{s}$ |
| 12        | Reference voltage                           | $V_{REF+}$   | $V_{REF-}$ |      | $V_{DD}$   | V             |
| 13        |   | $V_{REF-}$   | $V_{SS}$   |      | $V_{REF+}$ |               |
| 14        | Analog input voltage                        |  | $V_{REF-}$ |      | $V_{REF+}$ |               |
| 15        | Analog input leakage current                | When $V_{DAIN} = 0 \sim 5\text{V}$ is off  |            |      | $\pm 2$    | $\mu\text{A}$ |
| 16        | Reference voltage pin input leakage current | When $V_{REF-}$ is off<br>$V_{REF-} \leq V_{REF+} \leq V_{DD}$   |            |      | $\pm 10$   | $\mu\text{A}$ |
| 17        | Value of ladder resistor                    | $R_{ladd}$<br>$V_{DD} = 5.0\text{V}$   | 20         | 50   | 80         | k $\Omega$    |

### 1-5-5 Bus Timing (0 wait states) during Memory Expansion

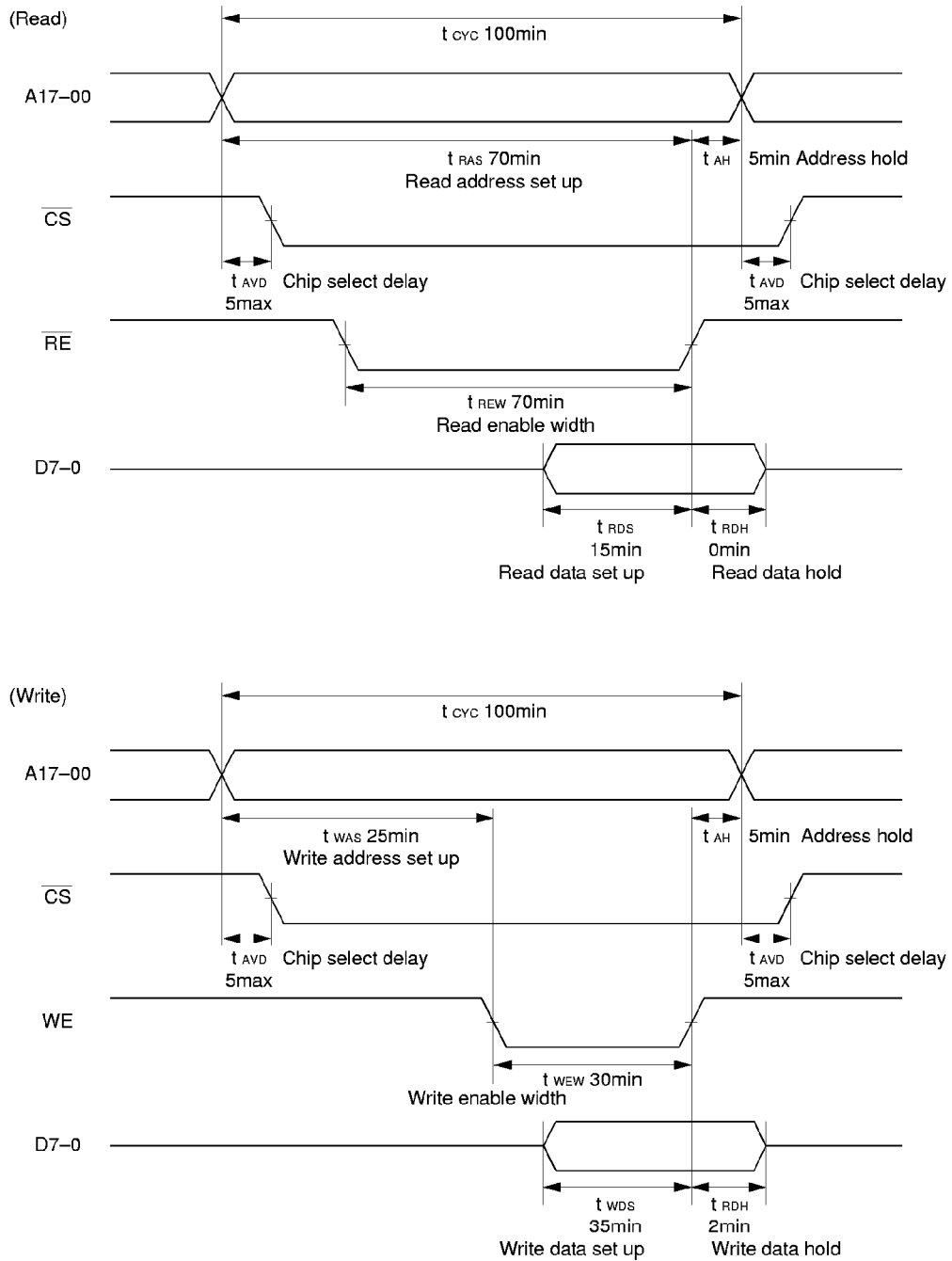


Figure 1-5-6 Bus Timing for Memory Expansion Mode with 0 Wait States

## 1-6 Mask Option Form

Date:

SE No. \_\_\_\_\_

|            |        |
|------------|--------|
| Model Name | MN101C |
|------------|--------|

|          |  |          |  |
|----------|--|----------|--|
| Customer |  | Approval |  |
|----------|--|----------|--|

### 1. Oscillation mode

| Type A | Type B |
|--------|--------|
|        |        |

Note: Type A: Operation begins from the reset cycle in the NORMAL mode.  
 Type B: Operation begins from the reset cycle in the SLOW mode.

### 2. Watchdog timer period setting

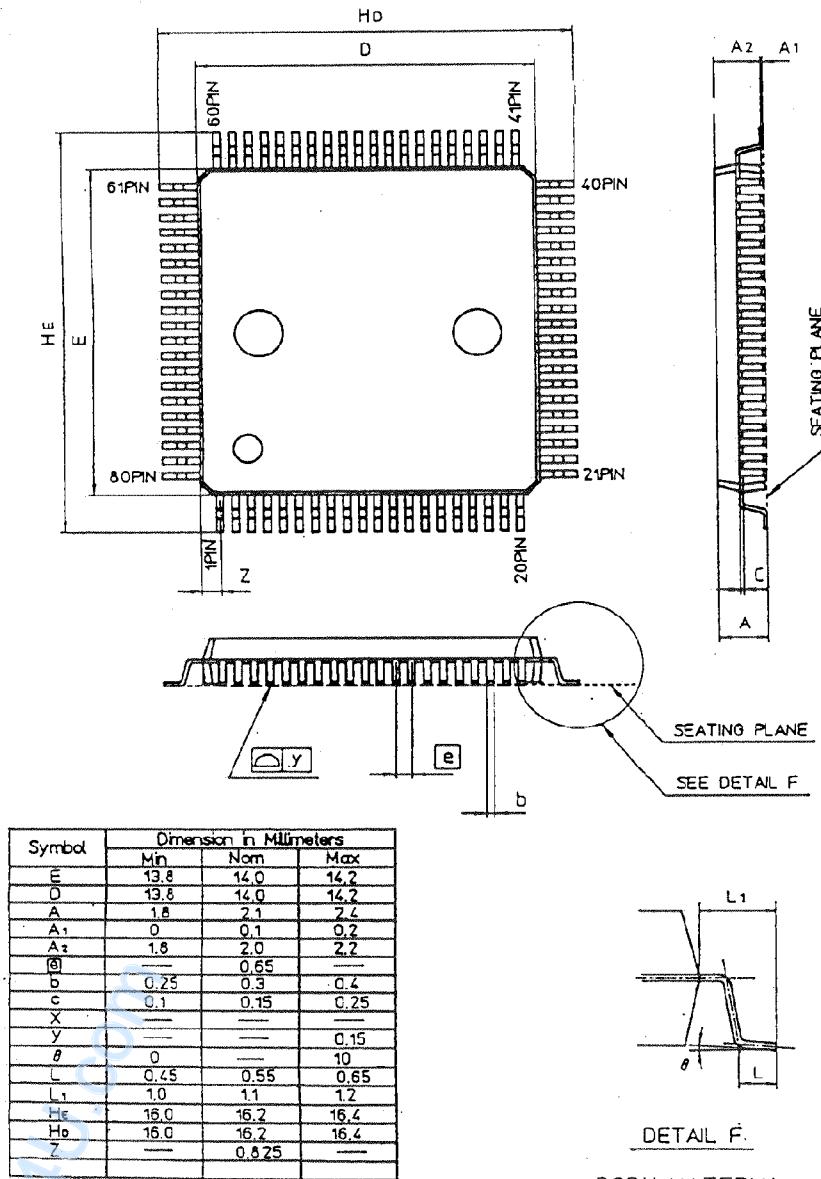
| Detection Period | Selection |
|------------------|-----------|
| $fs/2^{16}$      |           |
| $fs/2^{18}$      |           |
| $fs/2^{20}$      |           |



Contents of mask option are subject to change.


When placing an order for masks, please request the most recent option list from the sales office.

### 1-7 External Dimensions



BODY MATERIAL : Epoxy Resin  
 LEAD MATERIAL : Fe-Ni  
 LEAD FINISH METHOD : Solder Plate

Figure 1-7-1 80-Pin QFS

 The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales office.





Chapter 2 Basic CPU  
Functions



## 2-1 Overview

Basic CPU functions are in conformance with the MN101C00 series manual (architecture manual). This chapter describes specifications unique to the MN101C01D.

## 2-2 Address Space

### 2-2-1 Memory Configuration

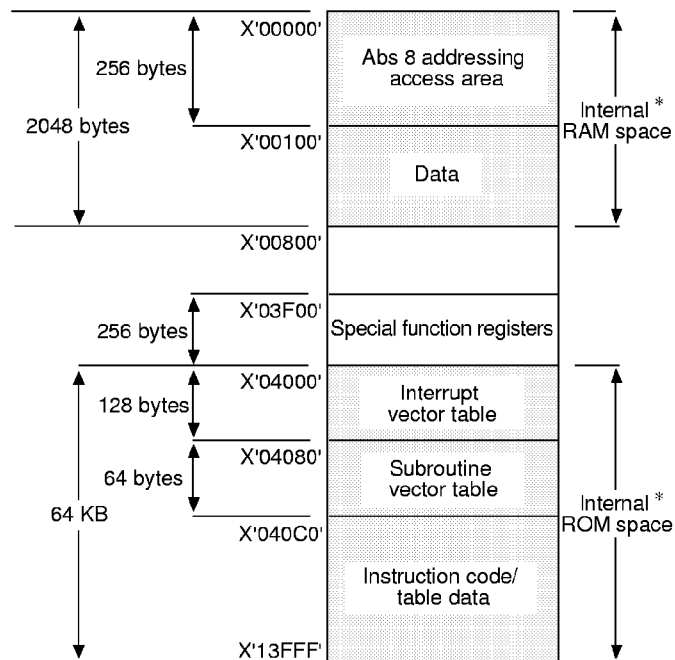


Figure 2-2-1 Memory Map

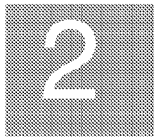
\* Differs depending upon the model.

|            |              |                   |            |
|------------|--------------|-------------------|------------|
| MN101C01A  | Internal RAM | X'00000'~X'005FF' | 1536 bytes |
|            | Internal ROM | X'04000'~X'0BFFF' | 32 KB      |
| MN101C01C  | Internal RAM | X'00000'~X'007FF' | 2048 bytes |
|            | Internal ROM | X'04000'~X'0FFFF' | 48 KB      |
| MN101CP01D | Internal RAM | X'00000'~X'007FF' | 2048 bytes |
|            | Internal ROM | X'04000'~X'13FFF' | 64 KB      |

## 2-2-2 Special Function Registers

Table 2-2-1 Register Map

|       | 0      | 1      | 2      | 3      | 4      | 5      | 6      | 7      | 8      | 9      | A      | B      | C      | D      | E         | F      |                          |
|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-----------|--------|--------------------------|
| 03F0X | CPUM   | MEMCTR | WDCTR  | DLYCTR |        |        |        |        |        |        |        |        |        |        | EX<br>ADV |        | CPU mode, memory control |
| 03F1X | P0OUT  | P1OUT  | P2OUT  | P3OUT  | P4OUT  | P5OUT  | P6OUT  | P7OUT  | P8OUT  |        |        |        |        |        |           | SYSVD  | Port output              |
| 03F2X | P0IN   | P1IN   | P2IN   | P3IN   | P4IN   | P5IN   | P6IN   | P7IN   | P8IN   |        | PAIN   |        |        |        |           |        | Port input               |
| 03F3X | P0DIR  | P1DIR  |        | P3DIR  | P4DIR  | P5DIR  | P6DIR  | P7DIR  | P8DIR  | P1CMD  | PAIMD  |        | P4IMD  |        |           |        | I/O mode control         |
| 03F4X | P0PLU  | P1PLU  | P2PLU  | P3PLU  | P4PLU  | P5PLU  | P6PLU  | P7PLUD | P8PLU  |        | PAPLUD | FLOAT1 | FLOAT2 |        |           |        | Resistor control         |
| 03F5X | SC0MD0 | SC0MD1 | SC0MD2 | SC0MD3 | SC0CTR | SC0TRB | SC0RXB | SC1MD0 | SC1MD1 | SC1TRB | SC2MD0 | SC2MD1 | SC2CTR | SC2TRB |           |        | Serial interface control |
| 03F6X | TM0EC  | TM1BC  | TM2BC  | TM3BC  | TM4BC  | TM4BC  | TM4CH  | TM4CL  | TM4C1  | TM5BC  |        |        |        |        |           |        | Timer control            |
| 03F7X | TM0CC  | TM1CC  | TM2CC  | TM3CC  | TM4CC  | TM4CH  |        |        | TM5CC  |        |        |        |        |        |           |        |                          |
| 03F8X | TM0MD  | TM1MD  | TM2MD  | TM3MD  | TM4MD  |        |        |        | TM5MD  | RMCTR  | NFCTR  |        |        |        |           |        |                          |
| 03F9X | ANCTR0 | ANCTR1 | ANBUFC | ANBUF1 |        |        |        |        |        |        |        |        |        |        |           |        | A/D control              |
| 03FAX | ATMD   | ATCNT  | ATTAPL | ATTAPH | ATIAP  |        |        |        |        |        |        |        |        |        |           |        | ATC control              |
| 03FBX |        |        |        |        |        |        |        |        |        |        |        |        |        |        |           |        | Reserved                 |
| 03FCX |        |        |        |        |        |        |        |        |        |        |        |        |        |        |           |        |                          |
| 03FDX |        |        |        |        |        |        |        |        |        |        |        |        |        |        |           |        |                          |
| 03FEX |        | NM1CR  | IRQ0CR | IRQ1CR | TM01CR | TM1CR  | TM21CR | TB1CR  | SC01CR | ATC1CR | AD1CR  | RQ2CR  | IRC3CR | IRQ4CR | TM31CR    | TM41CR | Interrupt control        |
| 03FFX | TM51CR | SC11CR | SC21CR |        |        |        |        |        |        |        |        |        |        |        |           |        |                          |



## 2-3 Bus Interface

### 2-3-1 Overview

The MN101C01D has a maximum memory space of 256 KB that may be connected to ROM, RAM or external I/O devices. There are two external expansion modes, memory expansion mode and processor mode.

### 2-3-2 Memory Expansion Mode

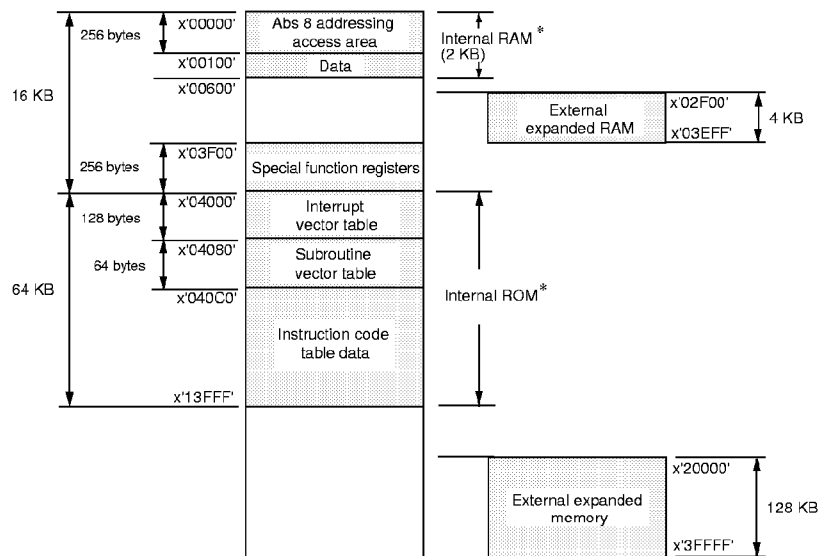
This mode uses both internal ROM/RAM and external expanded ROM/RAM.

The memory expansion mode is set by assigning bit 4 (EXMEM) of the memory control register (MEMCTR) to a value of '1', and by setting bits 7~5 of the expansion address control register (EXADV) to enable pins A8~A17.

Memory areas can be externally expanded as follows:

ROM area ... X'20000'~X'3FFFF' 128 KB

RAM area ... X'02F00'~X'03EFF' 4 KB



\* Differs depending upon the model.  
 [\*] 2-2-1 "Memory Configuration"

MMOD pin = L  
 EXMEM flag = 1

Figure 2-3-1 Memory Expansion Mode

### 2-3-3 Processor Mode

This mode uses internal RAM and external expanded ROM/RAM.

The processor mode is set by pulling the MMOD pin to high.

Memory areas can be externally expanded as follows:

ROM area ... X'04000'~X'3FFFF' 240 KB

RAM area ... X'02F00'~X'03EFF' 4 KB

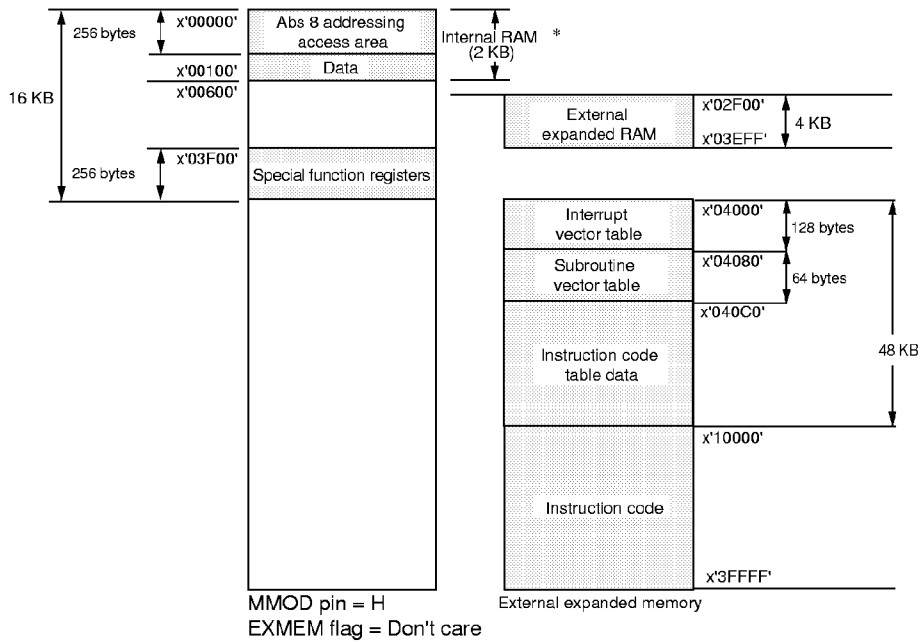


Figure 2-3-2 Processor Mode

\*Differs depending upon the model.

|            |              |                   |            |
|------------|--------------|-------------------|------------|
| MN101C01A  | Internal RAM | X'00000'~X'005FF' | 1536 bytes |
| MN101C01C  | Internal RAM | X'00000'~X'007FF' | 2048 bytes |
| MN101CP01D | Internal RAM | X'00000'~X'007FF' | 2048 bytes |

### 2-3-4 External Memory Connection Example

■ ROM Connection Example (processor mode)

This example shows connection to 512 KB of ROM.

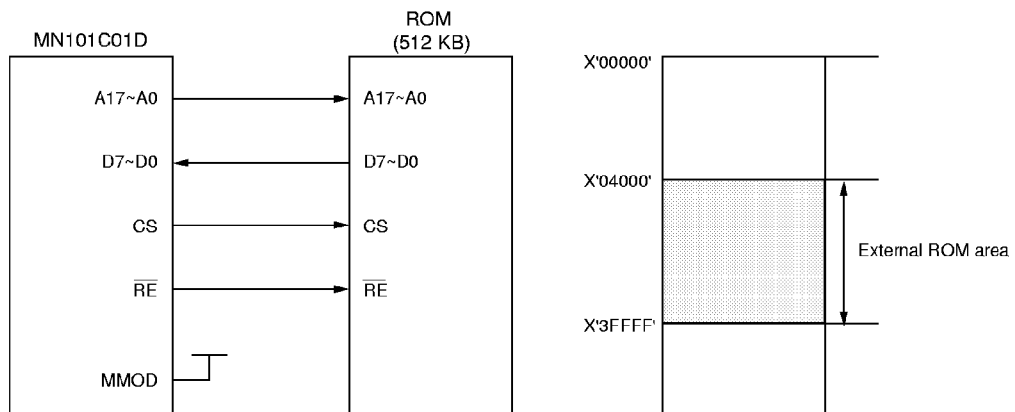


Figure 2-3-3 ROM Connection Example

■ SRAM Connection Example

This example shows connection to 64 KB of SRAM.

The external expansion RAM area is X'002F00'~X'03EFF'.

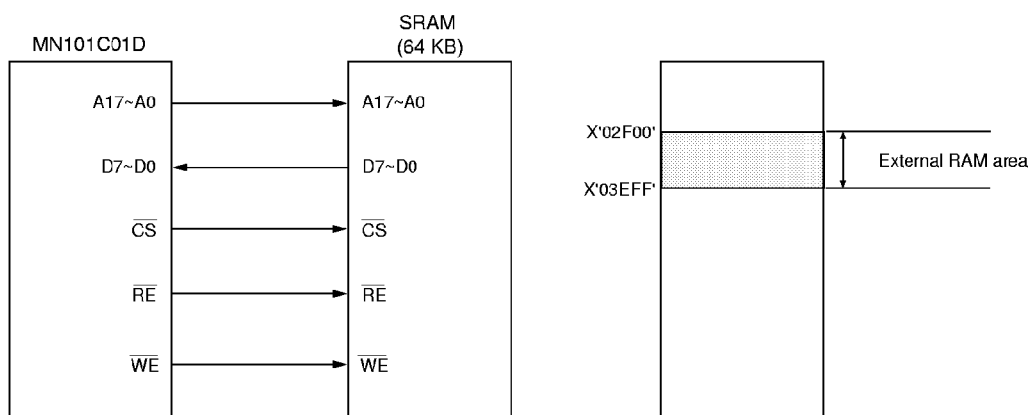


Figure 2-3-4 SRAM Connection Example

■ Access Timing with No Wait Cycles

The  $\overline{RE}$  or  $\overline{WE}$  timing is determined by OSC2. However, since the delay from OSC2 to  $\overline{RE}$  or  $\overline{WE}$  varies depending upon the product, use  $\overline{RE}$  or  $\overline{WE}$  as the reference when synchronizing with other devices. For detailed timing information, refer to the product bus timing specification.

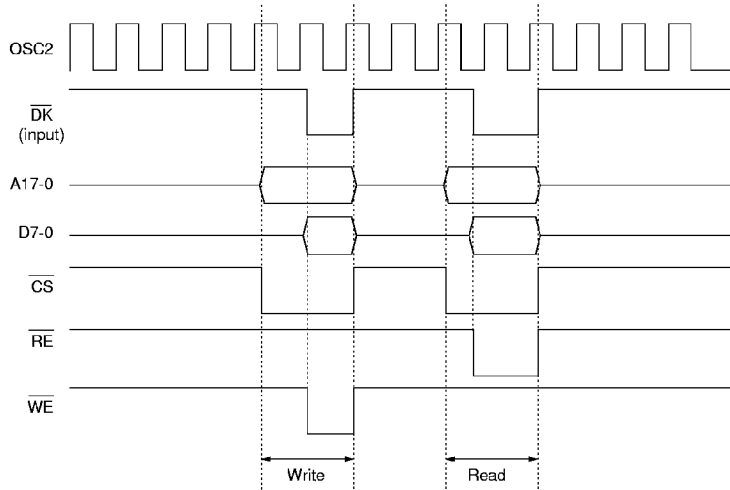


Figure 2-3-5 ROM and RAM Access Timing with No Wait Cycles

■ Access Timing with 1 Wait Cycle

Access timing with 2 and 3 wait cycles follows the same pattern. The latter part of the cycle is extended and the timing is the same.

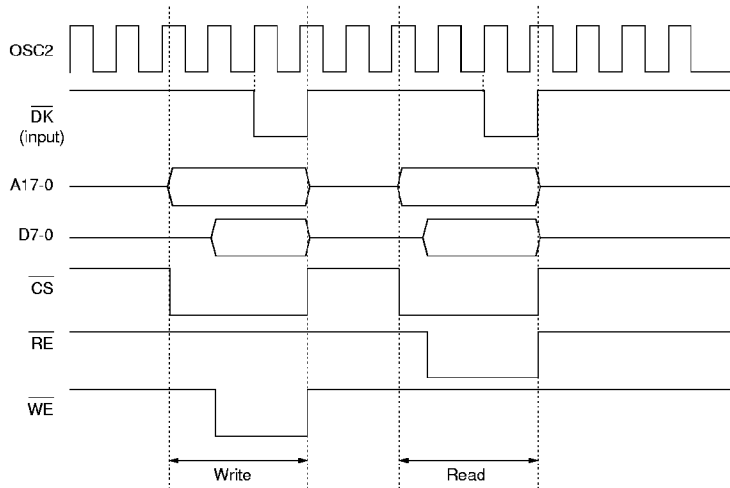


Figure 2-3-6 ROM and RAM Access Timing with 1 Wait Cycle



### 2-3-5 Control Registers

Two byte-length registers control the bus interface: the memory control register (MEMCTR) and the expansion address control register (EXADV).

(1) Memory control register (MEMCTR)

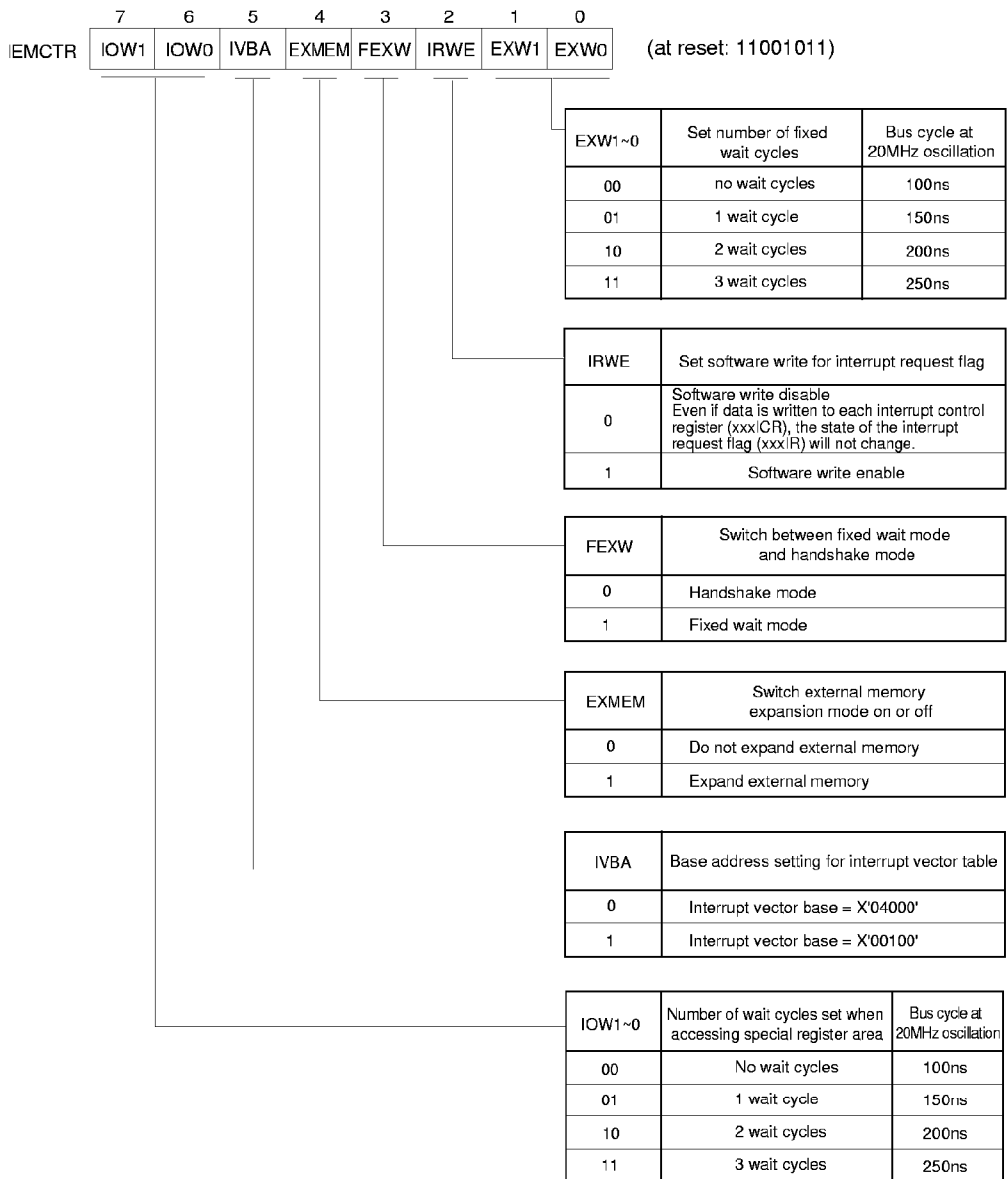


Figure 2-3-7 Memory Control Register (MEMCTR: X'03F01', R/W)

## (2) Expansion address control register (EXADV)

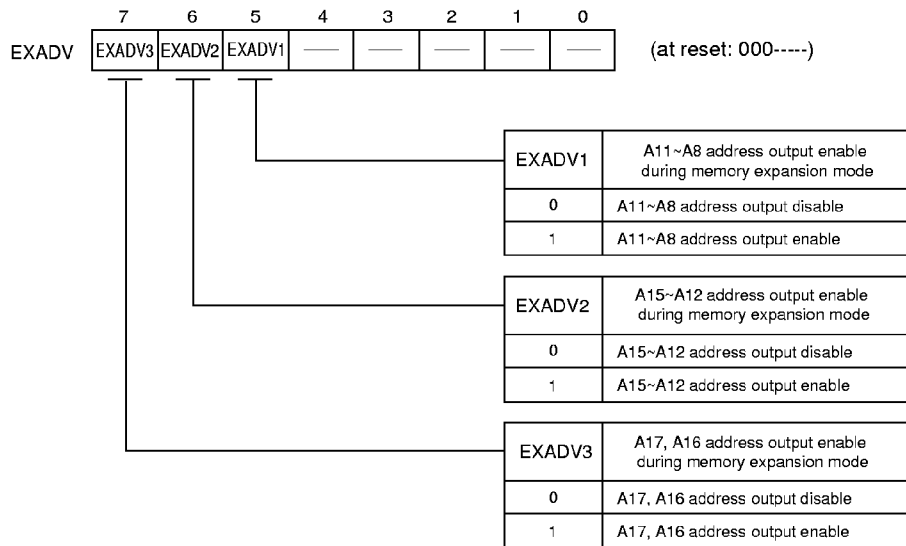


Figure 2-3-8 Expansion Address Control Register (EXADV: X'03F0E', R/W)

## 2-4 Interrupts

### 2-4-1 Accepting and Returning from Interrupts

In the MN101C00 series, when an interrupt is accepted, the hardware pushes the program's return address and the PSW, on to the stack, and branches to the beginning address of the interrupt program specified by the interrupt vector table.

#### ■ Operation when Interrupt is Accepted

1. The stack pointer (SP) contents are update. (SP-6 → SP)
2. The handy address register (HA) is pushed on to the stack.  
 HA upper byte → (SP+5)  
 HA lower byte → (SP+4)
3. The program counter (PC = return address) contents are pushed on to the stack.  
 PC (bit 18~bit 17, bit 0) → (SP+3)  
 PC (bit 16~bit 9) → (SP+2)  
 PC (bit 8~bit 1) → (SP+1)
4. The PSW is pushed on to the stack.  
 PSW → (SP)
5. Copy xxxLVn of the accepted interrupt is copied to IM of the PSW.  
 Interrupt level → IM
6. Execution branches to vector table.

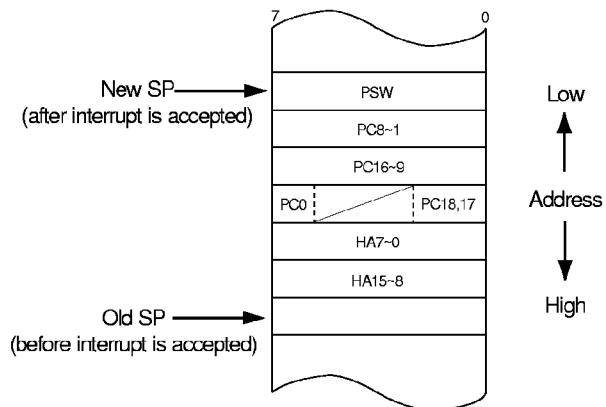


Figure 2-4-1 Stack Status during an Interrupt



Since the contents of data and address registers are not saved, use PUSH instructions in the program to save these values as necessary on the stack.

**■ Operation when Returning from Interrupt**

After the program POPS the register and other values saved by the interrupt service routine, an RTI instruction is implemented to return to the program that was being executed when the interrupt was received.

The processing sequence for the return from interrupt instruction, RTI, is listed below.

1. The processor status word (PSW) is pulled from the stack. (SP)
2. The program counter (PC = return address) is pulled from the stack. (SP+1~3)
3. The handy address register (HA) is pulled from the stack. (SP+4, 5)
4. The SP is pulled. (SP+6 → SP)
5. Execution branches to the address indicated by the PC.

## 2-4-2 Interrupt Sources and Vector Addresses

In addition to reset, there are 20 interrupt vectors that indicate the starting addresses of interrupt programs. These vectors are located in the 80-byte ROM address area X'04004'~X'04053'.

Table 2-4-1 Interrupt Control Registers

| Vector Number | Interrupt Source                | Control Register (address) | Vector Address |
|---------------|---------------------------------|----------------------------|----------------|
| 0             | Reset                           | —————                      | X'04000'       |
| 1             | Non-maskable interrupt (NMI)    | NMICR (X'03FE1')           | X'04004'       |
| 2             | External interrupt 0 (IRQ0)     | IRQ0ICR (X'03FE2')         | X'04008'       |
| 3             | External interrupt 1 (IRQ1)     | IRQ1ICR (X'03FE3')         | X'0400C'       |
| 4             | Timer 0 compare-match (TM0IRQ)  | TM0ICR (X'03FE4')          | X'04010'       |
| 5             | Timer 1 compare-match (TM1IRQ)  | TM1ICR (X'03FE5')          | X'04014'       |
| 6             | Timer 2 compare-match (TM2IRQ)  | TM2ICR (X'03FE6')          | X'04018'       |
| 7             | Time base period (TBIRQ)        | TBICR (X'03FE7')           | X'0401C'       |
| 8             | SC0 transfer complete (SC0IRQ)  | SC0ICR (X'03FE8')          | X'04020'       |
| 9             | ATC transfer complete (ATCIRQ)  | ATCICR (X'03FE9')          | X'04024'       |
| 10            | A/D conversion complete (ADIRQ) | ADICR (X'03FEA')           | X'04028'       |
| 11            | External interrupt 2 (IRQ2)     | IRQ2ICR (X'03FEB')         | X'0402C'       |
| 12            | External interrupt 3 (IRQ3)     | IRQ3ICR (X'03FEC')         | X'04030'       |
| 13            | External interrupt 4 (IRQ4)     | IRQ4ICR (X'03FED')         | X'04034'       |
| 14            | Timer 3 compare-match (TM3IRQ)  | TM3ICR (X'03FEE')          | X'04038'       |
| 15            | Timer 4 compare-match (TM4IRQ)  | TM4ICR (X'03FEF')          | X'0403C'       |
| 16            | Timer 5 compare-match (TM5IRQ)  | TM5ICR (X'03FF0')          | X'04040'       |
| 17            | SC1 transfer complete (SC1IRQ)  | SC1ICR (X'03FF1')          | X'04044'       |
| 18            | SC2 transfer complete (SC2IRQ)  | SC2ICR (X'03FF2')          | X'04048'       |
| 19            | Reserved                        | (X'03FF3')                 | X'0404C'       |
| 20            | Reserved                        | (X'03FF4')                 | X'04050'       |



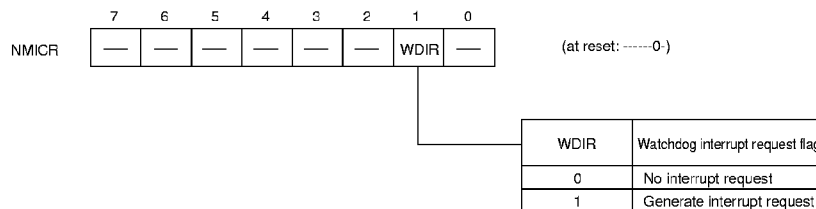
**Set the vector addresses for reserved and unused interrupts to an address containing an RTI instruction.**

## 2-4-3 Interrupt Control Registers

Interrupt control registers consist of the following: a non-maskable interrupt control register (NMICR), external interrupt control registers (IRQnICR), and internal interrupt control registers (TMnICR, TBICR, SCnICR, ATCICR, ADICR).

### ■ Non-maskable Interrupt Control Register (NMICR)

Non-maskable interrupt factors are stored in the non-maskable interrupt control register (NMICR), and are used when a non-maskable interrupt is generated.

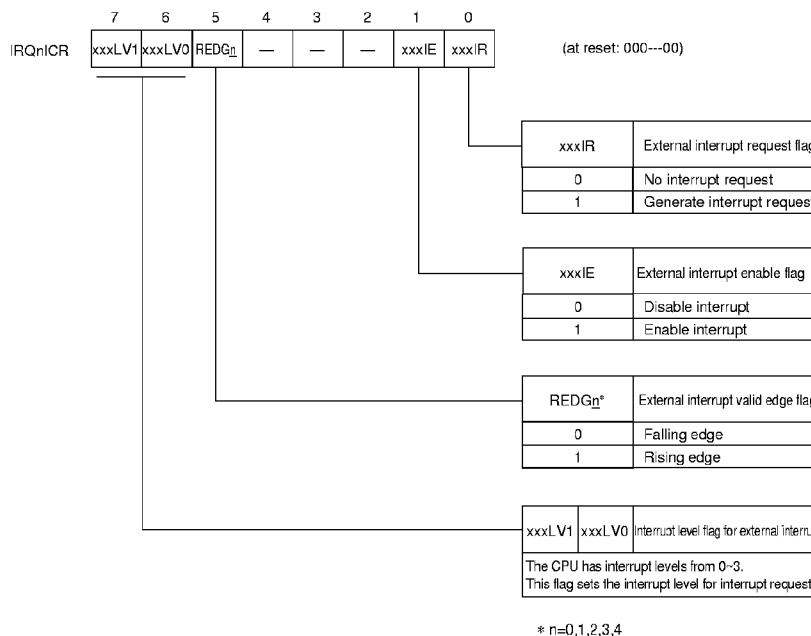


*Be sure to use the MIE flag of the PSW register to write to all interrupt control registers.*

Figure 2-4-2 Non-maskable Interrupt Control Register (NMICR: X'03FE1', R/W)

### ■ External Interrupt Control Registers (IRQnICR)

The external interrupt control registers (IRQnICR) control the interrupt level, valid edge, and request/enable.



*By setting xxxLVn to '11' (level 3), the corresponding interrupt vector will be disabled, regardless of the state of the interrupt enable and interrupt request flags.*

Figure 2-4-3 External Interrupt Control Register (IRQnICR: X'03FE2'~X'03FE3', X'03FEB'~X'03FED', R/W)

■ Internal Interrupt Control Registers (TMnICR, TBICR, SCnICR, ATCICR, ADICR)  
 The internal interrupt control registers (TMnICR, TBICR, SCnICR, ATCICR, ADICR) control the interrupt levels of internal interrupts, timer interrupts, serial interrupts, A/D conversion complete interrupts, and interrupt request/enable.

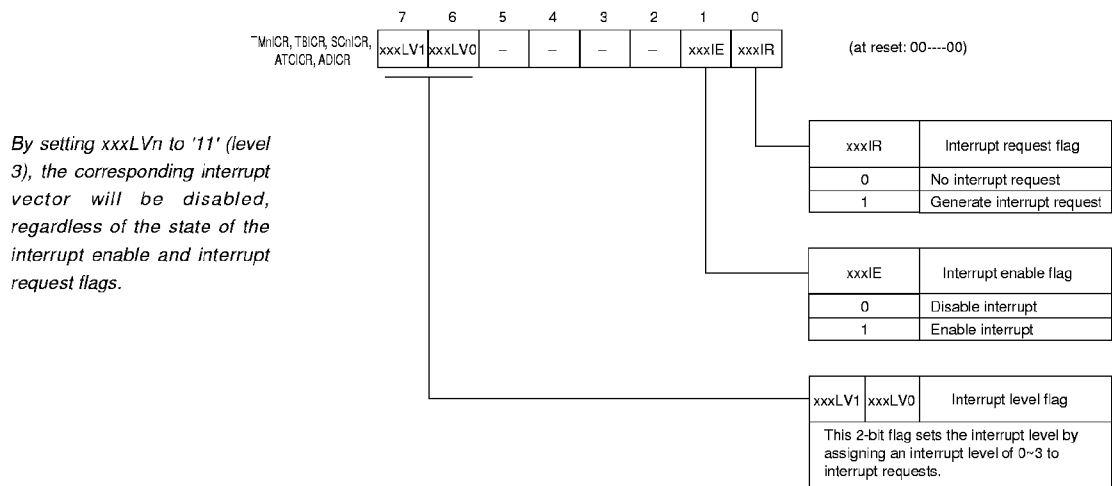


Figure 2-4-4 Internal Interrupt Control Registers (TMnICR, TBICR, SCnICR, ATCICR, ADICR: X'03FE4'~X'03FEA', X'03FEE'~X'03FF4', R/W)

## 2-5 Reset

The CPU contents are reset and registers are initialized when the  $\overline{\text{RST}}$  pin is pulled to low.

### ■ Initiating a Reset

There are two methods to initiate a reset.

- (1) Drive the  $\overline{\text{RST}}$  pin low for at least four clock cycles.

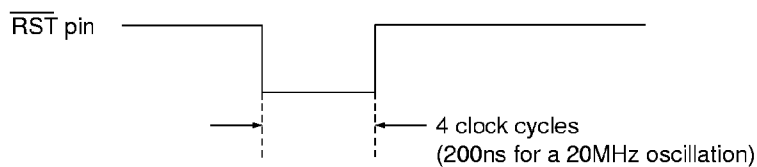


Figure 2-5-1 Minimum Reset Pulse Width

*For the reset to be stable, the low pulse must be maintained for at least four clock cycles. However, it is important to minimize noise, since a reset may occur in a smaller number of clock cycles.*

- (2) Set bit 7 (P2OUT7 flags) of the P2OUT register to "0." After reset is released, the P2OUT flag will be "1."

### ■ Releasing the Reset

When the  $\overline{\text{RST}}$  pin changes from low to high, an internal 15-bit counter begins counting at the oscillation clock frequency. The interval from when this counter begins counting until it overflows is known as the stabilization wait time. After waiting for this amount of time, the internal reset is released and the CPU begins operation.

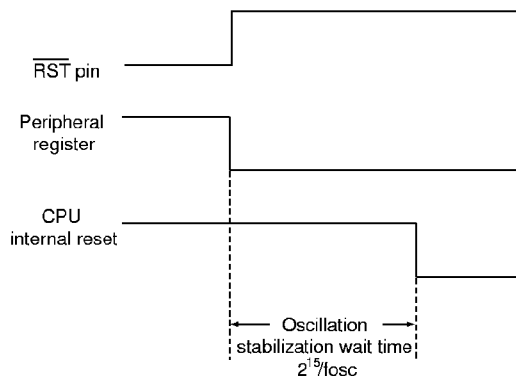


Figure 2-5-2 Reset Release Sequence



When returning from the STOP mode is terminating, the software can use the DLYCTR register to select an oscillation stabilization wait time of 0,  $2^7/f_{osc}$ ,  $2^{11}/f_{osc}$ , or  $2^{15}/f_{osc}$ .





Chapter 3 Port Functions



## 3-1 Overview

A total of 71 pins on the MN101C01D, including those shared with special function pins, are allocated for the 10 ports of P0~P8, and PA.

Each I/O port is assigned according to the special function register area in memory. I/O ports are operated in byte or bit units in the same way as RAM.



**For each I/O port, the PnOUT register (port n output register) that sets the output value is assigned to memory address X'3F1n', and the PnIN register (port n input register) from which the input value is monitored is assigned to memory address X'3F2n'.**

- This I/O control is valid even when special functions are selected for the dual function pins.
- However, when set to the processor mode, registers cannot be used to control the I/O of P06, P50~P54, P60~P67, P70~P77, and P80~P87.

Table 3-1-1 Status When Port Is Reset (single-chip mode)

| Port   | I/O Mode   | Pull-up/Pull-down Resistor     | I/O Port or Special Function |
|--------|------------|--------------------------------|------------------------------|
| Port 0 | Input mode | No pull-up resistor            | I/O port                     |
| Port 1 | Input mode | No pull-up resistor            | I/O port                     |
| Port 2 | Input mode | No pull-up resistor            | I/O port                     |
| Port 3 | Input mode | No pull-up resistor            | I/O port                     |
| Port 4 | Input mode | No pull-up resistor            | I/O port                     |
| Port 5 | Input mode | No pull-up resistor            | I/O port                     |
| Port 6 | Input mode | No pull-up resistor            | I/O port                     |
| Port 7 | Input mode | No pull-up/pull-down resistors | I/O port                     |
| Port 8 | Input mode | No pull-up/pull-down resistors | I/O port                     |
| Port A | Input mode | No pull-up/pull-down resistors | I/O port                     |

Table 3-1-2 Status When Port Is Reset (processor mode)

| Port    | I/O Mode    | Pull-up/Pull-down Resistor   | I/O Port or Special Function |
|---------|-------------|--|------------------------------|
| Port 0* | Input mode  | No pull-up resistor  | I/O port                     |
| Port 1  | Input mode  | No pull-up resistor  | I/O port                     |
| Port 2  | Input mode  | No pull-up resistor  | I/O port                     |
| Port 3  | Input mode  | No pull-up resistor  | I/O port                     |
| Port 4  | Input mode  | No pull-up resistor  | I/O port                     |
| Port 5  | Output mode | Pins $\overline{WE}$ , $\overline{RE}$ , $\overline{CS}$ , A16, A17 are enabled. |                              |
| Port 6  | Output mode | Pins A0~A7 are enabled.  |                              |
| Port 7  | Output mode | Pins A8~A15 are enabled.   |                              |
| Port 8  | Input mode  | Pins D0~D7 are enabled.  |                              |
| Port A  | Input mode  | No pull-up/pull-down resistors   | I/O port                     |

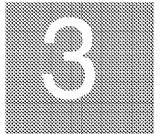
\*P06 enables the  $\overline{DK}$  pin (input mode).

■ Port 0 (P0)

7-bit CMOS tri-state I/O port.

Table 3-1-3 Port 0 Functions

| Pin Name | Type | Dual Function  | Description   |
|----------|------|--|---|
| P00~P06  | I/O  | SBO0(TXD),<br>SBI0(RXD),<br>SBT0,SBO1,<br>SBI1,SBT1,<br>$\overline{DK}$ (BUZZER) | Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output). |



■ Port 1 (P1)

5-bit CMOS tri-state I/O port.

Table 3-1-4 Port 1 Functions

| Pin Name | Type | Dual Function                   | Description   |
|----------|------|---------------------------------|---|
| P10~P14  | I/O  | TM0IO<br>(RMOU),<br>TM1IO~TM4IO | Each bit can be set individually as either an input or output by the P1DIR register. A pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output). |

■ Port 2 (P2)

5-bit CMOS tri-state input port.

Table 3-1-5 Port 2 Functions

| Pin Name | Type  | Dual Function                  | Description  |
|----------|-------|--------------------------------|--|
| P20~P24  | Input | IRQ0,<br>IRQ1(SENS),<br>IRQ2~4 | A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode pull-up resistors are disabled (high impedance output). |

■ Port 3 (P3)

8-bit CMOS tri-state I/O port.

Table 3-1-6 Port 3 Functions

| Pin Name | Type | Dual Function   | Description   |
|----------|------|---|---|
| P30~P37  | I/O  | SBO2,SB12,<br>SBT2, $\overline{BR}$ ,<br>$\overline{BG}$ , $\overline{LDDMA}$ ,<br>$\overline{STDMA}$ ,<br>$\overline{DKDMA}$ | Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode pull-up resistors are disabled (high impedance output). |

■ Port 4 (P4)

8-bit CMOS tri-state I/O port.

Table 3-1-7 Port 4 Functions

| Pin Name | Type | Dual Function | Description   |
|----------|------|---------------|---|
| P40~P47  | I/O  | KEY0~7        | Each bit can be set individually as either an input or output by the P4DIR register. A pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode pull-up resistors are disabled (high impedance output). |

### ■ Port 5 (P5)

5-bit CMOS tri-state I/O port.

Table 3-1-8 Port 5 Functions

| Pin Name | Type | Dual Function  | Description  |
|----------|------|--|--|
| P50~P54  | I/O  | $\overline{WE}, \overline{RE}, \overline{CS}$ ,<br>A16,A17 | Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, when single-chip mode is selected, the input mode pull-up resistors for P50~P54 are disabled (high impedance output). During processor mode, $\overline{WE}$ , $\overline{RE}$ , $\overline{CS}$ , A16, and A17 are selected. |

### ■ Port 6 (P6)

8-bit CMOS tri-state I/O port.

Table 3-1-9 Port 6 Functions

| Pin Name | Type | Dual Function | Description  |
|----------|------|---------------|--|
| P60~P67  | I/O  | A0~A7         | Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, when single chip mode is selected, the input mode pull-up resistors for P60~P67 are disabled (high impedance output). During processor mode, output mode is selected for A0~A7. |

### ■ Port 7 (P7)

8-bit CMOS tri-state I/O port.

Table 3-1-10 Port 7 Functions

| Pin Name | Type | Dual Function | Description  |
|----------|------|---------------|--|
| P70~P77  | I/O  | A8~A15        | Each individual bit can be switched to an input or output by the P7DIR register. A pull-up or pull-down resistor for each bit can be selected individually by the P7PLU register.<br><br>However, pull-up and pull-down resistors cannot be mixed. At reset, when single chip mode is selected, the input mode pull-up resistors for P70~P77 are disabled (high impedance output). During processor mode, A8~A15 (address signals) are set to output mode. |

■ Port 8 (P8)

8-bit CMOS tri-state I/O port.

Table 3-1-11 Port 8 Functions

| Pin Name | Type | Dual Function     | Description  |
|----------|------|-------------------|--|
| P80~P87  | I/O  | LED0~7<br>(D0~D7) | Each individual bit can be switched to an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. When configured as outputs, it is possible to drive segments.<br><br>At reset, when single chip mode is selected, the input mode pull-up resistors for P80~P87 are disabled (high impedance output). During processor mode, D0~D7 (data signals) are set to high impedance outputs. |

■ Port A (PA)

8-bit CMOS tri-state input port.

Table 3-1-12 Port A Functions

| Pin Name | Type  | Dual Function | Description   |
|----------|-------|---------------|---|
| PA0~PA7  | Input | AN0~AN7       | A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD register. However, pull-up and pull-down resistors cannot be mixed.<br><br>At reset, the input mode pull-up resistors for PA0~PA7 are disabled. |

## 3-2 Port Control Registers

### 3-2-1 Overview

Forty-three registers control the I/O ports. See table 3-2-1.

Table 3-2-1 I/O Port Control Registers (1/2)

| Name  | Address  | R/W | Function                            |
|-------|----------|-----|-------------------------------------|
| P0OUT | X'03F10' | R/W | Port 0 output register              |
| P1OUT | X'03F11' | R/W | Port 1 output register              |
| P2OUT | X'03F12' | R/W | Port 2 output register              |
| P3OUT | X'03F13' | R/W | Port 3 output register              |
| P4OUT | X'03F14' | R/W | Port 4 output register              |
| P5OUT | X'03F15' | R/W | Port 5 output register              |
| P6OUT | X'03F16' | R/W | Port 6 output register              |
| P7OUT | X'03F17' | R/W | Port 7 output register              |
| P8OUT | X'03F18' | R/W | Port 8 output register              |
| SYSMO | X'03F1F' | R/W | Synchronous output control register |
| P0IN  | X'03F20' | R   | Port 0 input register               |
| P1IN  | X'03F21' | R   | Port 1 input register               |
| P2IN  | X'03F22' | R   | Port 2 input register               |
| P3IN  | X'03F23' | R   | Port 3 input register               |
| P4IN  | X'03F24' | R   | Key interrupt control register      |
| P5IN  | X'03F25' | R   | Port 5 input register               |
| P6IN  | X'03F26' | R   | Port 6 input register               |
| P7IN  | X'03F27' | R   | Port 7 input register               |
| P8IN  | X'03F28' | R   | Port 8 input register               |
| PAIN  | X'03F2A' | R   | Port A input register               |
| P0DIR | X'03F30' | R/W | Port 0 direction control register   |
| P1DIR | X'03F31' | R/W | Port 1 direction control register   |
| P3DIR | X'03F33' | R/W | Port 3 direction control register   |



Table 3-2-1 I/O Port Control Registers (2/2)

| Name   | Address  | R/W | Function                                  |
|--------|----------|-----|---|
| P4DIR  | X'03F34' | R/W | Port 4 direction control register         |
| P5DIR  | X'03F35' | R/W | Port 5 direction control register         |
| P6DIR  | X'03F36' | R/W | Port 6 direction control register         |
| P7DIR  | X'03F37' | R/W | Port 7 direction control register         |
| P8DIR  | X'03F38' | R/W | Port 8 direction control register         |
| P1OMD  | X'03F39' | R/W | Port 1 output mode register               |
| PAIMD  | X'03F3A' | R/W | Port A input mode register                |
| P4IMD  | X'03F3C' | R/W | Key interrupt control register            |
| P0PLU  | X'03F40' | R/W | Port 0 pull-up control register           |
| P1PLU  | X'03F41' | R/W | Port 1 pull-up control register           |
| P2PLU  | X'03F42' | R/W | Port 2 pull-up control register           |
| P3PLU  | X'03F43' | R/W | Port 3 pull-up control register           |
| P4PLU  | X'03F44' | R/W | Port 4 pull-up control register           |
| P5PLU  | X'03F45' | R/W | Port 5 pull-up control register           |
| P6PLU  | X'03F46' | R/W | Port 6 pull-up control register           |
| P7PLUD | X'03F47' | R/W | Port 7 pull-up/pull-down control register |
| P8PLU  | X'03F48' | R/W | Port 8 pull-up control register           |
| PAPLUD | X'03F4A' | R/W | Port A pull-up/pull-down control register |
| FLOAT1 | X'03F4B' | R/W | Pin control register 1                    |
| FLOAT2 | X'03F4C' | R/W | Pin control register 2                    |

|       | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |                       |
|-------|--------|--------|--------|--------|--------|--------|--------|--------|-----------------------|
| P0OUT | —      | P0OUT6 | P0OUT5 | P0OUT4 | P0OUT3 | P0OUT2 | P0OUT1 | P0OUT0 | (at reset: -0000000)  |
| P1OUT | —      | —      | —      | P1OUT4 | P1OUT3 | P1OUT2 | P1OUT1 | P1OUT0 | (at reset: ---00000)  |
| P2OUT | P2OUT7 | —      | —      | —      | —      | —      | —      | —      | (at reset: 1-----)    |
| P3OUT | P3OUT7 | P3OUT6 | P3OUT5 | P3OUT4 | P3OUT3 | P3OUT2 | P3OUT1 | P3OUT0 | (at reset: 00000000)  |
| P0IN  | —      | P0IN6  | P0IN5  | P0IN4  | P0IN3  | P0IN2  | P0IN1  | P0IN0  | (at reset: XXXXXXXXX) |
| P1IN  | —      | —      | —      | P1IN4  | P1IN3  | P1IN2  | P1IN1  | P1IN0  | (at reset: ---XXXXXX) |
| P2IN  | —      | —      | —      | P2IN4  | P2IN3  | P2IN2  | P2IN1  | P2IN0  | (at reset: ---XXXXXX) |
| P3IN  | P3IN7  | P3IN6  | P3IN5  | P3IN4  | P3IN3  | P3IN2  | P3IN1  | P3IN0  | (at reset: XXXXXXXXX) |
| P0DIR | —      | P0DIR6 | P0DIR5 | P0DIR4 | P0DIR3 | P0DIR2 | P0DIR1 | P0DIR0 | (at reset: -0000000)  |
| P1DIR | —      | —      | —      | P1DIR4 | P1DIR3 | P1DIR2 | P1DIR1 | P1DIR0 | (at reset: ---00000)  |
| P3DIR | P3DIR7 | P3DIR6 | P3DIR5 | P3DIR4 | P3DIR3 | P3DIR2 | P3DIR1 | P3DIR0 | (at reset: 00000000)  |
| P1OMD | —      | —      | —      | P14TCO | P13TCO | P12TCO | P11TCO | P10TCO | (at reset: 00000000)  |
| P0PLU | —      | P0PLU6 | P0PLU5 | P0PLU4 | P0PLU3 | P0PLU2 | P0PLU1 | P0PLU0 | (at reset: -0000000)  |
| P1PLU | —      | —      | —      | P1PLU4 | P1PLU3 | P1PLU2 | P1PLU1 | P1PLU0 | (at reset: ---00000)  |
| P2PLU | —      | —      | —      | P2PLU4 | P2PLU3 | P2PLU2 | P2PLU1 | P2PLU0 | (at reset: ---00000)  |
| P3PLU | P3PLU7 | P3PLU6 | P3PLU5 | P3PLU4 | P3PLU3 | P3PLU2 | P3PLU1 | P3PLU0 | (at reset: 00000000)  |

Figure 3-2-1 Port Control Registers (1/3)

|       | 7       | 6      | 5      | 4      | 3       | 2       | 1       | 0       |                      |
|-------|---------|--------|--------|--------|---------|---------|---------|---------|----------------------|
| P4OUT | P4OUT7  | P4OUT6 | P4OUT5 | P4OUT4 | P4OUT3  | P4OUT2  | P4OUT1  | P4OUT0  | (at reset: 00000000) |
| P5OUT | —       | —      | —      | P5OUT4 | P5OUT3  | P5OUT2  | P5OUT1  | P5OUT0  | (at reset: ---00000) |
| P6OUT | P6OUT7  | P6OUT6 | P6OUT5 | P6OUT4 | P6OUT3  | P6OUT2  | P6OUT1  | P6OUT0  | (at reset: 00000000) |
| P4IN  | P4IN7   | P4IN6  | P4IN5  | P4IN4  | P4IN3   | P4IN2   | P4IN1   | P4IN0   | (at reset: XXXXXXXX) |
| P5IN  | —       | —      | —      | P5IN4  | P5IN3   | P5IN2   | P5IN1   | P5IN0   | (at reset: ---XXXXX) |
| P6IN  | P6IN7   | P6IN6  | P6IN5  | P6IN4  | P6IN3   | P6IN2   | P6IN1   | P6IN0   | (at reset: XXXXXXXX) |
| P4DIR | P4DIR7  | P4DIR6 | P4DIR5 | P4DIR4 | P4DIR3  | P4DIR2  | P4DIR1  | P4DIR0  | (at reset: 00000000) |
| P5DIR | —       | —      | —      | P5DIR4 | P5DIR3  | P5DIR2  | P5DIR1  | P5DIR0  | (at reset: ---00000) |
| P6DIR | P6DIR7  | P6DIR6 | P6DIR5 | P6DIR4 | P6DIR3  | P6DIR2  | P6DIR1  | P6DIR0  | (at reset: 00000000) |
| P4IMD | IRQ4SEL | —      | —      | —      | P4KYEN4 | P4KYEN3 | P4KYEN2 | P4KYEN1 | (at reset: 0---0000) |
| P4PLU | P4PLU7  | P4PLU6 | P4PLU5 | P4PLU4 | P4PLU3  | P4PLU2  | P4PLU1  | P4PLU0  | (at reset: 00000000) |
| P5PLU | —       | —      | —      | P5PLU4 | P5PLU3  | P5PLU2  | P5PLU1  | P5PLU0  | (at reset: ---00000) |
| P6PLU | P6PLU7  | P6PLU6 | P6PLU5 | P6PLU4 | P6PLU3  | P6PLU2  | P6PLU1  | P6PLU0  | (at reset: 00000000) |

Figure 3-2-1 Port Control Registers (2/3)

|        | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |                       |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|-----------------------|
| P7OUT  | P7OUT7  | P7OUT6  | P7OUT5  | P7OUT4  | P7OUT3  | P7OUT2  | P7OUT1  | P7OUT0  | (at reset: 00000000)  |
| P8OUT  | P8OUT7  | P8OUT6  | P8OUT5  | P8OUT4  | P8OUT3  | P8OUT2  | P8OUT1  | P8OUT0  | (at reset: 00000000)  |
| P7IN   | P7IN7   | P7IN6   | P7IN5   | P7IN4   | P7IN3   | P7IN2   | P7IN1   | P7IN0   | (at reset: XXXXXXXXX) |
| P8IN   | P8IN7   | P8IN6   | P8IN5   | P8IN4   | P8IN3   | P8IN2   | P8IN1   | P8IN0   | (at reset: XXXXXXXXX) |
| PAIN   | PAIN7   | PAIN6   | PAIN5   | PAIN4   | PAIN3   | PAIN2   | PAIN1   | PAIN0   | (at reset: XXXXXXXXX) |
| P7DIR  | P7DIR7  | P7DIR6  | P7DIR5  | P7DIR4  | P7DIR3  | P7DIR2  | P7DIR1  | P7DIR0  | (at reset: 00000000)  |
| P8DIR  | P8DIR7  | P8DIR6  | P8DIR5  | P8DIR4  | P8DIR3  | P8DIR2  | P8DIR1  | P8DIR0  | (at reset: 00000000)  |
| PAIMD  | PAAIN7  | PAAIN6  | PAAIN5  | PAAIN4  | PAAIN3  | PAAIN2  | PAAIN1  | PAAIN0  | (at reset: 00000000)  |
| SYSDM  | SYSDM7  | SYSDM6  | SYSDM5  | SYSDM4  | SYSDM3  | SYSDM2  | SYSDM1  | SYSDM0  | (at reset: 00000000)  |
| P7PLUD | P7PLUD7 | P7PLUD6 | P7PLUD5 | P7PLUD4 | P7PLUD3 | P7PLUD2 | P7PLUD1 | P7PLUD0 | (at reset: 00000000)  |
| P8PLU  | P8PLU7  | P8PLU6  | P8PLU5  | P8PLU4  | P8PLU3  | P8PLU2  | P8PLU1  | P8PLU0  | (at reset: 00000000)  |
| PAPLUD | PAPLUD7 | PAPLUD6 | PAPLUD5 | PAPLUD4 | PAPLUD3 | PAPLUD2 | PAPLUD1 | PAPLUD0 | (at reset: 00000000)  |

Figure 3-2-1 Port Control Registers (3/3)

### 3-2-2 I/O Port Control Registers

This section describes the special function registers that control the MN101C01D's I/O ports.

#### ■ Data Registers

##### • PnOUT registers

Data registers to output to the ports.

Data written to these registers is output from the ports.

|   |                             |
|---|-----------------------------|
| 0 | Low (Vss level) is output.  |
| 1 | High (Vdd level) is output. |

##### • PnIN registers (Read-only registers)

Data registers to input data from the ports.

The value of data at the pins can be input by reading these registers.

|   |              |
|---|--------------|
| 0 | Pin is low.  |
| 1 | Pin is high. |

Input and output registers are mapped to separate addresses.

To use these ports for I/O, configure them as I/O ports in the PnOMD/PnIMD registers, described in this section.

#### ■ Direction Control Registers

##### • PnDIR registers

These registers set the port for use as an input or output.

|   |             |
|---|-------------|
| 0 | Input mode  |
| 1 | Output mode |

#### ■ Pull-up/Pull-down Resistor Control Registers

##### • PnPLU registers

These register settings determine whether internal pull-up resistors are added to the ports.

|   |                     |
|---|---------------------|
| 0 | No pull-up resistor |
| 1 | Pull-up resistor    |

##### • PnPLUD registers

These register settings determine whether internal pull-up or pull-down resistors are added to the ports.

|   |                     |
|---|---------------------|
| 0 | No pull-up resistor |
| 1 | Pull-up resistor    |

■ Synchronous Output Control Register

• SYSMD register

This register determines whether the port pins (P77~P70) are used as I/O ports or as synchronous output pins.

If used as synchronous output pins, the P7DIR, P7PLUD, FLOAT1, and other registers must be set.

|   |                        |
|---|------------------------|
| 0 | I/O port               |
| 1 | Synchronous output pin |

■ Port Output/Input Mode Registers

• PnOMD/PnIMD registers

These register settings determine whether the port pins are used as I/O ports or as special function pins (dual function).

If the special (dual) functions used, the PnDIR, PnPLU, PnPLUD, and other registers must be set.

|   |                      |
|---|----------------------|
| 0 | I/O port             |
| 1 | Special function pin |

■ Key Interrupt Control Register

• P4IMD register

P4 pins can be selected in 2-bit units as key input pins. If even one of the selected ports falls to a low level, a key input interrupt will be generated at that falling edge.

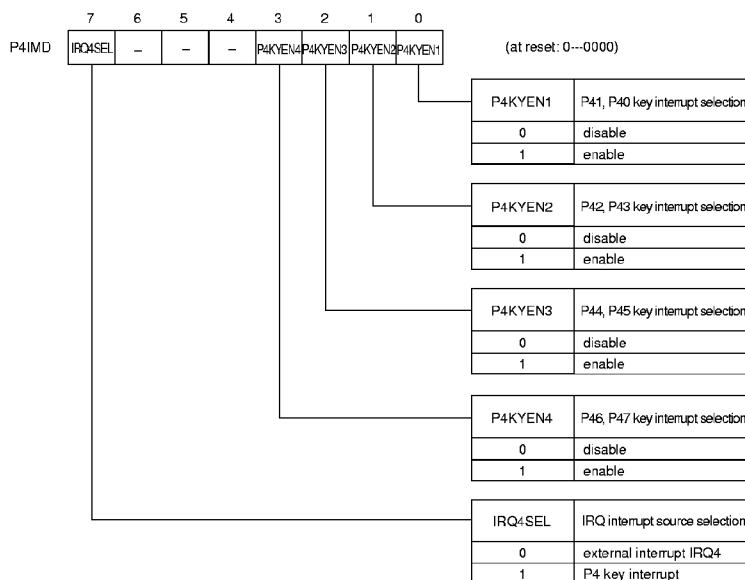


Figure 3-2-2 Key Interrupt Control Register (P4IMD)

**!**  
Setting the PAIMD register prevents unnecessary current from flowing in a pin when an intermediate voltage (analog voltage) is applied to the pin.

**!**  
Set the REDG4 flag (bit 5 of the IRQ4ICR) to "0" (falling edge) when P4 key interrupts are to be used.

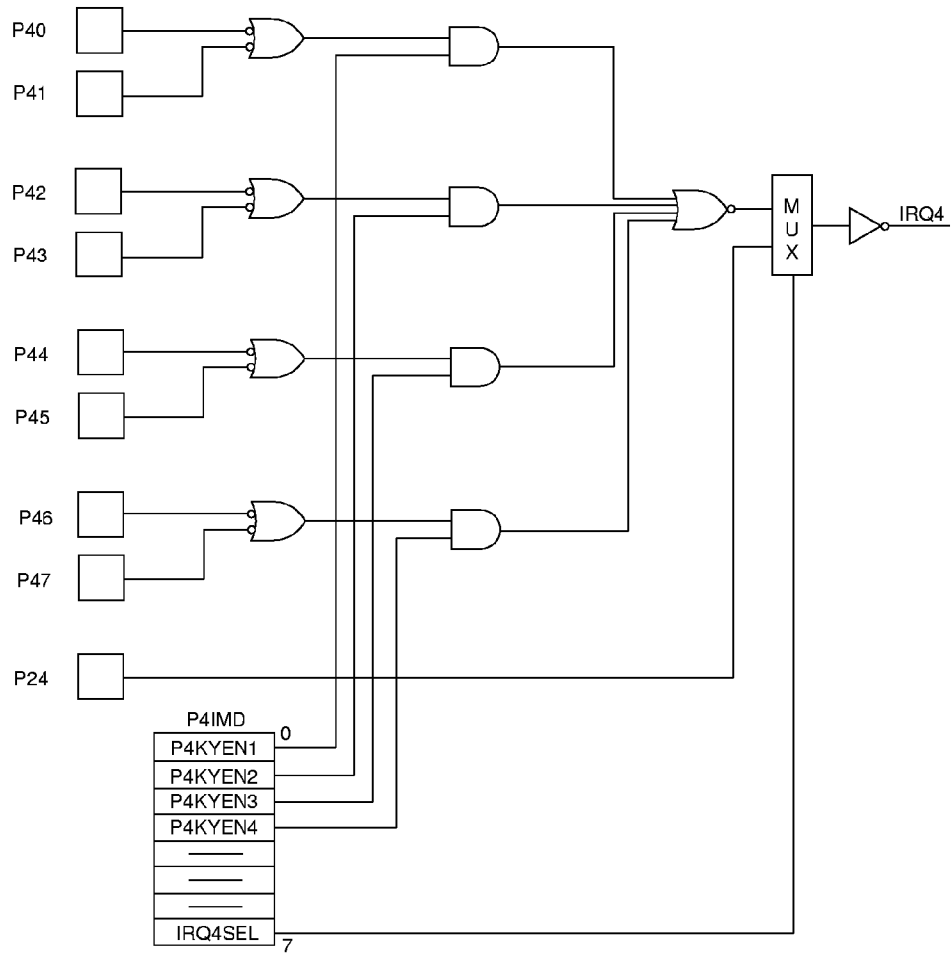


Figure 3-2-3 Key Interrupt Control Block Diagram

■ Pin Control Registers

• FLOAT1 registers

This register specifies whether the resistors attached to pins P7 and PA are pull-up resistors or pull-down resistors.

In addition, this register selects either zero cross input or Schmitt trigger input for pin P21.

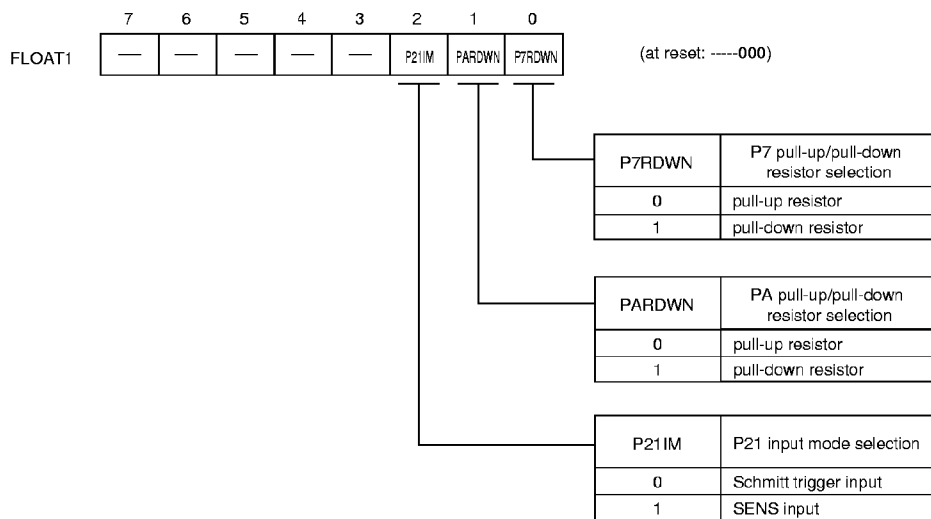


Figure 3-2-4 Pin Control Register 1 (FLOAT1: X'03F4B', R/W)

• FLOAT2 registers

This register selects the output event when P7 is used as a synchronous output.

External interrupts (IRQ2), timer 1 interrupts, timer 2 interrupts or timer 4 interrupts can be selected as the output event.

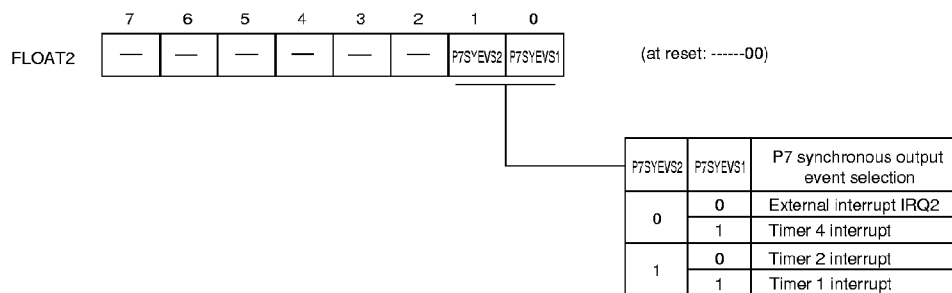
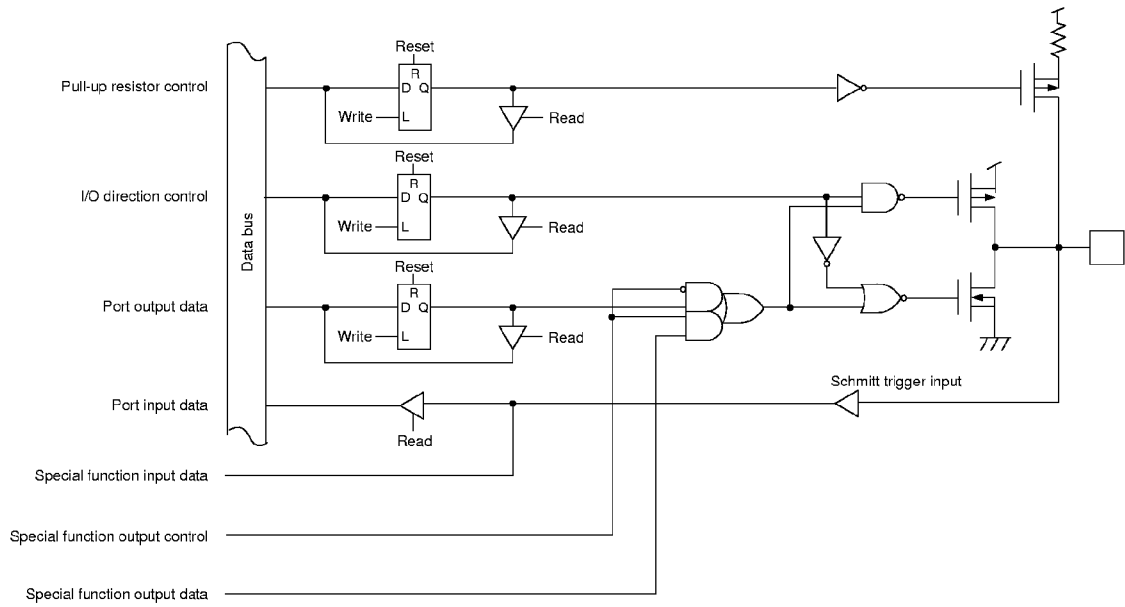


Figure 3-2-5 Pin Control Register 2 (FLOAT2: X'03F4C', R/W)



### 3-3 I/O Port Configuration and Functions

■ P00,P02,P03,P05,P10~P14,P30,P32

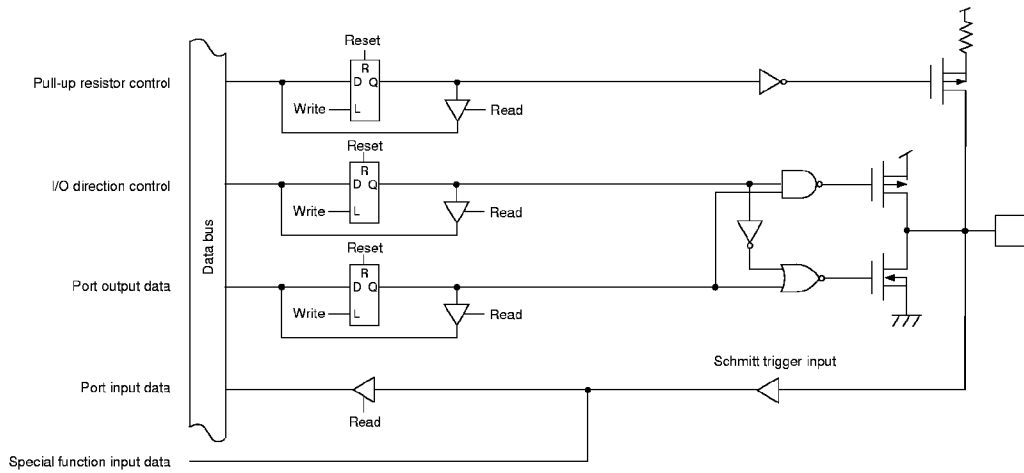


|                                     |                    | P00               | P02     | P03               | P05     | P10                   | P11                   | P12                   | P13                   | P14                   | P30              | P32               |
|-------------------------------------|--------------------|-------------------|---------|-------------------|---------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|------------------|-------------------|
| Pull-up resistor control            | Control bit        | POPLU0            | POPLU2  | POPLU3            | POPLU5  | P1PLU0                | P1PLU1                | P1PLU2                | P1PLU3                | P1PLU4                | E3PLU0           | P3PLU2            |
|                                     | Register (address) | POPLC (X'03140')  |         |                   |         |                       | P1PLU (X'03141')      |                       |                       |                       | P3PLU (X'03143') |                   |
| I/O direction control               | Control bit        | PODIR0            | PODIR2  | PODIR3            | PODIR5  | P1DIR0                | P1DIR1                | P1DIR2                | P1DIR3                | P1DIR4                | E3DIR0           | P3DIR2            |
|                                     | Register (address) | PODIR (X'03F30')  |         |                   |         |                       | P1DIR (X'03F31')      |                       |                       |                       | P3DIR (X'03F33') |                   |
| Port output                         | Control bit        | POOUT0            | POOUT2  | POOUT3            | POOUT5  | P1OUT0                | P1OUT1                | P1OUT2                | P1OUT3                | P1OUT4                | P3OUT0           | P3OUT2            |
|                                     | Register (address) | POOUT (X'03F10')  |         |                   |         |                       | P1OUT (X'03F11')      |                       |                       |                       | P3OUT (X'03F13') |                   |
| Port input                          | Control bit        | POIN0             | POIN2   | POIN3             | POIN5   | P1IN0                 | P1IN1                 | P1IN2                 | P1IN3                 | P1IN4                 | P3IN0            | P3IN2             |
|                                     | Register (address) | POIN (X'03F20')   |         |                   |         |                       | P1IN (X'03F21')       |                       |                       |                       | P3IN (X'03F23')  |                   |
| Output format control               | Control bit        | SC0SBOM           | SC0SBTM | SC1SBOM           | SC1SBTM |                       |                       |                       |                       |                       | SC2SBOM          | SC2SBTM           |
|                                     | Register (address) | SC0MD3 (X'03F53') |         | SC1MD1 (X'03F58') |         |                       |                       |                       |                       |                       |                  | SC2MD1 (X'03F5B') |
| Special function input              | Special function   |                   |         |                   |         | TM0IO                 | TM1IO                 | TM2IO                 | TM3IO                 | TM4IO                 |                  |                   |
| Special function output control (1) | Special function   | SB00(TXD)         | SB10    | SB01              | SB11    | Special function PORT | Special function PORT | Special function PORT | Special function PORT | Special function PORT | SBO2             | SBT2              |
|                                     | Register (address) | SC0SBOS           |         | SC1SBOS           |         | P10TCO                | P11TCO                | P12TCO                | P13TCO                | P14TCO                | SC2SBOS          | SC2SBTS           |
| Special function input              | Special function   |                   |         |                   |         |                       |                       |                       |                       |                       |                  |                   |
| Special function output control (2) | Special function   | SB00(TXD)         |         |                   |         | Special function PORT |                       |                       |                       |                       |                  |                   |
|                                     | Register (address) | SC0CMD            |         |                   |         | RMCTR (X'3F89)        |                       |                       |                       |                       |                  |                   |

\* The TM0RM flag of the RMCTR register is used to switch between remote control output and timer output.

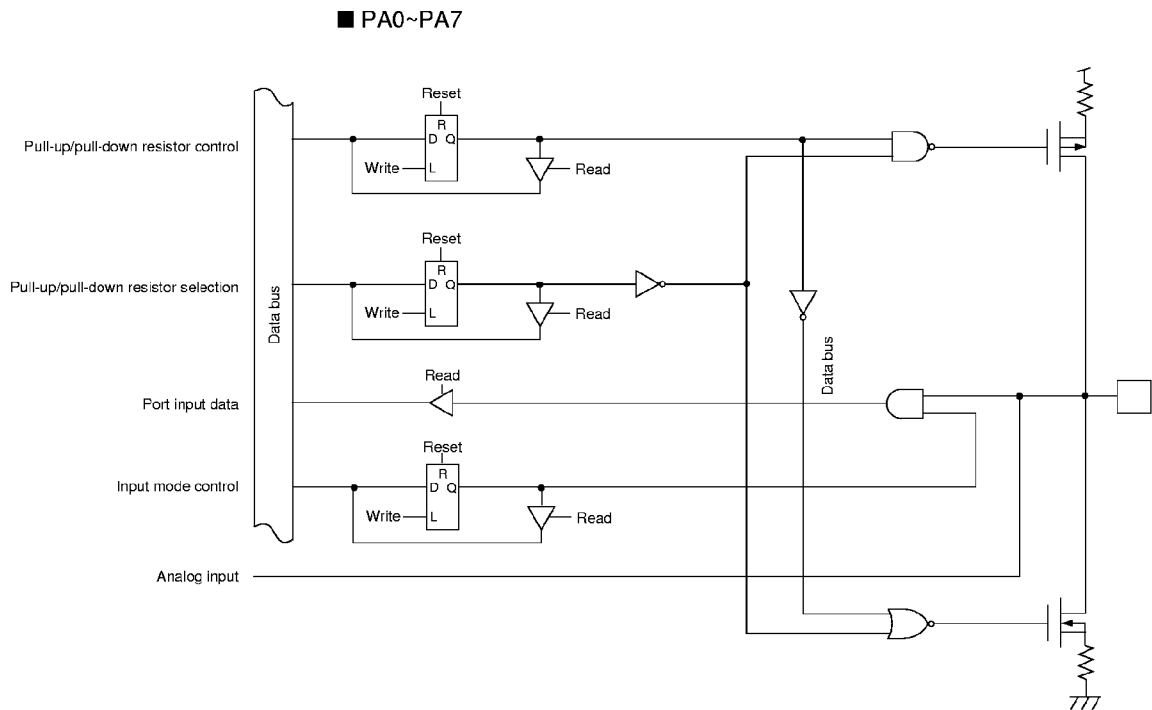
Figure 3-3-1 Configuration and Functions of P00, P02, P03, P05, P10~P14, P30, P32

■ P01,P04,P06,P31



|                                     |                    | P01              | P04    | P06               | P31              |
|-------------------------------------|--------------------|------------------|--------|-------------------|------------------|
| Pull-up resistor control            | Control bit        | P0PLU1           | P0PLU4 | P0PLU6            | P3PLU1           |
|                                     | Register (address) | P0PLU (X'03F40') |        |                   | P3PLU (X'03F43') |
| I/O direction control               | Control bit        | P0DIR1           | P0DIR4 | P0DIR6            | P3DIR1           |
|                                     | Register (address) | P0DIR (X'03F30') |        |                   | P3DIR (X'03F33') |
| Port output                         | Control bit        | P0OUT1           | P0OUT4 | P0OUT6            | P3OUT1           |
|                                     | Register (address) | P0OUT (X'03F10') |        |                   | P3OUT (X'03F13') |
| Port input                          | Control bit        | P0IN1            | P0IN4  | P0IN6             | P3IN1            |
|                                     | Register (address) | P0IN (X'03F20')  |        |                   | P3IN (X'03F23')  |
| Special function input              | Special function   | SBI0/RXD         | SBI1   | $\overline{DK}$   | SBI2             |
| Special function output control (1) | Special function   | ————             | ————   | BUZZER            | ————             |
|                                     | Control bit        | ————             | ————   | BUZZOE            | ————             |
|                                     | Register (address) | ————             | ————   | DLYCTR (X'03F03') | ————             |
| Special function input              | Special function   |                  |        |                   |                  |
| Special function output control (2) | Special function   |                  |        |                   |                  |
|                                     | Control bit        |                  |        |                   |                  |
|                                     | Register (address) |                  |        |                   |                  |

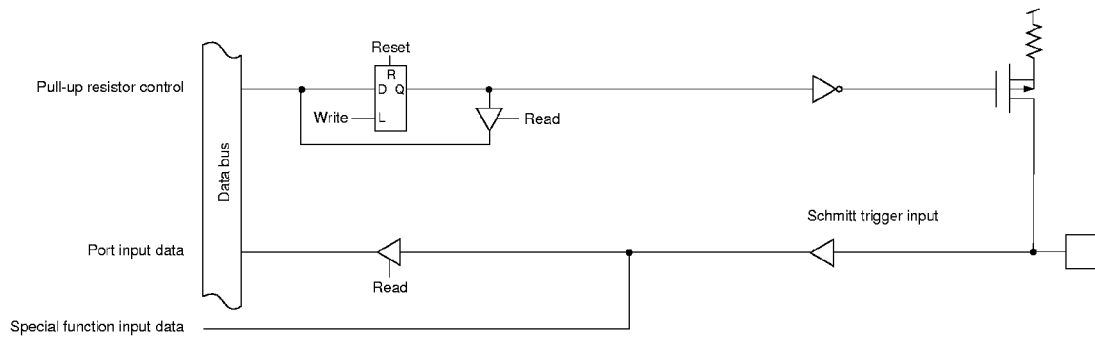
Figure 3-3-2 Configuration and Functions of P01, P04, P06, P31



|                                    |                    | PA0               | PA1     | PA2     | PA3     | PA4     | PA5     | PA6     | PA7     |
|------------------------------------|--------------------|-------------------|---------|---------|---------|---------|---------|---------|---------|
| Pull-up resistor control           | Control bit        | PAPLUD0           | PAPLUD1 | PAPLUD2 | PAPLUD3 | PAPLUD4 | PAPLUD5 | PAPLUD6 | PAPLUD7 |
|                                    | Register (address) | PAPLUD (X'03F4A') |         |         |         |         |         |         |         |
| Pull-up/pull-down resistor control | Control bit        | PARDWN            |         |         |         |         |         |         |         |
|                                    | Register (address) | FLOAT1 (X'03F4B') |         |         |         |         |         |         |         |
| Input mode control                 | Control bit        | PAAIN0            | PAAIN1  | PAAIN2  | PAAIN3  | PAAIN4  | PAAIN5  | PAAIN6  | PAAIN7  |
|                                    | Register (address) | PAIMD (X'03F3A')  |         |         |         |         |         |         |         |
| Port input                         | Control bit        | PAIN0             | PAIN1   | PAIN2   | PAIN3   | PAIN4   | PAIN5   | PAIN6   | PAIN7   |
|                                    | Register (address) | PAIN (X'03F2A')   |         |         |         |         |         |         |         |
| Special function input             | Special function   | AN0               | AN1     | AN2     | AN3     | AN4     | AN5     | AN6     | AN7     |

Figure 3-3-3 Configuration and Functions of PA0~PA7

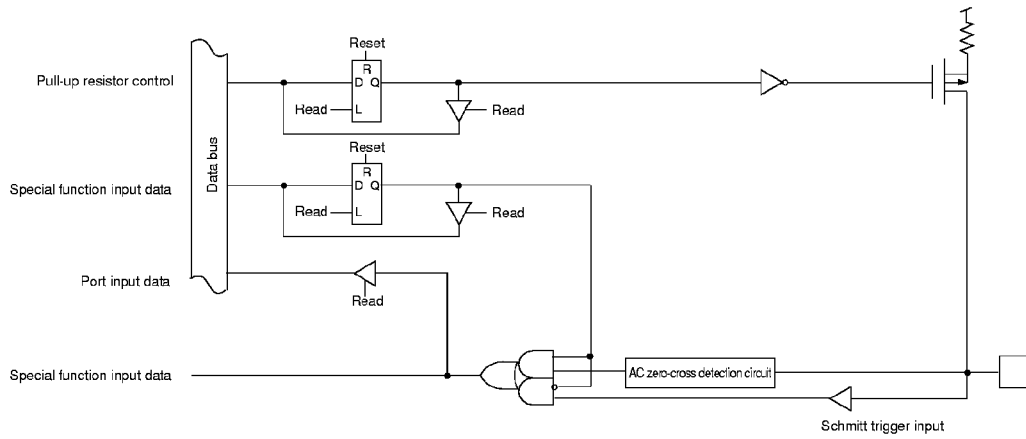
■ Pin Configuration for P20, P22~P24



|                          |                    | P20              | P22    | P23    | P24    |
|--------------------------|--------------------|------------------|--------|--------|--------|
| Pull-up resistor control | Control bit        | P2PLU0           | P2PLU2 | P2PLU3 | P2PLU4 |
|                          | Register (address) | P2PLU (x'03F42') |        |        |        |
| Port input               | Control bit        | P2IN0            | P2IN2  | P2IN3  | P2IN4  |
|                          | Register (address) | P2IN (x'03F22')  |        |        |        |
| Special function input   | Interrupt input    | IRQ0             | IRQ2   | IRQ3   | IRQ4   |

Figure 3-3-4 Configuration and Functions of P20, P22~P24

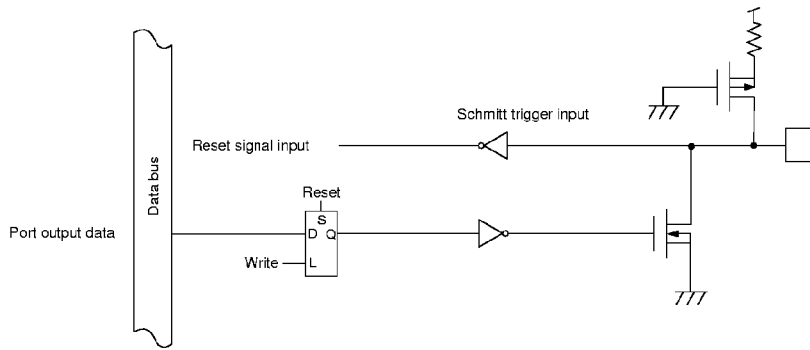
■ P21



|                                  |                    | P21               |
|----------------------------------|--------------------|-------------------|
| Pull-up resistor control         | Control bit        | P2PLU1            |
|                                  | Register (address) | P2PLU (x'03F42')  |
| Port input                       | Control bit        | P2IN1             |
|                                  | Register (address) | P2IN (x'03F22')   |
| Special function input selection | Special function   | SENS              |
|                                  | Control bit        | P2IIM             |
|                                  | Register (address) | FLOAT1 (x'03F4B') |

Figure 3-3-5 Configuration and Functions of P21

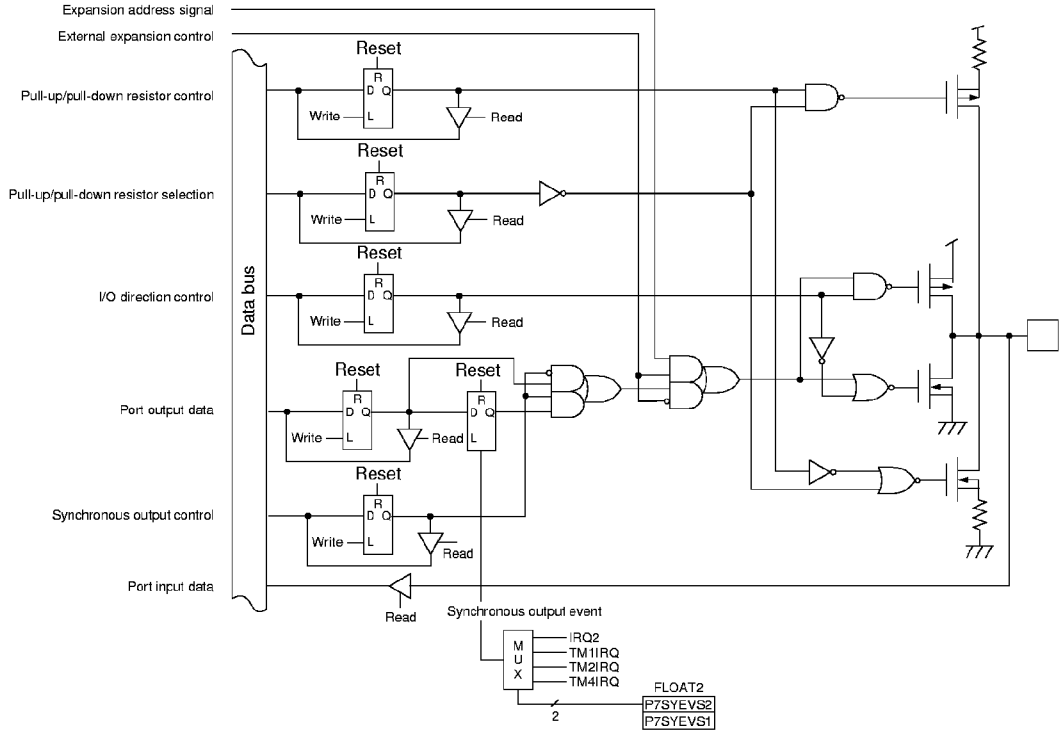
■ P27



|                         |                    |                   |
|-------------------------|--------------------|-------------------|
|                         |                    | P27               |
| Special input           |                    | $\overline{RST}$  |
| Special function output | Special function   | Soft reset output |
|                         | Control bit        | P2OUT7            |
|                         | Register (address) | P2OUT (x'03F12')  |

Figure 3-3-6 Configuration and Functions of P27

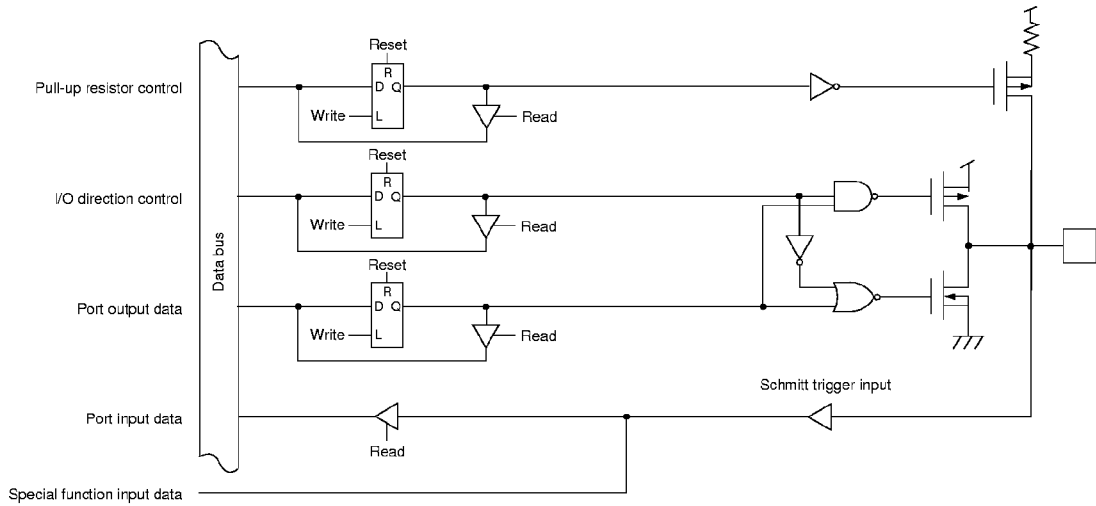
■ P70~P77



|  |                       | P70                     | P71     | P72     | P73     | P74     | P75     | P76     | P77     |
|--|-----------------------|-------------------------|---------|---------|---------|---------|---------|---------|---------|
| Pull-up/<br>pull-down<br>resistor control    | Control bit           | P7PLUD0                 | P7PLUD1 | P7PLUD2 | P7PLUD3 | P7PLUD4 | P7PLUD5 | P7PLUD6 | P7PLUD7 |
|  | Register<br>(address) | P7PLUD<br>(X'03F47')    |         |         |         |         |         |         |         |
| Pull-up/<br>pull-down<br>resistor control    | Control bit           | P7RDWN                  |         |         |         |         |         |         |         |
|  | Register<br>(address) | FLOAT1<br>(X'03F4B')    |         |         |         |         |         |         |         |
| I/O direction<br>control                     | Control bit           | P7DIR0                  | P7DIR1  | P7DIR2  | P7DIR3  | P7DIR4  | P7DIR5  | P7DIR6  | P7DIR7  |
|  | Register<br>(address) | P7DIR<br>(X'03F37')     |         |         |         |         |         |         |         |
| Port input                                   | Control bit           | P7IN0                   | P7IN1   | P7IN2   | P7IN3   | P7IN4   | P7IN5   | P7IN6   | P7IN7   |
|  | Register<br>(address) | P7IN<br>(X'03F27')      |         |         |         |         |         |         |         |
| Port output                                  | Control bit           | P7OU10                  | P7OU11  | P7OUT2  | P7OUT3  | P7OU14  | P7OU15  | P7OU16  | P7OU17  |
|  | Register<br>(address) | P7OUT<br>(X'03F17')     |         |         |         |         |         |         |         |
| Special<br>function<br>output<br>control (1) | Special function      | PORT/Synchronous output |         |         |         |         |         |         |         |
|  | Control bit           | SYSDM0                  | SYSDM1  | SYSDM2  | SYSDM3  | SYSDM4  | SYSDM5  | SYSDM6  | SYSDM7  |
|  | Register<br>(address) | SYSDM<br>(X'03F1F')     |         |         |         |         |         |         |         |
| Special<br>function<br>output<br>control (2) | Special function      | A8                      | A9      | A10     | A11     | A12     | A13     | A14     | A15     |
|  | Control bit           | MMOD pin                |         |         |         |         |         |         |         |

Figure 3-3-7 Configuration and Functions of P70~P77

■ P33,P35,P36,P40~P47

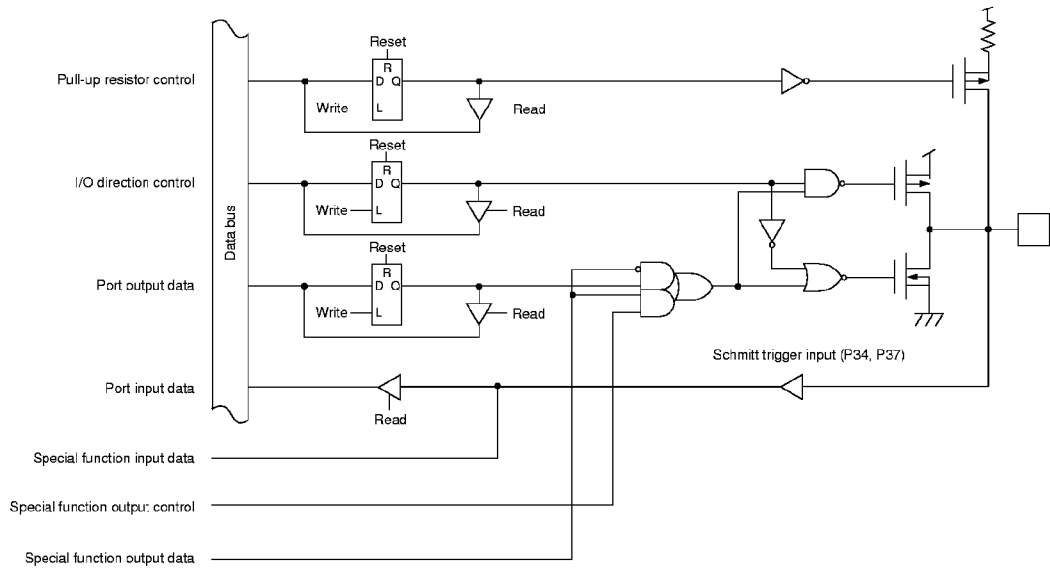


|                                     |                    | P33                | P35    | P36                   | P40              | P41                   | P42    | P43                   | P44    | P45                   | P46    | P47    |
|-------------------------------------|--------------------|--------------------|--------|-----------------------|------------------|-----------------------|--------|-----------------------|--------|-----------------------|--------|--------|
| Pull-up resistor control            | Control bit        | P3PLU3             | P3PLU5 | P3PLU6                | P4PLU0           | P4PLU1                | P4PLU2 | P4PLU3                | P4PLU4 | P4PLU5                | P4PLU6 | P4PLU7 |
|                                     | Register (address) | P3PLU (x'03F43')   |        |                       | P4PLU (X'03F44') |                       |        |                       |        |                       |        |        |
| I/O direction control               | Control bit        | P3DIR3             | P3DIR5 | P3DIR6                | P4DIR0           | P4DIR1                | P4DIR2 | P4DIR3                | P4DIR4 | P4DIR5                | P4DIR6 | P4DIR7 |
|                                     | Register (address) | P3DIR (x'03F33')   |        |                       | P4DIR (X'03F34') |                       |        |                       |        |                       |        |        |
| Port output                         | Control bit        | P3OUT3             | P3OUT5 | P3OUT6                | P4OUT0           | P4OUT1                | P4OUT2 | P4OUT3                | P4OUT4 | P4OUT5                | P4OUT6 | P4OUT7 |
|                                     | Register (address) | P3OUT (x'03F13')   |        |                       | P4OUT (X'03F14') |                       |        |                       |        |                       |        |        |
| Port input                          | Control bit        | P3IN3              | P3IN5  | P3IN6                 | P4IN0            | P4IN1                 | P4IN2  | P4IN3                 | P4IN4  | P4IN5                 | P4IN6  | P4IN7  |
|                                     | Register (address) | P3IN (x'03F23')    |        |                       | P4IN (X'03F24')  |                       |        |                       |        |                       |        |        |
| Special function input              | Special function   | BR                 | LDDMA  | STDMA                 | KEY0             | KEY1                  | KEY2   | KEY3                  | KEY4   | KEY5                  | KEY6   | KEY7   |
| Special function output control (1) | Special function   | Key interrupt/IRQ4 |        |                       |                  |                       |        |                       |        |                       |        |        |
|                                     | Control bit        | IRQ4SEL            |        |                       |                  |                       |        |                       |        |                       |        |        |
|                                     | Register (address) | P4IMD (x'03F3C')   |        |                       |                  |                       |        |                       |        |                       |        |        |
| Special function output control (2) | Special function   | —                  |        | Special function/PORT |                  | Special function/PORT |        | Special function/PORT |        | Special function/PORT |        |        |
|                                     | Control bit        | —                  |        | P4KYEN1               |                  | P4KYEN2               |        | P4KYEN3               |        | P4KYEN4               |        |        |
|                                     | Register (address) | —                  |        | P4IMD (x'03F3C')      |                  |                       |        |                       |        |                       |        |        |

Figure 3-3-8 Configuration and Functions of P33, P35, P36, P40~P47



■ P34,P37,P50~P54,P60~P67,P80~P87



|                                 |                    | P34              | P37    | P50              | P51             | P52             | P53    | P54    |
|---------------------------------|--------------------|------------------|--------|------------------|-----------------|-----------------|--------|--------|
| Pull-up resistor control        | Control bit        | P3PLU4           | P3PLU7 | P5PLU0           | P5PLU1          | P5PLU2          | P5PLU3 | P5PLU4 |
|                                 | Register (address) | P3PLU (x'03F43') |        | P5PLU (x'03F45') |                 |                 |        |        |
| I/O direction control           | Control bit        | P3DIR4           | P3DIR7 | P5DIR0           | P5DIR1          | P5DIR2          | P5DIR3 | P5DIR4 |
|                                 | Register (address) | P3DIR (x'03F33') |        | P5DIR (x'03F35') |                 |                 |        |        |
| Port output                     | Control bit        | P3OUT4           | P3OUT7 | P5OUT0           | P5OUT1          | P5OUT2          | P5OUT3 | P5OUT4 |
|                                 | Register (address) | P3OUT (x'03F13') |        | P5OUT (x'03F15') |                 |                 |        |        |
| Port input                      | Control bit        | P3IN4            | P3IN7  | P5IN0            | P5IN1           | P5IN2           | P5IN3  | P5IN4  |
|                                 | Register (address) | P3IN (x'03F23')  |        | P5IN (x'03F25')  |                 |                 |        |        |
| Special function output control | Special function   | BG               | DKDMA  | $\overline{WE}$  | $\overline{RE}$ | $\overline{CS}$ | A16    | A17    |
|                                 | Control bit        | MMOD pin         |        |                  |                 |                 |        |        |

Figure 3-3-9 Configuration and Functions of P34, P37, P50~P54

|                                 |                    | P60                 | P61    | P62    | P63    | P64    | P65    | P66    | P67    |
|---------------------------------|--------------------|---------------------|--------|--------|--------|--------|--------|--------|--------|
| Pull-up resistor control        | Control bit        | P6PLU0              | P6PLU1 | P6PLU2 | P6PLU3 | P6PLU4 | P6PLU5 | P6PLU6 | P6PLU7 |
|                                 | Register (address) | P6PLU<br>(x'03F46') |        |        |        |        |        |        |        |
| I/O direction control           | Control bit        | P6DIR0              | P6DIR1 | P6DIR2 | P6DIR3 | P6DIR4 | P6DIR5 | P6DIR6 | P6DIR7 |
|                                 | Register (address) | P6DIR<br>(x'03F36') |        |        |        |        |        |        |        |
| Port output                     | Control bit        | P6OUT0              | P6OUT1 | P6OUT2 | P6OUT3 | P6OUT4 | P6OUT5 | P6OUT6 | P6OUT7 |
|                                 | Register (address) | P6OUT<br>(x'03F16') |        |        |        |        |        |        |        |
| Port input                      | Control bit        | P6IN0               | P6IN1  | P6IN2  | P6IN3  | P6IN4  | P6IN5  | P6IN6  | P6IN7  |
|                                 | Register (address) | P6IN<br>(x'03F26')  |        |        |        |        |        |        |        |
| Special function output control | Special function   | A0                  | A1     | A2     | A3     | A4     | A5     | A6     | A7     |
|                                 | Control bit        | MMOD pin            |        |        |        |        |        |        |        |

Figure 3-3-10 Configuration and Functions of P60~67

|                                 |                    | P80                 | P81    | P82    | P83    | P84    | P85    | P86    | P87    |
|---------------------------------|--------------------|---------------------|--------|--------|--------|--------|--------|--------|--------|
| Pull-up resistor control        | Control bit        | P8PLU0              | P8PLU1 | P8PLU2 | P8PLU3 | P8PLU4 | P8PLU5 | P8PLU6 | P8PLU7 |
|                                 | Register (address) | P8PLU<br>(x'03F48') |        |        |        |        |        |        |        |
| I/O direction control           | Control bit        | P8DIR0              | P8DIR1 | P8DIR2 | P8DIR3 | P8DIR4 | P8DIR5 | P8DIR6 | P8DIR7 |
|                                 | Register (address) | P8DIR<br>(x'03F38') |        |        |        |        |        |        |        |
| Port output                     | Control bit        | P8OUT0              | P8OUT1 | P8OUT2 | P8OUT3 | P8OUT4 | P8OUT5 | P8OUT6 | P8OUT7 |
|                                 | Register (address) | P8OUT<br>(x'03F18') |        |        |        |        |        |        |        |
| Port input                      | Control bit        | P8IN0               | P8IN1  | P8IN2  | P8IN3  | P8IN4  | P8IN5  | P8IN6  | P8IN7  |
|                                 | Register (address) | P8IN<br>(x'03F28')  |        |        |        |        |        |        |        |
| Special function output control | Special function   | D0                  | D1     | D2     | D3     | D4     | D5     | D6     | D7     |
|                                 | Control bit        | MMOD pin            |        |        |        |        |        |        |        |

Figure 3-3-11 Configuration and Functions of P80~P87



Chapter 4 Timer Functions



## 4-1 Overview

The MN101C01D contains five 8-bit timers, one 16-bit timer, a watchdog timer, a time base timer, and circuits for remote control output and buzzer output.

Table 4-1-1 Summary of Timer Functions

|                                      | Timer 0<br>(8-bit)                      | Timer 1<br>(8-bit) | Timer 2<br>(8-bit) | Timer 3<br>(8-bit)                      | Timer 4<br>(16-bit)  | Timer 5<br>(8-bit)                  | Time Base                |
|--------------------------------------|---|--------------------|--------------------|---|----------------------|-------------------------------------|--------------------------|
| Interrupt                            | TM0IRQ                                  | TM1IRQ             | TM2IRQ             | TM3IRQ                                  | TM4IRQ               | TM5IRQ                              | TBIRQ                    |
| Timer operation                      | ✓                                       | ✓                  | ✓                  | ✓                                       | ✓                    | ✓                                   | ✓                        |
| Event counter                        | ✓                                       | ✓                  | ✓                  | ✓                                       | ✓                    | —                                   | —                        |
| Timer pulse output                   | ✓                                       | ✓                  | ✓                  | ✓                                       | ✓                    | —                                   | —                        |
| Serial transmission clock            | ✓<br>(SIF2)                             | —                  | —                  | ✓<br>(SIF0,1)                           | —                    | —                                   | —                        |
| Synchronous output timing generation | —                                       | ✓                  | ✓                  | —                                       | ✓                    | —                                   | —                        |
| PWM output                           | ✓                                       | —                  | ✓                  | —                                       | ✓                    | —                                   | —                        |
| Cascade connection                   | ✓                                       |                    | ✓                  |   | —                    | —                                   | —                        |
| Capture function                     | —                                       | —                  | —                  | —                                       | ✓                    | —                                   | —                        |
| Clock source                         | 0                                       | fosc               | fs/16              | fs                                      | fosc                 | fosc                                | fosc                     |
|                                      | 1                                       | fs                 | fs/64              | fs/4                                    | fs/4                 | fs/4                                | fx                       |
|                                      | 2                                       | fs/4               | fx                 | fx                                      | fs/16                | fs/16                               | fx                       |
|                                      | 3                                       | TM0IO input        | TM1IO input        | TM2IO input                             | TM3IO input          | TM4IO input                         | fosc, fx/2 <sup>13</sup> |
| Other                                | Remote control carrier pulse generation |                    |                    | Remote control carrier pulse generation | Pulse added type PWM | Not possible to temporarily halt BC |                          |

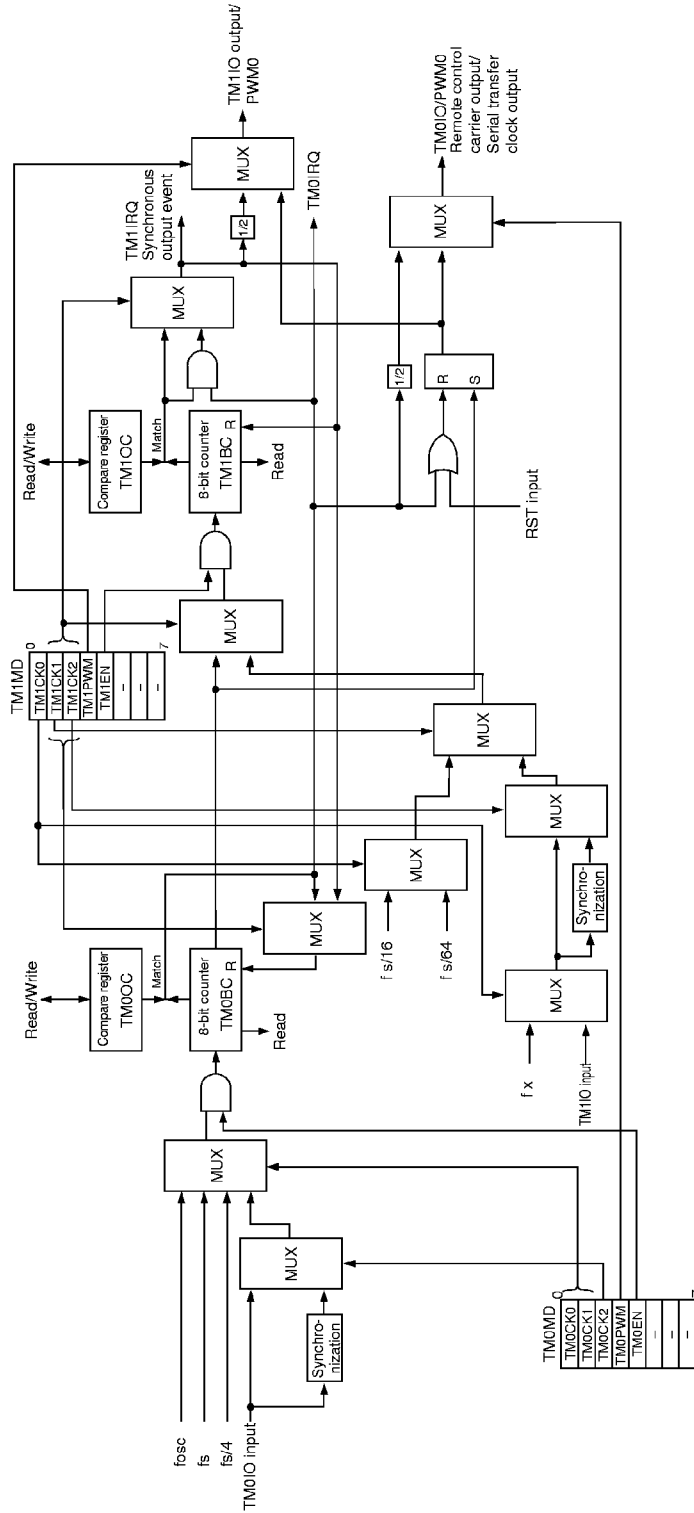
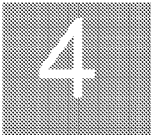


Figure 4-1-1 Timers 0, 1 Block Diagram



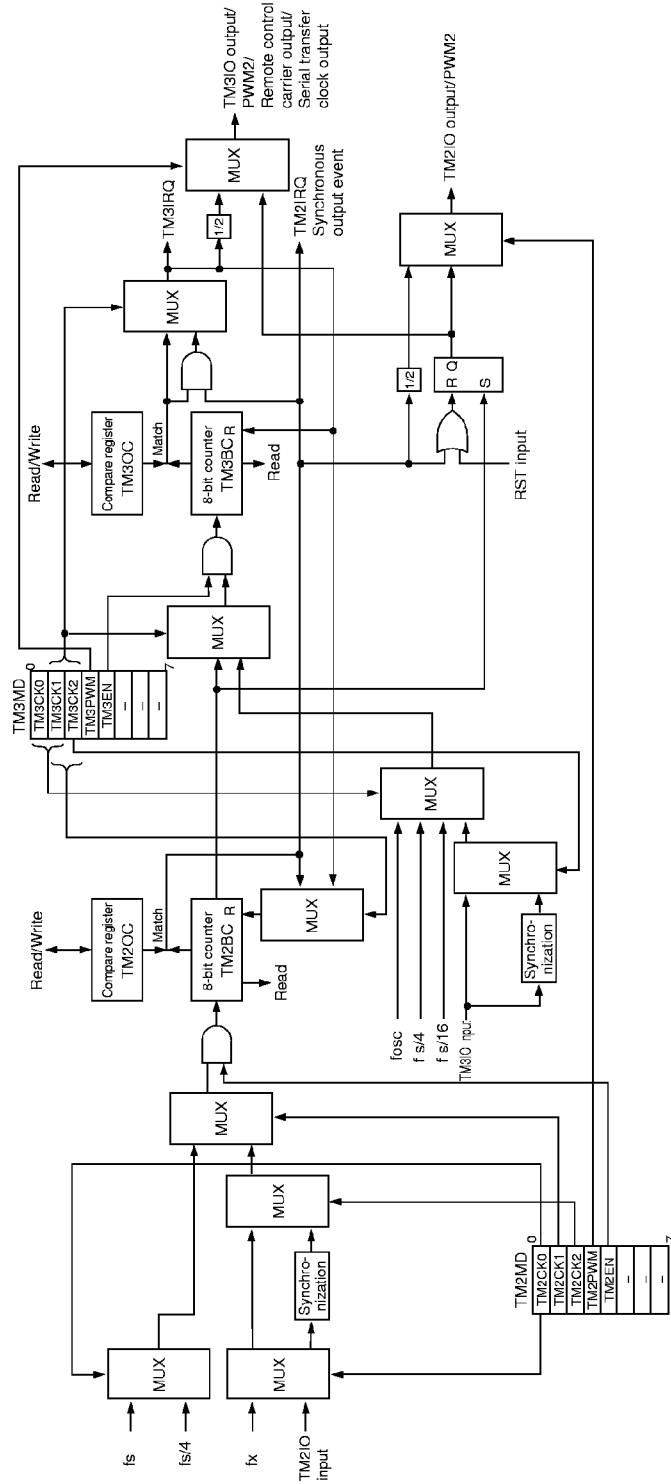


Figure 4-1-2 Timers 2, 3 Block Diagram

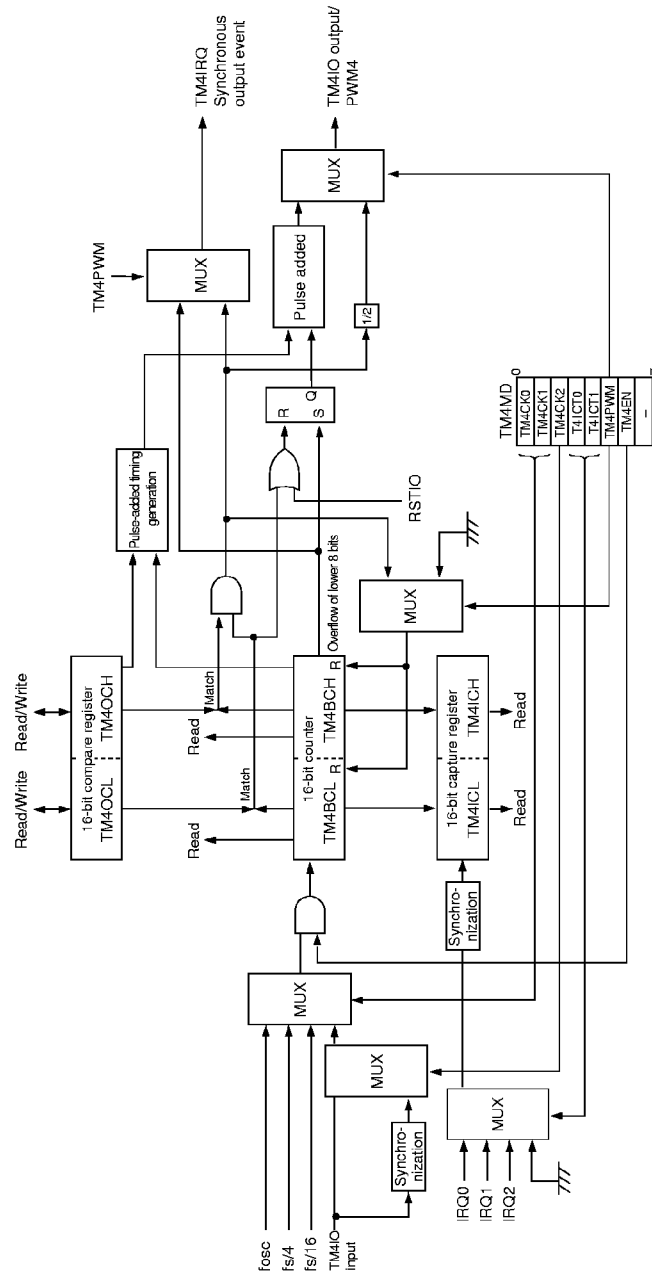


Figure 4-1-3 Timer 4 Block Diagram



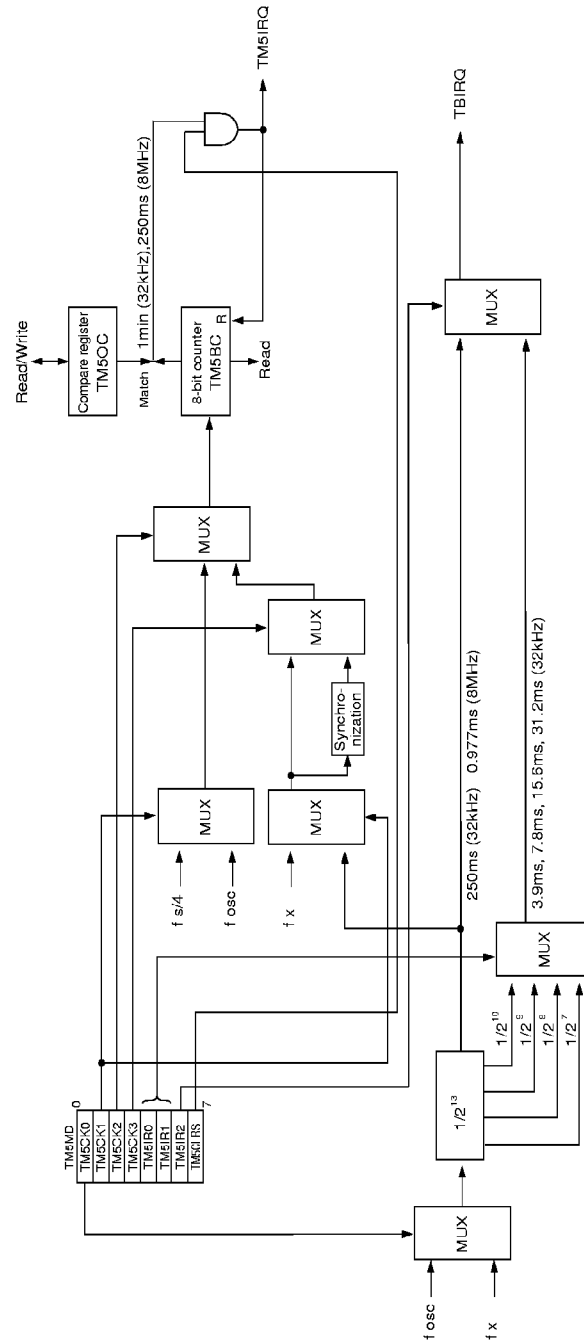


Figure 4-1-4 Timer 5/Time Base Block Diagram

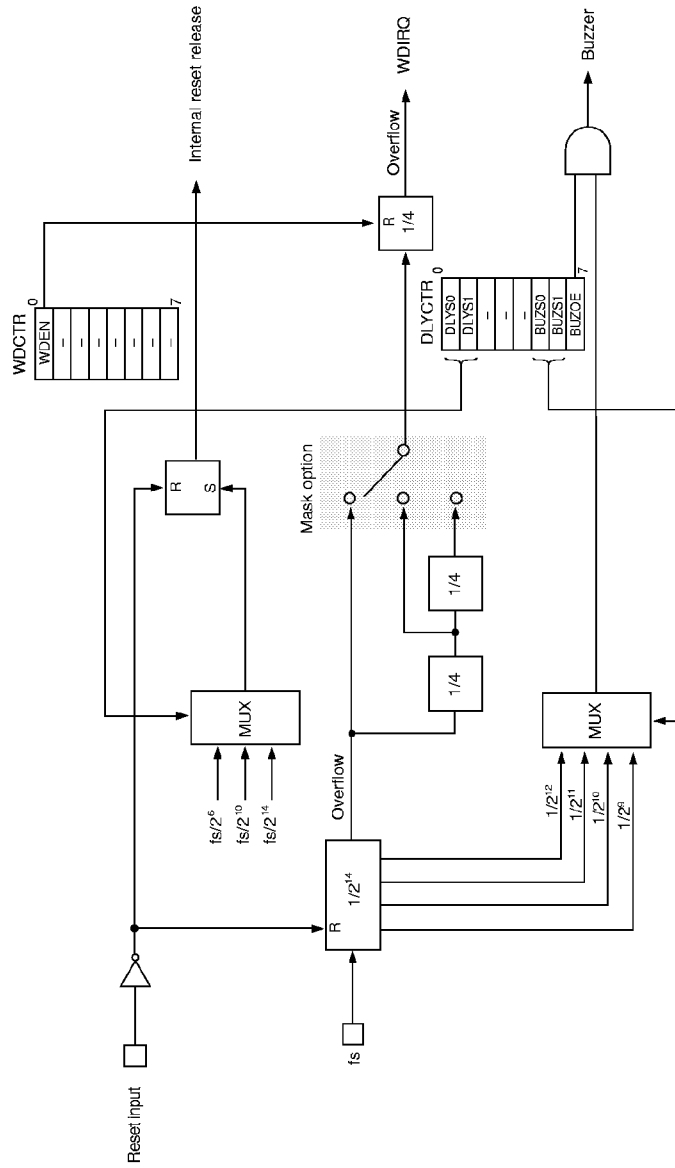


Figure 4-1-5 Watchdog Timer, Buzzer Block Diagram

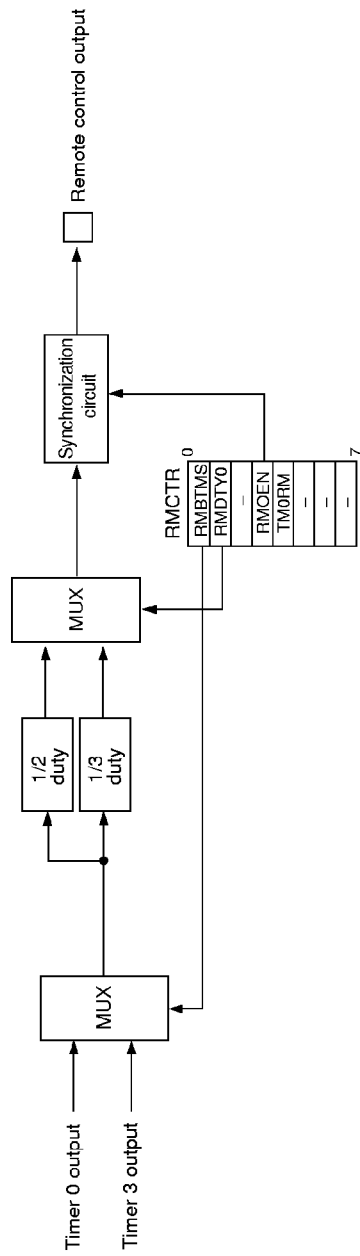


Figure 4-1-6 Remote Control Transmission Block Diagram

## 4-2 8-bit Timer Operation (timers 0, 1)

### 4-2-1 Overview

Functions for timers 0 and 1 are listed below.

Table 4-2-1 Summary of 8-bit Timer Functions

|   | Timer 0<br>(8-bit) | Timer 1<br>(8-bit) |
|---|--------------------|--------------------|
| Interrupt                               | TM0IRQ             | TM1IRQ             |
| Timer operation                         | ✓                  | ✓                  |
| Event counter                           | ✓                  | ✓                  |
| Timer pulse output                      | ✓                  | ✓                  |
| Serial transmission clock               | ✓<br>(SIF2)        | —                  |
| Synchronous output timing generation    | —                  | ✓                  |
| PWM output                              | ✓                  | —                  |
| Cascade connection                      | ✓                  |                    |
| Remote control carrier pulse generation | ✓                  | —                  |

## 4-2-2 Operation

### ■ Timer Operation (timers 0, 1)

*When servicing an interrupt, reset the timer 0 interrupt request flag before starting timer 0.*

*During a count operation, be careful if the value set in TM0OC is smaller than the value of binary counter 0, since the count-up operation will continue until overflow occurs.*

Settings for timer operation are listed below. Timer 0 is used as an example.

- (1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the count operation of timer 0.
- (2) Set the TM0CK2~0 flags of the TM0MD register to select fosc, fs, or fs/4 as the clock source.
- (3) Set the TM0PWM flag of the TM0MD register to "0" so that normal timer operation is selected.
- (4) Set a value in compare register 0 (TM0OC).
- (5) Set the TM0EN flag of the TM0MD register to "1" to start the timer.
- (6) When timer 0 begins operation, binary counter 0 (TM0BC) will count upward from X'00'.
- (7) When the value of binary counter 0 matches that of the TM0OC register, the timer 0 interrupt request flag is set, and the binary counter is reset to X'00' and begins to count upward again.

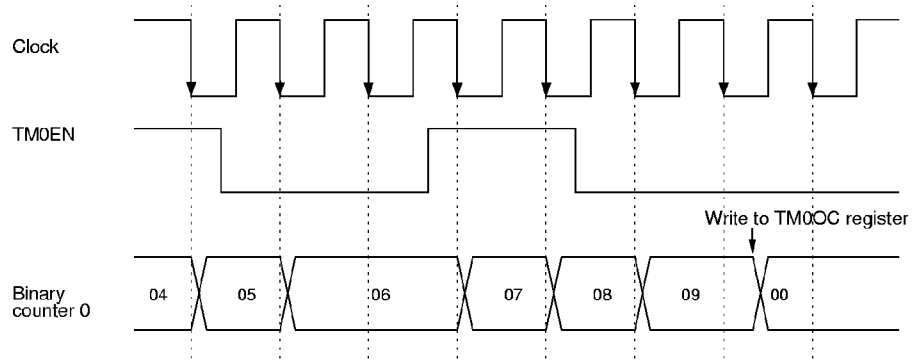


Figure 4-2-1 Binary Counter 0 (TM0BC) Count Timing



**If the TM0EN flag of TM0MD register is changed simultaneously with other bits, the switching operation may cause binary counter 0 to be incremented.**



**If the value of TM0OC register is overwritten while timer 0 has stopped counting, binary counter 0 will be reset to X'00'.**

■ Event Count Function (timers 0, 1)

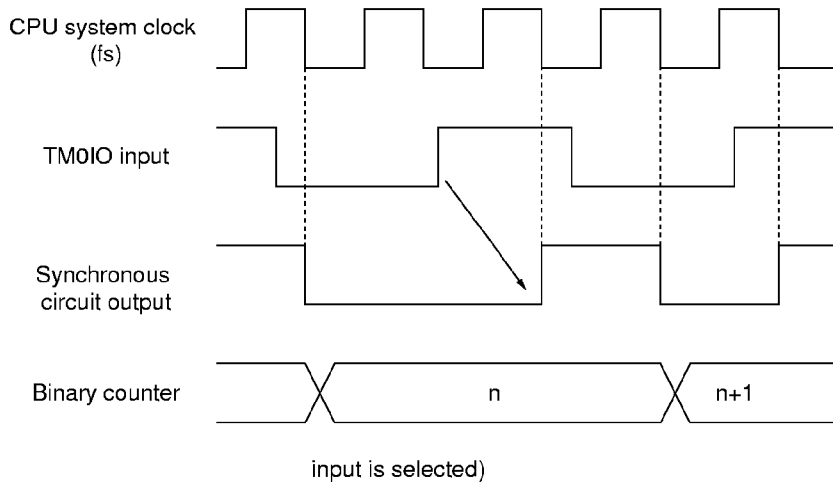
Settings for the event count function are listed below. Timer 0 is used as an example.

- (1) Set the TMOEN flag of the timer 0 mode register (TM0MD) to "0" to stop the count operation of timer 0.
- (2) Use the TMOCK2~0 flags of the TM0MD register to select TM0IO input or synchronous TM0IO input as the clock source.
- (3) Set the TMO PWM flag of the TM0MD register to "0" so that normal timer operation is selected.
- (4) Set a value in compare register 0 (TM0OC).
- (5) Set the TMOEN flag of the TM0MD register to "1" to start the timer.
- (6) When timer 0 begins operation, binary counter 0 will count upward from X'00'.
- (7) When the value of binary counter 0 matches that of the TM0OC register, the timer 0 interrupt request flag is set, and the binary counter 0 is reset to X'00' and begins to count upward again.

*If TM0IO input is selected as the clock source and the value of binary counter 0 is to be read during operation, select synchronous TM0IO input to avoid reading data that may be incomplete during count-up transitions. However, with synchronous TM0IO input, it is not possible to return from STOP/HALT modes.*

When synchronous TM0IO is selected, the timer 0 clock source is synchronized with the system clock after a transition of the TM0IO input signal. Binary counter 0 counts upward based on a signal synchronized to the system clock. Therefore, correct values can be read from binary counter 0.

Figure 4-2-2 Timer 0 Event Counter Timing (when synchronous TM0IO



The period of a signal output to the port is 1/2 of the period set in the TM0OC register.

If port 1 is to be used as a pulse output pin, it is necessary to set the port 1 output direction control register (P1DIR) and the port 1 pull-up/pull-down resistor control register (P1PLU).

■ Timer Pulse Output Function (timers 0, 1)

Settings for the timer pulse output function are listed below. Timer 0 is used as an example.

- (1) Set the 'TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the count operation of timer 0.
- (2) Set bit 0 of the port 1 output/input mode register (P1OMD) to "1" to set the special function pin. Bit 0 of port 1 will be the pulse output pin.
- (3) Set the TM0CK2~0 flags of the TM0MD register to select fosc, fs, or fs/4 as the clock source.
- (4) Set the TM0PWM flag of the TM0MD register to "0" so that normal timer operation is selected.
- (5) Set a value in compare register 0 (TM0OC).
- (6) Set the 'TM0EN flag of the TM0MD register to "1" to start the timer.
- (7) When timer 0 begins operation, binary counter 0 will count upward from X'00'.
- (8) When the value of binary counter 0 matches that of the TM0OC register, the timer 0 interrupt request flag is set, and the binary counter 0 is reset to X'00' and begins to count upward again.

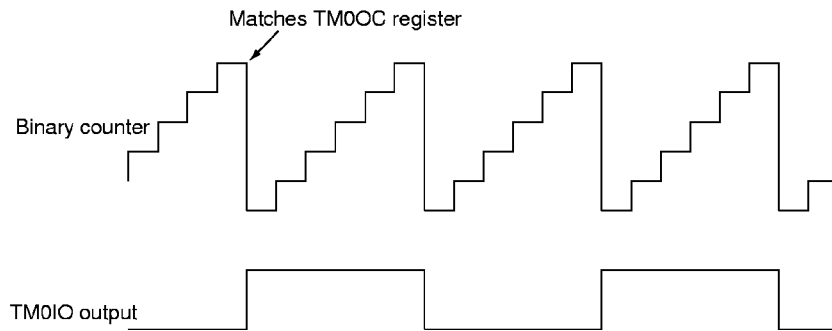


Figure 4-2-3 Timer Pulse Output Timing

#### ■ Synchronous Output Timing Generation Function (timer 1)

Settings for the synchronous output timing generation function are listed below.

- (1) Set the TM1EN flag of the timer 1 mode register (TM1MD) to "0" so that the count operation of timer 1 is stopped.
- (2) Set the P7SYEVS2 and P7SYEVS1 flags of pin control register 2 (FLOAT2) to select timer 1 interrupts.
- (3) Set the synchronous output control register (SYSMD) to configure port 7 bits for use as synchronous output pins.
- (4) Set the TM1CK2~0 flags of the TM1MD register to select fs/16, fs/64, fx or synchronous fx as the clock source.
- (5) Set the TM1PWM flag of the TM1MD register to "0" so that normal timer operation is selected.
- (6) Set a value in compare register 1 (TM1OC).
- (7) Set the TM1EN flag of the TM1MD register to "1" to start the timer.
- (8) When timer 1 begins operation, binary counter 1 will count upward from X'00'.
- (9) When the value of binary counter 1 matches that of the TM1OC register, the timer 1 interrupt request flag is set, binary counter 1 is reset to X'00' and begins to count upward again.
- (10) At the timing when the value of binary counter 1 matches that of the TM1OC register, the values at port 7 synchronous output pins will change.



If the *TM1PWM* flag of the *TM1MD* register is set to "1" and timer 0 PWM output is selected, the PWM output of timer 0 will also be output from the *TM1IO* pin.

If port 1 is to be used as a PWM output pin, the *P1DIR* and *P1PLU* registers must be set.

■ PWM Output Function (Timer 0)

Settings for the PWM output function are listed below.

- (1) Set the *TM0EN* flag of the timer 0 mode register (*TM0MD*) to "0" to stop the count operation of timer 0.
- (2) Set bit 0 of the port 1 output/input mode register (*PIOMD*) to the special function pin setting. Bit 0 of port 1 will be the PWM output pin.
- (3) Set the *TM0CK2~0* flags of the *TM0MD* register to select *fosc*, *fs*, or *fs/4* as the clock source. The period of the output waveform is determined based on the clock source.
- (4) Set the *TM0PWM* flag of the *TM0MD* register to "1" so that PWM operation is selected.
- (5) Set a value in compare register 0 (*TM0OC*). The high interval of the output waveform is determined based on the value of the *TM0OC* compare register.
- (6) Set the *TM0EN* flag of the *TM0MD* register to "1" to start the timer.
- (7) When timer 0 begins operation, binary counter 0 will count upward from X'00'.
- (8) A high-level signal is output from the port beginning when binary counter 0 starts counting at X'00' and ending when the value of binary counter 0 matches the value set in the *TM0OC* register.
- (9) When the value of binary counter 0 matches that of the *TM0OC* register, a low-level signal is output from the port.
- (10) Binary counter 0 continues to count upward until X'FF' is reached. At the next count-up cycle, the value of binary counter 0 is reset to X'00', a high-level signal is output from the port, and counting begins again.

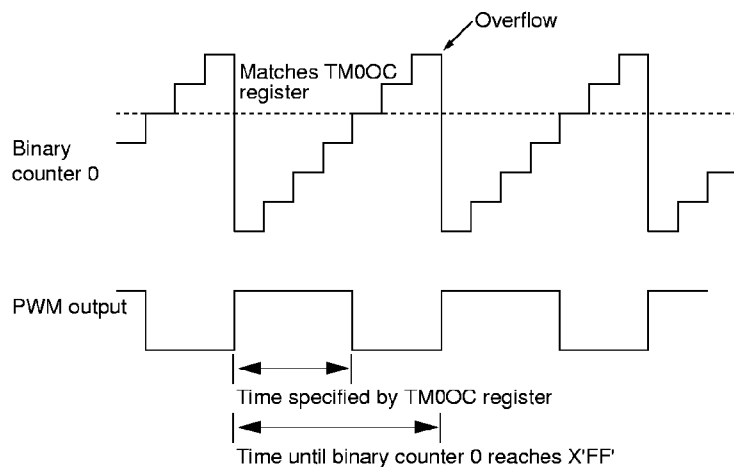


Figure 4-2-4 PWM Output Timing

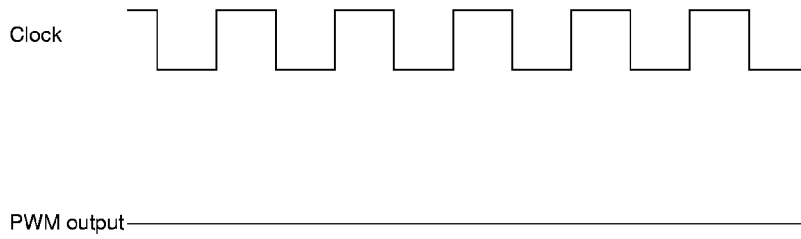


Figure 4-2-5 PWM Output Timing (when TM0OC register is X'00')

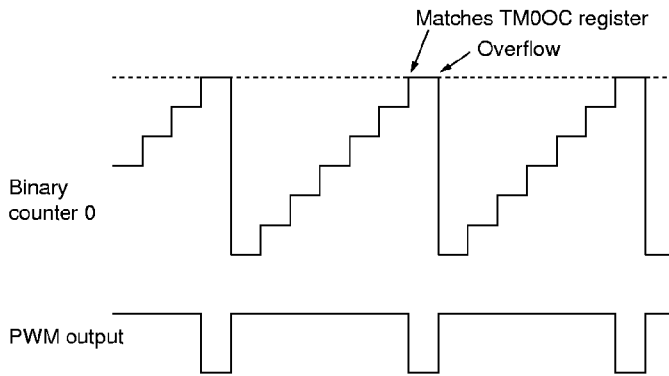


Figure 4-2-6 PWM Output Timing (when TM0OC register is X'FF')

*The serial interface clock source has a frequency that is 1/2 of the overflow output of timer 0.*

*See chapter 5 for serial interface settings, refer to the chapter on serial functions.*

■ Serial Transfer Clock Function (timer 0)

Settings for the serial transfer clock function are listed below.

- (1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the count operation of timer 0.
- (2) Set the SC2CK1 and SC2CK0 flags of the serial interface 2 mode register 1 (SC2MD1) to select 1/2 of the timer 0 overflow frequency as the clock source.
- (3) Set the TM0CK2~0 flags of the TM0MD register to select fosc, fs, or fs/4 as the clock source.
- (4) Set the TM0PWM flag of the TM0MD register to "0" to select normal timer operation.
- (5) Set a value in compare register 0 (TM0OC).
- (6) Set the TM0EN flag of the TM0MD register to "1" to start the timer.
- (7) When timer 0 begins operation, binary counter 0 counts upward from X'00'.
- (8) When the value of binary counter 0 matches that of the TM0OC register, the timer 0 interrupt request flag is set, the value of binary counter 0 is reset to X'00', and counting begins again.

■ Cascade Connection Function (timer 0 + timer 1)

Settings for the cascade connection function are listed below. Timer 0 and timer 1 are connected to operate as a 16-bit timer. Output from the timer is also possible.

- (1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the count operation of timer 0.
- (2) Set the TM1EN flag of the timer 1 mode register (TM1MD) to "0" to stop the count operation of timer 1.
- (3) Set the TM0CK2~0 flags of the TM0MD register to select fosc, fs, or fs/4 as the clock source.
- (4) Use the TM1CK2~0 flags of the TM1MD register to set the clock source as a cascaded connection with timer 0.
- (5) Set the TM0PWM flag of the TM0MD register to "0" to select normal timer operation.
- (6) Set values in compare register 0 (TM0OC) and compare register 1 (TM1OC).
- (7) Set the TM0EN flag of the TM0MD register to "1" to start the timer 0.
- (8) Set the TM1EN flag of the TM1MD register to "1" to start the timer 1.
- (9) When timers 0 and 1 begin operation, the binary counters begin counting upward from X'0000' as a 16-bit counter.
- (10) When the value of the 16-bit binary counter matches that of the 16-bit compare register (TM0OC+TM1OC), the timer 1 interrupt request flag is set, the value of the 16-bit binary counter is reset to X'0000', and counting begins again.

*Disable the timer 0 interrupt.*



**Use a 16-bit access instruction to set the (TM1OC+TM0OC) register.**

## 4-3 8-bit Timer Operation (timers 2, 3)

### 4-3-1 Overview

Functions for timers 2 and 3 are listed below.

Table 4-3-1 Summary of 8-bit Timer Functions

|   | Timer 2<br>(8-bit) | Timer 3<br>(8-bit) |
|---|--------------------|--------------------|
| Interrupt                               | TM2IRQ             | TM3IRQ             |
| Timer operation                         | ✓                  | ✓                  |
| Event counter                           | ✓                  | ✓                  |
| Timer pulse output                      | ✓                  | ✓                  |
| Serial transmission clock               | —                  | ✓<br>(SIF0,1)      |
| Synchronous output timing generation    | ✓                  | —                  |
| PWM output                              | ✓                  | —                  |
| Cascade connection                      | ✓                  |                    |
| Remote control carrier pulse generation | —                  | ✓                  |

When servicing an interrupt, reset the timer 2 interrupt request flag before starting timer 2.

During a count operation, be careful if the value set in TM2OC is smaller than the value of binary counter 2, since the count-up operation will continue until overflow occurs.

If fx is to be selected as the clock source and the value of binary counter 2 is to be read during operation, select synchronized fx in order to avoid reading data that may be incomplete during count-up transitions. However, with synchronized fx, it is not possible to return from STOP/HALT modes.

### 4-3-2 Operation

#### ■ Timer Operation (timers 2, 3)

Settings for timer operation are listed below. Timer 2 is used as an example.

- (1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.
- (2) Set the TM2CK2~0 flags of the TM2MD register to select fs, fs/4, fx, or synchronized fx as the clock source.
- (3) Set the TM2PWM flag of the TM2MD register to "0" so that normal timer operation is selected.
- (4) Set a value in compare register 2 (TM2OC).
- (5) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
- (6) When timer 2 begins operation, binary counter 2 (TM2BC) will count upward from X'00'.
- (7) When the value of binary counter 2 matches that of the TM2OC register, the timer 2 interrupt request flag is set, and the binary counter 2 is reset to X'00' and begins to count upward again.

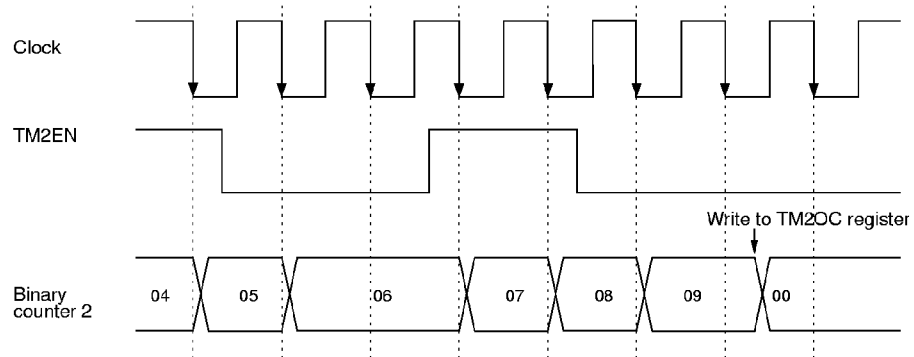


Figure 4-3-1 Binary Counter 2 (TM2BC) Count Timing



If the TM2EN flag of TM2MD register is changed simultaneously with other bits, the switching operation may cause binary counter 2 to be incremented.



If the value of TM2OC register is overwritten while timer 2 has stopped counting, binary counter 2 will be reset to X'00'.

■ Event Count Function (timers 2, 3)

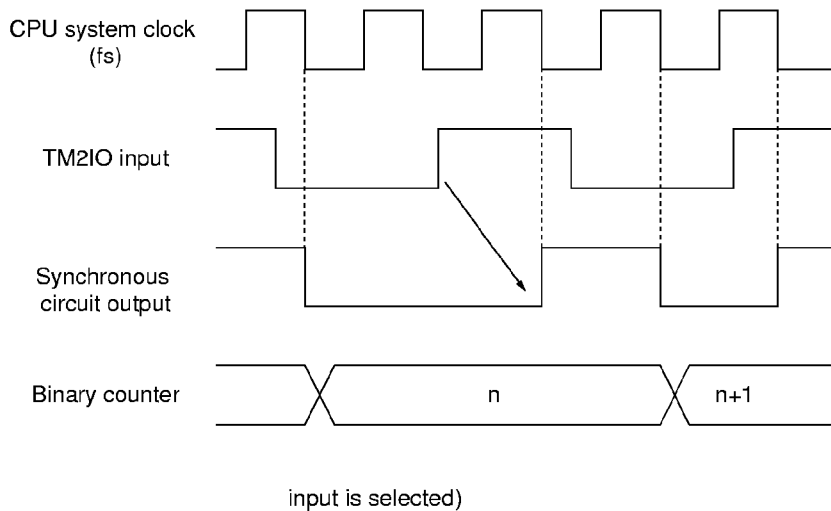
Settings for the event count function are listed below. Timer 2 is used as an example.

- (1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.
- (2) Use the TM2CK2-0 flags of the TM2MD register to select TM2IO input or synchronous TM2IO input as the clock source.
- (3) Set the TM2PWM flag of the TM2MD register to "0" so that normal timer operation is selected.
- (4) Set a value in compare register 2 (TM2OC).
- (5) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
- (6) When timer 2 begins operation, binary counter 2 will count upward from X'00'.
- (7) When the value of binary counter 2 matches that of the TM2OC register, the timer 2 interrupt request flag is set, and the binary counter 2 is reset to X'00' and begins to count upward again.

*If TM2IO input is selected as the clock source and the value of binary counter 2 is to be read during operation, select synchronized TM2IO input to avoid reading data that may be incomplete during count-up transitions. However, with synchronized TM2IO input, it is not possible to return from STOP/HALT modes.*

When synchronized TM2IO is selected, the timer 2 clock source is synchronized with the system clock after a transition of the TM2IO input signal. Binary counter 2 counts upward based on a signal synchronized to the system clock. Therefore, correct values can be read from binary counter 2.

Figure 4-2-2 Timer 2 Event Counter Timing (when synchronous TM2IO



The period of a signal output to the port is 1/2 of the period set in the TM2OC register.

If port 1 is to be used as a pulse output pin, it is necessary to set the port 1 output direction control register (P1DIR) and the port 1 pull-up/pull-down resistor control register (P1PLU).

■ Timer Pulse Output Function (timers 2, 3)

Settings for the timer pulse output function are listed below. Timer 2 is used as an example.

- (1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.
- (2) Set bit 2 of the port 1 output/input mode register (P1OMD) to "1" to set the special function pin. Bit 2 of port 1 will be specified as the pulse output pin.
- (3) Set the TM2CK2~0 flags of the TM2MD register to select fs, fs/4, fx, or synchronized fx as the clock source.
- (4) Set the TM2PWM flag of the TM2MD register to "0" so that normal timer operation is selected.
- (5) Set a value in compare register 2 (TM2OC).
- (6) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
- (7) When timer 2 begins operation, binary counter 2 will count upward from X'00'.
- (8) When the value of binary counter 2 matches that of the TM2OC register, the timer 2 interrupt request flag is set, and the binary counter 2 is reset to X'00' and begins to count upward again.

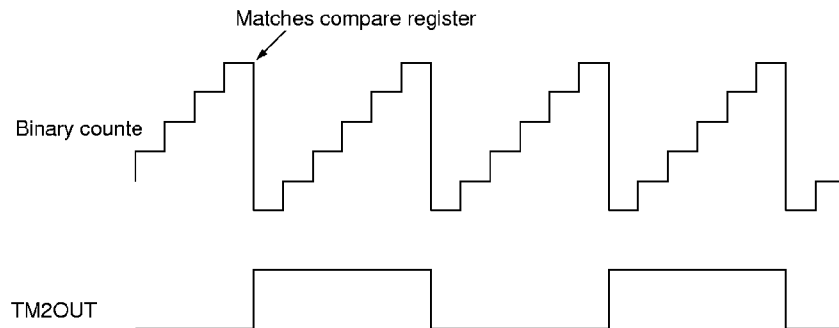


Figure 4-3-3 Timer Pulse Output Timing

### ■ Synchronous Output Timing Generation Function (timer 2)

Settings for the synchronous output timing generation function are listed below.

- (1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" so that the count operation of timer 2 is stopped.
- (2) Set the P7SYEVS2 and P7SYEVS1 flags of pin control register 2 (FLOAT2) to select timer 2 interrupts.
- (3) Set the synchronous output control register (SYSMD) to configure port 7 bits for use as synchronous output pins.
- (4) Set the TM2CK2~0 flags of the TM2MD register to select fs, fs/4, fx or synchronous fx as the clock source.
- (5) Set the TM2PWM flag of the TM2MD register to "0" so that normal timer operation is selected.
- (6) Set a value in compare register 2 (TM2OC).
- (7) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
- (8) When timer 2 begins operation, binary counter 2 will count upward from X'00'.
- (9) When the value of binary counter 2 matches that of the TM2OC register, the timer 2 interrupt request flag is set, binary counter 2 is reset to X'00' and begins to count upward again.
- (10) At the timing when the value of binary counter 2 matches that of the TM2OC register, the values at port 7 synchronous output pins will change.

*If port 7 pins are to be used as pulse output pins, it is necessary to set the P7DIR register and the P7PLUD register.*

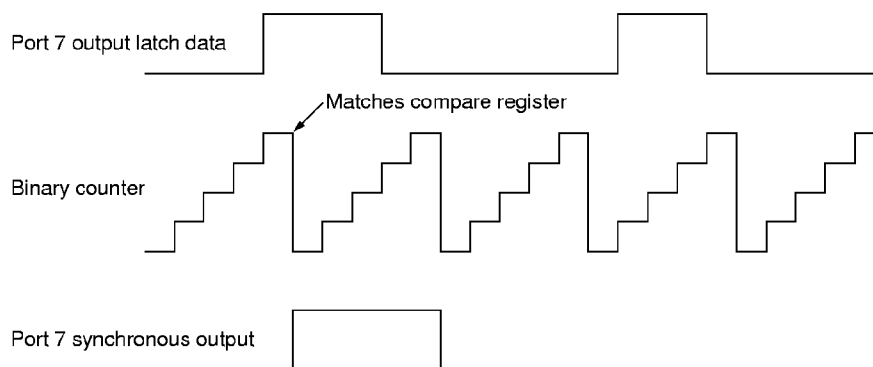


Figure 4-3-4 Port 7 Synchronous Output Timing



If the TM3PWM flag of the TM3MD register is set to "1" and timer 2 PWM output is selected, the PWM output of timer 2 will also be output from the TM3IO pin.

If port 1 is to be used as a PWM output pin, the P1DIR and P1PLU registers must be set.

■ PWM Output Function (Timer 2)

Settings for the PWM output function are listed below.

- (1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 0.
- (2) Set bit 2 of the port 1 output/input mode register (P1OMD) to the special function pin setting. Bit 2 of port 1 will be specified as the PWM output pin.
- (3) Set the TM2CK2~0 flags of the TM2MD register to select fs, fs/4, fx, or synchronous fx as the clock source. The period of the output waveform is determined based on the clock source.
- (4) Set the TM2PWM flag of the TM2MD register to "1" so that PWM operation is selected.
- (5) Set a value in compare register 2 (TM2OC). The high interval of the output waveform is determined based on the value of the TM2OC compare register.
- (6) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
- (7) When timer 2 begins operation, binary counter 2 will count upward from X'00'.
- (8) A high-level signal is output from the port beginning when binary counter 2 starts counting at X'00' and ending when the value of binary counter 2 matches the value set in the TM2OC register.
- (9) When the value of binary counter 2 matches that of the TM2OC register, a low-level signal is output from the port.
- (10) Binary counter 2 continues to count upward until X'FF' is reached. At the next count-up cycle, the value of binary counter 2 is reset to X'00', a high-level signal is output from the port, and counting begins again.

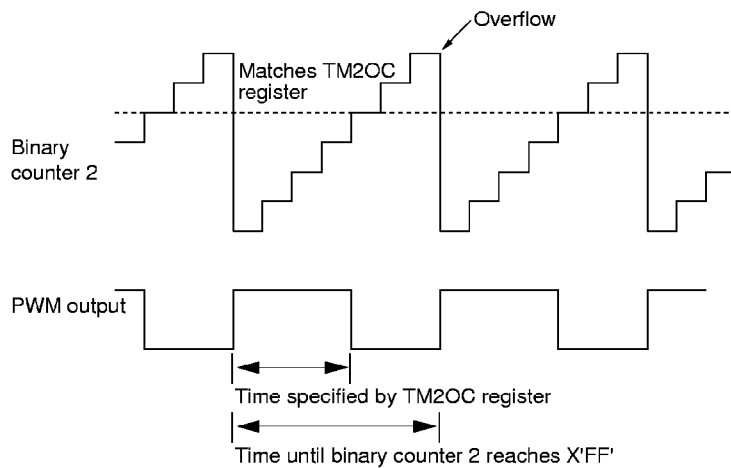


Figure 4-3-5 PWM Output Timing

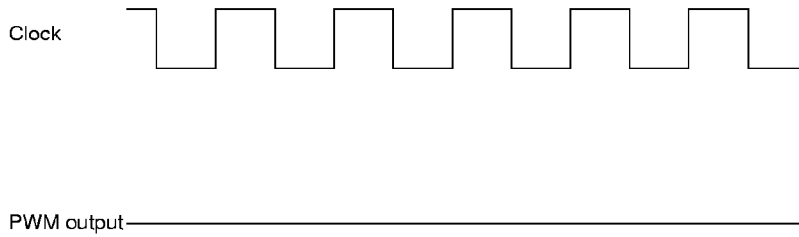


Figure 4-3-6 PWM Output Timing (when TM2OC register is X'00')

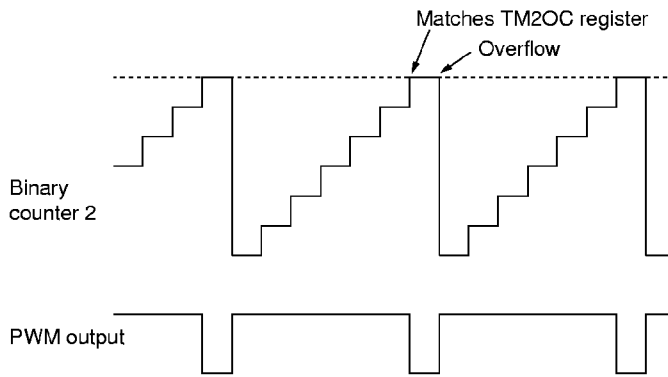


Figure 4-3-7 PWM Output Timing (when TM2OC register is X'FF')

The clock source for the serial interface has a frequency that is 1/2 of the overflow output of timer 3.

For serial interface settings, refer to the chapter on serial functions.

#### ■ Serial Transfer Clock Function (timer 3)

Settings for the serial transfer clock function are listed below.

- (1) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop the count operation of timer 3.
- (2) Set the SC0CK1 and SC0CK0 flags of the serial interface 0 mode register 1 (SC0MD1) to select 1/2 of the timer 3 overflow frequency as the clock source.
- (3) Set the TM3CK2~0 flags of the TM3MD register to select fosc, fs, fs/4, or fs/16 as the clock source.
- (4) Set the TM3PWM flag of the TM3MD register to "0" to select timer 3 output.
- (5) Set a value in compare register 3 (TM3OC).
- (6) Set the TM3EN flag of the TM3MD register to "1" to start the timer.
- (7) When timer 3 begins operation, binary counter 3 counts upward from X'00'.
- (8) When the value of binary counter 3 matches that of the TM3OC register, the timer 3 interrupt request flag is set, the value of binary counter 3 is reset to X'00', and counting begins again.

#### ■ Cascade Connection Function (timer 2 + timer 3)

Settings for the cascade connection function are listed below. Timer 2 and timer 3 are connected to operate as a 16-bit timer.

- (1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.
- (2) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop the count operation of timer 3.
- (3) Set the TM2CK2~0 flags of the TM2MD register to select fs, fs/4, fx, or synchronized fx as the clock source.
- (4) Use the TM3CK2~0 flags of the TM3MD register to set the clock source as a cascade connection with timer 2.
- (5) Set the TM2PWM flag of the TM2MD register to "0" to select normal timer operation.
- (6) Set values in compare register 2 (TM2OC) and compare register 3 (TM3OC).
- (7) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
- (8) Set the TM3EN flag of the TM3MD register to "1" to start the timer.
- (9) When timers 2 and 3 begin operation, the binary counters begin counting upward from X'0000' as a 16-bit counter.
- (10) When the value of the 16-bit binary counter matches that of the 16-bit register (TM3OC+TM2OC), the timer 3 interrupt request flag is set, the value of the 16-bit binary counter is reset to X'0000', and counting begins again.

Disable the timer 2 interrupt.



**Use a 16-bit access instruction to set the (TM3OC+TM2OC) register.**

## 4-4 16-bit Timer Operation (timer 4)

### 4-4-1 Overview

Timer 4 is a 16-bit programmable counter that can be used as an event counter. A signal with a frequency of 1/2 of the timer 4 overflow signal can be output from the TM4IO pin. An input capture function and pulse added type PWM output function can also be used.

### 4-4-2 Operation

#### ■ Timer Operation

Settings for timer operation are listed below.

- (1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.
- (2) Set the TM4CK2~0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source.
- (3) Set the TM4PWM flag of the TM4MD register to "0" to select 16-bit timer operation.
- (4) Set a value in compare register 4 (TM4OCH, TM4OCL).
- (5) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
- (6) When timer 4 begins operation, binary counter 4 counts upward from X'0000'.
- (7) When the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the timer 4 interrupt request flag is set, the value of binary counter 4 is reset to X'0000', and counting begins again.

*When servicing an interrupt, reset the timer 4 interrupt request flag before operating timer 4.*

*During a count operation, be careful if the value set in TM4OCH and TM4OCL is smaller than the value of binary counter 4, since the count-up operation will continue until overflow occurs.*

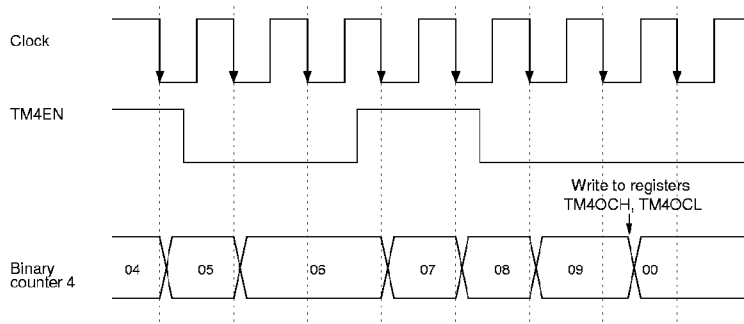




Figure 4-4-1 Binary Counter 4 (TM4BC) Count Timing

 If the TM4EN flag of the TM4MD register is changed simultaneously with other bits, the switching operation may cause binary counter 4 to be incremented.

 If the value of the TM4OCH, TM4OCL register is overwritten while timer 4 has stopped counting, binary counter 4 will be reset to X'0000'.

■ Event Count Function

Settings for the event count function are listed below.

- (1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.
- (2) Use the TM4CK2~0 flags of the TM4MD register to select TM4IO input or synchronized TM4IO input as the clock source.
- (3) Set the TM4PWM flag of the TM4MD register to "0" so that 16-bit timer operation is selected.
- (4) Set a value in compare register 4 (TM4OCH, TM4OCL).
- (5) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
- (6) When timer 4 begins operation, binary counter 4 will count upward from X'0000'.
- (7) When the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the timer 4 interrupt request flag is set, and the binary counter is reset to X'0000' and begins to count upward again.

*If TM4IO input is selected as the clock source and the value of binary counter 4 is to be read during operation, select synchronized TM4IO input to avoid reading data that may be incomplete during count-up transitions. However, with synchronized TM4IO input, it is not possible to return from STOP/HALT modes.*

When synchronized TM4IO is selected, the timer 4 clock source is synchronized with the system clock after a transition of the TM4IO input signal. Binary counter 4 counts upward based on a signal synchronized to the system clock. Therefore, correct values can be read from binary counter 4.

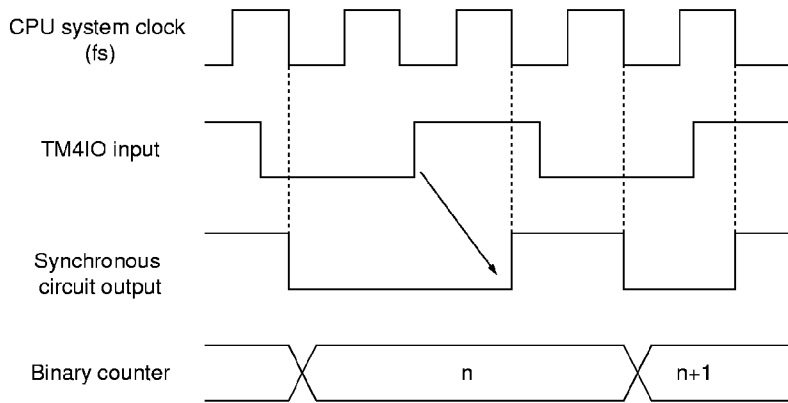


Figure 4-4-2 Timer 4 Event Counter Timing (when synchronous TM4IO input is selected)

*The period of the output signal from the port is 1/2 of the period set in the TM4OCH, TM4OCL register.*

■ Timer Pulse Output Function

Settings for the timer pulse output function are listed below.

- (1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" so that the count operation of timer 4 is stopped.
- (2) Set bit 4 of the port 1 output/input mode register (P1OMD) to the special function pin setting. Bit 4 of port 1 will be specified as the pulse output pin.
- (3) Use the TM4CK2~0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source.
- (4) Set the TM4PWM flag of the TM4MD register to "0" so that 16-bit timer operation is selected.
- (5) Set a value in compare register 4 (TM4OCIL, TM4OCL).
- (6) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
- (7) When timer 4 begins operation, binary counter 4 will count upward from X'0000'.
- (8) When the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the timer 4 interrupt request flag is set, and the binary counter is reset to X'0000' and begins to count upward again.

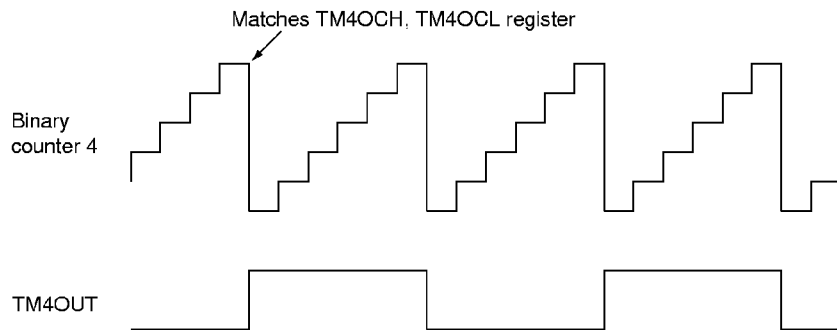


Figure 4-4-3 Timer Pulse Output Timing

### ■ Synchronous Output Timing Generation Function

Settings for the synchronous output timing generation function are listed below.

- (1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" so that the count operation of timer 4 is stopped.
- (2) Set the P7SYEVS2 and P7SYEVS1 flags of pin control register 2 (FLOAT2) to select timer 4 interrupts.
- (3) Set the synchronous output control register (SYSMD) to configure port 7 bits for use as synchronous output pins.
- (4) Set the TM4CK2~0 flags of the TM4MD register to select  $f_{osc}$ ,  $f_s/4$ , or  $f_s/16$  as the clock source.
- (5) Set the TM4PWM flag of the TM4MD register to "0" so that 16-bit timer operation is selected.
- (6) Set a value in compare register 4 (TM4OCH, TM4OCL).
- (7) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
- (8) When timer 4 begins operation, binary counter 4 will count upward from X'0000'.
- (9) When the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the timer 4 interrupt request flag is set, binary counter 4 is reset to X'0000' and begins to count upward again.
- (10) At the timing when the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the values at port 7 synchronous output pins will change.

*If port 7 pins are to be used as pulse output pins, it is necessary to set the P7DIR register.*

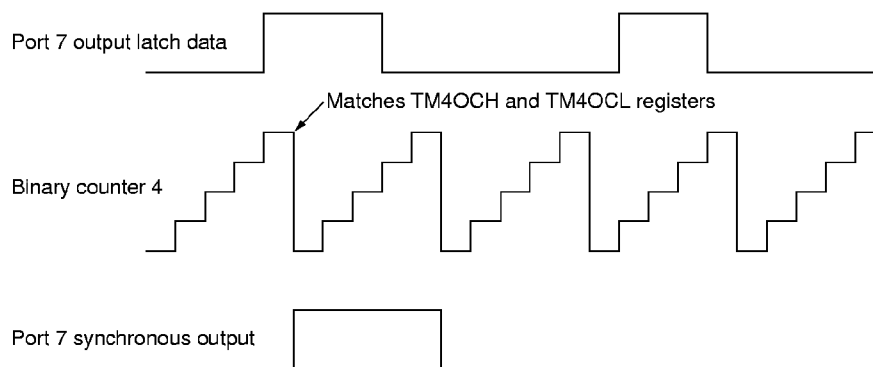


Figure 4-4-4 Port 7 Synchronous Output Timing




If bit 4 of port 1 is to be used as a PWM output pin, set the P1DIR and P1PLU registers.

■ Pulse Added Type PWM Output Function

In the pulse added method, a 1-bit output is appended to the basic component of the 8-bit PWM output. Precise control is possible based on the number of PWM repetitions (256 times) to which this bit is appended. Settings for the pulse added type PWM output function are listed below.

- (1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.
- (2) Set bit 4 of the port 1 output/input mode register (P1OMD) to the special function pin setting. Bit 4 of port 1 will be specified as the PWM output pin.
- (3) Use the TM4CK2~0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source. The period of the output waveform is determined based on the clock source.
- (4) Set the TM4PWM flag of the TM4MD register to "1" so that PWM operation is selected.
- (5) Set a value in the lower 8 bits of compare register 4 (TM4OCL). The high interval of the output waveform is determined based on the value of the lower 8 bits of compare register 4 (TM4OCL).
- (6) Set the position of the added pulse in the upper 8 bits of compare register 4 (TM4OCH).
- (7) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
- (8) When timer 4 begins operation, binary counter 4 will count upward from X'00'.
- (9) A high-level signal is output from the port beginning when binary counter 4 starts counting from X'00' and ending when the value of binary counter 4 matches the value set in the TM4OCL register.
- (10) When the value of binary counter 4 matches that of the TM4OCL register, a low-level signal is output from the port.
- (11) Binary counter 4 continues to count upward until X'FF' is reached. At the next count-up cycle, the value of binary counter 4 is reset to X'00', and counting begins again. A high-level signal is output from the port.

 Use a 16-bit access instruction to set the TM4OCH, TM4OCL register.

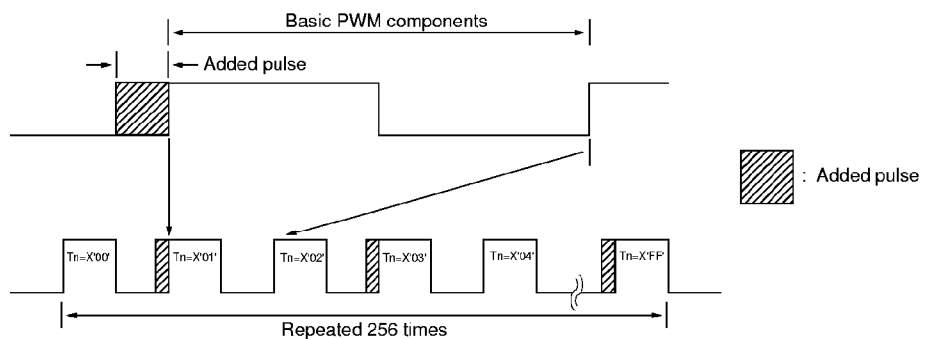


Figure 4-4-5 Pulse Added Type PWM Output

■ Setting the Added Pulse Position

[\*5] 5-2-3 "Serial Interface Transfer Timing"

The upper 8 bits of compare register 4 (TM4OCH) set the position of the added pulse. If the TM4OCH register is set to X'00', an additional bit is not appended to the basic PWM component. If the TM4OCH register is set to X'FF', an additional bit is repeatedly appended to the 255 basic PWM components during the period. The relation between the value set in the TM4OCH register and the added pulse is shown in the table below. If X'03' is set in the TM4OCH register, bits are appended to pulse positions for X'01' and X'02', shown in table 4-4-1. The relation between the value set in the TM4OCH register and the position of the added bit is shown in figure 4-4-6.

Table 4-4-1 Pulse-Added PWM Output

| Value Set in TM4OCH Register | Added Pulse Position (value of Tn)                               |
|------------------------------|--|
| 0 0 0 0 0 0 0 0              |  |
| 0 0 0 0 0 0 0 1              | X'80'  |
| 0 0 0 0 0 0 1 0              | X'40', X'C0'   |
| 0 0 0 0 0 1 0 0              | X'20', X'60', X'A0', X'E0'                                       |
| 0 0 0 0 1 0 0 0              | X'10', X'30', X'50', X'70', X'90', X'B0', X'D0', X'F0'           |
| 0 0 0 1 0 0 0 0              | X'08', X'18', X'28', X'38', X'48', X'58' . . . . ., X'E8', X'F8' |
| 0 0 1 0 0 0 0 0              | X'04', X'0C', X'14', X'1C', X'24', X'2C' . . . . ., X'F4', X'FC' |
| 0 1 0 0 0 0 0 0              | X'02', X'06', X'0A', X'0E', X'12', X'16' . . . . ., X'FA', X'FE' |
| 1 0 0 0 0 0 0 0              | X'01', X'03', X'05', X'07', X'09', X'0B' . . . . ., X'FD', X'FF' |
| (MSB)                        | (LSB)  |

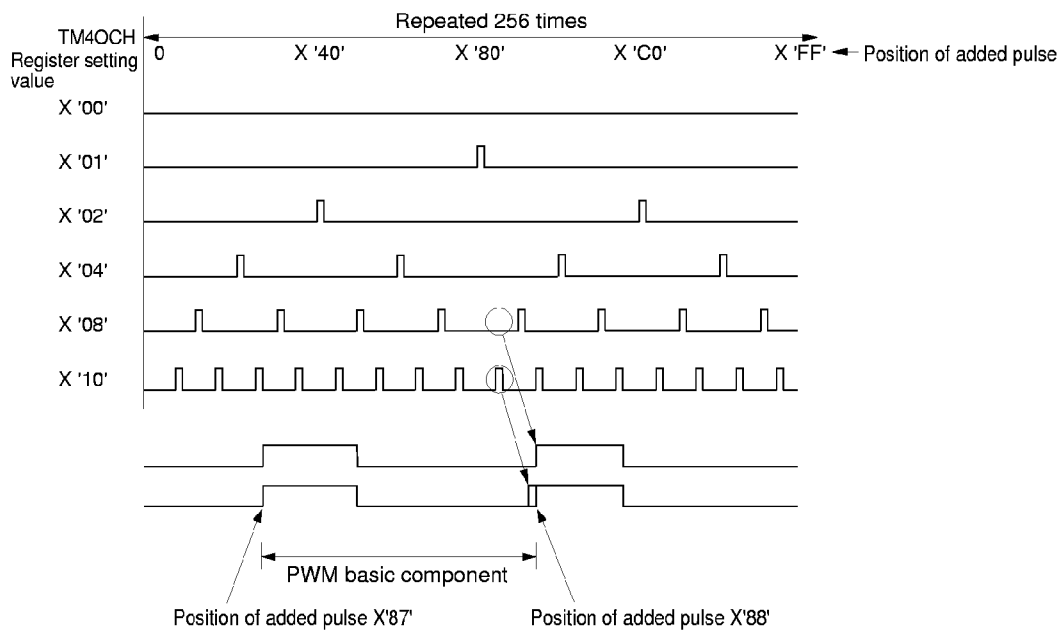


Figure 4-4-6 Pulse Added Type PWM Output

■ Capture Function

Settings for the capture function are listed below.

- (1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.
- (2) Use the TM4CK2~0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source. The period of the output waveform is determined based on the clock source.
- (3) Use the T4ICTS1 and T4ICTS0 flags of the TM4MD register to select IRQ2, IRQ1, or IRQ0 as the input capture trigger.
- (4) Set the REDGn flag of the external interrupt control register to specify the valid edge for the interrupt selected as the TM4 input capture trigger.
- (5) Set the TM4PWM flag of the TM4MD register to "1" to select 16-bit timer operation.
- (6) Set a value in compare register 4 (TM4OCH, TM4OCL).
- (7) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
- (8) When timer 4 begins operation, binary counter 4 will count upward from X'0000' until it reaches the value set in compare register 4.
- (9) If the binary counter is to be used as a free-running counter that counts from X'0000'~X'FFFF', set the compare register 4 to X'FFFF'.  
When the value of binary counter 4 matches that of the TM4OCH, TM4OCL register, the timer 4 interrupt request flag is set, binary counter 4 is reset to X'0000', and counting begins again.
- (10) If the external interrupt selected as the TM4 input capture trigger is received during timer 4 operation, the value of binary counter 4 will be written into the input capture register (TM4ICHI, TM4ICL).

*Setting a value in compare register 4, clears binary counter 4.*

*If the event occurs before a read, that data will be overwritten.*

## 4-5 8-bit Timer Operation (timer 5)

### 4-5-1 Overview

Timer 5 is an 8-bit timer that can have  $f_{osc}$ ,  $f_s/4$ ,  $f_x$ , or time base output as its clock source.

### 4-5-2 Operation

#### ■ Timer Operation

Settings for timer operation are listed below.

- (1) Set the TM5CLRS flag of the timer 5 mode register (TM5MD) to "0."
- (2) Use the TM5CK3~1 flags of the TM5MD register to select  $f_{osc}$ ,  $f_s/4$ ,  $f_x$ , synchronized  $f_x$ , time base timer output, or time base timer synchronized output as the clock source.
- (3) Set a value in compare register 5 (TM5OC). At this time, if the TM5CLRS flag is "0," binary counter 5 will be initialized to X'00'.
- (4) Binary counter 5 (TM5OC) counts upward from X'00'.
- (5) When the value of binary counter 5 matches that of the TM5OC register, the timer 5 interrupt request flag is set, the binary counter is reset to X'00', and counting begins again.

*When servicing an interrupt, reset the timer 5 interrupt request flag before starting timer 5.*

*When choosing either time base timer output or time base timer synchronized output for the timer 5 clock source, the time base must be set up.*

*During a count operation, be careful if the value set in TM5OC is smaller than the value of binary counter 5, since the count-up operation will continue until overflow occurs.*

*If  $f_x$  input is selected as the clock source and the value of binary counter 5 is to be read during operation, select synchronized  $f_x$  input to avoid reading data that may be incomplete during count-up transitions. However, with synchronized  $f_x$  input, it is not possible to return from STOP/HALT modes.*



**If the TM5CLRS flag of the TM5MD register is set to "0," binary counter 5 will be initialized every time data in the TM5OC register is overwritten. Timer 5 interrupts are disabled in this mode. If timer 5 interrupts are to be used, the TM5CLRS flag must be reset to "1" after writing to the TM5OC register.**



**Timer 5 operation cannot be halted.**

## 4-6 Time Base Operation

### 4-6-1 Overview

The clock source for the time base timer can be set to  $f_{osc}$  or  $f_x$ . Also, the interrupt period for time base timer (TBIRQ) can be set to  $1/2^7$ ,  $1/2^8$ ,  $1/2^9$ ,  $1/2^{10}$ , or  $1/2^{13}$  of the clock source.

### 4-6-2 Operation

#### ■ Time Base Function

Settings for the time base function are listed below.

- (1) Use the TM5CK0 flag of the timer 5 modc register (TM5MD) to select  $f_{osc}$  or  $f_x$  as the clock source.
- (2) Use the TM5IR2~0 flags of the TM5MD register to select the time base timer interrupt source.
- (3) When the selected time interval passes, the interrupt request flag of the time base interrupt control register (TBICR) is set.



**Time base operation cannot be halted.**

Table 4-6-1 Base Time Settings

| Clock Source \ TM5IR2~0 |           | 000             | 001             | 010             | 011                | 1XX                |
|-------------------------|-----------|-----------------|-----------------|-----------------|--------------------|--------------------|
|                         |           | $\frac{1}{2^7}$ | $\frac{1}{2^8}$ | $\frac{1}{2^9}$ | $\frac{1}{2^{10}}$ | $\frac{1}{2^{13}}$ |
| $f_{osc}$               | 20MHz     | 6.4 $\mu$ s     | 12.8 $\mu$ s    | 25.6 $\mu$ s    | 51.2 $\mu$ s       | 409.6 $\mu$ s      |
|                         | 8.38MHz   | 15.2 $\mu$ s    | 30.5 $\mu$ s    | 61.0 $\mu$ s    | 122.0 $\mu$ s      | 976.4 $\mu$ s      |
| $f_x$                   | 32.768kHz | 3.9ms           | 7.8ms           | 15.6ms          | 31.2ms             | 250ms              |

## 4-7 Watchdog Timer Operation

### 4-7-1 Overview

The watchdog timer is controlled by the watchdog control register (WDCTR) and can be used for runaway program detection.

### 4-7-2 Setup and Operation

- (1) Set the WDEN flag of the watchdog timer control register (WDCTR) to "1" to start the watchdog timer.
- (2) Operate the watchdog timer by clearing the WDEN flag to "0" within the fixed amount of time ( $T_{wd}$ ), and then resetting the WDEN flag to "1."  
If the WDEN flag is not cleared, a WDT interrupt will be generated after the fixed amount of time passes.
- (3) When a runaway of program is detected, the program encoded at the location of the WDT interrupt routine is executed.

$T_{wd}$  is set by the mask option as  $fs/2^{16}$ ,  $fs/2^{18}$ , or  $fs/2^{20}$ .

*The upper 2 bits of the watchdog timer are cleared when the WDEN flag is set to "0." Therefore, depending on the timing of this clear the watchdog timer may be reset at  $3/4T_{wd}$ . If the WDEN bit is to be repeatedly cleared and set at regular intervals, those operations should be performed within  $3/4$  of the  $T_{wd}$  period.*

## 4-8 Remote Control Output Operation

### 4-8-1 Overview

A remote control carrier pulse can be generated using the overflow of timer 3. Two duty ratios of 1/2 or 1/3 can be selected.

### 4-8-2 Setup and Operation

*Set bit 0 of the P10MD register to "1" at the same time the remote control output is switched on, and to "0" at the same time the remote control output is switched off.*

- (1) Set the RMOEN flag of the remote control output control register (RMCTR) to "0" so that the remote control carrier output is switched off. Set the RMBTMS flag to select the base period timer for the remote control carrier.
- (2) Set timer 0 or timer 3 to select the base period of the remote control carrier (the width that the remote control carrier output pulse is held at a high level).
- (3) Set the RMDTY0 flag of the RMCTR register to select the carrier duty.
- (4) Set the P10 output data to "0" and set P10 to the output mode. Also, set TM0RM flag of the RMCTR register to "0" and select remote control carrier output.
- (5) The RMOEN flag of the RMCTR register controls whether the remote control carrier output is on or off.  
Even if the carrier output is at a high level, and the RMOEN flag is set to "0" (off), the carrier waveform will be maintained by the synchronous circuit.

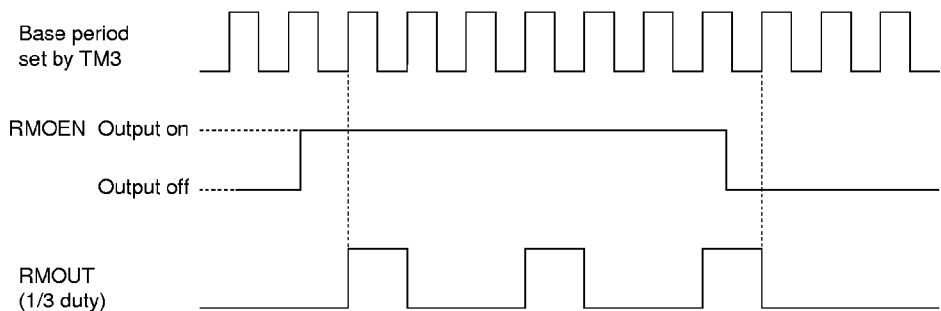


Figure 4-8-1 Remote Control Carrier Output Waveform

## 4-9 Buzzer Output

### 4-9-1 Buzzer Output Setup and Operation

The square wave having a frequency  $1/2^9 \sim 1/2^{12}$  of the system clock can be output from the P06/BUZZER pin.

- (1) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "0" so that the buzzer output is turned off.
- (2) Set the buzzer output frequency with the BUZCK1 and BUZCK0 flags of the DLYCTR.
- (3) Set the BUZOE flag of the DLYCTR register to "1" and set P06 to the buzzer output mode.
- (4) The BUZOE flag of the DLYCTR register controls whether the buzzer output is on or off.



## 4-10 Timer Function Control Registers

### 4-10-1 Overview

Twenty-five registers control the timers. See table 4-10-1.

Table 4-10-1 Timer Control Registers

| Name   | Address  | R/W | Function  |
|--------|----------|-----|---|
| TM0OC  | X'03F70' | R/W | Compare register 0                              |
| TM0BC  | X'03F60' | R   | Binary counter 0                                |
| TM0MD  | X'03F80' | R/W | Timer 0 mode register                           |
| TM1OC  | X'03F71' | R/W | Compare register 1                              |
| TM1BC  | X'03F61' | R   | Binary counter 1                                |
| TM1MD  | X'03F81' | R/W | Timer 1 mode register                           |
| TM2OC  | X'03F72' | R/W | Compare register 2                              |
| TM2BC  | X'03F62' | R   | Binary counter 2                                |
| TM2MD  | X'03F82' | R/W | Timer 2 mode register                           |
| TM3OC  | X'03F73' | R/W | Compare register 3                              |
| TM3BC  | X'03F63' | R   | Binary counter 3                                |
| TM3MD  | X'03F83' | R/W | Timer 3 mode register                           |
| TM4OCL | X'03F74' | R/W | Compare register 4 (lower 8 bits)               |
| TM4OCH | X'03F75' | R/W | Compare register 4 (upper 8 bits)               |
| TM4BCL | X'03F64' | R   | Binary counter 4 (lower 8 bits)                 |
| TM4BCH | X'03F65' | R   | Binary counter 4 (upper 8 bits)                 |
| TM4ICL | X'03F66' | R   | Input capture register (lower 8 bits)           |
| TM4ICH | X'03F67' | R   | Input capture register (upper 8 bits)           |
| TM4MD  | X'03F84' | R/W | Timer 4 mode register                           |
| TM5OC  | X'03F78' | R/W | Compare register 5                              |
| TM5BC  | X'03F68' | R   | Binary counter 5                                |
| TM5MD  | X'03F88' | R/W | Timer 5 mode register                           |
| WDCTR  | X'03F02' | R/W | Watchdog timer control register                 |
| DLYCTR | X'03F03' | R/W | Oscillation stabilization wait control register |
| RMCTR  | X'03F89' | R/W | Remote control carrier output control register  |

R/W: Readable and writable

R: Read only

## 4-10-2 Programmable Timer/Counters

Timers 0~5 all contain a programmable 8-bit timer/counter (16-bit in timer 4). Programmable timer/counters consist of a compare register and a binary counter.

(1) Compare register 0 (TM0OC)

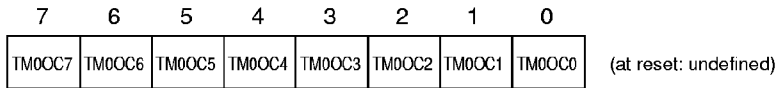


Figure 4-10-1 Compare Register 0 (TM0OC: X'03F70', R/W)

(2) Binary counter 0 (TM0BC)



Figure 4-10-2 Binary Counter 0 (TM0BC: X'03F60', R)

(3) Compare register 1 (TM1OC)

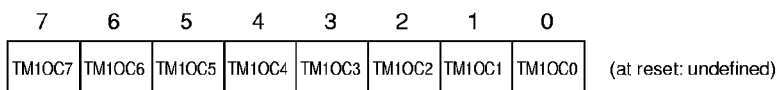


Figure 4-10-3 Compare Register 1 (TM1OC: X'03F71', R/W)

(4) Binary counter 1 (TM1BC)



Figure 4-10-4 Binary Counter 1 (TM1BC: X'03F61', R)

(5) Compare register 2 (TM2OC)



Figure 4-10-5 Compare Register 2 (TM2OC: X'03F72', R/W)

(6) Binary counter 2 (TM2BC)

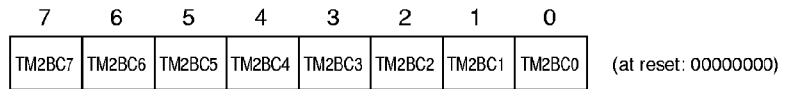


Figure 4-10-6 Binary Counter 2 (TM2BC: X'03F62', R)

(7) Compare register 3 (TM3OC)



Figure 4-10-7 Compare Register 3 (TM3OC: X'03F73', R/W)

(8) Binary counter 3 (TM3BC)



Figure 4-10-8 Binary Counter 3 (TM3BC: X'03F63', R)

(9) Compare register 4 (TM4OCL) (lower 8 bits)

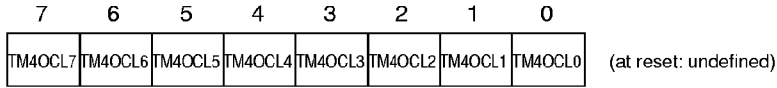


Figure 4-10-9 Compare Register 4 (TM4OCL: X'03F74', R/W)

(10) Compare register 4 (TM4OCH) (upper 8 bits)

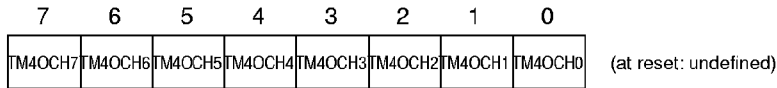


Figure 4-10-10 Compare Register 4 (TM4OCH: X'03F75', R/W)

(11) Binary counter 4 (TM4BCL) (lower 8 bits)

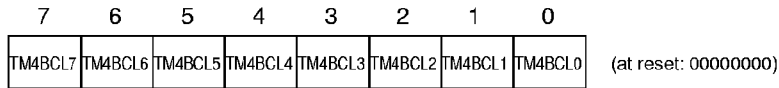


Figure 4-10-11 Binary Counter 4 (TM4BCL: X'03F64', R)

(12) Binary counter 4 (TM4BCH) (upper 8 bits)

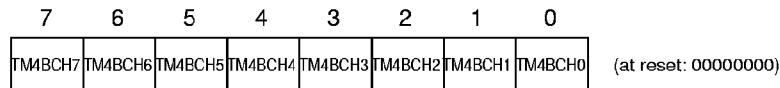


Figure 4-10-12 Binary Counter 4 (TM4BCH: X'03F65', R)

(13) Input capture register (TM4ICL) (lower 8 bits)

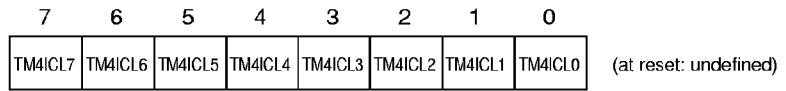


Figure 4-10-13 Input Capture Register (TM4ICL: X'03F66', R)

(14) Input capture register (TM4ICH) (upper 8 bits)

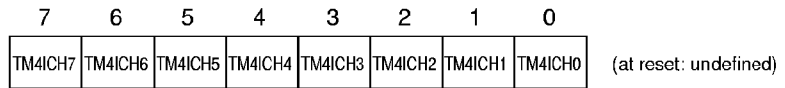


Figure 4-10-14 Input Capture Register (TM4ICH: X'03F67', R)

(15) Compare register 5 (TM5OC)

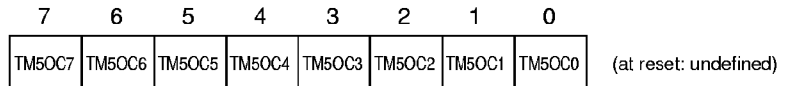


Figure 4-10-15 Compare Register 5 (TM5OC: X'03F78', R/W)

(16) Binary counter 5 (TM5BC)



Figure 4-10-16 Binary Counter 5 (TM5BC: X'03F68', R)

### 4-10-3 Timer Mode Registers

Four readable and writable timer mode registers. Control timers 0, 1, 2, 3, 4, 5, and the time base.

(1) Timer 0 mode register (TM0MD)

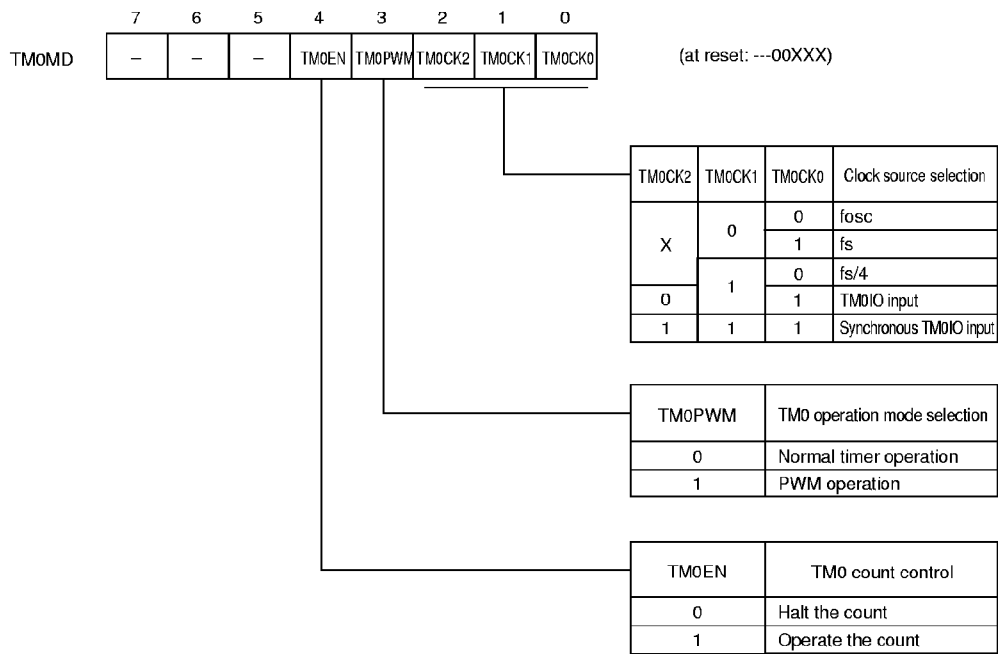


Figure 4-10-17 Timer 0 Mode Register (TM0MD: X'03F80', R/W)

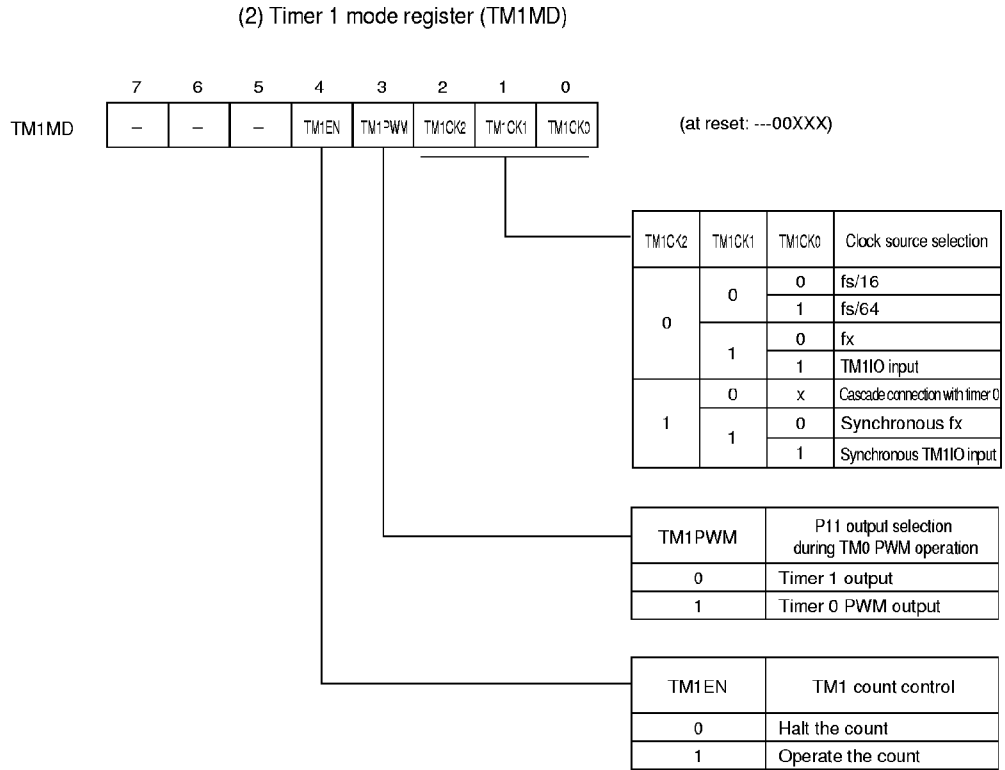


Figure 4-10-18 Timer 1 Mode Register (TM1MD: X'03F81', R/W)

(3) Timer 2 mode register (TM2MD)

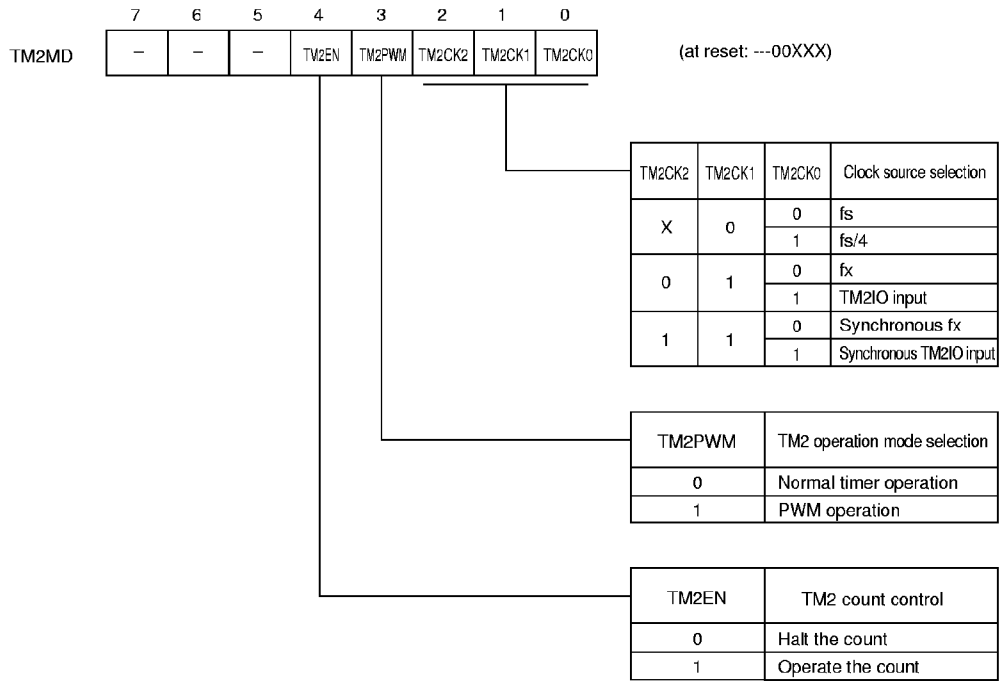


Figure 4-10-19 Timer 2 Mode Register (TM2MD: X'03F82', R/W)



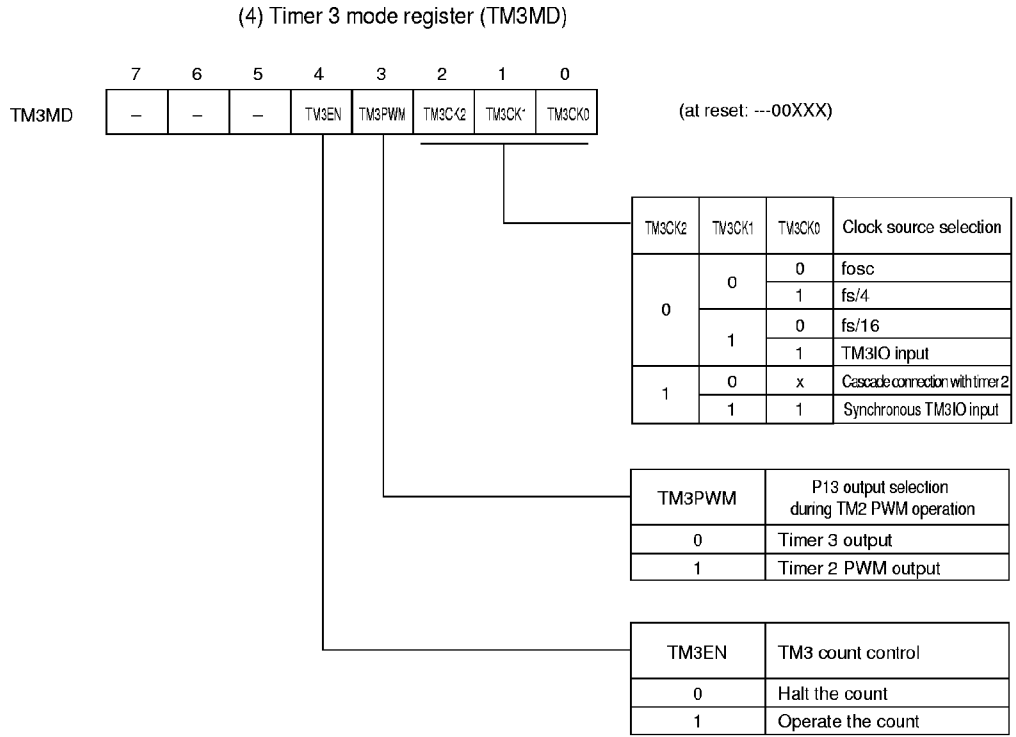


Figure 4-10-20 Timer 3 Mode Register (TM3MD: X'03F83', R/W)

(5) Timer 4 mode register (TM4MD)

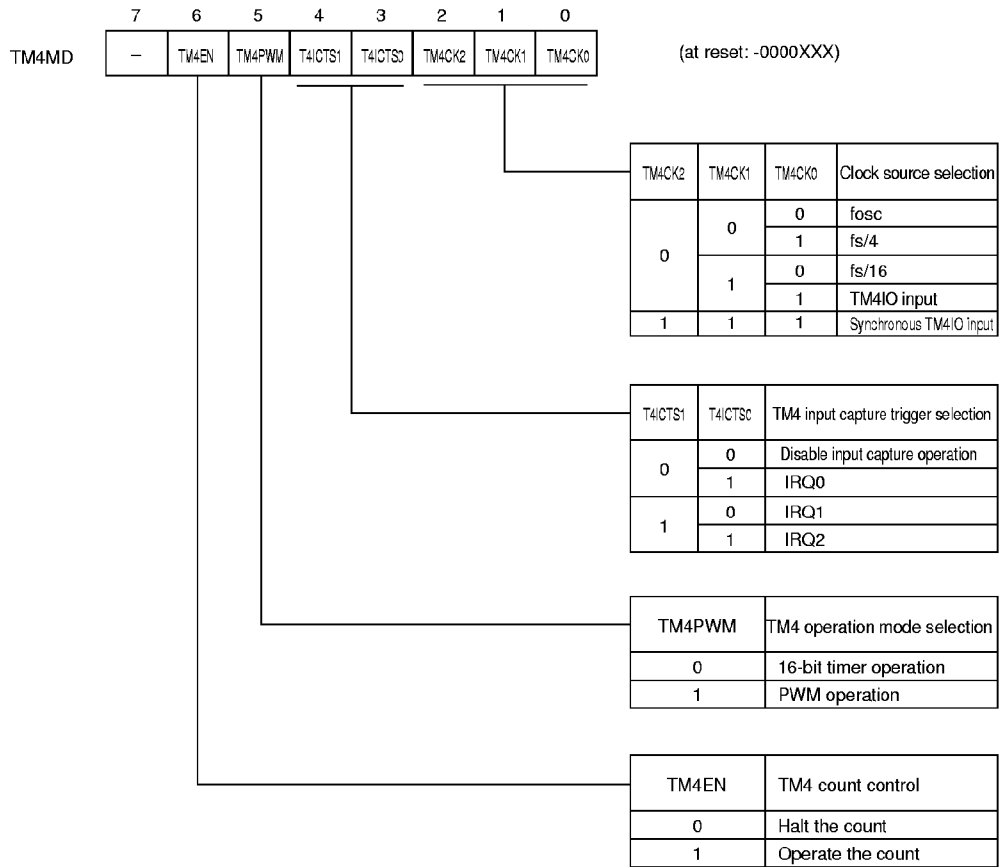


Figure 4-10-21 Timer 4 Mode Register (TM4MD: X'03F84', R/W)

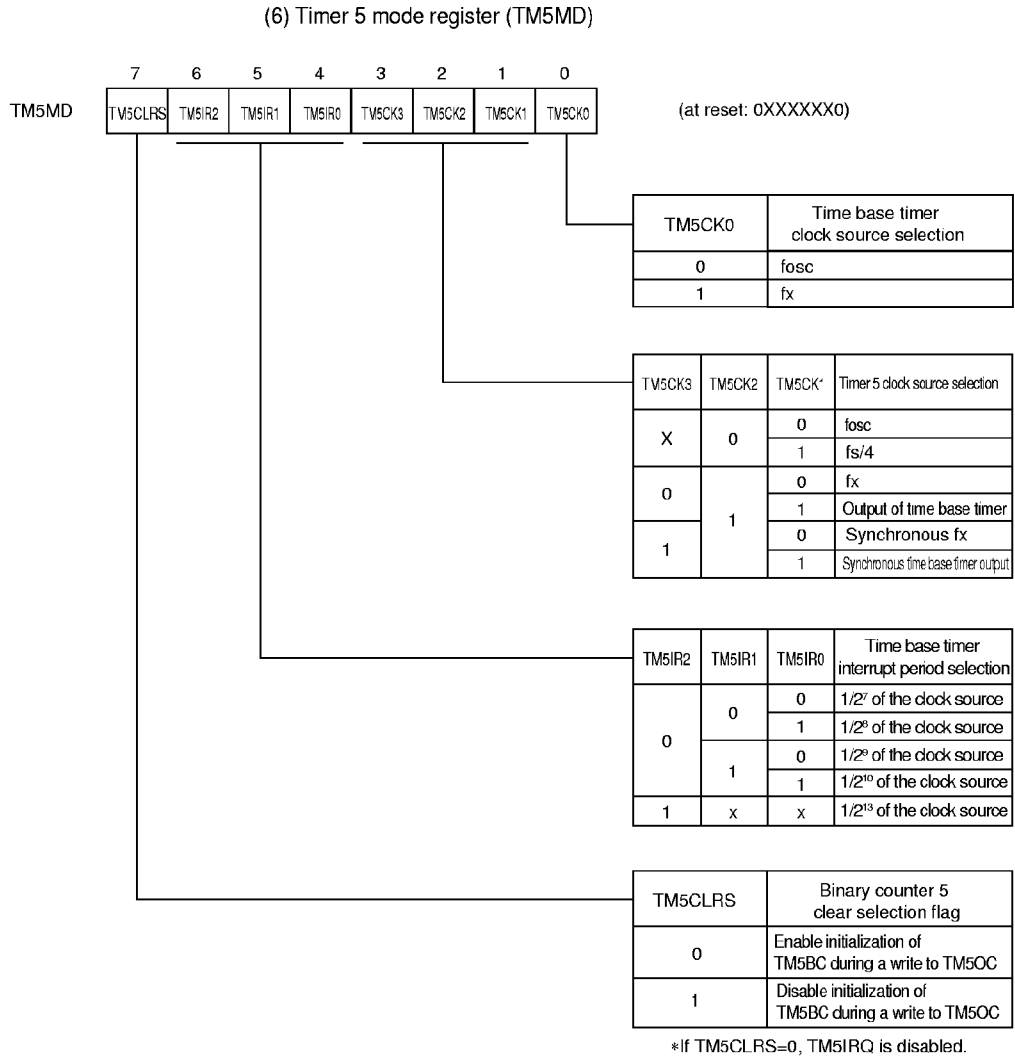


Figure 4-10-22 Timer 5 Mode Register (TM5MD: X'03F88', R/W)

## 4-10-4 Timer Control Registers

(1) Watchdog timer control register (WDCTR)

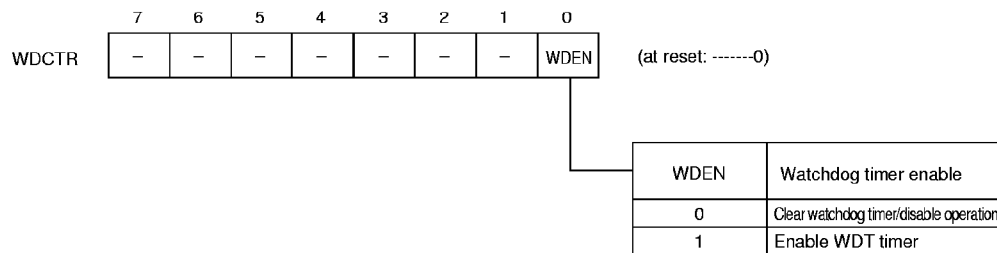


Figure 4-10-23 Watchdog Timer Control Register (WDCTR: X'03F02', R/W)

(2) Oscillation stabilization control register (DLYCTR)

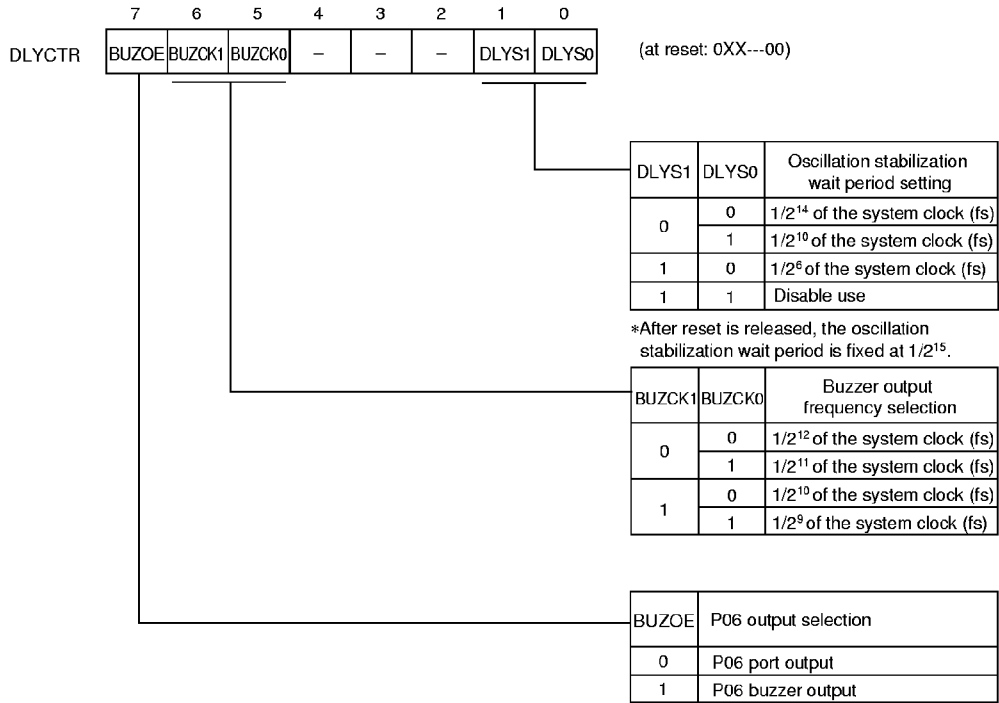


Figure 4-10-24 Oscillation Stabilization Wait Counter Control Register (DLYCTR: X'03F03', R/W)

(3) Remote control carrier output control register (RMCTR)

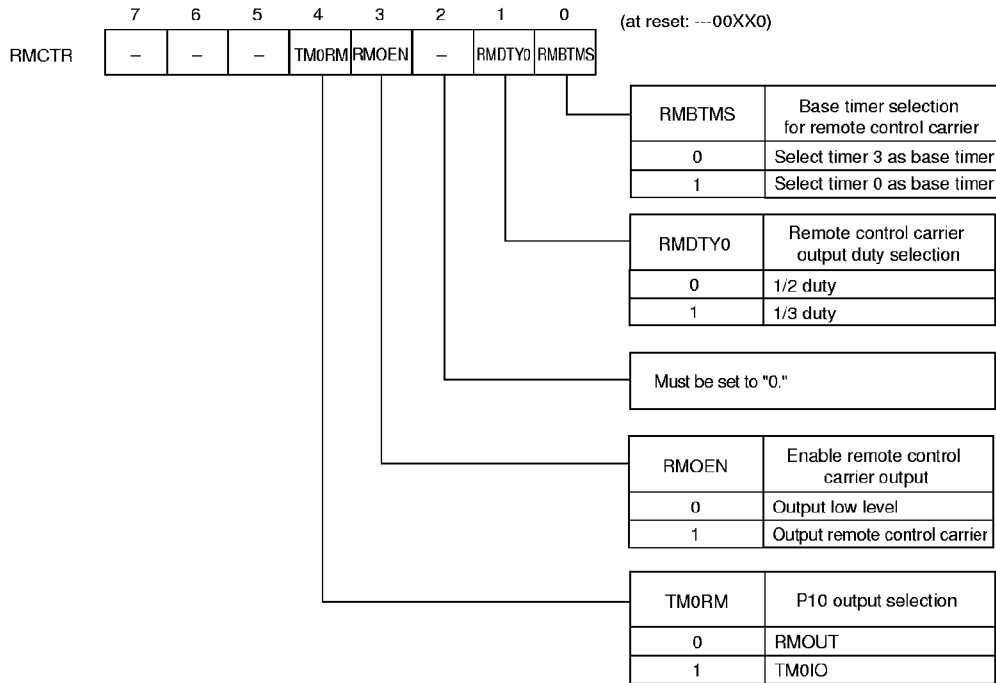


Figure 4-10-25 Remote Control Carrier Control Register  
(RMCTR: X'03F89', R/W)

(2) Oscillation stabilization control register (DLYCTR)

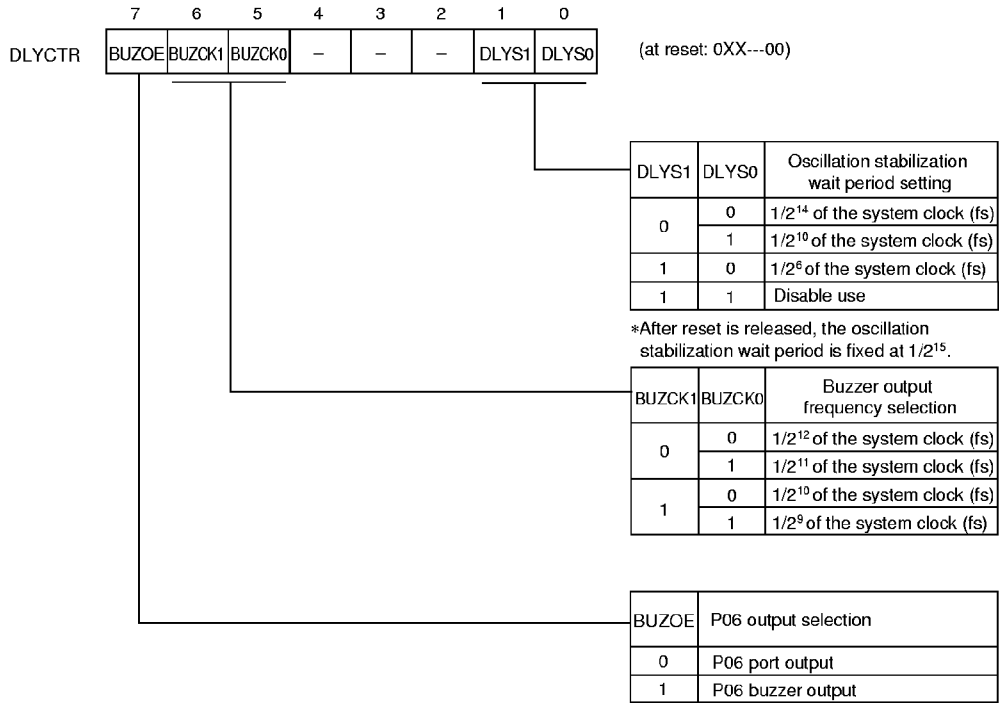


Figure 4-10-24 Oscillation Stabilization Wait Counter Control Register (DLYCTR: X'03F03', R/W)

Chapter 5 Serial Functions





## 5-1 Overview

The MN101C01D contains a serial interface that can operate in synchronous and simple UART modes.

An overview of serial functions is shown below.

Table 5-1-1 Overview of Serial Functions

|                     | Serial 0   | Serial 1   | Serial 2  |
|---------------------|--|--|---|
| Interrupt           | SC0ICR   | SC1ICR   | SC2ICR  |
| Synchronous         | ✓  | ✓  | ✓   |
| Simple UART         | ✓  | —  | —   |
| Simple IIC          | —  | —  | ✓   |
| Clock selection     | fs/2<br>fs/4<br>fs/16<br><br>BC3×1/2<br>External | fs/2<br>fs/8<br>fs/64<br><br>BC3×1/2<br>External | fs<br>fs/2<br>fs/4<br>fs/8<br>BC0×1/2<br>External |
| 1/8 clock frequency | ✓  | —  | —   |

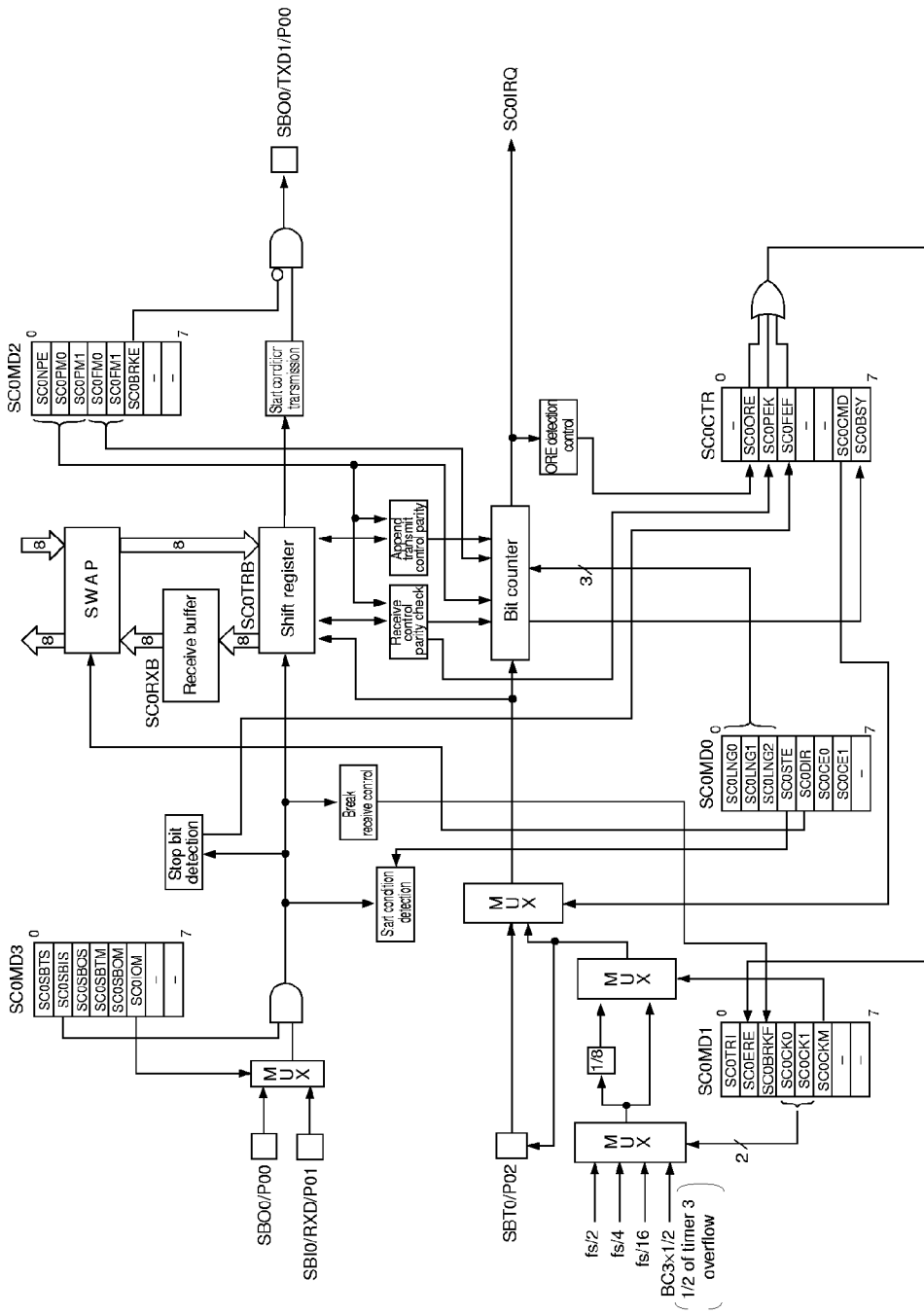
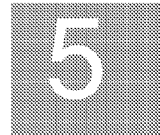


Figure 5-1-1 Serial 0 Block Diagram



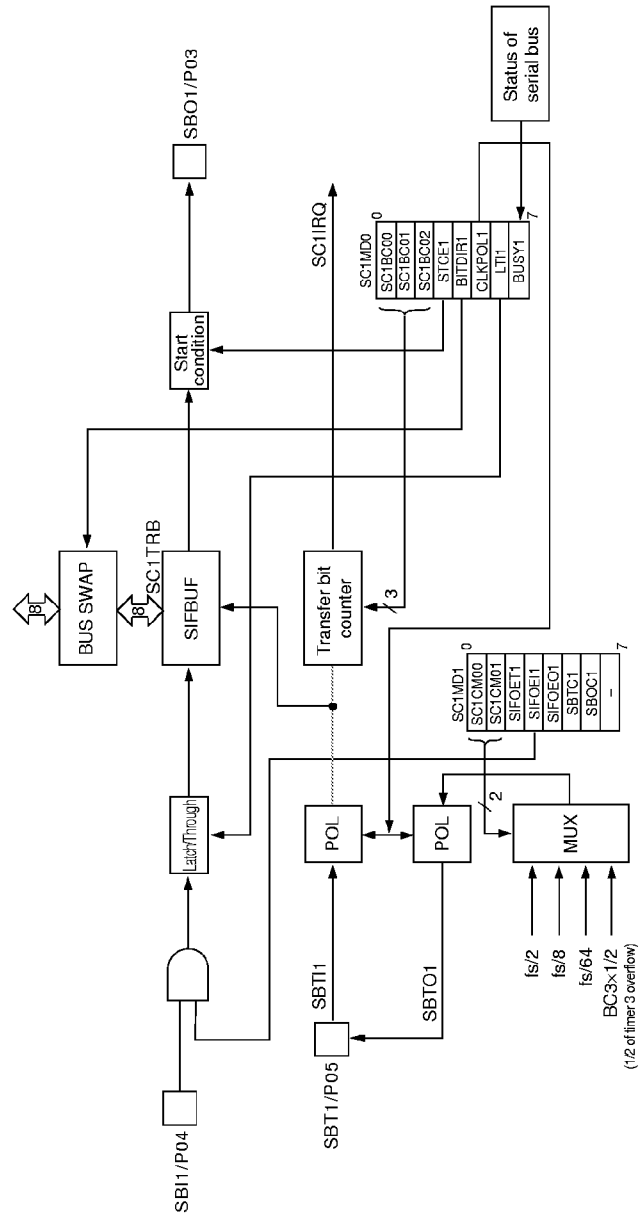


Figure 5-1-2 Serial 1 Block Diagram



## 5-2 Synchronous Serial Interface

### 5-2-1 Overview

A serial interface begins operation when data is written to the shift buffer. A bit counter is incremented at each 1-bit transfer. The transfer is complete when the counter overflows.

Bit transfers of an arbitrary 1~8 bits can be performed. The transfer bit count must be set before performing the transfer.

### 5-2-2 Setup and Operation

#### ■ Transmission

- (1) Select the synchronous serial interface by setting the SCOCMD flag of the serial interface 0 control register (SCOCTR) to "0."
- (2) Select the transfer bit count with the SCOLNG2~0 flags of the serial interface 0 mode register 0 (SCOMD0). The transfer bit count can be set as 1 to 8 bits.
- (3) Specify whether the start condition is enabled or disabled with the SCOSTE flag of the SCOMD0 register.
- (4) Specify the first bit to be transferred (MSB first or LSB first) with the SCODIR flag of the SCOMD0 register.
- (5) Select the valid edge of the clock signal with the SCOCE1~0 flags of the SCOMD0 register.
- (6) When the clock source is an internal clock:
  - Select the clock source with the SCOCK1~0 flags of serial interface 0 mode register 1 (SCOMD1).
  - Set the SCOCKM flag of the SCOMD1 register specify whether or not the clock source frequency will be divided by 8.
  - Select serial clock operation by setting the SCOSBTS flag of the serial interface 0 mode register 3 (SCOMD3) to "1."
  - Set the SCOSBTM flag of the SCOMD3 register.
  - Set bit 0 of the port 0 direction control register (PODIR) to the output mode.
  - Set bit 0 of the port 0 pull-up resistor control register (POPLU).

[<sup>158</sup> Section 5-2-3, "Serial Interface Transfer Timing"]

When the clock source is an external clock (SBT0 pin input):

- Set the SC0SBTM flag of the SC0MD3 register.
  - Set bit 0 of the PODIR register to input mode.
  - Set bit 0 of the POPLU register.
- (7) Select the SC0SBOM flag of the SC0MD3 register.
  - (8) Select the SC0IOM flag of the SC0MD3 register.
  - (9) Select serial communication by setting the SC0SBOS flag of the SC0MD3 register to "1."
  - (10) Set transmit data to serial interface 0 transmit/receive shift register (SC0TRB). This will start the serial transmission.
  - (11) When serial transmission begins, the SC0BSY flag of the SC0CTR register is set to "1," indicating that a serial transfer is in progress.
  - (12) When the serial transmission has completed, the SC0BSY flag of the SC0CTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SC0TRI flag of SC0MD1 register 1 is cleared to "0."



**After the transfer is complete, the transfer bit count in the SC0LNG2~0 flags of the SC0MD0 register will be changed. Except in an 8-bit transfer, reset the transfer bit count at the time of the next transmission.**



**When switching from transmission to reception, set the SC0SBOS flag of the SC0MD3 register to "0" and then set the SC0SBIS flag to "1." Do not change both of these flags at the same time.**



**The SC0SBTS flag of the SC0MD3 register must be set to "1" before the SC0SBOS flag of the SC0MD3 register is set to "1."**

*When the serial port is enabled and the SC0CE1~0 flags of the SC0MD0 register are changed, the transfer bit count in the SC0LNG2~0 flags of the SC0MD0 register may be incremented.*

*Enabling the start condition drives the SBO0 pin high for a fixed time interval (1/2 the clock source cycle) after the transmission is completed. If the start condition is disabled, the SBO0 pin will remain at the value of the of the last data bit.*

*If the SC0IOM flag of the SC0MD3 register is set for a pin connection, the SBI0 pin can be used as a port. The SBO0 pin receives data during the input mode and transmits data during the output mode.*

*The SC0LNG2~0 flags change at the opposite edge of the transmit data output edge.*

*Serial interface 0 begins operation when the SC0SBOS flag or the SC0SBIS flag is set to "1." Set the SC0SBOS flag or the SC0SBIS flag after all conditions have been set.*

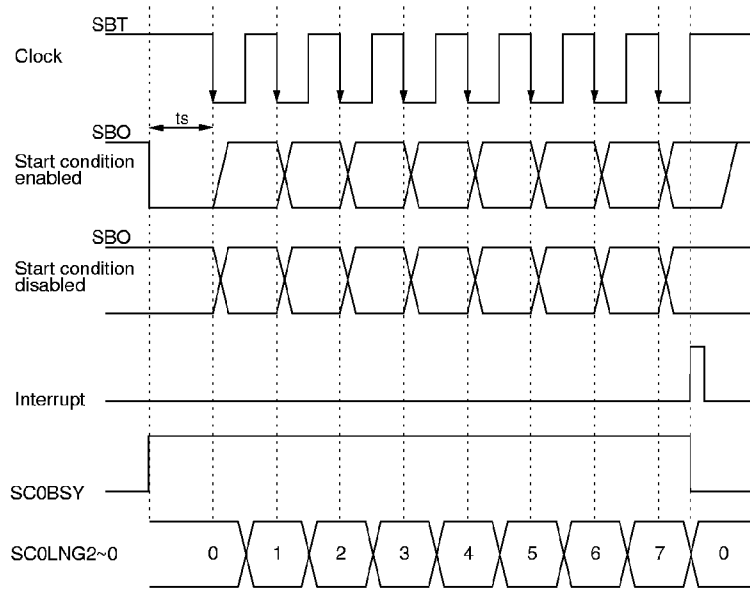


Figure 5-2-1 Synchronous Serial Interface Transmission Timing (falling edge)

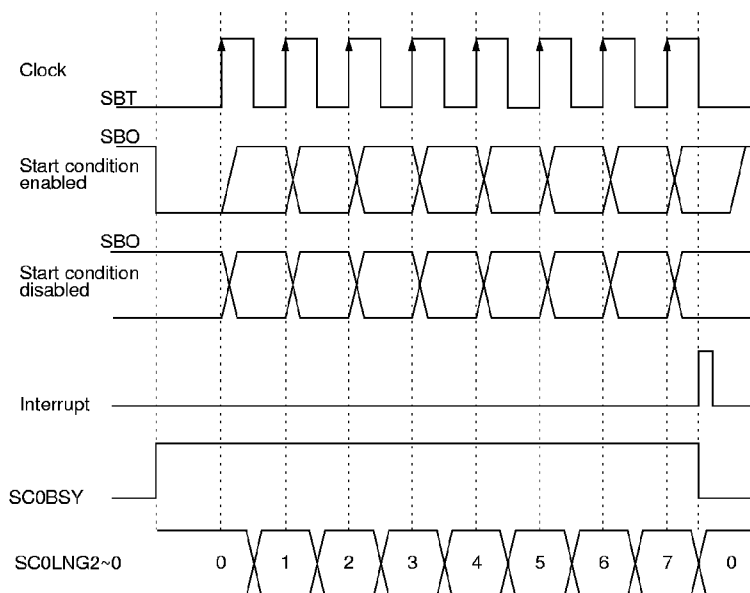


Figure 5-2-2 Synchronous Serial Interface Transmission Timing (rising edge)

## ■ Reception

- (1) Select the synchronous serial interface by setting the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "0."
- (2) Select the transfer bit count with the SC0LNG2~0 flags of the serial interface 0 mode register 0 (SC0MD0). The transfer bit count can be set as 1 to 8 bits.
- (3) Specify whether the start condition is enabled or disabled with the SC0STE flag of the SC0MD0 register.
- (4) Specify the first bit to be transferred (MSB first or LSB first) with the SC0DIR flag of the SC0MD0 register.
- (5) Select the valid edge of the clock signal with the SC0CE1~0 flags of the SC0MD0 register.
- (6) When the clock source is an internal clock:
  - Select the clock source with the SC0CK1~0 flags of serial interface 0 mode register 1 (SC0MD1).
  - Set the SC0CKM flag of the SC0MD1 register to specify whether or not the clock source frequency will be divided by 8.
  - Select serial clock pin operation by setting the SC0SBTS flag of the serial interface 0 mode register 3 (SC0MD3) to "1."
  - Set the SC0SBTM flag of the SC0MD3 register.
  - Set bit 2 of the port 0 direction control register (P0DIR) to the output mode (P02/SBT0 output mode).
  - If necessary, set bit 2 of the port 0 pull-up resistor control register (POPLU) to add the pull-up resistor.
 When the clock source is an external clock (SBT0 pin input):
  - Set bit 2 of the P0DIR register to the input mode.
  - If necessary, set bit 2 of the POPLU register.
- (7) Select the SC0IOM flag of the SC0MD3 register.
- (8) Select serial communication by setting the SC0SBIS flag of the SC0MD3 register to "1." (Reception data wait.)
- (9) When the serial reception begins, the SC0BSY flag of the serial interface 0 control register (SC0CTR) is set to "1," indicating that a serial transfer is in progress.
- (10) When the serial reception is complete, the SC0BSY flag of the SC0CTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SC0TRI flag of the SC0MD1 register is set to "1."



**After the transfer is complete, the transfer bit count in the SC0LNG2~0 flags of the SC0MD0 register will be changed. Except in an 8-bit transfer count, reset the transfer bit count at the time of the next reception.**



**When switching from reception to transmission, set the SC0SBIS flag of the SC0MD3 register to "0" and then set the SC0SBOS flag to "1." Do not change both of these flags at the same time.**

*When the serial port is enabled and the SC0CE1~0 flags of the SC0MD0 register are changed, the transfer bit count in the SC0LNG2~0 flags of the SC0MD0 register may be incremented.*

*[☞ Section 5-2-3, "Serial Interface Transfer Timing"]*

*If the start condition is enabled, the SC0LNG2~0 flags of the SC0MD0 register will be cleared when the start condition is received. In this case, the receive bit count is fixed at 8 bits.*

*The SC0SBTS flag of the SC0MD3 register must be set to "1" before setting the SC0SBIS flag of the SC0MD3 register to "1."*

*If the internal clock is selected as the clock source, after setting the SC0SBIS flag of the SC0MD3 register to "1," write dummy data to the SC0TRB register. If there is to be another reception, write dummy data again to the SC0TRB register.*

*The SC0LNG2~0 flags change at the opposite edge of the transmit data output edge.*

*Serial interface 0 begins operation when the SC0SBOS flag or the SC0SBIS flag is set to "1." Set the SC0SBOS flag or the SC0SBIS flag after all conditions have been set.*



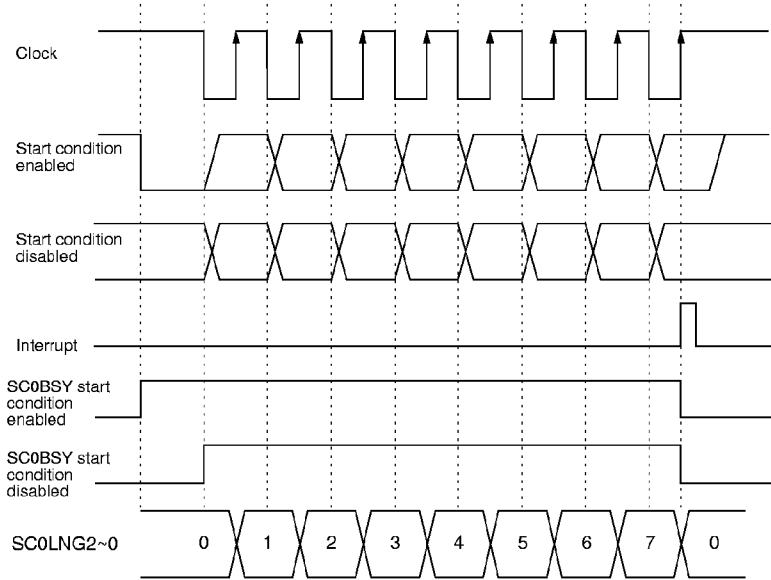


Figure 5-2-3 Synchronous Serial Interface Reception Timing  
(reception at rising edge)

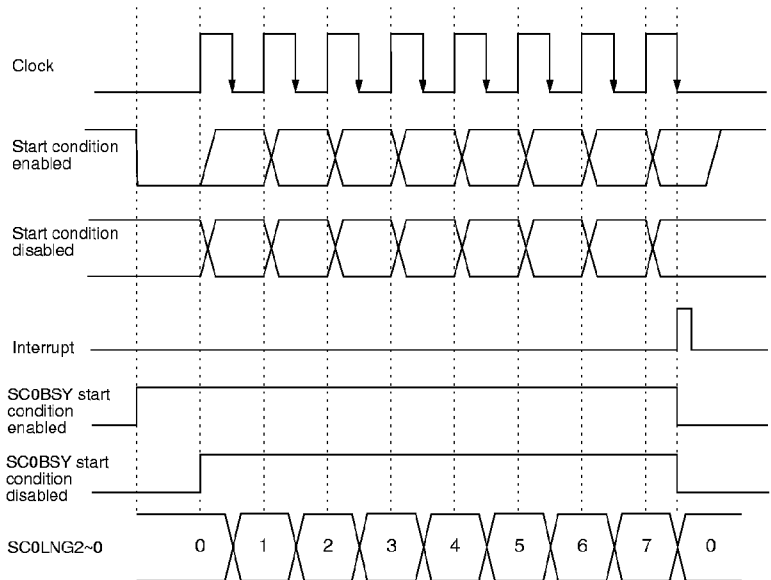


Figure 5-2-4 Synchronous Serial Interface Reception Timing  
(reception at falling edge)


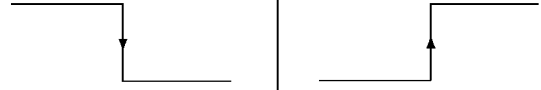
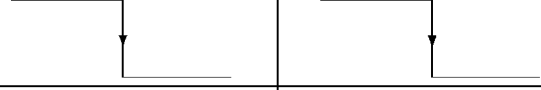
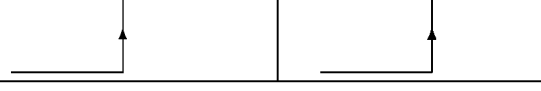
### 5-2-3 Serial Interface Transfer Timing

Serial interface 0 uses the SC0CE0 and SC0CE1 flags of serial interface 0 mode register 0 (SC0MD0), and serial interface 1 uses the SC1CE0 and SC1CE1 flags of serial interface 1 mode register 0, to control the edge at which transmission data is output and the edge at which reception data is input.

During transmission, when the SCnCE1 flag is "0," data output is synchronized to the falling edge of the clock.

During reception, when the SCnCE0 flag is "0," data reception is synchronized to the opposite polarity edge of the transmit data edge. When the SCnCE0 flag is "1," data reception is synchronized to the same polarity edge as the transmit data edge.

Table 5-2-1 Serial Data Input Edge and Output Edge (serial interface 0, 1)

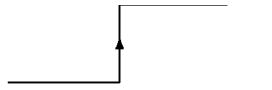
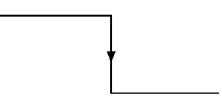
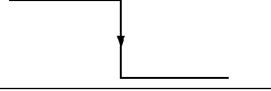
| SC0CE0 | SC0CE1 | Receive Data Input Edge   | Transmit Data Output Edge |
|--------|--------|---|---------------------------|
| 0      | 0      |  |                           |
| 0      | 1      |  |                           |
| 1      | 0      |  |                           |
| 1      | 1      |  |                           |

Serial interface 2 uses the SC2CE0 flag of the serial interface 2 mode register 0 to control the edge at which reception data is input.

During transmission, data is output in synchronization with the falling edge of the clock.

During reception, when the SC2CE0 flag is "0", data is input in synchronization with the rising edge of the clock. When the SC2CE0 flag is "1", data is input in synchronization with the falling edge of the clock.

Table 5-2-2 Serial Data Input Edge and Output Edge (serial interface 2)

| SC2CE0 | Receive Data Input Edge   | Transmit Data Output Edge   |
|--------|---|---|
| 0      |  |  |
| 1      |  |   |

When serial interface 0 and/or serial interface 1 are used for simultaneous transmission and reception, set the SCnCE0 and SCnCE1 flags of the SCnMD0 register to "00" or "01", so that the reception data input edge is opposite in polarity to the transmit data output edge. Also, the polarity of the reception data input edge is opposite polarity of the transmit data output edge of the other device.

When serial interface 2 is to be used for simultaneous synchronous serial transmission and reception, set the SC2CE0 flag of the SC2MD0 register to "0", so that the receive data input edge is opposite in polarity to the transmit data output edge. Also, set the transmit data output edge of the other device to the falling edge of the clock.

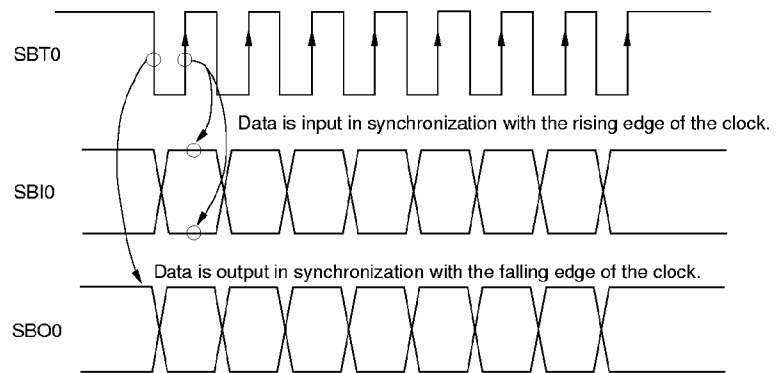


Figure 5-2-5 Synchronous Serial Transmit/Receive Timing  
(data is received at the rising edge and transmitted at the falling edge)

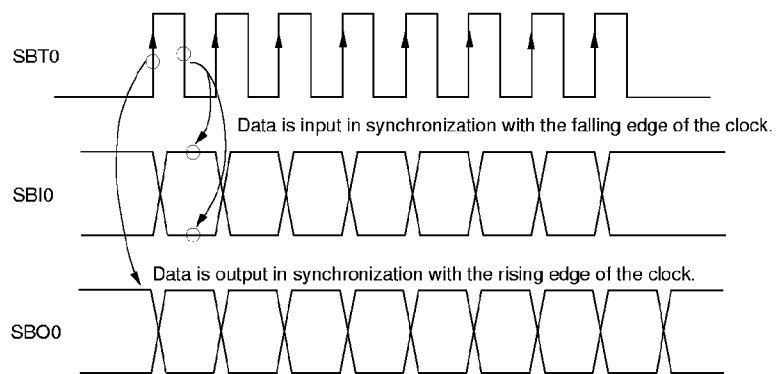


Figure 5-2-6 Synchronous Serial Transmit/Receive Timing  
(data is received at the falling edge and transmitted at the rising edge)

## 5-3 Simple UART Serial Interface

### 5-3-1 Overview

Setup and operation of UART transmission and reception are described below.

### 5-3-2 Setup and Operation

#### ■ Transmission

- (1) Select UART by setting the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "1."
- (2) Specify the first bit to be transferred (MSB first or LSB first) with the SCODIR flag of the serial interface 0 mode register 0 (SC0MD0).
- (3) Select the valid edge of the clock signal with the SC0CE1~0 flags of the SC0MD0 register.
- (4) Select the clock source with the SC0CK1~0 flags of serial interface 0 mode register 1 (SC0MD1).
- (5) Set the SC0CKM flag of the SC0MD1 register to "1" to divide the clock source frequency by 8.
- (6) Set the SC0NPE flag of the serial interface 0 mode register 2 (SC0MD2) to enable or disable parity.
- (7) If parity is enabled by the SC0NPE flag of the SC0MD2 register, set the SC0PM1~0 flags of the SC0MD2 register to specify the added parity bit.

*When the serial port is enabled and the SC0CE1~0 flags of the SC0MD0 register are toggled, the transfer bit count may change.*

*The TXD pin goes to a high level after transmission is complete.*



Setting the SC0FM flag of the SC0MD2 register to frame mode automatically sets the SC0LNG2~0 flags of the SC0MD0 register.



After the transfer is complete, the SC0LNG2~0 flags of the SC0MD0 register are automatically set with the transfer bit count.

*Serial interface 0 begins operation when the SC0SBOS flag or the SC0SBIS flag is set to "1." Set the SC0SBOS flag or the SC0SBIS flag after all conditions have been set.*

- (8) Set the SC0FM1~0 flags of the SC0MD2 register to specify the frame mode.
- (9) Set the SC0BRKE flag of the SC0MD2 register to control break status transmission.
- (10) Select the SC0SBOM flag of the SC0MD3 register.
- (11) Select the SC0IOM flag of the SC0MD3 register.
- (12) Set bit 0 of the port 0 direction control register (PODIR) to the output mode.
- (13) Select serial communication by setting the SC0SBOS flag of the SC0MD3 register to "1."
- (14) Set transmit data to serial interface 0 transmit/receive shift register (SC0TRB). This will start the serial transmission.
- (15) When the serial transmission begins, the SC0BSY flag of the SC0CTR register is set to "1," indicating that a serial transfer is in progress.
- (16) When the serial transmission is complete, the SC0BSY flag of the SC0CTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SC0TRI flag of the SC0MD1 register is cleared to "0."

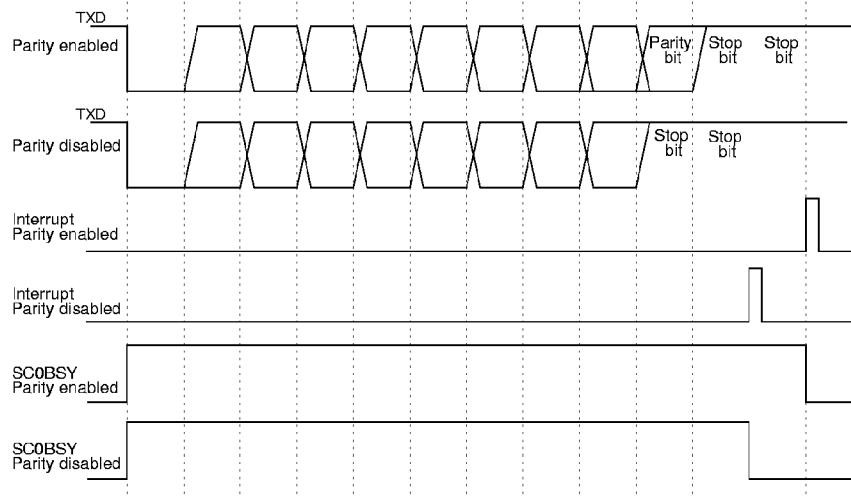


Figure 5-3-1 UART Transmission Timing

## ■ Reception

- (1) Select UART by setting the SCOCMD flag of the serial interface 0 control register (SCOCTR) to "1."
- (2) Specify the first bit to be transferred (MSB first or LSB first) with the SCODIR flag of the serial interface 0 mode register 0 (SCOMD0).
- (3) Select the valid edge of the clock signal with the SCOCE1~0 flags of the SCOMD0 register.
- (4) Select the clock source with the SCOCK1~0 flags of serial interface 0 mode register 1 (SCOMD1).
- (5) Set the SCOCKM flag of the SCOMD1 register to "1" to divide the clock source frequency by 8.
- (6) Set the SCONPE flag of the serial interface 0 mode register 2 (SCOMD2) to enable or disable parity.
- (7) If parity is enabled by the SCONPE flag of the SCOMD2 register, set the SCOPM1~0 flags of the SCOMD2 register to specify the added parity bit.
- (8) Set the SCOFM1~0 flags of the SCOMD2 register to specify the frame mode.
- (9) Select the SCOIOM flag of the SCOMD3 register.
- (10) When the SCOIOM flag of the SCOMD3 register is specified that the pin is independent, set bit 1 of the port 0 direction control register (PODIR) to the input mode.
- (11) Set bit 0 of the port 0 pull-up resistor control register (POPIU).
- (12) Select serial communication by setting the SCOSBIS flag of the SCOMD3 register to "1."
- (13) When the serial transmission begins, the SCOSBY flag of the SCOCTR register is set to "1," indicating that a serial transfer is in progress.
- (14) When the serial transmission is complete, the SCOSBY flag of the SCOCTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SCOTRI flag of the SCOMD1 register is cleared to "1."

*When the serial port is enabled and the SCOCE1~0 flags of the SCOMD0 register are toggled, the transfer bit count may change.*

*The TXD pin goes to a high level after reception is complete.*

*Serial interface 0 begins operation when the SCOSBOS or SCOSBIS flag is set to "1." Set the SCOSBOS or SCOSBIS flag after all conditions have been set.*

*One machine cycle after the stop bit has been received, the start condition will no longer be accepted. Therefore, consecutive reception must be performed carefully.*



**Setting the SCOFM flag of the SCOMD2 register to frame mode automatically sets the SCOLNG2~0 flags of the SCOMD0 register.**



**After the transfer is complete, the SCOLNG2~0 flags of the SCOMD0 register are automatically set with the transfer bit count.**

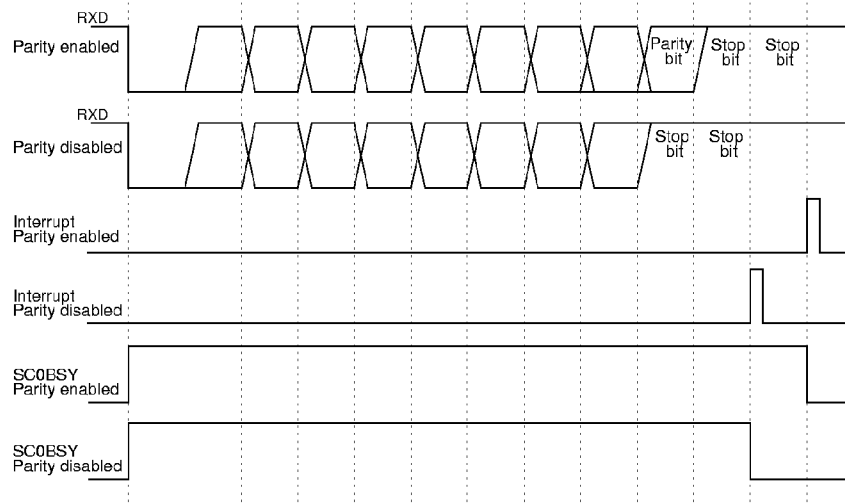


Figure 5-3-2 UART Reception Timing

### 5-3-3 How to Use the Baud Rate Timer

Refer to the following when using the baud rate timer to set the UART transfer speed.

- (1) Specifying the timer clock source

The clock source is specified by the TM3CK3~1 flags of the timer 3 mode register (TM3MD).

- (2) Setting the compare register

The compare register value is set in the timer 3 compare register (TM3OC).

This set value is computed according to the following formula:

$$\text{overflow period} = (\text{compare register set value} + 1) \times \text{timer clock period}$$

$$\text{baud rate} = 1/(\text{overflow period} \times 2 \times 8)$$

$$\uparrow \text{SC0MD1(SC0CKM)}$$

$$\text{compare register set value} = \text{timer clock frequency}/(\text{baud rate} \times 2 \times 8) - 1$$

Table 5-3-1 UART Transfer Rate

| Transfer Speed<br>fosc<br>(MHz) | Transfer Speed<br>(bps) | 300       |                  | 1200      |                  | 2400      |                  | 4800      |                  | 9600      |                  | 19200     |                  |
|---------------------------------|-------------------------|-----------|------------------|-----------|------------------|-----------|------------------|-----------|------------------|-----------|------------------|-----------|------------------|
|                                 |                         | Set Value | Calculated Value | Set Value | Calculated Value | Set Value | Calculated Value | Set Value | Calculated Value | Set Value | Calculated Value | Set Value | Calculated Value |
| 4.0                             | fosc                    | —         | —                | 208       | 1202             | 104       | 2403             | 52        | 4807             | 26        | 9615             | 13        | 19230            |
|                                 | fs/4                    | 104       | 300              | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
|                                 | fs/16                   | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
| 4.19                            | fosc                    | —         | —                | 218       | 1201             | 109       | 2402             | 55        | 4761             | 27        | 9699             | —         | —                |
|                                 | fs/4                    | 109       | 300              | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
|                                 | fs/16                   | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
| 8.0                             | fosc                    | —         | —                | —         | —                | 208       | 2404             | 104       | 4807             | 52        | 9615             | 26        | 19230            |
|                                 | fs/4                    | 208       | 300              | 52        | 1201             | —         | —                | —         | —                | —         | —                | —         | —                |
|                                 | fs/16                   | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
| 8.38                            | fosc                    | —         | —                | —         | —                | 218       | 2403             | 109       | 4805             | 55        | 9523             | 27        | 19398            |
|                                 | fs/4                    | 218       | 300              | 55        | 1190             | —         | —                | —         | —                | —         | —                | —         | —                |
|                                 | fs/16                   | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
| 12.0                            | fosc                    | —         | —                | —         | —                | —         | —                | 156       | 4808             | 78        | 9615             | 39        | 19230            |
|                                 | fs/4                    | —         | —                | 78        | 1202             | 39        | 2403             | —         | —                | —         | —                | —         | —                |
|                                 | fs/16                   | 78        | 300              | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
| 16.0                            | fosc                    | —         | —                | —         | —                | —         | —                | 208       | 4808             | 104       | 9615             | 52        | 19230            |
|                                 | fs/4                    | —         | —                | 104       | 1202             | 52        | 2404             | —         | —                | —         | —                | —         | —                |
|                                 | fs/16                   | 104       | 300              | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
| 16.76                           | fosc                    | —         | —                | —         | —                | —         | —                | 218       | 4805             | 109       | 9610             | 55        | 19045            |
|                                 | fs/4                    | —         | —                | 109       | 1201             | 55        | 2381             | —         | —                | —         | —                | —         | —                |
|                                 | fs/16                   | 109       | 300              | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |
| 20.0                            | fosc                    | —         | —                | —         | —                | —         | —                | —         | —                | 130       | 9615             | 65        | 19231            |
|                                 | fs/4                    | —         | —                | 130       | 1202             | 65        | 2404             | 33        | 4735             | —         | —                | —         | —                |
|                                 | fs/16                   | 130       | 300              | —         | —                | —         | —                | —         | —                | —         | —                | —         | —                |

Set the values from this table (minus 1) in the compare register.

Example:

The timer 3 clock source is fs/4 (fosc = 8MHz) and a baud rate of 300 bps is desired.

Since fs=fosc/2,

$$\text{compare register set value} = (8 \times 10^6/2/4)/(300 \times 2 \times 8) - 1$$

$$=207$$

$$= \text{X'CF'}$$



## 5-4 Simple IIC Serial Interface

### 5-4-1 Overview

The simple IIC serial interface is a single master bus. Several devices may be connected as slaves.

### 5-4-2 Setup and Operating Procedure

#### ■ Transmission (1-byte transmission, then transmission of n-bytes)

*Set the CLKPOL2 flag of the SC2MD0 register to "1" before setting the SC2LNG3~0 flags of the SC2MD0 register.*

- (1) Set bit 2 of port 3.
  - Set bit 2 of the port 3 output register (P3OUT) to "1" ("H" level).
  - Set bit 2 of the port 3 direction control register (P3DIR) to "1" (output mode).
- (2) Set bit 0 of port 3.
  - Set bit 0 of the P3OUT register to "1" ("H" level).
  - Set bit 0 of the P3DIR register to "1" (output mode).
- (3) Set bit 0 of the port 3 output register (P3OUT) to "0" ("L" level) to output the start condition.
- (4) Set the SC2MD0 register.
  - Set the SC2CMD flag of the SC2MD0 register to "1" (IIC mode).
  - Set the SC2LNG3~0 flags of the SC2MD0 register to specify the transfer bit count as 9 bits.
  - Set the SC2STE flag of the SC2MD0 register to disable the start condition.
  - Set the SC2DIR flag of the SC2MD0 register to MSB first.
  - Set the SC2CE0 flag of the SC2MD0 register so that reception data is input on the falling edge.
- (5) Set the SC2MD1 register.
  - Set the SC2CK2~0 flags of the SC2MD1 register to specify the clock source as 1/2 of the overflow of timer 0.
  - Set the SC2SBTS flag of the SC2MD1 register to "1" (serial clock pin).
  - Set the SC2SBTM flag of the SC2MD1 register.
  - Set the SC2SBOM flag of the SC2MD1 register.
- (6) Set the SC2CTR register.
  - Set the SC2ACKO flag of the SC2CTR register to "1" ("H" level). (During transmission, the output level is the same as the 9th bit of data (the ACK bit)).
  - Set the SC2ACKS flag of the SC2CTR register to "1" to enable the ACK bit.
  - Set the SC2SBOM flag of the SC2CTR register to "1" (connected).

*The SC2SPKF, SC2STKF, SC2SPEN, and SC2STEN flags of the SC2CTR register are normally set to "0".*

- (7) Set the SIFOEO2 and SIFOEI2 flags of the SC2MD1 register to "1" to enable the serial port.
- (8) Write data to the serial interface 2 transmit/receive shift register (SC2TRB) to start the serial transmission.
- (9) When the transmission of 9-bit data (8 data bits + ACK bit) is complete, the SC2 transfer complete interrupt will be received.
- (10) Read the SIFACK flag of the SC2CTR register and determine the value of the ACK bit.  
If the transmission is complete, go to (13).  
If the transmission is continuing, go to (11).
- (11) Set the SC2MD0 register.  
• Set the SC2LNG3~0 flags of the SC2MD0 register to specify the transfer bit count as 9 bits.
- (12) Set the SC2CTR register.  
• Set the SC2ACKO flag of the SC2CTR register to "1" ("H" level). (During transmission, the output level is the same as the 9th bit of data (the ACK bit)).  
Repeat processing from step (8).
- (13) Set bit 2 and bit 0 of the P3OUT register to "0".
- (14) Set the SC2SBOS, SC2SBIS, SC2SBTS flags of the SC2MD1 register to "0".  
(Switch the SBT2 and SBO2 pins to function as ports.)
- (15) Set bit 2 of the P3OUT register to "1".
- (16) Set bit 0 of the P3OUT register to "1".

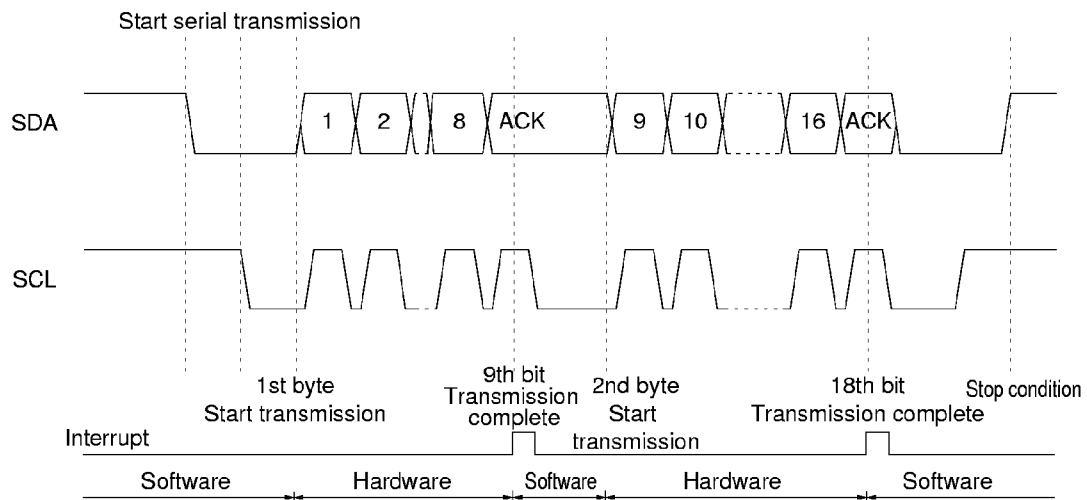


Figure 5-4-1 Master Transmission

■ Reception (1-byte transmission, then reception of n-bytes)

- (1) Set bit 2 of port 3.
  - Set bit 2 of the port 3 output register (P3OUT) to "1" ("H" level).
  - Set bit 2 of the port 3 direction control register (P3DIR) to "1" (output mode).
- (2) Set bit 0 of port 3.
  - Set bit 0 of the P3OUT register to "1" ("H" level).
  - Set bit 0 of the P3DIR register to "1" (output mode).
- (3) Set bit 0 of the port 3 output register (P3OUT) to "0" ("L" level) to output the start condition.
- (4) Set the SC2MD0 register.
  - Set the SC2CMD flag of the SC2MD0 register to "1" (IIC mode).
  - Set the SC2LNG3~0 flags of the SC2MD0 register to specify the transfer bit count as 9 bits.
  - Set the SC2STE flag of the SC2MD0 register to disable the start condition.
  - Set the SC2DIR flag of the SC2MD0 register to MSB first.
  - Set the SC2CE0 flag of the SC2MD0 register so that reception data is input on the falling edge.
- (5) Set the SC2MD1 register.
  - Set the SC2CK2~0 flags of the SC2MD1 register to specify the clock source as 1/2 of the overflow of timer 0.
  - Set the SC2SB1S flag of the SC2MD1 register to "1" (serial clock pin).
  - Set the SC2SBTM flag of the SC2MD1 register.
  - Set the SC2SBOM flag of the SC2MD1 register.
- (6) Set the SC2CTR register.
  - Set the SC2ACKO flag of the SC2CTR register to "1" ("H" level). (During transmission, the output level is the same as the 9th bit of data (the ACK bit)).
  - Set the SC2ACKS flag of the SC2CTR register to "1" to enable the ACK bit.
  - Set the SC2SBOM flag of the SC2CTR register to "1" (connected).
- (7) Set the SC2SBOS and SC2SBIS flags of the SC2MD1 register to "1" to enable the serial port.
- (8) Write data to the serial interface 2 transmit/receive shift register (SC2TRB) to start the serial transmission.
- (9) When the transmission of 9-bit data (8 data bits + ACK bit) is complete, an SC2 transfer complete interrupt will be received.
- (10) Read the SIFACK flag of the SC2CTR register and determine the value of the ACK bit.

*Set the SC2CMD flag of the SC2MD0 register to "1" before setting the SC2LNG3~0 flags of the SC2MD0 register.*

*The SC2SPKF, SC2STKF, SC2SPEN, and SC2STEN flags of the SC2CTR register are normally set to "0".*

The reception process is described in the following steps.

- (11) Set the SC2MD0 register.
  - Set the SC2LNG3~0 flags of the SC2MD0 register to specify the transfer bit count as 8 bits.
- (12) Set bit 0 of the P3DIR register to "0" (input mode).
- (13) Write dummy data to the serial interface 2 transmit/receive shift register (SC2TRB) to start the serial reception.
- (14) When the reception of 8-bit data is complete, the SC2 transfer complete interrupt will be received. The 8-bit received data is input to the serial interface 2 transmit/receive shift register (SC2TRB).

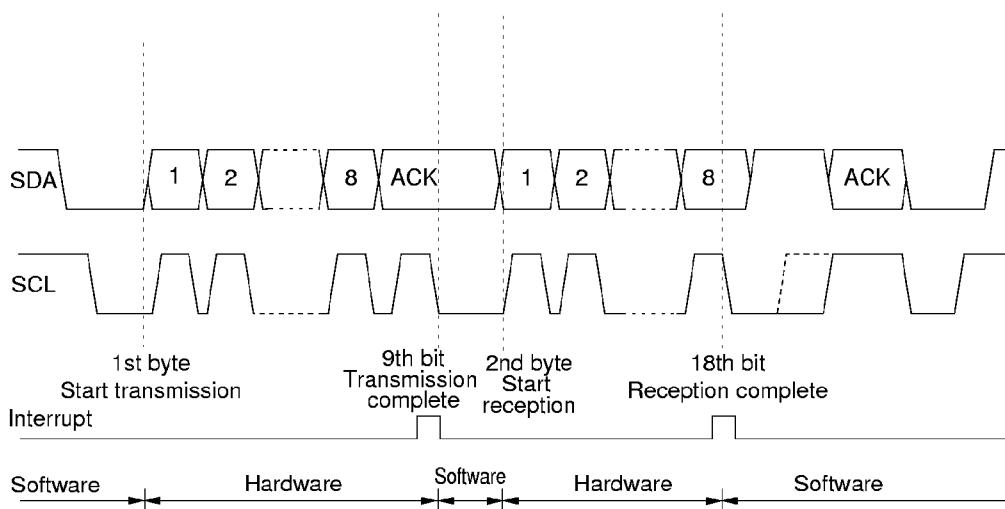


Figure 5-4-2 Master Reception

Control and processing of the ACK bit are described in steps (15)~(19) below.

- (15) Set bit 2 of the P3OUT register to "0".
- (16) Set the SC2SBOS, SC2SBIS, SC2SBTS flags of the SC2MD1 register to "0".  
(Switch the SBT2 and SBO2 pins to function as ports.)
- (17) Set bit 2 of the P3OUT register to "1".
- (18) Set bit 0 of the P3OUT register to "0". (In the case of NACK, set to "1").
- (19) Set bit 0 of the P3DIR register to "1" (output mode).  
If the reception is complete, go to (23).  
If the reception is continuing, go to (20).
- (20) Set the SC2MD0 register.
  - Set the SC2BC03~0 flags of the SC2MD0 register to specify the transfer bit count as 8 bits.
- (21) Set the SC2SBTS flag of the SC2MD1 register to "1". (Switch the SBT2 pin to a serial clock pin).
- (22) Set the SC2SBOS and SC2SBIS flags of the SC2MD1 register to "0". (Switch the SBO2 pin to serial).  
Repeat processing from step (13).
- (23) Set bit 2 and bit 0 of the P3OUT register to "0".
- (24) Set the SC2SBOS, SC2SBIS and SC2SBTS flags of the SC2MD1 register to "0". (Switch the SBT2 and SBO2 pins to function as ports.)
- (25) Set bit 2 of the P3OUT register to "1".
- (26) Set bit 0 of the P3OUT register to "1".

*The SC2SBTS flags of the SC2MD1 register must be set to "1" before setting the SC2SBOS and SC2SBIS flags of the SC2MD1 register to "1".*

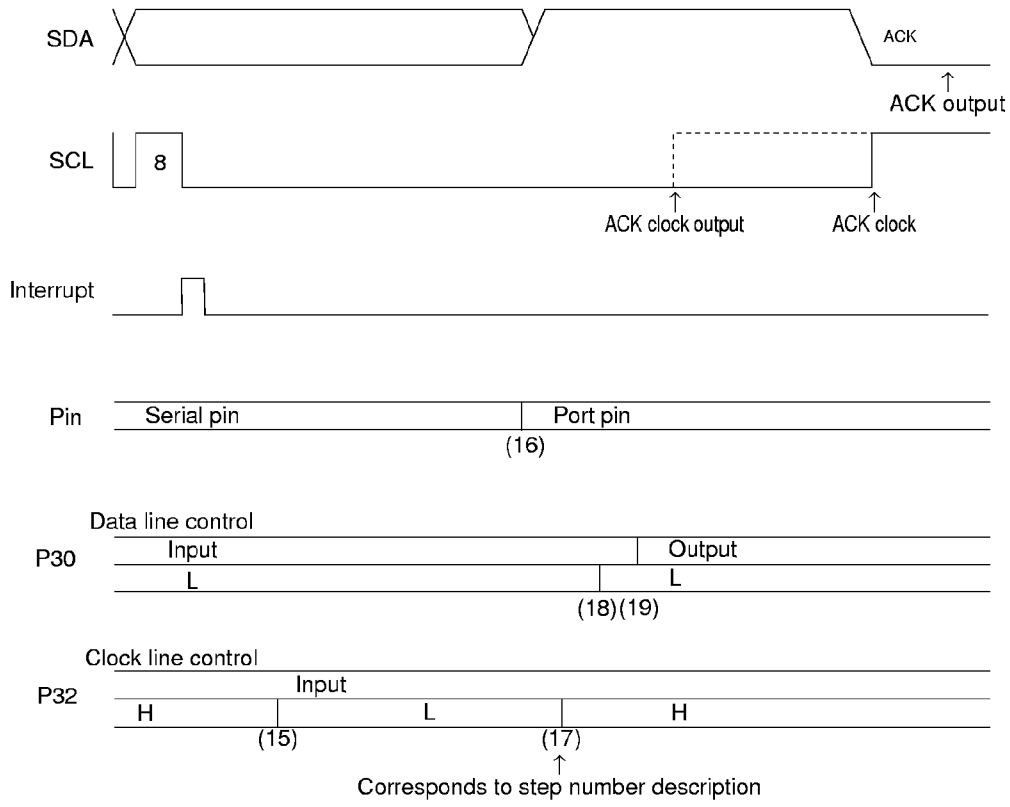


Figure 5-4-3 ACK Processing during Reception

## 5-5 Serial Interface Control Registers

### 5-5-1 Overview

Fourteen registers control the serial interface. See table 5-5-1.

Table 5-5-1 Serial Interface Registers

| Name   | Address  | R/W | Function   |
|--------|----------|-----|--|
| SC0MD0 | X'03F50' | R/W | Serial interface 0 mode register 0                 |
| SC0MD1 | X'03F51' | R/W | Serial interface 0 mode register 1                 |
| SC0MD2 | X'03F52' | R/W | Serial interface 0 mode register 2                 |
| SC0MD3 | X'03F53' | R/W | Serial interface 0 mode register 3                 |
| SC1MD0 | X'03F57' | R/W | Serial interface 1 mode register 0                 |
| SC1MD1 | X'03F58' | R/W | Serial interface 1 mode register 1                 |
| SC2MD0 | X'03F5A' | R/W | Serial interface 2 mode register 0                 |
| SC2MD1 | X'03F5B' | R/W | Serial interface 2 mode register 1                 |
| SC0CTR | X'03F54' | R/W | Serial interface 0 control register                |
| SC2CTR | X'03F5C' | R/W | Serial interface 2 control register                |
| SC0TRB | X'03F55' | W   | Serial interface 0 transmit/receive shift register |
| SC0RXB | X'03F56' | R   | Serial interface 0 receive data buffer             |
| SC1TRB | X'03F59' | R/W | Serial interface 1 transmit/receive shift register |
| SC2TRB | X'03F5D' | R/W | Serial interface 2 transmit/receive shift register |

## 5-5-2 Transmit/Receive Shift Registers, Receive Data Buffer

### (1) Serial interface 0 transmit/receive shift register (SC0TRB)

This 8-bit, writable register shifts the transmission data and the reception data. The direction of transfer can be specified as LSB first or MSB first.

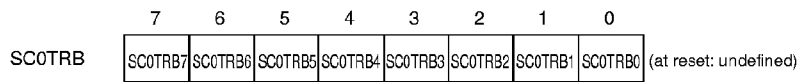


Figure 5-5-1 Serial Interface 0 Transmit/Receive Shift Register  
(SC0TRB: X'03F55', W)

### (2) Serial interface 0 received data buffer (SC0RXB)

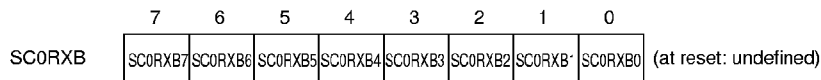


Figure 5-5-2 Serial Interface 0 Receive Data Buffer  
(SC0RXB: X'03F56', R)

### (3) Serial interface 1 transmit/receive shift register (SC1TRB)

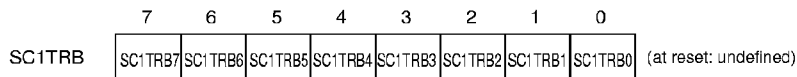


Figure 5-5-3 Serial Interface 1 Transmit/Receive Shift Register  
(SC1TRB: X'03F59', R/W)

### (3) Serial interface 2 transmit/receive shift register (SC2TRB)

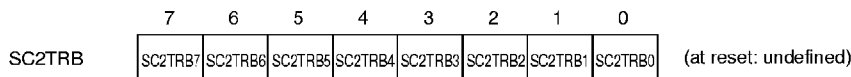


Figure 5-5-4 Serial Interface 2 Transmit/Receive Shift Register  
(SC2TRB: X'03F5D', R/W)



### 5-5-3 Serial Interface Mode Registers

(1) Serial interface 0 mode register (SC0MD0)

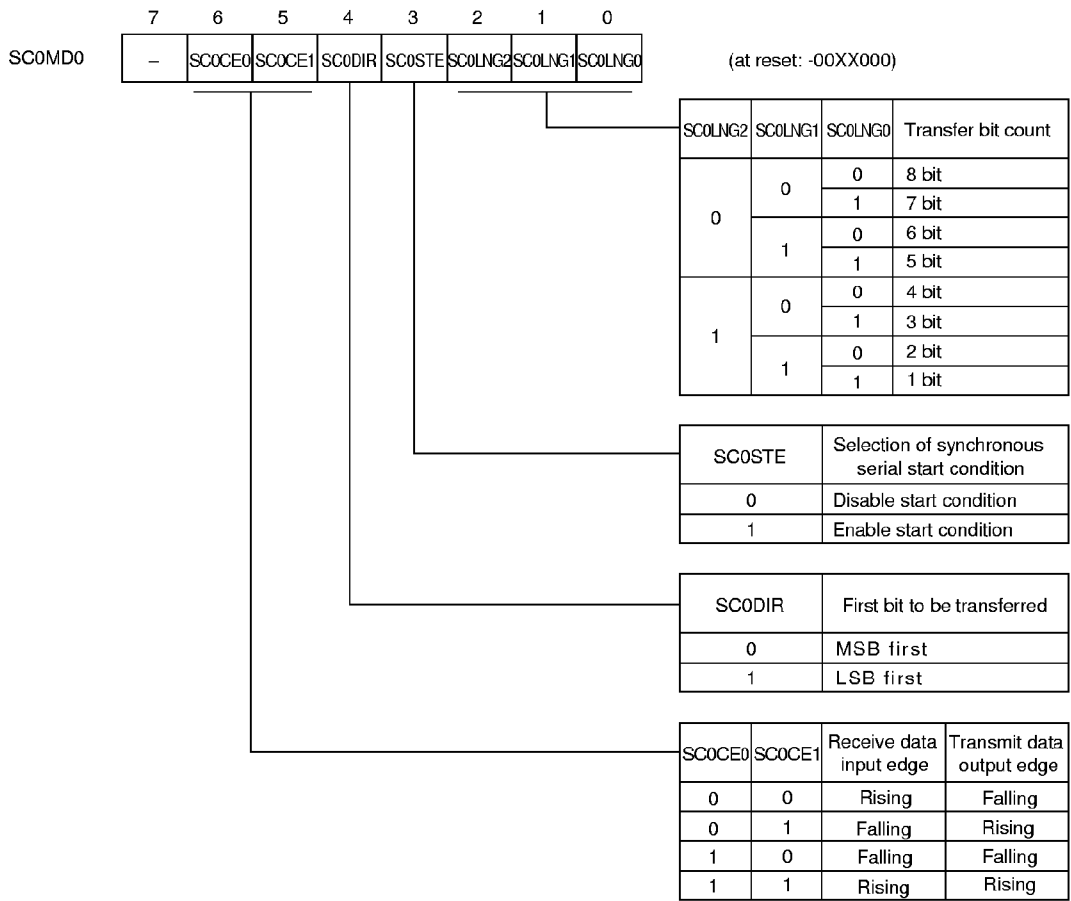


Figure 5-5-5 Serial Interface 0 Mode Register 0 (SC0MD0: X'03F50', R/W)

(2) Serial interface 0 mode register 1 (SC0MD1)

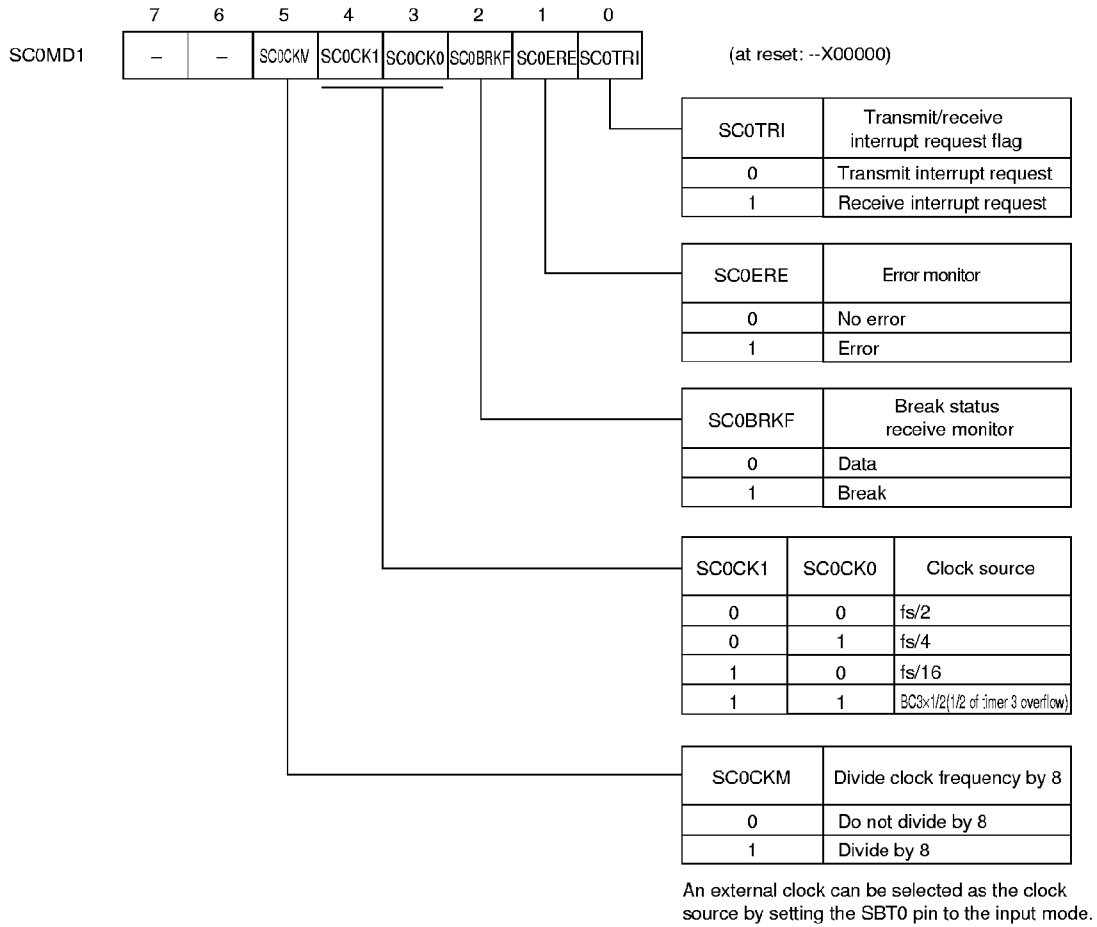


Figure 5-5-6 Serial Interface 0 Mode Register 1 (SC0MD1: X'03F51', R/W)

(3) Serial interface 0 mode register 2 (SC0MD2)

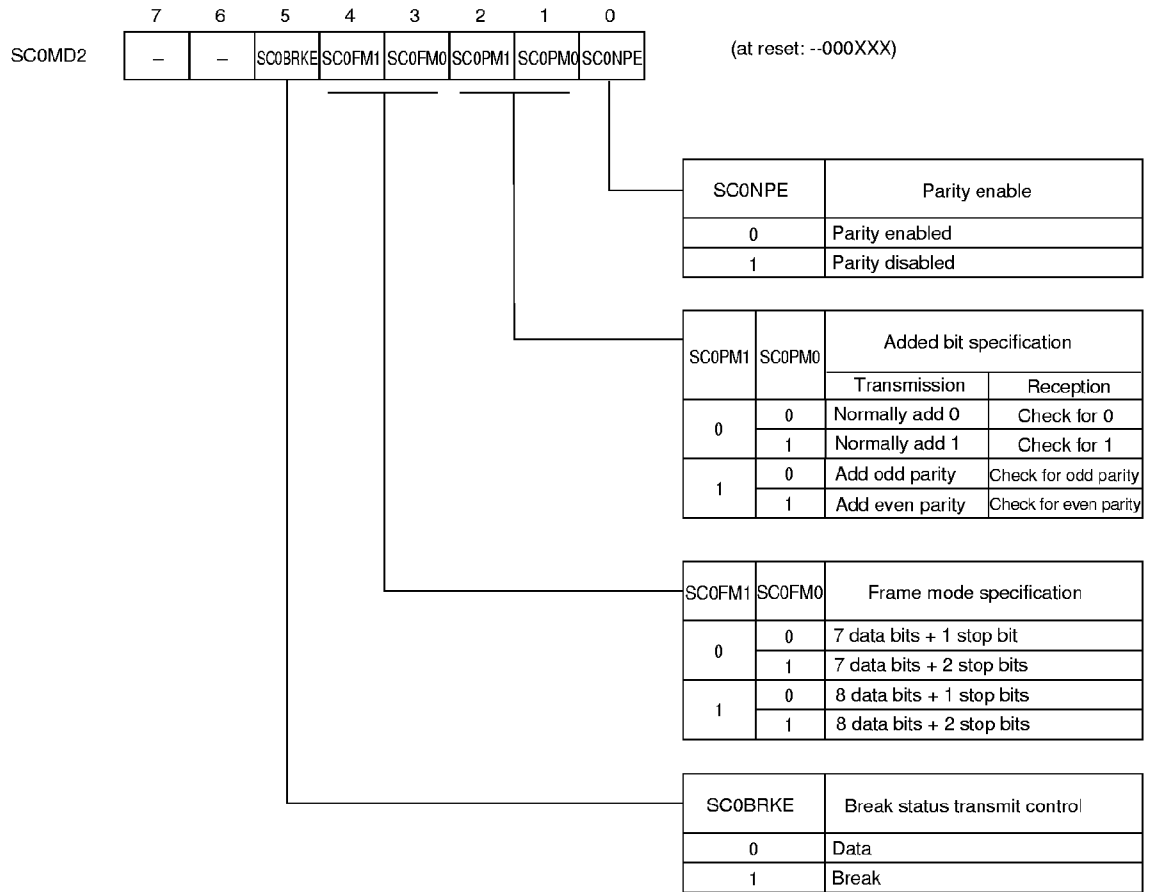


Figure 5-5-7 Serial Interface 0 Mode Register 2 (SC0MD2: X'03F52', R/W)

(4) Serial interface 0 mode register 3 (SC0MD3)

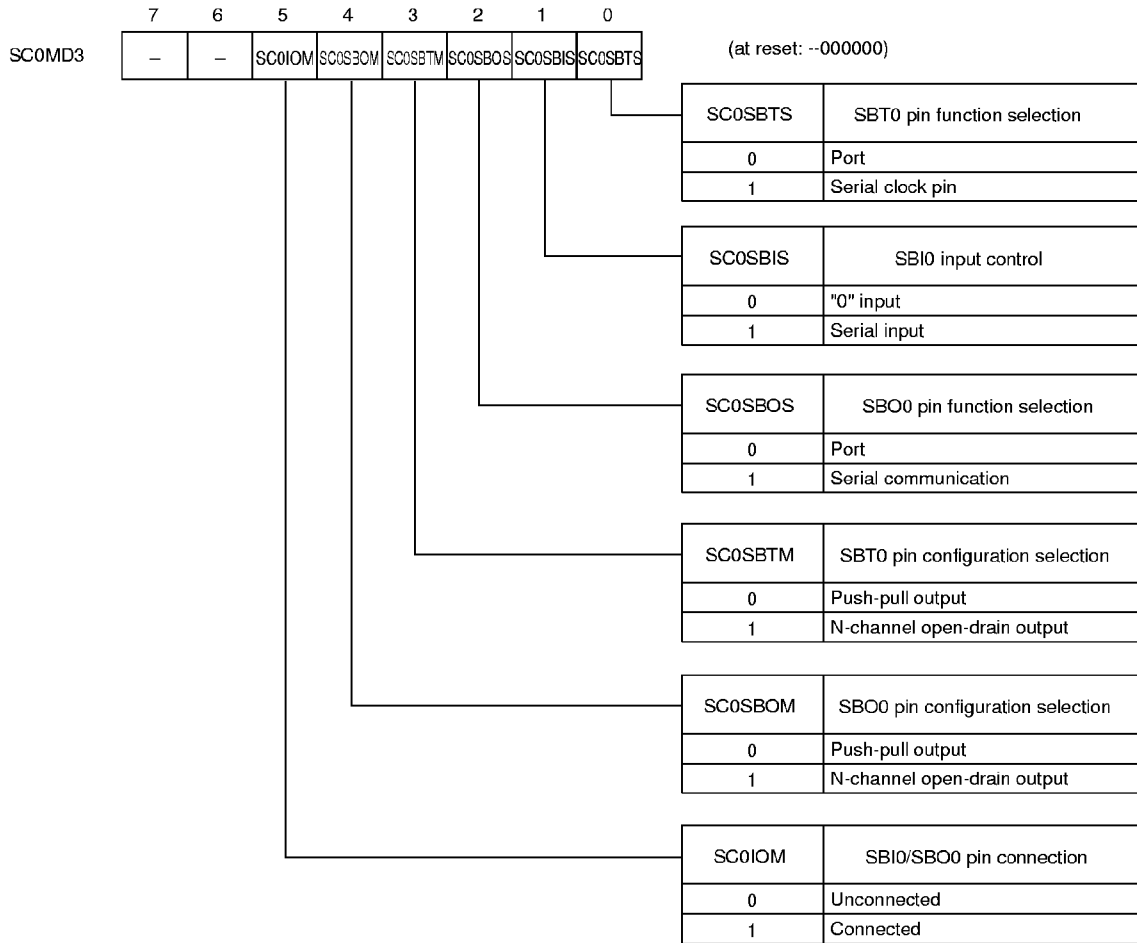


Figure 5-5-8 Serial Interface 0 Mode Register 3 (SC0MD3: X'03F53', R/W)

(5) Serial interface 1 mode register 0 (SC1MD0)

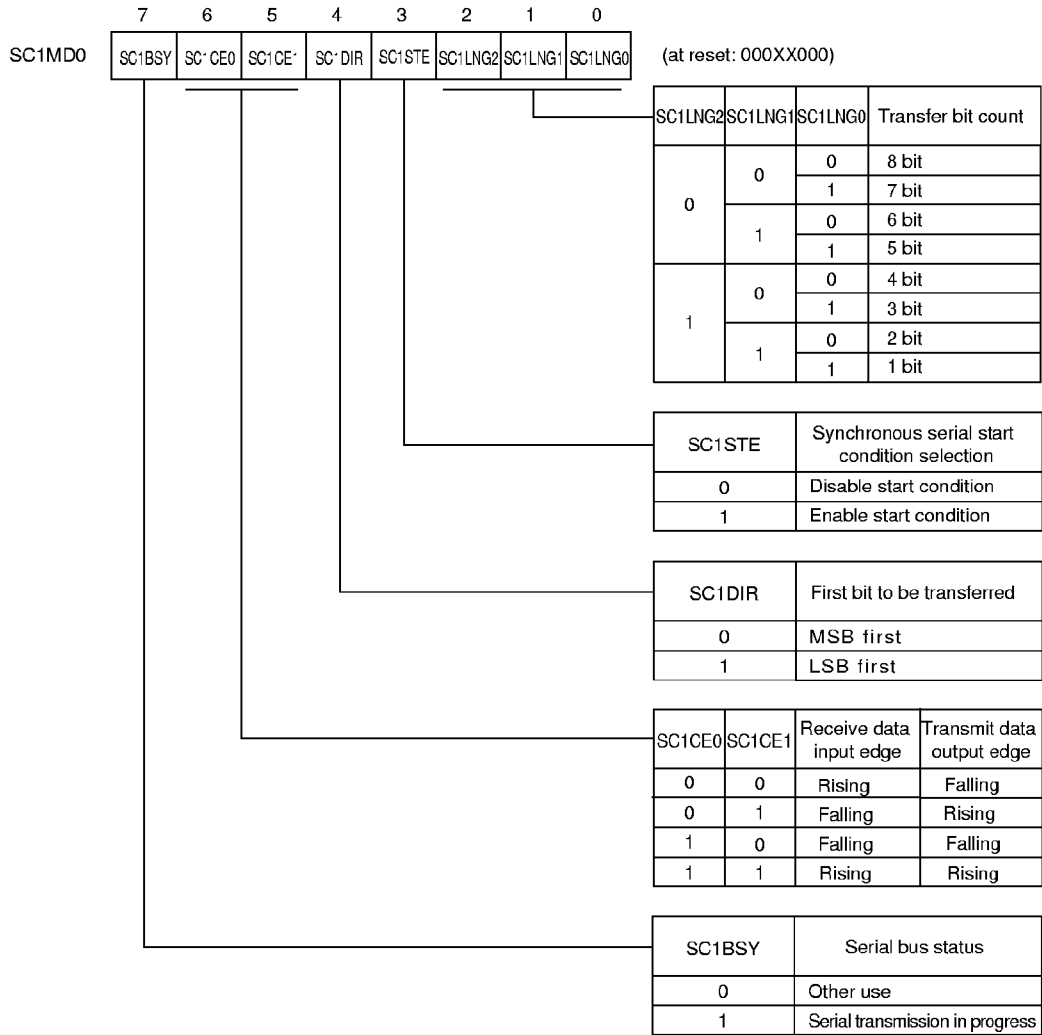


Figure 5-5-9 Serial Interface 1 Mode Register 0 (SC1MD0: X'03F57', R/W)

(6) Serial interface 1 mode register 1 (SC1MD1)

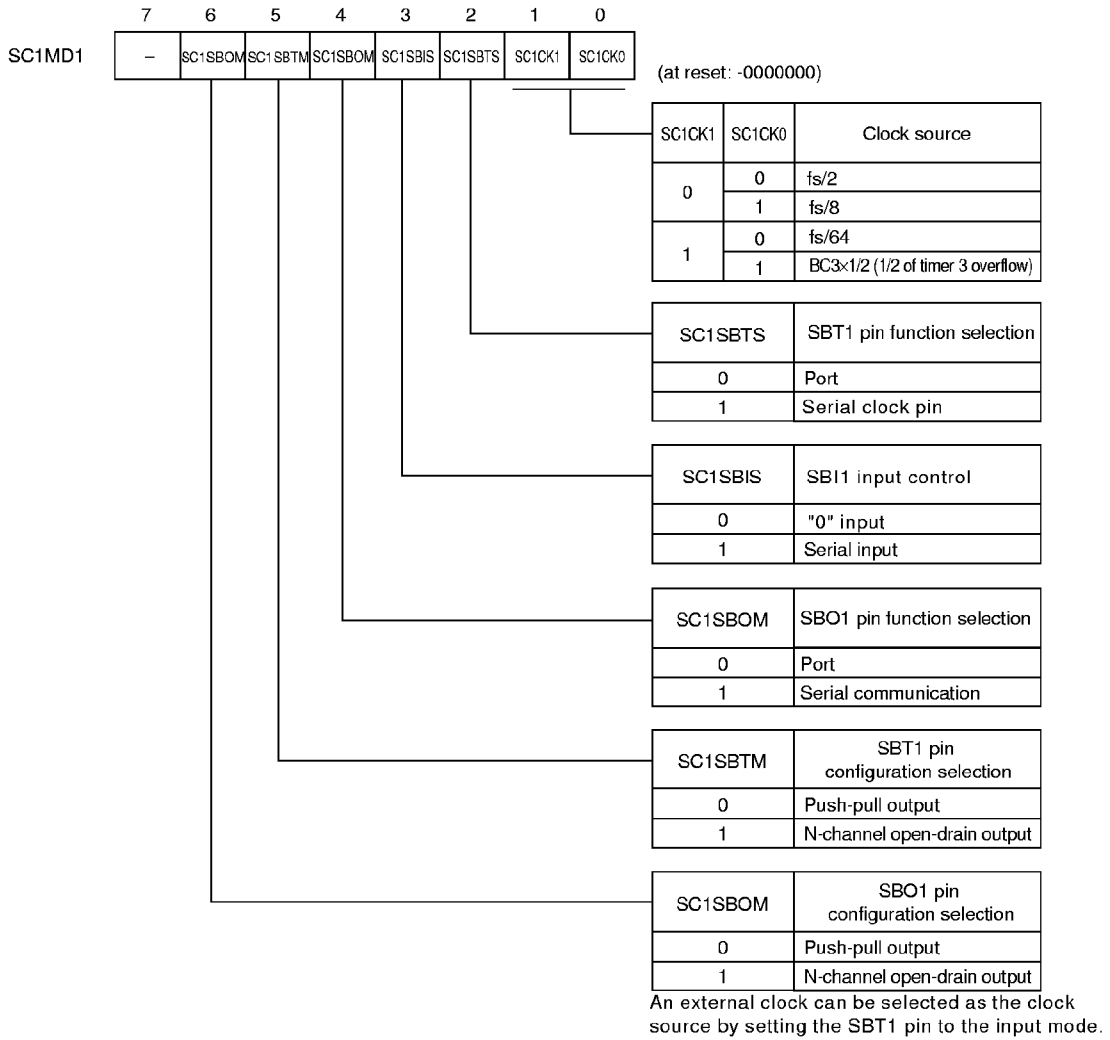


Figure 5-5-10 Serial Interface 1 Mode Register 1 (SC1MD1: X'03F58', R/W)

(7) Serial interface 2 mode register 0 (SC2MD0)

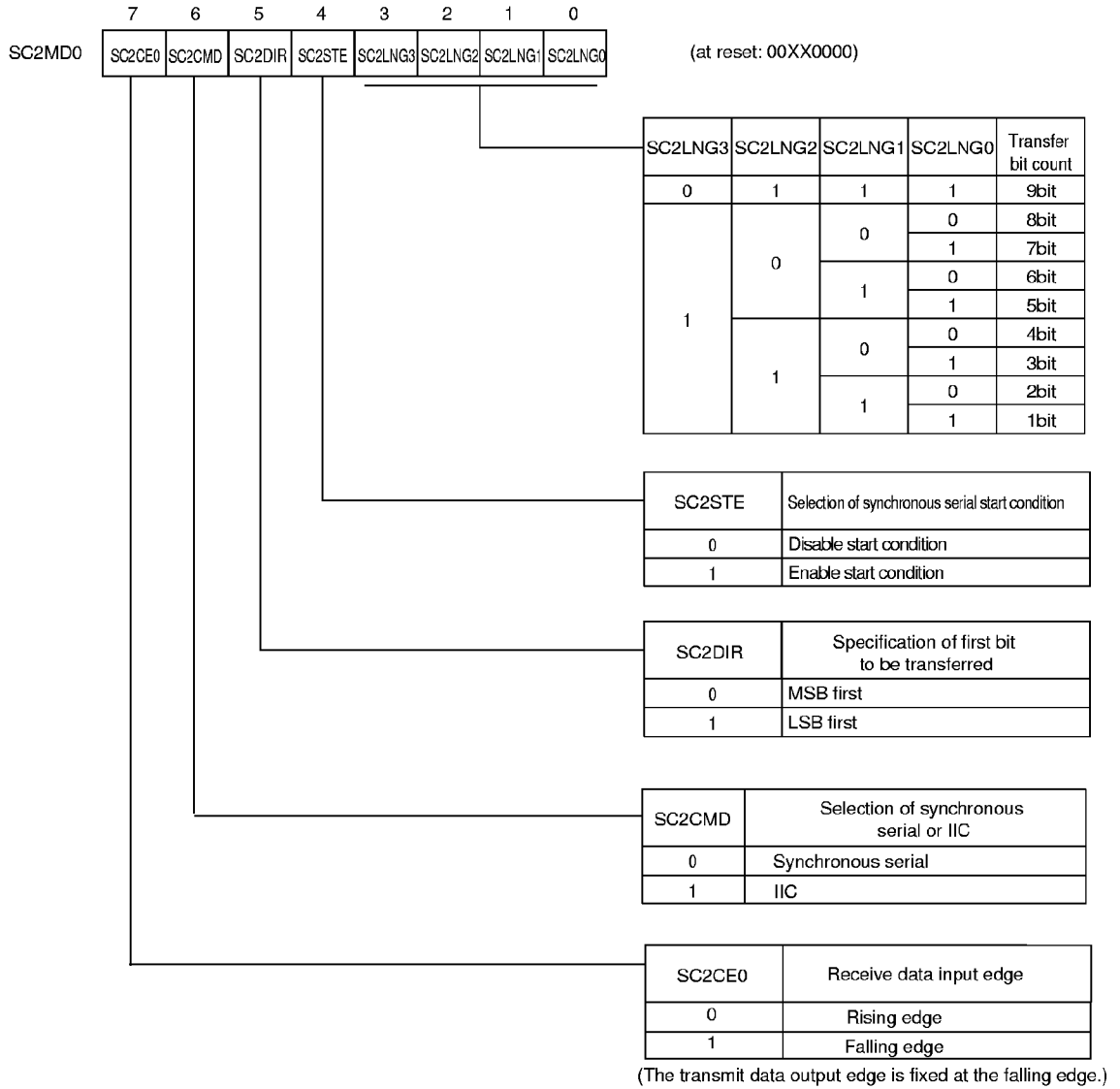


Figure 5-5-11 Serial Interface 2 Mode Register 0 (SC2MD0: X'03F5A', R/W)

(8) Serial interface 2 mode register 1 (SC2MD1)

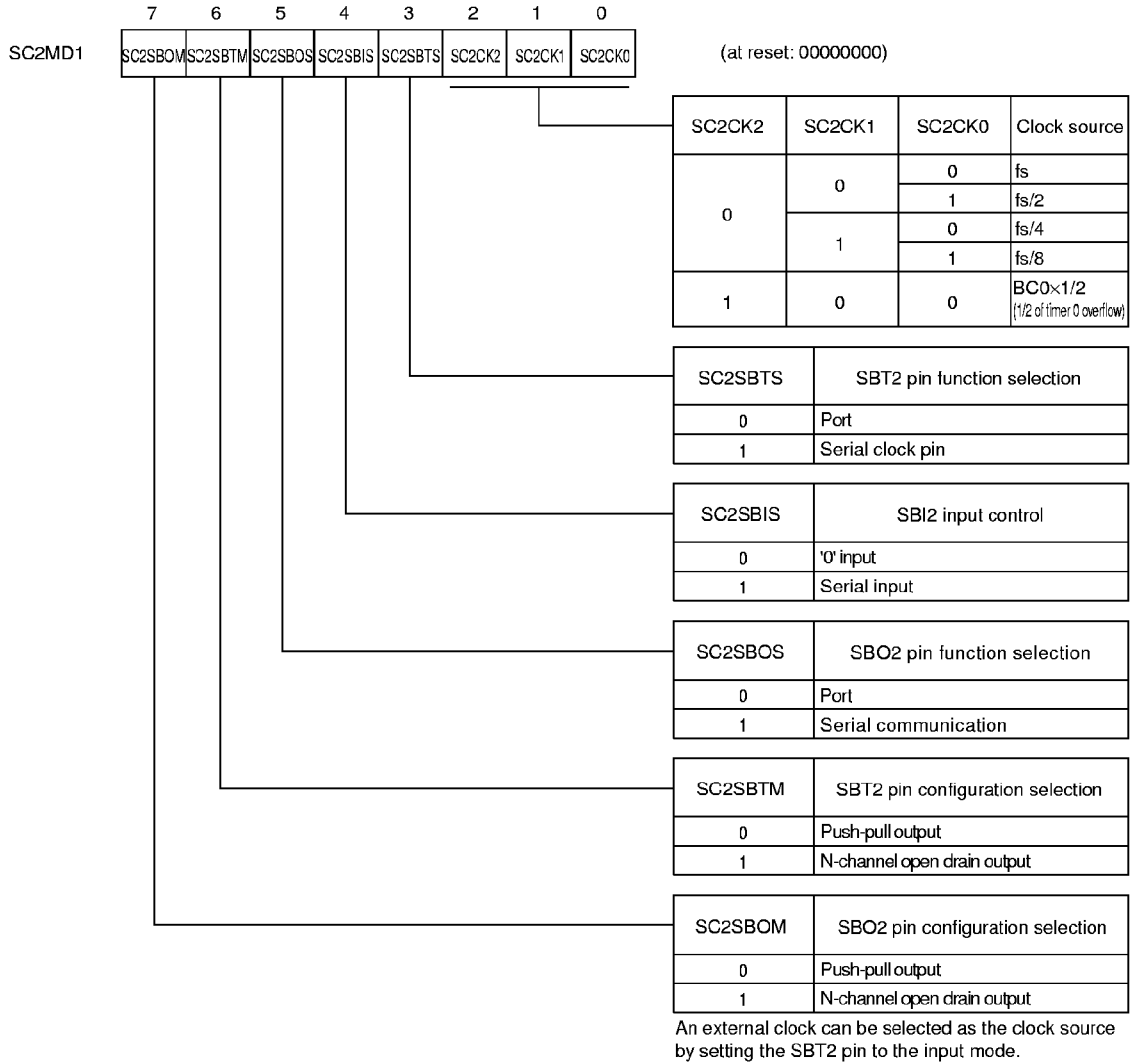


Figure 5-5-12 Serial Interface 2 Mode Register 1 (SC2MD1: X'03F5B', R/W)



### 5-5-4 Serial Interface Control Register

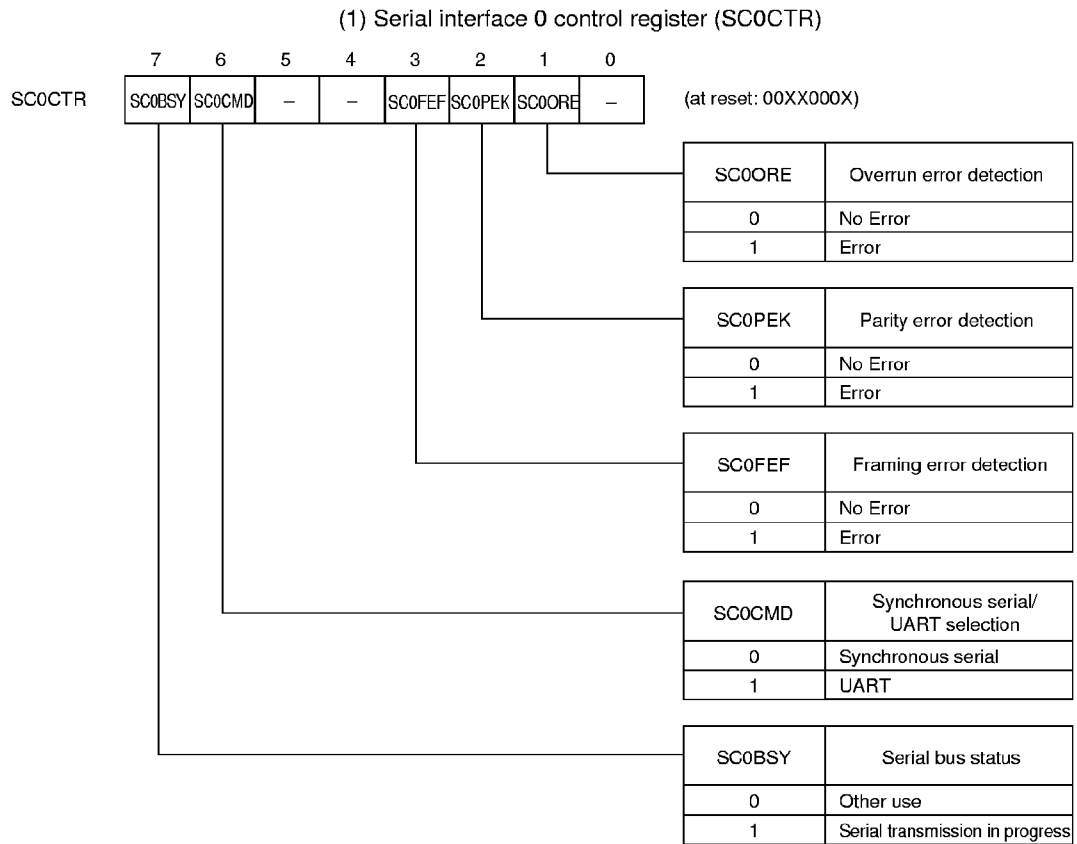


Figure 5-5-13 Serial Interface 0 Control Register (SC0CTR: X'03F54', R/W)

(2) Serial interface 2 control register (SC2CTR)

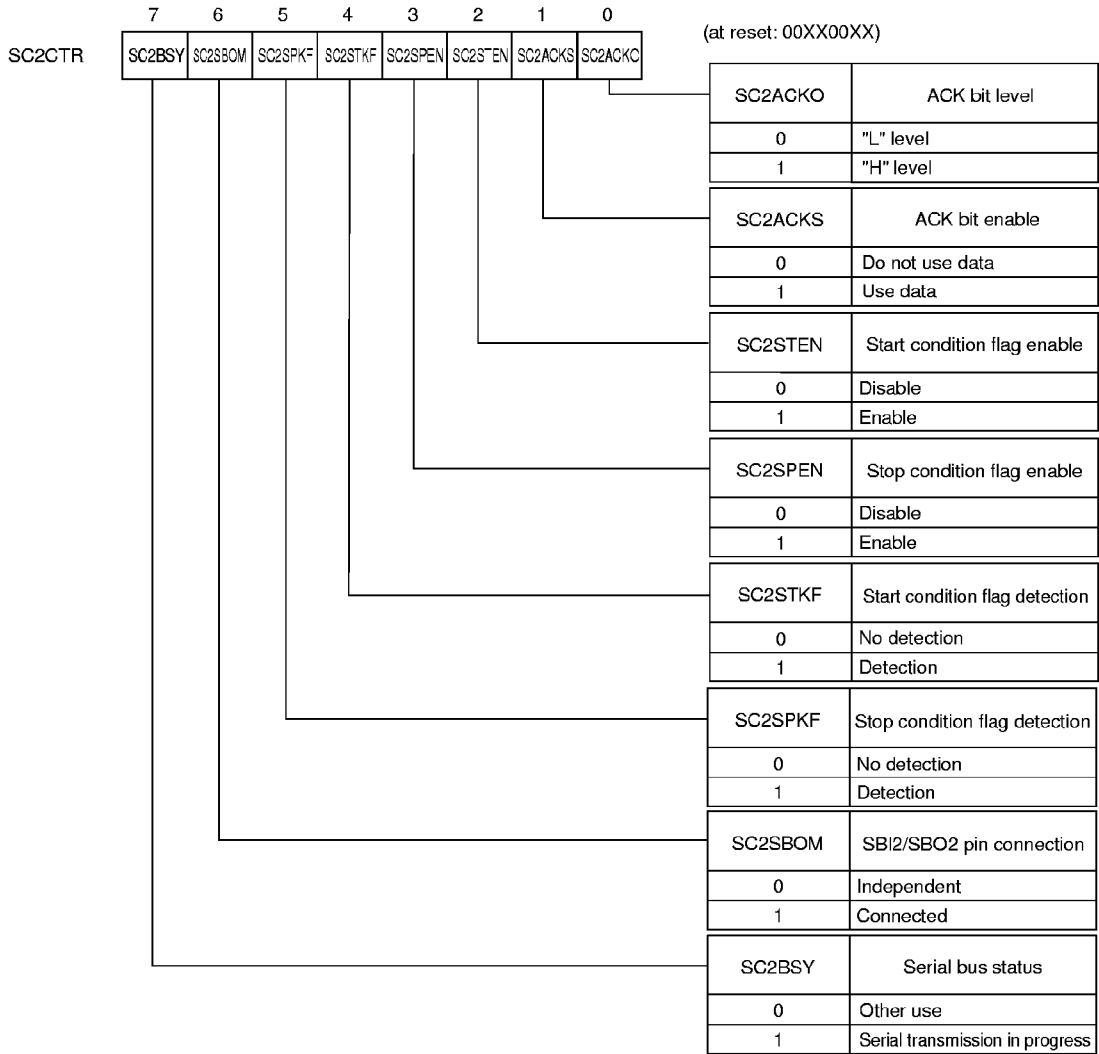


Figure 5-5-14 Serial Interface 2 Control Register (SC2CTR: X'03F5C', R/W)



Chapter 6

A/D Conversion  
Functions



## 6-1 Overview

The MN101C01D has an internal A/D converter with 10-bit resolution. A sample-and-hold circuit is contained on-chip and software can switch the analog input between channels 0~7 (AN0~AN7).

When the A/D converter is stopped, power consumption can be reduced by turning off the internal ladder resistors.

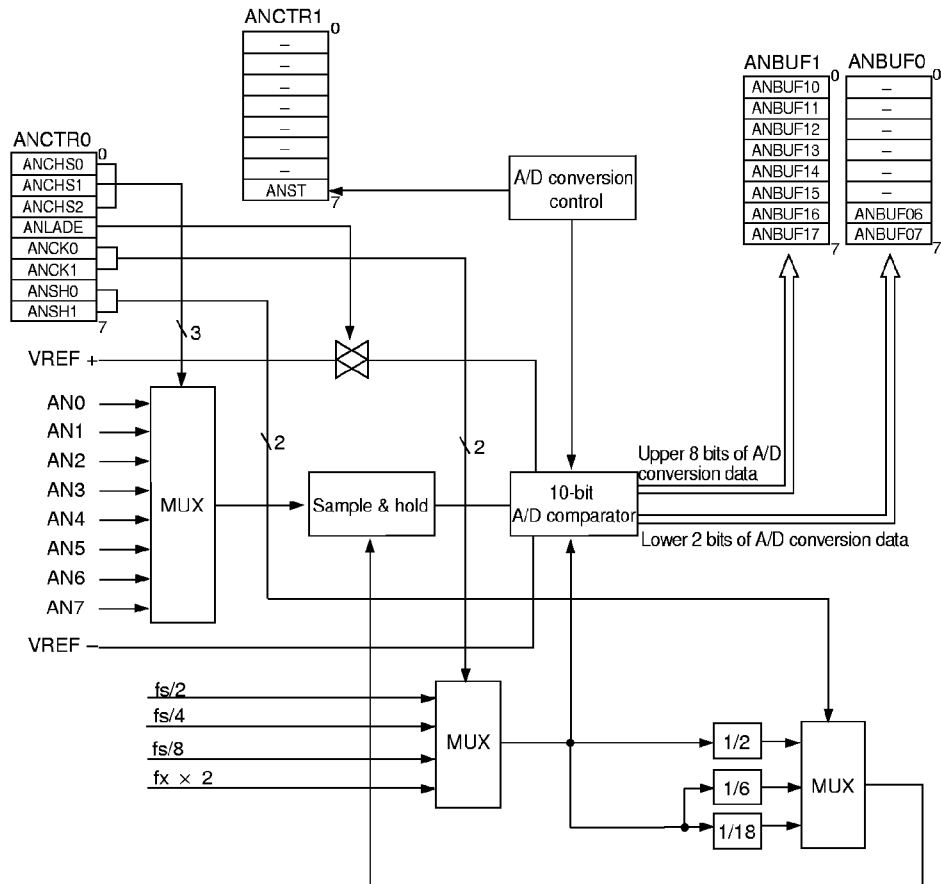


Figure 6-1-1 A/D Converter Block Diagram

## 6-2 A/D Conversion

The procedures for operating the A/D conversion circuit are listed below.

- (1) Set the ANCIIS2~ANCIIS0 flags of A/D control register 0 (ANCTR0) to specify one of pins AN7~AN0 (PA7~PA0) as the analog input.
- (2) Set the ANCK1 and ANCK0 flags of A/D control register 0 to select the A/D conversion clock. Make this setting such that the period of the conversion clock ( $T_{AD}$ ), which is based on the oscillator, is greater than 800ns.
- (3) With the ANSH1 and ANSH0 flags of A/D control register 0, set the sample-and-hold time. Select a value for the sample and hold time that is suitable for the analog input impedance.
- (4) Set the ANLADE flag of A/D control register 0 to "1" so that current flows through the ladder resistors and the A/D converter is on standby.  
Note: Steps 1~4 above may performed all at the same time.
- (5) Set the ANST flag of A/D control register 1 (ANCTR1) to "1" to start the A/D conversion.
- (6) After the sample-and-hold time set in step 3, the sampled A/D conversion data is sequentially compared to determine its value beginning with the MSB.
- (7) When the A/D conversion is complete, the ANST bit is cleared to "0" and conversion results are stored in A/D buffers (ANBUF0, 1). At the same time, an A/D complete interrupt request (ADIRQ) is generated.

*Start the A/D conversion after the current flowing through the ladder resistors stabilizes. The time constant calculated time from the ladder resistance (max. 80 k $\Omega$ ) and the external bypass capacitor connected between  $V_{ref+}$  and  $V_{ref-}$  should be used as the criteria for the wait time.*

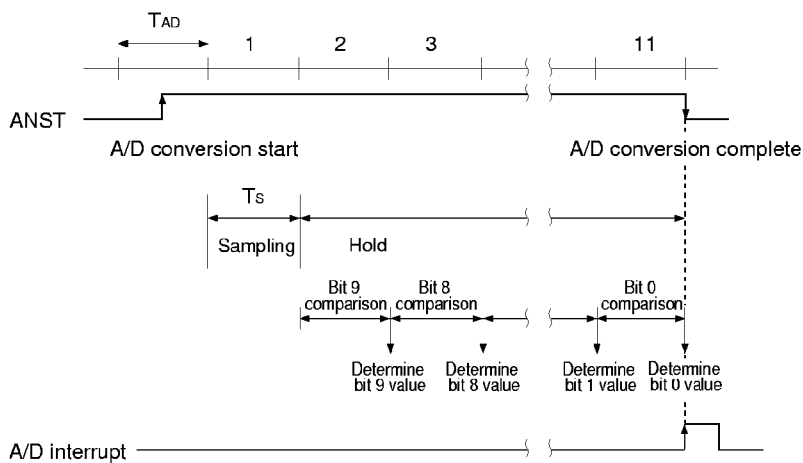
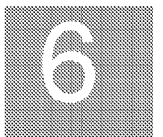


Figure 6-2-1 A/D Conversion Timing



## 6-3 A/D Converter Control Registers

### 6-3-1 Overview

Four registers control the A/D converter. See table 6-3-1.

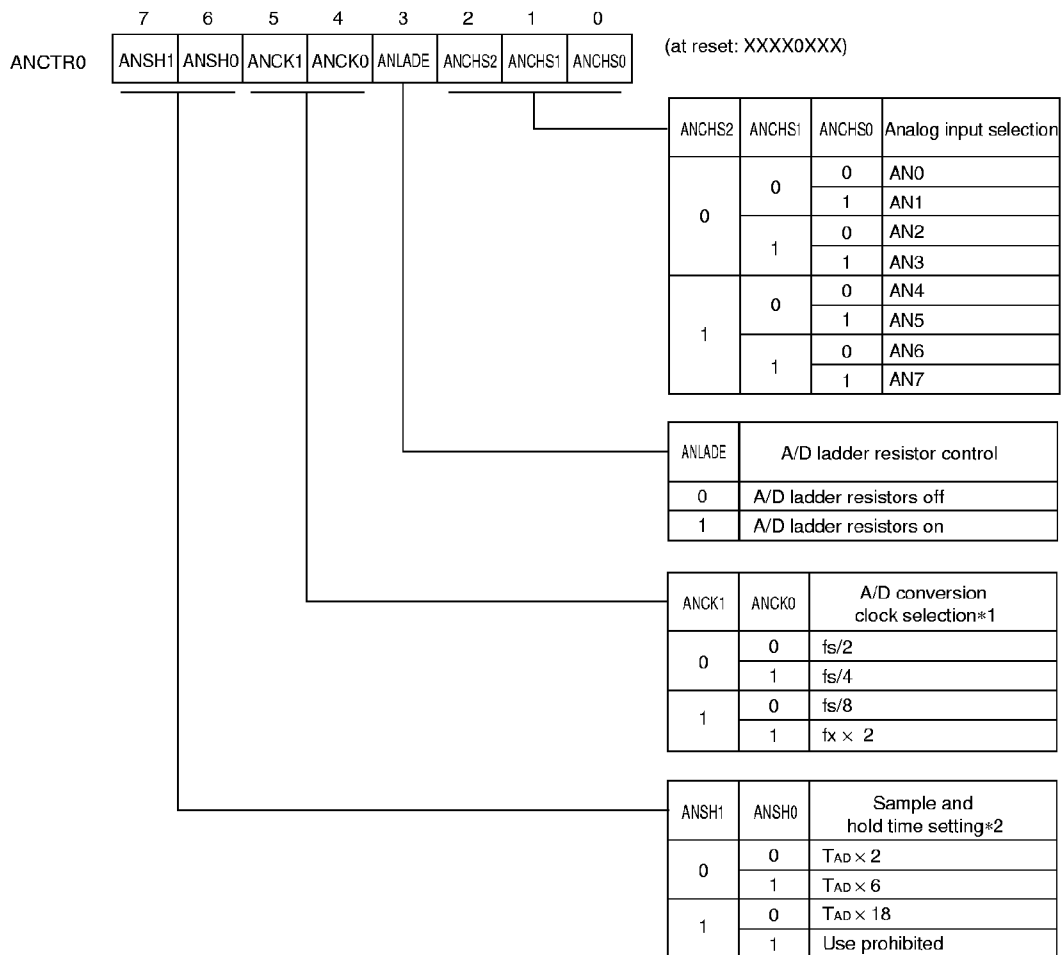
Table 6-3-1 A/D Converter Control Registers

| Name   | Address  | R/W | Function               |
|--------|----------|-----|------------------------|
| ANCTR0 | X'03F90' | R/W | A/D control register 0 |
| ANCTR1 | X'03F91' | R/W | A/D control register 1 |
| ANBUF0 | X'03F92' | R   | A/D buffer 0           |
| ANBUF1 | X'03F93' | R   | A/D buffer 1           |

### 6-3-2 A/D Control Register (ANCTR)

This readable and writable 8-bit register controls the operation of the A/D converter.

#### (1) A/D control register 0 (ANCTR0)



\*1: Specify that where the period of the A/D conversion clock is greater than 800ns.

\*2: Sample-and-hold time is determined by the analog input impedance.  $T_{AD}$  indicates the period of the A/D conversion clock.

Figure 6-3-1 A/D Control Register 0 (ANCTR0: X'03F90', R/W)



(2) A/D conversion control register 1 (ANCTR1)

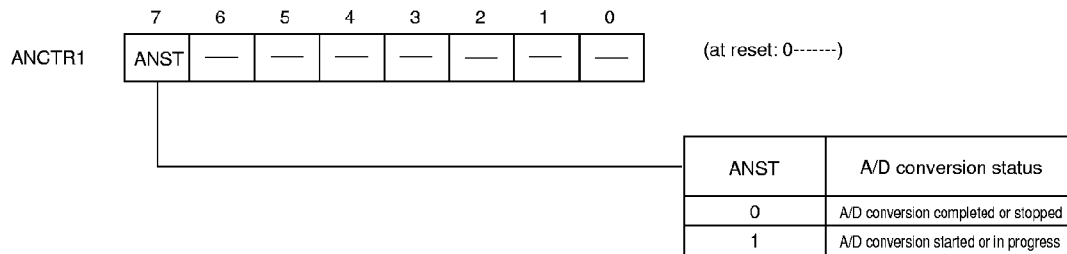


Figure 6-3-2 A/D Control Register 1 (ANCTR1: X'03F91', R/W)

### 6-3-3 A/D Buffers (ANBUF)

These read-only registers store the A/D conversion results.

#### (1) A/D buffer 0 (ANBUF0)

This register stores the lower 2 bits of the A/D conversion results.

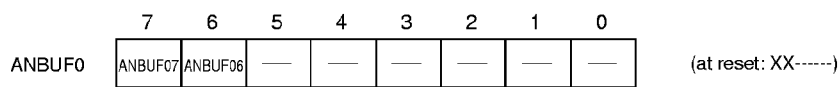


Figure 6-3-3 A/D Buffer 0 (ANBUF0: X'03F92', R)

#### (2) A/D buffer 1 (ANBUF1)

This register stores the upper 8 bits of the A/D conversion results.

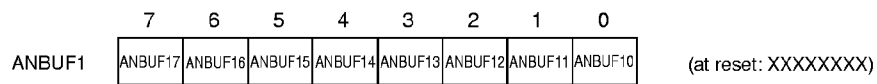


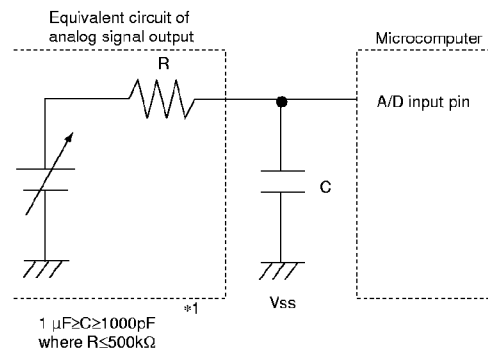
Figure 6-3-4 A/D Buffer 1 (ANBUF1: X'03F93', R)

### 6-3-4 Warning when Using the A/D Converter



The following items must be implemented to maintain the accuracy of the A/D converter:

1. Use a maximum input pin impedance,  $R$ , of  $500\text{k}\Omega^{*1}$  with an external capacitor,  $C$ , that is minimum  $1,000\text{pF}$  and maximum  $1\mu\text{F}^{*1}$ .
2. Take the RC time into consideration when setting the A/D conversion interval.
3. Changing the output level of the microcomputer or switching peripheral circuitry on or off when the A/D converter is in use may cause the analog input pin or current pin to fluctuate resulting in a loss of precision. During setup and evaluation, verify the waveform of the analog input pin.



\*1 These values are reference values.

Figure 6-3-5 Recommended Circuit When Using A/D Conversion

Chapter 7

AC Zero-Cross  
Circuit/Noise Filter



## 7-1 Overview

The P21/SENS pin is the input pin for the AC zero-cross detection circuit. The AC zero-cross detection circuit outputs a high level when the input is at an intermediate level, and a low level at all other times.

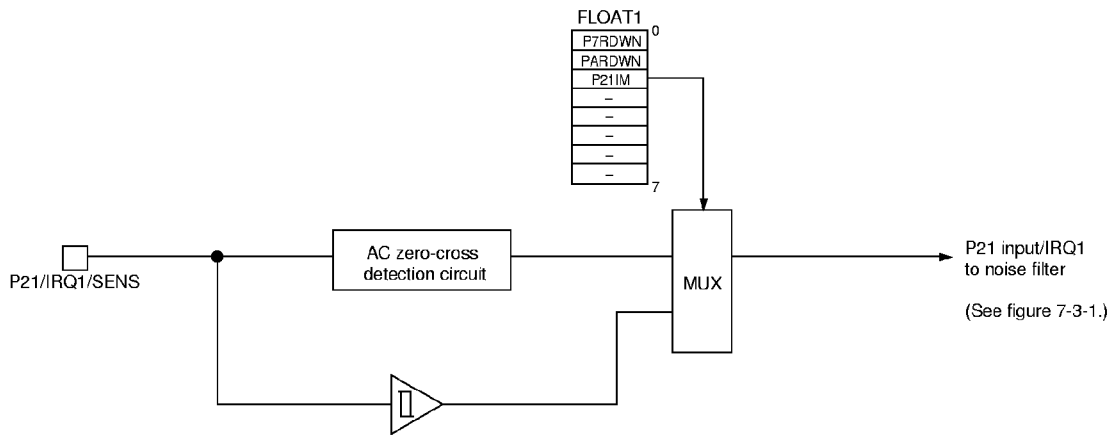


Figure 7-1-1 P21 Input Circuit Block Diagram

## 7-2 AC Zero-Cross Circuit Operation

### 7-2-1 Setup and Operation

Settings for zero-cross circuit operation are listed below.

- (1) Set the REDG1 flag of the IRQ1ICR register to select the valid edge for IRQ1.
- (2) Set the NF1EN and NF1CK2~1 flags of the NFCTR register to set the noise filter and its sampling clock.
- (3) With the P21IM flag of the FLOAT1 register, set the P21 pin to zero-cross detection.
- (4) An IRQ1 interrupt is generated when the waveform of the AC line voltage intersects  $1/2V_{DD}$ .

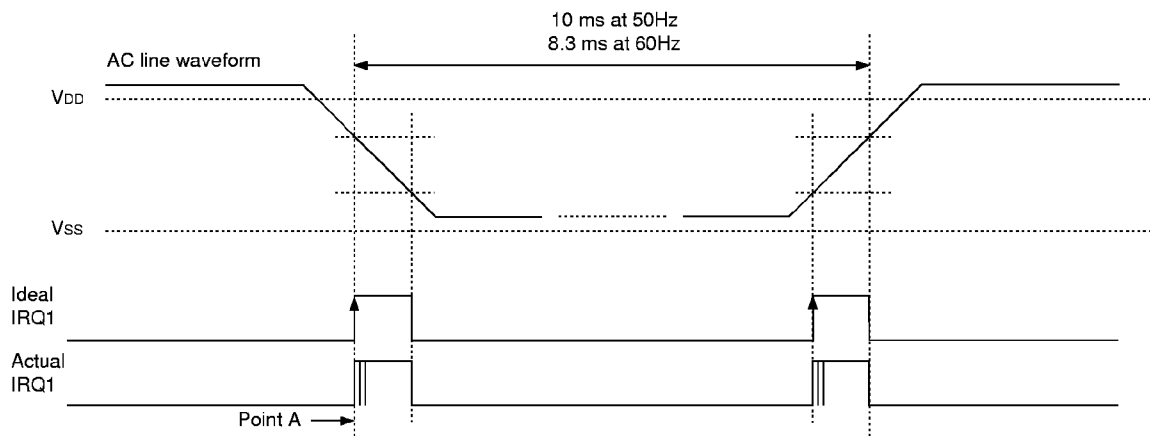
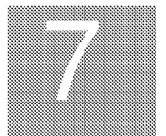


Figure 7-2-1 AC Line Waveform and IRQ Generation Timing

When the AC line waveform intersects  $1/2V_{DD}$ , actual IRQ interrupt requests will be generated multiple times. Therefore, the software must filter this signal before making any evaluations.

When noise filtering is selected for use, the amount of evaluation processing by the software will be reduced. However, if the OSC stops, a return from the backup mode will not be possible.



## 7-3 Noise Filter

### 7-3-1 Overview

External interrupt pins IRQ0 and IRQ1 contain noise filtering circuit. This circuitry can be used for remote control signal reception.

IRQ0: External interrupt 0

IRQ1: External interrupt 1

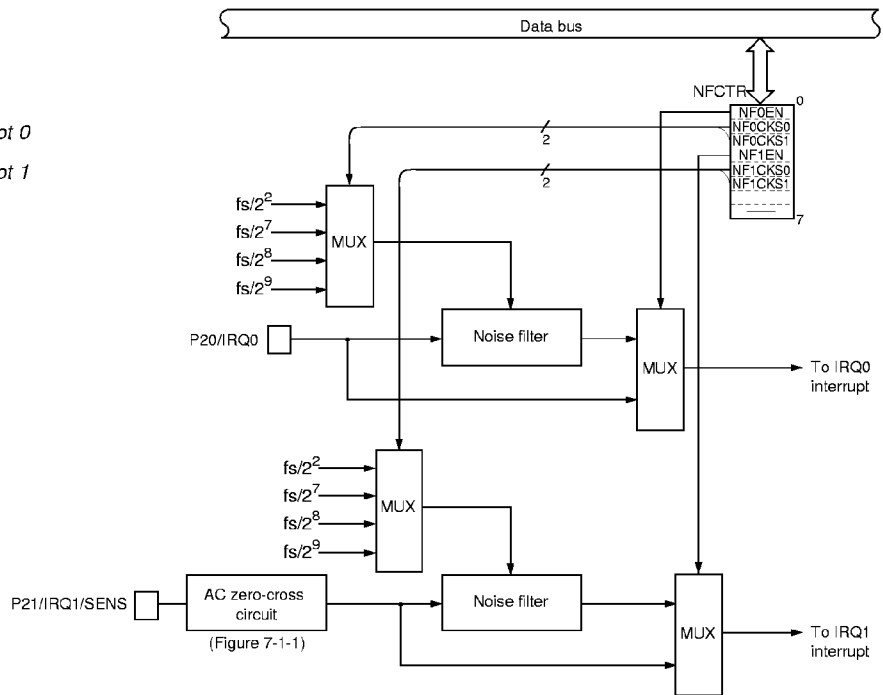


Figure 7-3-1 Noise Filtering Circuit Block Diagram

### 7-3-2 Example Input and Output Waveforms for Noise Filter

When the noise filter is used, the waveform input to the IRQ0 pin is sampled based on the clock specified by the NFOCKS0 and NFOCKS1 flags of the noise filter control register (NFCTR). The waveform input to the IRQ1 pin is also sampled based on the clock specified by the NFOCKS0 and NFOCKS1 flags. If the sampled level remains the same for 3 consecutive samples, it is sent the CPU; otherwise, the previous level is maintained.



*Noise filtering cannot be used in the STOP or HALT modes.*

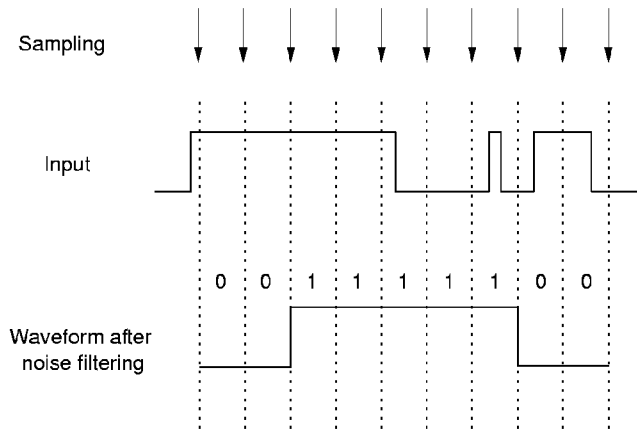


Figure 7-3-2 Noise Filter Input and Output Waveform Example



## 7-4 AC Zero-Cross Control Register

### 7-4-1 Overview

Three registers control the AC zero-cross circuit.

Table 7-4-1 AC Zero-Cross Control Register

| Name    | Address  | R/W | Function                              |
|---------|----------|-----|---------------------------------------|
| IRQ0ICR | X'03FE2' | R/W | External interrupt control register 0 |
| IRQ1ICR | X'03FE3' | R/W | External interrupt control register 1 |
| FLOAT1  | X'03F4B' | R/W | Pin control register 1                |
| NFCTR   | X'03F8A' | R/W | Noise filter control register         |

[REF 2-4-3 "Interrupt Control Registers ■ External Interrupt Control Registers"]

[REF 3-2-2 "I/O Port Control Registers ■ Pin Control Registers"]

### 7-4-2 Noise Filter Control Register (NFCTR)

This 6-bit readable and writable register controls the noise filter.

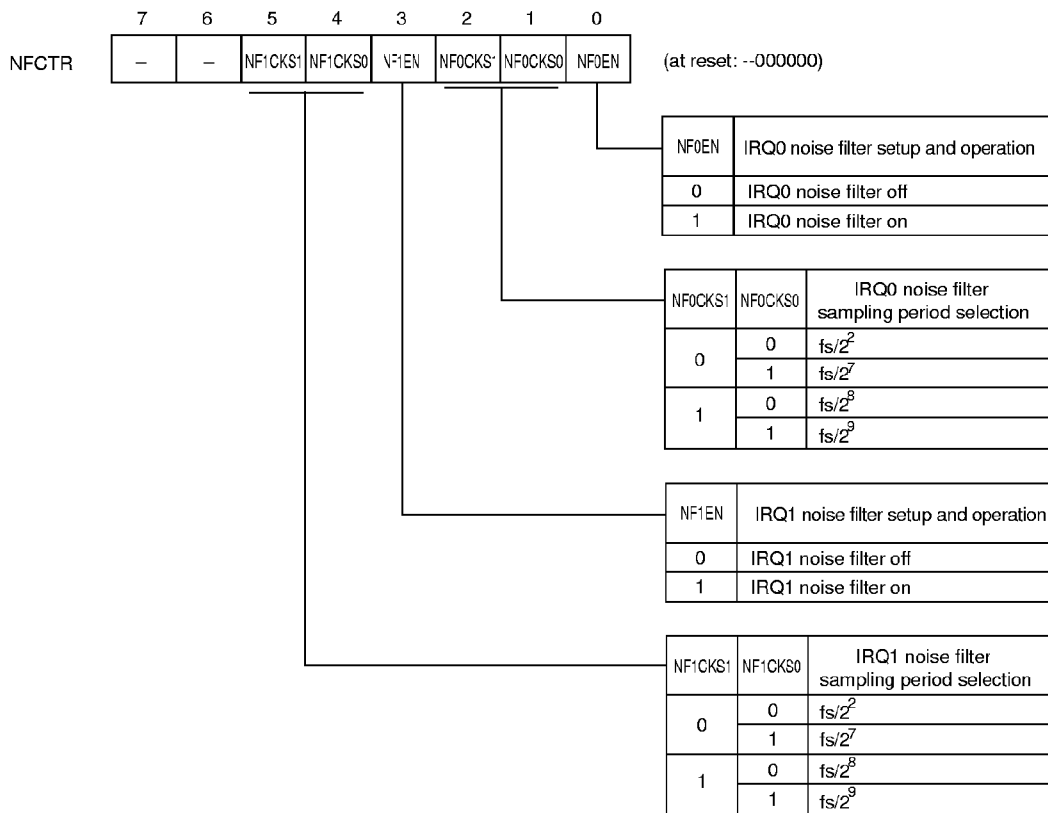


Figure 7-4-1 Noise Filter Control Register (NFCTR: X'03F8A', R/W)



Chapter 8

Automatic Data  
Transfer Control  
Function



## 8-1 Overview

The MN101C01D has the automatic data transfer control (ATC) function that can transfer data by hardware between the memory space and the internal special function register space.

Any of the interrupts listed in table 8-1-1 can be selected as the source to activate the ATC. Each time the interrupt once occurs, an 8-bit or 16-bit address is transferred. The number of transfers set in the transfer word count register has been reached, the automatic data transfer control interrupt is occurred.

For multiple (16-bit) transfers, disable interrupts from the interrupt control register of the selected ATC activation source (xxxIF=0).

The one-word transfer mode is used to transfer the 16-bit capture register, 10-bit A/D data, etc. The one-word transfer begins at an even address and consecutively transfers data from two consecutive addresses.

Table 8-1-1 Summary of the Automatic Data Transfer Control Function

|                    |   |
|--------------------|---|
| Directions         | Memory→Special Function Register      Special Function Register→Memory<br>(Memory→Memory transfers are not allowed)   |
| Formats            | 1 byte (8 bits) or 1 word (16 bits)   |
| Activation sources | A/D conversion complete interrupt<br>Serial 0 transfer complete interrupt<br>Serial 1 transfer complete interrupt<br>Serial 2 transfer complete interrupt<br>Timer 2 compare-match interrupt<br>Timer 4 compare-match interrupt<br>External interrupt IRQ0<br>External interrupt IRQ1 |

## 8-2 Automatic Data Transfer Control Operation

### 8-2-1 Overview

Automatic data transfer control (ATC) is specified by the automatic data control register (ATMD).

The ATC can transfer from 1 to 256 bytes, as specified in the ATCNT register. After the specified transfer is complete, the automatic data transfer interrupt (ATCIRQ) is generated.

The target address pointer (ATTAP) for the ATC can be specified to increment or hold constant.

### 8-2-2 Automatic Data Transfer

The transfer procedures are listed below.

(1) Disable the automatic data transfer

Set bit 6 (ATEN) of the ATMD register to "0" to disable the transfer function.

(At reset: 0)

(2) Select internal ATC

Set bit 7 (ATEXT) of the ATMD register to "0".

(At reset: 0)

(3) Select ATC activation source

Set bits 2~0 (ATBG2~0) of the ATMD register to select the interrupt that will activate the transfer.

000: A/D conversion complete interrupt

001: Serial 0 transfer complete interrupt

010: Serial 1 transfer complete interrupt

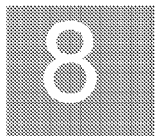
011: Serial 2 transfer complete interrupt

100: Timer 2 compare-match interrupt

101: Timer 4 compare-match interrupt

110: External interrupt IRQ0

111: External interrupt IRQ1



(4) Select transfer address mode

Select the transfer address mode with bit 3 (ATINC) of the ATMD register.

- 0: Fixed ATTAP address
- 1: Incrementing ATTAP address

(5) Select transfer unit

Select the transfer unit with bit 5 (ATWID) of the ATMD register.

- 0: Byte (8-bit) transfer
- 1: Word (16-bit) transfer

(6) Select transfer direction

Select the transfer direction with bit 4 (ATDIR) of the ATMD register.

- 0: The transfer target address pointer (for memory) is specified as the source pointer.
- 1: The transfer target address pointer (for memory) is specified as the destination pointer.

(7) Set transfer word count

Set the transfer word count in the ATCNT register.

The order of settings in steps (2)~(7) can be changed.

(8) Enable data transfer

Set bit 6 (ATEN) of the ATMD register to "1" to enable the transfer function.

(9) Transfer complete

When all transfers are complete, ATEN will be cleared to "0" and an ATCIRQ interrupt generated.

### 8-2-3 Transfer Timing

The load cycle and store cycle execution times are determined by the memory space being accessed and the number of wait cycles set in the MEMCTR register.

The number of execution cycles for access of each type of memory are listed below.

- Special function register space: 3 cycles (when no wait cycles are set)
- Internal ROM/RAM: 2 cycles
- External ROM/RAM: 2 cycles (when no wait cycles are set)

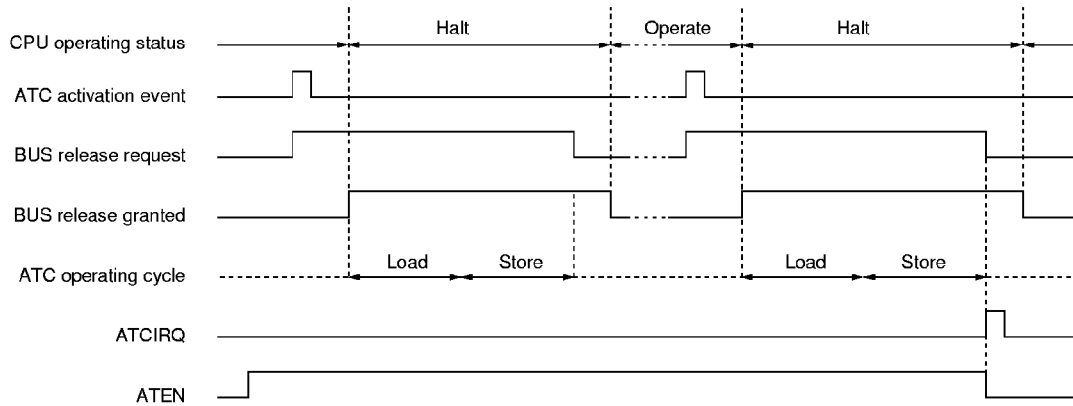


Figure 8-2-1 ATC Operation Timing Chart



## 8-3 Automatic Data Transfer Control Registers

### 8-3-1 Overview

Five registers to control the automatic data transfer control function (ATC). See table 8-3-1.

Table 8-3-1 Automatic Data Transfer Function Control Registers

| Name   | Address  | R/W | Function  |
|--------|----------|-----|---|
| ATMD   | X'03FA0' | R/W | Automatic data transfer control register            |
| ATCNT  | X'03FA1' | R/W | Transfer word counter                               |
| ATTAPL | X'03FA2' | R/W | Data transfer target address pointer (lower 8 bits) |
| ATTAPH | X'03FA3' | R/W | Data transfer target address pointer (upper 8 bits) |
| ATIAP  | X'03FA4' | R/W | Data transfer internal address pointer              |

The automatic data transfer control register (ATMD) controls the operation of the ATC (activation source selection, transfer address mode selection, transfer direction/unit selection, and transfer enable status).

The data transfer target address pointer (ATTAPL, ATTAPH) points to a memory space.

The data transfer internal address pointer (ATIAP) points to an internal special function register space.

### 8-3-2 Automatic Data Transfer Control Register (ATMD)

This readable and writable 8-bit register controls the automatic data transfer control function.

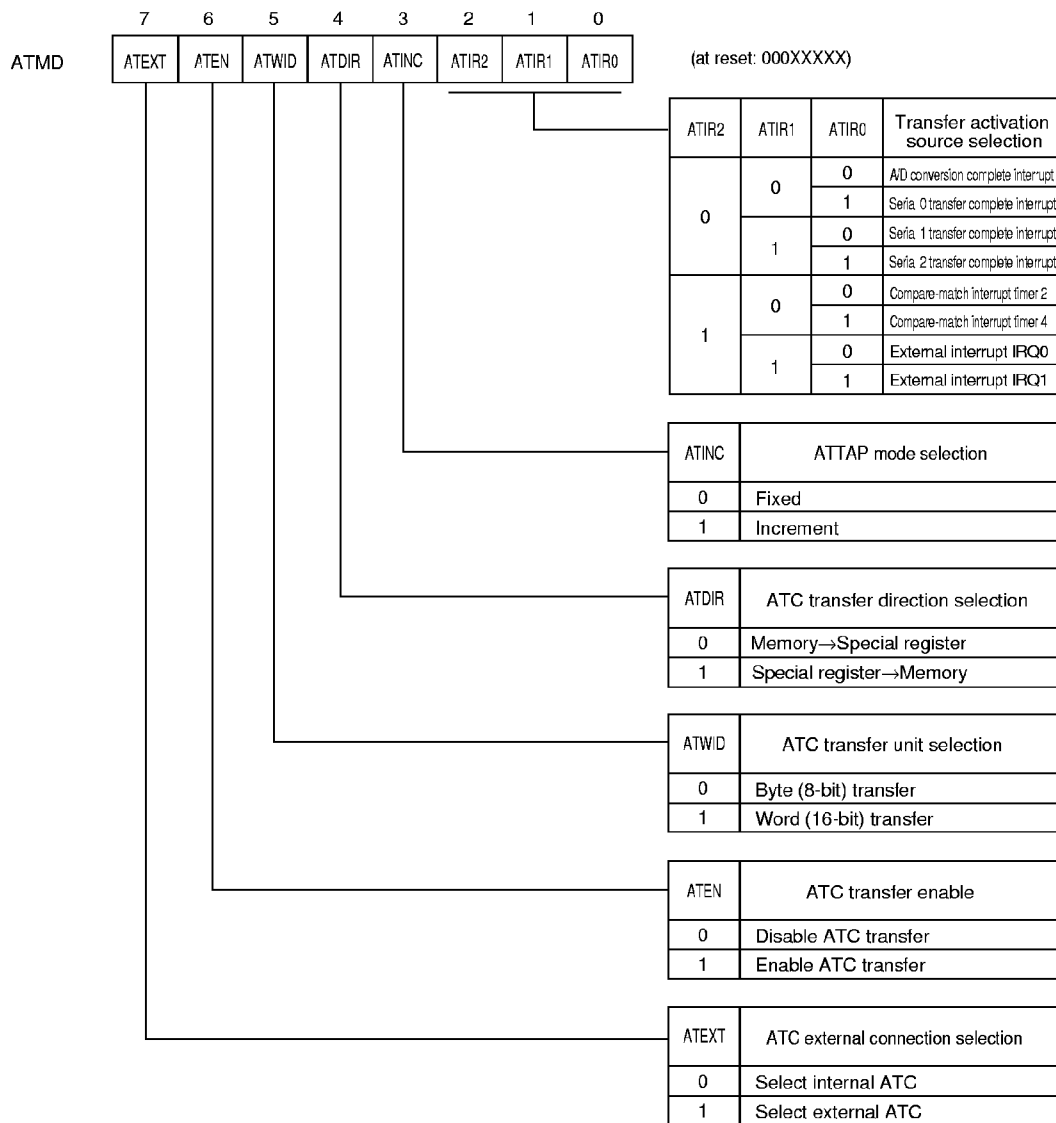


Figure 8-3-1 Automatic Data Transfer Control Register (ATMD: X'03FA0', R/W)

### 8-3-3 Transfer Word Counter (ATCNT)

This 8-bit readable and writable register sets the total number of bytes for the data transfer. The contents of ATCNT are decremented (-1) at each 1 byte transfer. When X'00' is reached, an automatic data transfer interrupt (ATCIRQ) is generated, the ATC transfer enabled flag (ATEN) is cleared to "0", and the transfer is complete.

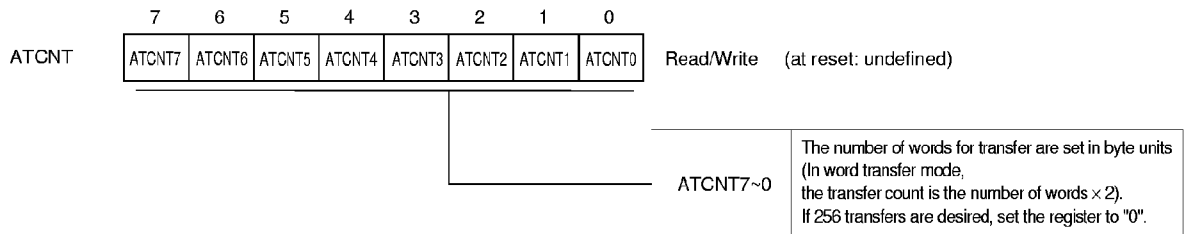


Figure 8-3-2 Transfer Word Counter (ATCNT: X'03FA1', R/W)

### 8-3-4 Transfer Address Pointers

The transfer address pointers are a 16-bit and an 8-bit readable and writable register.

(1) Data transfer target address pointer (ATTAPH, ATTAPL)

This pointer specifies the RAM address of the transfer target.

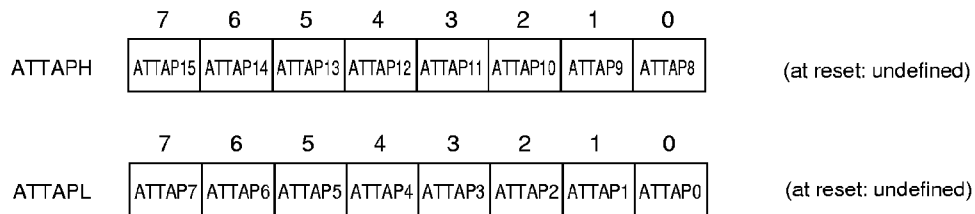


Figure 8-3-3 Data Transfer Target Address Pointer  
(ATTAPH: X'03FA3', R/W; ATTAPL: X'03FA2', R/W)

(2) Data transfer internal address pointer (ATIAP)

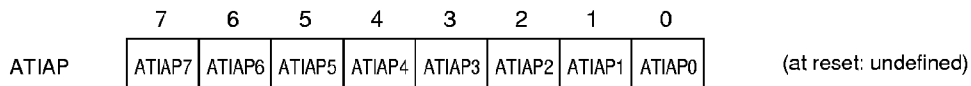


Figure 8-3-4 Data Transfer Internal Address Pointer (ATIAP: X'03FA4', R/W)



Appendices



Appendices

MN101C00 SERIES INSTRUCTION SET

| Group                         | Mnemonic            | Operation               | Affected Flag    |    |    |    | Code Size | Cycle | Repeat | Machine Code              |                          |                               |   |   |   |   |   |   |    |    | Notes | Page |    |
|-------------------------------|---------------------|-------------------------|------------------|----|----|----|-----------|-------|--------|---------------------------|--------------------------|-------------------------------|---|---|---|---|---|---|----|----|-------|------|----|
|                               |                     |                         | VF               | NF | CF | ZF |           |       |        | 1                         | 2                        | 3                             | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |       |      |    |
| <b>Data move instructions</b> |                     |                         |                  |    |    |    |           |       |        |                           |                          |                               |   |   |   |   |   |   |    |    |       |      |    |
| MOV                           | MOV Dn,Dm           | Dn→Dm                   | -                | -  | -  | -  | 2         | 1     |        | 1010 DnDm                 |                          |                               |   |   |   |   |   |   |    |    |       | 25   |    |
|                               | MOV imm8,Dm         | imm8→Dm                 | -                | -  | -  | -  | 4         | 2     |        | 1010DmDm <#8. ...>        |                          |                               |   |   |   |   |   |   |    |    |       | 25   |    |
|                               | MOV Dn,PSW          | Dn→PSW                  | ●                | ●  | ●  | ●  | 3         | 3     | 0010   | 1001                      | 01Dn                     |                               |   |   |   |   |   |   |    |    | 26    |      |    |
|                               | MOV PSW,Dm          | PSW→Dm                  | -                | -  | -  | -  | 3         | 2     | 0010   | 0001                      | 01Dm                     |                               |   |   |   |   |   |   |    |    | 26    |      |    |
|                               | MOV (An),Dm         | mem8(An)→Dm             | -                | -  | -  | -  | 2         | 2     |        | 0100 1ADm                 |                          |                               |   |   |   |   |   |   |    |    |       | 27   |    |
|                               | MOV (d8,An),Dm      | mem8(d8+An)→Dm          | -                | -  | -  | -  | 4         | 2     |        | 0110 1ADm <d8. ...>       |                          |                               |   |   |   |   |   |   |    |    | *1    | 27   |    |
|                               | MOV (d16,An),Dm     | mem8(d16+An)→Dm         | -                | -  | -  | -  | 7         | 4     | 0010   | 0110                      | 1ADm                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 28   |    |
|                               | MOV (d4,SP),Dm      | mem8(d4+SP)→Dm          | -                | -  | -  | -  | 3         | 2     |        | 0110 01Dm <d4>            |                          |                               |   |   |   |   |   |   |    |    | *2    | 28   |    |
|                               | MOV (d8,SP),Dm      | mem8(d8+SP)→Dm          | -                | -  | -  | -  | 5         | 3     | 0010   | 0110                      | 01Dm                     | <d8. ...>                     |   |   |   |   |   |   |    |    | *3    | 29   |    |
|                               | MOV (d16,SP),Dm     | mem8(d16+SP)→Dm         | -                | -  | -  | -  | 7         | 4     | 0010   | 0110                      | 00Dm                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 29   |    |
|                               | MOV (io8),Dm        | mem8(IOTOP+io8)→Dm      | -                | -  | -  | -  | 4         | 2     |        | 0110 00Dm <io8. ...>      |                          |                               |   |   |   |   |   |   |    |    |       | 30   |    |
|                               | MOV (abs8),Dm       | mem8(abs8)→Dm           | -                | -  | -  | -  | 4         | 2     |        | 0100 01Dm <abs 8.>        |                          |                               |   |   |   |   |   |   |    |    |       | 30   |    |
|                               | MOV (abs12),Dm      | mem8(abs12)→Dm          | -                | -  | -  | -  | 5         | 2     |        | 0100 00Dm <abs 12.. ...>  |                          |                               |   |   |   |   |   |   |    |    |       | 31   |    |
|                               | MOV (abs16),Dm      | mem8(abs16)→Dm          | -                | -  | -  | -  | 7         | 4     | 0010   | 1100                      | 00Dm                     | <abs 16.. .... ...>           |   |   |   |   |   |   |    |    |       | 31   |    |
|                               | MOV Dn,(Am)         | Dn→mem8(Am)             | -                | -  | -  | -  | 2         | 2     |        | 0101 1aDn                 |                          |                               |   |   |   |   |   |   |    |    |       | 32   |    |
|                               | MOV Dn,(d8,Am)      | Dn→mem8(d8+Am)          | -                | -  | -  | -  | 4         | 2     |        | 0111 1aDn <d8. ...>       |                          |                               |   |   |   |   |   |   |    |    | *1    | 32   |    |
|                               | MOV Dn,(d16,Am)     | Dn→mem8(d16+Am)         | -                | -  | -  | -  | 7         | 4     | 0010   | 0111                      | 1aDn                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 33   |    |
|                               | MOV Dn,(d4,SP,Am)   | Dn→mem8(d4+SP,Am)       | -                | -  | -  | -  | 3         | 2     |        | 0111 01Dn <d4>            |                          |                               |   |   |   |   |   |   |    |    | *2    | 33   |    |
|                               | MOV Dn,(d8,SP,Am)   | Dn→mem8(d8+SP,Am)       | -                | -  | -  | -  | 5         | 3     | 0010   | 0111                      | 01Dn                     | <d8. ...>                     |   |   |   |   |   |   |    |    | *3    | 34   |    |
|                               | MOV Dn,(d16,SP,Am)  | Dn→mem8(d16+SP,Am)      | -                | -  | -  | -  | 7         | 4     | 0010   | 0111                      | 00Dn                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 34   |    |
|                               | MOV Dn,(io8,Am)     | Dn→mem8(IOTOP+io8,Am)   | -                | -  | -  | -  | 4         | 2     |        | 0111 00Dn <io8. ...>      |                          |                               |   |   |   |   |   |   |    |    |       | 35   |    |
|                               | MOV Dn,(abs8,Am)    | Dn→mem8(abs8,Am)        | -                | -  | -  | -  | 4         | 2     |        | 0101 01Dn <abs 8.>        |                          |                               |   |   |   |   |   |   |    |    |       | 35   |    |
|                               | MOV Dn,(abs12,Am)   | Dn→mem8(abs12,Am)       | -                | -  | -  | -  | 5         | 2     |        | 0101 00Dn <abs 12.. ...>  |                          |                               |   |   |   |   |   |   |    |    |       | 36   |    |
|                               | MOV Dn,(abs16,Am)   | Dn→mem8(abs16,Am)       | -                | -  | -  | -  | 7         | 4     | 0010   | 1101                      | 00Dn                     | <abs 16.. .... ...>           |   |   |   |   |   |   |    |    |       | 36   |    |
|                               | MOV imm8,(io8,Am)   | imm8→mem8(IOTOP+io8,Am) | -                | -  | -  | -  | 6         | 3     | 0000   | 0010                      | <io8. ...> <#8. ...>     |                               |   |   |   |   |   |   |    |    | 37    |      |    |
|                               | MOV imm8,(abs8,Am)  | imm8→mem8(abs8,Am)      | -                | -  | -  | -  | 6         | 3     | 0001   | 0100                      | <abs 8.> <#8. ...>       |                               |   |   |   |   |   |   |    |    | 37    |      |    |
|                               | MOV imm8,(abs12,Am) | imm8→mem8(abs12,Am)     | -                | -  | -  | -  | 7         | 3     | 0001   | 0101                      | <abs 12.. ...> <#8. ...> |                               |   |   |   |   |   |   |    |    | 38    |      |    |
|                               | MOV imm8,(abs16,Am) | imm8→mem8(abs16,Am)     | -                | -  | -  | -  | 9         | 5     | 0011   | 1101                      | 1001                     | <abs 16.. .... ...> <#8. ...> |   |   |   |   |   |   |    |    |       | 38   |    |
|                               | MOV Dn,(HA,Am)      | Dn→mem8(HA,Am)          | -                | -  | -  | -  | 2         | 2     |        | 1101 00Dn                 |                          |                               |   |   |   |   |   |   |    |    |       | 39   |    |
|                               | MOVW                | MOVW (An),DWm           | mem16(An)→DWm    | -  | -  | -  | -         | 2     | 3      |                           | 1110 00Ad                |                               |   |   |   |   |   |   |    |    |       |      | 40 |
|                               |                     | MOVW (An),Am            | mem16(An)→Am     | -  | -  | -  | -         | 3     | 4      | 0010                      | 1110                     | 10Aa                          |   |   |   |   |   |   |    |    | *4    | 40   |    |
|                               |                     | MOVW (d4,SP),DWm        | mem16(d4+SP)→DWm | -  | -  | -  | -         | 3     | 3      |                           | 1110 011d <d4>           |                               |   |   |   |   |   |   |    |    |       | *2   | 41 |
|                               |                     | MOVW (d4,SP),Am         | mem16(d4+SP)→Am  | -  | -  | -  | -         | 3     | 3      |                           | 1110 010a <d4>           |                               |   |   |   |   |   |   |    |    |       | *2   | 41 |
| MOVW (d8,SP),DWm              |                     | mem16(d8+SP)→DWm        | -                | -  | -  | -  | 5         | 4     | 0010   | 1110                      | 011d                     | <d8. ...>                     |   |   |   |   |   |   |    |    | *3    | 42   |    |
| MOVW (d8,SP),Am               |                     | mem16(d8+SP)→Am         | -                | -  | -  | -  | 5         | 4     | 0010   | 1110                      | 010a                     | <d8. ...>                     |   |   |   |   |   |   |    |    | *3    | 42   |    |
| MOVW (d16,SP),DWm             |                     | mem16(d16+SP)→DWm       | -                | -  | -  | -  | 7         | 5     | 0010   | 1110                      | 001d                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 43   |    |
| MOVW (d16,SP),Am              |                     | mem16(d16+SP)→Am        | -                | -  | -  | -  | 7         | 5     | 0010   | 1110                      | 000a                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 43   |    |
| MOVW (abs8),DWm               |                     | mem16(abs8)→DWm         | -                | -  | -  | -  | 4         | 3     |        | 1100 011d <abs 8.>        |                          |                               |   |   |   |   |   |   |    |    |       | 44   |    |
| MOVW (abs8),Am                |                     | mem16(abs8)→Am          | -                | -  | -  | -  | 4         | 3     |        | 1100 010a <abs 8.>        |                          |                               |   |   |   |   |   |   |    |    |       | 44   |    |
| MOVW (abs16),DWm              |                     | mem16(abs16)→DWm        | -                | -  | -  | -  | 7         | 5     | 0010   | 1100                      | 011d                     | <abs 16.. .... ...>           |   |   |   |   |   |   |    |    |       | 45   |    |
| MOVW (abs16),Am               |                     | mem16(abs16)→Am         | -                | -  | -  | -  | 7         | 5     | 0010   | 1100                      | 010a                     | <abs 16.. .... ...>           |   |   |   |   |   |   |    |    |       | 45   |    |
| MOVW DWn,(Am)                 |                     | DWn→mem16(Am)           | -                | -  | -  | -  | 2         | 3     |        | 1111 00aD                 |                          |                               |   |   |   |   |   |   |    |    |       | 46   |    |
| MOVW An,(Am)                  |                     | An→mem16(Am)            | -                | -  | -  | -  | 3         | 4     | 0010   | 1111                      | 10aA                     |                               |   |   |   |   |   |   |    | *4 | 46    |      |    |
| MOVW DWn,(d4,SP,Am)           |                     | DWn→mem16(d4+SP,Am)     | -                | -  | -  | -  | 3         | 3     |        | 1111 011D <d4>            |                          |                               |   |   |   |   |   |   |    |    | *2    | 47   |    |
| MOVW An,(d4,SP,Am)            |                     | An→mem16(d4+SP,Am)      | -                | -  | -  | -  | 3         | 3     |        | 1111 010A <d4>            |                          |                               |   |   |   |   |   |   |    |    | *2    | 47   |    |
| MOVW DWn,(d8,SP,Am)           |                     | DWn→mem16(d8+SP,Am)     | -                | -  | -  | -  | 5         | 4     | 0010   | 1111                      | 011D                     | <d8. ...>                     |   |   |   |   |   |   |    |    | *3    | 48   |    |
| MOVW An,(d8,SP,Am)            |                     | An→mem16(d8+SP,Am)      | -                | -  | -  | -  | 5         | 4     | 0010   | 1111                      | 010A                     | <d8. ...>                     |   |   |   |   |   |   |    |    | *3    | 48   |    |
| MOVW DWn,(d16,SP,Am)          |                     | DWn→mem16(d16+SP,Am)    | -                | -  | -  | -  | 7         | 5     | 0010   | 1111                      | 001D                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 49   |    |
| MOVW An,(d16,SP,Am)           |                     | An→mem16(d16+SP,Am)     | -                | -  | -  | -  | 7         | 5     | 0010   | 1111                      | 000A                     | <d16. .... ...>               |   |   |   |   |   |   |    |    |       | 49   |    |
| MOVW DWn,(abs8,Am)            |                     | DWn→mem16(abs8,Am)      | -                | -  | -  | -  | 4         | 3     |        | 1101 011D <abs 8.>        |                          |                               |   |   |   |   |   |   |    |    |       | 50   |    |
| MOVW An,(abs8,Am)             |                     | An→mem16(abs8,Am)       | -                | -  | -  | -  | 4         | 3     |        | 1101 010A <abs 8.>        |                          |                               |   |   |   |   |   |   |    |    |       | 50   |    |
| MOVW DWn,(abs16,Am)           |                     | DWn→mem16(abs16,Am)     | -                | -  | -  | -  | 7         | 5     | 0010   | 1101                      | 011D                     | <abs 16.. .... ...>           |   |   |   |   |   |   |    |    |       | 51   |    |
| MOVW An,(abs16,Am)            |                     | An→mem16(abs16,Am)      | -                | -  | -  | -  | 7         | 5     | 0010   | 1101                      | 010A                     | <abs 16.. .... ...>           |   |   |   |   |   |   |    |    |       | 51   |    |
| MOVW DWn,(HA,Am)              |                     | DWn→mem16(HA,Am)        | -                | -  | -  | -  | 2         | 3     |        | 1001 010D                 |                          |                               |   |   |   |   |   |   |    |    |       | 52   |    |
| MOVW An,(HA,Am)               |                     | An→mem16(HA,Am)         | -                | -  | -  | -  | 2         | 3     |        | 1001 011A                 |                          |                               |   |   |   |   |   |   |    |    |       | 52   |    |
| MCVW imm8,DWm                 |                     | sign(imm8)→DWm          | -                | -  | -  | -  | 4         | 2     | 0000   | 110d                      | <#8. ...>                |                               |   |   |   |   |   |   |    | *5 | 53    |      |    |
| MCVW imm8,Am                  |                     | zero(imm8)→Am           | -                | -  | -  | -  | 4         | 2     | 0000   | 111a                      | <#8. ...>                |                               |   |   |   |   |   |   |    | *6 | 53    |      |    |
| MCVW imm16,DWm                |                     | imm16→DWm               | -                | -  | -  | -  | 6         | 3     |        | 1100 111d <#16. .... ...> |                          |                               |   |   |   |   |   |   |    |    |       | 54   |    |

Note: "Page" refers to the corresponding page in the Instruction Manual.

- \*1 d8 sign extended
- \*2 d4 zero extended
- \*3 d8 zero extended
- \*4 A=An, a=Am
- \*5 #8 sign extended
- \*6 #8 zero extended

MN101C00 SERIES INSTRUCTION SET

| Group | Mnemonic      | Operation            | Affected Flag |    |    |    | Code Size | Cycle | Repeat | Machine Code |      |      |     |     |     |   |   |   |    |    | Notes | Page |  |    |    |
|-------|---------------|----------------------|---------------|----|----|----|-----------|-------|--------|--------------|------|------|-----|-----|-----|---|---|---|----|----|-------|------|--|----|----|
|       |               |                      | VF            | NF | CF | ZF |           |       |        | 1            | 2    | 3    | 4   | 5   | 6   | 7 | 8 | 9 | 10 | 11 |       |      |  |    |    |
|       | MOVW imm16,Am | imm16→Am             | -             | -  | -  | -  | 6         | 3     |        | 1101         | 111a | <#16 | ... | ... | ... |   |   |   |    |    |       |      |  | 54 |    |
|       | MOVW SP,Am    | SP→Am                | -             | -  | -  | -  | 3         | 3     |        | 0010         | 0000 | 100a |     |     |     |   |   |   |    |    |       |      |  |    | 55 |
|       | MOVW An,SP    | An→SP                | -             | -  | -  | -  | 3         | 3     |        | 0010         | 0000 | 101A |     |     |     |   |   |   |    |    |       |      |  |    | 55 |
|       | MOVW DWn,DWm  | DWn→DWm              | -             | -  | -  | -  | 3         | 3     |        | 0010         | 1000 | 00Dd |     |     |     |   |   |   |    |    |       |      |  | *1 | 56 |
|       | MOVW DWn,Am   | DWn→Am               | -             | -  | -  | -  | 3         | 3     |        | 0010         | 0100 | 11Da |     |     |     |   |   |   |    |    |       |      |  |    | 56 |
|       | MOVW An,DWm   | An→DWm               | -             | -  | -  | -  | 3         | 3     |        | 0010         | 1100 | 11Ad |     |     |     |   |   |   |    |    |       |      |  |    | 57 |
|       | MOVW An,Am    | An→Am                | -             | -  | -  | -  | 3         | 3     |        | 0010         | 0000 | 00Aa |     |     |     |   |   |   |    |    |       |      |  | *2 | 57 |
| PUSH  | PUSH Dn       | SP-1→SP,Dn→mem8(SP)  | -             | -  | -  | -  | 2         | 3     |        | 1111         | 10Dn |      |     |     |     |   |   |   |    |    |       |      |  |    | 58 |
|       | PUSH An       | SP-2→SP,An→mem16(SP) | -             | -  | -  | -  | 2         | 5     |        | 0001         | 011A |      |     |     |     |   |   |   |    |    |       |      |  |    | 58 |
| POP   | POP Dn        | mem8(SP)→Dn,SP+1→SP  | -             | -  | -  | -  | 2         | 3     |        | 1110         | 10Dn |      |     |     |     |   |   |   |    |    |       |      |  |    | 59 |
|       | POP An        | mem16(SP)→An,SP+2→SP | -             | -  | -  | -  | 2         | 4     |        | 0000         | 011A |      |     |     |     |   |   |   |    |    |       |      |  |    | 59 |
| EXT   | EXT Dn,DWm    | sign(Dn)→DWm         | -             | -  | -  | -  | 3         | 3     |        | 0010         | 1001 | 000d |     |     |     |   |   |   |    |    |       |      |  | *3 | 60 |

Arithmetic instructions

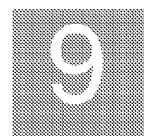
|       |                       |                        |   |   |   |   |   |   |   |      |      |          |          |     |     |     |  |  |  |  |  |  |  |    |    |    |
|-------|-----------------------|------------------------|---|---|---|---|---|---|---|------|------|----------|----------|-----|-----|-----|--|--|--|--|--|--|--|----|----|----|
| ADD   | ADD Dn,Dm             | Dm+Dn→Dm               | ● | ● | ● | ● | 3 | 2 | ○ | 0011 | 0011 | DnDm     |          |     |     |     |  |  |  |  |  |  |  |    | 61 |    |
|       | ADD imm4,Dm           | Dm+sign(imm4)→Dm       | ● | ● | ● | ● | 3 | 2 |   | 1000 | 00Dm | <#4>     |          |     |     |     |  |  |  |  |  |  |  |    | *6 | 61 |
|       | ADD imm8,Dm           | Dm+imm8→Dm             | ● | ● | ● | ● | 4 | 2 |   | 0000 | 10Dm | <#8      | ...      |     |     |     |  |  |  |  |  |  |  |    |    | 62 |
| ADDC  | ADDC Dn,Dm            | Dm+Dn+CF→Dm            | ● | ● | ● | ● | 3 | 2 | ○ | 0011 | 1011 | DnDm     |          |     |     |     |  |  |  |  |  |  |  |    |    | 63 |
| ADDW  | ADDW DWn,DWm          | DWm+DWn→DWm            | ● | ● | ● | ● | 3 | 3 | ○ | 0010 | 0101 | 00Dd     |          |     |     |     |  |  |  |  |  |  |  | *1 | 64 |    |
|       | ADDW DWn,Am           | Am+DWn→Am              | ● | ● | ● | ● | 3 | 3 | ○ | 0010 | 0101 | 10Da     |          |     |     |     |  |  |  |  |  |  |  |    |    | 64 |
|       | ADDW imm4,Am          | Am+sign(imm4)→Am       | ● | ● | ● | ● | 3 | 2 |   | 1110 | 110a | <#4>     |          |     |     |     |  |  |  |  |  |  |  |    | *6 | 65 |
|       | ADDW imm8,Am          | Am+sign(imm8)→Am       | ● | ● | ● | ● | 5 | 3 |   | 0010 | 1110 | 110a     | <#8      | ... |     |     |  |  |  |  |  |  |  |    | *7 | 65 |
|       | ADDW imm16,Am         | Am+imm16→Am            | ● | ● | ● | ● | 7 | 4 |   | 0010 | 0101 | 011a     | <#16     | ... | ... | ... |  |  |  |  |  |  |  |    | 66 |    |
|       | ADDW imm4,SP          | SP+sign(imm4)→SP       | - | - | - | - | 3 | 2 |   | 1111 | 1101 | <#4>     |          |     |     |     |  |  |  |  |  |  |  |    | *6 | 66 |
|       | ADDW imm8,SP          | SP+sign(imm8)→SP       | - | - | - | - | 4 | 2 |   | 1111 | 1100 | <#8      | ...      |     |     |     |  |  |  |  |  |  |  |    | *7 | 67 |
|       | ADDW imm16,SP         | SP+imm16→SP            | - | - | - | - | 7 | 4 |   | 0010 | 1111 | 1100     | <#16     | ... | ... | ... |  |  |  |  |  |  |  |    | 67 |    |
|       | ADDW imm16,DWm        | DWm+imm16→DWm          | ● | ● | ● | ● | 7 | 4 |   | 0010 | 0101 | 010d     | <#16     | ... | ... | ... |  |  |  |  |  |  |  |    | 68 |    |
| ADDUW | ADDUW Dn,Am           | Am+zero(Dn)→Am         | ● | ● | ● | ● | 3 | 3 | ○ | 0010 | 1000 | 1aDn     |          |     |     |     |  |  |  |  |  |  |  |    | *8 | 69 |
| ADDSW | ADDSW Dn,Am           | Am+sign(Dn)→Am         | ● | ● | ● | ● | 3 | 3 | ○ | 0010 | 1001 | 1aDn     |          |     |     |     |  |  |  |  |  |  |  |    |    | 70 |
| SUB   | SUB Dn,Dm(when Dn=Dm) | Dm-Dn→Dm               | ● | ● | ● | ● | 3 | 2 | ○ | 0010 | 1010 | DnDm     |          |     |     |     |  |  |  |  |  |  |  |    | 71 |    |
|       | SUB Dn,Dn             | Dn-Dn→Dn               | 0 | 0 | 0 | 1 | 2 | 1 |   | 1000 | 01Dn |          |          |     |     |     |  |  |  |  |  |  |  |    | 71 |    |
|       | SUB imm8,Dm           | Dm-imm8→Dm             | ● | ● | ● | ● | 5 | 3 | ○ | 0010 | 1010 | DmDm     | <#8      | ... |     |     |  |  |  |  |  |  |  |    | 72 |    |
| SUBC  | SUBC Dn,Dm            | Dm-Dn-CF→Dm            | ● | ● | ● | ● | 3 | 2 |   | 0010 | 1011 | DnDm     |          |     |     |     |  |  |  |  |  |  |  |    | 73 |    |
| SUBW  | SUBW DWn,DWm          | DWm-DWn→DWm            | ● | ● | ● | ● | 3 | 3 |   | 0010 | 0100 | 00Dd     |          |     |     |     |  |  |  |  |  |  |  | *1 | 74 |    |
|       | SUBW DWn,Am           | Am-DWn→Am              | ● | ● | ● | ● | 3 | 3 |   | 0010 | 0100 | 10Da     |          |     |     |     |  |  |  |  |  |  |  |    | 74 |    |
|       | SUBW imm16,DWm        | DWm-imm16→DWm          | ● | ● | ● | ● | 7 | 4 |   | 0010 | 0100 | 010d     | <#16     | ... | ... | ... |  |  |  |  |  |  |  |    | 75 |    |
|       | SUBW imm16,Am         | Am-imm16→Am            | ● | ● | ● | ● | 7 | 4 |   | 0010 | 0100 | 011a     | <#16     | ... | ... | ... |  |  |  |  |  |  |  |    | 75 |    |
| MULU  | MULU Dn,Dm            | Dm*Dn→DWk              | 0 | ● | ● | ● | 3 | 8 |   | 0010 | 1111 | 111D     |          |     |     |     |  |  |  |  |  |  |  |    | *4 | 76 |
| DIVU  | DIVU Dn,DWm           | DWm/Dn→DWm-l...DWm-h   | ● | ● | ● | ● | 3 | 9 |   | 0010 | 1110 | 111d     |          |     |     |     |  |  |  |  |  |  |  |    | *5 | 77 |
| CMP   | CMP Dn,Dm             | Dm-Dn...PSW            | ● | ● | ● | ● | 3 | 2 |   | 0011 | 0010 | DnDm     |          |     |     |     |  |  |  |  |  |  |  |    | 78 |    |
|       | CMP imm8,Dm           | Dm-imm8...PSW          | ● | ● | ● | ● | 4 | 2 |   | 1100 | 00Dm | <#8      | ...      |     |     |     |  |  |  |  |  |  |  |    | 78 |    |
|       | CMP imm8,(abs8)       | mem8(abs8)-imm8...PSW  | ● | ● | ● | ● | 6 | 3 |   | 0000 | 0100 | <abs 8>  | <#8      | ... |     |     |  |  |  |  |  |  |  |    | 79 |    |
|       | CMP imm8,(abs12)      | mem8(abs12)-imm8...PSW | ● | ● | ● | ● | 7 | 3 |   | 0000 | 0101 | <abs 12> | <#8      | ... |     |     |  |  |  |  |  |  |  |    | 79 |    |
|       | CMP imm8,(abs16)      | mem8(abs16)-imm8...PSW | ● | ● | ● | ● | 9 | 5 |   | 0011 | 1101 | 1000     | <abs 16> | ... | ... | ... |  |  |  |  |  |  |  |    | 80 |    |
| CMPW  | CMPW DWn,DWm          | DWm-DWn...PSW          | ● | ● | ● | ● | 3 | 3 |   | 0010 | 1000 | 01Dd     |          |     |     |     |  |  |  |  |  |  |  | *1 | 81 |    |
|       | CMPW DWn,Am           | Am-DWn...PSW           | ● | ● | ● | ● | 3 | 3 |   | 0010 | 0101 | 11Da     |          |     |     |     |  |  |  |  |  |  |  |    | 81 |    |
|       | CMPW An,Am            | Am-An...PSW            | ● | ● | ● | ● | 3 | 3 |   | 0010 | 0000 | 01Aa     |          |     |     |     |  |  |  |  |  |  |  | *2 | 82 |    |
|       | CMPW imm16,DWm        | DWm-imm16...PSW        | ● | ● | ● | ● | 6 | 3 |   | 1100 | 110d | <#16     | ...      | ... | ... |     |  |  |  |  |  |  |  |    | 82 |    |
|       | CMPW imm16,Am         | Am-imm16...PSW         | ● | ● | ● | ● | 6 | 3 |   | 1101 | 110a | <#16     | ...      | ... | ... |     |  |  |  |  |  |  |  |    | 83 |    |

Logical instructions

|     |              |              |   |   |   |   |   |   |  |      |      |      |     |     |  |  |  |  |  |  |  |  |  |  |    |    |
|-----|--------------|--------------|---|---|---|---|---|---|--|------|------|------|-----|-----|--|--|--|--|--|--|--|--|--|--|----|----|
| AND | AND Dn,Dm    | Dm&Dn→Dm     | 0 | ● | 0 | ● | 3 | 2 |  | 0011 | 0111 | DnDm |     |     |  |  |  |  |  |  |  |  |  |  | 84 |    |
|     | AND imm8,Dm  | Dm&imm8→Dm   | 0 | ● | 0 | ● | 4 | 2 |  | 0001 | 11Dm | <#8  | ... |     |  |  |  |  |  |  |  |  |  |  | 84 |    |
|     | AND imm8,PSW | PSW&imm8→PSW | ● | ● | ● | ● | 5 | 3 |  | 0010 | 1001 | 0010 | <#8 | ... |  |  |  |  |  |  |  |  |  |  | 85 |    |
| OR  | OR Dn,Dm     | Dm Dn→Dm     | 0 | ● | 0 | ● | 3 | 2 |  | 0011 | 0110 | DnDm |     |     |  |  |  |  |  |  |  |  |  |  | 86 |    |
|     | OR imm8,Dm   | Dm imm8→Dm   | 0 | ● | 0 | ● | 4 | 2 |  | 0001 | 10Dm | <#8  | ... |     |  |  |  |  |  |  |  |  |  |  | 86 |    |
|     | OR imm8,PSW  | PSW imm8→PSW | ● | ● | ● | ● | 5 | 3 |  | 0010 | 1001 | 0011 | <#8 | ... |  |  |  |  |  |  |  |  |  |  | 87 |    |
| XOR | XOR Dn,Dm    | Dm^Dn→Dm     | 0 | ● | 0 | ● | 3 | 2 |  | 0011 | 1010 | DnDm |     |     |  |  |  |  |  |  |  |  |  |  | *9 | 88 |
|     | XOR imm8,Dm  | Dm^imm8→Dm   | 0 | ● | 0 | ● | 5 | 3 |  | 0011 | 1010 | DmDm | <#8 | ... |  |  |  |  |  |  |  |  |  |  | 88 |    |

Note: "Page" refers to the corresponding page in the Instruction Manual.

- \*1 D=DWn, d=DWm
- \*2 A=An, a=Am
- \*3 d=DWm
- \*4 D=DWk
- \*5 D=DWm
- \*6 #4 sign extended
- \*7 #8 sign extended
- \*8 Dn zero extended
- \*9 m≠n







MN101C00 SERIES INSTRUCTION SET

| Group                     | Mnemonic                  | Operation   | Affected Flag  |    |    |    | Code Size | Cycle | Repeat | Machine Code               |                         |          |          |     |     |     |     |     |     |     | Notes | Page |     |     |     |     |
|---------------------------|---------------------------|---|--|----|----|----|-----------|-------|--------|----------------------------|-------------------------|----------|----------|-----|-----|-----|-----|-----|-----|-----|-------|------|-----|-----|-----|-----|
|                           |                           |   | VF   | NF | CF | ZF |           |       |        | Expand                     | 1                       | 2        | 3        | 4   | 5   | 6   | 7   | 8   | 9   | 10  |       |      | 11  |     |     |     |
| Bcc                       | BGT label                 | $\text{if}((\text{VF} \wedge \text{NF}) \wedge \text{ZF} = 0), \text{PC} + 6 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}((\text{VF} \wedge \text{NF}) \wedge \text{ZF} = 1), \text{PC} + 6 \rightarrow \text{PC}$ | -  | -  | -  | -  | 6         | 3/4   |        | 0010 0011 0001 <d11 ...    | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 107 |     |
|                           | BHI label                 | $\text{if}(\text{CF} \wedge \text{ZF} = 0), \text{PC} + 5 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{CF} \wedge \text{ZF} = 1), \text{PC} + 5 \rightarrow \text{PC}$  | -  | -  | -  | -  | 5         | 3/4   |        | 0010 0010 0010 <d7 ...     | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 108 |     |
|                           | BHI label                 | $\text{if}(\text{CF} \wedge \text{ZF} = 0), \text{PC} + 6 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{CF} \wedge \text{ZF} = 1), \text{PC} + 6 \rightarrow \text{PC}$                                       | -  | -  | -  | -  | 6         | 3/4   |        | 0010 0011 0010 <d11 ...    | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 108 |     |
|                           | BLS label                 | $\text{if}(\text{CF} \wedge \text{ZF} = 1), \text{PC} + 5 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{CF} \wedge \text{ZF} = 0), \text{PC} + 5 \rightarrow \text{PC}$  | -  | -  | -  | -  | 5         | 3/4   |        | 0010 0010 0011 <d7 ...     | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 109 |     |
|                           | BLS label                 | $\text{if}(\text{CF} \wedge \text{ZF} = 1), \text{PC} + 6 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{CF} \wedge \text{ZF} = 0), \text{PC} + 6 \rightarrow \text{PC}$                                       | -  | -  | -  | -  | 6         | 3/4   |        | 0010 0011 0011 <d11 ...    | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 109 |     |
|                           | BNC label                 | $\text{if}(\text{NF} = 0), \text{PC} + 5 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{NF} = 1), \text{PC} + 5 \rightarrow \text{PC}$  | -  | -  | -  | -  | 5         | 3/4   |        | 0010 0010 0100 <d7 ...     | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 110 |     |
|                           | BNC label                 | $\text{if}(\text{NF} = 0), \text{PC} + 6 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{NF} = 1), \text{PC} + 6 \rightarrow \text{PC}$   | -  | -  | -  | -  | 6         | 3/4   |        | 0010 0011 0100 <d11 ...    | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 110 |     |
|                           | BNS label                 | $\text{if}(\text{NF} = 1), \text{PC} + 5 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{NF} = 0), \text{PC} + 5 \rightarrow \text{PC}$  | -  | -  | -  | -  | 5         | 3/4   |        | 0010 0010 0101 <d7 ...     | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 111 |     |
|                           | BNS label                 | $\text{if}(\text{NF} = 1), \text{PC} + 6 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{NF} = 0), \text{PC} + 6 \rightarrow \text{PC}$   | -  | -  | -  | -  | 6         | 3/4   |        | 0010 0011 0101 <d11 ...    | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 111 |     |
|                           | BVC label                 | $\text{if}(\text{VF} = 0), \text{PC} + 5 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{VF} = 1), \text{PC} + 5 \rightarrow \text{PC}$  | -  | -  | -  | -  | 5         | 3/4   |        | 0010 0010 0110 <d7 ...     | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 112 |     |
|                           | BVC label                 | $\text{if}(\text{VF} = 0), \text{PC} + 6 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{VF} = 1), \text{PC} + 6 \rightarrow \text{PC}$   | -  | -  | -  | -  | 6         | 3/4   |        | 0010 0011 0110 <d11 ...    | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 112 |     |
|                           | BVS label                 | $\text{if}(\text{VF} = 1), \text{PC} + 5 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{VF} = 0), \text{PC} + 5 \rightarrow \text{PC}$  | -  | -  | -  | -  | 5         | 3/4   |        | 0010 0010 0111 <d7 ...     | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 113 |     |
|                           | BVS label                 | $\text{if}(\text{VF} = 1), \text{PC} + 6 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{VF} = 0), \text{PC} + 6 \rightarrow \text{PC}$   | -  | -  | -  | -  | 6         | 3/4   |        | 0010 0011 0111 <d11 ...    | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 113 |     |
|                           | BRA label                 | $\text{PC} + 3 + d4(\text{label}) + \text{H} \rightarrow \text{PC}$   | -  | -  | -  | -  | 3         | 3     |        | 1110 111H <d4>             | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *1  | 114 |     |
|                           | BRA label                 | $\text{PC} + 4 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$   | -  | -  | -  | -  | 4         | 3     |        | 1000 1001 <d7 ...          | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 114 |     |
|                           | BRA label                 | $\text{PC} + 5 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$  | -  | -  | -  | -  | 5         | 3     |        | 1001 1001 <d11 ...         | ...                     | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 115 |     |
|                           | CBEQ                      | CBEQ imm8, Dm, label  | $\text{if}(\text{Dm} = \text{imm8}), \text{PC} + 6 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{Dm} \neq \text{imm8}), \text{PC} + 6 \rightarrow \text{PC}$  | ●  | ●  | ●  | ●         | 6     | 3/4    |                            | 1100 10Dm <#8 ...>      | <d7 ...  | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | ... | *2  | 116 |
|                           |                           | CBEQ imm8, Dm, label  | $\text{if}(\text{Dm} = \text{imm8}), \text{PC} + 8 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{Dm} \neq \text{imm8}), \text{PC} + 8 \rightarrow \text{PC}$ | ●  | ●  | ●  | ●         | 8     | 4/5    |                            | 0010 1100 10Dm <#8 ...> | <d11 ... | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *3  | 116 |     |
| CBEQ imm8, (abs8), label  |                           | $\text{if}(\text{mem8}(\text{abs8}) = \text{imm8}), \text{PC} + 9 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs8}) \neq \text{imm8}), \text{PC} + 9 \rightarrow \text{PC}$                     | ●  | ●  | ●  | ●  | 9         | 6/7   |        | 0010 1101 1100 <abs 8...>  | <#8 ...>                | <d7 ...  | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *2  | 117 |     |     |
| CBEQ imm8, (abs8), label  |                           | $\text{if}(\text{mem8}(\text{abs8}) = \text{imm8}), \text{PC} + 10 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs8}) \neq \text{imm8}), \text{PC} + 10 \rightarrow \text{PC}$                  | ●  | ●  | ●  | ●  | 10        | 6/7   |        | 0010 1101 1101 <abs 8...>  | <#8 ...>                | <d11 ... | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *3  | 117 |     |     |
| CBEQ imm8, (abs16), label |                           | $\text{if}(\text{mem8}(\text{abs16}) = \text{imm8}), \text{PC} + 11 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs16}) \neq \text{imm8}), \text{PC} + 11 \rightarrow \text{PC}$                 | ●  | ●  | ●  | ●  | 11        | 7/8   |        | 0011 1101 1100 <abs 16...> | ...                     | <#8 ...> | <d7 ...  | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *2  | 118 |     |     |
| CBEQ imm8, (abs16), label |                           | $\text{if}(\text{mem8}(\text{abs16}) = \text{imm8}), \text{PC} + 12 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs16}) \neq \text{imm8}), \text{PC} + 12 \rightarrow \text{PC}$                | ●  | ●  | ●  | ●  | 12        | 7/8   |        | 0011 1101 1101 <abs 16...> | ...                     | <#8 ...> | <d11 ... | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *3  | 118 |     |     |
| CBNE                      | CBNE imm8, Dm, label      | $\text{if}(\text{Dm} = \text{imm8}), \text{PC} + 6 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{Dm} \neq \text{imm8}), \text{PC} + 6 \rightarrow \text{PC}$   | ●  | ●  | ●  | ●  | 6         | 3/4   |        | 1101 10Dm <#8 ...>         | <d7 ...                 | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | ... | *2  | 119 |     |
|                           | CBNE imm8, Dm, label      | $\text{if}(\text{Dm} = \text{imm8}), \text{PC} + 8 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{Dm} \neq \text{imm8}), \text{PC} + 8 \rightarrow \text{PC}$  | ●  | ●  | ●  | ●  | 8         | 4/5   |        | 0010 1101 10Dm <#8 ...>    | <d11 ...                | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *3  | 119 |     |     |
|                           | CBNE imm8, (abs8), label  | $\text{if}(\text{mem8}(\text{abs8}) \neq \text{imm8}), \text{PC} + 9 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs8}) = \text{imm8}), \text{PC} + 9 \rightarrow \text{PC}$                     | ●  | ●  | ●  | ●  | 9         | 6/7   |        | 0010 1101 1110 <abs 8...>  | <#8 ...>                | <d7 ...  | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *2  | 120 |     |     |
|                           | CBNE imm8, (abs8), label  | $\text{if}(\text{mem8}(\text{abs8}) \neq \text{imm8}), \text{PC} + 10 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs8}) = \text{imm8}), \text{PC} + 10 \rightarrow \text{PC}$                  | ●  | ●  | ●  | ●  | 10        | 6/7   |        | 0010 1101 1111 <abs 8...>  | <#8 ...>                | <d11 ... | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *3  | 120 |     |     |
|                           | CBNE imm8, (abs16), label | $\text{if}(\text{mem8}(\text{abs16}) \neq \text{imm8}), \text{PC} + 11 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs16}) = \text{imm8}), \text{PC} + 11 \rightarrow \text{PC}$                 | ●  | ●  | ●  | ●  | 11        | 7/8   |        | 0011 1101 1110 <abs 16...> | ...                     | <#8 ...> | <d7 ...  | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *2  | 121 |     |     |
|                           | CBNE imm8, (abs16), label | $\text{if}(\text{mem8}(\text{abs16}) \neq \text{imm8}), \text{PC} + 12 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs16}) = \text{imm8}), \text{PC} + 12 \rightarrow \text{PC}$                | ●  | ●  | ●  | ●  | 12        | 7/8   |        | 0011 1101 1111 <abs 16...> | ...                     | <#8 ...> | <d11 ... | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *3  | 121 |     |     |
| TBZ                       | TBZ (abs8)bp, label       | $\text{if}(\text{mem8}(\text{abs8}) \text{bp} = 0), \text{PC} + 7 + d7(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs8}) \text{bp} = 1), \text{PC} + 7 \rightarrow \text{PC}$                        | 0  | ●  | 0  | ●  | 7         | 6/7   |        | 0011 0000 0bp <abs 8...>   | <d7 ...                 | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *2  | 122 |     |     |
|                           | TBZ (abs8)bp, label       | $\text{if}(\text{mem8}(\text{abs8}) \text{bp} = 0), \text{PC} + 8 + d11(\text{label}) + \text{H} \rightarrow \text{PC}$<br>$\text{if}(\text{mem8}(\text{abs8}) \text{bp} = 1), \text{PC} + 8 \rightarrow \text{PC}$                       | 0  | ●  | 0  | ●  | 8         | 6/7   |        | 0011 0000 1bp <abs 8...>   | <d11 ...                | ...      | ...      | ... | ... | ... | ... | ... | ... | ... | ...   | ...  | *3  | 122 |     |     |

Note: "Page" refers to the corresponding page in the Instruction Manual.

- \*1 d4 sign extended
- \*2 d7 sign extended
- \*3 d11 sign extended

Appendices

MN101C00 SERIES INSTRUCTION SET

| Group | Mnemonic             | Operation  | Affected Flag |    |    | Code Size | Cycle | Repeat | Machine Code |      |      |      |      |      |      |      |      |    |     | Notes | Page |
|-------|----------------------|--|---------------|----|----|-----------|-------|--------|--------------|------|------|------|------|------|------|------|------|----|-----|-------|------|
|       |                      |  | VF            | NF | CF |           |       |        | ZF           | 1    | 2    | 3    | 4    | 5    | 6    | 7    | 8    | 9  | 10  |       |      |
| TBZ   | TBZ (io8)bp,label    | if(mem8(OTOP+io8)bp=0),PC+7-d7(label)+H→PC<br>if(mem8(OTOP+io8)bp=1),PC+7→PC   | 0             | ●  | 0  | ●         | 7     | 6/7    |              | 0011 | 0100 | 0bp. | <io8 | ...  | <d7. | ...H |      | *1 | 123 |       |      |
|       | TBZ (io8)bp,label    | if(mem8(OTOP+io8)bp=0),PC+8-d11(label)+H→PC<br>if(mem8(OTOP+io8)bp=1),PC+8→PC  | 0             | ●  | 0  | ●         | 8     | 6/7    |              | 0011 | 0100 | 1bp. | <io8 | ...  | <d11 | ...H |      | *2 | 123 |       |      |
|       | TBZ (abs16)bp,label  | if(mem8(abs16)bp=0),PC+5+c7(label)+H→PC<br>if(mem8(abs16)bp=1),PC+9→PC   | 0             | ●  | 0  | ●         | 9     | 7/8    |              | 0011 | 1110 | 0bp. | <abs | 16.. | ...  | <d7. | ...H |    | *1  | 124   |      |
|       | TBZ (abs16)bp,label  | if(mem8(abs16)bp=0),PC+10+d11(label)+H→PC<br>if(mem8(abs16)bp=1),PC+10→PC  | 0             | ●  | 0  | ●         | 10    | 7/8    |              | 0011 | 1110 | 1bp. | <abs | 16.. | ...  | <d11 | ...H |    | *2  | 124   |      |
| TBNZ  | TBNZ (abs8)bp,label  | if(mem8(abs8)bp=1),PC+7-d7(label)+H→PC<br>if(mem8(abs8)bp=0),PC+7→PC   | 0             | ●  | 0  | ●         | 7     | 6/7    |              | 0011 | 0001 | 0bp. | <abs | 8.>  | <d7. | ...H |      | *1 | 125 |       |      |
|       | TBNZ (abs8)bp,label  | if(mem8(abs8)bp=1),PC+8-d11(label)+H→PC<br>if(mem8(abs8)bp=0),PC+8→PC  | 0             | ●  | 0  | ●         | 8     | 6/7    |              | 0011 | 0001 | 1bp. | <abs | 8.>  | <d11 | ...H |      | *2 | 125 |       |      |
|       | TBNZ (io8)bp,label   | if(mem8(io)bp=1),PC+7+d7(label)+H→PC<br>if(mem8(io)bp=0),PC+7→PC   | 0             | ●  | 0  | ●         | 7     | 6/7    |              | 0011 | 0101 | 0bp. | <io8 | ...  | <d7. | ...H |      | *1 | 126 |       |      |
|       | TBNZ (io8)bp,label   | if(mem8(io)bp=1),PC+8+d11(label)+H→PC<br>if(mem8(io)bp=0),PC+8→PC  | 0             | ●  | 0  | ●         | 8     | 6/7    |              | 0011 | 0101 | 1bp. | <io8 | ...  | <d11 | ...H |      | *2 | 126 |       |      |
|       | TBNZ (abs16)bp,label | if(mem8(abs16)bp=1),PC+5+c7(label)+H→PC<br>if(mem8(abs16)bp=0),PC+9→PC   | 0             | ●  | 0  | ●         | 9     | 7/8    |              | 0011 | 1111 | 0bp. | <abs | 16.. | ...  | <d7. | ...H |    | *1  | 127   |      |
|       | TBNZ (abs16)bp,label | if(mem8(abs16)bp=1),PC+10+d11(label)+H→PC<br>if(mem8(abs16)bp=0),PC+10→PC  | 0             | ●  | 0  | ●         | 10    | 7/8    |              | 0011 | 1111 | 1bp. | <abs | 16.. | ...  | <d11 | ...H |    | *2  | 127   |      |
| JMP   | JMP (An)             | 0→PC.17-16,An→PC.15-0,0→PC.H   | -             | -  | -  | -         | 3     | 4      |              | 0010 | 0001 | 00A0 |      |      |      |      |      |    | 128 |       |      |
|       | JMP label            | abs18(label)+H→PC  | -             | -  | -  | -         | 7     | 5      |              | 0011 | 1001 | 0aaH | <abs | 18b  | p15- | 0..> |      | *5 | 128 |       |      |
| JSR   | JSR (An)             | SP-3→SP,(PC+3).bp7-0→mem8(SP)<br>(PC+3).bp15-8→mem8(SP+1)<br>(PC+3).H→mem8(SP+2).bp7,<br>0→mem8(SP+2).bp6-2,<br>(PC+3).bp17-16→mem8(SP+2).bp1-0<br>0→PC.bp17-16<br>An→PC.bp15-0,0→PC.H   | -             | -  | -  | -         | 3     | 7      |              | 0010 | 0001 | 00A1 |      |      |      |      |      |    | 129 |       |      |
|       | JSR label            | SP-3→SP,(PC+5).bp7-0→mem8(SP)<br>(PC+5).bp15-8→mem8(SP+1)<br>(PC+5).H→mem8(SP+2).bp7,<br>0→mem8(SP+2).bp6-2,<br>(PC+5).bp17-16→mem8(SP+2).bp1-0<br>PC+5+d12(label)+H→PC  | -             | -  | -  | -         | 5     | 6      |              |      | 0001 | 000H | <d12 | ...  | ...  |      |      | *3 | 129 |       |      |
|       | JSR label            | SP-3→SP,(PC+6).bp7-0→mem8(SP)<br>(PC+6).bp15-8→mem8(SP+1)<br>(PC+6).H→mem8(SP+2).bp7,<br>0→mem8(SP+2).bp6-2,<br>(PC+6).bp17-16→mem8(SP+2).bp1-0<br>PC+6+d16(label)+H→PC  | -             | -  | -  | -         | 6     | 7      |              |      | 0001 | 001H | <d16 | ...  | ...  |      |      | *4 | 130 |       |      |
|       | JSR label            | SP-3→SP,(PC+7).bp7-0→mem8(SP)<br>(PC+7).bp15-8→mem8(SP+1)<br>(PC+7).H→mem8(SP+2).bp7,<br>0→mem8(SP+2).bp6-2,<br>(PC+7).bp17-16→mem8(SP+2).bp1-0<br>abs18(label)+H→PC   | -             | -  | -  | -         | 7     | 8      |              | 0011 | 1001 | 1aaH | <abs | 18b  | p15- | 0..> |      | *5 | 130 |       |      |
|       | JSRV (tb4)           | SP-3→SP,(PC+3).bp7-0→mem8(SP)<br>(PC+3).bp15-8→mem8(SP+1)<br>(PC+3).H→mem8(SP+2).bp7<br>0→mem8(SP+2).bp6-2,<br>(PC+3).bp17-16→mem8(SP+2).bp1-0<br>mem8(x'004080+tb4<<2)→PC.bp7-0<br>mem8(x'004080+tb4<<2+1)→PC.bp15-8<br>mem8(x'004080+tb4<<2+2)bp7→PC.H<br>mem8(x'004080+tb4<<2+2).bp1-0<br>PC.bp17-16<br>PC+2→PC | -             | -  | -  | -         | 3     | 9      |              |      | 1111 | 1110 | <t4> |      |      |      |      |    |     | 131   |      |
|       | NOP                  | NOP  |               | -  | -  | -         | -     | 2      | 1            |      | 0000 | 0000 |      |      |      |      |      |    |     | 132   |      |

Note: "Page" refers to the corresponding page in the Instruction Manual.

- \*1 d7 sign extended
- \*2 c11 sign extended
- \*3 c12 sign extended
- \*4 c16 sign extended
- \*5 aa=abs18.17-16

MN101C00 SERIES INSTRUCTION SET

| Group               | Mnemonic | Operation  | Affected Flag |    |    | Code Size | Cycle | Repeat | Machine Code |        |      |   |   |   |   |   |   |   |   | Notes | Page |    |    |     |     |
|---------------------|----------|--|---------------|----|----|-----------|-------|--------|--------------|--------|------|---|---|---|---|---|---|---|---|-------|------|----|----|-----|-----|
|                     |          |  | VF            | NF | CF |           |       |        | ZF           | Expand | 1    | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |       |      | 10 | 11 |     |     |
| RTS                 | RTS      | mem8(SP)→(PC).bp7~0<br>mem8(SP+1)→(PC+3).bp15~8<br>mem8(SP+2).bp7→(PC+3).H<br>mem8(SP+2).bp1~0→(PC+3).tp17~16<br>SP+3→SP   | -             | -  | -  | 2         | 7     |        | 0000         | 0001   |      |   |   |   |   |   |   |   |   |       |      |    |    | 133 |     |
| RTI                 | RTI      | mem8(SP)→PSW<br>mem8(SP+1)→(PC).bp7~0<br>mem8(SP+2)→(PC+3).bp15~8<br>mem8(SP+3).bp7→(PC+3).H<br>mem8(SP+3).bp1~0→(PC+3).bp17~16<br>mem8(SP+4)→HA-l<br>mem8(SP+5)→HA-h<br>SP+6→SP | ●             | ●  | ●  | 2         | 11    |        | 0000         | 0011   |      |   |   |   |   |   |   |   |   |       |      |    |    | 134 |     |
| Control instruction |          |  |               |    |    |           |       |        |              |        |      |   |   |   |   |   |   |   |   |       |      |    |    |     |     |
| REP                 | REP imm3 | imm3→RPC   | --            | -- | -- | 3         | 2     |        | 0010         | 0001   | 1rep |   |   |   |   |   |   |   |   |       |      |    |    | *1  | 135 |

Note: "Page" refers to the corresponding page in the Instruction Manual.

\*1 Number of repeats is 0 when imm3=0.

### MN101C00 SERIES INSTRUCTION MAP

| 1st nibble |                                    | 2nd nibble     |              |                       |                       |                  |                |               |         |         |              |             |              |         |         |  |  |
|------------|------------------------------------|----------------|--------------|-----------------------|-----------------------|------------------|----------------|---------------|---------|---------|--------------|-------------|--------------|---------|---------|--|--|
| 0          | 1                                  | 2              | 3            | 4                     | 5                     | 6                | 7              | 8             | 9       | A       | B            | C           | D            | E       | F       |  |  |
| 0          | NOP                                | RTS            | MOV #8,(io8) | RTI                   | CMP #8,(abs8)/(abs12) | POP An           |                | ADD #8,Dm     |         |         |              | MOVW #8,DWm | MOVW #8,Am   |         |         |  |  |
| 1          | JSR d12(label)                     | JSR d16(label) |              | MOV #8,(abs8)/(abs12) |                       | PUSH An          |                | OR #8,Dm      |         |         |              | AND #8,Dm   |              |         |         |  |  |
| 2          | When the extension code is b'0010' |                |              |                       |                       |                  |                |               |         |         |              |             |              |         |         |  |  |
| 3          | When the extension code is b'0011' |                |              |                       |                       |                  |                |               |         |         |              |             |              |         |         |  |  |
| 4          | MOV (abs12),Dm                     |                |              | MOV (abs8),Dm         |                       |                  | MOV (An),Dm    |               |         |         |              |             |              |         |         |  |  |
| 5          | MOV Dn,(abs12)                     |                |              | MOV Dn,(abs8)         |                       |                  | MOV Dn,(Am)    |               |         |         |              |             |              |         |         |  |  |
| 6          | MOV (io8),Dm                       |                |              | MOV (d4,SP),Dm        |                       |                  | MOV (d8,An),Dm |               |         |         |              |             |              |         |         |  |  |
| 7          | MOV Dn,(io8)                       |                |              | MOV Dn,(d4,SP)        |                       |                  | MOV Dn,(d8,Am) |               |         |         |              |             |              |         |         |  |  |
| 8          | ADD #4,Dm                          |                |              | SUB Dn,Dn             |                       |                  | BGE d7         |               | BRA d7  | BEQ d7  | BNE d7       | BCC d7      | BCS d7       | BLT d7  | BLE d7  |  |  |
| 9          | BEQ d4                             |                | BNE d4       | MOVW DWn,(HA)         |                       | MOVW An,(HA)     |                | BGE d11       | BRA d11 | BEQ d11 | BNE d11      | BCC d11     | BCS d11      | BLT d11 | BLE d11 |  |  |
| A          | MOV Dn,Dm / MOV #8,Dm              |                |              |                       |                       |                  |                |               |         |         |              |             |              |         |         |  |  |
| B          | BSET (abs8)bp                      |                |              |                       |                       |                  |                | BCLR (abs8)bp |         |         |              |             |              |         |         |  |  |
| C          | CMP #8,Dm                          |                |              | MOVW (abs8),Am        |                       | MOVW (abs8),DWn  |                | CBEQ #8,Dm,d7 |         |         | CMPW #16,DWm |             | MOVW #16,DWm |         |         |  |  |
| D          | MOV Dn,(HA)                        |                |              | MOVW An,(abs8)        |                       | MOVW DWn,(abs8)  |                | CBNE #8,Dm,d7 |         |         | CMPW #16,Am  |             | MOVW #16,Am  |         |         |  |  |
| E          | MOVW (An),DWm                      |                |              | MOVW (d4,SP),Am       |                       | MOVW (d4,SP),DWm |                | POP Dn        |         |         | ADDW #4,Am   |             | BRA d4       |         |         |  |  |
| F          | MOVW DWn,(Am)                      |                |              | MOVW An,(d4,SP)       |                       | MOVW DWn,(d4,SP) |                | PUSH Dn       |         |         | ADDW #8,SP   | ADDW #4,SP  | JSRV (tbl4)  |         |         |  |  |

Extension code: b'0010'

| 1st nibble |                          | 2nd nibble |                   |                 |            |                  |                 |                |            |   |                       |        |                       |   |   |  |  |
|------------|--------------------------|------------|-------------------|-----------------|------------|------------------|-----------------|----------------|------------|---|-----------------------|--------|-----------------------|---|---|--|--|
| 0          | 1                        | 2          | 3                 | 4               | 5          | 6                | 7               | 8              | 9          | A | B                     | C      | D                     | E | F |  |  |
| 0          | MOVW An,Am               |            |                   | CMPW An,Am      |            |                  | MOVW SP,Am      |                | MOVW An,SP |   | BTST #8,Dm            |        |                       |   |   |  |  |
| 1          | JMP (A0)                 | JSR (A0)   | JMP (A1)          | JSR (A1)        | MOV PSW,Dm |                  |                 | REP #3         |            |   |                       |        |                       |   |   |  |  |
| 2          |                          | BGT d7     | BHI d7            | BLS d7          | BNC d7     | BNS d7           | BVC d7          | BVS d7         | NOT Dn     |   |                       | ROR Dn |                       |   |   |  |  |
| 3          |                          | BGT d11    | BHI d11           | BLS d11         | BNC d11    | BNS d11          | BVC d11         | BVS d11        | ASR Dn     |   |                       | LSR Dn |                       |   |   |  |  |
| 4          | SUBW DWn,DWm             |            |                   | SUBW #16,DWm    |            | SUBW #16,Am      |                 | SUBW DWn,Am    |            |   | MOVW DWn,Am           |        |                       |   |   |  |  |
| 5          | ADDW DWn,DWm             |            |                   | ADDW #16,DWm    |            | ADDW #16,Am      |                 | ADDW DWn,Am    |            |   | CMPW DWn,Am           |        |                       |   |   |  |  |
| 6          | MOV (d16,SP),Dm          |            |                   | MOV (d8,SP),Dm  |            |                  | MOV (d16,An),Dm |                |            |   |                       |        |                       |   |   |  |  |
| 7          | MOV Dn,(d16,SP)          |            |                   | MOV Dn,(d8,SP)  |            |                  | MOV Dn,(d16,Am) |                |            |   |                       |        |                       |   |   |  |  |
| 8          | MOVW DWn,DWm (NOPL @n=m) |            |                   | CMPW DWn,DWm    |            |                  | ADDUW Dn,Am     |                |            |   |                       |        |                       |   |   |  |  |
| 9          | EXT Dn,DWm               |            | AND #8,PSW        | OR #8,PSW       | MOV Dn,PSW |                  |                 | ADDSW Dn,Am    |            |   |                       |        |                       |   |   |  |  |
| A          | SUB Dn,Dm / SUB #8,Dm    |            |                   |                 |            |                  |                 |                |            |   |                       |        |                       |   |   |  |  |
| B          | SUBC Dn,Dm               |            |                   |                 |            |                  |                 |                |            |   |                       |        |                       |   |   |  |  |
| C          | MOV (abs16),Dm           |            |                   | MOVW (abs16),Am |            | MOVW (abs16),DWm |                 | CBEQ #8,Dm,d12 |            |   | MOVW An,DWm           |        |                       |   |   |  |  |
| D          | MOV Dn,(abs16)           |            |                   | MOVW An,(abs16) |            | MOVW DWn,(abs16) |                 | CBNE #8,Dm,d12 |            |   | CBEQ #8,(abs8),d7/d11 |        | CBNE #8,(abs8),d7/d11 |   |   |  |  |
| E          | MOVW (d16,SP),Am         |            | MOVW (d16,SP),DWm | MOVW (d8,SP),Am |            | MOVW (d8,SP),DWm |                 | MOVW (An),Am   |            |   | ADDW #8,Am            |        | DIVU                  |   |   |  |  |
| F          | MOVW An,(d16,SP)         |            | MOVW DWn,(d16,SP) | MOVW An,(d8,SP) |            | MOVW DWn,(d8,SP) |                 | MOVW An,(Am)   |            |   | ADDW #16,SP           |        | MULU                  |   |   |  |  |

Extension code: b'0011'  
 2nd nibble\3rd nibble

|   | 0                     | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8                  | 9 | A              | B | C | D | E                    | F |                      |  |
|---|-----------------------|---|---|---|---|---|---|---|--------------------|---|----------------|---|---|---|----------------------|---|----------------------|--|
| 0 | TBZ (abs8)bp,d7       |   |   |   |   |   |   |   | TBZ (abs8)bp,d11   |   |                |   |   |   |                      |   |                      |  |
| 1 | TBNZ (abs8)bp,d7      |   |   |   |   |   |   |   | TBNZ (abs8)bp,d11  |   |                |   |   |   |                      |   |                      |  |
| 2 | CMP Dn,Dm             |   |   |   |   |   |   |   |                    |   |                |   |   |   |                      |   |                      |  |
| 3 | ADD Dn,Dm             |   |   |   |   |   |   |   |                    |   |                |   |   |   |                      |   |                      |  |
| 4 | TBZ (io8)bp,c7        |   |   |   |   |   |   |   | TBZ (io8)bp,d11    |   |                |   |   |   |                      |   |                      |  |
| 5 | TBNZ (io8)bp,d7       |   |   |   |   |   |   |   | TBNZ (io8)bp,d11   |   |                |   |   |   |                      |   |                      |  |
| 6 | OR Dn,Dm              |   |   |   |   |   |   |   |                    |   |                |   |   |   |                      |   |                      |  |
| 7 | AND Dn,Dm             |   |   |   |   |   |   |   |                    |   |                |   |   |   |                      |   |                      |  |
| 8 | BSET (io8)bp          |   |   |   |   |   |   |   | BCLR (io8)bp       |   |                |   |   |   |                      |   |                      |  |
| 9 | JMP abs18(label)      |   |   |   |   |   |   |   | JSR abs18(label)   |   |                |   |   |   |                      |   |                      |  |
| A | XOR Dn,Dm / XOR #8,Dm |   |   |   |   |   |   |   |                    |   |                |   |   |   |                      |   |                      |  |
| B | ADDC Dn,Dm            |   |   |   |   |   |   |   |                    |   |                |   |   |   |                      |   |                      |  |
| C | BSET (abs16)bp        |   |   |   |   |   |   |   | BCLR (abs16)bp     |   |                |   |   |   |                      |   |                      |  |
| D | BTST (abs16)bp        |   |   |   |   |   |   |   | cmp #8,(abs16)     |   | mov #8,(abs16) |   |   |   | CBEQ #8,(abs16),d7/1 |   | CBNE #8,(abs16),d7/1 |  |
| E | TBZ (abs16)bp,d7      |   |   |   |   |   |   |   | TBZ (abs16)bp,d11  |   |                |   |   |   |                      |   |                      |  |
| F | TBNZ (abs16)bp,d7     |   |   |   |   |   |   |   | TBNZ (abs16)bp,d11 |   |                |   |   |   |                      |   |                      |  |

Summary of Special Function Registers (1/6)

| Address | Register | Bit Symbol  |   |  |  |   |   |   |                        | Reference Page             |
|---------|----------|---|---|--|--|---|---|---|------------------------|----------------------------|
|         |          | Bit 7   | Bit 6   | Bit 5  | Bit 4                                    | Bit 3                                   | Bit 2   | Bit 1   | Bit 0                  |                            |
| X'3F00' | CPUM     |   |   |  | Must be set to "0"                       | STOP transfer request                   | HALT transfer request                             | Oscillation control                                 |                        | MN101C00 Series LSI Manual |
| X'3F01' | MEMCTR   | IOW1  | IOW0  | IVBA   | EXMEM                                    | EXWH                                    | IRWE  | EXW1  | EXW0                   | 34                         |
|         |          | Specifies number of I/O bus wait cycles                     |   | Specifies base address of interrupt vector table           | Specifies external memory expansion mode | Switches fixed wait mode/handshake mode | Software write setting for interrupt request flag | Specifies number of wait cycles for external memory |                        |                            |
| X'3F02' | WDCTR    |   |   |  |  |   |   |   | WDEN                   | 117                        |
|         |          |   |   |  |  |   |   |   | Enables watchdog timer |                            |
| X'3F03' | DLYCTR   | BUZOE   | BUZCK1  | BUZCK0   |  |   |   | DLYS1   | DLYS0                  | 118                        |
|         |          | Selects P06 output  | Selects buzzer output frequency                             |  |  |   |   | Sets oscillation stabilization wait period          |                        |                            |
| X'3F0E' | EXADV    | EXADV3  | EXADV2  | EXADV1   |  |   |   |   |                        | 35                         |
|         |          | Enables A17-A16 address output during memory expansion mode | Enables A15-A12 address output during memory expansion mode | Enables A11-A8 address output during memory expansion mode |  |   |   |   |                        |                            |
| X'3F10' | P0OUT    |   | P0OUT6  | P0OUT5   | P0OUT4                                   | P0OUT3                                  | P0OUT2  | P0OUT1  | P0OUT0                 | 49,54                      |
|         |          |   | Port 0 output   |  |  |   |   |   |                        |                            |
| X'3F11' | P1OUT    |   |   |  | P1OUT4                                   | P1OUT3                                  | P1OUT2  | P1OUT1  | P1OUT0                 | 49,54                      |
|         |          |   | Port 1 output   |  |  |   |   |   |                        |                            |
| X'3F12' | P2OUT    | P2OUT7  |   |  |  |   |   |   |                        | 49,54                      |
|         |          | Port 2 output   |   |  |  |   |   |   |                        |                            |
| X'3F13' | P3OUT    | P3OUT7  | P3OUT6  | P3OUT5   | P3OUT4                                   | P3OUT3                                  | P3OUT2  | P3OUT1  | P3OUT0                 | 49,54                      |
|         |          | Port 3 output   |   |  |  |   |   |   |                        |                            |
| X'3F14' | P4OUT    | P4OUT7  | P4OUT6  | P4OUT5   | P4OUT4                                   | P4OUT3                                  | P4OUT2  | P4OUT1  | P4OUT0                 | 49,54                      |
|         |          | Port 4 output   |   |  |  |   |   |   |                        |                            |
| X'3F15' | P5OUT    |   |   |  | P5OUT4                                   | P5OUT3                                  | P5OUT2  | P5OUT1  | P5OUT0                 | 49,54                      |
|         |          |   |   |  | Port 5 output                            |   |   |   |                        |                            |
| X'3F16' | P6OUT    | P6OUT7  | P6OUT6  | P6OUT5   | P6OUT4                                   | P6OUT3                                  | P6OUT2  | P6OUT1  | P6OUT0                 | 49,54                      |
|         |          | Port 6 output   |   |  |  |   |   |   |                        |                            |
| X'3F17' | P7OUT    | P7OUT7  | P7OUT6  | P7OUT5   | P7OUT4                                   | P7OUT3                                  | P7OUT2  | P7OUT1  | P7OUT0                 | 49,54                      |
|         |          | Port 7 output   |   |  |  |   |   |   |                        |                            |
| X'3F18' | P8OUT    | P8OUT7  | P8OUT6  | P8OUT5   | P8OUT4                                   | P8OUT3                                  | P8OUT2  | P8OUT1  | P8OUT0                 | 49,54                      |
|         |          | Port 8 output   |   |  |  |   |   |   |                        |                            |
| X'3F1F' | SYSDM    | SYSDM7  | SYSDM6  | SYSDM5   | SYSDM4                                   | SYSDM3                                  | SYSDM2  | SYSDM1  | SYSDM0                 | 49,55                      |
|         |          | I/O port/Synchronous output control                         |   |  |  |   |   |   |                        |                            |
| X'3F20' | P0IN     |   | P0IN6   | P0IN5  | P0IN4                                    | P0IN3                                   | P0IN2   | P0IN1   | P0IN0                  | 49,54                      |
|         |          |   | Port 0 input  |  |  |   |   |   |                        |                            |
| X'3F21' | P1IN     |   |   |  | P1IN4                                    | P1IN3                                   | P1IN2   | P1IN1   | P1IN0                  | 49,54                      |
|         |          |   | Port 1 input  |  |  |   |   |   |                        |                            |
| X'3F22' | P2IN     |   |   |  | P2IN4                                    | P2IN3                                   | P2IN2   | P2IN1   | P2IN0                  | 49,54                      |
|         |          |   | Port 2 input  |  |  |   |   |   |                        |                            |
| X'3F23' | P3IN     | P3IN7   | P3IN6   | P3IN5  | P3IN4                                    | P3IN3                                   | P3IN2   | P3IN1   | P3IN0                  | 49,54                      |
|         |          | Port 3 input  |   |  |  |   |   |   |                        |                            |
| X'3F24' | P4IN     | P4IN7   | P4IN6   | P4IN5  | P4IN4                                    | P4IN3                                   | P4IN2   | P4IN1   | P4IN0                  | 49,54                      |
|         |          | Port 4 input  |   |  |  |   |   |   |                        |                            |
| X'3F25' | P5IN     |   |   |  | P5IN4                                    | P5IN3                                   | P5IN2   | P5IN1   | P5IN0                  | 49,54                      |
|         |          |   | Port 5 input  |  |  |   |   |   |                        |                            |

Summary of Special Function Registers (2/6)

| Address  | Register | Bit Symbol                             |        |        |        |  |  |  |  | Reference Page |
|--|----------|--|--------|--------|--------|--|--|--|--|----------------|
|  |          | Bit 7                                  | Bit 6  | Bit 5  | Bit 4  | Bit 3                                    | Bit 2                                    | Bit 1                                    | Bit 0                                    |                |
| X'3F26'  | P6IN     | P6IN7                                  | P6IN6  | P6IN5  | P6IN4  | P6IN3                                    | P6IN2                                    | P6IN1                                    | P6IN0                                    | 49,54          |
| Port 6 input                                     |          |  |        |        |        |  |  |  |  |                |
| X'3F27'  | P7IN     | P7IN7                                  | P7IN6  | P7IN5  | P7IN4  | P7IN3                                    | P7IN2                                    | P7IN1                                    | P7IN0                                    | 49,54          |
| Port 7 input                                     |          |  |        |        |        |  |  |  |  |                |
| X'3F28'  | P8IN     | P8IN7                                  | P8IN6  | P8IN5  | P8IN4  | P8IN3                                    | P8IN2                                    | P8IN1                                    | P8IN0                                    | 49,54          |
| Port 8 input                                     |          |  |        |        |        |  |  |  |  |                |
| X'3F2A'  | PAIN     | PAIN7                                  | PAIN6  | PAIN5  | PAIN4  | PAIN3                                    | PAIN2                                    | PAIN1                                    | PAIN0                                    | 49,54          |
| Port A input                                     |          |  |        |        |        |  |  |  |  |                |
| X'3F30'  | P0DIR    |  | P0DIR6 | P0DIR5 | P0DIR4 | P0DIR3                                   | P0DIR2                                   | P0DIR1                                   | P0DIR0                                   | 49,54          |
| Port 0 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F31'  | P1DIR    |  |        |        | P1DIR4 | P1DIR3                                   | P1DIR2                                   | P1DIR1                                   | P1DIR0                                   | 49,54          |
| Port 1 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F33'  | P3DIR    | P3DIR7                                 | P3DIR6 | P3DIR5 | P3DIR4 | P3DIR3                                   | P3DIR2                                   | P3DIR1                                   | P3DIR0                                   | 49,54          |
| Port 3 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F34'  | P4DIR    | P4DIR7                                 | P4DIR6 | P4DIR5 | P4DIR4 | P4DIR3                                   | P4DIR2                                   | P4DIR1                                   | P4DIR0                                   | 50,54          |
| Port 4 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F35'  | P5DIR    |  |        |        | P5DIR4 | P5DIR3                                   | P5DIR2                                   | P5DIR1                                   | P5DIR0                                   | 50,54          |
| Port 5 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F36'  | P6DIR    | P6DIR7                                 | P6DIR6 | P6DIR5 | P6DIR4 | P6DIR3                                   | P6DIR2                                   | P6DIR1                                   | P6DIR0                                   | 50,54          |
| Port 6 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F37'  | P7DIR    | P7DIR7                                 | P7DIR6 | P7DIR5 | P7DIR4 | P7DIR3                                   | P7DIR2                                   | P7DIR1                                   | P7DIR0                                   | 50,54          |
| Port 7 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F38'  | P8DIR    | P8DIR7                                 | P8DIR6 | P8DIR5 | P8DIR4 | P8DIR3                                   | P8DIR2                                   | P8DIR1                                   | P8DIR0                                   | 50,54          |
| Port 8 I/O direction control                     |          |  |        |        |        |  |  |  |  |                |
| X'3F39'  | P1OMD    |  |        |        | P14TCO | P13TCO                                   | P12TCO                                   | P11TCO                                   | P10TCO                                   | 50,55          |
| I/O port/Special function pin control            |          |  |        |        |        |  |  |  |  |                |
| X'3F3A'  | PAIMD    | PAAIN7                                 | PAAIN6 | PAAIN5 | PAAIN4 | PAAIN3                                   | PAAIN2                                   | PAAIN1                                   | PAAIN0                                   | 50,55          |
| I/O port/Special function pin control            |          |  |        |        |        |  |  |  |  |                |
| X'3F3C'  | P4IMD    | IRQ4SEL<br>Select IRQ interrupt source |        |        |        | P4KYEN4<br>Select PA6, PA7 key interrupt | P4KYEN3<br>Select PA4, PA5 key interrupt | P4KYEN2<br>Select PA2, PA3 key interrupt | P4KYEN1<br>Select PA0, PA1 key interrupt | 50,55          |
| X'3F40'  | P0PLU    |  | P0PLU6 | P0PLU5 | P0PLU4 | P0PLU3                                   | P0PLU2                                   | P0PLU1                                   | P0PLU0                                   |                |
| Port 0 pull-up resistor ON/OFF control           |          |  |        |        |        |  |  |  |  |                |
| X'3F41'  | P1PLU    |  |        |        | P1PLU4 | P1PLU3                                   | P1PLU2                                   | P1PLU1                                   | P1PLU0                                   | 50,54          |
| Port 1 pull-up resistor ON/OFF control           |          |  |        |        |        |  |  |  |  |                |
| X'3F42'  | P2PLU    |  |        |        | P2PLU4 | P2PLU3                                   | P2PLU2                                   | P2PLU1                                   | P2PLU0                                   | 50,54          |
| Port 2 pull-up resistor ON/OFF control           |          |  |        |        |        |  |  |  |  |                |
| X'3F43'  | P3PLU    | P3PLU7                                 | P3PLU6 | P3PLU5 | P3PLU4 | P3PLU3                                   | P3PLU2                                   | P3PLU1                                   | P3PLU0                                   | 50,54          |
| Port 3 pull-up/pull-down resistor ON/OFF control |          |  |        |        |        |  |  |  |  |                |
| X'3F44'  | P4PLU    | P4PLU7                                 | P4PLU6 | P4PLU5 | P4PLU4 | P4PLU3                                   | P4PLU2                                   | P4PLU1                                   | P4PLU0                                   | 50,54          |
| Port 4 pull-up resistor ON/OFF control           |          |  |        |        |        |  |  |  |  |                |
| X'3F45'  | P5PLU    |  |        |        | P5PLU4 | P5PLU3                                   | P5PLU2                                   | P5PLU1                                   | P5PLU0                                   | 50,54          |
| Port 5 pull-up resistor ON/OFF control           |          |  |        |        |        |  |  |  |  |                |



Summary of Special Function Registers (3/6)

| Address | Register | Bit Symbol   |  |                                    |  |  |                                |                                     |   | Reference Page |
|---------|----------|--|--|------------------------------------|--|--|--------------------------------|-------------------------------------|---|----------------|
|         |          | Bit 7  | Bit 6  | Bit 5                              | Bit 4                                      | Bit 3                                      | Bit 2                          | Bit 1                               | Bit 0                                   |                |
| X'3F46' | P6PLU    | P6PLU7   | P6PLU6   | P6PLU5                             | P6PLU4                                     | P6PLU3                                     | P6PLU2                         | P6PLU1                              | P6PLU0                                  | 50,54          |
|         |          | Port 6 pull-up resistor ON/OFF control             |  |                                    |  |  |                                |                                     |   |                |
| X'3F47' | P7PLUD   | P7PLUD7  | P7PLUD6  | P7PLUD5                            | P7PLUD4                                    | P7PLUD3                                    | P7PLUD2                        | P7PLUD1                             | P7PLUD0                                 | 50,54          |
|         |          | Port 7 pull-up/pull-down resistor ON/OFF control   |  |                                    |  |  |                                |                                     |   |                |
| X'3F48' | P8PLU    | P8PLU7   | P8PLU6   | P8PLU5                             | P8PLU4                                     | P8PLU3                                     | P8PLU2                         | P8PLU1                              | P8PLU0                                  | 50,54          |
|         |          | Port 8 pull-up resistor ON/OFF control             |  |                                    |  |  |                                |                                     |   |                |
| X'3F4A' | PAPLUD   | PAPLUD7  | PAPLUD6  | PAPLUD5                            | PAPLUD4                                    | PAPLUD3                                    | PAPLUD2                        | PAPLUD1                             | PAPLUD0                                 | 50,54          |
|         |          | Port A pull-up/pull-down resistor ON/OFF control   |  |                                    |  |  |                                |                                     |   |                |
| X'3F4B' | FLOAT1   |  |  |                                    |  |  | P21M                           | PARDWN                              | P7RDWN                                  | 50,57          |
|         |          |  |  |                                    |  |  | Select P21 input mode          | Selects port A pull-up/pull-down    | Selects port 7 pull-up/pull-down        |                |
| X'3F4C' | FLOAT2   |  |  |                                    |  |  |                                | P7SYEVS2                            | P7SYEVS1                                | 50,57          |
|         |          |  |  |                                    |  |  |                                | Selects P7 synchronous output event |   |                |
| X'3F50' | SC0MD0   |  | SC0CE0   | SC0CE1                             | SC0DIR                                     | SC0STE                                     | SC0LNG2                        | SC0LNG1                             | SC0LNG0                                 | 146            |
|         |          |  | Set edges for input of received data and output of transmission data |                                    | Specifies first bit of transfer            | Selects synchronous serial start condition | Number of transfer bits        |                                     |   |                |
| X'3F51' | SC0MD1   |  |  | SC0CKM                             | SC0CK1                                     | SC0CK0                                     | SC0BRKF                        | SC0ERE                              | SC0TRI                                  | 147            |
|         |          |  |  | Selects 1/8th of frequency         | Selects clock source                       |  | Break status reception monitor | Error monitor                       | Transmit/receive interrupt request flag |                |
| X'3F52' | SC0MD2   |  |  | SC0BRKE                            | SC0FM1                                     | SC0FM0                                     | SC0PM1                         | SC0PM0                              | SC0NPE                                  | 148            |
|         |          |  |  | Controls break status transmission | Specifies frame mode                       |  | Specifies added bit            |                                     | Enables parity                          |                |
| X'3F53' | SC0MD3   |  |  | SC0IOM                             | SC0SBOM                                    | SC0SBTM                                    | SC0SBOS                        | SC0SBIS                             | SC0SBTS                                 | 149            |
|         |          |  |  | SB0/SBC0 pin connection            | Selects SBO0 pin format                    | Selects SBT0 pin format                    | Selects SBO0 pin function      | Controls SB0 input                  | Selects SBT0 pin function               |                |
| X'3F54' | SC0CTR   | SC0BSY   | SC0CMD   |                                    |  | SC0FEF                                     | SC0PEK                         | SC0ORE                              |   | 154            |
|         |          | Status of serial bus                               | Selects synchronous serial UART                                      |                                    |  | Detect framing errors                      | Detect parity errors           | Detect overrun errors               |   |                |
| X'3F55' | SC0TRB   | SC0TRB7  | SC0TRB6  | SC0TRB5                            | SC0TRB4                                    | SC0TRB3                                    | SC0TRB2                        | SC0TRB1                             | SC0TRB0                                 | 145            |
|         |          | Serial interface 0 transmit/receive shift register |  |                                    |  |  |                                |                                     |   |                |
| X'3F56' | SC0RXB   | SC0RXB7  | SC0RXB6  | SC0RXB5                            | SC0RXB4                                    | SC0RXB3                                    | SC0RXB2                        | SC0RXB1                             | SC0RXB0                                 | 145            |
|         |          | Serial interface 0 receive data buffer             |  |                                    |  |  |                                |                                     |   |                |
| X'3F57' | SC1MD0   | SC1BSY   | SC1CE0   | SC1CE1                             | SC1DIR                                     | SC1STE                                     | SC1LNG2                        | SC1LNG1                             | SC1LNG0                                 | 150            |
|         |          | Status of serial bus                               | Set edges for input of received data and output of transmission data |                                    | Specifies first bit of transfer            | Selects synchronous serial start condition | Number of transfer bits        |                                     |   |                |
| X'3F58' | SC1MD1   |  | SC1SBOM  | SC1SBTM                            | SC1SBOS                                    | SC1SBIS                                    | SC1SBTS                        | SC1CK1                              | SC1CK0                                  | 151            |
|         |          |  | Selects SBO1 pin format  | Selects SBT1 pin format            | Selects SBO1 pin function                  | Selects SB1 pin function                   | Selects SBT1 pin function      | Selects clock source                |   |                |
| X'3F59' | SC1TRB   | SC1TRB7  | SC1TRB6  | SC1TRB5                            | SC1TRB4                                    | SC1TRB3                                    | SC1TRB2                        | SC1TRB1                             | SC1TRB0                                 | 145            |
|         |          | Serial interface 1 transmit/receive shift register |  |                                    |  |  |                                |                                     |   |                |
| X'3F5A' | SC2MD0   | SC2CE0   | SC2CMD   | SC2DIR                             | SC2STE                                     | SC2LNG3                                    | SC2LNG2                        | SC2LNG1                             | SC2LNG0                                 | 152            |
|         |          | Set edges for input of received data               | Selects synchronous serial IIC                                       | Specifies first bit of transfer    | Selects synchronous serial start condition | Number of transfer bits                    |                                |                                     |   |                |
| X'3F5B' | SC2MD1   | SC2SBOM  | SC2SBTM  | SC2SBOS                            | SC2SBIS                                    | SC2SBTS                                    | SC2CK2                         | SC2CK1                              | SC2CK0                                  | 153            |
|         |          | Selects SBO2 pin format                            | Selects SBT2 pin format  | Selects SBO2 pin function          | Controls SB2 input                         | Selects SBT2 pin function                  | Selects clock source           |                                     |   |                |
| X'3F5C' | SC2CTR   | SC2BSY   | SC2SBOM  | SC2SPKF                            | SC2STKF                                    | SC2SPEN                                    | SC2STEN                        | SC2ACKS                             | SC2ACKO                                 | 155            |
|         |          | Status of serial bus                               | Connects SB2/SC2 pin   | Detects stop condition flag        | Detects start condition flag               | enables stop condition flag                | enables start condition flag   | ACK bit enable                      | ACK bit level                           |                |
| X'3F5D' | SC2TRB   | SC2TRB7  | SC2TRB6  | SC2TRB5                            | SC2TRB4                                    | SC2TRB3                                    | SC2TRB2                        | SC2TRB1                             | SC2TRB0                                 | 145            |
|         |          | Serial interface 2 transmit/receive shift register |  |                                    |  |  |                                |                                     |   |                |
| X'3F60' | TM0BC    | TM0BC7   | TM0BC6   | TM0BC5                             | TM0BC4                                     | TM0BC3                                     | TM0BC2                         | TM0BC1                              | TM0BC0                                  | 107            |
|         |          | Binary counter 0                                   |  |                                    |  |  |                                |                                     |   |                |

Summary of Special Function Registers (4/6)

| Address | Register | Bit Symbol                             |  |                   |                        |  |                      |                      |                                      | Reference Page |     |
|---------|----------|--|--|-------------------|------------------------|--|----------------------|----------------------|--------------------------------------|----------------|-----|
|         |          | Bit 7                                  | Bit 6                                    | Bit 5             | Bit 4                  | Bit 3                                      | Bit 2                | Bit 1                | Bit 0                                |                |     |
| X'3F61' | TM1BC    | TM1BC7                                 | TM1BC6                                   | TM1BC5            | TM1BC4                 | TM1BC3                                     | TM1BC2               | TM1BC1               | TM1BC0                               | 107            |     |
|         |          | Binary counter 1                       |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F62' | TM2BC    | TM2BC7                                 | TM2BC6                                   | TM2BC5            | TM2BC4                 | TM2BC3                                     | TM2BC2               | TM2BC1               | TM2BC0                               | 108            |     |
|         |          | Binary counter 2                       |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F63' | TM3BC    | TM3BC7                                 | TM3BC6                                   | TM3BC5            | TM3BC4                 | TM3BC3                                     | TM3BC2               | TM3BC1               | TM3BC0                               | 108            |     |
|         |          | Binary counter 3                       |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F64' | TM4BCL   | TM4BCL7                                | TM4BCL6                                  | TM4BCL5           | TM4BCL4                | TM4BCL3                                    | TM4BCL2              | TM4BCL1              | TM4BCL0                              | 109            |     |
|         |          | Binary counter 4 (lower 8 bits)        |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F65' | TM4BCH   | TM4BCH7                                | TM4BCH6                                  | TM4BCH5           | TM4BCH4                | TM4BCH3                                    | TM4BCH2              | TM4BCH1              | TM4BCH0                              | 109            |     |
|         |          | Binary counter 4 (upper 8 bits)        |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F66' | TM4ICL   | TM4ICL7                                | TM4ICL6                                  | TM4ICL5           | TM4ICL4                | TM4ICL3                                    | TM4ICL2              | TM4ICL1              | TM4ICL0                              | 110            |     |
|         |          | Input capture register (lower 8 bits)  |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F67' | TM4ICH   | TM4ICH7                                | TM4ICH6                                  | TM4ICH5           | TM4ICH4                | TM4ICH3                                    | TM4ICH2              | TM4ICH1              | TM4ICH0                              | 110            |     |
|         |          | Input capture register (upper 8 bits)  |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F68' | TM5BC    | TM5BC7                                 | TM5BC6                                   | TM5BC5            | TM5BC4                 | TM5BC3                                     | TM5BC2               | TM5BC1               | TM5BC0                               | 110            |     |
|         |          | Binary counter 5                       |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F70' | TM0OC    | TM0OC7                                 | TM0OC6                                   | TM0OC5            | TM0OC4                 | TM0OC3                                     | TM0OC2               | TM0OC1               | TM0OC0                               | 107            |     |
|         |          | Compare register 0                     |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F71' | TM1OC    | TM1OC7                                 | TM1OC6                                   | TM1OC5            | TM1OC4                 | TM1OC3                                     | TM1OC2               | TM1OC1               | TM1OC0                               | 107            |     |
|         |          | Compare register 1                     |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F72' | TM2OC    | TM2OC7                                 | TM2OC6                                   | TM2OC5            | TM2OC4                 | TM2OC3                                     | TM2OC2               | TM2OC1               | TM2OC0                               | 108            |     |
|         |          | Compare register 2                     |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F73' | TM3OC    | TM3OC7                                 | TM3OC6                                   | TM3OC5            | TM3OC4                 | TM3OC3                                     | TM3OC2               | TM3OC1               | TM3OC0                               | 108            |     |
|         |          | Compare register 3                     |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F74' | TM4OCL   | TM4OCL7                                | TM4OCL6                                  | TM4OCL5           | TM4OCL4                | TM4OCL3                                    | TM4OCL2              | TM4OCL1              | TM4OCL0                              | 109            |     |
|         |          | Compare register 4 (lower 8 bits)      |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F75' | TM4OCH   | TM4OCH7                                | TM4OCH6                                  | TM4OCH5           | TM4OCH4                | TM4OCH3                                    | TM4OCH2              | TM4OCH1              | TM4OCH0                              | 109            |     |
|         |          | Compare register 4 (upper 8 bits)      |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F78' | TM5OC    | TM5OC7                                 | TM5OC6                                   | TM5OC5            | TM5OC4                 | TM5OC3                                     | TM5OC2               | TM5OC1               | TM5OC0                               | 110            |     |
|         |          | Compare register 5                     |  |                   |                        |  |                      |                      |                                      |                |     |
| X'3F80' | TM0MD    |  |  |                   | TM0EN                  | TM0PWN                                     | TM0CK2               | TM0CK1               | TM0CK0                               | 111            |     |
|         |          |  |  |                   | Controls counting      | Selects operation mode                     | Selects clock source |                      |                                      |                |     |
| X'3F81' | TM1MD    |  |  |                   | TM1EN                  | TM1PWM                                     | TM1CK2               | TM1CK1               | TM1CK0                               | 112            |     |
|         |          |  |  |                   | Controls counting      | Selects P11 output during TM0PWN operation | Selects clock source |                      |                                      |                |     |
| X'3F82' | TM2MD    |  |  |                   | TM2EN                  | TM2PWM                                     | TM2CK2               | TM2CK1               | TM2CK0                               | 113            |     |
|         |          |  |  |                   | Controls counting      | Selects operation mode                     | Selects clock source |                      |                                      |                |     |
| X'3F83' | TM3MD    |  |  |                   | TM3EN                  | TM3PWM                                     | TM3CK2               | TM3CK1               | TM3CK0                               | 114            |     |
|         |          |  |  |                   | Controls counting      | Selects P13 output during TM2PWN operation | Selects clock source |                      |                                      |                |     |
| X'3F84' | TM4MD    |  |  | TM4EN             | TM4PWM                 | T4ICTS1                                    | T4ICTS0              | TM4CK2               | TM4CK1                               | TM4CK0         | 115 |
|         |          |  |  | Controls counting | Selects operation mode | Selects input capture trigger              |                      | Selects clock source |                                      |                |     |
| X'3F88' | TM5MD    | TM5CLRS                                | TM5IR2                                   | TM5IR1            | TM5IR0                 | TM5CK3                                     | TM5CK2               | TM5CK1               | TM5CK0                               | 116            |     |
|         |          | Selects binary counter 5 to be cleared | Selects time base timer interrupt period |                   |                        | Timer 5 Selects clock source               |                      |                      | Selects time base timer clock source |                |     |

Summary of Special Function Registers (5/6)

| Address | Register       | Bit Symbol   |                              |  |   |  |  |   |  | Reference Page |
|---------|----------------|--|------------------------------|--|---|--|--|---|--|----------------|
|         |                | Bit 7  | Bit 6                        | Bit 5  | Bit 4                                   | Bit 3  | Bit 2  | Bit 1   | Bit 0  |                |
| X'3F89' | RMCTR          |  |                              |  | TM0RM<br>Selects P10 output             | RMOEN<br>Enables remote control carrier output | Must be set to "0"                                   | RMDTY0<br>Selects duty of remote control carrier output | RMBTMS<br>Selects base timer of remote control carrier | 119            |
| X'3F8A' | NFCTR          |  |                              | NF1CKS1<br>Selects IRQ1 noise filter sampling period | NF1CKS0                                 | NF1EN<br>Sets IRQ1 noise filter operation      | NF0CKS1<br>Selects IRQ0 noise filter sampling period | NF0CKS0   | NF0EN<br>Sets IRQ0 noise filter operation              | 171            |
| X'3F90' | ANCTR0         | ANSH1<br>Sets sample and hold time                         | ANSH0                        | ANCK1<br>Selects A/D conversion clock                | ANCK0                                   | ANLADE<br>Controls A/D ladder resistors        | ANCHS2<br>Selects analog input                       | ANCHS1  | ANCHS0   | 161            |
| X'3F91' | ANCTR1         | ANST<br>A/D conversion status                              |                              |  |   |  |  |   |  | 162            |
| X'3F92' | ANBUF0         | ANBUF07<br>A/D buffer 0                                    | ANBUF06                      |  |   |  |  |   |  | 163            |
| X'3F93' | ANBUF1         | ANBUF17<br>A/D buffer 1                                    | ANBUF16                      | ANBUF15  | ANBUF14                                 | ANBUF13  | ANBUF12  | ANBUF11   | ANBUF10  | 163            |
| X'3FA0' | ATMD           | ATEXT<br>Selects ATC external connection                   | ATEN<br>Enables ATC transfer | ATWID<br>Selects ATC transfer unit                   | ATDIR<br>Selects ATC transfer direction | ATINC<br>Selects ATTAP mode                    | ATIR2<br>Transfer activation interrupt selection     | ATIR1   | ATIR0  | 179            |
| X'3FA1' | ATCNT          | ATCNT7   | ATCNT6                       | ATCNT5   | ATCNT4                                  | ATCNT3   | ATCNT2   | ATCNT1  | ATCNT0   | 180            |
| X'3FA2' | ATTAPL         | ATTAP7   | ATTAP6                       | ATTAP5   | ATTAP4                                  | ATTAP3   | ATTAP2   | ATTAP1  | ATTAP0   | 181            |
| X'3FA3' | ATTAPH         | ATTAP15  | ATTAP14                      | ATTAP13  | ATTAP12                                 | ATTAP11  | ATTAP10  | ATTAP9  | ATTAP8   | 181            |
| X'3FA4' | ATIAP          | ATIAP7   | ATIAP6                       | ATIAP5   | ATIAP4                                  | ATIAP3   | ATIAP2   | ATIAP1  | ATIAP0   | 181            |
| X'3FE0' | Disable to use |  |                              |  |   |  |  |   |  | —              |
| X'3FE1' | NMICH          |  |                              |  |   |  | WDIR<br>Watchdog interrupt request flag              |   |  | 39             |
| X'3FE2' | IRQ0ICR        | IRQ0LV1<br>Interrupt level flag for external interrupt     | IRQ0LV0                      | REDG0<br>External interrupt valid edge flag          |   |  | IRQ0IE<br>Interrupt enable flag                      | IRQ0IR<br>Interrupt request flag                        |  | 39             |
| X'3FE3' | IRQ1ICR        | IRQ1LV1<br>Interrupt level flag for external interrupt     | IRQ1LV0                      | REDG1<br>External interrupt valid edge flag          |   |  | IRQ1IE<br>Interrupt enable flag                      | IRQ1IR<br>Interrupt request flag                        |  | 39             |
| X'3FE4' | TM0ICR         | TM0LV1<br>Interrupt level flag for timer 0 interrupt       | TM0LV0                       |  |   |  | TM0IE<br>Interrupt enable flag                       | TM0IR<br>Interrupt request flag                         |  | 40             |
| X'3FE5' | TM1ICR         | TM1LV1<br>Interrupt level flag for timer 1 interrupt       | TM1LV0                       |  |   |  | TM1IE<br>Interrupt enable flag                       | TM1IR<br>Interrupt request flag                         |  | 40             |
| X'3FE6' | TM2ICR         | TM2LV1<br>Interrupt level flag for timer 2 interrupt       | TM2LV0                       |  |   |  | TM2IE<br>Interrupt enable flag                       | TM2IR<br>Interrupt request flag                         |  | 40             |
| X'3FE7' | TBICR          | TBLV1<br>Interrupt level flag for time base interrupt      | TBLV0                        |  |   |  | TBIE<br>Interrupt enable flag                        | TBIR<br>Interrupt request flag                          |  | 40             |
| X'3FE8' | SC0ICR         | SC0LV1<br>Interrupt level flag for serial 0 interrupt      | SC0LV0                       |  |   |  | SC0IE<br>Interrupt enable flag                       | SC0IR<br>Interrupt request flag                         |  | 40             |
| X'3FE9' | ATCICR         | ATCLV1<br>Interrupt level flag for data transfer interrupt | ATCLV0                       |  |   |  | ATC<br>Interrupt enable flag                         | ATC<br>Interrupt request flag                           |  | 40             |



## Appendix: Overview of MN101CP01D Internal EPROM

The MN101CP01D microcomputer replaces the mask ROM of the MN101C01\* with an electronically programmable 64-KB EPROM.

Because the MN101CP01DAQ is sealed in plastic, once data is written to the internal PROM it cannot be erased. Because the MN101CP01DAQ is sealed in a ceramic package that has a window, written data can be erased by illumination with ultraviolet light.

Both the plastic and ceramic packages use a 80-pin flat package.

Setting the MN101CP01D to EPROM mode, halts microcomputer functions, and the internal EPROM can be programmed. Refer to the EPROM mode pin diagram in figure 1.

The specifications for writing to the internal EPROM are the same as for a general-purpose 1-megabit EPROM ( $V_{pp}=12.5V$ ,  $t_{pw}=0.2ms$ ). Therefore, by replacing the MN101CP01D's 80-pin socket with a special 32-pin MN101CP01D socket adapter (supplied by Panasonic) having the same configuration as a normal EPROM, a general-purpose EPROM writer can be used to perform read and write operations.

Specific instructions for writing to the internal EPROM with a Panasonic writer are provided in section (2). The internal EPROM can be used to set high-speed or low-speed oscillation start control and the runaway detection period for the MN101CP01D. Details are shown in (3). Precautions are listed in (4). Instructions for erasing data from a window packaged part are provided in (5). The difference between the MN101CP01D (internal EPROM version) and the MN101C01D (mask ROM version) is shown in (6).

## (1) Internal EPROM Considerations

- Write #FF data to the #00000~#03FFF memory area.  
Use the #04000~#13FFF (64K) memory area as a continuous area.
- If the EPROM is to be programmed with a PROM writer, be sure to verify that the socket adapter and product are properly mounted. If not properly mounted, the product may be damaged.
- The MN101CP01D programming voltage is specified as 12.5V. Therefore, writing a program with a 21V system specification will damage the product. If a PROM writer will be used for programming, set the specifications for a general-purpose 1-megabit EPROM ( $V_{pp}=12.5V$ ,  $tpw=0.2ms$ ).



This product does not contain an ID code such as "Silicon Signature" or "Intelligent Identifier" for the writer's auto-device selection command. Consequently, the auto-device selection command should never be used with this product, as the device might be damaged.

---

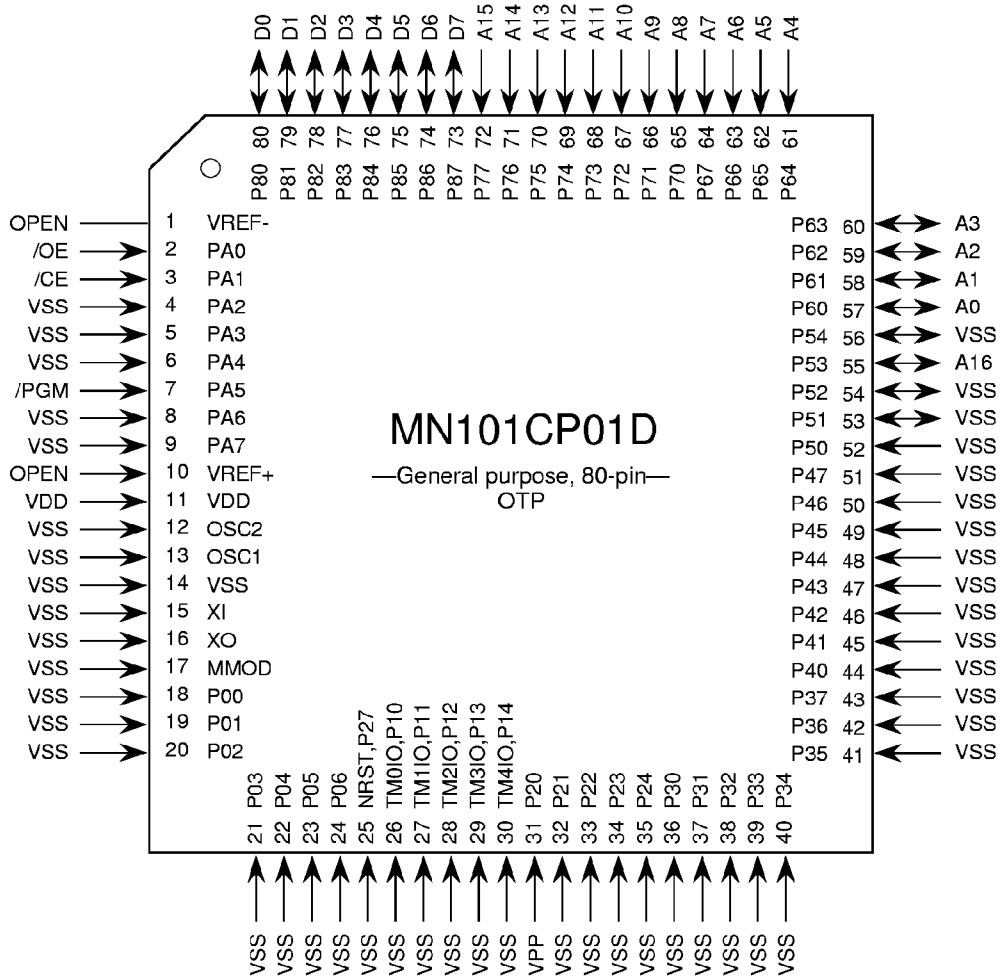



Figure 1 MN101CP01D EPROM Write Adapter Pin Diagram

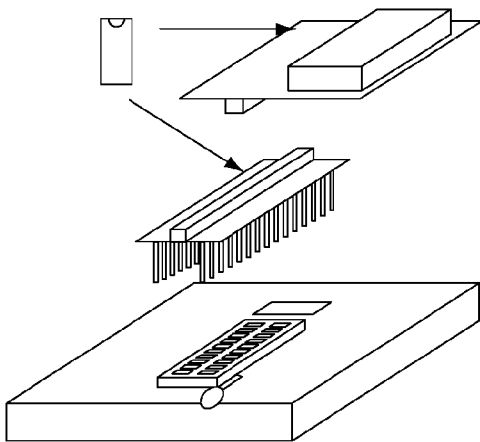
## (2) Writing to the Internal EPROM

### • When using the PanaXIPW writer

OTP adapter setup method

Align the  and connect the OTP and general-purpose sections.

Align the  and the IPW ROM insertion direction and insert.



IPW settings (after normal IPW activation)


| Priority                                      |                        |
|---|------------------------|
| Device selection (F1)                         |                        |
| Type  | Select EPROM.          |
| Manufacturer name selection                   | Select HITACHI.        |
| Device name selection                         | Select HN27C101AG.     |
| Write sequence                                | Select 1-Byte Program. |
| After selecting, implement.                   |                        |
| -----   |                        |
| Loading file: Load (F9)                       |                        |
| File name                                     |                        |
| Start address                                 | ****                   |
| -----   |                        |
| Write: Write (F3)                             |                        |
| ROM start address                             | 00004000               |
| ROM end address                               | 00013FFF               |
| Memory start address                          | 00004000               |
| Erase check selection                         | Perform erase check.   |
| After selecting, perform the write operation. |                        |
| -----   |                        |
| An additional method.                         |                        |
| DEVICE selection (F1)                         |                        |
| Type  | Select OTCPU.          |
| Manufacturer name selection                   | *****                  |
| Device name selection                         | Select MN101CPXXX.     |
| Write sequence                                | Select 1-Byte Program. |
| After selecting, implement.                   |                        |

If a write operation is to be performed, use the same settings as above.

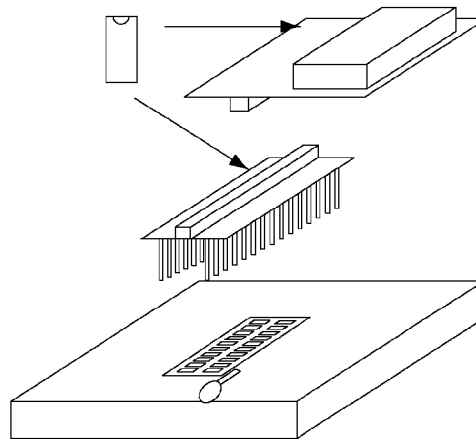


• When using the PanaXEPP writer

OTP adapter setup method

Align the  and connect the OTP and general-purpose sections.

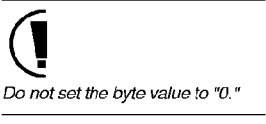
Align the  and the EPP ROM insertion direction and insert.



EPP settings (after normal EPP activation)

- |                         |                                    |
|-------------------------|------------------------------------|
| Menu screen             | 1. Select DEVICE&MODE setup screen |
|                         | ↓                                  |
| Device selection screen | 6. Select 1 MB                     |
|                         | ↓                                  |
| Mode selection screen   | 7. Select HITACHI quick            |
|                         | ↓                                  |
|                         | Return to main menu                |
|                         | ↓                                  |
| Menu screen             | 2. Select write setup screen       |

File Name: user file name  
 ROM Start address: 4000 or 0  
 File Start address: 4000 or 0  
 Byte: 10000 or actual ROM size



After setting up, perform the write operation.

### (3) EPROM option bits

The MN101CP01D can use bits 0~2 of address #1FF02 of the internal EPROM to set high-speed or low-speed oscillation start control and the runaway detection (watch-dog) period.

The address of this option is in an area that does not exist in the ROM version.

The option bit specifications are listed in table 1.

Table 1 Option Bit Specifications

| Option Bit   | Address                            | Setting Item             | Program Contents   |
|--------------|------------------------------------|--------------------------|--|
| OPT0         | x'1FF02' (bit0)                    | Oscillation mode         | 1: Type A<br>0: Type B   |
| OPT1<br>OPT2 | x'1FF02' (bit1)<br>x'1FF02' (bit2) | Runaway detection period | bit1 bit2<br>1 1: $f_s/2^{20}$<br>0 1: $f_s/2^{18}$<br>0 0: $f_s/2^{16}$ |

Type A: In the NORMAL mode, operation begins from the reset cycle.

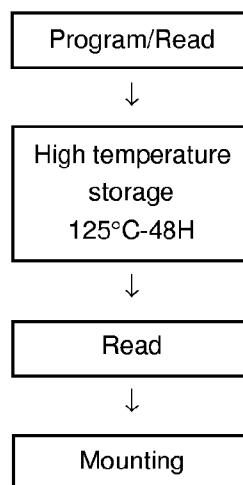
Type B: In the SLOW mode, operation begins from the reset cycle.



*Options are set in the area of #1FF00~#1FFFF. With the exception of the 3 option bits, set the data to "1". Verify the settings to make sure there are no errors.*

#### (4) Cautions

- The MN101CP01D differs from the MN101C01\* in some of its electrical characteristics. The user should be aware of these differences.
- To prevent data from being erased by ultraviolet light after a program is written, affix seals impermeable to UV rays to the glass sections at the top and side sections of the CPU.
- From the time after a program is written until just before mounting, storage at a high temperature is recommended.



- Due to device characteristics of the OTP version, a writing test cannot be performed on all bits. Therefore, storage of the written data cannot be fully guaranteed in some cases.
- Verify that VCC power supply (6V) is connected before applying the VPP power supply (12.5V). Disconnect the VPP supply before disconnecting the VCC supply.
- VPP should never exceed 13.5V including overshoot.
- If a device is removed while a VPP of +12.5V is applied, device reliability may be damaged.
- At CE=VIL, do not change VPP from VIL to +12.5V or from +12.5V to VIL.

## (5) Erasing data in windowed packages

In an internal EPROM with windowed packaging, data is erased ("0"→"1") when UV light at 2537 Å permeates the window to irradiate the chip.

The recommended exposure is 10W•s/cm<sup>2</sup>. This coverage can be achieved by using a commercial UV lamp positioned 2~3 cm above the package for 15~20 minutes (when the illumination intensity of the package surface is 12000μW/cm<sup>2</sup>). Remove any filters attached to the lamp. By installing a mirrored reflector plate in the lamp, illumination intensity will increase by a factor of 1.4~1.8, decreasing the erasure time.

If the window becomes dirty with oil, adhesive, etc., UV light permeability will decrease, causing the erasure time to increase considerably. If this happens, clean with alcohol or another solvent that will not harm the package. The recommended above provides sufficient leeway, with several times the amount of time it takes to erase all the bits. However, this value will reliably erase data over all temperature and voltage ranges, and should not be altered. The level of illumination should be regularly checked and the lamp operation verified.

Erasure begins when the EPROM is exposed to light with a wavelength shorter than 4000 Å. Since fluorescent light and sunlight have wavelengths in this range, exposure to these light sources for extended periods of time could cause inadvertent erasure. To prevent this, cover the window with an opaque label.

Data is not erased at wavelengths. However, because of typical semiconductor characteristics, the circuit may malfunction if the chip is exposed to an extremely high illumination intensity. The chip will operate normally if this exposure is stopped. However, for areas where it is continuous, take necessary precautions.

### (6) MN101CP01D characteristics

The MN101C01D (mask ROM version) and the MN101CP01D (internal EPROM version), both 80-pin, 8-bit microcomputers with internal LCD drivers, have the following differences.

|   | MN101C01D (ROM version)   | MN101CP01D (EPROM version)   |
|---|---|--|
| ROM size  | 65336 bytes   | <u>65336 bytes</u>   |
| RAM size  | 2048 bytes  | <u>2048 bytes</u>  |
| Ambient operating temp.   | -40~85°C  | <u>-20~70°C</u>  |
| Operating voltage   | 4.5~5.5V<br>(for 0.1μS/20MHz)<br>2.7~5.5V<br>(for 0.25μS/8MHz)<br>2.0~5.5V<br>(for 1.00μS/2MHz)   | 4.5~5.5V<br>(for 0.1μS/20MHz)<br>2.7~5.5V<br>(for 0.25μS/8MHz)<br><u>2.7~5.5V</u><br>(for 1.00μS/2MHz) |
| Pin DC characteristics  | Output current, input current, input determination level<br>Both ROM and EPROM versions were designed with the same product specifications. |  |
| Pull-up resistor connection   | Pull-up via software  | Pull-up via software   |
| Options for high/low speed oscillation start control, run-away detection period setting | Mask option   | <u>EPROM option*</u>   |

\*EPROM data is used as the option data.

There are no other functional differences.

**MN101C01D**  
**LSI User's Manual**

JANUARY,1997 Version 2.1

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c Matsushita Electronics Corporation