❑ MN101D01C / D / E / F / G

Type	MN101D01C / D / E / F / G
ROM (x8-bit)	48K / 64K / 80K / 96K / 128K
RAM (x8-bit)	1536 / 2048 / 2304 / 2560 / 3072
Minimum Instruction Execution Time	With Main Clock operated **0.1397 µs (at 4.0 to 5.5V, 14.32MHz)** **0.1128 µs (at 4.0 to 5.5V, 17.73MHz)** When Sub-clock operated **143 µs (at 2.7 to 5.5V fixed to 14.32MHz internal division)** **122 µs (at 2.7 to 5.5V, 32.768MHz)**
Interrupts	• RESET • Runaway • External 0, 1, 2, 3, 4/key input (P50 to 54) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Capstan FG • Control • HSW • Cylinder FG • VSYNC • Continuous Synchronous Output • OSD • XDS • Serial 0 • Serial 1 • Serial 2 • A/D (common with PWM 14 reference frequency)

Timer Counter

Timer Counter 0: 16-bit x 1 (Timer Output, Clock Function [max. 2 s])
Clock Source.....1/2, 1/4, 1/8, 1/16 of System Clock, 1/512 of XI Oscillation Clock or OSC Oscillation Clock
Interrupt Source.....Overflow of Timer Counter 0

Timer Counter 1: 16-bit x 1 (Timer Output, linear Timer Counter Function)
Clock Source.....1/2, 1/4, 1/8, 1/16, CTL Signal of System Clock
Interrupt Source.....Overflow of Timer Counter 1

Timer Counter 2: 16-bit x 1 (Timer Output, Input Capture (DCTL Specified Edge), Duty Judgment of DCTL Signal)
Clock Source.....1/2, 1/4, 1/8, 1/12, 1/16, 1/24 of System Clock
Interrupt Source.....Overflow of Timer Counter 2, Input of DCTL Specified Edge, Underflow of Timer 2 Shift Register 4-bit Counter, Coincidence of Timer 2 Shift Register with Timer 2 Shift Register Compare Register

Timer Counter 3: 16-bit x 1 (Timer Output, Detection of Serial Indexing, Generation of Remote Control Output Carrier Frequency)
Clock Source.....1/2, 1/4, 1/8, 1/16 of System Clock
Interrupt Source.....Overflow of Timer Counter 3

Timer Counter 4: 16-bit x 1 (Timer Output, Event Count (P15 Input), Generation of Serial Transmission Clock)
Clock Source.....1/8, 1/16 of System Clock, External Clock Input
Interrupt Source.....Overflow of Timer Counter 4, Coincidence of Timer Counter 4 with OCR4

Timer Counter 5: 17-bit x 1 (Watchdog, Stable Oscillation Waiting Function)
Clock Source.....System Clock
Watchdog Interrupt Source ....$1/2^{13}$, $1/2^{16}$ of Timer Counter 5
Clear by Stable Oscillation...After 256 Counts by Timer Counter 5 (2^{18} Counts of OSC Oscillation Clock)

Timer Counter 6: 16-bit x 1 (Clock Function [max. 2 s])
Clock Source.....1/512 of OSC Oscillation Clock, XI Oscillation Clock, 1/4, 1/8, 1/64, 1/128 of System Clock
Interrupt Source.....$1/2^{13}$, $1/2^{14}$, $1/2^{15}$, Overflow of Timer Counter 6

Serial Interface

Serial 0: 8-bit x 1 (Synchronous Type/Start-stop Synchronous Type) (Transfer Direction of MSB/LSB Selectable)
Synchronous Type Clock Source...1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of System Clock, 2-division timer 4 output, $\overline{SBT0}$ pin input
Clock for UART .....8-division of Above Clock, 2-division Timer 4 Output, $\overline{SBT0}$ Pin Input

Serial 1: 8-bit x 1 (Synchronous Type/Remote Control Transmission/Simple Remote Control Receive) (Transfer Direction of MSB/LSB Selectable, Start Condition Function)
Clock Source.....1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of System Clock, 2-division Timer 4 Output, $\overline{SBT1}$ Pin Input
Remote Control Clock....2-division Timer Output

Serial 2: 8-bit x 1 (Sync/I²C) (Master Transmission/Reception, Slave Transmission/Reception)
Clock Source.....1/72, 1/80, 1/84, 1/96, 1/102, 1/112, 1/128, 1/144, 1/160, 1/168, 1/192, 1/224, 1/256, 1/320, SCK Pin Input of System Clock

OSD

Accommodation with Menu or Super Impose Display
Applicable Broadcasting System: NTSC, PAL, PAL-M, PAL-N

Screen Configuration	: 24 Characters x 2n Rows (n=1 to 6)
Character Type	: Max. 512 Character Types (Variable)
Character Size	: 12x18 Dots
Enlarged Characters	: Each x 2, x 3 or x 4 Settings in Horizontal and Vertical
Character Interpolation	: None
Background Color	: 8 Gradations Settable (Settable in The Row Unit at Menu Display)
Background Intensity	: 8 Gradations Settable in The Row Unit
Character Color	: White
Character Intensity	: 8 Gradations Settable in The Row Unit
Frame Function	: 1-Dot frame in 4 or 8 Directions
Frame Intensity	: 4 Gradations Settable in The Row Unit
Box Shade Function	: Settable in The Character Unit (Only at Composite Output with 128 Character Types or More)
Blinking	: None (Covered by Software)
Inverted Character	: Settable in The Character Unit
Halftone	: Settable in The Row Unit in 2 Intensity Gradations (Setting in The Row Unit)
Input	: Composite Video Signal Input (Output Level: 1 Vpp/2 Vpp)
Clamp Method	: Sync Chip Clamp, Clamp Level in 4 Levels
Output	: Composite Video Output : Digital Output (6 pins) 8 Character and Background Colors Each Settable at Digital Output.
Measure Against Image Fluctuation	: Built-in AFC Circuit
Sync Signal Detection Function	: Detection Functions for Horizontal and Vertical Sync Signals (Integral System) With Horizontal Sync Signal Interpolation Function

XDS

Built-in U.S. Closed Caption Data Slicer (Optional 2 Line Data can be Extracted.)

ROM Correction

Correcting Address Designation: Up to 2 Addresses Possible
Correction Method: Correction Program Being Saved in Internal RAM

I/O Pins

I/O	73	• Common use: 73 ports 0, 1, 2, 4, 5, 6, 7, A, B, by-bit
Input	4	• Common use: 4

A/D

8-bit x 12ch (Without S/H)

PWM

13-bit x 2ch (at Repetition Cycle 572µs, 14.32MHz),
10-bit x 2ch (at Repetition Cycle 71.5µs, 14.32MHz), 14-bit x 1ch (at Repetition Cycle 1144µs, 14.32MHz)

ICR

18-bit x 6ch

OCR

16-bit x 7ch, 8-bit x 1ch

Special Ports

Buzzer Output, 3-State Output (PTO) VLP Pin, Synchronous Output: 7, 3-State Synchronous Output: 4, Remote Control Receive, CTL Amp, Built-in FG Amp,
Output of 1/2 OSC Oscillation Clock (2Vpp), Output of 1/4 OSC Oscillation Clock (1 Vpp)

Notes

VISS/VASS Detection Function

Package

QFP-100-P-1818

Electrical Characteristics

Supply Current

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Operating Supply Current	IDD1	14.32MHz operation without load		30	60	mA
	IDD2	14.32MHz oscillation SLOW operation without load		2	5	mA
	IDD3	Stop of 14.32MHz oscillation 32kHz oscillation operation without load		0.1	1.0	mA
Supply Current at STOP	IDSP	Stop of oscillation without load			20	µA
Supply Current at HALT	IDHT0	14.32MHz oscillation without load		5	15	mA
	IDHT1	Stop of 14.32MHz oscillation 32kHz oscillation operation without load		5	20	µA

(Ta=25±2°C, VDD=5.0V, VSS=0V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Conversion Relative Error	ΔNLad				±3	LSB
A/D Conversion Time	Tad	fosc = 14.32Mhz		8		µs
Analog Input Voltage			0.5		4.5	V

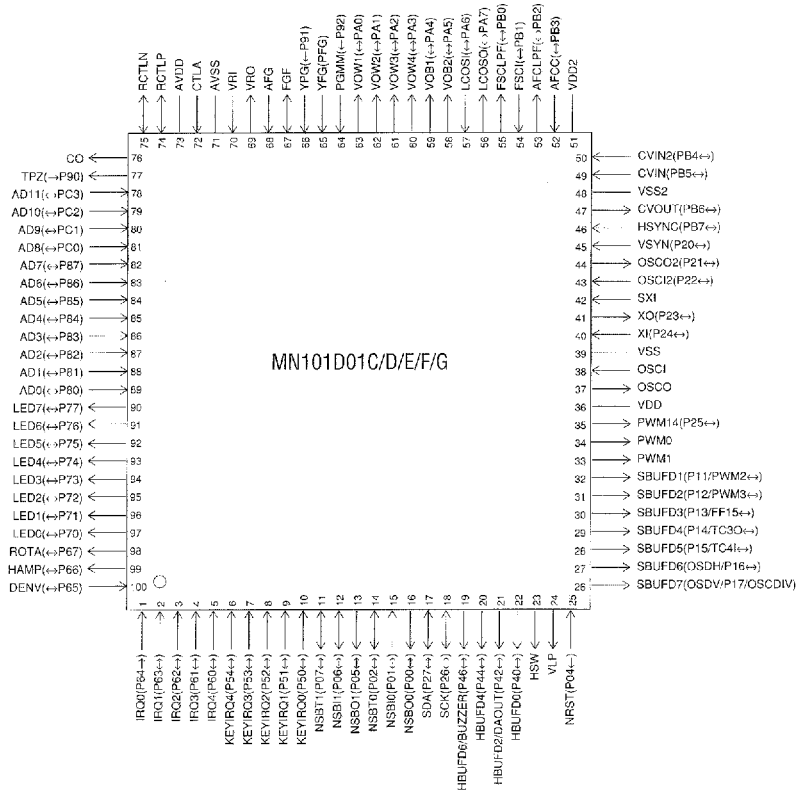
(Ta= 25±2°C, VDD=5.0V, VSS=0V)

Support Tool

In-Circuit Emulator PX-ICE1880-2 + PX-PRB67508

EPROM built-in Type Use MN101DP01G [ES (Engineering available)].

Pin Assignment



QFP100-P-1818B