MN101E31 Series

8-bit Single-chip Microcontroller

■ Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. The MN101E31 series have an internal 128 KB/64 KB (maximum) of ROM and 6 KB/4 KB(maximum) of RAM. Peripheral functions include 6 external interrupts, 23 internal interrupts including NMI, 9 timer counters, 5 sets of serial interfaces, A/D converter, LCD driver, watchdog timer, 1 set of automatic data transfer, synchronous output function and buzzer output. The configuration of this microcomputer is well suited for application as a system controller in camera, timer selector for VCR, CD player, or minicomponent.

With three oscillation system (high frequency : max. 10 MHz / low frequency : 32.768 kHz and PLL : frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high frequency input (high speed mode), PLL input (PLL mode), or to low frequency input (low speed mode).
The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software. High speed mode has the normal mode which is based on 2-cycle clock (fpll/2) and the double speed mode which is based on the not-devided clock with fpll.

A machine cycle (min. instructions execution) in the normal mode is 200 ns when fosc is 10 MHz (at the time that PLL is not used). A machine cycle in the double speed mode is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).The package is 80-pin, LQFP.

■ Product Summary

This manual describes the following models of the MN101E31 series. These products have identical functions. Please note that mainly dealed here is MN101E31G.

Model	ROM Size	RAM Size	Classification	Package
MN101E31G	128 KB	6 KB	Mask ROM version	LQFP080-P-1414A
MN101E31D	64 KB	4 KB		
MN101E31A	32 KB	2 KB		
MN101EF31G	128 KB + 4 KB	6 KB	Flash EEPROM version	
MN101EF31D	64 KB + 8 KB	4 KB		

■ Features

- ROM Capacity
  128 / 64 / 32 Kbyte (MN101EF31G: 128 Kbyte + 4 Kbyte, MN101EF31D: 64 Kbyte + 8 Kbyte)

- RAM Capacity
  6 / 4 / 2 Kbyte

- Package
  80pin LQFP (14 mm square, 0.65 mm pitch)

- Machine Cycle
  High speed mode
  0.10 µs / 10 MHz (2.2 V to 5.5 V) (MN101EF31D: 2.7 V to 5.5 V)
  PLL mode
  0.05 µs / 20 MHz (2.2 V to 5.5 V) (MN101EF31D: 2.7 V to 5.5 V)
  Low speed mode
  62.5 µs / 32 kHz (2.2 V to 5.5 V) (MN101EF31D: 2.7 V to 5.5 V)

- Clock Gear
  Operation speed of system clock is variable by changing the frequency.

- Multiplied Clock
  High-speed frequency clock (fosc) can be multiplied by 2, 3, 4, 5, 6, 8 and 10.

- Memory bank
  Data memory space is expanded by the bank system.
  Bank for the source address/Bank for the destination address.

- ROM correction
  Correcting address designation : up to 7 addresses possible

- Operating Mode
  NORMAL mode (High speed mode)
  PLL mode
  SLOW mode (Low speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)

- Operating Voltage
  2.2 V to 5.5 V (MN101EF31D: 2.7 V to 5.5 V)

- Operating Temperature
  –40°C to +85°C

■ Features (continued)

- Interrupt: 29 levels

<Watchdog timer>

NMI-Watchdog timer overflow

<Timer interrupts>

TM0IRQ-Timer 0 interrupt (8-bit timer)
TM1IRQ-Timer 1 interrupt (8-bit timer)
TM2IRQ-Timer 2 interrupt (8-bit timer)
TM3IRQ-Timer 3 interrupt (8-bit timer)
TM4IRQ-Timer 4 interrupt (8-bit timer)
TM6IRQ-Timer 6 interrupt (8-bit timer)
TBIRQ-Clock timer interrupt
TM7IRQ-Timer 7 interrupt (16-bit timer)
T7OC2IRQ- Timer 7 interrupt (16-bit timer)
TM8IRQ-Timer 8 interrupt (16-bit timer)
T8OC2IRQ- Timer 8 interrupt (16-bit timer)

<Serial interrupts>

SC0TIRQ-Serial interface 0 interrupt (UART transmission, synchronous)
SC0RIRQ-Serial interface 0 interrupt (UART reception) (Peripheral function group interrupt)
SC1TIRQ-Serial interface 1 interrupt (UART transmission, synchronous)
SC1RIRQ-Serial interface 1 interrupt (UART reception) (Peripheral function group interrupt)
SC2TIRQ-Serial interface 2 interrupt (UART transmission, synchronous)
SC2RIRQ-Serial interface 2 interrupt (UART reception)
SC4TIRQ- Serial interface 4 interrupt (synchronous)
SC4SIRQ- Serial interface 4 interrupt (Multi master IIC, Stop condition) (Peripheral function group interrupt)
SC5TIRQ- Serial interface 5 interrupt (Slave IIC) (Peripheral function group interrupt)

<A/D conversion end>

ADIRQ-AD conversion end

<Automatic Transfer Controller interrupts>

ATC1IRQ (Peripheral function group interrupt)

<External interrupts> Edge selectable

IRQ0:External interrupt (AC zero-cross detector, With/Without noise filter)
IRQ1:External interrupt (AC zero-cross detector, With/Without noise filter)
IRQ2:External interrupt (Both edges interrupt)
IRQ3:External interrupt (Both edges interrupt)
IRQ4:External interrupt (Both edges interrupt)
IRQ5:External interrupt (Key scan interrupt only)

■ Features (continued)

- Timer Counter: 10 timers All timer counters generate interrupt (9 can be operated independently)

8-bit timer for general use : 5 sets
8-bit free-running timer : 1 set
Time base timer : 1 set
16-bit timer for general use : 2 sets
Simple 8-bit timer : 1 set

Timer 0 (8-bit timer for general use)
Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM0IOB), event count, remote control carrier output, simple pulse with measurement
Clock source: fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output
Real timer output control
Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; "High" -fixed, "LOW" -fixed and "Hi-Z" -fixed

Timer 1 (8-bit timer for general use)
Square wave output(timer pulse output), event count, 16-bit cascade connected (timer0, 1), timer synchronous output event
Clock source: fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 2 (8-bit timer for general use)
Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM2IOB), event count, simple pulse with measurement, 24-bit cascade connected (timer0, 1), timer synchronous output event
Clock source: fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output
Real timer output control
Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; "High" -fixed, "LOW" -fixed and "Hi-Z" -fixed

Timer 3 (8-bit timer for general use)
Square wave output(timer pulse output), event count, remote control carrier output, 16bit cascade connected (timer2), 32-bit cascade connected (timer0, 1, 2)
Clock source: fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 4 (8-bit timer for general use)
Square wave output (timer pulse output), added pulse(2-bit) system PWM output, event count, serial transfer clock, simple pulse measurement
Clock source: fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 6 (8-bit free-running timer, Time base timer)
8-bit free-running timer
Clock source: fpll, fpll/2^{12}, fpll/2^{13}, fs, fx, fx/2^{12}, fx/2^{13}
Time base timer
Interrupt generation cycle: fpll/2^{7}, fpll/2^{8}, fpll/2^{9}, fpll/2^{10}, fpll/2^{13}, fpll/2^{15}, fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

■ Features (continued)

- Timer Counter (contined)

Timer 7 (16-bit timer for general use)

Clock source: fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output

Hardware organization

Compare register with double buffer : 2 sets
Input capture register : 1 set
Timer interrupt : 2 vectors

Timer functions

Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable),
IGBT output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOB
Timer synchronous output, event count, Input capture function (Both edges can be operated)

Real timer output control

Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; "High" -fixed, "LOW" -fixed and "Hi-Z" -fixed

Timer 8 (16-bit timer for general use)

Clock source: fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output

Hardware organization

Compare register with double buffer : 2 sets
Input capture register : 1 set
Timer interrupt : 2 vectors

Timer functions

Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture (Both edge available),
32-bit cascade connected (Timer7, 8), 32-bit PWM output, Input capture is available at 32-bit cascade

TimerA output (Simple timer counter A)

Clock output for peripheral function

- Watchdog timer

Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
On detection of errors, hard reset is done inside LSI.

- Synchronous output function

Timer synchronous output, interrupt synchronous output
Port 8 outputs the latched data, on the event timing of the synchronous output signal of timer
Timer1, Timer2, or Timer7, or of the external interrupt 2 (IRQ2).

- Buzzer Output/Reverse Buzzer Ouput:

Output frequency can be selected from $fpll/2^9$, $fpll/2^{10}$, $fpll/2^{11}$, $fpll/2^{12}$, $fpll/2^{13}$, $fpll/2^{14}$, $fx/2^3$, $fx/2^4$.

- Remote Control Carrier Output:

A remote control carrier output with duty cycle of 1/2 or 1/3 of timer 0 or timer 3 output are available.

- A/D Converter

10-bit × 12 channels

■ Features (continued)

- Data automatic transfer : 1 system

ATC1

Data is transferred automatically in all memory space
External request/internal event request/software request
Maximum transfer cycles are 255
Support continuous serial transmission / reception.
Burst transfer function (Urgent stop of interrupts is contained.)

- Serial Interface: 5 channels

Serial 0 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
Transfer clock source: fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
Sequence transmission, reception or both are available.
Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
Parity check, Overrun error / Framing error detection
Transfer size 7 to 8 bits can be selected.

Serial 1 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
Transfer clock source: fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
Sequence transmission, reception or both are available.
Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
Parity check, Overrun error / Framing error detection
Transfer size 7 to 8 bits can be selected.

Serial 2 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
Transfer clock source: fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output,external clock
MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
Sequence transmission, reception or both are available.
Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
Parity check, Overrun error / Framing error detection
Transfer size 7 to 8 bits can be selected.

Serial 4 (multi master IIC / Synchronous serial interface)
Synchronous serial interface
Transfer clock source: fpll/2, fpll/4, fpll/8, fpll/32, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
Sequence transmission, reception or both are available.
Multi master IIC
7-bit of slave address can be set.
General call communication mode handling

Serial5
IIC slave interface
IIC high-speed transfer mode (communication speed: 400 kbps)
7-bit or 10-bit of slave address can be set.
General call communication mode handling

■ Features (continued)

- LED Driver: 7 pins (Push-pull structure)

- Automatic Reset

- LCD Driver: LCD driver pins

  Segment output max. 41 pins (SEG0 to 40)

  SEG0 to 40 can be switched to I/O ports by 1 pin

  Note: At reset, SEG0 to 40 are input ports.

  Common output pins:4 pins

  COM0 to 3 can be switched to I/O ports by 1 pin

  Display mode selection

  Static

  1/2 duty, 1/2 bias

  1/3 duty, 1/3 bias

  1/4 duty, 1/3 bias

  LCD driver clock

  When the source clock is the main clock (fpll)

  $1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$

  When the source clock is the sub clock (fx)

  $1/2^{9}$, $1/2^{8}$, $1/2^{7}$, $1/2^{6}$

  When the source clock is the main clock

  Timer0, 1, 2, 3, 4 and A output

  LCD power supply

  Use at $V_{DD5} \geq V_{LC1}$

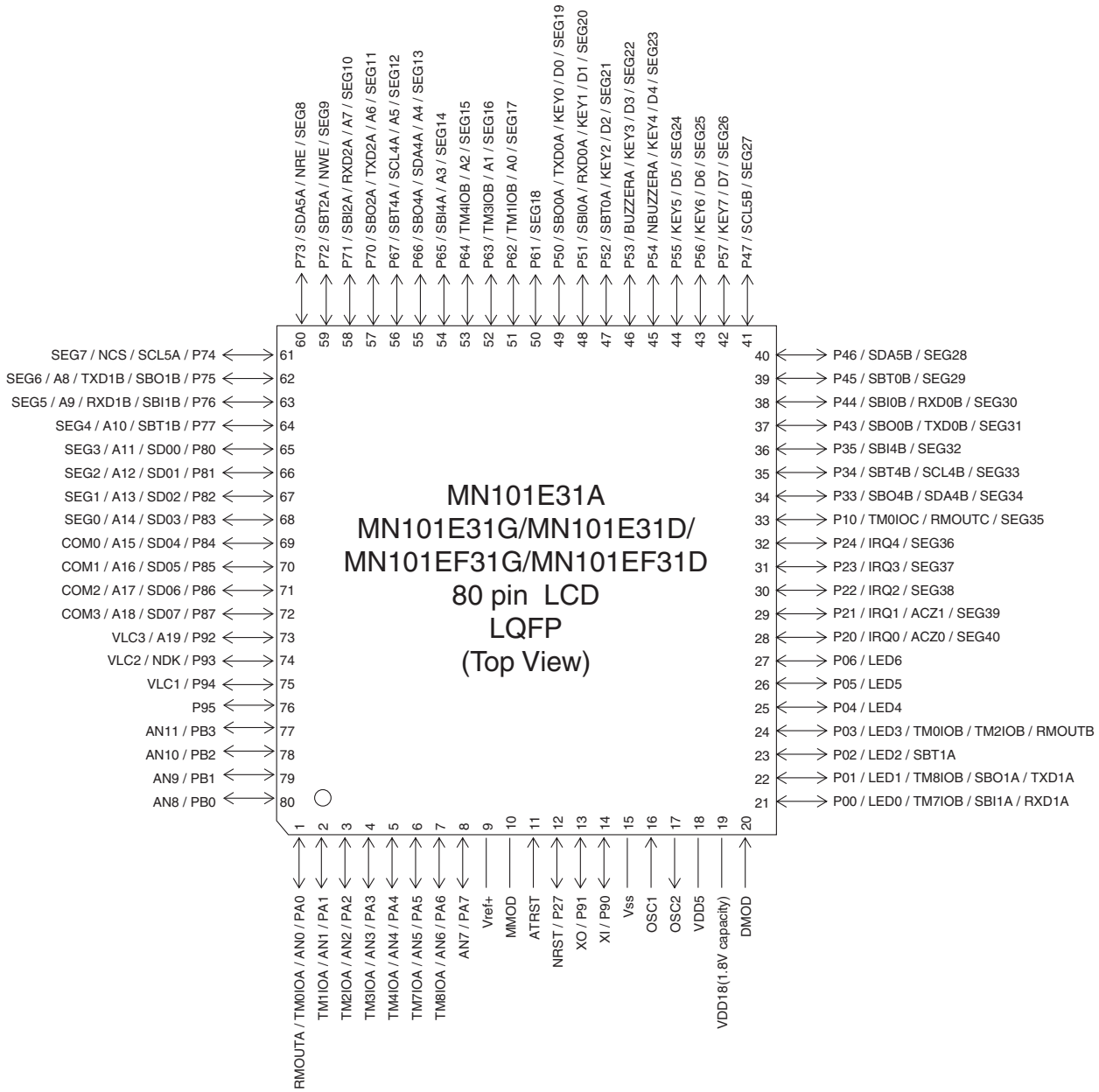
  External supply voltage is input from V_{LC1}, V_{LC2}, V_{LC3} pins or voltage applied to V_{LC1} is divided by internal resistance and supplied to V_{LC2} and V_{LC3} pins.

- Port:

I/O ports:	70 pins
LED (large current) driver pins:	7 pins
LCD driver for segment:	41 pins
LCD driver for common:	4 pins
Serial interface pin:	25 pins
Timer I/O:	15 pins
Buzzer output:	2 pins
A/D input:	12 pins
External interrupt pin:	5 pins
LCD power:	3 pins
XI/XO:	2 pins
Special pins:	10 pins
Operation mode input pins:	3 pins
Analog reference voltage input pin:	1 pin
Reset input pin:	1 pin
Oscillation pins:	2 pins
Power pins:	3 pins

■ Pin Description

• LQFP080-P-1414A



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