1.1 Overview

1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EF94G has an internal 128 KB of ROM and 6 KB of RAM. MN101EF94F has an internal 96 KB of ROM and 6 KB of RAM. Peripheral functions include 5 external interrupts, 29 internal interrupts including NMI, 11 timer counters, 6 types of serial interfaces, A/D converter, LCD driver, 2 types of watchdog timer, data automatic function and buzzer output. The system configuration is suitable for in camera, timer selector for VCR, CD player, or minicomponent.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz), high-speed (crystal/ceramic frequency: max. 10 MHz) / low-speed (internal frequency: 30 kHz), low-speed (crystal/ceramic frequency: 32.768 kHz) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

1.1.2 Product Summary

This manual describes the following model.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
MN101EF94G	128 KB	6 KB	Flash EEPROM version	100 Pin LQFP
MN101EF94F	96 KB	6 KB		

1.2 Hardware Functions

■ Feature

- ROM / RAM capacity:
  MN101EF94G: ROM 128 KB / RAM 6 KB
  MN101EF94F:ROM 96 KB / RAM 6 KB

- Package:
  LQFP100-P-1414C (14 mm × 14 mm / 0.5 mm pitch, halogen free)

  Panasonic "halogen free" semiconductor products refer to the products made of molding resin and interposer which conform to the following standards.
  - Bromine : 900 ppm (Maximum Concentration Value)
  - Chlorine : 900 ppm (Maximum Concentration Value)
  - Bromine + Chlorine : 1500 ppm (Maximum Concentration Value)

  The above-mentioned standards are based on the numerical value described in IEC61249-2-21.
  Antimony and its compounds are not added intentionally.

- Machine Cycle:

  NORMAL mode
  0.05 μs/ 20 MHz (2.7 V to 5.5 V)
  0.125 μs/ 8 MHz (1.8 V to 5.5 V)

  SLOW mode
  62.5 μs/ 32 kHz (1.8 V to 5.5 V)

- Oscillation Circuit

  High-speed (Internal oscillation: frc = 16MHz)
  High-speed (External oscillation: fosc)
  Low-speed (Internal oscillation: frcs = 32.5kHz)
  Low-speed (External oscillation: fx)

- PLL:

  PLL clock (fpll): fosc multiplied by 2, 3, 4, 5, 6, 8, 10
  frc multiplied by 2, 2.5

- Memory Bank

  Data area consists of memory banks 0 to 2 with each bank consisting of 64 KB.

- Operation Mode

  NORMAL/SLOW/HALT/LP/STOP

- Operating Voltage: 1.8 V to 5.5 V

- Operation Ambient Temperature: -40 °C to +85 °C

- External Interrupts: 5

  IRQ0/IRQ1/IRQ2/IRQ3/IRQ4

- Timer Counter: 11

  - General-purpose 8-bit timer × 5
  - General-purpose 16-bit timer × 2
  - Motor control 16-bit timer × 1
  - 8-bit free-run timer × 1
  - Time-base timer × 1
  - Baud rate timer × 1

  Timer 0 (General-purpose 8-bit timer)

  - Square wave output (Timer pulse output), added pulse (2 bits) type PWM output, event count, simple pulse width measurement
  - Clock source
    fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
  - Real-time control
    Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

  Timer 1 (General-purpose 8-bit timer)

  - Square wave output (Timer pulse output), event count
    16-bit cascade connection (connected with timer 0)
  - Clock source
    fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

  Timer 2 (General-purpose 8-bit timer)

  - Square wave output (Timer pulse output), added pulse (2 bits) type PWM output, event count, simple pulse width measurement,
    24-bit cascade connection (connected with timer 0, 1), timer synchronous output
  - Double-buffered compare register (× 1)
  - Clock source
    fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
  - Real-time control
    Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

  Timer 3 (General-purpose 8-bit timer)

  - Square wave output (Timer pulse output), event count
    16-bit cascade connection (connected with timer 2),
    32-bit cascade connection (connected with timer 0, 1, 2)
  - Double-buffered compare register (× 1)
  - Clock source
    fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

  Timer 4 (General-purpose 8-bit timer)

  - Square wave output (Timer pulse output), added pulse (2-bit) type PWM output, event count, simple pulse width measurement
  - Clock source
    fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 6 (8-bit free-run timer, time-base timer)

8-bit free-run timer
- Clock source
  fpll-div, fpll-div/2^2, fpll-div/2^3, fpll-div/2^{12}, fpll-div/2^{13}, fs, fslow,
  fslow/2^2, fslow/2^3, fslow/2^{12}, fslow/2^{13}

Time-base timer
- Interrupt generation cycle
  fpll-div/2^7, fpll-div/2^8, fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{13},
  fpll-div/2^{15},fslow/2^7, fslow/2^8, fslow/2^9, fslow/2^{10}, fslow/2^{13}, fslow/2^{15}

Timer 7 (General-purpose 16-bit timer)

- Clock source
  fpll-div, fs, external clock, timer A output, serial 0 transfer clock output,
  timer 6 compare match cycle divided by 1, 2, 4, 16
- Hardware configuration
  Double-buffered compare register (× 2)
  Double-buffered input capture register (× 2)
  Timer interrupt (× 2 vector)
- Timer function
  Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable), timer synchronous output, event count,
  input capture function (both edges operable)
- Real-time control
  Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "High Impedance" at falling edge of external interrupt 0 (IRQ0)

Timer 8 (General-purpose 16-bit timer)

- Clock source
  fpll-div, fs, external clock, timer A output, timer 6 compare match cycle divided by 1, 2, 4, 16
- Hardware configuration
  Double-buffered compare register (× 2)
  Double-buffered input capture register (× 1)
  Timer interrupt (× 2 vector)
- Timer function
  Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable), event count, pulse width measurement,
  input capture function (both edges operable)
  32-bit cascade connection (connected with timer 7), 32-bit PWM output,
  input capture is available in 32-bit cascade

Timer 9 (Motor control 16-bit timer)

- Clock source
  fpll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16
- Hardware configuration
  Double-buffered compare register (× 2)
  Timer interrupt (× 3 vector)
- Timer function
  Square wave output (Timer pulse output), complementary 3-phase PWM output, triangle wave and saw tooth wave are supported,
  dead time insertion available, event count
- Pin output control
  PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4)
  ("High Impedance", output data fixed)

Timer A (Baud rate timer)

- Clock output for peripheral functions
- Clock source
  fpll-div divided by 1, 2, 4, 8, 16, 32, and fs divided by 2, 4

- Watchdog Timer

Overrun detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
Forced to reset inside LSI by hardware when a software processing error is detected twice

- Watchdog Timer 2

Overrun detection cycle is selectable from $frcs/2^4$, $frcs/2^5$, $frcs/2^6$, $frcs/2^7$, $frcs/2^8$, $frcs/2^9$, $frcs/2^{10}$, $frcs/2^{11}$, $frcs/2^{12}$, $frcs/2^{13}$, $frcs/2^{14}$, $frcs/2^{15}$
Forced to reset inside LSI by hardware when a software processing error is detected twice

- Synchronous Output

Latch data is output from port 8 at the event timing of synchronous output signal of timer 1, timer 2, timer 7, or external interrupt2 (IRQ2)

- Buzzer Output

Output frequency can be selected from $fpll\text{-}div/2^9$, $fpll\text{-}div/2^{10}$, $fpll\text{-}div/2^{11}$, $fpll\text{-}div/2^{12}$, $fpll\text{-}div/2^{13}$, $fpll\text{-}div/2^{14}$, $fslow/2^3$, $fslow/2^4$

- A/D Converter
  10-bit × 19 channels

- Data Automatic Transfer
  Data is automatically transferred in all memory space
  - External interrupt activation/internal event activation/software activation
  - Max. 255 byte continuous transfer
  - Serial continuous transmission and reception is supported
  - Burst transfer function (Including interrupt emergency stop)

- Serial Interface: 6 systems

Serial Interface 0 (Full duplex UART / Clock synchronous serial interface)

Clock synchronous serial interface
- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, number of bits to transfer is selectable from 1 to 8
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Number of bits to transfer is selectable from 7 to 8

Serial Interface 1 (Full duplex UART / Clock synchronous serial interface)

Clock synchronous serial interface
- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, number of bits to transfer is selectable from 1 to 8
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Number of bits to transfer is selectable from 7 to 8

Serial Interface 2 (Full duplex UART / Clock synchronous serial interface)

Clock synchronous serial interface
- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, number of bits to transfer is selectable from 1 to 8
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Number of bits to transfer is selectable from 7 to 8
- 38 kHz Carrier pulse output

Serial Interface 3 (Full duplex UART / Clock synchronous serial interface)

Clock synchronous serial interface
- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, number of bits to transfer is selectable from 1 to 8
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Number of bits to transfer is selectable from 7 to 8

Serial Interface 4 (Multi master IIC / Clock synchronous serial interface)

Clock synchronous serial interface
- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4,
  Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, number of bits to transfer is selectable from 1 to 8
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Multi master IIC
- 7, 10-bit slave address is selectable
- General call communication mode is supported

Serial Interface 5 (Full duplex UART / Clock synchronous serial interface)

Clock synchronous serial interface
- MSB/LSB first selectable, number of bits to transfer is selectable from 1 to 8
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART
- Parity check, overrun error/framing error are detected
- Number of bits to transfer is selectable from 7 to 8
- Clock output for IC card interface

- Auto Reset Circuit

- Low Voltage Detection Circuit

- Clock Monitoring Function

- LED Driver: 8

- LCD Driver

Segment output
Maximum 55 pins (SEG0 to SEG54)
Segment output pins can be switched to I/O ports individually.
* At reset, Segment outputs are input ports.
Common output: 8 pins
COM0 to 3 and COM0A to 3A can be switched to I/O ports in 1 bit.
* COM0A to 3A are shared with SEG0 to 3
Display mode selection
Static
1/2 duty, 1/2 bias
1/3 duty, 1/3 bias
1/4 duty, 1/3 bias
1/8 duty, 1/3 bias
LCD driver clock
When the source clock is the main clock (fpll)
1/218,1/217,1/216,1/215,1/214,1/213,1/212,1/211
When the source clock is the sub clock (fslow)
1/29,1/28,1/27,1/26
Timer 0 to 4, Timer A output
LCD power supply
LCD power supply is separated from VDD5. (can be used when $V_{LC1} \leq V_{DD5}$)
External power supply voltage can be selectable, and is supplied from VLC1, VLC2 and VLC3.
Internal resistors can divide the voltage input to VLC1.

1.3 Pin Description

1.3.1 Pin configuration

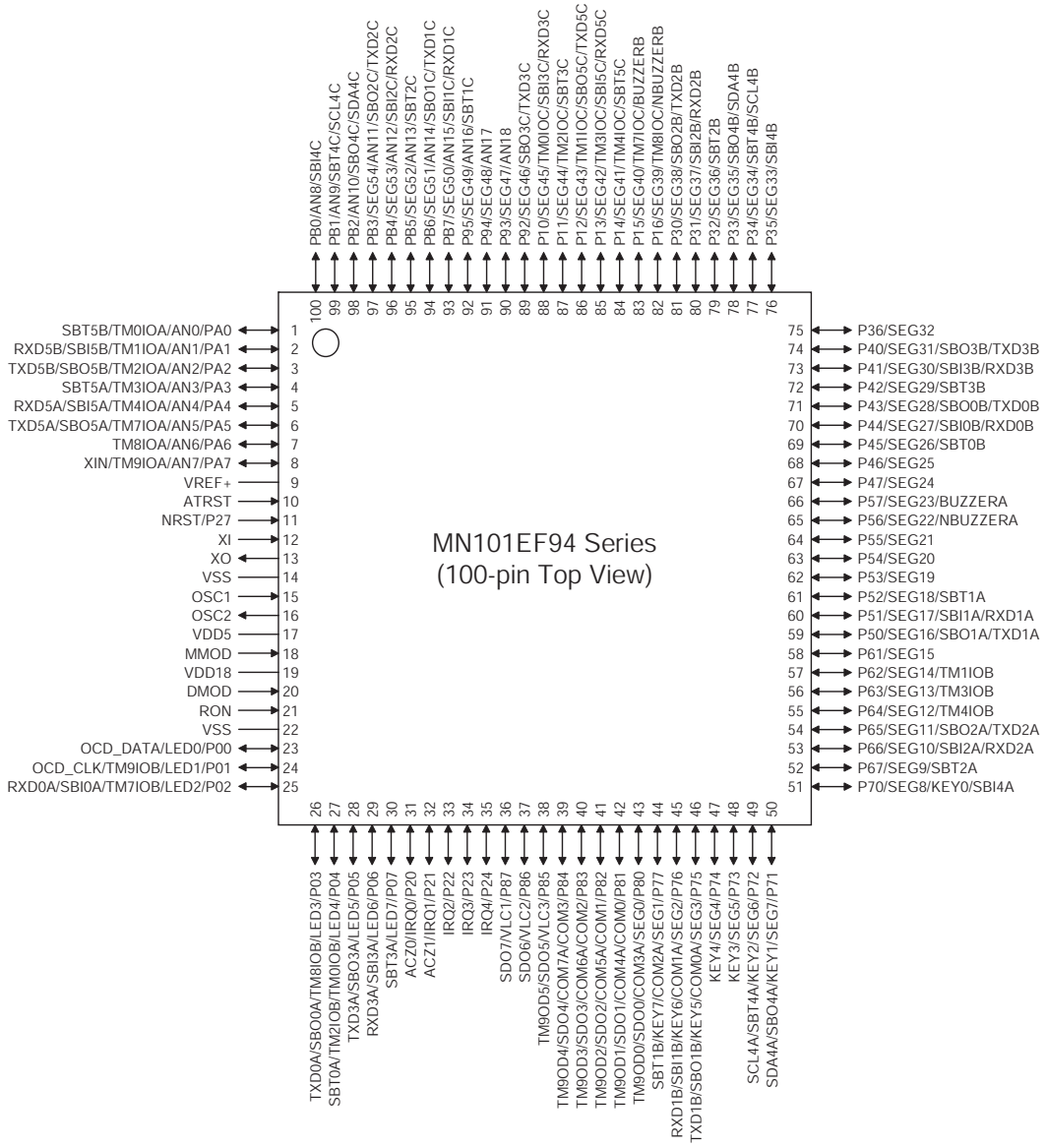

Figure:1.3.1 Pin Configuration

1.3.2 Pin Functions

Table:1.3.1 Pin Functions

Pins	Pin No.	I/O	Functions	Descriptions
VSS VDD5	14, 22 17	-	Power supply	Supply 1.8 V to 5.5 V to V_{DD5}, and 0 V to V_{SS}. Connect 0.1μF and more than 1 μF of bypass capacitor for internal power stabilization
VDD18	19	-	Internal power output	Outputs internal power voltage 1.8 V. Connect 0.1 μF and more than 1 μF of bypass capacitor between V_{DD18} and V_{SS} pins for internal power stabilization.
OSC1 OSC2	15 16	Input Output	High-speed oscillation clock input High-speed oscillation clock output	Connect these oscillation pins to ceramic oscillator or crystal oscillator for high-speed operation clock. For external clock input, input to OSC1 and open OSC2.
XI XO	12 13	Input Output	Low-speed oscillation clock input Low-speed oscillation clock output	Connect these oscillation pins to ceramic oscillator or crystal oscillator for low-speed operation clock.
NRST	11	Input	Reset [Active low]	The LSI is reset when NRST pin is driven to low-level. NRST pin has an internal pull-up resistor (Typical 50 kΩ), and Nch open-drain output. If a capacitor is connected between NRST and V_{SS}, it is recommended that a discharge diode be placed between NRST and V_{DD5}.
ATRST	10	Input	Auto reset control	Pull-up (when auto reset function is enabled) or pull-down (when auto reset function is disabled) the pin with the resistor.
P00 P01 P02 P03 P04 P05 P06 P07	23 24 25 26 27 28 29 30	I/O	I/O port 0	General-purpose I/O ports.
P10 P11 P12 P13 P14 P15 P16	88 87 86 85 84 83 82	I/O	I/O port 1	
P20 P21 P22 P23 P24	31 32 33 34 35	I/O	I/O port 2	
P27	11	Input	Input port 2	P27 is an Nch open-drain port. and a low-level is output by setting the P2OUT7 flag of P2OUT register to “0”. (Software reset)
P30 P31 P32 P33 P34 P35 P36	81 80 79 78 77 76 75	I/O	I/O port 3	General-purpose I/O ports.
P40 P41 P42 P43 P44 P45 P46 P47	74 73 72 71 70 69 68 67	I/O	I/O port 4	
P50 P51 P52 P53 P54 P55 P56 P57	59 60 61 62 63 64 65 66	I/O	I/O port 5	

Pins	Pin No.	I/O	Functions	Descriptions
P61	58	I/O	I/O port 6	General-purpose I/O ports.
P62	57			
P63	56			
P64	55			
P65	54			
P66	53			
P67	52			
P70	51	I/O	I/O port 7	
P71	50			
P72	49			
P73	48			
P74	47			
P75	46			
P76	45			
P77	44			
P80	43	I/O	I/O port 8	
P81	42			
P82	41			
P83	40			
P84	39			
P85	38			
P86	37			
P87	36			
P92	89	I/O	I/O port 9	
P93	90			
P94	91			
P95	92			
PA0	1	I/O	I/O port A	
PA1	2			
PA2	3			
PA3	4			
PA4	5			
PA5	6			
PA6	7			
PA7	8			
PB0	100	I/O	I/O port B	
PB1	99			
PB2	98			
PB3	97			
PB4	96			
PB5	95			
PB6	94			
PB7	93			
SBO0A	26	Output	Serial interface data output	Transmission data output pins for serial interface 0, 1, 2, 3, 4 and 5.
SBO0B	71			
SBO1A	59			
SBO1B	46			
SBO1C	94			
SBO2A	54			
SBO2B	81			
SBO2C	97			
SBO3A	28			
SBO3B	74			
SBO3C	89			
SBO4A	50			
SBO4B	78			
SBO4C	98			
SBO5A	6			
SBO5B	3			
SBO5C	86			

Pins	Pin No.	I/O	Functions	Descriptions
SBI0A	25	Input	Serial interface data input	Reception data input pins for serial interface 0, 1, 2, 3, 4 and 5.
SBI0B	70			
SBI1A	60			
SBI1B	45			
SBI1C	93			
SBI2A	53			
SBI2B	80			
SBI2C	96			
SBI3A	29			
SBI3B	73			
SBI3C	88			
SBI4A	51			
SBI4B	76			
SBI4C	100			
SBI5A	5			
SBI5B	2			
SBI5C	85			
SBT0A	27	I/O	Serial interface clock I/O	Clock I/O pins for serial interface 0, 1, 2, 3, 4 and 5.
SBT0B	69			
SBT1A	61			
SBT1B	44			
SBT1C	92			
SBT2A	52			
SBT2B	79			
SBT2C	95			
SBT3A	30			
SBT3B	72			
SBT3C	87			
SBT4A	49			
SBT4B	77			
SBT4C	99			
SBT5A	4			
SBT5B	1			
SBT5C	84			
TXD0A	26	Output	UART data output	In the serial interface 0, 1, 2, 3 and 5 in UART mode, these pins are configured as the transmission data output pin.
TXD0B	71			
TXD1A	59			
TXD1B	46			
TXD1C	94			
TXD2A	54			
TXD2B	81			
TXD2C	97			
TXD3A	28			
TXD3B	74			
TXD3C	89			
TXD5A	6			
TXD5B	3			
TXD5C	86			
RXD0A	25	Input	UART data input pins	In the serial interface 0, 1, 2, 3 and 5 in UART mode, these pins are configured as the reception data input pin.
RXD0B	70			
RXD1A	60			
RXD1B	45			
RXD1C	93			
RXD2A	53			
RXD2B	80			
RXD2C	96			
RXD3A	29			
RXD3B	73			
RXD3C	88			
RXD5A	5			
RXD5B	2			
RXD5C	85			
SDA4A	50	I/O	IIC data I/O	In the serial interface 4 in IIC mode, these pins are configured as the data input / output pin.
SDA4B	78			
SDA4C	98			
SCL4A	49	I/O	IIC clock I/O	In the serial interface 4 in IIC mode, these pins are configured as the clock input / output pin.
SCL4B	77			
SCL4C	99			

Pins	Pin No.	I/O	Functions	Descriptions
OCD_DATA	23	I/O	On-board programmer data I/O	Data I/O pin and clock input pin for the on-board programmer. Refer to [Chapter 21 Internal Flash Memory] of LSI User's Manual .
OCD_CLK	24	Input	On-board programmer clock input	
TM0IOA	1	I/O	8-bit timer I/O	Event count clock input, timer output, and PWM signal output pins for 8-bit timer 0 to 4.
TM0IOB	27			
TM0IOC	88			
TM1IOA	2			
TM1IOB	57			
TM1IOC	86			
TM2IOA	3			
TM2IOB	27			
TM2IOC	87			
TM3IOA	4			
TM3IOB	56			
TM3IOC	85			
TM4IOA	5			
TM4IOB	55			
TM4IOC	84			
BUZZERA	66	Output	Buzzer output	Piezoelectric buzzer output pin.
NBUZZERA	65			
BUZZERB	83			
NBUZZERB	82			
TM7IOA	6	I/O	16-bit timer I/O	Event count clock input, timer output, and PWM signal output pins for 16-bit timer 7, 8 and 9.
TM7IOB	25			
TM7IOC	83			
TM8IOA	7			
TM8IOB	26			
TM8IOC	82			
TM9IOA	8			
TM9IOB	24			
TM9OD0	43	Output	16-bit timer output	Timer output and PWM signal output pins for 16-bit timer.
TM9OD1	42			
TM9OD2	41			
TM9OD3	40			
TM9OD4	39			
TM9OD5	38			
SDO0	43	Output	Synchronous output	8-bit synchronous output pins.
SDO1	42			
SDO2	41			
SDO3	40			
SDO4	39			
SDO5	38			
SDO6	37			
SDO7	36			
VREF+	9	-	A/D reference power supply	Reference power supply pin for the A/D converter. This pin is generally used as $V_{REF+} = V_{DD5}$.
AN0	1	Input	Analog input	Analog input pins to A/D converter.
AN1	2			
AN2	3			
AN3	4			
AN4	5			
AN5	6			
AN6	7			
AN7	8			
AN8	100			
AN9	99			
AN10	98			
AN11	97			
AN12	96			
AN13	95			
AN14	94			
AN15	93			
AN16	92			
AN17	91			
AN18	90			
IRQ0	31	Input	External interrupt input	External interrupt input pins.
IRQ1	32			
IRQ2	33			
IRQ3	34			
IRQ4	35			

Pins	Pin No.	I/O	Functions	Descriptions
ACZ0	31	Input	AC zero-cross input	Input pins to AC zero-cross detection circuit.
ACZ1	32			
KEY0	51	Input	KEY interrupt input	Input pins for interrupt based on ORed result of KEY inputs.
KEY1	50			
KEY2	49			
KEY3	48			
KEY4	47			
KEY5	46			
KEY6	45			
KEY7	44			
LED0	23	Output	LED driver	Large current output pins.
LED1	24			
LED2	25			
LED3	26			
LED4	27			
LED5	28			
LED6	29			
LED7	30			
COM0	42	Output	LCD common output	Common signal output pins for LCD display. Connect these pins to the common ports of LCD display panel.
COM0A	46			
COM1	41			
COM1A	45			
COM2	40			
COM2A	44			
COM3	39			
COM3A	43			
COM4A	42			
COM5A	41			
COM6A	40			
COM7A	39			
VLC1	36	-	LCD power supply	Apply voltage of 5.5 V ≥ V_{LC1} ≥ V_{LC2} ≥ V_{LC3} ≥ 0 V.
VLC2	37			
VLC3	38			

Pins	Pin No.	I/O	Functions	Descriptions
SEG0	43	Output	LCD segment output pins	Segment output pins for LCD display. Connect these pins to the segment ports of the LCD panel.
SEG1	44			
SEG2	45			
SEG3	46			
SEG4	47			
SEG5	48			
SEG6	49			
SEG7	50			
SEG8	51			
SEG9	52			
SEG10	53			
SEG11	54			
SEG12	55			
SEG13	56			
SEG14	57			
SEG15	58			
SEG16	59			
SEG17	60			
SEG18	61			
SEG19	62			
SEG20	63			
SEG21	64			
SEG22	65			
SEG23	66			
SEG24	67			
SEG25	68			
SEG26	69			
SEG27	70			
SEG28	71			
SEG29	72			
SEG30	73			
SEG31	74			
SEG32	75			
SEG33	76			
SEG34	77			
SEG35	78			
SEG36	79			
SEG37	80			
SEG38	81			
SEG39	82			
SEG40	83			
SEG41	84			
SEG42	85			
SEG43	86			
SEG44	87			
SEG45	88			
SEG46	89			
SEG47	90			
SEG48	91			
SEG49	92			
SEG50	93			
SEG51	94			
SEG52	95			
SEG53	96			
SEG54	97			
MMOD	18	Input	Memory mode control	Set to V_{DD5}-level or V_{SS}-level via pull-up (when BOOT mode is enabled) or pull-down (when BOOT mode is disabled) resistor.
DMOD	20	Input	Mode control	Set always to V_{DD5}-level with pull-up resistor.
RON	21	Input	Regulator control	When connecting the pull-up resistor with this pin, make it to 200 Ω or less. Set always to V_{DD5}-level.
XIN	8	Input	External slow clock input	When external slow clock is used, input through XIN pin.

1.4 Electrical Characteristics

When using this LSI, contact our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General-purpose
Function	CMOS 8-bit single chip microcomputer

1.4.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 *4 V_{SS} = 0 V

Parameter			Symbol	Rating	Unit
A1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
A2	Power supply voltage		V_{DD18}	-0.3 to +2.5	
A3	Input clamp current (ACZ)		I_C	-500 to +500	μA
A4	Input pin voltage		V_I	-0.3 to V_{DD5} +0.3 (upper limit 7.0 V)	V
A5	Output pin voltage		V_O	-0.3 to V_{DD5} +0.3 (upper limit 7.0 V)	
A6	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} +0.3 (upper limit 7.0 V)	
A7	XI/XO pin voltage		V_{XIO}	-0.3 to V_{DD18} +0.3 (upper limit 2.5 V)	
A8	Peak output current	LED output	I_{OL1} (peak)	30	mA
A9		Other than LED output	I_{OL2} (peak)	20	
A10		All pins	I_{OH} (peak)	-10	
A11	Average output current *1	LED output	I_{OL1} (avg)	20	
A12		Other than LED output	I_{OL2} (avg)	15	
A13		All pins	I_{OH} (avg)	-5	
A14	Power dissipation		P_T	400	mW
A15	Operating ambient temperature		T_{opr}	-40 to +85	°C
A16	Storage temperature		T_{STG}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one capacitor of 0.1 μF and 1.0 μF or larger between pin VDD5 and pin VSS for the internal power voltage stabilization.

*3 Connect 0.1 μF and 1.0 μF capacitor between pin VDD18 and pin VSS, near the microcontroller according to the figure shown below for the internal power supply stabilization.

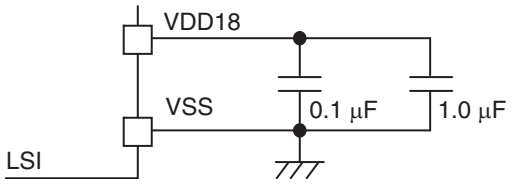

Figure:1.4.1 Capacitor Connection between VDD18 and VSS Pins

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

1.4.2 Operating Conditions

B. Operating Conditions

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *5							
B1	Power supply voltage	V_{DD1}	fs ≤ 20 MHz *7	2.7		5.5	V
B2		V_{DD2}	fs ≤ 10 MHz *8	2.7		5.5	
B3		V_{DD3}	fs ≤ 8 MHz *7	1.8		5.5	
B4		V_{DD4}	fs ≤ 8 MHz *7, *9	2.0		5.5	
B5		V_{DD6}	fs ≤ 4 MHz *8	1.8		5.5	
B6		V_{DD7}	fs ≤ 4 MHz *8, *10	2.0		5.5	
B7		V_{DD8}	fs = 16.384 kHz	1.8		5.5	
B8	RAM retention power supply voltage	V_{DD9}	During STOP mode	1.8		5.5	
Operating speed *6							
B9	Instruction execution time fs	t_{c1}	V_{DD5} = 2.7 V to 5.5 V *7	0.05			µs
B10		t_{c2}	V_{DD5} = 2.7 V to 5.5 V *8	0.10			
B11		t_{c3}	V_{DD5} = 1.8 V to 5.5 V *7	0.125			
B12		t_{c4}	V_{DD5} = 2.0 V to 5.5 V *7, *9	0.125			
B13		t_{c5}	V_{DD5} = 1.8 V to 5.5 V *8	0.25			
B14		t_{c6}	V_{DD5} = 2.0 V to 5.5 V *8, *10	0.25			
B15		t_{c7}	V_{DD5} = 1.8 V to 5.5 V	61			

*5 fs : Machine clock frequency

*6 tc1 to 6 : when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscillations multiplied by PLL.
tc7 : when the machine clock is selected from external low-speed oscillation or internal low-speed oscillation.

*7 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b1”

*8 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b0”

*9 When setting frc=16 MHz, fs=frc/2

*10 When setting frc=16 MHz, fs=frc/4

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External Oscillator 1 Figure:1.4.2							
B16	Frequency	f_{hosc1}	V_{DD5} is within the specified operating power supply voltage range. (Refer to the ratings B1 to B6 for the specified operating power supply voltage range)	2.0		10	MHz
B17	Internal feedback resistor	R_{f10}	V_{DD5} = 5.0 V		980		kΩ
External Oscillator 2 Figure:1.4.3							
B18	Frequency	f_{sosc1}	V_{DD5} = 1.8 V to 5.5 V		32.768		kHz
B19	Internal feedback resistor	R_{f20}	V_{DD5} = 5.0 V		16.0		MΩ

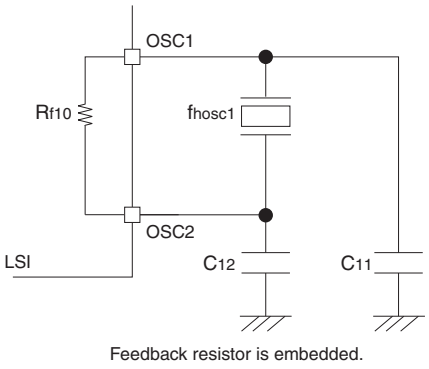

Figure:1.4.2 External Oscillator 1

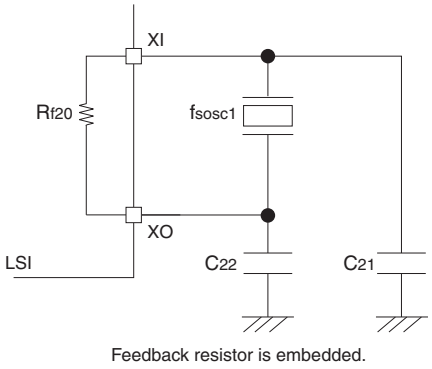

Figure:1.4.3 External Oscillator 2

Connect external capacitors suited for the used oscillator.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor.
Please consult the oscillator manufacturer and perform matching tests to determine the appropriate values of external capacitors.

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
B20	Clock frequency	f_{hosc2}		2		10.0	MHz
B21	High-level pulse width *11	t_{wh1}	Figure:1.4.4	45			ns
B22	Low-level pulse width *11	t_{wl1}		45			
B23	Rising time	t_{wr1}	Figure:1.4.4	0		5.0	
B24	Falling time	t_{wf1}		0		5.0	
External clock input 2 XIN							
B25	Clock frequency	f_{sosc2}			32.768		kHz
B26	High-level pulse width *11	t_{wh2}	Figure:1.4.5		4.5		µs
B27	Low-level pulse width *11	t_{wl2}			4.5		
B28	Rising time	t_{wr2}	Figure:1.4.5	0		20	ns
B29	Falling time	t_{wf2}		0		20	

*11 The clock duty ratio should be 45% to 55%

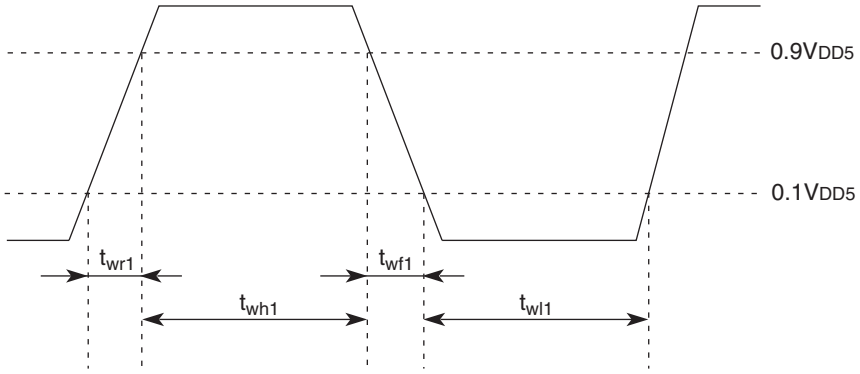

Figure:1.4.4 OSC1 Timing Chart

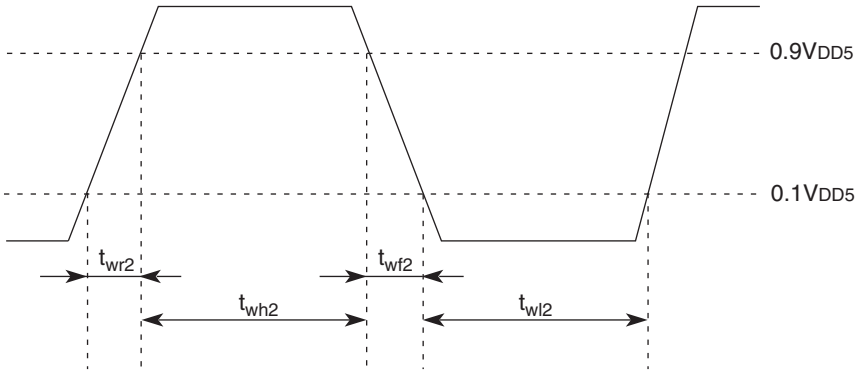

Figure:1.4.5 XIN Timing Chart

Pin XI and XO are used for self-excited oscillation only. therefore, do not use for separately-excited oscillation.

1.4.3 DC Characteristics

C. DC Characteristics

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
Power supply current *13							
C1	Power supply current during operation	I_{DD1}	fosc=10 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (PLL is not used) *14		5	14	mA
C2		I_{DD2}	fosc=4 MHz [Multiply by 10: fs=20 MHz] V_{DD5}=5 V (PLL is used) *14		8	18	
C3		I_{DD3}	fx=32.768 kHz [fs=fx/2] V_{DD5}=3 V Ta=25 °C CPU executes the program in ROM.		35	65	µA
C4			fx=32.768 kHz [fs=fx/2] V_{DD5}=3 V Ta=85 °C CPU executes the program in ROM.			150	
C5		I_{DD4}	fx=32.768 kHz [fs=fx/2] V_{DD5}=3 V Ta=25 °C CPU executes the program in RAM. *15		5	20	
C6			fx=32.768 kHz [fs=fx/2] V_{DD5}=3 V Ta=85 °C CPU executes the program in RAM. *15			65	
C7	Power supply current during HALT1 mode	I_{DD5}	fx=32.768 kHz, V_{DD5}=3 V Ta=25 °C		3	10	
C8			fx=32.768 kHz, V_{DD5}=3 V Ta=85 °C			50	
C9	Power supply current during LP1 mode	I_{DD6}	fx=32.768 kHz, V_{DD5}=3 V Ta=25 °C		2	9	
C10			fx=32.768 kHz, V_{DD5}=3 V Ta=85 °C			50	
C11	Power supply current during STOP mode	I_{DD7}	V_{DD5}=5 V, Ta=25 °C		1	5	
C12			V_{DD5}=5 V, Ta=85 °C			45	

*13 Measured without loading (pull-up and pull-down resistors are not connected.)

I_{DD1} to I_{DD2} are measured on the following condition that:
1. Set the all I/O pins to input mode.
2. Set CPU mode to <NORMAL mode>.
3. Fix MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.
4. Input the square wave of 10 MHz (4 MHz), which has amplitude of V_{DD5} and V_{SS} potential, from OSCI1 pin.

I_{DD3} and I_{DD4} are measured on the following condition that:
1. Set the all I/O pins to input mode.
2. Set CPU mode to <SLOW mode>.
3. Fix MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.

I_{DD5} is measured on the following condition that:
1. Set the all I/O pins to input mode.
2. Set CPU mode to <HALT1 mode>.
3. Fix MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.

I_{DD6} is measured on the following condition that:
1. Set the all I/O pins to input mode.
2. Set CPU mode to <LP1 mode>.
3. Fix MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.

I_{DD7} is measured on the following condition that:
1. Set the CPU mode to <STOP mode>.
2. Fix MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.
3. Open OSC1 pin.

*14 When bp2 of HANDSHAKE register (0x03F06) is set to “1'b1”

*15 When bp3 of FEWSPD register (0x03FBF) to “1'b1”

V_{DD5} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 RON							
C13	Input high voltage	V_{IH1}		$0.8V_{DD5}$		V_{DD5}	V
C14	Input low voltage	V_{IL1}		0		$0.2V_{DD5}$	
Input pin 2 ATRST, MMOD							
C15	Input high voltage	V_{IH2}		$0.8V_{DD5}$		V_{DD5}	V
C16	Input low voltage	V_{IL2}		0		$0.2V_{DD5}$	
C17	Input leakage current	I_{LK1}	V_{IN} = 0 V to V_{DD5}			± 2	μA
Input pin 3 DMOD							
C18	Input high voltage	V_{IH3}		$0.8V_{DD5}$		V_{DD5}	V
C19	Input low voltage	V_{IL3}		0		$0.2V_{DD5}$	
C20	Pull-up resistor	R_{RH1}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
Input pin 4 P27/NRST							
C21	Input high voltage	V_{IH4}		$0.8V_{DD5}$		V_{DD5}	V
C22	Input low voltage	V_{IL4}		0		$0.15V_{DD5}$	
C23	Pull-up resistor	R_{RH2}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
I/O pin 1 P00 to P07							
C24	Input high voltage	V_{IH5}		$0.8V_{DD5}$		V_{DD5}	V
C25	Input low voltage	V_{IL5}		0		$0.2V_{DD5}$	
C26	Input leakage current	I_{LK2}	V_{IN} = 0 V to V_{DD5}			± 2	μA
C27	Pull-up resistor	R_{RH3}	V_{DD5} = 5 V , V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C28	Pull-down resistor	R_{RL1}	V_{DD5} = 5 V , V_{IN} = V_{DD5} Pull-down resistor ON	10	50	100	

V_{DD5} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C29	Output high voltage	V_{OH1}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C30	Output low voltage 1	V_{OL1}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA LED output OFF			0.5	
C31	Output low voltage 2	V_{OL2}	V_{DD5} = 5.0 V, I_{OL} = 15.0 mA LED output ON			1.0	

V_{DD5} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 2 P20 to P24, P30 to P36, P61 to P67, P80 to P87, P92 to P95, PB0 to PB7							
C32	Input high voltage	V_{IH6}		$0.8V_{DD5}$		V_{DD5}	V
C33	Input low voltage	V_{IL6}		0		$0.2V_{DD5}$	
C34	Input leakage current	I_{LK3}	V_{IN} = 0 V to V_{DD5}			± 2	μA
C35	Pull-up resistor	R_{RH4}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C36	Output high voltage	V_{OH2}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C37	Output low voltage	V_{OL3}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA			0.5	
I/O pin 3 P10 to P16, P40 to P47, P50 to P57, P70 to P77							
C38	Input high voltage	V_{IH7}		$0.8V_{DD5}$		V_{DD5}	V
C39	Input low voltage	V_{IL7}		0		$0.2V_{DD5}$	
C40	Input leakage current	IL_{K4}	V_{IN} = 0 V to V_{DD5}			± 2	μA
C41	Pull-up resistor	R_{RH5}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C42	Pull-down resistor	R_{RL2}	V_{DD5} = 5 V, V_{IN} = V_{DD5} Pull-down resistor ON	10	50	100	
C43	Output high voltage	V_{OH3}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C44	Output low voltage	V_{OL4}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA			0.5	
I/O pin 4 PA0 to PA7							
C45	Input high voltage	V_{IH8}	*16	$0.8V_{DD5}$		V_{DD5}	V
C46	Input high voltage	V_{IH9}	*17	$0.54V_{DD5}$		V_{DD5}	
C47	Input low voltage	V_{IL8}		0		$0.2V_{DD5}$	
C48	Input leakage current	I_{LK5}	V_{IN} = 0 V to V_{DD5}			± 2	μA
C49	Pull-up resistor	R_{RH6}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C50	Output high voltage	V_{OH4}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C51	Output low voltage	V_{OL5}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA			0.5	

*16 When bp2 of SWCNT register (0x03E8F) is set to “1’b0”.

*17 When bp2 of SWCNT register (0x03E8F) is set to “1’b1”.

V_{DD5} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 5 P20, P21 (during used as ACZ)							
C52	Input high voltage 1	V_{DHH}	Figure:1.4.6	4.5			V
C53	Input high voltage 2	V_{DHL}		1.5			
C54	Input low voltage 1	V_{DLH}				3.5	
C55	Input low voltage 2	V_{DLL}				0.5	
C56	Input clamp current	I_{C1}	$V_{IN} > V_{DD5}$, $V_{IN} < 0$ V			±500	μA
Display output pin 1 COM0 to COM3, COM0A to COM3A (At V_{LC1}, V_{SS} voltage output)							
C57	Output impedance	Z_{OCOM1}	$V_{DD5} = V_{LC1}$ = 5.0 V Icom = 10 μA			0.6	V
Display output pin 2 SEG0 to SEG54 (At V_{LC1}, V_{SS} voltage output) *18							
C58	Output impedance	Z_{OSEG1}	$V_{DD5} = V_{LC1}$ = 5.0 V I_{seg} = 2 μA			0.6	V
Display power pin 1 VLC1, VLC2, VLC3							
C59	Internal dividing resistor	R_{VL1}	Ta = +25 °C (Impedance between VLC1 and VSS) *19	15	30	60	kΩ
C60		R_{VL2}		30	60	120	
C61		R_{VL3}		145	300	570	
C62		R_{VL4}		320	660	1260	

*18 COM0 to COM3 and COM0A to COM3A can be switched to general purpose ports individually.
(COM0A to COM3A are shared with SEG0 to SEG3)

*19 Total resistance of 3 resistors between VLC1 and VLC2, VLC2 and VLC3, VLC3 and VSS.

1.4.4 AC Characteristics

D. AC Characteristics

V_{DD5} = 5.0 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D. ACZ pin							
D1	Rising time	t_{rs}	Figure:1.4.6	30			µs
D2	Falling time	t_{fs}		30			

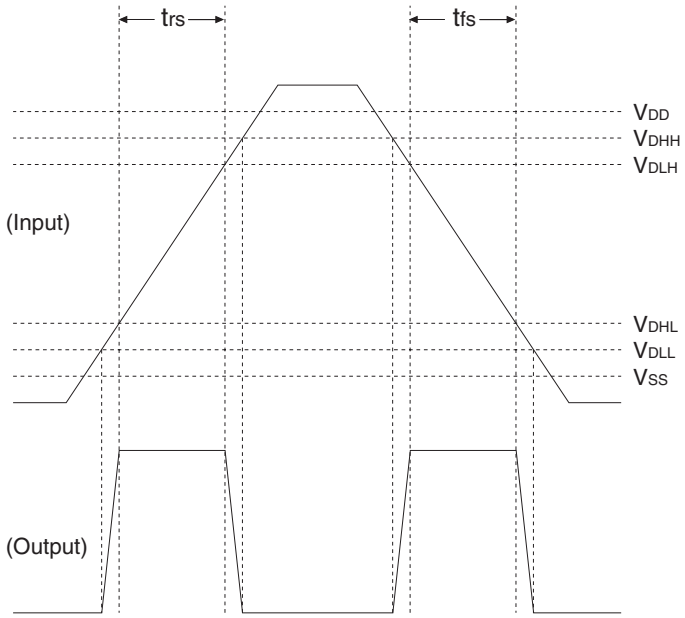

Figure:1.4.6 AC zero-volt detection circuit operation

1.4.5 A/D Converter Characteristics

E. A/D Converter Characteristics *20

V_{DD5} = 5.0 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
E1	Resolution					10	Bits
E2	Non-linearity error 1		V_{DD5} = 5.0 V, V_{SS} = 0 V V_{REF+} = 5.0 V T_{AD} = 800 ns			± 3	LSB
E3	Differential linearity error 1					± 3	
E4	Zero transition voltage		V_{DD5} = 5.0 V, V_{SS} = 0 V V_{REF+} = 5.0 V T_{AD} = 800 ns		10	30	mV
E5	Full-scale transition voltage			4970	4990		
E6	A/D conversion time		T_{AD} = 800 ns	12.93			µs
E7			fx = 32.768 kHz, T_{AD} = 15.26 µs	427.25			
E8	Sampling time		T_{AD} = 800 ns	1.6			
E9			fx = 32.768 kHz, T_{AD} = 15.26 µs	30.52			
E10	Reference voltage	V_{REF+}		1.8		V_{DD5}	V
E11	Analog input voltage			V_{SS}		V_{REF+}	
E12	Analog input leakage current		Channel OFF V_{ADIN} = V_{SS} to V_{DD5}			± 2	µA
E13	Reference voltage pin input leakage current		Ladder resistance OFF $V_{SS} \leq V_{REF+} \leq V_{DD5}$			± 5	
E14	Ladder resistance	R_{LADD}	V_{DD5} = 5.0 V	15	40	80	kΩ

*20 T_{AD} is A/D conversion clock cycle.
The values of E2 to E5 are guaranteed on the condition of V_{DD5} = V_{REF+} = 5 V, V_{SS} = 0 V.

1.4.6 Auto Reset Characteristics

F. Auto Reset Characteristics

$V_{DD5} = V_{RST}$ to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
F1	Operating supply voltage	V_{DD9}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
F2	Power detection level	V_{RST1}	At rising	1.90	2.20	2.45	V
F3	Power detection level	V_{RST2}	At falling	1.80	1.90	2.00	V
F4	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V
Consumption current							
F5	Auto reset power consumption	I_{DD8}	V_{DD5} = 5 V		1.5	3	μA

1.4.7 Power Supply Voltage Detection Circuit

G. Power Supply Voltage Detection Circuit

V_{DD5} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage detection level							
G1	Power supply voltage detection level 1-1	V_{LVI11}	At rising	3.8	4.0	4.2	V
G2	Power supply voltage detection level 1-2	V_{LVI12}	At falling	3.7	3.9	4.1	
G3	Power supply voltage detection level 2-1	V_{LVI21}	At rising	2.7	2.8	2.9	
G4	Power supply voltage detection level 2-2	V_{LVI22}	At falling	2.6	2.7	2.8	
G5	Minimum pulse width	T_W		20	60		µs
G6	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V
Consumption current							
G7	Consumption current in power supply voltage detection circuit	I_{DD16}	V_{DD5} = 5.0 V		2	4	µA

1.4.8 Internal Oscillation Circuit

H. Internal High-speed Oscillation Circuit

V_{DD5} = 2.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
H1	Internal high-speed oscillation circuit frequency	f_{rc16}		15.2	16	16.8	MHz

I. Internal Low-speed Oscillation Circuit

V_{DD5} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I1	Internal low-speed oscillation circuit frequency	f_{rcs}		29.2	32.5	35.8	kHz

1.4.9 Flash EEPROM Program Conditions

J. Flash EEPROM Program Conditions

V_{DD5} = 2.7 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
J1	Data retention period		Guaranteed programming times 1000 times	10			Year

1.5 Package Dimension

■ Package code: LQFP100-P-1414CUnit: mm

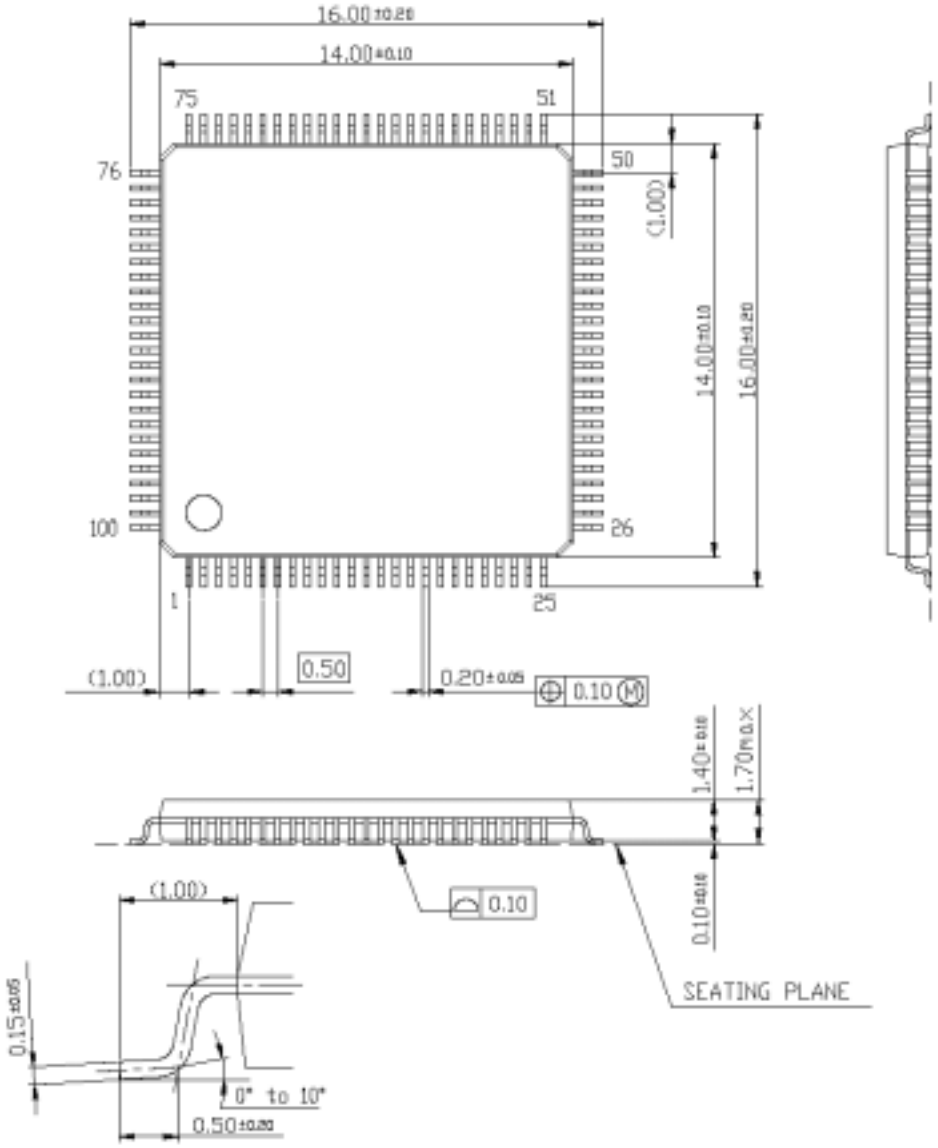

Figure:1.5.1 100-pin LQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

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Consult our sales staff in advance for information on the following applications:
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(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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