❑ MN1021617 / F1617

Type		**MN1021617 / F1617**
ROM (×8-Bit)		128 K / 128 K (Flash)
RAM (×8-Bit)		4 K / 4 K
Minimum Instruction Execution Time	With Main Clock operated	**MN1021617 : 50 ns (at 3.0 V to 3.6 V, 40 MHz)** **MN1021617 : 100 ns (at 2.0 V to 3.6 V, 20 MHz)** **MN102F1617 : 66.6 ns (at 2.7 V to 3.6 V, 30 MHz)**
Interrupts		• $\overline{\text{RST}}$ Pin • Watchdog • NMI Pin • Timer Counter 4 to15 • Timer Counter 16, 17, 21 • Timer Counter 16 to 20 Compare Capture A • Timer Counter 16 to 20 Compare Capture B • Timer Counter 21 Capture A • Timer Counter 21 Capture B • Timer Counter 21 Capture D • Timer Counter 21 Capture E • Timer Counter 21 Capture F • ATC ch 0 to 3 Transfer finish • External 0 to 7 • Serial ch 0 to 3 Transmission • Serial ch 0 to 3 Reception • $\overline{\text{KI}}$ Pin (OR) • A/D Conversion finish
Timer Counter		**Timer Counter 0 : 8-Bit × 1** (Prescalers) Clock Source 1/2 of System Clock, Timer Counter 1 Output **Timer Counter 1 : 8-Bit × 1** (Prescalers) Clock Source 1/2 of System Clock, Timer Counter 0 Output **Timer Counter 2 : 8-Bit × 1** (UART Baud Rate Generator) Clock Source 1/2 of System Clock, External Clock Input, Timer Counter 0 Output **Timer Counter 3 : 8-Bit × 1** (UART Baud Rate Generator) Clock Source 1/2 of System Clock, Timer Counter 0 Output **Timer Counter 4 : 8-Bit × 1** (Timer Output, A/D Conversion Start up) Clock Source 1/2 of System Clock, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source . Underflow of Timer Counter 4 **Timer Counter 5, 9 : 8-Bit × 1** (UART Baud Rate Generator) Clock Source 1/2 of System Clock, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 5, 9 **Timer Counter 6, 10, 11 : 8-Bit × 1** (Timer Output) Clock Source . 1/2 of System Clock, External Clock Input, Timer Counter 0 Output Interrupt Source . .Underflow of Timer Counter 6, 10, 11 **Timer Counter 7 : 8-Bit × 1** (Timer Output) Clock Source . .1/2 of System Clock, External Clock Input, Timer Counter 0 Output Interrupt Source Underflow of Timer Counter 7 **Timer Counter 8 : 8-Bit × 1** (Timer Output) Clock Source 1/2 of System Clock, External Clock Input, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 8 **Timer Counter 12 : 8-Bit × 1** (Timer Output) Clock Source . . 1/2 of System Clock, External Clock Input with Edge, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 12 **Timer Counter 13 : 8-Bit × 1** (Timer Output) Clock Source 1/2 of System Clock, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 13 **Timer Counter 14 : 8-Bit × 1** (Timer Output) Clock Source 1/2 of System Clock, External Clock Input with Edge, Timer Counter 0 Output Interrupt Source . . . .Underflow of Timer Counter 14

Timer Counter (Continue)

Timer Counter 15 : 8-Bit × 1 (Timer Output)
- Clock Source: 1/2 of System Clock, External Clock Input with Edge, Timer Counter 0 Output
- Interrupt Source: Underflow of Timer Counter 15

(Connectable) Timer Counter 0 to 3, 4 to 7, 8 to 11, 12 to 15

Timer Counter 16, 17 : 16-Bit × 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encorder Input)
- Clock Source: 1/2 of System Clock, External Clock Input (with Edge, Timer Counter 17 only), Timer Counter 0 Output, Timer Counter 1 Output (Timer Counter 16 only)
- Interrupt Source: Coincidence with Compare Capture A or at Capture; Coincidence with Compare Capture B or at Capture; Underflow of Timer Counter 16, 17

Timer Counter 18 : 16-Bit × 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encorder Input)
- Clock Source: 1/2 of System Clock, External Clock Input, Timer Counter 0 Output, Timer Counter 1 Output
- Interrupt Source: Coincidence with Compare Capture A or at Capture; Coincidence with Compare Capture B or at Capture; Underflow of Timer Counter 18, 19, 20

Timer Counter 19, 20 : 16-Bit × 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encorder Input)
- Clock Source ..: 1/2 of System Clock, Timer Counter 0 Output, Timer Counter 1 Output
- Interrupt Source ..: Coincidence with Compare Capture A or at Capture; Coincidence with Compare Capture B or at Capture; Underflow of Timer Counter 18, 19, 20

Timer Counter 21 : 24-Bit × 1 (Servo Control)
- Clock Source: 1/2 of System Clock, Timer Counter 1 Output
- Interrupt Source: When capturing to Capture A; When capturing to Capture B; When capturing to Capture D; When coinciding to Compare E; When coinciding to Compare F

Serial Interface

Serial 0, 1 : 8-Bit × 1 (Transfer direction of MSB / LSB selectable, Transmission / Reception of 7, 8-Bit length)
- Clock Source: 1/8 of Timer Counter 2, 1/8, 1/2 of Timer Counter 5, External Clock

Serial 2, 3 : 8-Bit × 1 (Transfer direction of MSB / LSB selectable, Transmission / Reception of 7, 8-Bit length)
- Clock Source: 1/8 of Timer Counter 3, 1/8, 1/2 of Timer Counter 9, External Clock

UART × 4 (Common use with Serial 0 to 3)
I^2C × 2 (Common use with Serial 1, 3, Single Master)

I/O Pins	**I/O**	**100**	• Common use 56 (Address Data Separate 8-Bit Mode) • Common use 73 (Address Data Multiplex 8-Bit Mode)
	Input	**8**	• Common use 8
A/D			10-Bit × 12ch (Maximum input is 16) (with S/H)
PWM			16-Bit × 5ch (Timer Counter 16 to 20)
ICR			16-Bit × 5ch, 24-Bit × 1ch (Timer Counter 16 to 21)
OCR			16-Bit × 5ch, 24-Bit × 1ch (Timer Counter 16 to 21)
Notes			Address / Data Multiplex Bus Interface, Address / Data Separate Bus Interface, 8-Bit / 16-Bit Bus Width selectable, DRAM Refresh Controller built-in
Package			LQFP128-P-1818C, FLGA165-C-1111

See the next page for support tool, pin assignment and electrical characteristics.

Electrical Characteristics

A/D Characteristics

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Non-Linear Error		10-Bit			±4	LSB
A/D Conversion Time		at 40 MHz	28			µs
Analog Input Voltage	VIA		VSS		VDD	V

(Ta = 25 °C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Supply Current

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Operating Supply Current	IDDopr	VI = VDD or VSS, Output release f = 40 MHz, VDD = 3.3 V			50	mA
Supply Current at STOP	IDDS	Pin with pull-up resistor is open All other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level			50	µA
Supply Current at HALT	IDDH	f = 40 MHz, VDD = 3.3 V Output release			25	mA

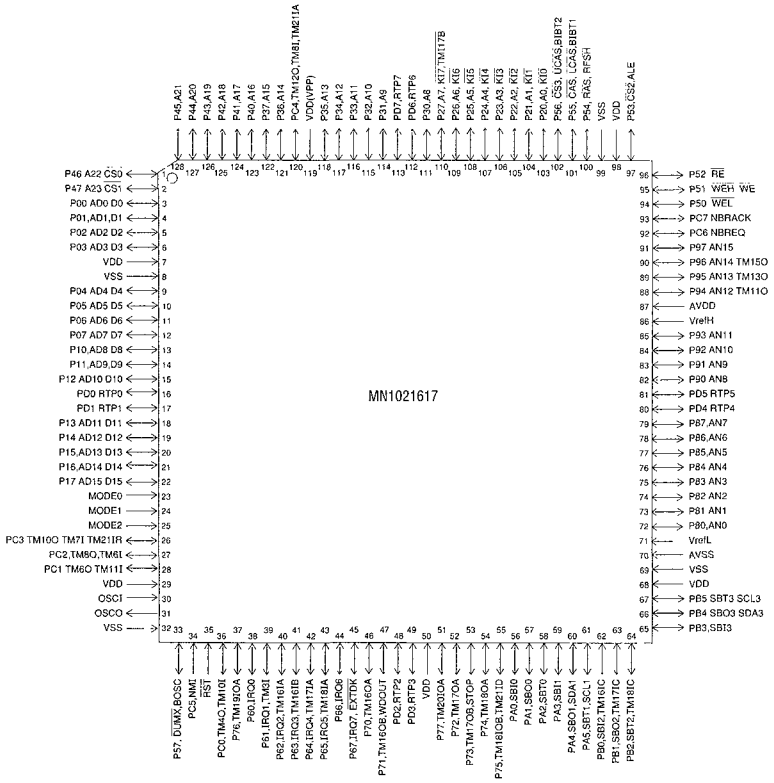
(Ta = –20 °C to + 70 °C, VDD = AVVD = 3.3 V, VSS = AVSS = 0 V)

Support Tool

In Circuit Emulator

PX-ICE102H1617

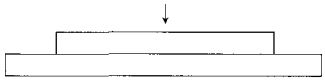
Pin Assignment



LQFP128-P-1818C

Pin Assignment (Continue)

Perspective



N.C.	N.C.	PB5,SBT3 SCL3	AVDD	P81,AN1	P83 AN3	P87,AN7	AVDD	P94,AN12, TM11O	AVDD	P50,/WEL	N.C.	N.C.	M
N.C.	N.C.	PB3,SBI3	VSS	VrefL	P85,AN5	PD5,RTP5	P93,AN11	P96 AN14 TM15O	PC6 NBREQ	P52,/RE	N.C.	N.C.	
VSS	PB2,SBT2, TM18IC	PB1,SBO2, TM17IC	PB4,SBO3, SDA3	P80,AN0	P84,AN4	AVSS	P91,AN9	P95,AN13, TM13O	PC7, NBRACK	P51,/WEH, /WE	VDD	P54,/RAS, /RFSH	L
PB0,SBI2 TM16IC	PA4,SBO1, SDA1	PA5,SBT1, SCL1	VDD	AVSS	P86,AN6	P90,AN8	P92,AN10	P97,AN15	VSS	P53,/CS2, ALE	P56,/CS3, /UCAS, BIBT2	VDD	K
PA1,SBO0	PA3,SBI1	PA0,SBI0	PA2,SBT0	AVSS	P82,AN2	PD4,RTP4	VrefH	P55,/CAS, /LCAS, BIBT1	VPP	P20,A0,/KI0	P21,A1,/KI1	P23,A3,/KI3	J
P75, TM18IOB, TM21ID	P73, TM17OB STOP	P77, TM20IOA	P72, TM17OA	P74, TM18OA	N.C.	N.C.	N.C.	P22,A2,/KI2	P26,A6,/KI6	P24,A4,/KI4	P27,A7,/KI7, TMI17B	P25,A5,/KI5	H
P71, TM16OB, WDOUT	PD3 RTP3	VDD	VDD	PD2,RTP2	N.C.	N.C.	N.C.	P30,A8	PD7 RTP7	VPP	P31 A9	PD6,RTP6	G
P65,IRQ5,TM 18IA	P67,IRQ7,/EX TDK	P66,IRQ6	P70,TM16OA	P64,IRQ4, TM17IA	N.C.	N.C.	N.C.	P34,A12	P32 A10	P33 A11	P35,A13	PC4,TM12O, TM8I, TM21IA	F
P63 IRQ3, TM16IB	P61,IRQ1 TM3I	P62,IRQ2 TM16IA	VDD	P60,IRQ0	MODE0	PD0,RTP0	P05,AD5 D5	P03,AD3,D3	P36,A14	VPP	P41,A17	P37,A15	E
VSS	P76, TM19IOA	PC0,TM4O, TM10I	VDD	PC2,TM8O, TM6I	P15,AD13, D13	P13,AD11, D11	P11,AD9,D9	VSS	P01,AD1 D1	P42,A18	P40,A16	VDD	D
/RST	P57,/DUMX, BOSC	PC5,NMI	OSCO	MODE2	P14,AD12, D12	VSS	P07,AD7,D7	VSS	P47,A23, /CS1	P44,A20	P45,A21	P43,A19	C
N.C.	N.C.	VSS	PC1 TM6O, TM11I	PC3,TM10O, TM7I, TM21IR	P16,AD14, D14	PD1,RTP1	P10,AD8,D8	VDD	P02,AD2,D2	P46,A22, /CS0	N.C.	N.C.	B
N.C.	N.C.	OSCI	VSS	MODE1	P17 AD15,D1 5	P12,AD10 D10	P06 AD6,D6	P04,AD4,D4	VDD	P00,AD0,D0	N.C.		A
13	12	11	10	9	8	7	6	5	4	3	2	1	

FLGA165-C-1111

MN1021617 / F1617

The MN102F1617 is manufactured and sold under license agreement with BULL CP8 Inc Note that MN102F1617 cannot be used as the IC card

* A1 has no electrode (pin)

* N D (not defined) has an electrode (pin) but not guaranteed for N C (not connected) Pay sufficient attention so as not to cause shorting with any other wiring on the user board

* VPP, VDD, VSS, AVDD and AVSS has multiple electrodes (pins) Electrodes having the same name are shorted internally